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DIAGNOSIS OF PHOSPHORUS MONOLAYER DOPING IN SILICON BASED ON NANOWIRE ELECTRICAL CHARACTERISATION

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ABSTRACT: The advent of high surface-to-volume ratio devices has necessitated a revised approach to parameter extraction and process evaluation in field-effect transistor (FET) technologies. In this work active doping concentrations are extracted from electrical analysis of Si nanowire devices with high surface-to-volume ratios. Nanowire resistance and Si resistivity are extracted, by first extracting and subtracting out contact resistance. Resistivity (ρ) is selected as the benchmark parameter to compare different doping processes with each other. The impact of nanowire diameter scaling to 10 nm and nanowire spacing scaling to <20 nm are extracted for monolayer doping and beam-line ion implantation. Despite introducing significant crystal damage, P beam-line ion implantation beats allydiphenylphosphine (ADP) P monolayer doping with an SiO_2 cap in terms of lower Si resistivity and higher dopant activation, with dependencies on nanowire width greater than on nanowire spacing. Limitations in ADP P monolayer doping with an SiO_2 cap are due to the

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difficulties of dopant incorporation, as it is based on in-diffusion and P atoms must overcome a potential barrier at the Si surface.

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I. INTRODUCTION

With logic devices in the fin field effect transistor (FinFET) era,[1,2,3,4] and heading towards the gate-all-around (GAA) nanowire architecture,[5,6,7] it is critical that novel material and process options consider high surface-to-volume thin-body structures for the diagnosis of their suitability for future technology applications. In these devices surfaces dominate, as there are proportionately more atoms bound-to or located close to the surface.

Doping processes have historically been characterised on planar Si substrates for a number of reasons, typically because these substrates were relevant to the technology and FET devices of the past, as well as being compatible with many material analysis methods, such as Secondary Ion Mass Spectrometry and Spreading Resistance Microscopy. Nowadays, with FinFET fins widths in the sub-10 nm regime and edging towards 5 nm, fabrication processes must now be evaluated with this in mind.

In these high surface-to-volume ratio structures, careful consideration must be made of surface integrity, surface etching, and roughness or gentleness of a particular process. Previously if some surface roughening occurred during processing this could practically be absorbed without significant impact on device or circuit performance. Times have changed, gentleness of a processing technique is now a key metric for GAA technologies. For example monolayer doping (MLD) has been proposed by several groups[8,9,10,11,12] as a novel alternative to conventional doping techniques, such as beam-line ion implantation and plasma doping, however if one examines the literature on MLD there is very little data or discussion referring to surface integrity or surface etching. This should be highlighted in future publications in the field.

Doping related issues that potentially hinder performance in conventional thin-body devices include the crystal damage introduced by ion implantation, lack of dopant conformality, and dramatic dopant trapping at the oxide interface in plasma doped processes.

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The state-of-the-art in semiconductor doping is beam-line ion implantation.[13,14,15] It is the industry standard because it can generate a single ion species with a single energy in an industrially friendly highly controlled fashion. Plasma doping[16,17,18,19] (PLAD) has the advantage of generating more conformal doping profiles than ion implantation but it causes damage to the target as ions strike. PLAD also has issues surrounding the surface quality post-dopant activation that require understanding of surface science to properly optimise. MLD is promising as it is surface-based, whereby organic molecules are covalently bonded to the semiconductor surface at relatively low processing temperatures.[20,21] A thermal treatment is then applied to diffuse dopant atoms into the semiconductor. One of the main advantages of MLD is that it is a low-temperature process, typically processing is done at room temperature or at temperatures in the order of 100-180 °C. In comparison, in-situ doped epitaxial growth[22,23] has a significant thermal budget, with temperatures in the order of 400-800 °C depending on what material is being grown, while the temperature required to prevent damage accumulation during ion implantation is in the range of 400 °C.[24,25] Furthermore MLD is a surface reaction based technique so should resolve these line-of-sight issues other doping approaches struggle with. Irrespective of the nanowire or fin shape and dimension, the molecules should bind to each surface. P is the most commonly applied dopant for n-type MLD,[26,27,28,29,30,31,32,33] with only a few of reports of As MLD in Si.[34,35]

Much of the MLD literature to date has been based on planar unpatterned substrates. There is now a pressing need to consider how suitable MLD can be for thin-body three-dimensional semiconductor devices with high surface-to-volume ratios. Furthermore a systematic benchmarking of MLD versus other processes such as ion implant is still lacking.

Another motivation for the work undertaken here centres around the use of nanowire resistors as a diagnostic tool for doping processes. One can extract active doping concentrations from electrical data analysis in nanowire devices with proper mask and device

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design. Of course there are well known metrology techniques to profile chemical concentrations such as Atom Probe Tomography[36,37] or active concentrations in cross-section by Scanning Spreading Resistance Microscopy,[38] however the approach presented here is an alternative and complimentary methodology.

Here we explore the concept of pitch scaling in nanowire devices. FinFET and GAA devices comprise of more than one parallel current channel, as there are multiple fins or nanowires running in parallel from source to drain. The next big push in device scaling will incorporate pitch or spacing scaling, and thus process evaluation must now also consider this aspect. Literature reports of MLD, or even ion implant, in nanowires are available, but typically on isolated lines. Having these features closer together (< 20 nm spacing) brings another set of physical and chemical challenges not considered before.

The International Technology Roadmap for Semiconductors (ITRS) [39] projections for FinFET and GAA devices are shown in Fig. 1. It is interesting to note that the fin or nanowire diameter doesn't scale dramatically, only going from 8 to 5 nm over 5 technology nodes. On the other hand fin or nanowire pitch scales from 42 to 10 nm in the same timeframe. Densely packed Si nanowires is the next big trend in device scaling, putting pressure on processing technologies where small gaps between features may cause issues and limitations.

In this work we electrically characterise Si nanowires with widths ranging from 10 to 300 nm, and with spacings ranging from 20 to 1000 nm. Nanowires are doped by ADP P MLD with an SiO_2 cap and benchmarked against beam-line P ion implantation. Through extensive electrical characterisation, total device resistance is extracted, and sub-components of total resistance are also determined, namely contact resistance ($R_{CONTACT}$) in order to assess nanowire resistance ($R_{NANOWIRE}$). Resistivity (ρ) is then determined, followed by active doping concentration based on well-established values for electron mobility in Si, which are used to benchmark competing processes against each other in this work, and also against

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values in literature. In conclusion the difficulties of doping thin-body Si devices, and problems associated with in-diffusion-based processes, will be analysed and discussed.

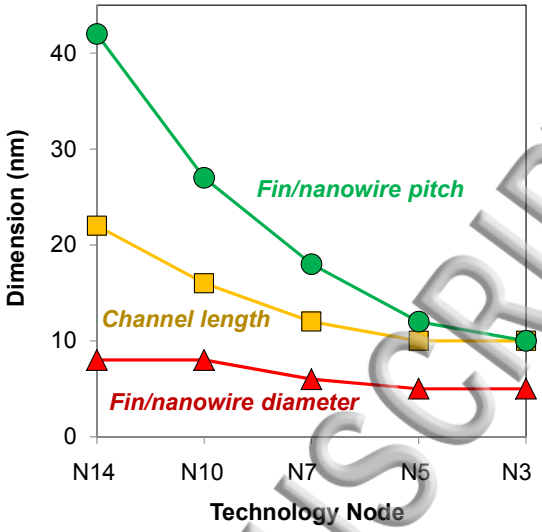


Figure 1 : ITRS 2.0 projections for multigate devices consisting of Si fins or nanowires. Pitch, channel length, and diameter are predicted to scale, with pitch scaling projected to undergo the largest change.

II. NANOWIRE DEVICE DESIGN

The devices under study to characterise the doping processes consist of a multi parallel nanowires to form a resistor structure shown in Fig. 2. This is a simple two pad test structure where current versus voltage characteristics are measured. The Si nanowire features are visible in the Scanning Electron Microscopy (SEM) image of Fig. 2(a). Either side are metal contact pads, which overlap the wider Si regions underneath. In this case the metals consist of a 10 nm Ti adhesion layer with a thicker 150 nm Au layer on top. In Fig 2(b) is a schematic of the Si portion of the test structure highlighting the variables in the device design on the mask layout. The nanowire width (W), length (L) and spacing (S) are all varied. In this way we can generate data required to extract $R_{CONTACT}$, $R_{NANOWIRE}$, and ultimately ρ.

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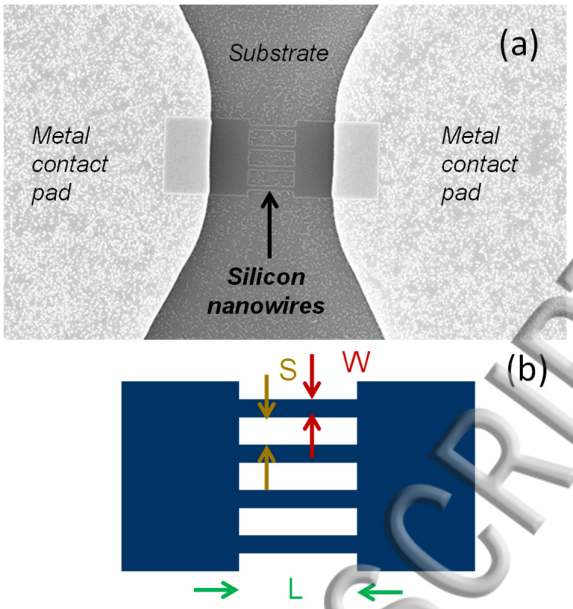


Figure 2 : (a) An SEM image zoomed into the Si nanowires, which are contacted by metal pads. (b) A schematic drawing of the 4-finger Si nanowire test structure, highlighting the variables width (W), length (L), and spacing (S).

Figure 3 helps explain the extraction methodology in more detail. Let us assume that the current flows uniformly throughout the cross-section of a nanowire, say like that of a metal track. From theory[40] we know that

$$R = \rho \frac{L}{A} = \rho \frac{L}{t.W} \quad (1)$$

where, A is cross-sectional area, t is thickness, with R, ρ, L, and W as defined previously. Measuring current versus voltage in the two pad test structure yields total resistance (R_{TOTAL}), and the total resistance path through the test structure is

$$R_{TOTAL} = 2R_{CONTACT} + \rho \frac{L}{t.W} \quad (2)$$

So by plotting R_{TOTAL} versus 1/W, $2R_{CONTACT}$ can be determined by the y-axis intercept at x=0, and thus removed from the equation, leaving behind just the resistance of the nanowires. Note of course when considering the cross-sectional area here, we must remember we have 4 nanowires in parallel. With everything else known, ρ can be extracted.

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$$R = \rho \frac{L}{A}$$

$$R = \frac{\rho}{t} \frac{L}{W}$$

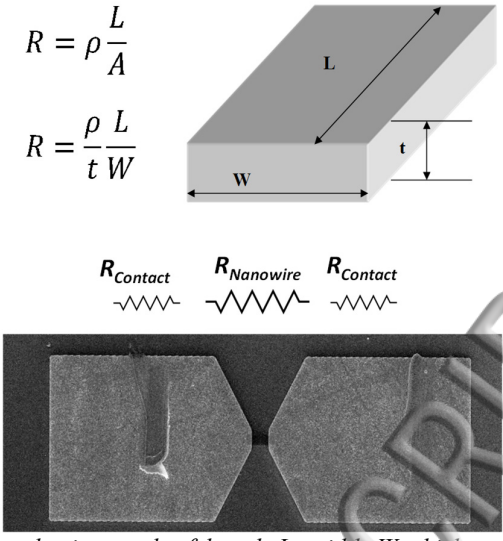


Figure 3 : A schematic of a conductive track of length L, width W, thickness t, along with the resistance components in the 2 contact pad test structure investigated in this work.

Moreover, once ρ is known we can use well established Si theory to extract a value for average active doping concentration in the nanowires. Most Si technology textbooks have a plot of ρ versus active carrier concentration which is partially reproduced in Fig. 4, for n-type Si.[41] The inset of Fig. 4 shows the dependence of electron mobility (μ) versus n-type active doping concentration (N). According to

$$\rho = \frac{1}{q.\mu.N} \qquad (3)$$

there is a strong dependence of ρ on μ and N. In summary once ρ is extracted experimentally, then we can use the graph in Fig. 4 to determine an average active doping concentration, N, throughout the nanowires, as a function of W, and S.

In order to familiarise ourselves with expected trends in R versus doping and W we carried out drift-diffusion based device simulations of nanowire resistors similar to those in the experimental sections. The simulations have been carried out in the same way of the electrical measurement, using the same dimensions and applied voltages. This is useful here because allows to have a preliminary idea of how the nanowire test structure should behave. Figure 5 shows the simulated data for R versus W and active doping concentration. In these

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idealised simulations non-idealities such as dopant trapping, quantisation effects, interface states, and Si bandgap variations versus W are not considered, as these would be the subject of a more detailed future modelling study. In Fig 5 it is clear R increases with decreased active doping concentration, and with decreased width due to the smaller current-carrying cross-sectional area.

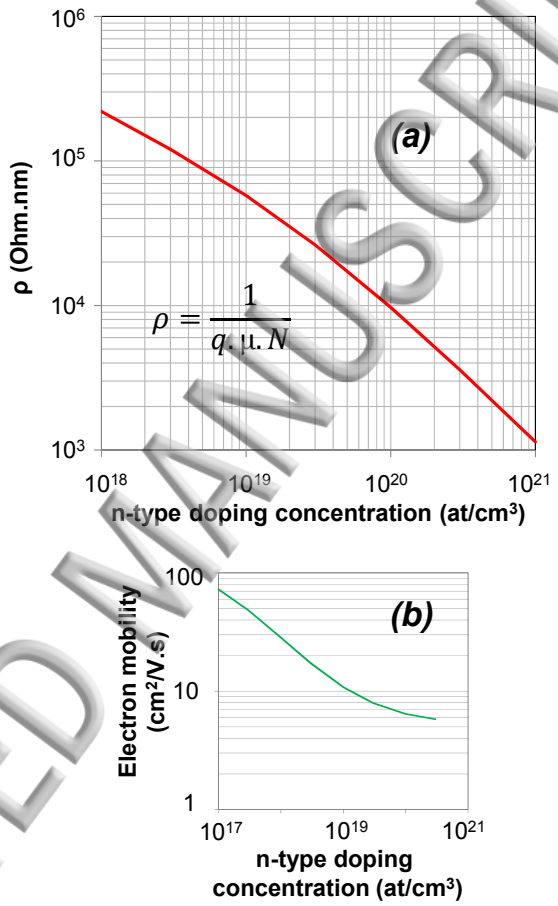


Figure 4 : (a) Si resistivity (ρ) as a function of n-type doping active concentration as derived from (b) standard Si theory for electron mobility.

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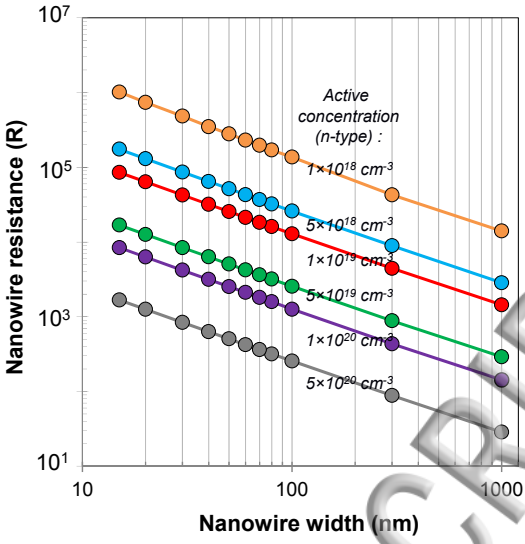


Figure 5 : Modelling results showing idealised trends of nanowire resistance (R) versus nanowire width. R increases with decreased active doping concentration, and with decreased width due to the smaller current-carrying cross-sectional area.

III. EXPERIMENTAL

There are two experimental sets presented in this work. In the first set we worked on short fat nanowire devices, fabricated from 30 nm thick Si-on-insulator (SOI) wafers, see Fig. 6 for the process flow. In that part the variables under study are the use of an RCA clean prior to MLD functionalisation, and the presence or absence of a capping SiO_2 layer during the drive-in rapid-thermal-anneal (RTA). In the second set of experiments tall nanowires were fabricated from 66 nm thick SOI wafers, see Fig. 11 for the process flow. There, pitch scaling is particularly interesting at the tall features form a "Manhattan skyline" type array, where it is envisaged that the narrow spaces combined with the tall features will make conformal doping difficult. ADP P MLD with an SiO_2 cap is benchmarked against a standard beam-line ion implant for P doping in that section.

Throughout this work nominally undoped (100) SOI substrates were used, with a Si thickness of 30 or 66 nm, and SiO_2 thickness of 145 nm. For nanowire processing the SOI substrates were patterned using the Raith VOYAGER electron beam lithography (EBL)

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system with a beam energy of 50 keV, and the high resolution EBL resist hydrogen silsesquioxane (HSQ, XR1541, 2%) from Dow Corning. The substrates were firstly degreased by ultra sonicating them in acetone and isopropyl alcohol (IPA) solvents. After drying the substrates HSQ resist has been spun at 4000 rpm to achieve 15 nm resist thickness. In another set, 6 nm thick layers have been prepared by diluting the resist to 1 %. Spin coating has been performed at 4500 rpm. The EBL exposure was a two-step process, namely a low current set-up pattern the high resolution nanowires structures, and in the second step, in a high current set-up, the contact pads were exposed. This was done to decrease the total exposure time while keeping the high resolution required for the nanowires. After the EBL exposures, the substrates were developed in NaCl (4%) and NaOH (1%) solutions for 4 min followed by 15 s rinse in de-ionised (DI) water and a second 15 s rinse in DI water in a second beaker.

The samples were etched in an Oxford Instruments System 100 ICP etcher operating in Reactive Ion Etch (RIE) mode. The etch chemistry was a Cl_2/N_2 gas mixture at flows of 20 and 40 sccm respectively with a process pressure of 10 mTorr and RF power of 80 W yielding a DC bias of 220 V. Sample temperature was controlled at 20 °C with Helium gas backside cooling with the sample mounted on a Si carrier wafer using Krytox® vacuum oil. Real time etch depth monitoring of the SOI film layer was achieved using an Intellemetrics LEP500 laser reflection system.

The P MLD process was then implemented on selected samples. To remove any physisorbed contaminants present on the samples a degreasing step was carried out. Thus, the samples were placed in acetone and ultra-sonicated for 2 minutes followed by an isopropyl alcohol dip and subsequent drying using a stream of nitrogen gas. A commonly used cleaning step in the semiconductor industry is the RCA clean. This involves immersion of a silicon sample in a solution containing a 5:1:1 ratio of DI water, ammonium hydroxide, and

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hydrogen peroxide at a temperature of 80 °C. This optional step was used in some studies to categorise whether it had a positive effect on MLD and to determine its usefulness for nanoscale nanowires. Removal of the native oxide layer from Si often requires quite harsh treatments involving hydrofluoric (HF) acid, which can etch away this layer to produce a hydrogen terminated surface. Native oxide removal occurred after degreasing or after an RCA clean in cases where it was applied. This hydrogen-terminated surface is prone to re-oxidation and was promptly placed into conditions where this was not possible, under N_2 on a Schlenk line.

A solution containing the chosen dopant molecule and solvent was then degassed using multiple freeze-pump-thaw cycles. N-type doping was carried out using allydiphenylphosphine (ADP) which provides P as the dopant molecule. Mesitylene was used as the solvent when carrying out MLD on oxide free Si. The degassed solution was cannulated into a round bottom flask containing the Si samples and set to reflux at 180 °C for 3 hours to enable functionalisation. Samples were then removed from the round bottom flask, ultra-sonicated in IPA for 1 minute and dried under a stream of nitrogen. In order to minimise oxidation of the now functionalised samples they were placed in gel-boxes and stored in a N_2 environment, either a glove-box or a sample preserver, awaiting thermal treatment. Once functionalised, samples required a thermal treatment to diffuse the target dopant atom into the crystalline Si and provide it with energy to activate through substitutional doping. A 50 nm sputtered SiO_2 capping layer was deposited on selected samples prior to RTA to prevent volatilisation of the dopant molecule. Samples were then treated with a 1050 °C 5 s RTA in N_2. Cap removal was initially carried out using a 5:1 Buffered Oxide Etch (BOE) solution, in which samples were immersed for 30 s.

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As a benchmark, some devices received a P 4×10^{15} cm^{-2} 3 keV 45° beam-line ion implant. This was done at room temperature, with half the dose from the left side of the nanowires, and half of the dose from the right side in the standard way.

A UV lithography based process was used to pattern the Ti/Au metal contact pads, based on a lift off technique. The steps are as follows; bake sample in Hexamethyldisilizane (HMDS) primer vapour oven at115 °C. spin on Micro Chem LOR3A lift-off resist at 3000 rpm for 50 s, hot-plate bake at 150 °C for 3 mins, spin on HMDS at 3000 rpm, spin on Micro Chem S1805 imaging resist at 3000 rpm, hot-plate bake at 115 °C for 2 min, align and expose in Karl Suss MA1006 aligner for 4.5 s, exposure dose = 45 mJ/cm^2, develop for 1 min in Microposit 319 developer, rinse in DI water for 1 min and blow dry with N_2, immerse in dilute HF (25:1) for 5 s and rinse in DI water and blow dry with N_2, load in Temescal FC2000 e-beam evaporator and pump system to $>5\times10^{-7}$ Torr, expose to Ar plasma for 20 s to improve metal to metal adhesion, evaporate Ti:Au (10:150 nm), lift-off resist and excess metal in Microposit R1165 resist remover at 90 °C for 1 hour, and finally rinse in DI water and blow dry with N_2.

Electrochemical Capacitance Voltage (ECV) profiling was also performed to determine active carrier concentration using dilute ammonium bifluoride as electrolyte. ECV profilers extract an error with every data point in the curve. For the data presented here the errors don't exceed 20 %. As doping concentration axes are plotted in log-scale, these errors are relatively small and do not affect the overall conclusions of this work. Cross-sectional Transmission Electron Microscopy (XTEM) was carried out using the JEOL 2100 HRTEM operated at 200 kV. Cross-section samples were prepared by focused ion beam etching using a FEI's Dual Beam Helios Nanolab system. For current versus voltage measurements the KEITHLEY 37100 and KEITHLEY 2602 were used.

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IV. RESULTS AND DISCUSSION

A. 30 NM TALL NANOWIRES; USE OF SIO_2 CAP AND RCA CLEAN

As stated previously the first set of experiments were performed on 30 nm tall nanowires. In this section, only ADP P MLD was evaluated in order to optimise the process before comparing it to beam-line ion implantation. The variables under study are the RCA clean step and the SiO_2 capping layer used during RTA. A schematic of the process flow is in Fig. 6, along with a representation of the ADP molecule used for P MLD.

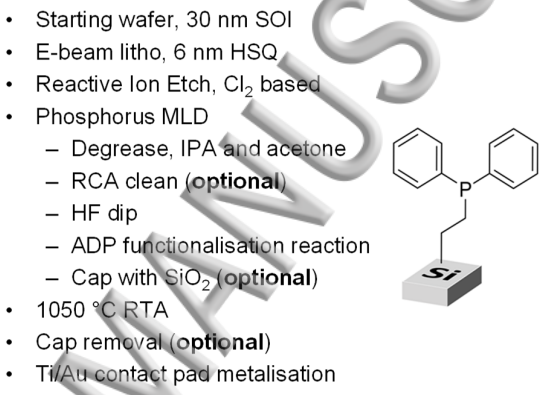


Figure 6 : Schematic representation of the ADP P MLD process flow on 30 nm tall devices. On the right hand side is a schematic of the ADP molecule bound to the Si surface.

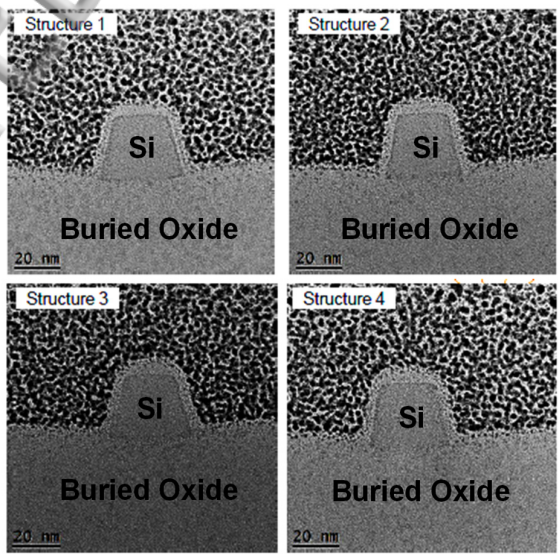


Figure 7 : Representative cross-sectional TEM images of the 30 nm tall Si nanowires after reactive ion etch. The four fingers within a single test structure are shown to demonstrate there is no significant difference between outer and inner nanowires in terms of cross-sectional shape.

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Figure 7 shows representative cross-sectional TEM images of the 30 nm tall nanowires fabricated from the 30 nm thick SOI substrates. In this case 6 nm HSQ resist was used to pattern the structures by e-beam lithography. Post RIE the four XTEM images in Fig. 7 show four nanowires from a single test structure, approximately 25 nm wide, where the nanowires were 1 μm apart. The sidewalls of the etched nanowires are quite smooth, with a slight taper, and the size and shape are quite reproducible within the test structure. In other words there is no significant difference in shape and size depending on whether we have an outer or inner wire in the set of four. Note there is a very thin native oxide around the outside of the nanowire due to exposure to the ambient.

In Fig. 8 are representative current versus voltage data from Si nanowire devices that were P MLD doped, as a function of nanowire W. Other device variables L and S were constant at 3000 nm and 1000 nm respectively. Current scales with W as expected, and forms a straight line through the origin. From this data R_{TOTAL} was extracted.

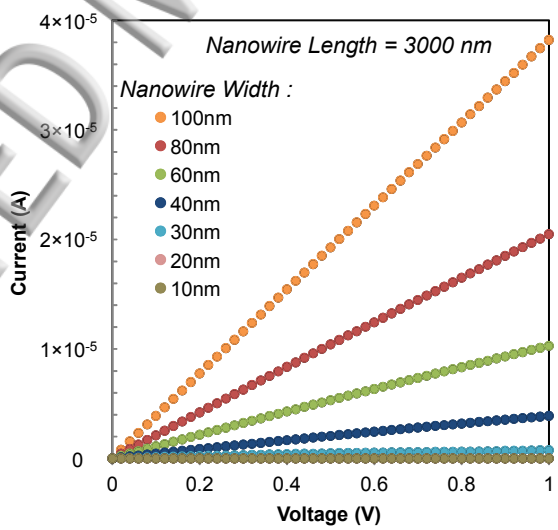


Figure 8 : Representative current versus voltage data from Si nanowire devices that were ADP P MLD doped, as a function of nanowire width. Length and spacing were constant at 3000 nm and 1000 nm respectively. Current scales with width as expected. From this data set, resistance was extracted.

Figure 9 shows the distribution of the number of devices within a R_{TOTAL} range. In Fig. 9(a) are the devices that had a SiO_2 cap during the RTA. Figure 9(b) shows the same

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type of plot but for the devices without the SiO_2 cap during the RTA, and it is observed that in that data there is a high count of devices in the R_{TOTAL} = 10^6-10^7 Ohm range. The RCA clean has little effect, if anything, it pushes the average R_{TOTAL} value higher. This was also noted in Fig. 9(a), and thus the RCA clean was dropped from future experiments.

Comparing the data with cap versus without cap gave an insight into the purpose of the SiO_2 cap. In Fig. 9(a) there is a bimodal R_{TOTAL} distribution and the lower R_{TOTAL} values in the 10^3-10^5 Ohm range look very promising, much better than those achieved without the SiO_2 cap. As a result it was concluded that capping is an important step to include for follow-on experiments. Furthermore in Fig. 9 we observed some very high R_{TOTAL} values (>10^{13} Ohm) corresponding to open circuits arising from broken nanowire devices. It was concluded that our original HF dip step for cap oxide removal prior to contact metal deposition was too harsh and was causing failure of some devices. An optimisation of this SiO_2 cap removal was undertaken and it will be seen in the next round of experiments to reduce the number of device failures seen here.

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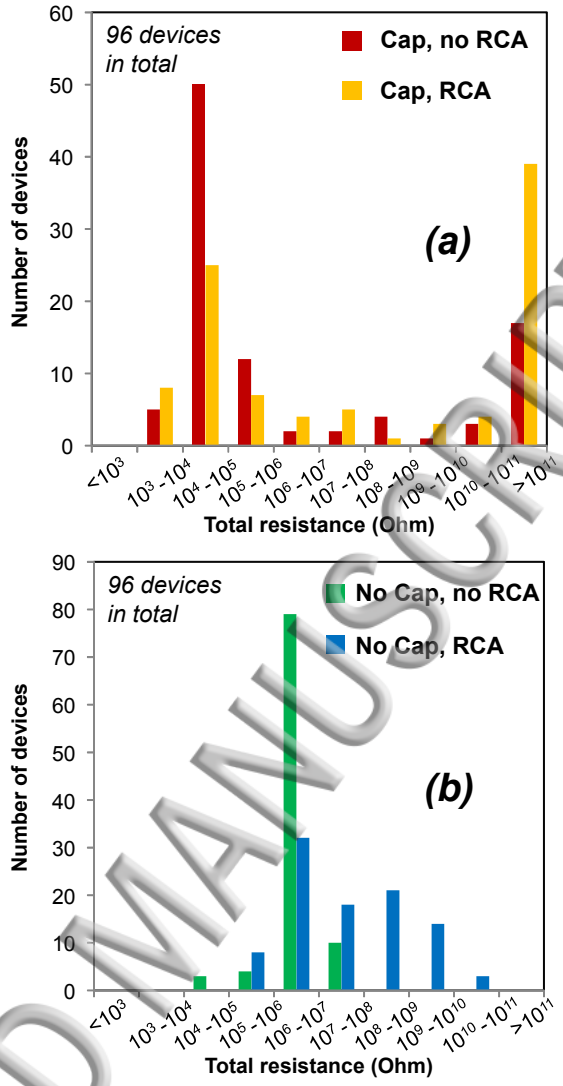


Figure 9 : Count (number of devices) versus total nanowire resistance in ADP P MLD nanowire devices. (a) Devices were capped during RTA. (b) Devices were not capped during RTA. The (lack of) effect of the RCA clean is also shown.

Of the four scenarios in this section the sample set that didn't have an RCA clean but did have an SiO_2 cap looked the most promising, thus we examined that data more closely. Plotted in Fig. 10 is R_{TOTAL} versus W for a fixed S (1 μm), and R_{TOTAL} versus S for a fixed W (60 nm). Note, due to the device loss, as shown in Fig. 9 it wasn't possible here to extract $R_{CONTACT}$ for this sample set, thus we're working with R_{TOTAL}, and not ρ, but this will be shown in the next section. From Fig. 10 we can conclude that R_{TOTAL} increases rapidly for W<50 nm, while remains relatively constant for S down to 20 nm. This independence of R

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relative to S may be due to the short nature of these devices. S scaling will be more difficult with taller features.

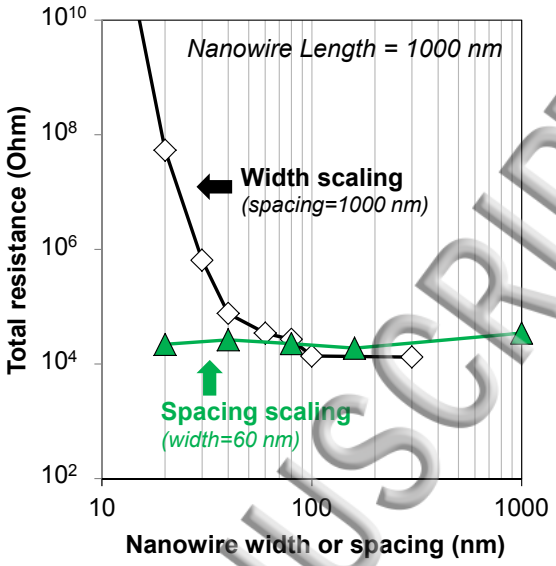


Figure 10 : Total resistance in the P MLD doped four finger nanowire test structure, 30 nm tall, as a function of W, with S fixed, and as a function of S with W fixed. These devices had a SiO_2 cap during RTA and had no RCA clean.

B. 66 NM TALL TIGHT-PITCH NANOWIRES; MLD VERSUS ION IMPLANT

In this part ADP P MLD with an SiO_2 cap and P ion implant are directly compared in terms of crystal damage, Si resistivity, W scaling, S scaling, and dopant activation. A schematic of the process flow is shown in Fig. 11. The lithography and patterning process was applied to 66 nm thick Si SOI in order to produce tall nanowire structures, suitable for evaluating whether MLD and ion implant can dope tall tight-pitch features with little inter-nanowire spacing. With the device trends towards tighter spacing and vertically stacked nanowires for GAA applications, doping processes must be tested on this type of test structure. In order to etch 66 nm tall nanowires, a thicker HSQ resist was used (15 nm). The RCA clean was dropped, and all devices had an SiO_2 cap during RTA. Due to the previous data showing device loss using a 5:1 BOE solution for cap removal, this part of the process was redesigned. The original 5:1 BOE solution was diluted further in a 5:1 ratio with DI,

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meaning we had a 25:1 strength BOE solution. A test piece of unpatterned Si with the SiO_2 cap was annealed side-by-side with the nanowire samples, and this was first subjected to the BOE based cap removal treatment. The sample was dipped into the solution and repeatedly checked for hydrophobicity, which is a sign the SiO_2 had been removed. The time was noted and this process was then repeated on the nanowire samples. Typically for 50 nm SiO_2 that had been annealed at 1050 °C, the 25:1 BOE solution was applied for 2 min.

The rest of the process was unchanged. As a benchmark, a set of devices were doped using a P 4×10^{15} cm^{-2} 3 keV 45° beam-line implant. This was done at room temperature, with half the dose from the left side of the nanowires, and half of the dose from the right side in the standard way.

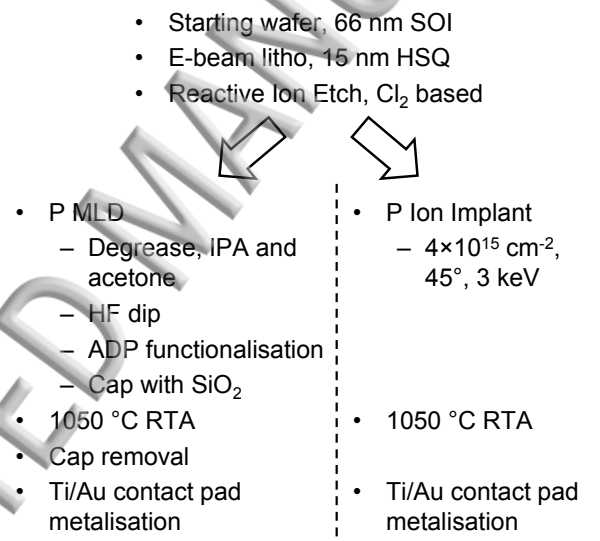


Figure 11 : Schematic representation of the ADP P MLD process flow on 66 nm tall devices, and of the P ion implant control process flow.

Figure 12 shows representative XTEM images of the test structures prior to doping. In Fig. 12(a) is an isolated Si nanowire which has smooth sidewalls that are slightly tapered. The bright region surrounding the Si is native oxide, seen before, due to ambient exposure. The underlying SiO_2 is slightly bloated on either side of the Si nanowire, but this is an XTEM imaging artefact, regularly seen in XTEM of SOI samples. This is also apparent in Fig 12(b)

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where the outer Si nanowires are leaning in towards the centre slightly. A wide view of Fig. 12(b) showed, under prolonged imaging than shown here, that the oxide on either side of the nanowires continued to bloat and expand upwards. This is possibly due to differences in self-heating of the different materials (e.g. SiO_2 versus Si) under electron irradiation. Regardless, in Fig 12(b) the closest features on the mask are shown, where the drawn spacing on the mask is 20 nm, but in practice, due to the tapered nature of the sidewalls, the spacing is <20 nm, approximately 12 nm at the foot of the nanowires. Note also that each individual nanowire in Fig. 12(b) looks like the others in that array, showing a good level of reproducibility. The outer and inner nanowires have practically the same size and shape. Finally, in Fig. 12(c) is the smallest resolved nanowire in this experiment which is 10 nm wide across the middle. Considering that the longest nanowires here are 3000 nm in length, the highest L:W aspect ratio in our nanowire devices is 300:1.

Figure 13 shows corresponding images to Fig. 12(b) but now after doping. Fig 13(a) shows tightly-packed tall nanowires after ion implant, and Fig. 13(b) shows tightly-packed tall nanowires after MLD. In both cases a 1050 °C RTA was applied to activate and/or drive-in the dopant. Note, although the XTEM image in the figure is zoomed into the inner structures for clarity, all four nanowires within each test structure showed the same trends.

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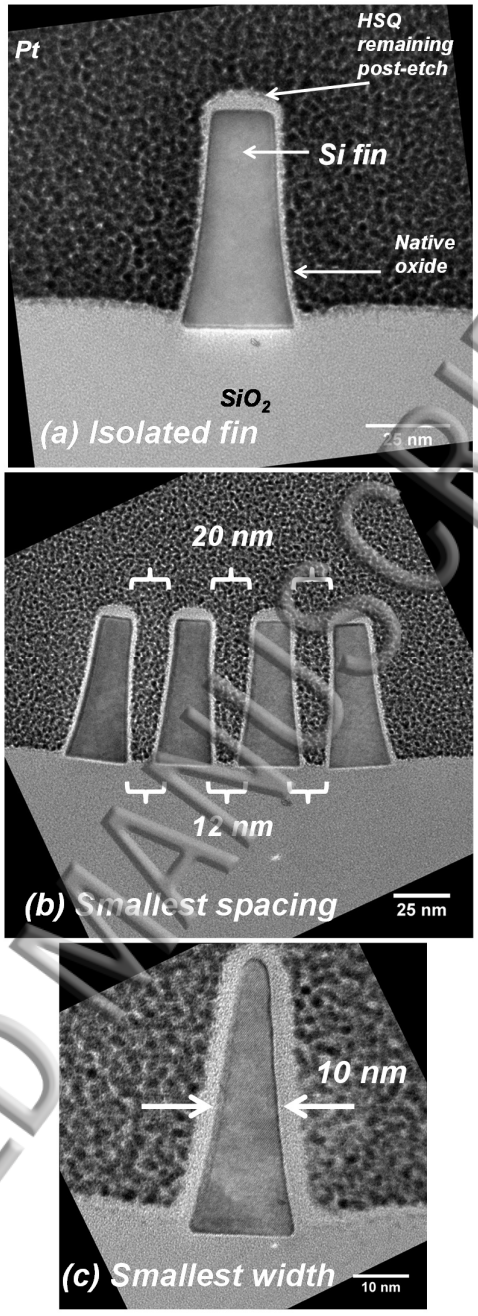


Figure 12 : Representative cross-sectional TEM images directly after etch, of the 66 nm tall So nanowire devices. (a) The isolated structures show smooth slightly tapered sidewalls. There is a small amount of HSQ resist remaining on the top of the nanowire and an approximately 1 nm thick native oxide on the sidewalls. (b)Four Si nanowires with a drawn spacing of 20 nm, resolved at the top of the features, which is 12 nm at the base of the structures. (c) The smallest feature resolved from the mask are 10 nm lines.

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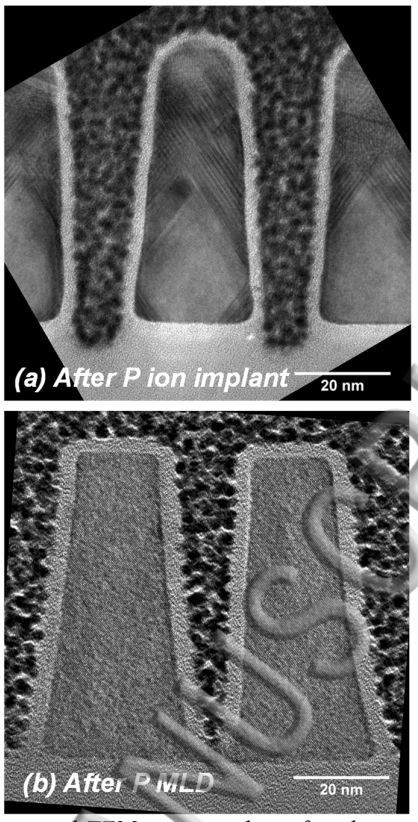


Figure 13 : Representative cross-sectional TEM images taken after doping of the Si nanowires, (a) shows the effect of P ion implantation performed at room temperature at 45° tilts left and right. The implant is partially amorphising, and the crystal has recrystallised during the RTA, but many crystal defects are evident. Note the tops of the nanowires are rounded due to sputter erosion during the ion implant. (b) On the other hand the ADP P MLD process is gentle, and there are no visible twin boundary type defects visible in the nanowires.

For the ion implantation case there is evidence of crystal damage. The tops of the nanowires have been partially eroded or sputtered by the implant. Also the characteristic amorphisation and recrystallisation type defects, such as {111} twin boundaries, are clearly visible. This is due to the well-known problems of thin-body Si recrystallisation, where the many surfaces and SiO_2-Si interfaces inhibit clean Si crystal recovery after amorphisation.[42,43,44,45] Evidently the P room temperature implant partially amorphised these structures. It is interesting to see the regions where twin boundaries exist in these structures. They appear well below half-way down the nanowires, despite the neighbouring nanowire shadowing the 45° beam-line implant to some degree. In fact it appears as if a significant amount of the 3 keV P implant has passed through the nanowire into the neighbouring nanowire. The projected range of a 3 keV P implant into Si is 6.7 nm.[46]

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For the MLD case in Fig. 13(b) there is no erosion and the body of the Si nanowire is free from visible crystal damage like {111} twin boundaries. The sidewalls of the nanowires look as smooth as before, indicating the gentleness of the ADP P MLD with an SiO_2 cap process here.

In this part of the experiment, with the improved SiO_2 cap removal process, we had better device yield and thus were able to proceed with $R_{CONTACT}$ extraction. Figure 14 shows a representative plot of R_{TOTAL} vs 1/W used to extract $R_{CONTACT}$ from the y-axis intercept at x=0. This example shows data for different L, to which linear fit lines were applied. From these $R_{CONTACT}$ was determined from the average y-axis intercept, in this case for P ion implant, to be 155 Ohm. From this data $R_{NANOWIRE}$ and ρ were calculated according to Equation 2.

Another electrical set of data of interest at this stage was the impact of S scaling. Figure 15 shows representative current versus voltage data from devices that were P ion implant doped, as a function of S, as drawn in the mask. L and W were constant at 1000 nm and 60 nm respectively. Current scales with spacing, due to shadowing effects during the implant. The current starts to saturate at the higher voltages here, this is thought to be related to the high current densities (>1 mA) through these devices, due to the small cross-sectional areas.

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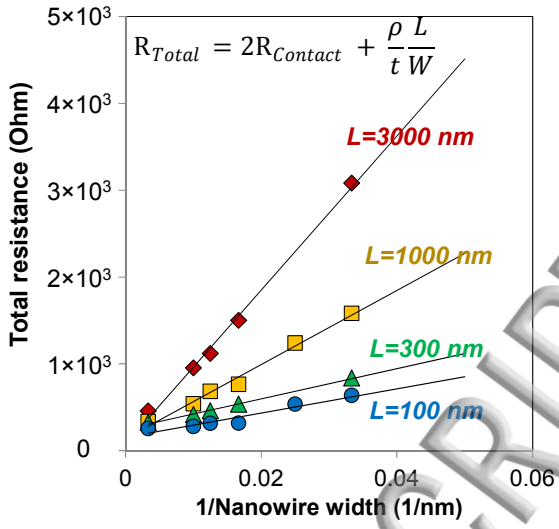


Figure 14 : Total nanowire resistance versus 1/W, which is used to extract contact resistance. This is a representative plot showing data grouped according to nanowire L. In this case process is P ion implant and the $R_{CONTACT}$ is 155 Ohm.

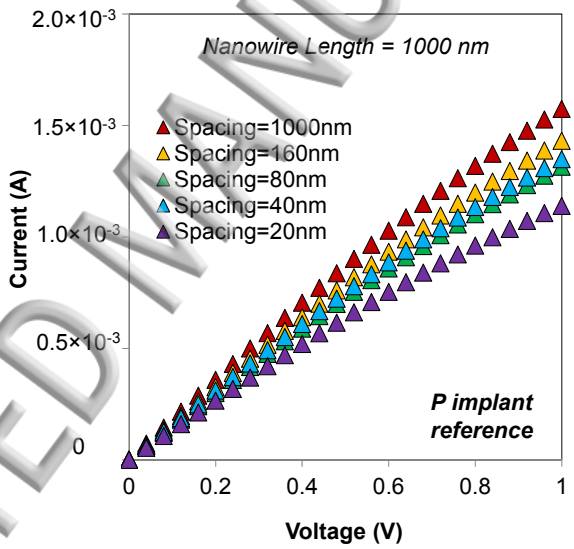


Figure 15 : Representative current versus voltage data from Si nanowire devices that were P ion implant doped, as a function of nanowire spacing (as drawn in the mask). Length and width were constant at 1000 nm and 60 nm respectively. Current scales with spacing, presumably due to shadowing effects.

After $R_{CONTACT}$ is subtracted out,

$$R_{NANOWIRE} = \rho \frac{L}{t.W} \quad (4)$$

and ρ is calculated based on L, W, and t=66 nm. This data is shown in Fig. 16 for both ADP P MLD and P ion implant, versus W scaling and versus S scaling. Furthermore active

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concentration was calculated from ρ according to Equation 3, and is plotted in Fig. 16 as horizontal lines of constant active concentration (N). Once again this assumes a constant active doping concentration within the nanowire, or could be thought of the "average" active doping concentration.

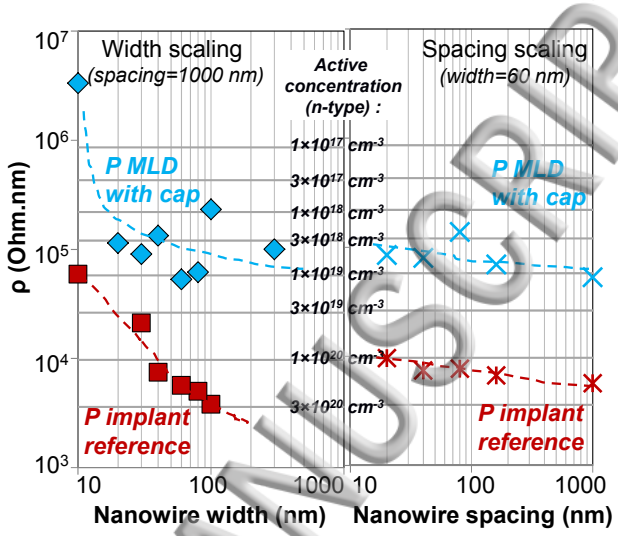


Figure 16 : Resistivity (ρ) in the ADP P MLD and P ion implanted doped four finger nanowire test structures, 66 nm tall, as a function of W with S fixed, and as a function of S with W fixed. The horizontal lines represent active concentration isolines associated with ρ as calculated using the Si mobility values in Fig. 4, assuming a uniformly doped nanowire. ADP P MLD with an SiO_2 cap reaches approximately 10^{19} cm^{-3}, while ion implant beats 2×10^{20} cm^{-3}.

Firstly focussing on the comparison of MLD versus ion implant it is clear that ADP P MLD with an SiO_2 cap does not beat the P ion implant reference in terms of ρ and N. For ion implant N >10^{20} cm^{-3} while for MLD it is close to 10^{19} cm^{-3}.

Examining the trends of ρ versus S, it seems neither doping method has a strong dependence of S scaling down to 20 nm. Note in the XTEM shown earlier S is practically <20 nm due to the tapered sidewall on the nanowires, but for the sake of consistency we refer to the dimensions on the mask in Fig. 16 and in the discussion here. There is 0.5× reduction in average carrier concentration going from S = 1000 nm to S = 20 nm. In comparison average carrier concentration drops orders of magnitude with similar W scaling.

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The S dependence of ρ is a consequence to two different effects for the two doping techniques. For the ion implant, shadowing will become a bigger problem for 45° tilt implants when the features are brought closer together. Even though there is some evidence that the 3 keV implant is partially passing through these structures, a 0.5× reduction in average carrier concentration is significant, but not an insurmountable problem. For MLD, the wet chemistry based technique may encounter surface coverage issues related to wettability in tight spaces. Conventional MLD is a wet-chemistry process, essentially where a liquid comes in contact with the semiconductor surface. As nanowire device pitches are scaled, the issue becomes whether the liquids involved can invade such tight spaces between fins and nanowires. There comes a point where pitches and spaces are just too small for wet chemistry.

The W dependence of ρ in Fig. 16 is far more significant. In the ADP P MLD with an SiO_2 cap case ρ and average carrier concentration stay relatively constant until W= 20 nm then degrade. The first part is due to the gentle nature of MLD, avoiding crystal damage which would be strongly influenced by W, and the second part is possibly due to the increased surface-to-volume ratio, which will be discussed further later in terms of an energy barrier at the SiO_2-Si interface limiting P in-diffusion. In the ion implant case, ρ and average carrier concentration degrade consistently versus W, which is linked to worsening crystal quality as a function of W with partially amorphising implants.[47] It is noteworthy to see the different ρ versus W trends for MLD and ion implant highlighting the resulting difference in crystal quality.

At this point it's important to compare these values of ρ against those reported for Si:P epi layers with and without a laser anneal treatment. Rosseel et al. reported ρ in the range of 0.6 mOhm.cm (=6×10^3 Ohm.nm) for Si:P epi, and ρ in the range of 0.3 mOhm.cm (=3×10^3 Ohm.nm) for Si:P epi with laser anneal.[22] It is difficult to compare directly with our

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data in Fig. 16, as we don't know the W in those Si:P epi structures, but the ion implanted data here is in the same order of that Si:P epi data.

To verify the extraction of average carrier concentration via analysis of nanowire electrical characterisation, control unpatterned bulk Si samples were doped in the same way as the nanowire devices, and Electrochemical Capacitance Voltage (ECV) carrier profiling was used to extract carrier concentration versus depth. Figure 17 shows indicative active concentration versus depth plots in bulk Si. For the P implant the peak of the profile is approximately 3×10^{20} cm^{-3} while for ADP P MLD it is 2×10^{19} cm^{-3}, comparable with the extracted values for N in the wide nanowires, verifying the electrical analysis.

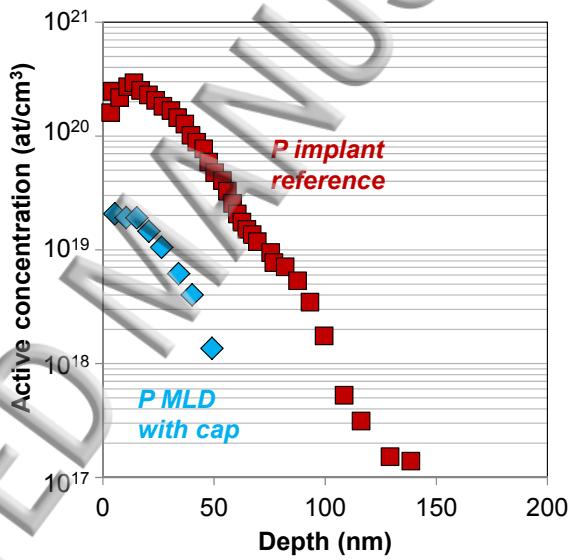


Figure 17 : Carrier concentration profiles versus depth into the Si determined by ECV analysis on bulk Si for ADP P MLD and P ion implant. These samples were processed in conjunction with the nanowire devices.

C. DIFFICULTIES FOR PHOSPHORUS IN-DIFFUSION

The problems of doping Si by MLD, or by ion implant, are manifold. The first problem occurs ever before we can consider activation issues or producing substitutional impurities in the Si lattice. The issues with doping semiconductors can usually be simplified into two sub-problems, namely (a) how to incorporate the dopant into the target, and (b) how

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to activate the incorporated dopant? The first big problem for MLD is related to how do we get the dopant impurity into the target to begin with. This is easier, but not trivial, for ion implant,[48] as we can relatively easily fire ions into a fin or nanowire target with a well-controlled energy, dose, and position. MLD on the other hand is based on placing organic molecules containing dopant atoms on the surface, covalently bound, and thereafter in-diffusing the dopant into the target. The apparent problem is that there is an energy barrier at the SiO_2-Si interface for P incorporation, shown schematically in Fig. 18(a). P atoms sitting at that interface have to climb over a barrier to enter the Si, from there they can diffuse around during the RTA. The evidence of this potential barrier comes from the relatively low P incorporation (~10^{19} cm^{-3}) when the equilibrium solid solubility of P in Si at 1050 °C is >10^{20} cm^{-3}.[49,50] Something must be preventing the P incorporation. It should be noted that several groups worldwide who have worked on P MLD on Si have also reported sub equilibrium solid solubility concentrations of incorporated P.[26-33]

So what's wrong? What is causing this energy barrier at the surface? One possibility is the P supply is not sufficient, as one monolayer of ADP molecule, based on its footprint and expected packing density, should yield a P dose of 2×10^{14} cm^{-2}, but we are incorporating only approximately 5×10^{13} cm^{-2} so that is unlikely to be the root of the problem. If we create multilayer doping, rather than monolayer doping, that could increase the P supply of course. On the other hand, we could consider the SiO_2-Si interface to be a trapping site for dopant atoms and thus produce an energy barrier for dopant release into the Si substrate. It's quite conceivable for trap sites to have a lower energy level to other energy levels surrounding them, as depicted in Fig. 18(a). Conversely a P atom already within the Si substrate could be trapped at the interface while diffusing around, such as is the case of uphill diffusion shown schematically in Fig. 18(b). Uphill diffusion was reported for P in Si,[51,52] as well as for B and As,[53,54,55] where there was an apparent shift of dopant profiles towards the surface during

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certain thermal treatments, leading to dopants moving towards regions of high concentration. The very concept of diffusion that something should move from a region of high concentration to a region of low concentration is a fairly fundamental principle, and the observation of the opposite trend is rather counter-intuitive. Nevertheless there have been many reports of uphill diffusion, or diffusion against the concentration gradient. The commonly-held physical explanation of that was linked to impurity trapping at the SiO_2-Si interface.[56,57]

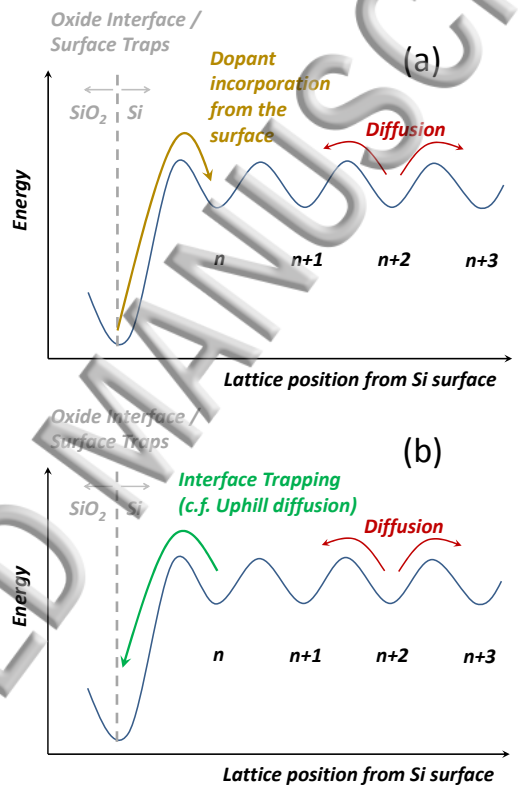


Figure 18 : (a) A schematic of the energy barriers to P in-diffusion from the surface into the Si substrate. (b) An equivalent schematic of the energy barriers for interface trapping of P, already in the Si substrate, which is evident during the uphill diffusion phenomenon.

Two further interesting points to note at this stage, firstly that in the area of gas-phase doping, in general P incorporation from phosphine has produced lower dopant concentrations, in the 10^{19} cm^{-3} range[58,59,60] compared to the equivalent experiments on As incorporation from arsine, which has produced dopant concentrations in the 10^{20} cm^{-3} range.[61,62] Secondly, Perego et al. have explored P in-situ doped Si nanocrystals with

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diameters in the order of 4 nm, [63] and have shown that P tends to be confined within Si at these dimensions, rather than go into SiO_2. The surface-to-volume ratios of 4 nm diameter nanocrystals will be extremely high, much greater than in the devices tested here. Furthermore, the ex-situ doping problem in our system, we have a significant amount of surface C present as a by-product of the ADP MLD process. It is possible it is this surface C is also playing a significant role here.

In essence any proposed ex-situ in-diffusion based process will have to overcome a surface barrier. Physically what is generating this, or creating interface traps, is open to debate. For sure the Si lattice is imperfect in that final monolayer before the surface, and is full of irregular coordinations and bonds of unusual angles and length.[64] Add to that the presence of C from the organic molecules used in MLD, which is a by-product of the process, may contribute to the inhibition of P uptake by the Si. It is clear there is some distance for ADP P MLD with an SiO_2 cap concentrations to reach 10^{20} cm^{-3}, although work is underway exploring alternative MLD methodologies at present. There are many potential ways to optimise the MLD procedure, ranging from molecule design, surface preparation methods, choice of capping layers, alteration of the thermal treatment strategy. For example gas-phase monolayer doping (GP-MLD),[65] monolayer contact doping (MLCD),[66,67] and remote-monolayer doping (R-MLD) [68] are just a few alternatives routes to potentially improve the P retention rate within Si nanostructures. The very fact that new and novel approaches are regularly being reported in the literature in this field proves that the area is dynamic, and that new and inventive approaches are constantly being demonstrated.

D. DIFFICULTIES DOPING SUB-10 NM SILICON

While MLD faces specific problems, all forms of doping technologies face similar challenges as we head towards GAA devices with 5 nm Si dimensions. At these scales other

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issues kick in which will need innovative solutions if conventional doping is to continue to be based on substitutional impurities in the Si crystal.

Firstly the bandgap of Si increases with scaled dimensions[69] and the ionisation energy for common dopants increases,[70] effectively decreasing doping efficiency,[71] even if the dopant atoms are substitutional. Hiller and König et al. have experimentally demonstrated difficulties doping Si nanocrystals with diameters in the order of 5 nm and below.[72,73,74] Furthermore, dopant trapping[75] at surfaces will increase with the ever-increasing surface-to-volume ratios, as proportionately more atoms in the target will be surface atoms, or bound to surface atoms. Next, nearby dielectric further increases ionisation energy due to screening[76] while electrically active interface states[77] will deplete a higher percentage of the Si structure, again due to the higher surface-to-volume ratios.

Innovative thinking will be needed to counteract these issues.

V. CONCLUSIONS

Regardless of doping process, electrical characterisation of nanowire devices is essential for proper diagnosis of any process proposed for GAA nanowire technologies. We have gone beyond the era of planar FET devices, and thus characterisation must also go beyond planar techniques and embrace non-planar type analysis. With the move towards dense pitches and tight spaced features, this aspect must also be incorporated into future works of this kind. When we are working on 5 nm Si structures, any surface etching will be amplified by the high surface-to-volume ratios, which would be a killer for devices.

In terms of evaluating ADP P MLD with an SiO_2 cap in Si against other doping techniques we must be realistic in terms of where it can or cannot offer solutions. It is challenging for ADP MLD with an SiO_2 cap to compete with ion implant or plasma doping,

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as the latter two can super-saturate the Si target, meaning millisecond type anneals[78,79] can generate above-equilibrium levels of dopant activation.[80] As an in-diffusion based technique MLD needs to overcome the equilibrium solubility limit in the target material, and work is progressing in the field in this regard. On the other hand MLD has been shown to be an extremely gentle process maintaining Si integrity both in terms of the internal crystal quality as well as external surface smoothness making it suitable for high surface-to-volume ratio type devices. Furthermore it is compatible with tight-pitch features, as it doesn't rely on the deposition of a thin-film layer, showing a relatively low ρ degradation with scaled spacings in this work.

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REFERENCES

[1] M. J. H. Van Dal, N. Collaert, G. Doornbos, G. Vellianitis, G. Curatola, B. J. Pawlak, R. Duffy, C. Jonville, B. Degroote, E. Altamirano, E. Kunnen, M. Demand, S. Beckx, T. Vandeweyer, C. Delvaux, F. Leys, A. Hikavyy, R. Rooyackers, M. Kaiser, R. G. R. Weemaes, S. Biesemans, M. Jurczak, K. Anil, L. Witters, R. J. P. Lander, 2007 Digest of Technical Papers - Symposium on VLSI Technology, 110 (2007).

[2] M. J. H. van Dal, G. Vellianitis, G. Doornbos, B. Duriez, T. M. Shen, C. C. Wu, R. Oxland, K. Bhuwalka, M. Holland, T. L. Lee, C. Wann, C. H. Hsieh, B. H. Lee, K. M. Yin, Z. Q. Wu, M. Passlack, and C. H. Diaz, Proc. IEEE Int. Electron Devices Meeting 2012, 521 (2012).

[3] A. Veloso, G. Hellings, M. J. Cho, E. Simoen, K. Devriendt, V. Paraschiv, E. Vecchio, Z. Tao, J. J. Versluijs, L. Souriau, H. Dekkers, S. Brus, J. Geypen, P. Lagrain, H. Bender, G. Eneman, P. Matagne, A. De Keersgieter, W. Fang, N. Collaert, and A. Thean, 2015 Symposium on VLSI Technology Digest of Technical Papers, T138 (2015).

[4] A. Veloso, A. De Keersgieter, P. Matagne, N. Horiguchi, N. Collaert, Materials Science in Semiconductor Processing 62, 2 (2017).

[5] N. Singh, A. Agarwal, L. K. Bera, T. Y. Liow, R. Yang, S. C. Rustagi, C. H. Tung, R. Kumar, G. Q. Lo, N. Balasubramanian, D. -L. Kwong, IEEE El. Dev. Lett. 27, 383 (2006).

[6] R. Gandhi, Z. Chen, N. Singh, K. Banerjee, S. Lee, IEEE El. Dev. Lett., 32, 1504 (2011).

[7] K. J. Kuhn, IEEE Trans. El. Dev. 59, 1813 (2012).

[8] J. C. Ho, R. Yerushalmi, Z. A. Jacobson, Z. Fan, R. L. Alley, and A. Javey, Nature Materials 7, 62 (2008).

[9] J. C. Ho, R. Yerushalmi, G. Smith, P. Majhi, J. Bennett, J. Halim, V. N. Faifer, and A. Javey, Nanoletters 9, 725 (2009).

[10] W. P. Voorthuijzen, M. D. Yilmaz, W. J. M. Naber, J. Huskens, W. G. van der Wiel, Adv. Mater. 23, 1346 (2011).

[11] K.-W. Ang, J. Barnett, W. –Y. Loh, J. Huang, B. –G. Min, P. Y. Hung, I. Ok, J. H. Yum, G. Bersuker, M. Rodgers, Proc. IEEE Int. Electron Devices Meeting 2011, 35.5.1 (2011).

[12] B. Long, G. Alessio Verni, J. O'Connell, J. Holmes, M. Shayesteh, D. O'Connell, R. Duffy, Proc. 20th International Conference on Ion Implantation Technology (IIT), pp 1–4 (2014).

[13] A. Renau, ECS Transactions 35, 173 (2011).

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This manuscript was accepted by J. Appl. Phys. Click here to see the version of record.

[14] M. I. Current, Industrial Accelerators and their Applications, pp. 9-56. (2012) DOI: 10.1142/9789814307055_0001

[15] B. Colombeau, B. Guo, H. -J.Gossmann, F. Khaja, N. Pradhan, A. Waite, K. V. Rao, C. Thomidis, K. -H.Shim, T. Henry, N. Variam, Physica Status Solidi (A) Applications and Materials Science 211,101 (2014).

[16] C. -N. Ni, , K. V. Rao, F. Khaja, S. Sharma, S. Tang, J. J. Chen, K. E. Hollar, N. Breil, X. Li, M. Jin, C. Lazik, J. Lee, H. Maynard, N. Variam, A. J. Mayur, S. Kim, H. Chung, M. Chudzik, R. Hung, N. Yoshida, N. Kim, Digest of Technical Papers - Symposium on VLSI Technology 2016, art. no. 7573383 (2016).

[17] P. K. Chu, S. Qin, C. Chan, N.W. Cheung, L.A. Larson, Materials Science & Engineering, R17, 207 (1996).

[18] Y. Sasaki, K. Okashita, B. Mizuo, M. Kubota, M. Ogura and O. Nishijima J. Appl. Phys. 111, 013712 (2012).

[19] B. H. Kim, S. M. Park, S. W. Park, Y. B. Park, H. J. Kim and C. G. Park, Appl. Phys. Lett. 101, 213113 (2012).

[20] L. Ye, A. González-Campo, T. Kudernac, R. Núñez, M. de Jong, W. G. van der Wiel, J. Huskens, Langmuir 33, 3635 (2017).

[21] B. Long, G. Alessio Verni, J. O'Connell, M. Shayesteh, A. Gangnaik, Y. M. Georgiev, P. Carolan, D. O'Connell, K. J. Kuhn, S. B. Clendenning, R. Nagle, R. Duffy, J. D. Holmes, Mater. Sci. Semicond. Process. 62, 196 (2017).

[22] E. Rosseel, H.B. Profijt, A. Hikavyy, J. Tolle, S. Kubicek, G. Mannaert, C. L'abbé, K. Wostyn, N. Horiguchi, T. Clarysse, B. Parmentier, S. Dhayalan, H. Bender, J.W. Maes, S. Mehta, R. Loo, ECS Transactions, 64, 977 (2014).

[23] A. Hikavyy, E. Rosseel, G. Eneman, P. Favia, R. Loo, ECS Transactions, 60, 497 (2014).

[24] L. Pelaz, R. Duffy, M. Aboy, L. Marques, P. Lopez, I. Santos, B. J. Pawlak, M. J. H. van Dal, B. Duriez, T. Merelle, G. Doornbos, N. Collaert, L. Witters, R. Rooyackers, W. Vandervorst, M. Jurczak, M. Kaiser, R. G. R. Weemaes, J. G. M. van Berkum, P. Breimer, R. J. P. Lander. Technical Digest - International Electron Devices Meeting, IEDM, art. no. 4796744 (2008).

[25] M. Togo, Y. Sasaki, G. Zschätzsch, G. Boccardi, R. Ritzenthaler, J. W. Lee, F. Khaja, B. Colombeau, L. Godet, P. Martin, S. Brus, S. E. Altamirano, G. Mannaert, H. Dekkers, G. Hellings, N. Horiguchi, W. Vandervorst, and A. Thean. Symposium on VLSI Technology Digest of Technical Papers,196 (2013).

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[26] O. Hazut, A. Agarwala, T. Subramani, S. Waichman, R. Yerushalmi, J. Vis. Exp. 2, 50770 (2013).

[27] Y. Shimizu, H. Takamizawa, K. Inoue, F. Yano, Y. Nagai, L. Lamagna, G. Mazzeo, M. Perego, E. Prati, Nanoscale 6, 706 (2014).

[28] R. A. Puglisi, S. Caccamo, L. D'Urso, G. Fisichella, F. Giannazzo, M. Italia, A. La Magna, Phys. Status Solidi A 212, 1685 (2015).

[29] L. Ye, S. P. Pujari, H. Zuilhof, T. Kudernac, M. P. de Jong, W. G. van der Wiel, J. Huskens, ACS Appl. Mater. Interfaces 7, 3231 (2015).

[30] E. Arduca, M. Mastromatteo, D. De Salvador, G. Seguini, C. Lenardi, E. Napolitani, M. Perego, Nanotechnology 27, 75606 (2016).

[31] T. Alphazan, L. Mathey, M. Schwarzwälder, T. –H. Lin, A. J. Rossini, R.l Wischert, V. Enyedi, H. Fontaine, M. Veillerot, A. Lesage, L. Emsley, L. Veyre, F. Martin, C. Thieuleux, C. Copéret, Chem. Mater. 28, 3634 (2016).

[32] J. Veerbeek, L. Ye, W. Vijselaar, T. Kudernac, W. G. van der Wiel, J. Huskens, Nanoscale 9, 2836 (2017).

[33] H. Wu, B. Guan, Y. Sun, Y. Zhu, Y. Dan, Sci. Rep. 7, 41299 (2017).

[34] J. O'Connell, G. A. Verni, A. Gangnaik, M. Shayesteh, B. Long, Y. M. Georgiev, N. Petkov, G. P. McGlacken, M. A. Morris, R. Duffy, J. D. Holmes, ACS Appl. Mater. Interfaces 7, 15514 (2015).

[35] J. O'Connell, G. Collins, G. P. McGlacken, R. Duffy, J. D. Holmes, ACS Appl. Mater. Interfaces 8, 4101 (2016).

[36] T. F. Kelly, M. K. Miller, Review of Scientific Instruments, 78, 031101, (2007).

[37] Z. Sun, O. Hazut, B. –C. Huang, Y.-P. Chiu, C.-S. Chang, R. Yerushalmi, L. J. Lauhon, D. N. Seidman, Nano Lett. 16, 4490 (2016).

[38] P. De Wolf, R. Stephenson, T. Trenkler, T. Clarysse, T. Hantschel, W. Vandervorst, Journal of Vacuum Science and Technology B 18, 361 (2000).

[39] [Online]. Available: http://www.itrs2.net/

[40] S. M. Sze, *VLSI Technology*, McGraw-Hill Book Co., Singapore (1983).

[41] R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits*, 2nd Ed., John Wiley & Sons, New York (1977).

[42] R. Duffy, M. J. H. Van Dal, B. J. Pawlak, M. Kaiser, R. G. R. Weemaes, B. Degroote, E. Kunnen, and E. Altamirano, Appl. Phys. Lett. 90, 241912 (2007).

ACCEPTED MANUSCRIPT

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This manuscript was accepted by J. Appl. Phys. Click here to see the version of record.

[43] L. Pelaz, L. Marques, M. Aboy, P. Lopez, I. Santos, and R. Duffy, Tech. Dig. - Int. Electron Devices Meeting 2009, 513.

[44] E. Lampin and C. Krzeminski, J. Appl. Phys. 109, 123509 (2011).

[45] I. Martin-Bragado, Appl. Phys. Lett. 98, 233109 (2011).

[46] [Online]. Available: http://www.srim.org

[47] R. Duffy, M. J. H. van Dal, B. J. Pawlak, N. Collaert, L. Witters, R. Rooyackers, M. Kaiser, R. Weemaes, M. Jurczak, R. Lander, Proc. European Solid-State Device Research Conference (ESSDERC) 2008, 334.

[48] M. Shayesteh and R. Duffy, IEEE Trans. Semiconductor Maufacturing 28, 508 (2015).

[49] F. A. Trumbore, Bell Syst. Tech. J. 39, 205 (1960).

[50] P. Pichler, *Intrinsic point defects, impurities, and their diffusion in silicon*, Springer, Berlin (2004).

[51] R. Duffy, V. C. Venezia, J. Loo, M. J. P. Hopstaken, M. A. Verheijen, J. G. M. Van Berkum, G. C. J. Maas, Y. Tamminga, T. Dao, and C. Demeurisse, Appl. Phys. Lett. 86, 081917 (2005).

[52] S. Ruffell, I. V. Mitchell, and P. J. Simpson, J. Appl. Phys. 97, 123518 (2005).

[53] H. C. H. Wang, C. –C. Wang, C. –S. Chang, T. Wang, P. B. Griffin, and C. H. Diaz, IEEE Electron Device Lett. 22, 65 (2001).

[54] R. Duffy, V. C. Venezia, A. Heringa, T. W. T. Hüsken, M. J. P. Hopstaken, N. E. B. Cowern, P. B. Griffin, and C. C. Wang, Appl. Phys. Lett. 82, 3647 (2003).

[55] M. J. P. Hopstaken, Y. Tamminga, M. A. Verheijen, R. Duffy, V. C. Venezia, and A. Heringa, Appl. Surf. Sci. 231-232, 688 (2004).

[56] M. Ferri, S. Solmi, D. Giubertoni, M. Bersani, J. J. Hamilton, M. Kah, K. Kirkby, E. J. H. Collart, and N. E. B. Cowern, J. Appl. Phys. 102, 103707 (2007).

[57] M. Ferri, S. Solmi, A. Parisini, M. Bersani, D. Giubertoni, and M. Barozzi, J. Appl. Phys. 99, 113508 (2006).

[58] B. Kalkofen, M. Lisker, E. P. Burte, Materials Science and Engineering B 114–115, 362 (2004).

[59] Y. Kiyota, T. Nakamura, K. Muraki, T. Inada, J. Electrochem. Soc, 141, 2241 (1994).

[60] Y. Kiyota, T. Inada, J. Vac. Sci. Technol. A 19, 2441 (2001).

[61] C. M. Ransom, T. N. Jackson, J. F. DeGelormo, C. Zeller, D. E. Kotecki, C. Graimann, D. K. Sadana, and J. Benedic, J. Electrochem. Soc.,141, 1378 (1994).

[62] Y.-H. Song, K. –T. Park, H. Kurino and M. Koyanagi, Jpn. J. Appl. Phys. 39, 26 (2000).

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[63] M. Perego, G. Seguini, E. Arduca, J. Frascaroli,D. De Salvador, M. Mastromatteo, A. Carnera, G. Nicotra, M. Scuderi, C. Spinella, G. Impellizzeri, C. Lenardie and E. Napolitani, Nanoscale 7, 14469 (2015).

[64] S. Pantelides, Solid State Communications 84, 221 (1992).

[65] P. Taheri, H. M. Fahad, M. Tosun, M. Hettick, D. Kiriya, K. Chen, and A. Javey, ACS Appl. Mater. Interfaces 9, 20648 (2017).

[66] O. Hazut, A. Agarwala, I. Amit, T. Subramani, S. Zaidiner, Y. Rosenwaks, and R. Yerushalmi, ACS Nano 6, 10311 (2012).

[67] L. Ye, A. Gonzalez-Campo, T. Kudernac, R. Nuńez, M. de Jong, W. G. van der Wiel, and J. Huskens, Langmuir 33, 3635 (2017).

[68] O. Hazut and R. Yerushalmi, Langmuir 33, 5371 (2017).

[69] L. Lin, Z. Li, J. Feng, Z. Zhang, Phys. Chem. Chem. Phys.15, 6063 (2013).

[70] G. Cantele, E. Degoli, E. Luppi, R. Magri, D. Ninno, G. Iadonisi, S. Ossicini, Phys. Rev B 72, 113303 (2005).

[71] T.-L. Chan, M. L. Tiago, E. Kaxiras, and J. R. Chelikowsky, Nanolett. 8, 596 (2008).

[72] D. Hiller, J. López-Vidrier, S. Gutsch, M. Zacharias, K. Nomoto, D. König, Sci. Rep. 7, 863 (2017).

[73] D. Hiller, J. López-Vidrier, S. Gutsch, M. Zacharias, M. Wahl, W. Bock, A. Brodyanski, M. Kopnarski, K. Nomoto, J. Valenta, D. König, Sci. Rep. 7, 8337 (2017).

[74] D. König, S. Gutsch, H. Gnaser, M. Wahl, M. Kopnarski, J. Göttlicher, R. Steininger, M. Zacharias, D. Hiller, Sci. Rep. 5, 9702 (2015).

[75] M.V. Fernández-Serra, Ch. Adessi, and X. Blase, Phys. Rev. Lett. 96, 166805 (2006).

[76] M. Diarra, Y. –M. Niquet, C. Delerue, Guy Allan, Phys. Rev B 75, 045301 (2007).

[77] M. T. Björk, H. Schmid, J. Knoch, H. Riel and W. Riess, Nature Nanotech. 4, 103 (2009).

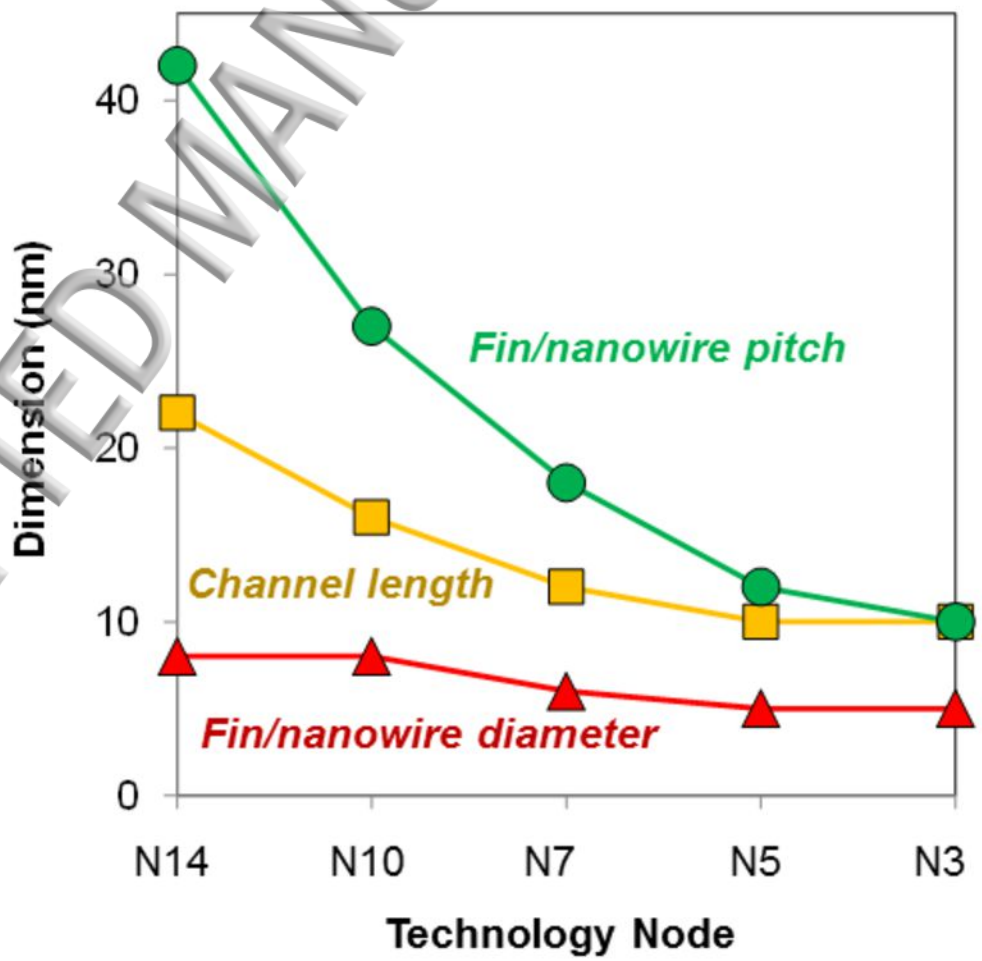
[78] S. H. Jain, P. B. Griffin, J. D. Plummer, S. McCoy, J. Gelpey, T. Selinger, and D. F. Downey, IEEE Trans. El. Dev. 52, 1610 (2005)

[79] S. Earles, M. Law, R. Brindos, K. Jones, S. Talwar, and S. Corcoran, IEEE Trans. El. Dev. 49, 1118 (2002).

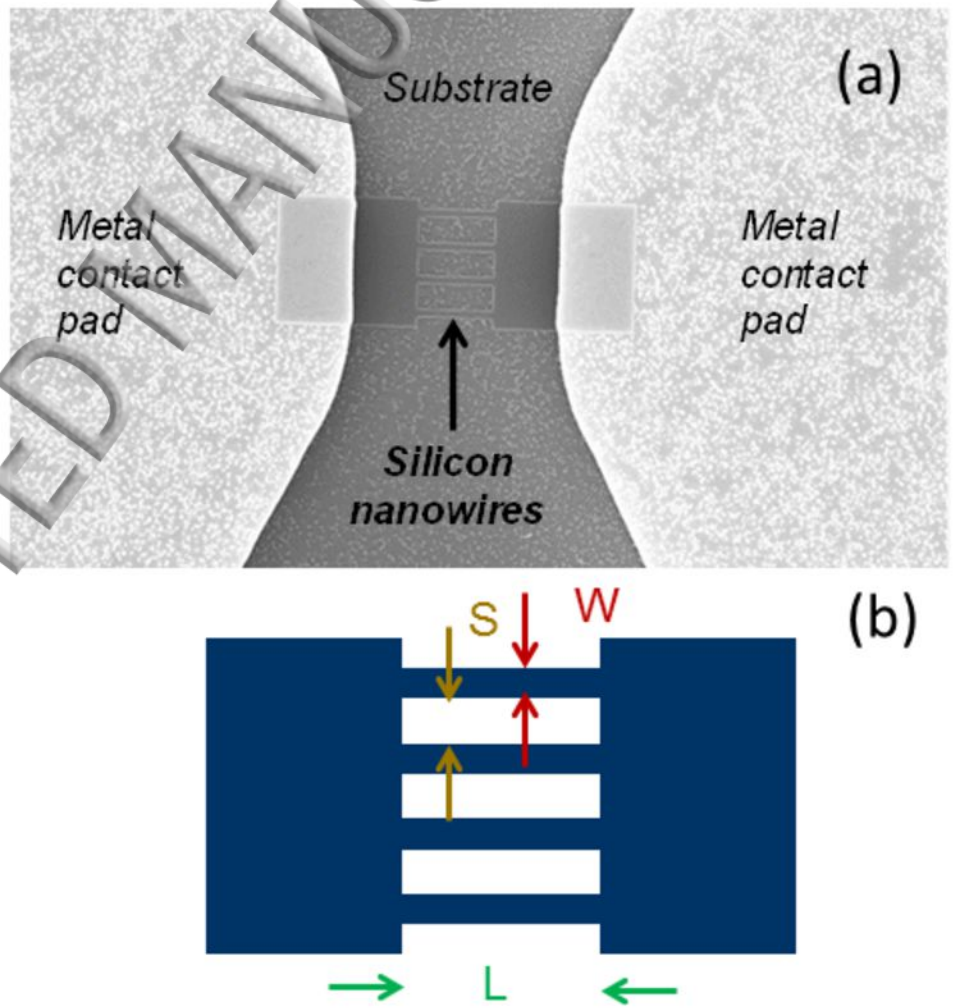
[80] R. Duffy, T. Dao, Y. Tamminga, K. van der Tak, F. Roozeboom, and E. Augendre, Appl. Phys. Lett. 89, 071915 (2006).

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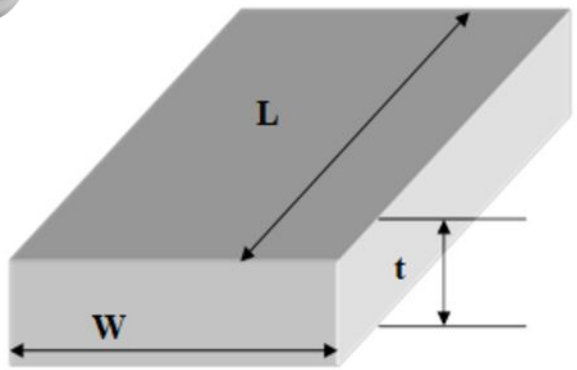
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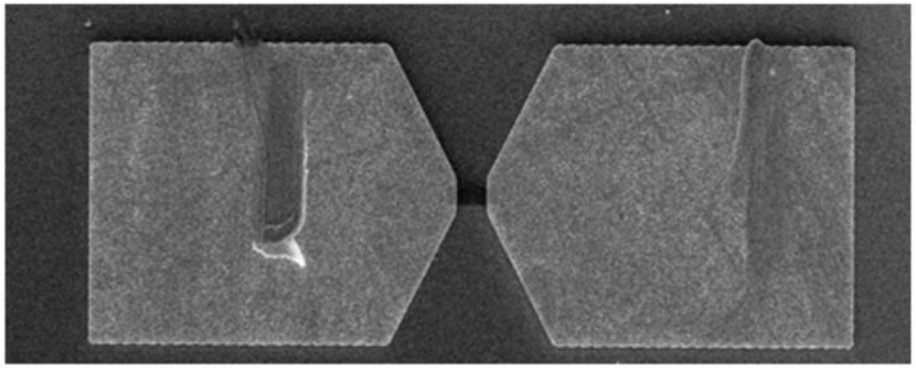
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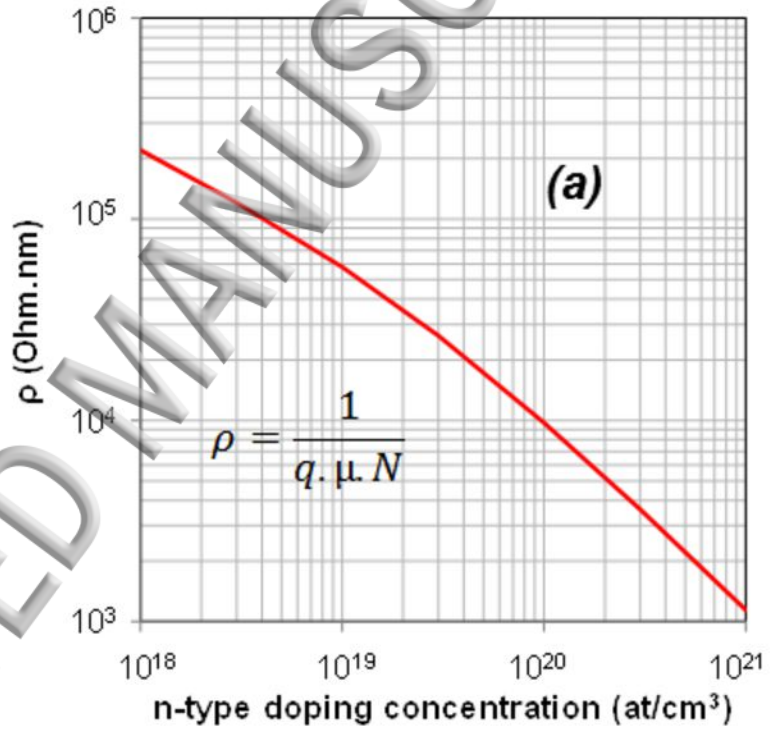
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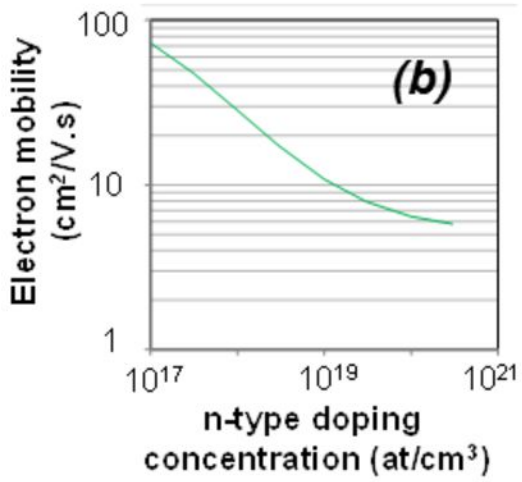
$$R = \frac{\rho}{t} \frac{L}{W}$$





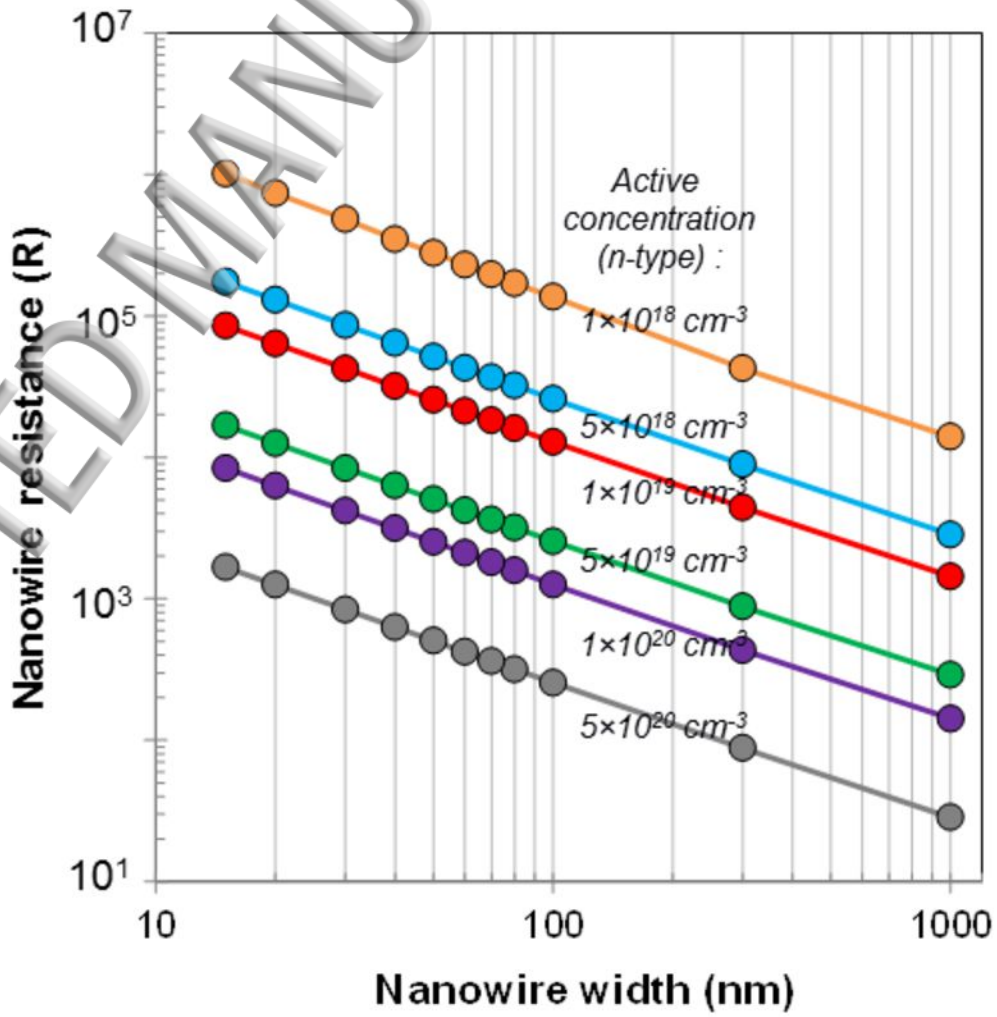






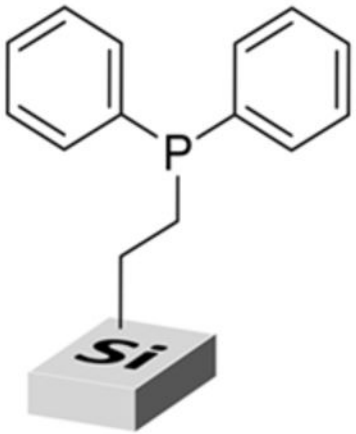
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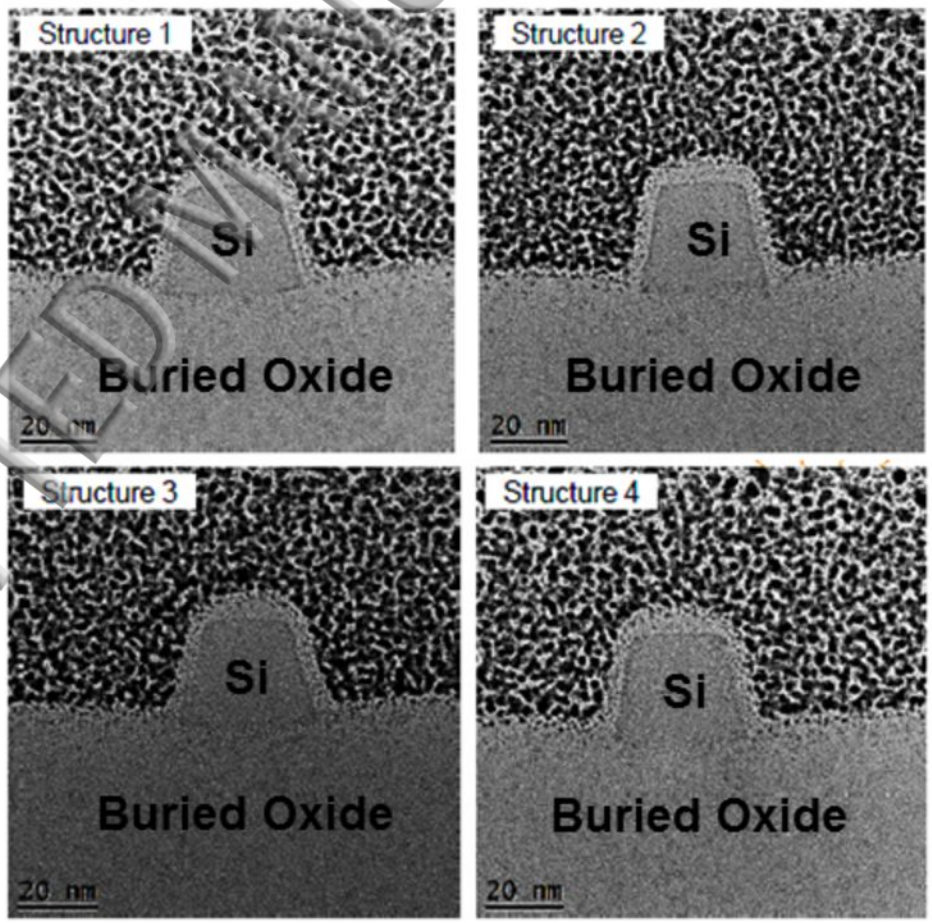


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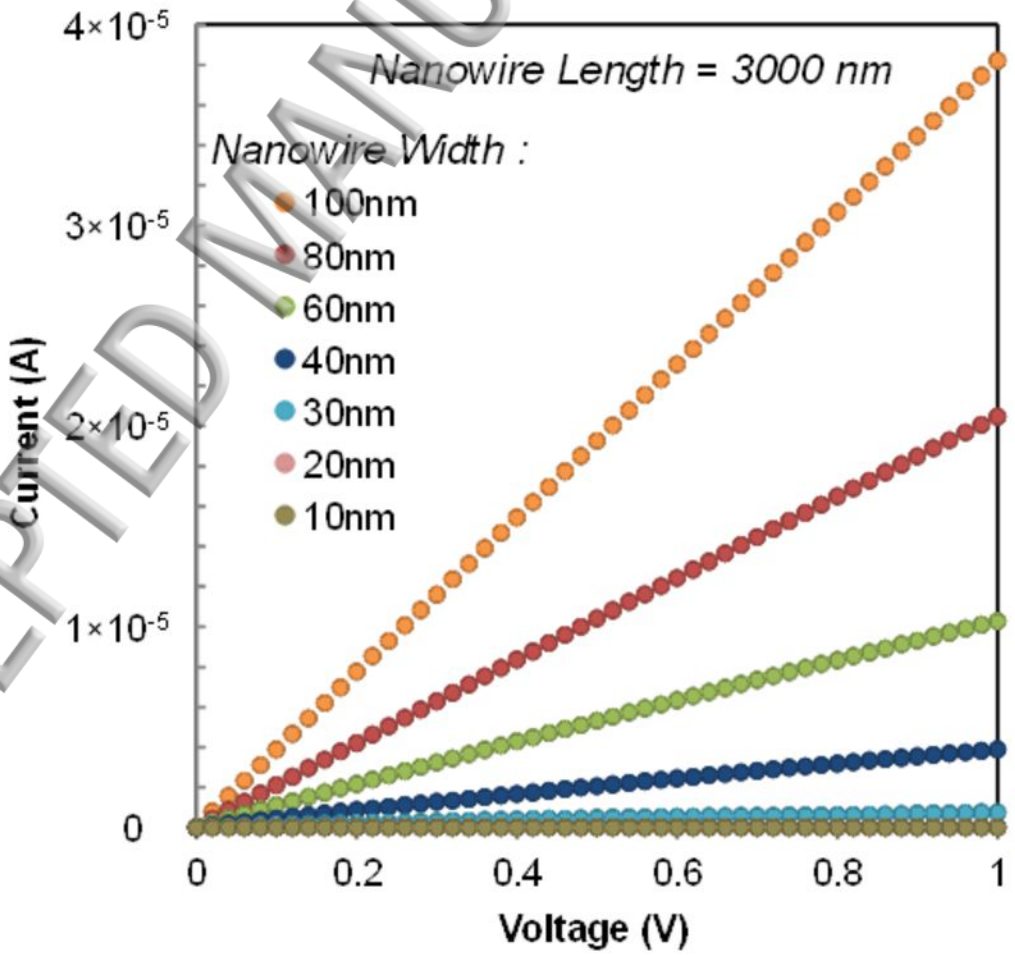
- Starting wafer, 30 nm SOI
- E-beam litho, 6 nm HSQ
- Reactive Ion Etch, Cl_2 based
- Phosphorus MLD
  - Degrease, IPA and acetone
  - RCA clean (**optional**)
  - HF dip
  - ADP functionalisation reaction
  - Cap with SiO_2 (**optional**)
- 1050 °C RTA
- Cap removal (**optional**)
- Ti/Au contact pad metalisation

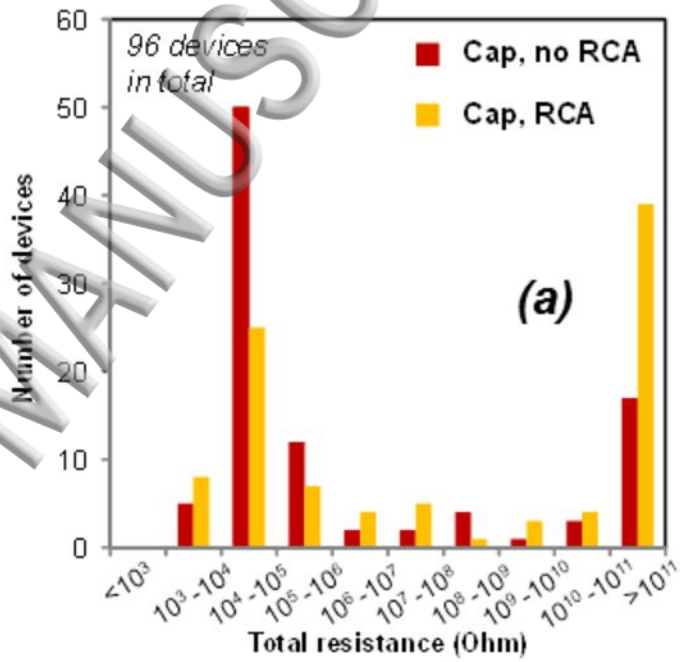


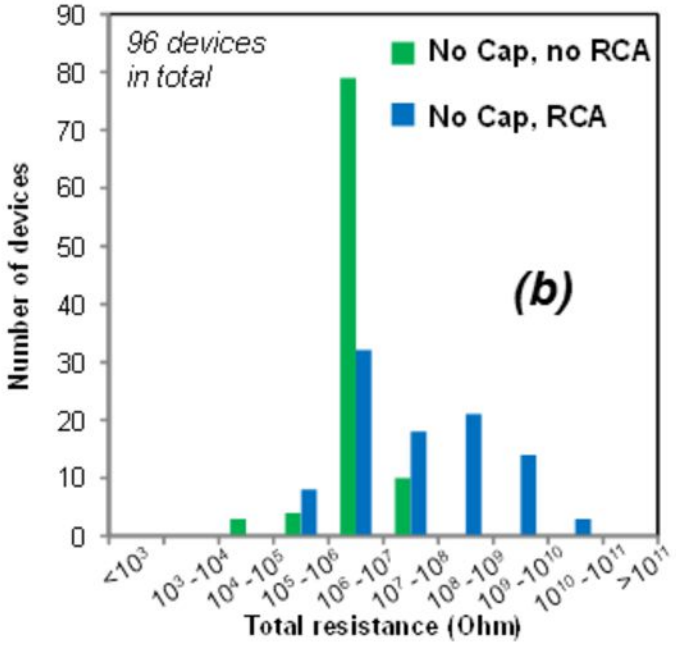
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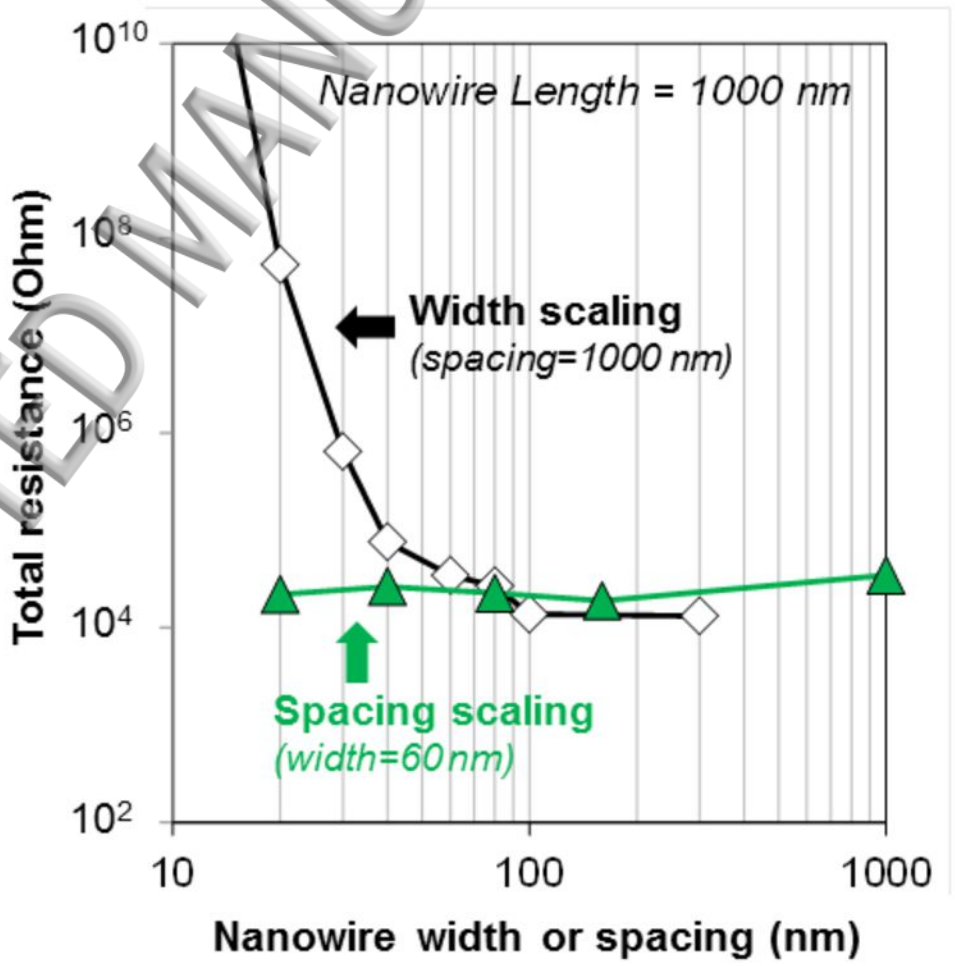






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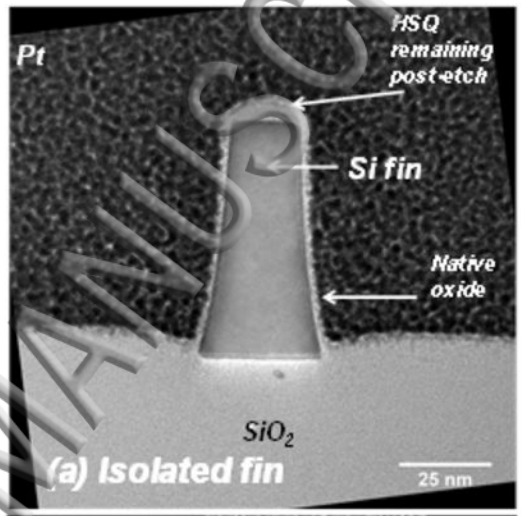


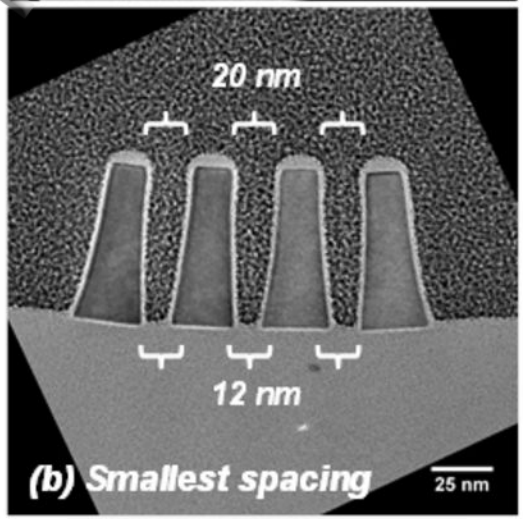
- Starting wafer, 66 nm SOI
- E-beam litho, 15 nm HSQ
- Reactive Ion Etch, Cl_2 based

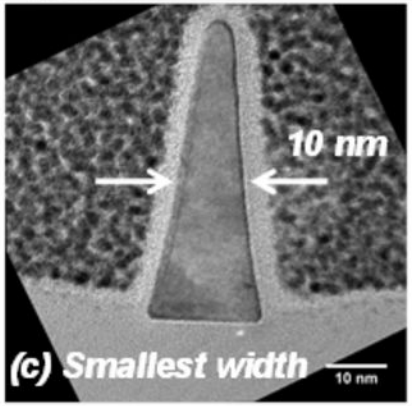
- P MLD
  - Degrease, IPA and acetone
  - HF dip
  - ADP functionalisation
  - Cap with SiO_2
- 1050 °C RTA
- Cap removal
- Ti/Au contact pad metalisation

- P Ion Implant
  - 4×10^{15} cm^{-2}, 45°, 3 keV
- 1050 °C RTA
- Ti/Au contact pad metalisation

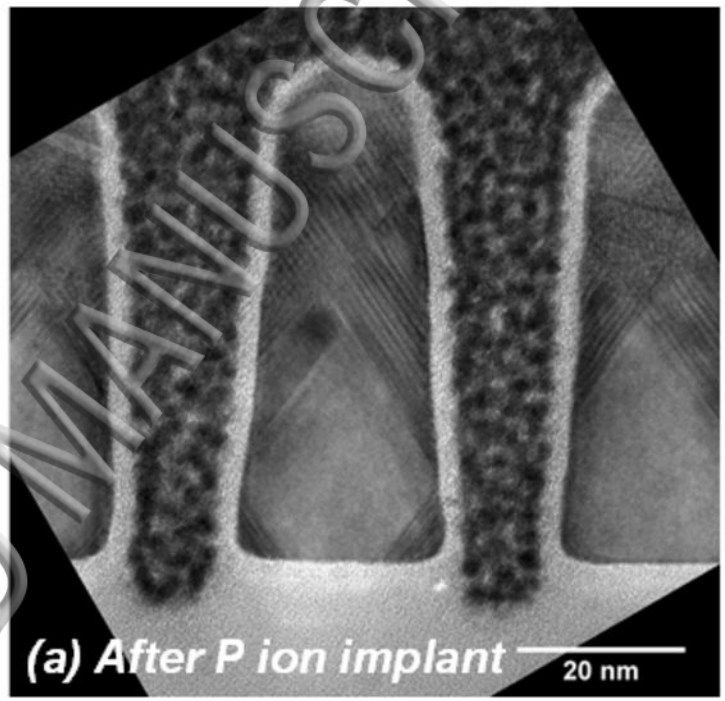
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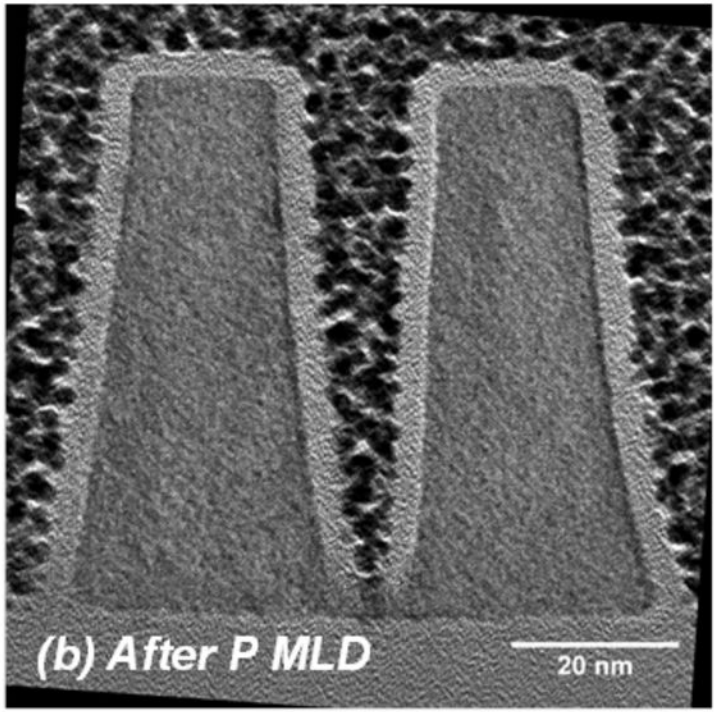






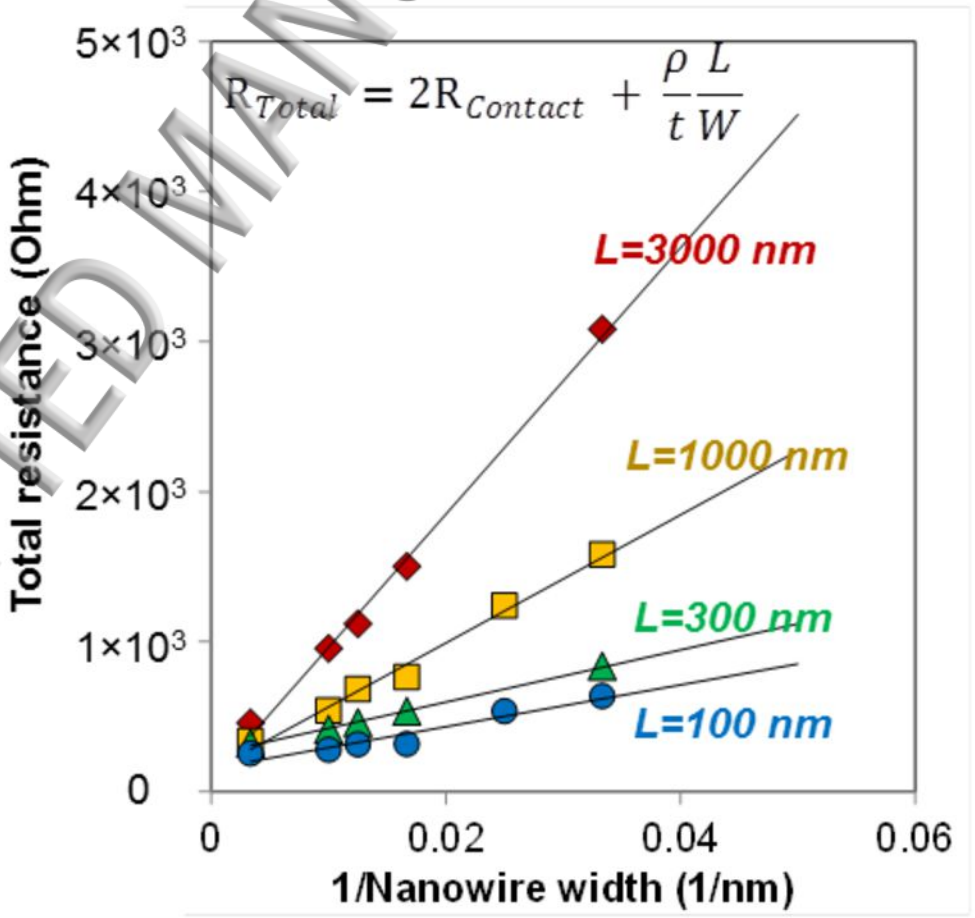
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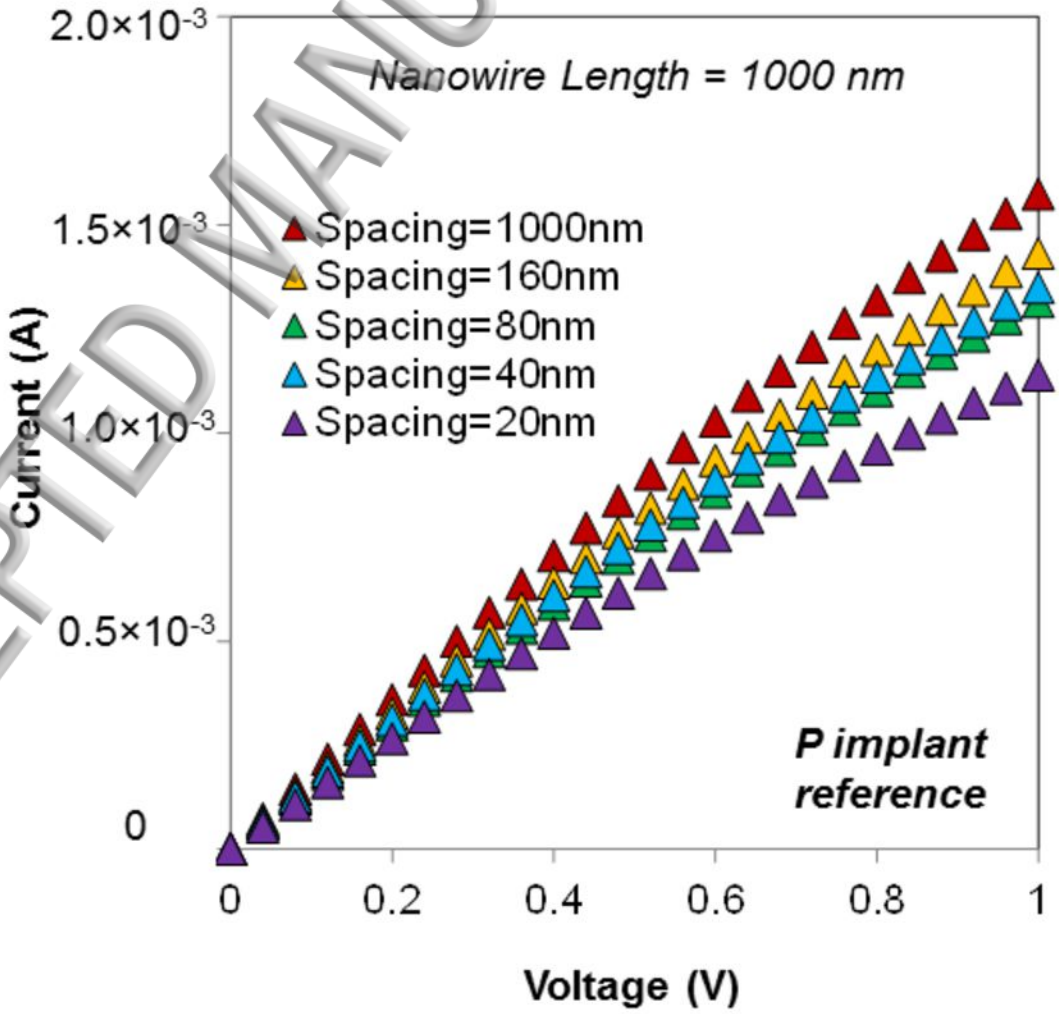


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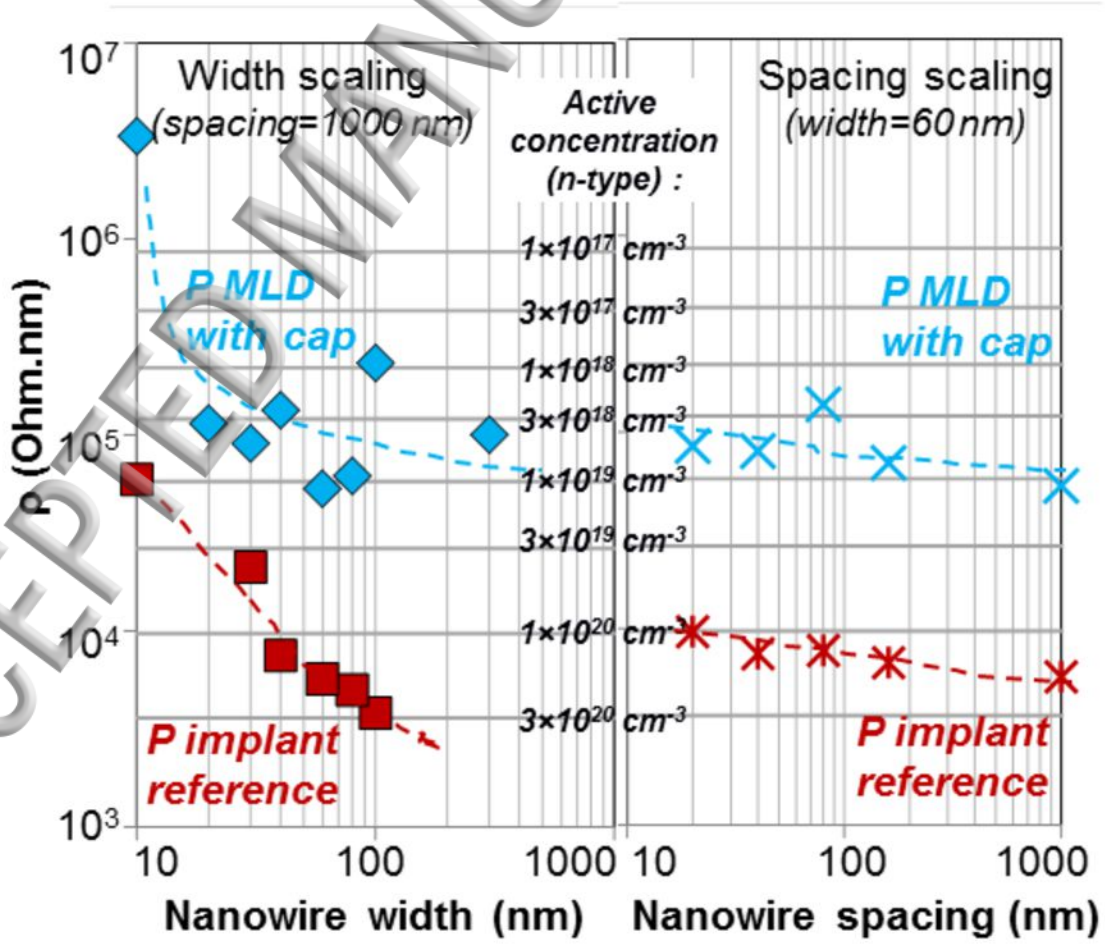
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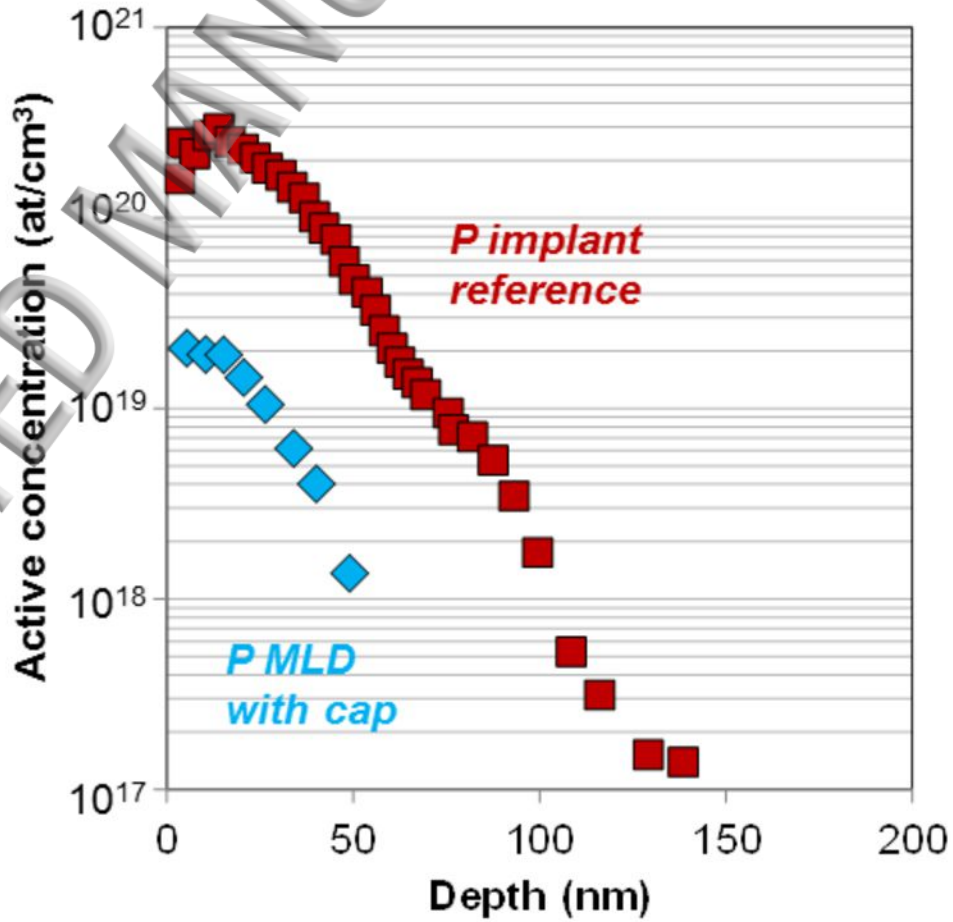
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