

Design of Clock and Data Recovery Circuits for Energy-Efficient Short-Reach Optical Transceivers

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List of Abbreviations

ADC		Analog-To-Digital Converter
AFE		Analog Front-End
AWG		Arbitrary Waveform Generator
BBPD		Bang-Bang Phase Detector
BER		Bit Error Rate
BERT		Bit Error Rate Tester
CDR		Clock And Data Recovery
CEI		Common Electrical Interface
CK/CLK		Clock
CL		Confidence Level
CM		Common Mode
CMFB		Common-Mode Feedback
CML		Current Mode Logic
CMOS		Complementary Metal-Oxide-Semiconductor
CP		Charge Pump
CPM		Clock Phase Margin
CTE		Coefficient of Thermal Expansion
CTLE		Continuous Time Linear Equalizer
DAC		Digital-To-Analog Converter
DCD		Duty Cycle Distortion
DCO		Digitally Controlled Oscillator
DDJ		Data Dependent Jitter
DPC		Digital-To-Phase Converter
DPO		Digital Phosphor Oscilloscope
DFE		Decision Feedback Equalization

DFF		D Flip Flop
DLC		Digital Loop Controller
DLF		Digital Loop Filter
DLL		Delay Lock Loop
DMUX		De-MUltipleXer
DEMUX		De-MUltipleXer
DNL		Differential Nonlinearity
DUT		Device Under Test
HDL		Hardware Description Language
EM		Electromagnetic
EQ		Equalizer
FA		Full Adder
FF		Flip Flop
FFE		Feed-Forward Equalization
FIR		Finite Impulse Response
IC		Integrated Circuit
IFFT		Inverse Fast Fourier Transform
IL		Insertion Loss
INL		Integral Nonlinearity
ISI		Intersymbol Interference
JG		Jitter Generation
JTOL		Jitter Tolerance
JTRAN		Jitter Transfer
LAN		Local-Area-Network
LPF		Low-Pass Filter
LF		Loop Filter
LSB		Least Significant Bit

LTI		Linear Time Invariant
MAC		Multiplier Accumulator
MPCG		Multi-Phase Clock Generator
MOSFET	...	Metal-Oxide Semiconductor Field Effect Transistor
MSB		Most Significant Bit
MV		Majority Voting
NRZ		Non-Return-To-Zero
OCV		On chip Variation
OIF		Optical Internetworking Forum
OOK		On-Off Keying
PAM		Pulse Amplitude Modulation
PCB		Printed Circuit Board
PD		Phase Detector
PDK		Process Design Kit
PDF		probability Density Function
PI		Phase Interpolator
PLL		Phase Lock Loop
PM		Phase Margin
ppm		part per million
PR		Phase Rotator
PRBS		Pseudo-Random Binary Sequence
PS		Phase Selector
PSD		Power Spectrum Density
PVT		Process, Voltage and Temperature
QPC		Quadrature Phase Corrector
RBW		Resolution Bandwidth
RMS		Root Mean Square

RTL		Register Transfer Level
RX		Receiver
SCR		Spur to Carrier Ratio
SDF		Standard Delay Format
SER		Symbol Error Rate
ISF		Impulse Sensitivity Function
SJ		Sinusoidal Jitter
SCR		Side-band to Carrier Ratio
SNR		Signal-To-Noise Ratio
SPI		Serial Peripheral Interface
SR		Slew Rate
STA		Static Timing Analysis
TIA		Transimpedance Amplifier
ToR		Top of the Rack
TSPC		True Single Phase Clock
TSV		Through Silicon Via
TX		Transmitter
UI		Unit Interval
VCDL		Voltage Controlled Delay Line
VCO		Voltage Controlled Oscillator
VNA		Vector Network Analyzer

List of publications

- Meysam M. Khanghah, Khosrov D. Sadeghipour, Denis Kelly, Cleitus Antony, Peter Ossieur, Paul D. Townsend, "A 7-Bit 7-GHz Multi-Phase Interpolator-Based DPC for CDR Applications" in *IEEE Transactions on circuits and systems-I*, (DOI: 10.1109/TCSI.2022.3191229).
- Meysam Khanghah, Khosrov D. Sadeghipour, Denis Kelly, Peter Ossieur, Paul D. Townsend, "A new PAM4 Clock and Data Recovery Circuit for Short Reach Optical Interconnects" in *2018 Photonics Ireland Conference*, Cork, Ireland, 2018.
- C. Antony, M. Khanghah, S. Murphy and P. D. Townsend, "Link optimisation for 100 Gb/s and beyond data centre interconnects," *2020 Photonics Ireland Conference*, pp. 110–111, 2020.

Abstract

Nowadays, the increasing demand for cloud based computing and social media services mandates higher throughput (at least 56 Gb/s per data lane with 400 Gb/s total capacity ¹) for short reach optical links (with the reach typically less than 2 km) inside data centres. The immediate consequences are the huge and power hungry data centers. To address these issues the intra-data-center connectivity by means of optical links needs continuous upgrading.

In recent years, the trend in the industry has shifted toward the use of more complex modulation formats like PAM4 due to its spectral efficiency over the traditional NRZ. Another advantage is the reduced number of channels count which is more cost-effective considering the required area and the I/O density. However employing PAM4 results in more complex transceivers circuitry due to the presence of multilevel transitions and reduced noise budget. In addition, providing higher speed while accommodating the stringent requirements of higher density and energy efficiency (< 5 pJ/bit), makes the design of the optical links more challenging and requires innovative design techniques both at the system and circuit level.

This work presents the design of a Clock and Data Recovery Circuit (CDR) as one of the key building blocks for the transceiver modules used in such fibre-optic links. Capable of working with PAM4 signalling format, the new proposed CDR architecture targets data rates of 50 – 56 Gb/s while achieving the required energy efficiency (< 5 pJ/bit).

At the system level, the design proposes a new PAM4 PD which provides a better trade-off in terms of bandwidth and systematic jitter generation in the CDR. By using a digital loop controller (DLC), the CDR gains considerable area reduction with flexibility to adjust the loop dynamics.

At the circuit level it focuses on applying different circuit techniques to mitigate the circuit imperfections. It presents a wideband analog front end (AFE), suitable for a 56 Gb/s, 28-Gbaud PAM-4 signal, by using an 8x interleaved, master/slave based sample and hold circuit. In addition, the AFE is equipped with a calibration scheme which corrects the errors associated with the sampling channels' offset voltage and gain mismatches. The presented digital to phase converter (DPC) features a modified phase interpolator (PI), a new quadrature phase corrector (QPC) and multi-phase output with de-skewing capabilities.

¹the numbers are for the time when this research project was initiated.

The DPC (as a standalone block) and the CDR (as the main focus of this work) were fabricated in 65-nm CMOS technology. Based on the measurements, the DPC achieves DNL/INL of 0.7/6 LSB respectively while consuming 40.5 mW power from 1.05 V supply. Although the CDR was not fully operational with the PAM4 input, the results from 25-Gbaud PAM2 (NRZ) test setup were used to estimate the performance. Under this scenario, the 1-UI JTOL bandwidth was measured to be 2 MHz with BER threshold of 10^{-4} . The chip consumes 236 mW of power while operating on 1 – 1.2 V supply range achieving an energy-efficiency of 4.27 pJ/bit.

I, Meysam M Khanghah, certify that this thesis is my own work and has not been submitted for another degree at University College Cork or elsewhere.

Meysam M Khanghah

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Chapter 1

Introduction

1.1 Motivation and Research Objectives

Nowadays, the increasing demand for cloud based computing and social media services mandates higher throughput (at least 56 Gb/s per data lane with 400 Gb/s total capacity) for short-reach optical links (typically < 2 km) inside data centres. Intra-data centre interconnects necessitate a large number of connections to facilitate the fanout/rich connectivity needed to realize a scaled-out multistage switching network like Clos fabric [1], [2], [3], (Fig. 1.1), and thus their cost is largely dominated by the transceivers [1]. Providing higher speed while accommodating the stringent requirements of higher density and energy efficiency (< 5 pJ/bit [4]) makes the design of optical transceivers more challenging and requires innovative design techniques both at the system and circuit level.

Traditionally NRZ is the main signalling format directly invoked to modulate the light intensity i.e. OOK (on-off keying) and has dominated the optical communication field for decades. However, at higher data rates scaling the interconnects capacity per lane by only resorting to increasing the symbol rate may not be a cost-effective method as it requires high frequency bandwidth [3]. One of the current trends to address this issue is to utilize more advanced modulation schemes like pulse amplitude modulation PAM4. The main advantage of PAM4 is its spectral efficiency due to encoding of two bits of information into one symbol therefore with the same bandwidth it doubles the bit-rate that could be achieved by NRZ signalling. At first sight it may be postulated that other aspects of transceivers performance, for instance power consumption can also benefit

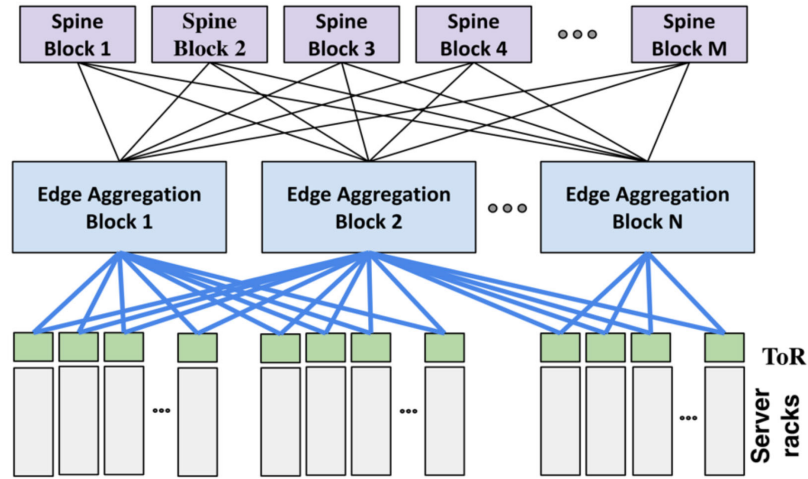


Figure 1.1: Example of intra-data centres network structure and interconnects, optical transceivers and links facilitate the connectivity between the different network blocks [1]

from the same level of scaling. However the caveat is that PAM4 compromises the swing in exchange for the bandwidth efficiency i.e. it has 4 levels with the data swings (for LSB values) equal to the one third of available headroom, therefore, there is an inherited 9.5 dB penalty ($= 20 \log(1/3)$) in SNR. Additionally, the required specifications can be quite different if not contradictory, for example, in PAM4 the linearity is an important feature whenever signal amplification is considered, this is not the case with NRZ as 1-bit data systematically favours strong amplitude saturation as it is compared against only one decision level. Thus many nonlinear equalization techniques cannot be readily applied to PAM4. PAM4 signalling entails another issue; the number of transitions is 16 in comparison to 2 in NRZ. The RX backend which includes the clock and data recovery (CDR) has to deal with multilevel transitions which would complicate the phase detection mechanism. These requirements make the design of PAM4 based transceivers more challenging. Despite all these drawbacks PAM4 has proved to be effective especially when the channel loss (including the Rx optical and electrical front-end) at high frequencies is extremely high and the frequency response cannot be equalized efficiently using the linear or nonlinear equalizers [5].

The focus of this research is on CDR design for the Rx part of an optical transceiver which uses silicon photonics in conjunction with CMOS technology to develop the next generation of more compact and high speed optical interconnects. The main design features a 28 GBd PAM4 CDR (56 Gb/s) in 65-nm bulk CMOS technology (STMicroelectronics). Other building blocks including the Tx and Rx

front-end have been developed successfully in other research projects carried out within our group (PSG) [6], [7]. The goal is to address some of the issues related to CDR applications in PAM4 signalling and provide solutions both at the system and circuit level. Our objective would be oriented around a certain type of CDR category which meets stringent design criteria. We will incorporate different methods and devise techniques that would enhance the CDR function and at the same time would be cost effective in terms of transceiver's power dissipation and footprint area. This is well-aligned with the main target in optical link design which seeks solutions that optimize the energy efficiency and density issues in intra-datacentre connectivity.

1.2 Thesis Organization

This thesis is organised in 5 chapters. The rest of Chapter 1 is dedicated to an introduction to CDRs and describes the overall architecture of our developed CDR.

Chapter 2 focuses on the system level implementation of the CDR. It presents a behavioural model for the CDR and analyses the loop dynamics. A new tri-level PAM4 PD is proposed which offers a better trade-off between the systematic jitter generation and BW reduction when the elimination of the middle transitions is considered. This Chapter also investigates the non-idealities introduced by the building blocks at circuit level, which motivates the addition of the trimming functionalities.

Chapter 3 focuses on the circuit level design of the AFE, DLC and DPC blocks in detail. The circuit techniques to achieve the required performance are discussed while also considering the impact on area, re-configurability and power efficiency.

Chapter 4 presents the experimental results for two chips: DPC as a stand-alone block and the CDR which has incorporated the DPC. The validation process for the DPC and CDR is a complex task which demands sophisticated testing methods. Every step is explained in detail. To tackle the packaging issues in the CDR a custom silicon interposer had to be designed and tested separately. The interposer is also covered in this chapter. In addition, Chapter 4 provides a performance comparison between the measurement results and some recent works. Finally, Chapter 5 will summarise the thesis and provide some suggestions for future works.

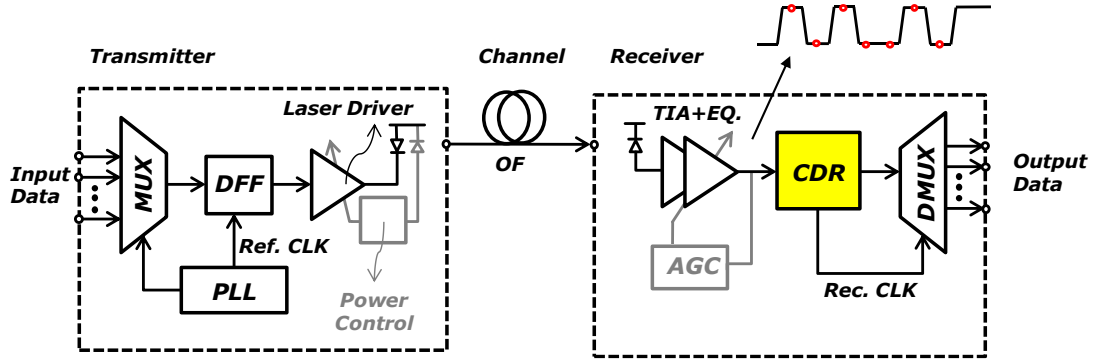


Figure 1.2: A generic view of an optical link, the CDR has to guarantee the sampling of the input at the points with high SNR and clock phase margin to reduce the BER

1.3 Clock and Data Recovery Basics

Fig. 1.2 depicts a generic view of a simple optical communication system. In the TX side, after serializing (multiplexing) and retiming of the inputs (some sort of channel equalization using FFE blocks may be performed) the electrical signals are converted to light using laser diodes which are driven by laser drivers. The system in its simplest form relies on the intensity modulation of the light. At the RX side the reverse function has to be implemented. The light is converted to electrical signal by the photo diode followed by a TIA, the subsequent blocks restore the signals to the required level by employing equalizers and hard limiters (in NRZ case).

The back-end block in the receiver chain is the CDR which has to extract the timing information from the input signal (clock recovery) and perform sampling (data re-timing) in high SNR regions to achieve minimum BER as predicted by [8]:

$$BER = Q\left(\frac{V_{pp}}{2\sigma_n}\right) \quad (1.1)$$

wherein Q-function is defined as $\int_t^{+\infty} e^{-(x^2/2)} dx$ and σ_n represents the random noise on the sampled signal with peak-to-peak swing of V_{pp} . In addition, the uncertainty in timing of transitions i.e. jitter can cause decision errors as described by¹ [9]:

$$BER = Q\left(\frac{T_b}{2\sigma_j}\right) \quad (1.2)$$

σ_j represents the RMS value for the total random jitter both on data and clock

¹In deriving the BERs we only assumed the influence of random components both on signal's amplitude and transition.

transitions. Eqn. 1.2 implies how the role of the CDR becomes crucial as the data rates increases. At higher speeds due to the limited BW, the signals' transition time would be comparable to the symbol-time (T_b), and hence reducing the sampling clock's phase margin (CPM). Other factors including the sampling circuit imperfections such as aperture time and sensitivity would narrow down this margin further.

1.3.1 CDR based on phase locking

The clock recovery by phase locking has a similar architecture to conventional PLLs except that the input is random data, and this is what makes the CDR realization entirely different. The main reason is that a normal PLL would fail to lock on the data due to the randomness of the transitions; in its basic form a simple PD based on XOR function would produce an output with an average being independent of the input phase error, Fig. 1.3. Because of the random transitions, the output average is not a one-to-one function of the input data as shown in Fig. 1.3. An alternative explanation can be drawn based on the frequency spectrum analysis [10]. Since the XOR operation is equivalent to a multiplier (mixer)² then the convolution of the data and clock spectra would lack DC components to drive the PLL toward the lock. This is due to the fact that a random data lacks the beats (spectral lines) at the frequency equal to the symbol-rate.

Among the phase detectors suitable to work with random patterns, the Hogge PD and Alexander PD, are the commonly used ones, while the former offers linear operation and minimum jitter generation the latter can be useful for targeting high speed designs.

The Hogge phase detector [11] delivers an output with an average proportional to the input phase error, Fig. 1.4. In the output A, the pulses width is equal to the clock width (half the CK period) minus the actual phase error. The output B generates constant pulse width equal to half the CK period. The purpose behind this additional output is to remove the dependency of the pulses width in A from the data transition density. Such linear operation impairs the application of Hogge PD to higher data rates as the generation of narrow-width pulses at the output of the XOR gates would be challenging.

The Alexander PD [12] also referred as binary or bang-bang is shown in Fig.

²Providing that the inputs are DC balanced.

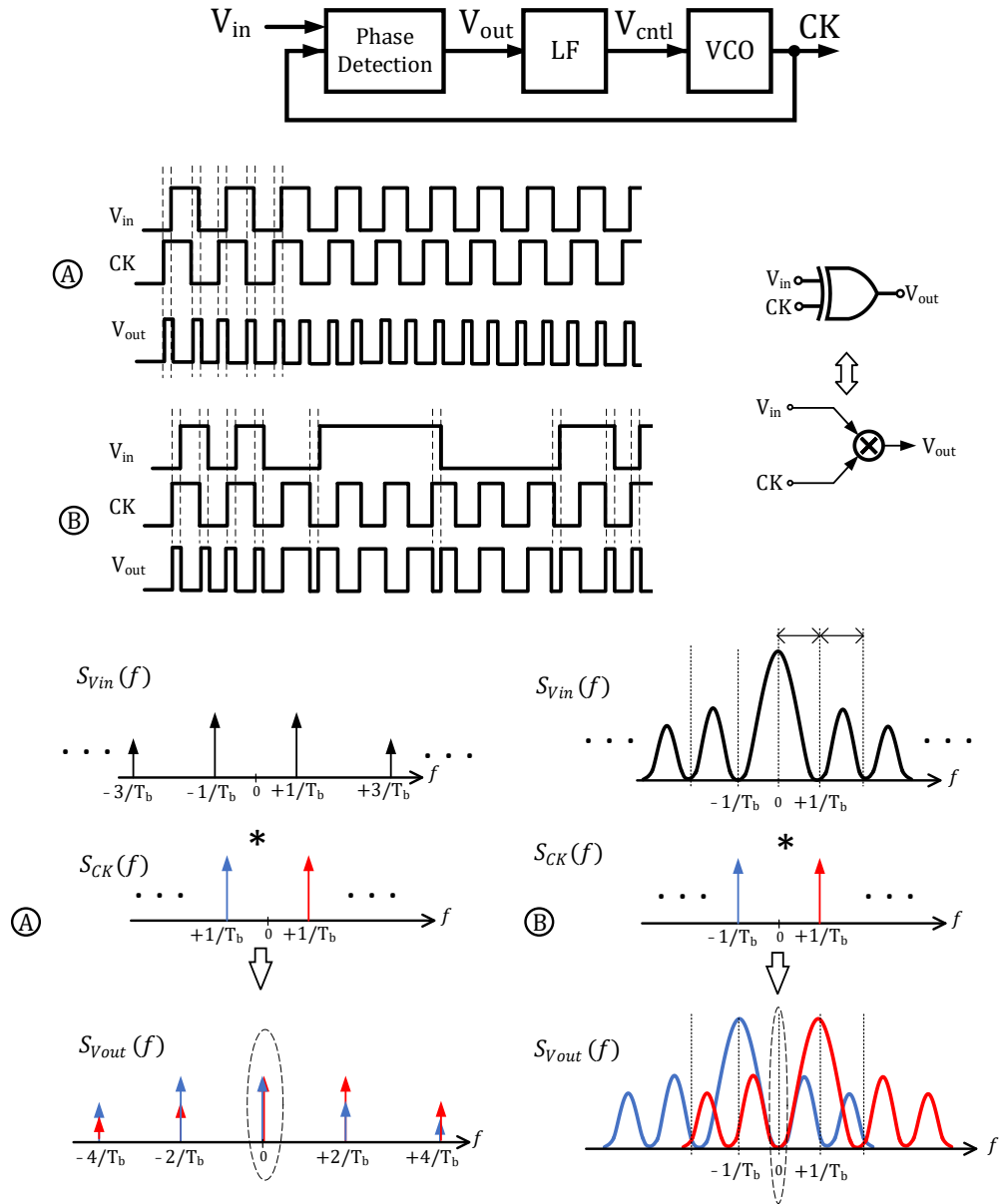
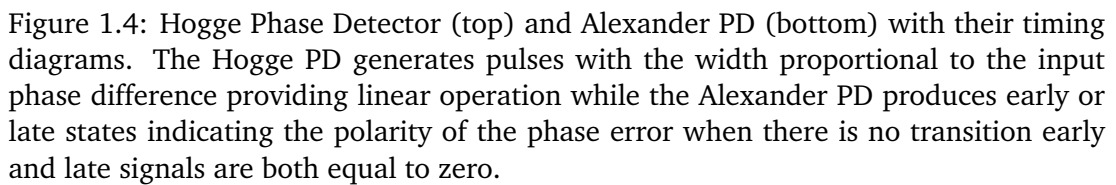


Figure 1.3: PLL block diagram, the timing diagrams indicate how the traditional PLL cannot lock on to random data due to the failure of the PD in producing unique DC components. In case A the input is a periodic signal while in case B the input is a random data.

1.4. The operation involves simply looking at the polarity of the phase error which corresponds to the sign function. Depending on whether the clock lags or leads the data the output states in E or L toggles. Hence regardless of the magnitude of the error the output is always $+1$, -1 or 0^3 . Such an output

³In the strictest sense, the Alexander PD resembles a ternary operation rather than a binary one. Although a BBPD could be built based on other architectures (e.g. a simple DFF), throughout this thesis we have used the BBPD term specifically to refer to the Alexander PD implementation.



1.3.2 CDR Topologies

Meysam M Khanghah

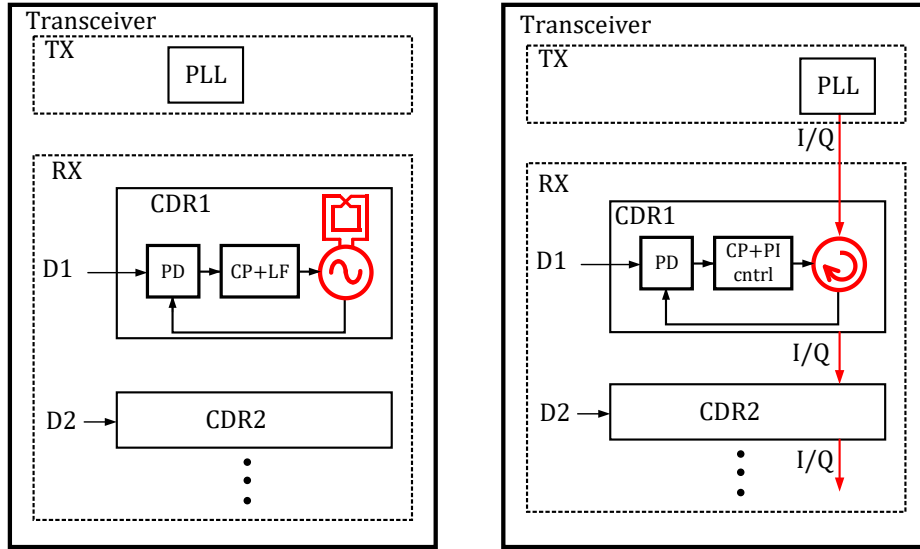


Figure 1.5: Transceiver architecture based on two different type of CDR (left) Reference-less (VCO-based) CDR (right) Referenced (PR-based CDR)

loop and the loop can control both the frequency and phase of the clock (Frequency Modulation), in the former the loop directly adjusts the phase of the clock (Phase Modulation). Although, VCO based CDRs have wider frequency range of operation, they might be disadvantageous in some applications. In the references-less or VCO-based CDR each lane/channel has a dedicated VCO. The large footprint, noise coupling and possible injection locking of the VCOs are among the main design issues. The area limitation could also escalate to be the main limitation factor since the VCO part is usually realized by means of LC oscillators to lessen the influence of phase noise on the jitter generation [8], [14]. The PR based CDR however can benefit from the sharing of one master clock generator and avoid the risks associated with the other architectures. In addition, CDRs with PR demonstrate better performance in terms of less jitter generation since the clock generating PLL resides outside of the CDR loop, hence they can use a clean clock source as a reference instead of the input with high jitter [15]. The main PR-based CDR's shortcoming is linked to the long interconnect routings which can cause large timing skews.

Although analog CDRs can be advantageous in terms of power consumption and less jitter generation, the “digital” counterpart offers the opportunities for considerable area reduction and loop re-configurability. For example, a digital loop-filter can eliminate the need for large (often off-chip) capacitors [16] when large damping factor is required to create first-order-like loop responses. This could greatly influence the loop dynamics if the packaging parasitic is taken

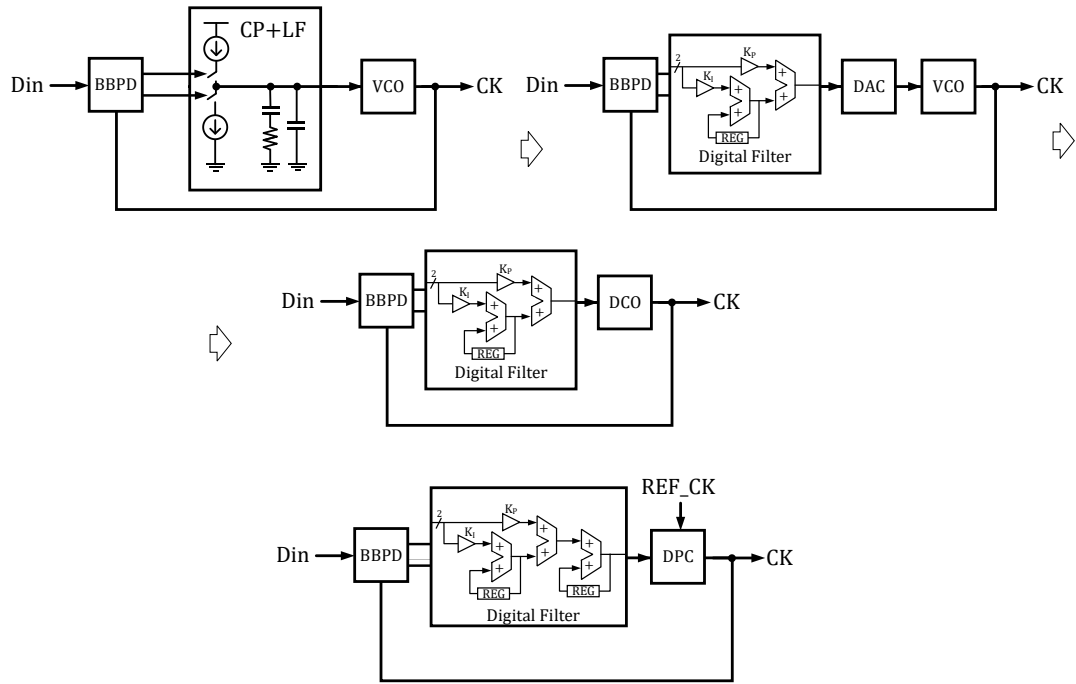


Figure 1.6: Transforming an analog CDR (VCO-based) to a digital CDR (DCO-based) the digital to analog conversion (DAC) is embedded inside DCO. Using similar approach DPC can replace the analog PR.

into account as it could increase the loop order. In addition, the need for other blocks such as charge-pumps or V/I converters is eliminated, simplifying the design complexity. By replacing the VCO or analog PR with the DCO or DPC (digital PR) the digital CDR emerges [Fig. 1.6]. For digital CDR the BBPD is the most preferred option as it already provides digital input for the loop in the form of quantized levels.

1.3.3 CDR Performance Metrics

CDR dynamics are described by three jitter characteristics. Jitter Transfer (JTRAN) which specifies the relation between the output (the recovered clock) phase, ϕ_{out} , and the input (data) phase, ϕ_{in} . It shows the removal of the jitter from the data transitions i.e. the “cleanness” of the recovered clock. This characteristic gains more importance for CDRs inside cascaded repeaters like those in long haul optical networks which have to moderate jitter accumulation, hence low BW is usually preferred [17]. In such applications the JTRAN must be free of any jitter peaking implying that the CDR loop has to provide high damping factor ($\zeta > 2$) [16]. Additionally, for the digital CDR it mandates reducing the loop latency resulted from the delays of digital blocks.

Closely related to JTRAN is the Jitter Generation metric which is a measure of jitter contribution from the CDR itself. The blocks such as VCO, PR and PD can be the source of phase noise and thus increase the amount of jitter present at the recovered clock even with a jitter-free input. To reduce the amount of jitter generated in the loop the CDR needs to retain high bandwidth. Note that this criterion demand is opposite of what is desired by the JTRAN characteristic so to refrain from “costly compromises” it is essential to minimize the amount of noise generated by these sources.

The input phase fluctuations ($d\phi_{in}/dt$) determines the CDR’s ability to track the input jitter. As the CDR loses lock, the data may be sampled closer to the transitions, hence the possibility of decision errors due the systematic errors and low SNR increases which increases the BER. The performance of the CDR in such scenarios can be quantified by another metric called Jitter Tolerance (JTOL).

The jitter tolerance is defined as the maximum jitter amplitude (ϕ_j) (at the input data transitions) that the CDR can track at a given jitter frequency (f_j) while keeping the BER under a certain threshold. With each wireline/optical standard there is a specification for JTOL described under a jitter tolerance mask which the Rx circuitry must satisfy. For JTOL, the input usually takes the sinusoidal form of $\phi_{in} = \phi_j \cos(2\pi f_j t)$, if the loop is able to track the input then $d\phi_{out}/dt = d\phi_{in}/dt$ is satisfied i.e. $\phi_e = \phi_{in} - \phi_{out} = 0$. Because of the limited BW, $d\phi_{out}/dt$ is bounded; therefore there is a maximum input jitter, ϕ_j that the loop can track. From this description we expect that, as f_j approaches higher values, ϕ_j decreases. In an ideal situation, the maximum ϕ_e is 0.5 UI. Assuming that the CDR is an LTI system with the open loop transfer function of $H(S)$, calculation of the closed loop response for ϕ_e results in:

$$\phi_e = \frac{\phi_{in}}{1 - H(s)} \quad (1.3)$$

Since $\phi_e = \phi_{in} - \phi_{out} < 0.5 \text{ UI}$ ⁴ then:

$$\phi_{in} < \frac{0.5 \text{ UI}}{1 - H(s)} \quad (1.4)$$

⁴One UI is equal to one symbol time. For example, for 56 Gb/s PAM4 it is approximately equal to 36 ps.

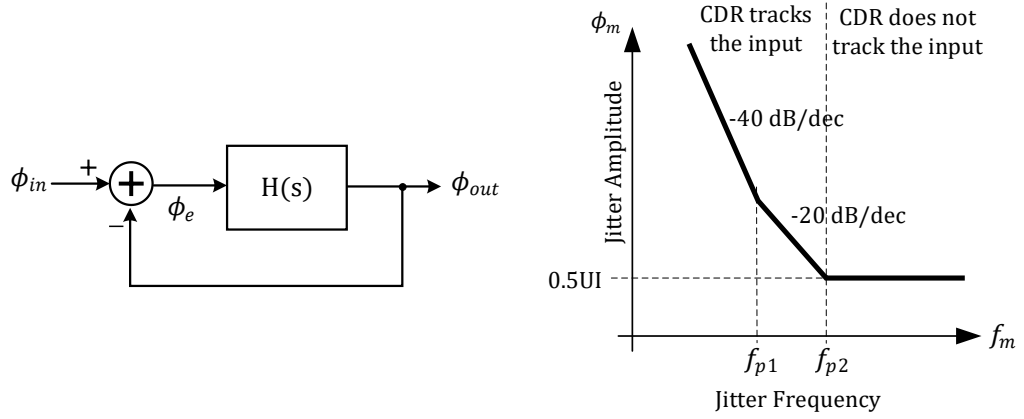


Figure 1.7: The JTOL curve for a CDR with a second order loop filter, the PD gain is considered inside $H(s)$.

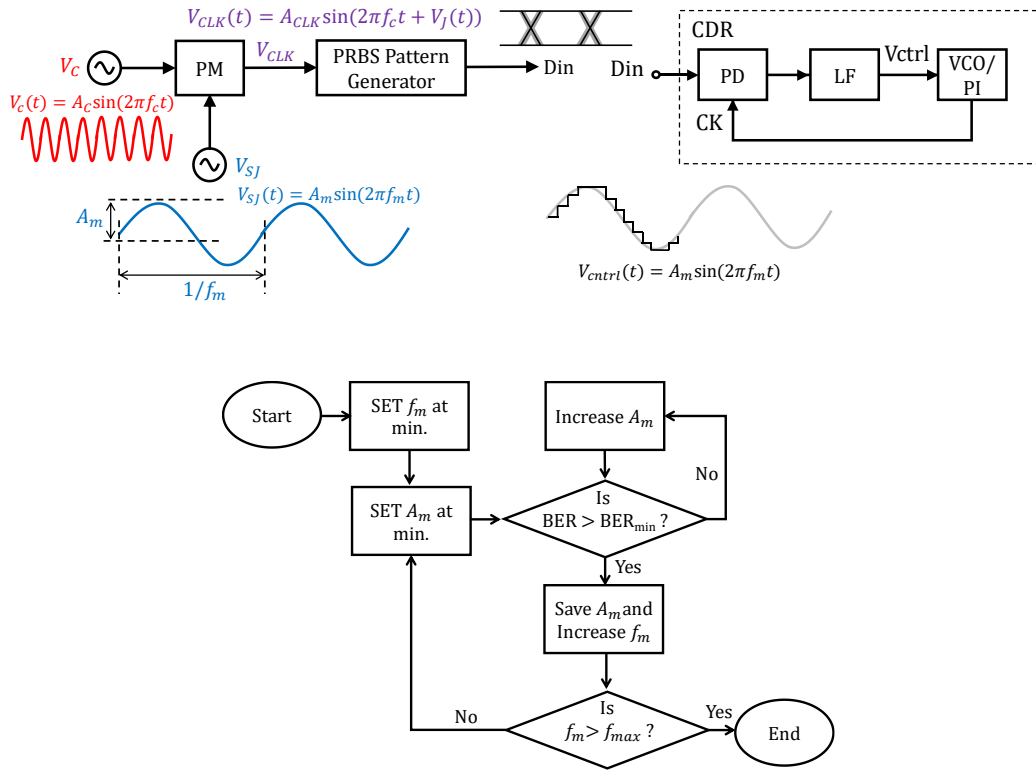


Figure 1.8: Setup illustrating the JTOL test implementation and the testing sequence

Substituting $H(s = j\omega)$ with its standard form for the second order loop, yields:

$$\phi_{in} < \frac{1}{2} \frac{s^2 + 2\zeta\omega_n s + \omega_n^2}{s^2} \text{UI} \quad (1.5)$$

Fig. 1.7 depicts the Jitter Tolerance curve for a CDR modelled as a standard second-order LTI system with the pole frequencies of $\omega_{p1} = 2\pi f_{p1}$ and $\omega_{p2} = 2\pi f_{p2}$ [8].

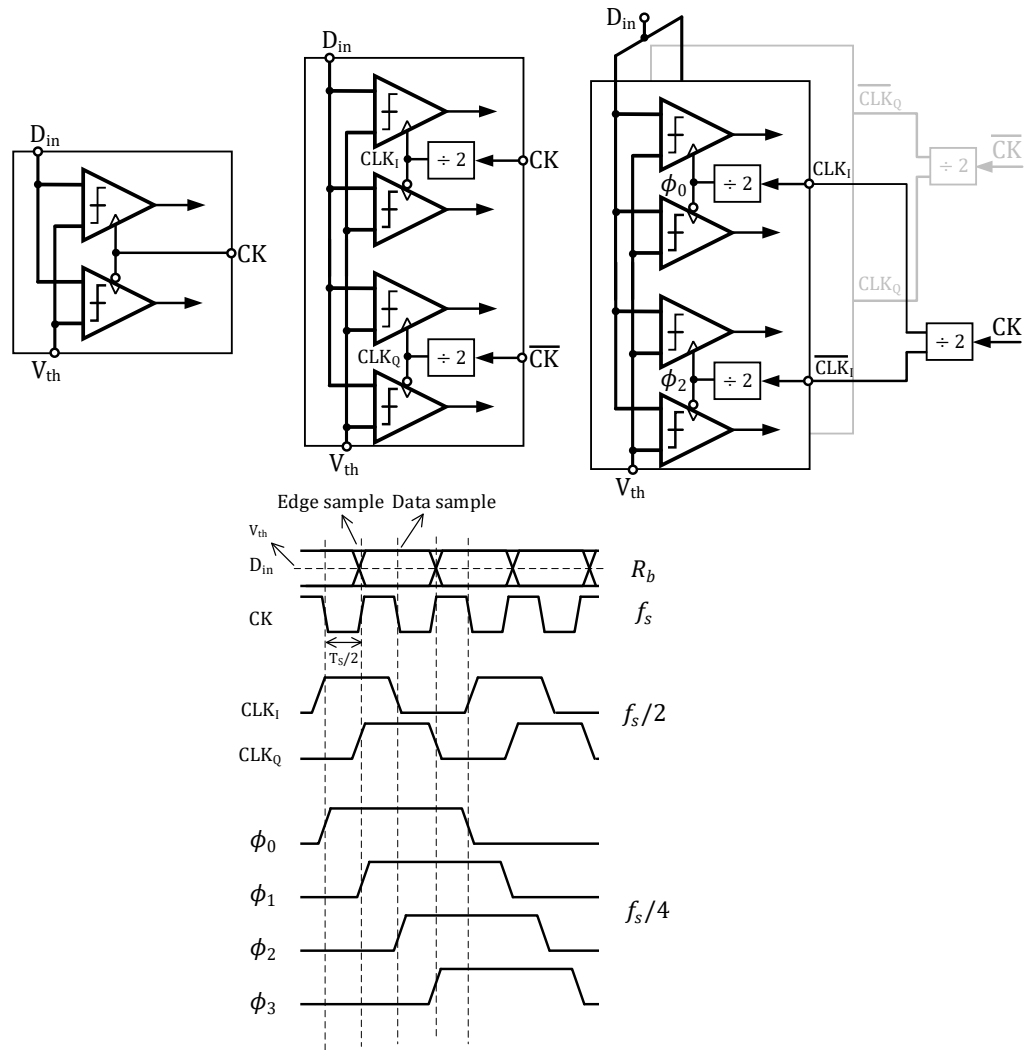


Figure 1.9: Time-interleaving can be used to increase the sampling rate and hence the input data rate, from left to right: Full rate, half rate and quarter rate CDR. Note that the CDR still takes 2 sample per bit (symbol).

The setup to measure the JTOL is shown in Fig. 1.8. wherein the pattern generator is clocked by a phase or frequency modulated signal modelling the input sinusoidal jitter. Like PLLs, the CDR can be regarded as a phase demodulator trying to extract the signal information (here sinusoidal jitter) from the carrier (data) transitions. Although the carrier lacks the periodicity, since the frequency of jitter is usually less than the data rate, even with high BER the CDR can follow the input phase. For this reason, unlike PLLs the ultimate indication of the true functionality is the output BER rather than the recovered phase.

1.3.4 High Speed CDRs

Physical implementation of the CDR system with a single sampler encounters numerous limitations when it operates at higher data rates. For example, in our design, the CDR specifications requires that the PD operates at 28GHz while the loop's update rate is set to the same value. This design may not be feasible in certain technologies and even so the power consumption of the resulting block would be enormous. As the desire for higher data rates grows with the advance of CMOS technology nodes the problem continues to manifest itself. To tackle this issue, we have to revise the CDR architecture to handle such scenarios.

The common approach [15], [18], [19] is to use interleaved PDs (parallel) which operate at lower clock w.r.t the input rate. By invoking such a method, architectures like half-rate or quarter-rate PDs can be realized⁵, Fig. 1.9. Due to the high frequency channel losses, the available swing at the input of the CDR is limited and detecting the data by using conventional CMOS flip-flops may not be feasible. For that reason the samplers are realized using CML logic or dynamic comparators with high input sensitivity to deal with relatively large vertical closure in the input's eye-diagram⁶.

1.4 Proposed PAM4 CDR

Our targeted CDR architecture [20] is shown in Fig. 1.10. The PR based CDR was chosen based on the top-level requirements of the transceiver because it would suit the multi-lane architecture in terms of area and compactness [16] since all the channels can share one PLL block for clock phase generation. Because the area is a concerning factor it is decided to use a digital loop filter and hence, a DPC based architecture. The CDR configuration for the PAM4 signal is almost identical to NRZ (PAM2) CDRs. The main difference is related to phase detection. The PD in PAM4 CDR has to deal with multi-level transitions. The combination of the available thresholds and corresponding transitions usually results in ignoring some edges hence affecting the CDR BW directly [see 2.1.1.1].

⁵It should be noted that the CDR would still be an oversampled CDR (two samples per UI), and should not be confused with the concept of baud rate CDRs which essentially take one sample per UI.

⁶An eye diagram or eye pattern is a common tool for visualisation of random data. It is constructed by segmenting the input data into shorter time intervals e.g. two symbols wide and overlapping them.

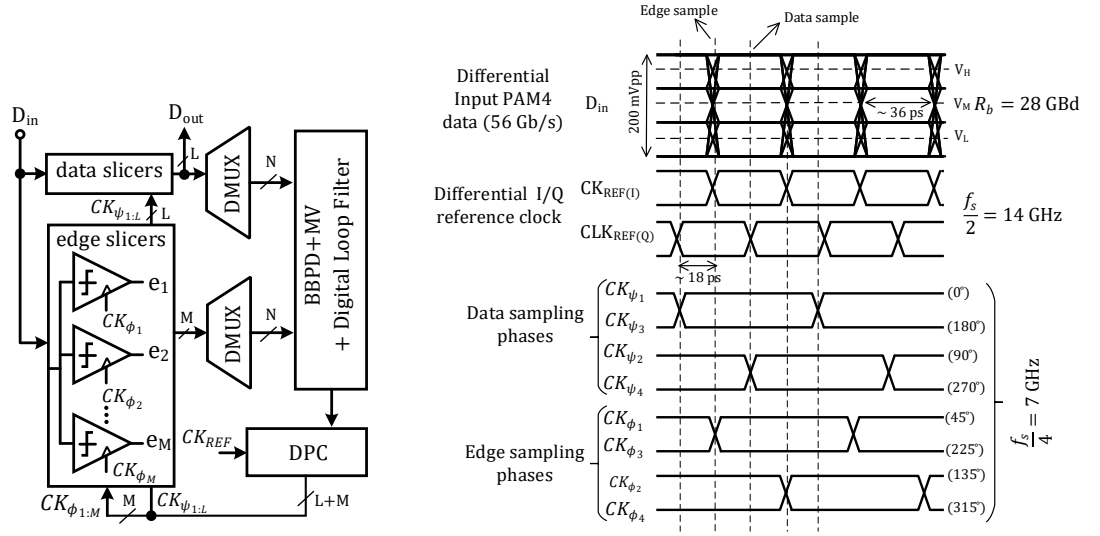


Figure 1.10: The block diagram of the selected architecture for the design of PAM4 CDR with the detailed input timing diagrams. Each slicer represents a bank of three comparators with their respective reference levels (V_L , V_M , V_H). The clock for the digital section is not shown.

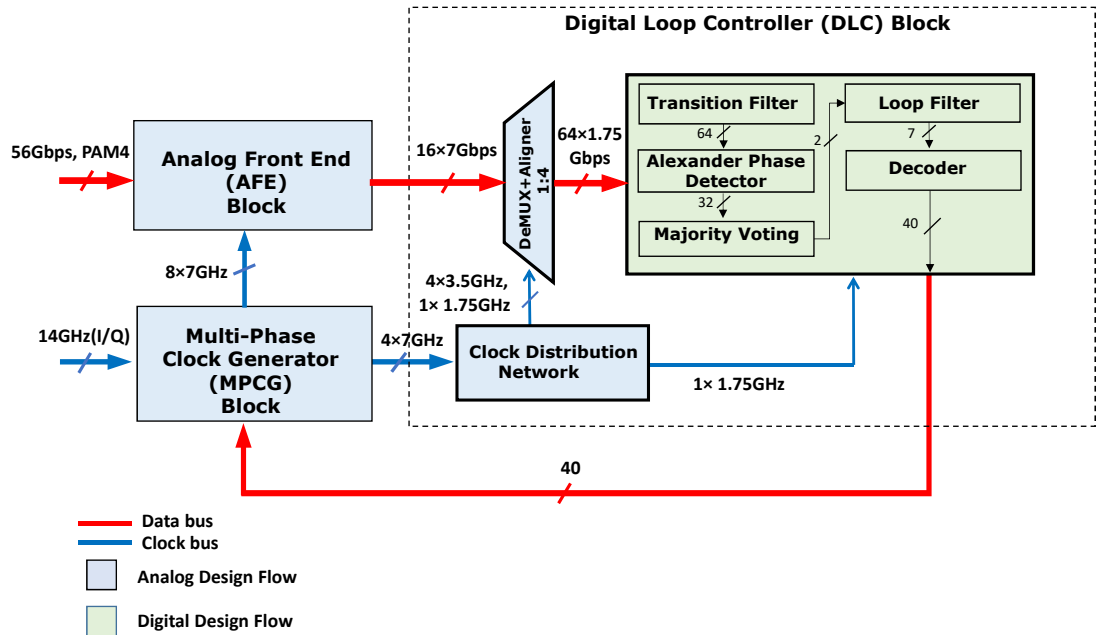


Figure 1.11: The detailed architecture of the proposed PAM4 CDR which consists of three main blocks: AFE, DLC and MPCG (DPC).

The CDR avails of time-interleaving, by de-multiplexing the input into $(M + L)$ different channels. The spacing between channels is $f_s/(M + L)$ wherein M and L are the number of edge and data sampling paths. Although it seems that increasing M and L indefinitely is possible however from the practical point of view the limitation on the number of phases, routing constraints including area

and timing delay or skew would be limiting factors in increasing the DEMUX ratio. The CDR front-end uses 8 channels ($M = L = 4$) with sampling frequency of 7 GHz to sample a 28 GBd PAM4 input. To implement the digital filter with the available standard cell library, the data rate at the output of the slicers (7 Gb/s) has to be reduced further by the factor of 4 using de-multiplexers. The CDR at the top level consists of three main building blocks: 1. Analog Front End (AFE) 2. Digital Loop Controller (DLC) and 3. Multi-Phase Clock Generator (MPCG) or Digital to Phase Converter (DPC) as shown in Fig. 1.11.

1.5 Design Methodology

The CDR has a complex operation and given the number of building blocks it requires a top-to-down design methodology. Such procedure involves multiple levels of abstractions in which certain design variables are considered.

At system level (Chapter 2) we only focus on parameters that describe the ideal CDR function in phase domain, this way the maximum expected performance is determined. For the system level design MATLAB/SIMULINK is used as the main simulation environment. Then the non-idealities from circuit level are modeled to investigate their impact on the CDR performance as explained in the end of Chapter 2.

The circuit level implementation (Chapter 3), prior to transistor-level design, requires to develop the voltage domain behavioral models of the blocks. Since the design includes both Analog and Digital components, for detailed architectural verification, Verilog A and Verilog (D) HDL are used in conjunction with the AMS design utility available in Cadence Virtuoso platform. At transistor level the circuit simulators for the Analog part is Spectre while the digital parts are mapped to standard cell libraries in 65 nm CMOS using RTL Compiler and the back-end place and routing is performed in SOC Encounter. Both tools are the products of Cadence Design Systems.

Fig. 1.11 also depicts the detailed CDR block diagram and the design flow chosen for implementation of the individual building blocks.

1.6 Chapter Summary

This Chapter laid out the research objectives behind the thesis. A brief introduction of the PAM4 signaling format and its advantages against the NRZ format was presented. The two major architectures (PR based or VCO based) in the category of PLL based CDRs are explained. The requirement of sharing a reference clock among multiple receiver channels combined with the area constraints made the PR based CDR the preferred choice for the purpose of this research. The incorporated design methodology is outlined which starts by focusing on CDR's system level (Chapter 2), identifying the sub-blocks specs and important circuit-level parameters and their impact on the CDR performance while the detail transistor level implementations is covered in Chapter 3.

Chapter 2

CDR's System Level Design

In this chapter we lay out the details of the PAM4 CDR architecture and describe the system level design. Individual building blocks including the PD, MV, LF and DPC are analysed and their behavioural models are extracted. Using these abstracted definitions, we can predict the dynamics of the CDR to meet certain design requirements. Such a top-down design approach allows us to narrow down the important variables' range for the circuit-level realization of each block. For example, using the LF parameters (K_P and K_I) the minimum register length i.e. the number of bits in the DLC section can be estimated. The DLC contains a delay due to the sequential nature of its operation. The influence of this delay N_d on the feedback loop is studied. The effects of AFE and MPCG (DPC) imperfections are inspected by the back annotation of circuit level non-idealities into the CDR system. This helps to determine the necessity for additional trimming or calibration procedures to amend the blocks functionalities hence improving the performance. We also propose a tri-level PD suitable for PAM4 data which enhances the trade-off between CDR bandwidth and systematic jitter generation when medium-level transitions are employed.

2.1 Phase Domain Modelling of the CDR

2.1.1 PAM4 PD

Multi-level signaling like PAM4 complicates the mechanism of phase detection and CDR due to the presence of multiple data transitions. As shown in Fig. 2.1 a PAM4 eye consists of six different non-return to zero (NRZ) eyes and the related transitions can be categorized as: a) small transitions from and to the

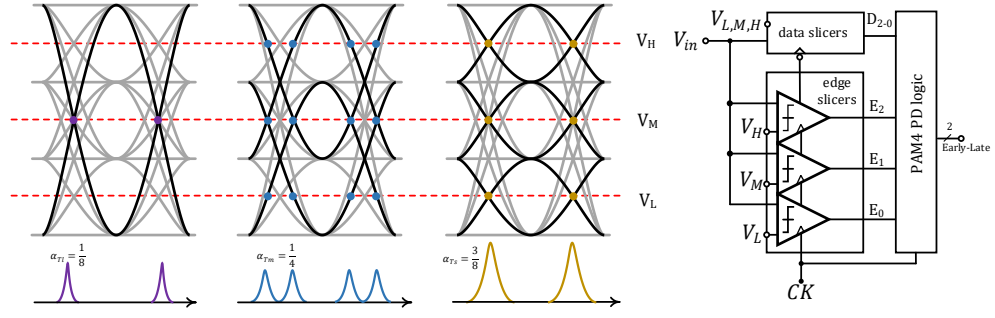


Figure 2.1: Decomposition of PAM4 eye diagram into three different NRZ eyes: large, medium and small transitions with threshold-crossing histograms formed by assuming random Gaussian jitter on the edges. Only edge samples are shown. The logic section contains PDs circuitry. Detailed block diagram is explained later.

adjacent data levels, forming the minimum height eyes in which only one slicer output state is involved at a time. b) medium transitions between every other data levels resulting in the mid-range eyes; the MSB and one of the LSB slicers states are flipped. c) large transitions associated with the maximum data swing where all the slicers states are toggled. In any PAM4 data pattern, out of 16 available data transitions, 12 transitions are between unequal data levels hence the maximum available transition density, α_T , is 0.75. In the case of a random pattern with equal probabilities for all data levels, the contribution from the small, medium and large transitions are $\alpha_{Ts} = \frac{6}{16} = 0.375$, $\alpha_{Tm} = \frac{4}{16} = 0.25$ and $\alpha_{Tl} = \frac{2}{16} = 0.125$, respectively. The Alexander phase detection method [12], also referred to as binary or bang-bang (BB), is one of the preferred choices to implement the PD block of CDRs in high-speed applications. In PAM4 CDRs when BBPDs are employed, usually the medium transitions are considered as idle [21], [19], [22], [23], [24], [25] since the data crossing points and the slicers' thresholds are not aligned with those of the small and large transitions Fig. 2.1. In other words, the thresholds are not located in the middle of the eyes. The phase detection based on a non-centered threshold gives rise to systematic data dependent jitter (DDJ). Such approaches compromise between the amount of systematic jitter generated in the loop and the available bandwidth, resulting in reduction of the latter by a factor equal to α_{Tm} .

In this section we present a tri-level PD which exhibits better functionality in handling medium transitions[26]. First the issues related to BBPD are investigated followed by an explanation of the proposed tri-level PD. Then the CDR equipped with the tri-level PD is analyzed. Although throughout this subsection we only concentrate on the PD block, it involves application of a simple and generic model of the CDR to better understand the tri-level PD advantages.

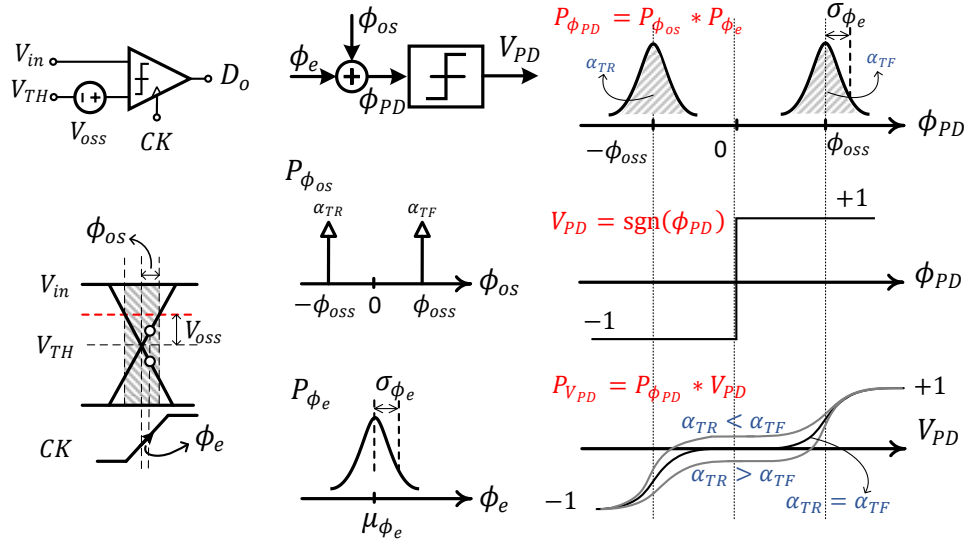


Figure 2.2: Effect of the slicer's threshold offset V_{os} during edge sampling: an edge sample depending on falling/rising data transition, can produce early or late output. Including V_{os} effect in BBPD's phase domain model, ϕ_e has Gaussian PDF while ϕ_{os} takes uniform distribution. The PD's input PDF is the convolution of the ϕ_e 's and ϕ_{os} 's PDFs. Likewise the PDF of the V_{PD} is the convolution of the PD's transfer characteristic (sign function) with its input. The vertical shift (specific to PAM4) is the function of the rising/falling edges density.

The complete PAM4 CDR system will be explained in the other sections.

2.1.1.1 BANG-BANG PHASE DETECTION OF PAM4 SIGNALS

The underlying mechanism for the jitter contribution can be elaborated by considering a simple case as follows. In Fig. 2.2 as slicers operate on both data rising and falling edges, in the presence of threshold offset, V_{OS} , an early clock for a rising edge is translated to a late clock for a falling edge and vice versa. Hence, depending on the edge type, the slicer's threshold offset results in opposite-sign phase errors. Assuming that data transitions are jittered by a random Gaussian noise with the mean of μ_{ϕ_e} and standard deviation of σ_{ϕ_e} , the effective input to output transfer can be obtained by sweeping μ_{ϕ_e} and calculating the PD's output average, $\overline{V_{PD}}$. This is equivalent to performing the convolution of the BBPD's phase transfer function and the input jitter's PDF [27]. As μ_{ϕ_e} takes values inside the interval specified by $\pm|\phi_{oss} - 2\sigma_{\phi_e}|$ ¹ considering $\sigma_{\phi_e} \leq \phi_{oss}/2$, over a long run the early-late outputs are nullified and $\overline{V_{PD}}$ falls to zero which manifest itself as a "dead zone" [Fig. 2.3] in the PDs characteristic [15], [16].

¹Although ϕ_{oss} may take any arbitrary value to model the slicer's offset effect, here it is defined based on PAM4 references levels, therefore it is calculated using equation Eqn. 2.4

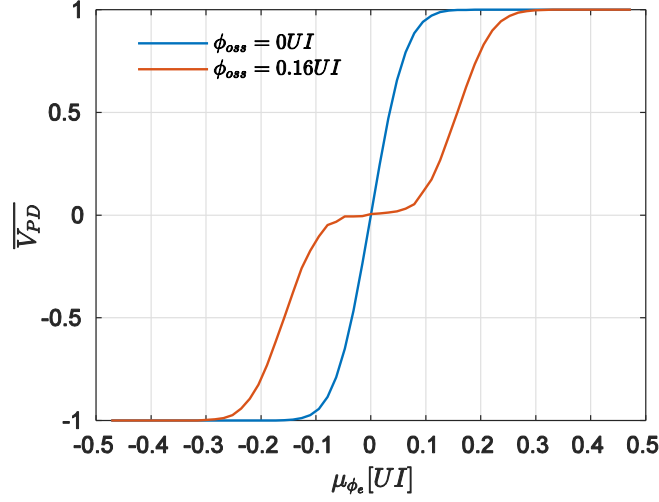


Figure 2.3: BBPD's average output vs input mean for $\sigma_{\phi_e} = 100$ mUI while $\alpha_{TR} = \alpha_{TF} = 0.5$, in the presence of the offset a dead zone emerges in the characteristic.

As shown in Fig. 2.2 such non-ideality in the phase domain can be modeled by adding an error source ², ϕ_{oss} , to the input of the PD with a PDF consisting of two impulses at $\pm\phi_{oss}$ while the weights α_{TR} and α_{TF} are the transition density of the respective rising and falling edges³. The PD's model is instantiated in a CDR loop as depicted in Fig. 2.4.

Depending on the application, CDRs conventionally are realized as either VCO-based or PI-based architectures. Nevertheless, as long as the typical loop dynamics are concerned the system-level-block diagrams are mostly similar. Therefore, we base the analysis on a generic behavioral model which is a discrete time, phase domain model of the CDR. For the loop filter, $H(z^{-1})$ we have:

$$H(z^{-1}) = \frac{K_P(1 - z^{-1}) + K_I}{(1 - z^{-1})^2} z^{-N_d} \quad (2.1)$$

K_P and $K_I (= K_P/T_n)$ are proportional and integral paths gains whereas T_n is the integral path time constant and N_d represents the delay around the loop. A random binary sequence, V_{TD} , is inserted to take into account the effect of α_{TF} . In addition, for the sake of simplicity, the other sources of jitter in the loop including phase noise of the VCO or quantization noise of the PI are ignored. This approximation would not lead to contradictory results since in BBPD based

²The PDF for the sum of two statistically independent variables is the convolution of the PDFs of the two individual variables.

³ α_{TR} and α_{TF} are defined based on available rising and falling transitions i.e. $\alpha_{TR} + \alpha_{TF} = 1$ and should not be confused with the overall transition densities like α_T , α_{TL} , α_{Tm} and α_{Ts} .

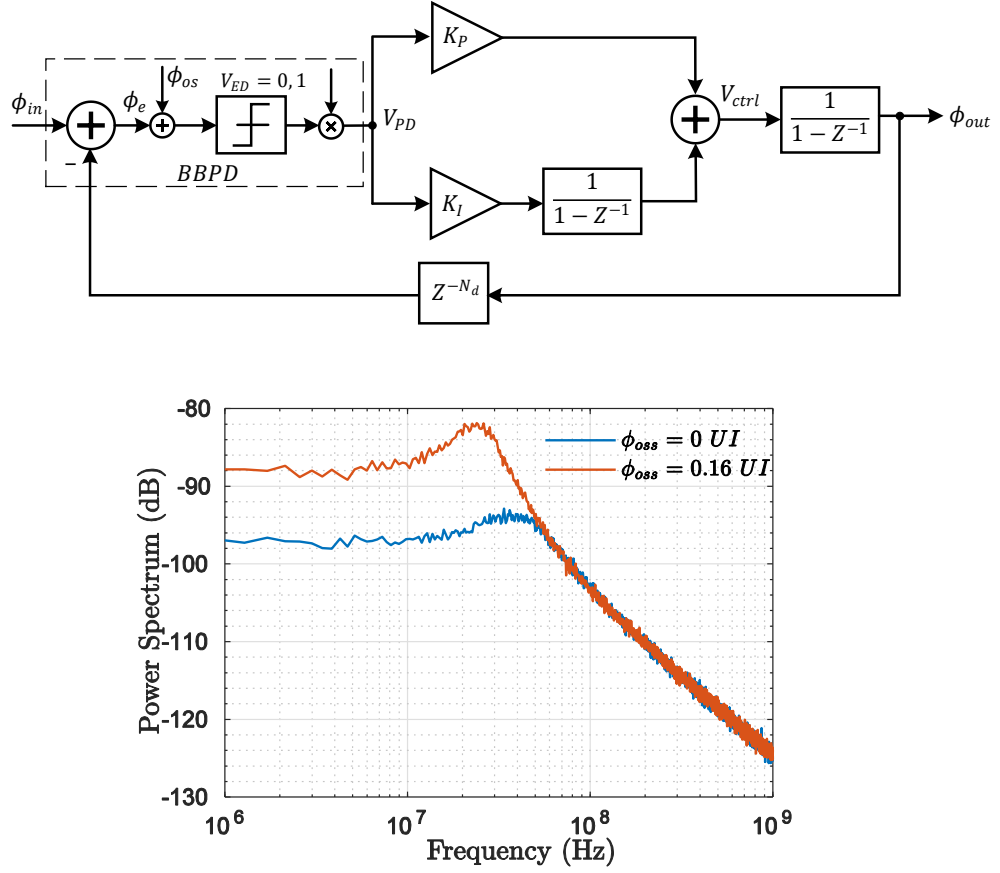


Figure 2.4: (Top) Simplified conventional CDR loop based on BBPD, V_{TD} is to add the transition effects. The loop filter, includes proportional and integral paths. (Bottom) PSD of ϕ_{out} with and without offset. The input is a white Gaussian noise with $\sigma_{\phi_{in}} = 100 \text{ mUI}$ ($\approx -105 \text{ dB/Hz}$) and $\alpha_T = 0.25$. Default loop parameters are: $K_P = 5 \text{ mUI}$, $T_n = 100$ and $N_d = 1$.

CDRs the input data and the PD are the dominant sources of jitter. Now we can postulate that for non-zero ϕ_{os} , near the flat zone, the effective loop gain starts to drop, consequently ϕ_{out} would wander unconstrained. This condition, which enhances the jitter generated in the loop, is evident from the power spectrum density (PSD) which is generated by taking FFT of ϕ_{out} in Fig. 2.4.

It should be noted that PAM4 signaling may exacerbate this situation as in worst case with the lack of a proper scrambling the data pattern may favor one medium rising or falling edge over another one⁴. Therefore, the resulting phase shift [Fig. 2.5] would oppose the PD's output from small/large transitions and such disturbances introduce stronger DDJ.

⁴One deterministic example of such PAM4 pattern could be a repeated sequence of symbols like $[012310 \dots]$ in which only one type of medium transitions happens.

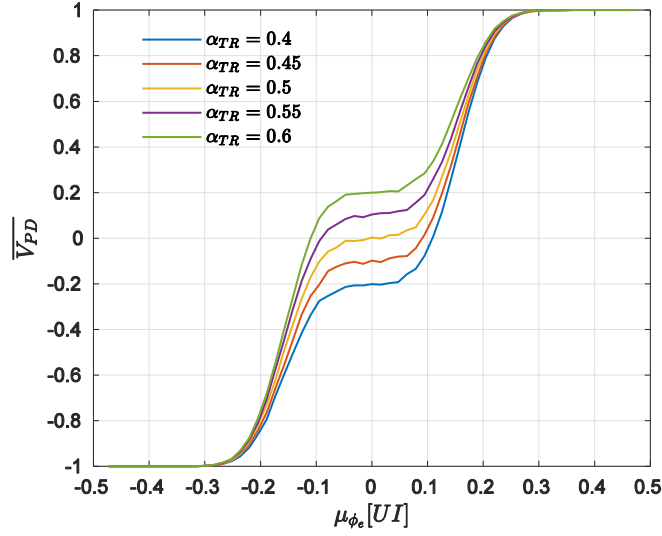


Figure 2.5: The variation in the average value of the PD's output as the number of falling and rising edges for the medium transitions deviates from the ideal value (0.5) in the absence of proper PAM4 scrambling.

2.1.1.2 TRI-LEVEL PAM4 PD

Further inspection of the eye diagrams in Fig. 2.1 reveals that, even though the thresholds for the middle eyes are not centered, as there are two edge samples per transition, the position of the clock may be determined more accurately by looking at the output of the two slicers simultaneously. Particularly, the samples before and after the thresholds still can be interpreted as an early or a late with respect to the middle crossing point regardless of their edge types. This is akin to performing Alexander phase detection on two-bit samples rather than single-bit values. This way the regions with conflicting outputs can be identified. As shown in Fig. 2.6, when the samples are between the two thresholds i.e. near the data crossing point, the results are not valid and the output should be discarded⁵.

With the mentioned modification, the PD exhibits a tri-level characteristic as depicted in Fig. 2.7(a) which may be described by $V_{PD} = 0.5(\text{sgn}(\phi_e + \phi_{oss}) + \text{sgn}(\phi_e - \phi_{oss}))$. For $|\phi_e| \leq \phi_{oss}$, the tri-level PD's output is zero thus would not fight with the other BBPD outputs in defining the final locking position, alleviating the aforementioned DDJ issue. However in the case that $|\phi_e| > \phi_{oss}$ the active output increases the effective gain of PD by a factor proportional to α_{Tm} i.e. the configuration enhances the loop bandwidth for samples far from

⁵Additional logic is required to distinguish medium transitions from those large/small ones based on the data samples; this part is discussed later on in this section

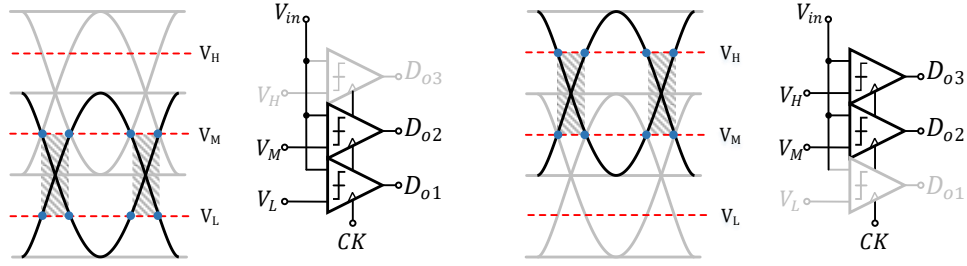


Figure 2.6: The samples taken outside of the shaded area can be used for the correct generation of early/late signals by looking at the output of the corresponding slicers simultaneously.

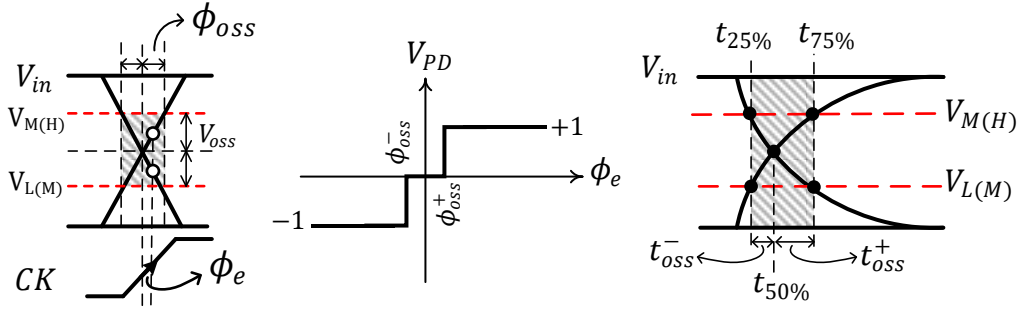


Figure 2.7: (left) Tri-level PD operation concept and the phase domain characteristic, the PD does not generate any output for $|\phi_e| < \phi_{oss}$. (right) calculation of ϕ_{oss} for the input shaped by the channel response.

the centers, for instance during initial phase acquisition or when the input data contains large amplitude jitter.

To determine the value for ϕ_{oss} we assume that the data channel's frequency response is in the form of a single-pole network with the bandwidth of f_{3dB} . As depicted in the Fig. 2.7(b), in each medium transition, two slicers are involved, therefore the phase offsets are calculated based on the time difference, t_{oss} , between the actual threshold crossings and mid-crossing points, denoted by $t_{25\%}$, $t_{75\%}$ and $t_{50\%}$ respectively. Since the normalized step response of the channel modeled by the single-pole network takes the form of $[1 - e^{(-2\pi f_{3dB}t)}]$ we can express t_{oss}^+ , t_{oss}^- as:

$$t_{oss}^+ = t_{75\%} - t_{50\%} = \frac{\ln(2)}{2\pi f_{3dB}} \quad (2.2)$$

$$t_{oss}^- = t_{25\%} - t_{50\%} = -\frac{\ln(1.5)}{2\pi f_{3dB}} \quad (2.3)$$

and for ϕ_{oss}^+ and ϕ_{oss}^- :

$$\phi_{oss}^+ = 2\pi R_b t_{oss}^+ = \ln(2) \frac{R_b}{f_{3dB}} \quad (2.4)$$

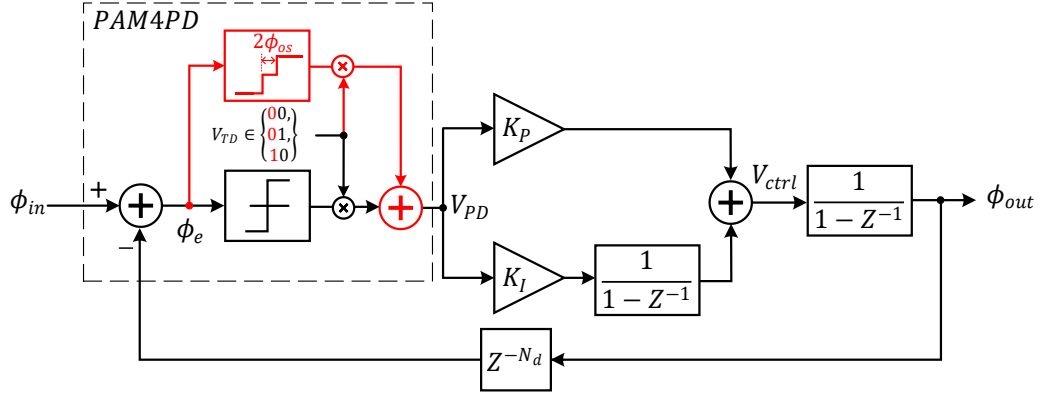


Figure 2.8: Block diagram of the CDR, the Tri-Level PD is in parallel with the BBPD which is used for the large and small transitions, V_{TD} is used to model the transition effects.

$$\phi_{oss}^- = 2\pi R_b t_{oss}^- = -\ln(1.5) \frac{R_b}{f_{3dB}} \quad (2.5)$$

wherein R_b refers to input baud rate. Usually an optimal value for f_{3dB} minimizes the inter symbol interference (ISI) by increasing f_{3dB} while keeping the signal to noise ratio (SNR) high enough to achieve the targeted bit error rate (BER). We choose $f_{3dB} = 0.7R_b$ [8] hence:

$$\phi_{oss}^+ = 0.99 \text{ rad} \approx 160 \text{ mUI} \quad (2.6)$$

$$\phi_{oss}^- = -0.58 \text{ rad} \approx -92 \text{ mUI} \quad (2.7)$$

Although unequal phase offsets make the tri-level PD's transfer asymmetrical, since the actual position of the lock is decided by the small and large transitions this would not be an issue for the true CDR operation. For simplicity the maximum value (160m UI) is used for both of ϕ_{oss}^+ and ϕ_{oss}^- . The tri-level PD model can be inserted inside the CDR loop in parallel with BBPD block for the small and large transitions, Fig. 2.8.

2.1.1.3 CDR WITH TRI-LEVEL PD

2.1.1.4 Jitter Transfer and Jitter Generation Analysis

Now we wish to examine the effect of the conditioned middle transitions on the CDR's jitter transfer function (JTRAN) and jitter generation (JG) merits. Employing the bang-bang and the tri-level PDs render the CDR block a nonlinear system therefore its behavior cannot be predicted readily. However, with suffi-

cient jitter present in the system and providing that the PD is not overloaded⁶, it is possible to invoke an equivalent linear model to simplify the analysis. For the BBPD the gain K_{PDsl} can be extracted by calculating $d(E[\mu_{sl}])/d\mu_e$ equivalent to the slope of the graph in Fig. 2.3. Using the provided analysis in [28], [29] the linearized gain and quantization noise variance, σ_{qsl}^2 , are:

$$K_{PDsl} = \sqrt{\frac{2}{\pi}} \frac{\alpha_{Tsl}}{\sigma_e} \quad (2.8)$$

$$\sigma_{qsl}^2 = \alpha_{Tsl} - \frac{2}{\pi} \alpha_{Tsl}^2 \quad (2.9)$$

wherein α_{Tsl} is the combined transition density for the large and small transitions.

For the tri-level PD, we resort to the same procedure as in [28] and [29], however with a subtle difference that the probabilities are calculated over truncated intervals. $E[\mu_m]$, the expected value (average) of the output μ_m , is the difference between the probabilities of the output being late or early hence:

$$E[\mu_m] = \alpha_{Tm}(P(\mu_m = 1) - P(\mu_m = -1)) \quad (2.10)$$

$$P(\mu_m = 1) = \int_{\phi_{oss}}^{+\infty} f_e(\phi_e) d\phi_e \quad (2.11)$$

$$P(\mu_m = -1) = \int_{-\infty}^{-\phi_{oss}} f_e(\phi_e) d\phi_e \quad (2.12)$$

while f_e is the PDF of ϕ_e and α_{Tm} is the associated transition densities for medium edges. Obtaining the gain:

$$\begin{aligned} K_{PDm} &= \frac{dE[\mu_m]}{d\mu_m} \\ &= \frac{\alpha_{Tm}}{\sigma_e \sqrt{2\pi}} (e^{-\left(\frac{\phi_{oss}-\mu_e}{\sigma_e \sqrt{2}}\right)^2} + e^{-\left(\frac{-\phi_{oss}-\mu_e}{\sigma_e \sqrt{2}}\right)^2}) \end{aligned} \quad (2.13)$$

Since in a locked CDR loop $\mu_e = 0$, it simplifies Eqn. 2.13 as:

$$K_{PDm} = \sqrt{\frac{2}{\pi}} \frac{\alpha_{Tm}}{\sigma_e} e^{-\left(\frac{\phi_{oss}}{\sigma_e \sqrt{2}}\right)^2} \quad (2.14)$$

If $\kappa = e^{-\left(\phi_{oss}/\sigma_e \sqrt{2}\right)^2}$, K_{PDm} and K_{PDsl} are related as follows:

$$K_{PDm} = \left(\frac{\sigma_{Tm}}{\sigma_{Tsl}}\right) \kappa K_{PDsl} \quad (2.15)$$

⁶A condition in which ϕ_{out} starts to slew.

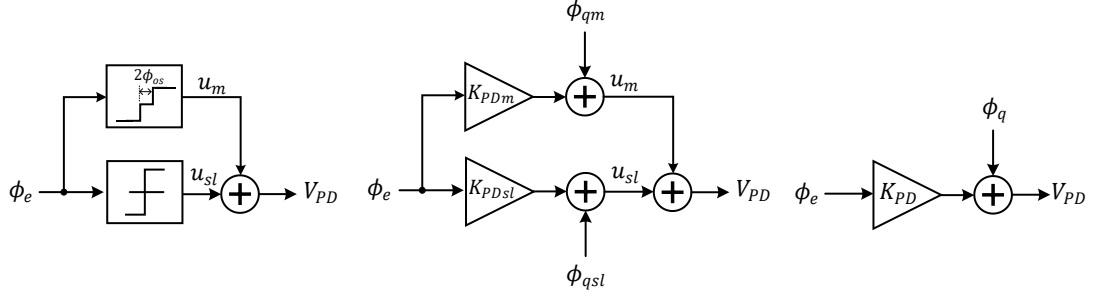


Figure 2.9: Steps for driving a combined linear model for BB and tri-level PDs, the effect of V_{TD} is included in K_{PD}

which indicates that $\kappa = 1$ for $\phi_{oss} = 0$ and the tri-level PD resembles a BBPD. To complete the model, the variance of ϕ_{qm} needs to be estimated:

$$\begin{aligned}\sigma_{qm}^2 &= E[\phi_{qm}^2] = E[(\mu_m - K_{PDm}\phi_e)^2] \\ &= E[(\mu_m)^2] + K_{PDm}^2\sigma_e^2 - 2K_{PDm}E[\mu_m\phi_e]\end{aligned}\quad (2.16)$$

In case of BBPD the output can take ± 1 or 0 when there is no transition, implying that the output variance (power) would be equal to α_{Tsl} . However, for the tri-level PD, 0 may also indicate that the input phase is in a certain interval as well, so we expect reduction in the output variance from α_{Tm} . The output variance $E[\mu_m^2]$ becomes:

$$\begin{aligned}E[(\mu_m)^2] &= 2\alpha_{Tm} \int_{\phi_{oss}}^{+\infty} f_e(\phi_e) d\phi_e \\ &= \alpha_{Tm} (1 - \text{erf}(\frac{\phi_{oss}}{\sigma_e\sqrt{2}}))\end{aligned}\quad (2.17)$$

in which $\text{erf}(\cdot)$ is the error function and for $E[\mu_m \cdot \phi_e]$ we have:

$$E[\mu_m\phi_e] = \sqrt{\frac{2}{\pi}} \alpha_{Tm} \sigma_e \kappa \quad (2.18)$$

Substituting Eqn. 2.17 and Eqn. 2.18 in Eqn. 2.16 yields:

$$\sigma_{qm}^2 = \alpha_{Tm} (1 - \text{erf}(\frac{\phi_{oss}}{\sigma_e\sqrt{2}})) - \frac{2}{\pi} \alpha_{Tm}^2 \kappa^2 \quad (2.19)$$

To build a final model for the modified PAM4 PD the linearized blocks have to

be combined, Fig. 2.9. The total gain, K_{PD} , is:

$$K_{PD} = K_{PDsl} + K_{PDm} = \sqrt{\frac{2}{\pi}} \frac{1}{\sigma_e} (\alpha_{Tsl} + \alpha_{Tm} \kappa) \quad (2.20)$$

For the total quantization noise σ_q note that as the blocks share the same input, their outputs are fully correlated. The jitter variance at the output of K_{PD} is:

$$\sigma_{V_{PD}}^2 = \sigma_e^2 (K_{PDsl}^2 + K_{PDm}^2) + 2\sigma_e^2 K_{PDm} K_{PDsl} \quad (2.21)$$

to compensate for the effect of the positive correlation factor the last term is deducted from the combination of σ_{qm}^2 and σ_{qsl}^2 :

$$\sigma_q^2 = \sigma_{qsl}^2 + \sigma_{qm}^2 - 2\sigma_e^2 K_{PDm} K_{PDsl} \quad (2.22)$$

yielding:

$$\sigma_q^2 = \sigma_{qsl}^2 + \sigma_{qm}^2 - \frac{4\kappa}{\pi} \alpha_{Tsl} \alpha_{Tm} \quad (2.23)$$

We utilize the forgoing PD model to analyze PAM4CDR dynamics while bearing in mind that this model is made under the assumption that ϕ_{in} is dominated by random components. Because the only noise source inside the loop is the quantization noise of the PD, the error signal at the input of the PD, ϕ_e , becomes:

$$\phi_e = \frac{1}{1 + K_{PD}H(z^{-1})} \phi_{in} - \frac{H(z^{-1})}{1 + K_{PD}H(z^{-1})} \phi_q \quad (2.24)$$

The PSD of ϕ_e , $S_{\phi_e}(f)$, can be determined as:

$$\begin{aligned} S_{\phi_e}(f) = & \left| \frac{1}{1 + K_{PD}H(f)} \right|^2 S_{\phi_{in}}(f) \\ & + \left| \frac{H(f)}{1 + K_{PD}H(f)} \right|^2 S_{\phi_q}(f) \end{aligned} \quad (2.25)$$

integrating $S_{\phi_e}(f)$ over the CDR's sampling bandwidth, $B = 0.5R_b$, results in:

$$\sigma_e^2 = \int_B S_{\phi_e}(f) df \quad (2.26)$$

Due to the feedback σ_e^2 , K_{PD} and σ_q^2 all are interdependent parameters and solving the described system of equations necessitates iterations. This is identical to implementing a system that adapts the gain and quantization noise while the CDR loop tries to minimize σ_e for a given σ_{in} and $H(z^{-1})$. When convergence is achieved, the system resembles the linearized equivalent of the

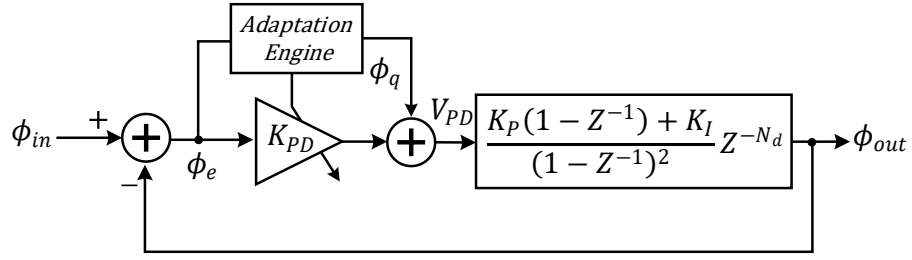


Figure 2.10: Combination of the CDR and an adaptation engine based on equations (8), (9) and (10). When the adaption engine achieves convergence the output resembles the response of the linearized system.

nonlinear CDR, Fig. 2.10.

To verify our analysis, multiple simulations with the nonlinear system and the equivalent linear model are performed. Fig. 2.11 illustrates the results and the comparisons under different loop parameters and inputs. By availing of the linearized model, the jitter transfer of the PAM4 CDR is obtained:

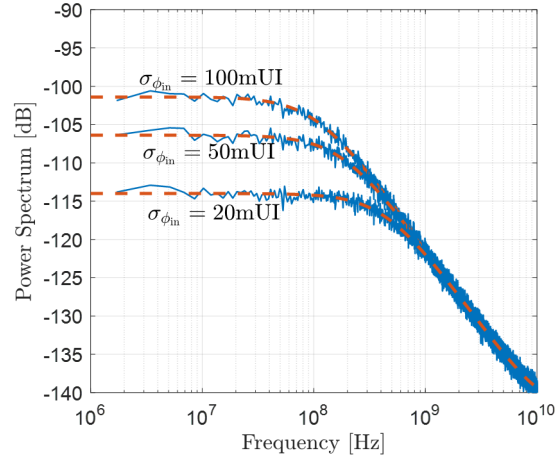
$$H_{JTRAN}(f) = \frac{K_{PD}H(f)}{1 + K_{PD}H(f)} \quad (2.27)$$

$$H(f) = \frac{K_P(1 - e^{-j2\pi f T_s}) + K_I}{(1 - e^{-j2\pi f T_s})^2} e^{-j2\pi f N_d T_s} \quad (2.28)$$

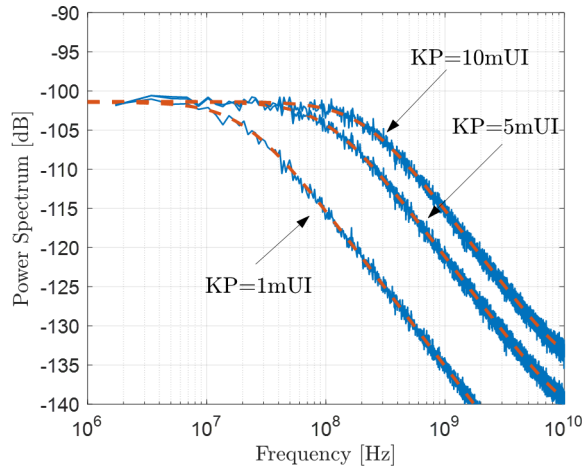
in which T_s is the period of the sampling clock⁷. As the input jitter RMS value, σ_{in} , approaches some fraction of ϕ_{oss} the modification in the PD comes into effect, which increases K_{PD} which, in turn, increases the loop gain and the bandwidth Fig. 2.12. Under low transition density, especially in the absence of enough small and large transitions (low α_{Tsl}) the PD can update the loop within shorter intervals providing stronger feedback.

Using Eqn. 2.27 and Eqn. 2.28 H_{JTRAN} has been illustrated in Fig. 2.13 for different value of α_{Tsl} . As can be seen, activating the tri-level PD enhances the loop bandwidth and this improvement is more evident when there are not enough small/large transitions available in the input data stream. This way the dependency of the loop on transition density variations and sensitivity to specific data patterns reduces, so does the value of DDJ. The linearized model also facilitates evaluating the contribution of the PD's quantization noise at the output. By rearranging Eqn. 2.25 the output power spectrum, $S_{\phi_{out}(f)}$, can be

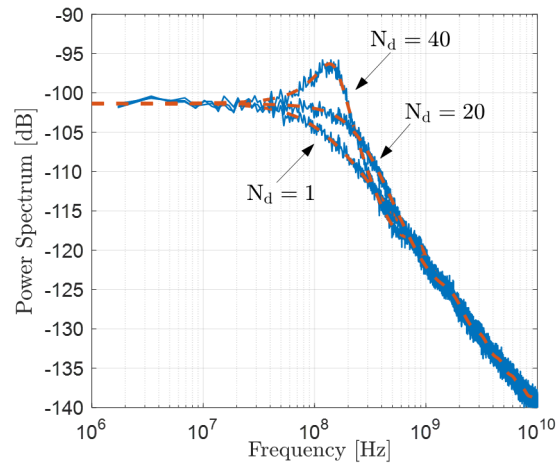
⁷In our simulations we have used $T_s = R_b^{-1}$ and $R_b = 28$ GBaud.



(a)



(b)



(c)

Figure 2.11: Comparison of CDR's output spectrum ($S_{\phi_{out}}$) for nonlinear(solid lines) and linearized models(dashed lines) for different value of (a) $\sigma_{\phi_{in}}$ (b) K_P and (c) N_d . In each case default parameters are $\sigma_{\phi_{in}} = 100$ mUI, $\alpha_{Tm} = 0.25$, $\alpha_{Tsl} = 0.5$, $K_P = 5$ mUI, $T_n = 100$ and $N_d = 1$.

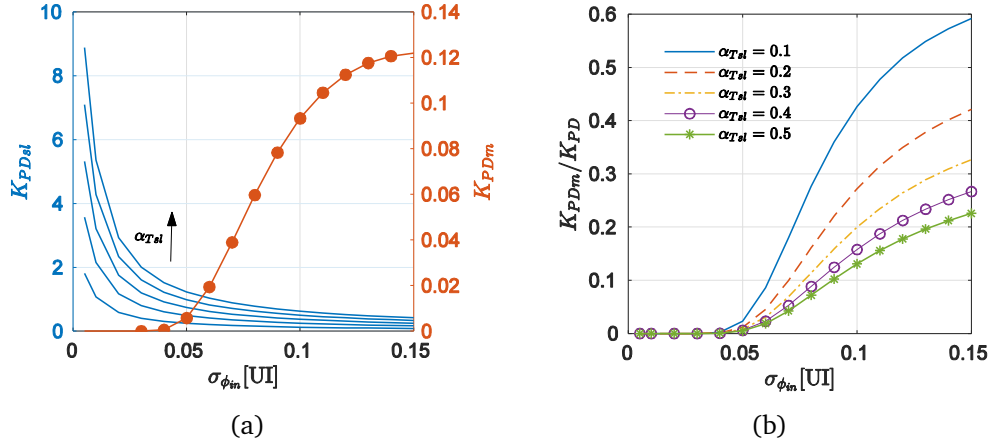


Figure 2.12: (a) As the input jitter increases the reduction in overall gain can be compensated by K_{PDm} , (b) the effect is more pronounced at lower α_{Tsl} while $\alpha_{Tm} = 0.25$, default parameters $K_P = 5$ mUI, $T_n = 100$ and $N_d = 1$.

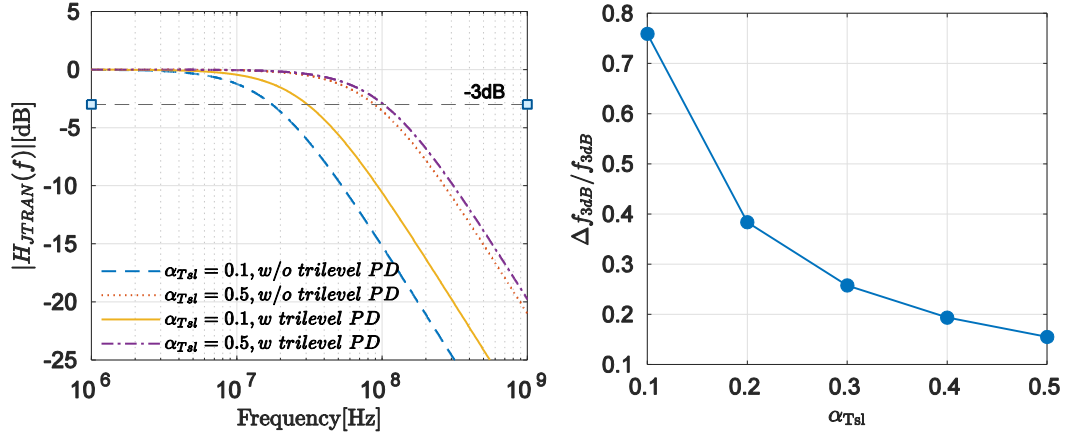


Figure 2.13: (left) Jitter transfer, H_{JTRAN} of the CDR with and without tri-level PD for different α_{Tsl} settings (right) Relative bandwidth improvement when the tri-level operation is activated. Default parameters are $\sigma_{\phi_{in}} = 100$ mUI, $\alpha_{Tm} = 0.25$, $K_P = 5$ mUI, $T_n = 100$ and $N_d = 1$.

written as:

$$S_{\phi_{out}}(f) = |H_{JTRAN}(f)|^2 S_{\phi_{in}}(f) + \left| \frac{H_{JTRAN}(f)}{K_{PD}} \right|^2 S_{\phi_q}(f) \quad (2.29)$$

the second term in the right side of Eqn. 2.29 is the jitter generated in the loop, $S_{\phi_{out,q}}$. As shown in Fig. 2.14 enabling tri-level PD, benefits from the inverse relation between $S_{\phi_{out,q}}$ and K_{PD} .

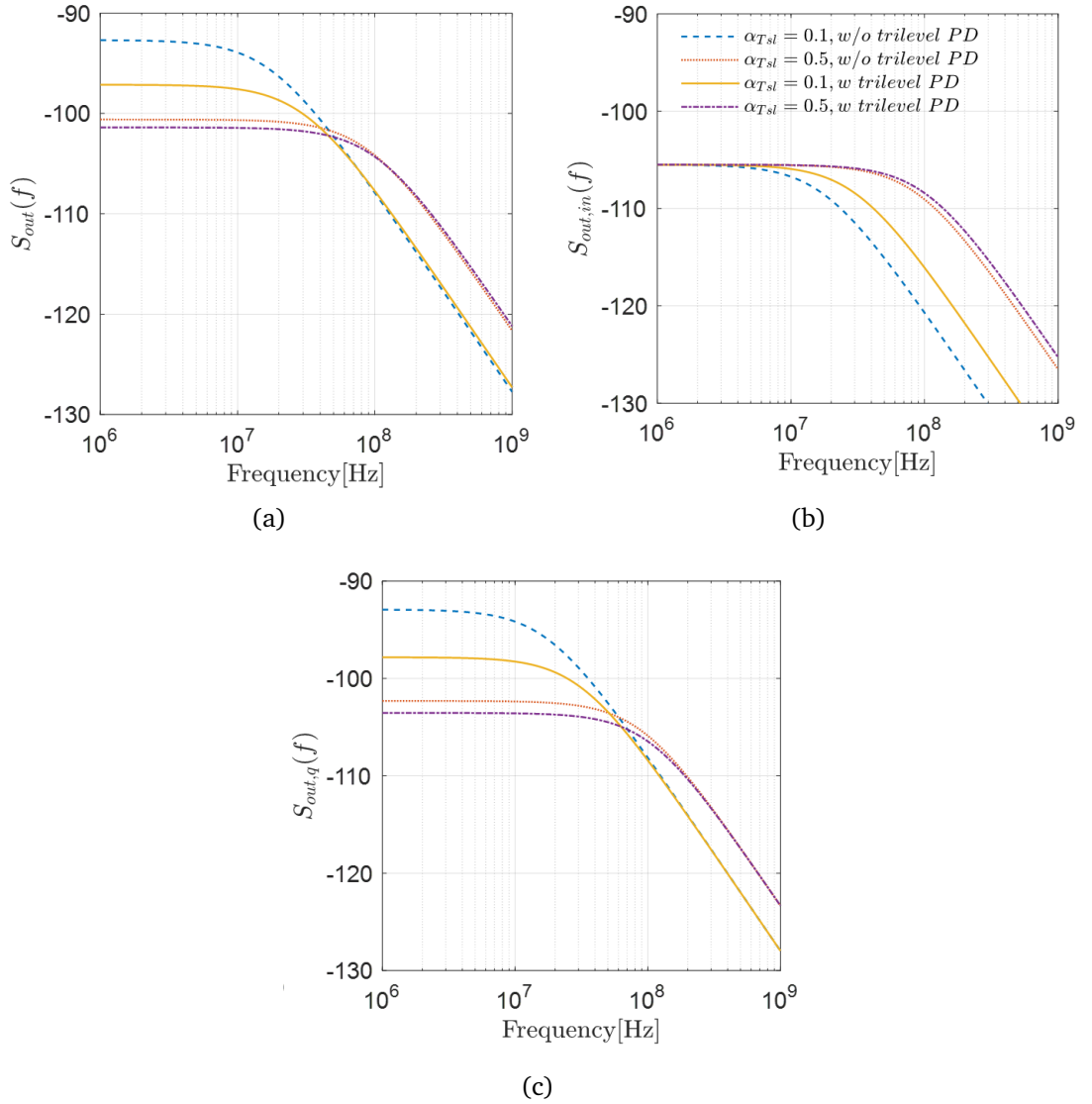


Figure 2.14: Decomposition of (a) $S_{\phi_{out}}$ to (b) $S_{\phi_{out,in}}$ and (c) $S_{\phi_{out,q}}$, shows the effect of activating tri-level PD on the jitter transmission and generation within CDR's loop with the same parameters settings as in Fig. 2.13

2.1.1.5 Jitter Tolerance Analysis

For the jitter tolerance analysis (JTOL), the CDR input is stimulated with a sinusoidal signal and at each frequency point the amplitude is increased until ϕ_e exceeds a margin defined by the BER requirements. We designate the maximum available value for ϕ_e which is 0.5 UI or π rad. In the jitter tolerance test environment, the amplitude of the sinusoidal jitter usually exceeds the RMS value of the random jitter and when the PD's input is overloaded by a large jitter amplitude the output phase starts to slew i.e. the loop is intentionally driven out of the linear regime and the linear model cannot be incorporated

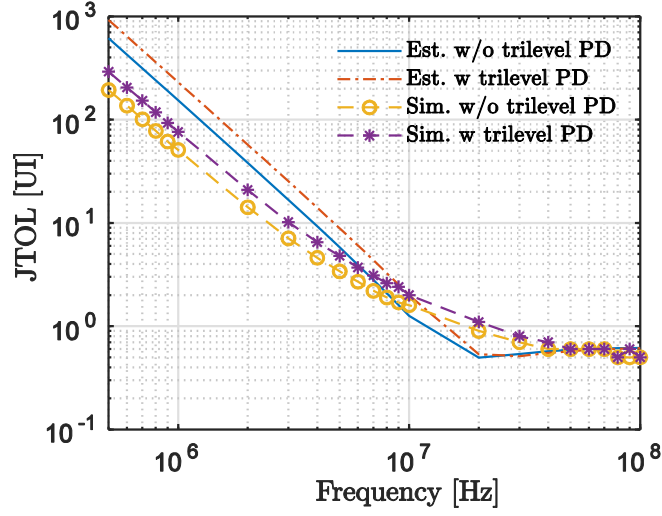


Figure 2.15: JTOL results for the CDR with/without Tri-level PD, Default parameters are $\sigma_{\phi_{in}} = 10$ mUI, $\alpha_{Tsl} = 0.5$, $\alpha_{Tm} = 0.25$, $K_P = 5$ mUI, $T_n = 100$ and $N_d = 1$.

here. Instead, we proceed with the described method in [27] which estimates the JTOL for a slewing loop.

Although in [27] the loop parameters are based on the continuous approximation of the VCO based CDR, by means of the backward difference substitution [15] the equations can be mapped to our discrete time model. Ignoring the effect of N_d , the jitter tolerance for $f \geq 0.315(K_I/T_s K_P)$ is derived:

$$H_{JTOL}(f) = \pi \sqrt{1 + \left(\frac{K_P}{4\pi f T_s}\right)^2 (\alpha_{Tsl} + \alpha_{Tm})^2} \quad (2.30)$$

and for low jitter frequencies we arrive at:

$$H_{JTOL}(f) \approx 0.08 K_I (\alpha_{Tsl} + \alpha_{Tm}) \left(\frac{1}{f T_s}\right)^2 \quad (2.31)$$

The simulation results are illustrated in Fig. 2.15. Despite the overestimated values made by Eqn. 2.31 the JTOL relatively improves by a factor close to $1 + \alpha_m/\alpha_{Tsl}$ when K_{PDm} is enabled. This was expected as the tolerable jitter amplitude in the moderate frequency range is well above ϕ_{oss} , meaning that the Tri-level PD regularly updates the loop.

2.1.1.6 Hardware Implementation of Tri-level PD

In general, performing PAM4 phase detection mandates extra logical operations due to the presence of the multiple transitions. Fig. 2.16 shows the required

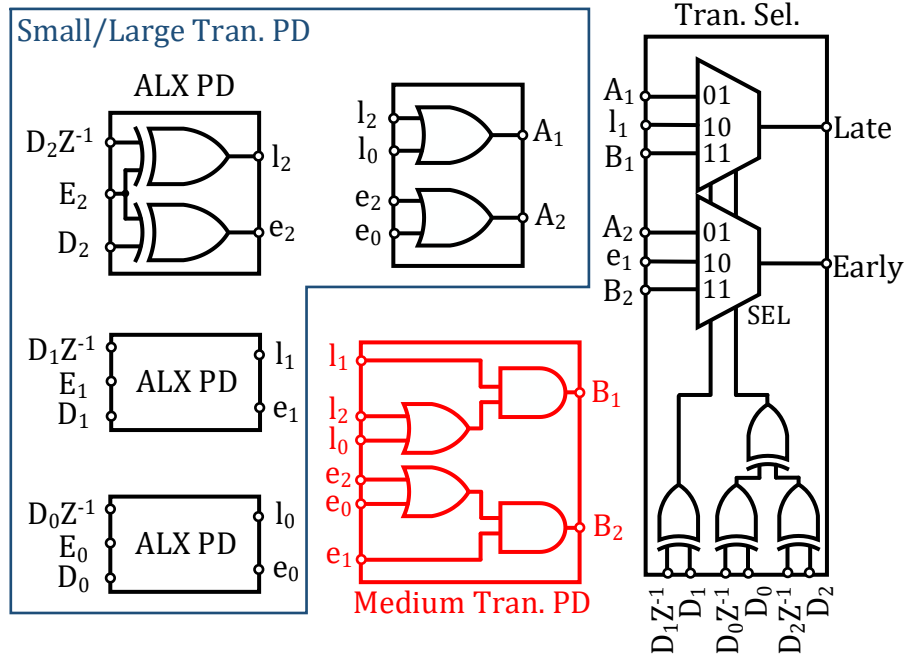


Figure 2.16: Logic circuits to implement the conventional BBPD (black) for PAM4 CDR, inclusion of Tri-level PD (red) by addition of extra gates

logic circuit to implement the conventional PAM4 PD. The transition selector/-filter is usually used to discriminate the edge type, thus eliminating the medium transitions for the reasons that were discussed in section 2.1.1. As shown with a little overhead in gates count, it is possible to exploit the same logic structure to add the tri-level PD feature.

2.1.2 Majority Voting (MV)

As explained in section 1.4, the CDR incorporates a time interleaved multi-lane architecture as shown in Fig. 1.10. The outputs of parallel BBPDs can be used to determine the amount of phase error across 16 consecutive samples. The straightforward solution is simply to add all the early-late results together and produce a final output which, on an integer scale, covers the $[-16, 16]$ range. This 6-bit output (including the sign bit) contains the polarity and the magnitude of 16 de-serialized phase errors. One general approach for implementing such a function could be pipelined layers of combinational logic: starting with a row of eight 2-bit full-adders (FAs) followed by four parallel 3-bit FAs in the second layer, two parallel 4-bit FAs in the third layer and a 5-bit FAs in the last stage resulting in a 6-bit outcome. This approach may require multiple clocks to render the output, hence imposing extra delays within the loop. However, the

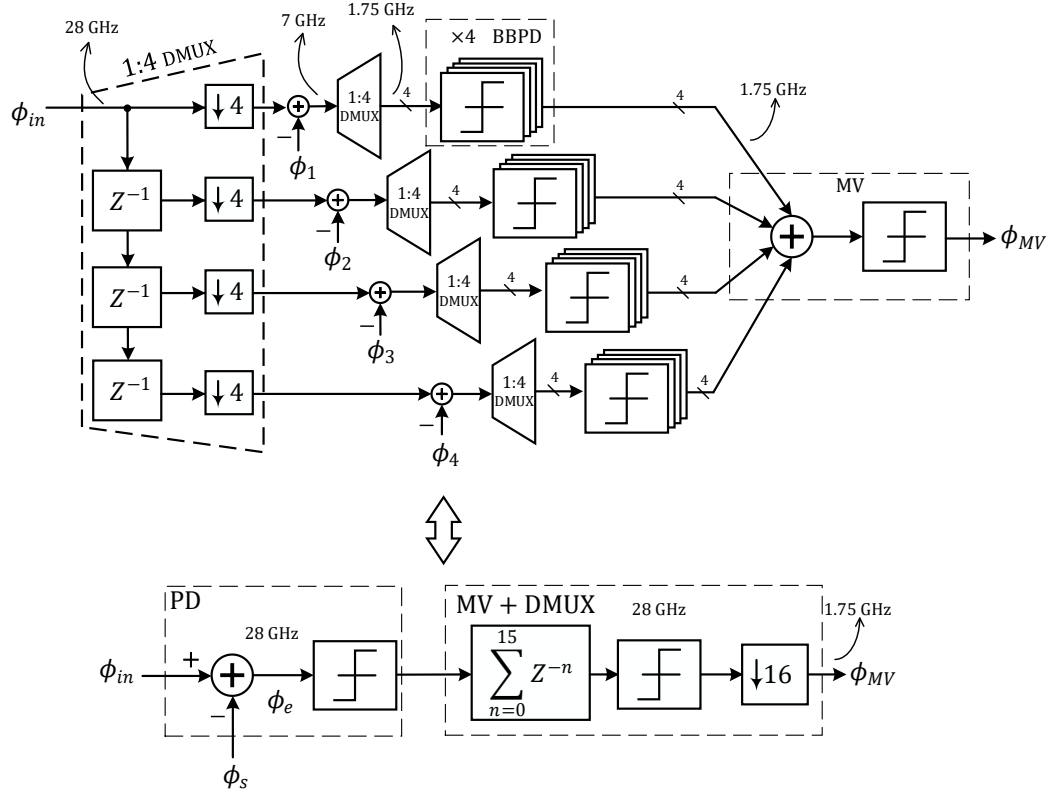


Figure 2.17: CDR's multi-lane PDs, MV and DEMUXs, (top) actual system level representation and (bottom) its single-lane equivalent to simplify the analysis.

main difficulty originates in the required resolution for the proceeding block i.e. the LF which includes multipliers and accumulators (MACs). The design complexity associated with high resolution processing would cause substantial penalty in terms of loop latency, area and power.

One common way to circumvent this issue is the application of majority voting to generate a final early/late outcome. Although the actual implementation may be different, majority voting is identical to truncating the output in which only the most significant bits (here the first MSB) is kept and the LSBs are discarded. In other words, we only consider the polarity of the error akin to performing BB operation. The main disadvantage here is the nonlinear nature of the MV block which increases the amount of quantization (truncation) noise in the loop and compromises the loop bandwidth due to the gain reduction. Hence to model the MV block, an adder, summing the output of 16 BBPDs is followed by a 1-bit quantizer as shown in Fig. 2.17.

Extra simplifications can be further applied to facilitate the system-level analysis. The parallel combination of the 16 BBPDs and the MV operates at $f_s/16$,

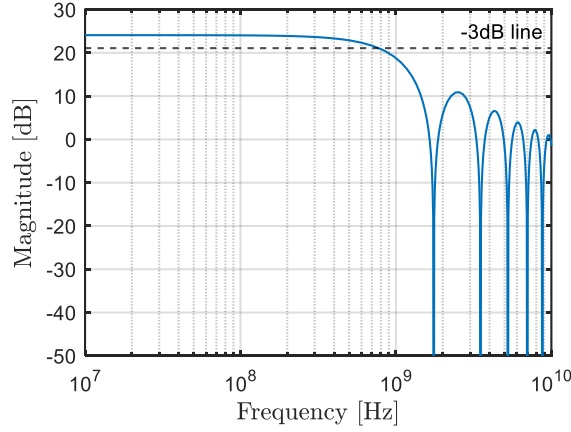


Figure 2.18: Moving Average filter's response.

can be moved before the DMUX section and substituted with one BBPD operating at f_s ; the multi-input adder is swapped by a moving average (MA) block having a window length of $N = 16$ samples while operating at a 16 times higher rate. The series combination of the two one-to-four DEMUX is substituted by one down-sampling block with the sampling rate reduction of 16, Fig. 2.17. The frequency response of the moving average filter, obtained from its transfer function is:

$$H_{MA}(z) = \sum_{k=0}^{N-1} z^{-k} = \frac{z^N - 1}{z^{N-1}(z - 1)} \xrightarrow{z=e^{j\omega}} \quad (2.32)$$

$$H_{MA}(e^{j\omega}) = \frac{\sin(N\omega/2)}{\sin(\omega/2)} e^{-jN\omega/2}$$

as $\omega = 2\pi f/f_s$ for $N = 16$ and $f_s = 28$ GHz it follows that $f_{3dB} \approx 800$ MHz. The frequency response of the moving average filter is shown in Fig. 2.18. Even though the BB-PD's noise is heavily suppressed by the low pass filtering of the MV, the overall quantization noise has been increased by the MV quantizer. It should be noted that the subsequent down-sampling block introduces aliasing hence the LF receives a white noise input regardless of noise shaping by MV, as shown in Fig. 2.19.

2.1.3 Loop Filter

The loop filter section consists of a proportional path gain, K_P , and an integration path (frequency accumulator) with the gain of K_I [Fig. 2.19]. The paths are followed by the phase integrator (phase accumulator). Since the CDR relies on the DPC for generating ϕ_{out} , to ensure the phase continuity, the phase

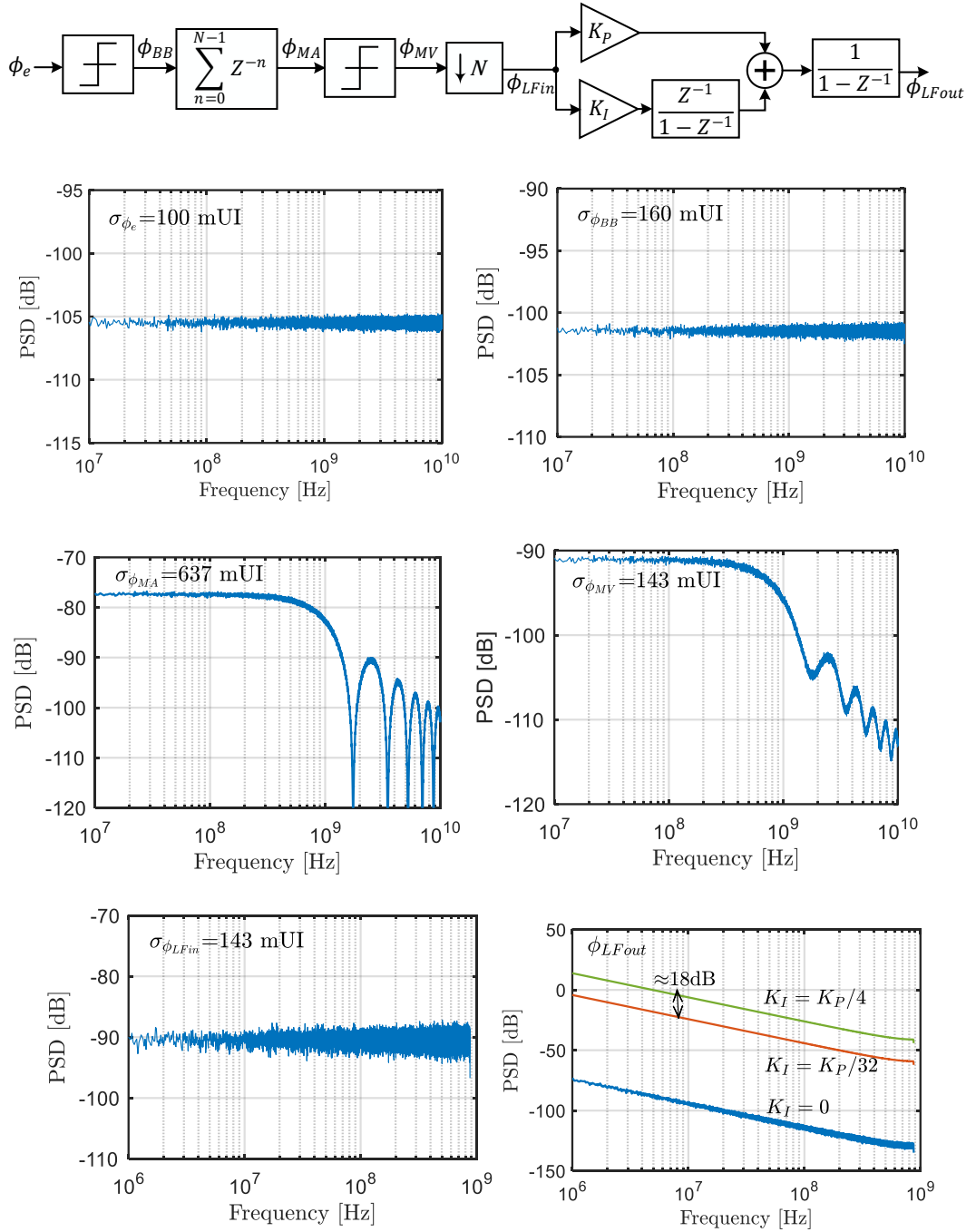


Figure 2.19: The feedforward response of BBPD, MV, DMUX and LF blocks (open loop mode) to a random jitter ($\sigma_e = 100\text{mUI}$), $N = 16$ and $K_P = 10 \text{ mUI}$. The down-sampling causes aliasing hence the LF input's spectrum exhibits a white noise profile.

accumulator is added to the design. Note that in case of VCO based CDR's this functionality is inherited in the nature of the VCO as a perfect phase integrator. The LF transfer function becomes:

$$H_{LF}(z) = (K_P + \frac{K_I z^{-1}}{1 - z^{-1}}) \frac{1}{1 - z^{-1}} \quad (2.33)$$

If the integration path is disabled i.e. ($K_I = 0$), the architecture is a type-one CDR with a first order LF. Being type-one implies the loop would not suffer from the static phase offset. Since the accumulators are implemented with the register in the main path the extra z^{-1} delay appears on the numerator of frequency accumulator⁸.

Although the CDR would meet most of the design specs by using a first order loop, it suffers from one serious drawback: degradation of the performance in the presence of frequency offset $\Delta f = f_{Din} - f_s$. Any frequency offset between the received data and the local sampling clock would stimulate the CDR input with a phase ramp ($\phi_{in} = 2\pi\Delta f t$)⁹. As the loop is type-one, a steady state error will be present. However, due to its nonlinear nature (BBPD and MV) the loop response is limited by the output linear slewing which determines the maximum rate of change in phase ($= d\phi_{out}/dt$). In the best case scenario the loop can update the output phase by K_P value in every 16 cycle of f_s (one LF clock period), therefore the maximum value of Δf is given by:

$$\Delta f_{max} = \max\left(\frac{1}{2\pi} \frac{d\phi_{out}}{dt}\right) = \frac{1}{2\pi} \frac{K_P f_s}{16} \approx 0.01 K_P f_s \quad (2.34)$$

in other words, unlike a linear loop, the steady state error continues to rise if the frequency offset is greater than Δf_{max} . For instance with $K_P = 5$ mUI, Δf_{max} is around 314 ppm (part per million) of the input baud rate. Even though $\Delta f < \Delta f_{max}$ may not cause loss of lock, the jitter tolerance of the CDR would be deteriorated. This happens because, in addition to tracking phase change due to the average frequency difference ($= 2\pi\Delta f$), the loop now has to correct for the momentary increase in $d\phi_{out}/dt$ due to the sinusoidal jitter at the input i.e. $\phi_{in} = 2\pi\Delta f t + \phi_j(t)$ while $\phi_j(t) = \phi_m \sin(2\pi f_m t)$ represents a sinusoidal jitter with amplitude and frequency of ϕ_m and f_m , respectively. Then to guarantee the phase lock:

$$\frac{d\phi_{out}}{dt} = \frac{d\phi_{in}}{dt} \quad (2.35)$$

$$\frac{d\phi_{out}}{dt} = 2\pi\Delta f + 2\pi f_m \phi_m \cos(2\pi f_m t) \quad (2.36)$$

⁸For the phase accumulator this delay is factored out and considered in z^{-N_a} .

⁹Throughout this chapter, in some equations we have used continuous notion for time for the sake of simpler and more familiar equation forms, this wouldn't produce contradictory results as the resolution for time $dt = f_s^{-1}$ is far smaller than the other time constants and interested signals' periods in the system.

to avoid the onset of slewing:

$$\max\left(\frac{1}{2\pi} \frac{d\phi_{out}}{dt}\right) \geq \Delta f + f_m \phi_m \quad (2.37)$$

substituting Eqn. 2.34 in Eqn. 2.37 yields:

$$\phi_m \leq \frac{0.01 K_P f_s - \Delta f}{f_m} \quad (2.38)$$

and with some modifications:

$$\phi_m \leq \left(0.01 K_P - \frac{\Delta f}{f_s}\right) \cdot \left(\frac{f_m}{f_s}\right)^{-1} \quad (2.39)$$

Eqn. 2.39 indicates that, for a certain jitter frequency a nonzero offset frequency would reduce the maximum jitter amplitude that can be tolerated by the loop.

This issue can be avoided by enabling the integration path ($K_I \neq 0$), which creates a type-two loop[30]. The type-two loop in its linear form can track the ramp input with zero steady error. In a nonlinear loop, the integration path provides variable steps that the output can make as opposed to those with the constant step size in the type-one case. The variable steps turn into a nonlinear slewing to track the input phase, hence minimizing the phase error.

2.1.4 Delay and Loop Latency

The discrete-time CDR inherently includes a delay of one clock cycle (here $16/f_s$), plus the time elapsed for the arrival of the signal from the samplers to DMUX output. Depending on the digital circuitry speed, excessive delays could be present. So if the DLF takes D clock cycles to render an output that can be represented in the model by the addition of $N_d = D + 1$ ¹⁰ delay elements (z^{-N_d}). The delay element introduces a pole at $z = 0$, with an order being equal to N_d , consequently increasing the order of the loop's transfer function [31].

2.1.5 DPC

The next block is the DPC. An ideal DPC can be modelled by a quantizer. The quantization interval Δ , is determined by ($\Delta = 2\pi/2^{N_{PI}}$), with N_{PI} being the DPC's resolution. Alternatively, the quantizer behaviour can be approximated

¹⁰Note that in contrast to previous section, here N_d measures the delay in cycles of down-sampled clock i.e. $f_s/16$ not f_s .

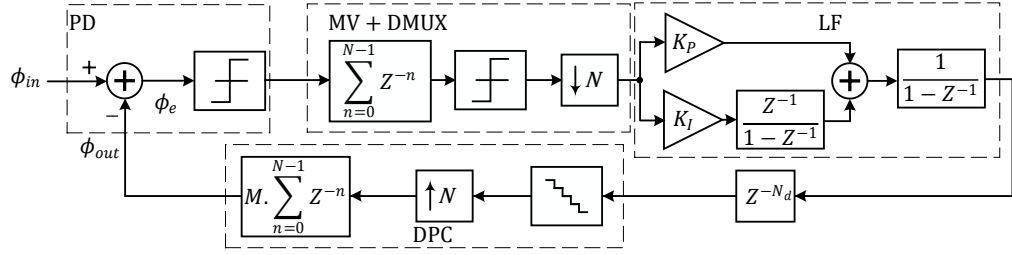


Figure 2.20: The complete block diagram of the CDR, the transition density multiplier at the PD output is not shown.

by a white noise source with Gaussian PDF and variance of $\Delta^2/12$. The DPC's input code is updated with the rate of $f_s/16$ same as with the LF. The output clock has $M=4$ phases (at $f_s/4$) dedicated for the edge sampling. Since we have merged the parallel BBPDs there is now one output phase operating at f_s . The rate transition also has to be taken into account. For this purpose, an up-sampling block is combined with a moving average filter, same as Eqn. 2.32, which inserts $N - 1$ i.e. 15 input replicas between the received values from the loop filter. The DPC model is not complete yet, the output of the filter also has to be scaled up by a conversion factor identical to $M(= 4)$ as the DPC output and the input data sweep the phase with different frequencies. The DPC resolution directly affects the amount of jitter generation in the loop. In order to reduce the jitter generation higher DPC resolution is required. However, since it is preferred to have $K_P \leq \Delta^{11}$, the main disadvantage of reducing the DPC resolution is the reduced loop gain and bandwidth as per Eqn. 2.39. This means that to retain the same $d\phi/dt$ for the output phase, the LF needs to be clocked twice for every additional bit, which in addition to power penalty, the de-multiplexing factor needs to be modified respectively. An option that might not be feasible to meet the digital implementation requirements in terms of timing closure with certain foundry based standard cell libraries. Typically, high frequency DPCs' resolution is in the range of 6 to 8 bits [19], [32], [33] and [34]. In our design $N_{PI} = 7$ which translates to $\sigma_{PI} \approx 1$ mUI.

2.1.6 CDR Model Analysis and Simulations

By combining all the blocks, the full system describing the CDRs behaviour is obtained as shown in Fig. 2.20. We have performed some simulations to inspect the dynamics of the CDR after the changes made to facilitate physical

¹¹Although technically it is possible to choose $K_P > \Delta$, this would make the LSBs of the DPC redundant.

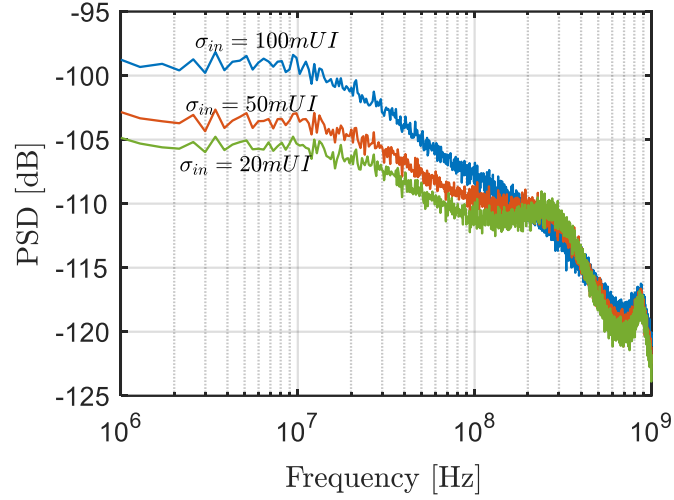


Figure 2.21: PSD of ϕ_{out} for different input values ϕ_{in} , the loop parameters are: $K_P = 5$ mUI, $K_I = 0$ and $N_d = 1$.

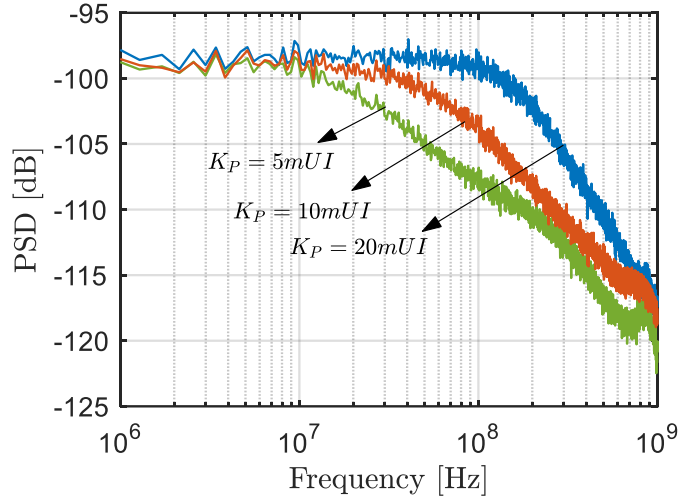


Figure 2.22: PSD of ϕ_{out} for different K_P values with $\phi_{in} = 100$ mUI (−105.5 dB), the loop parameters are: $K_I = 0$ and $N_d = 1$.

implementation. Fig. 2.21 to Fig. 2.25 illustrate the results for different parameters settings in various scenarios.

It should be noted that in DPC based CDR the clock's phase change is achieved by the direct control i.e. phase modulation as opposed to the VCO based CDR where the output phase advances by adjustment of the frequency i.e. frequency modulation. In such a system, any frequency offset can be corrected accurately by shifting the VCO's centre frequency, facilitating smoother transitions in the phase domain. However, in DPC based CDR with the lack of frequency tracking (as it set by the reference clock), in the presence of large frequency offsets the CDR has to compensate regularly for the frequency offset related errors

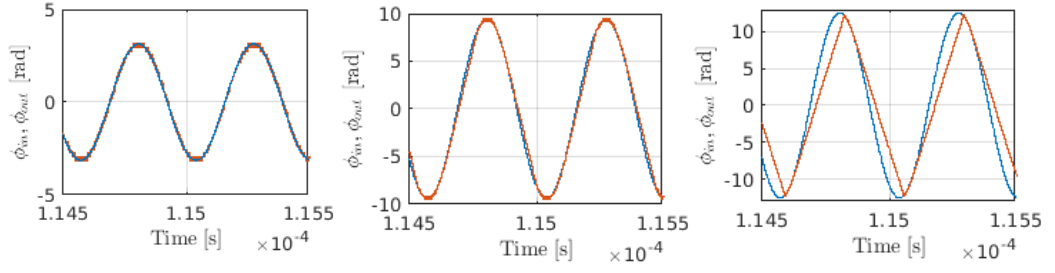


Figure 2.23: CDR's response to a sinusoidal jitter with the amplitude of (left) 0.5 UI, (middle) 1.5 UI and (right) 2 UI at $f_{in} \approx 2.1$ MHz, as the input amplitude increase the loop starts to slew failing to track the input as predicted by Eqn.(2.34). Loop parameters are: $K_P = 10$ mUI and $N_d = 1$.

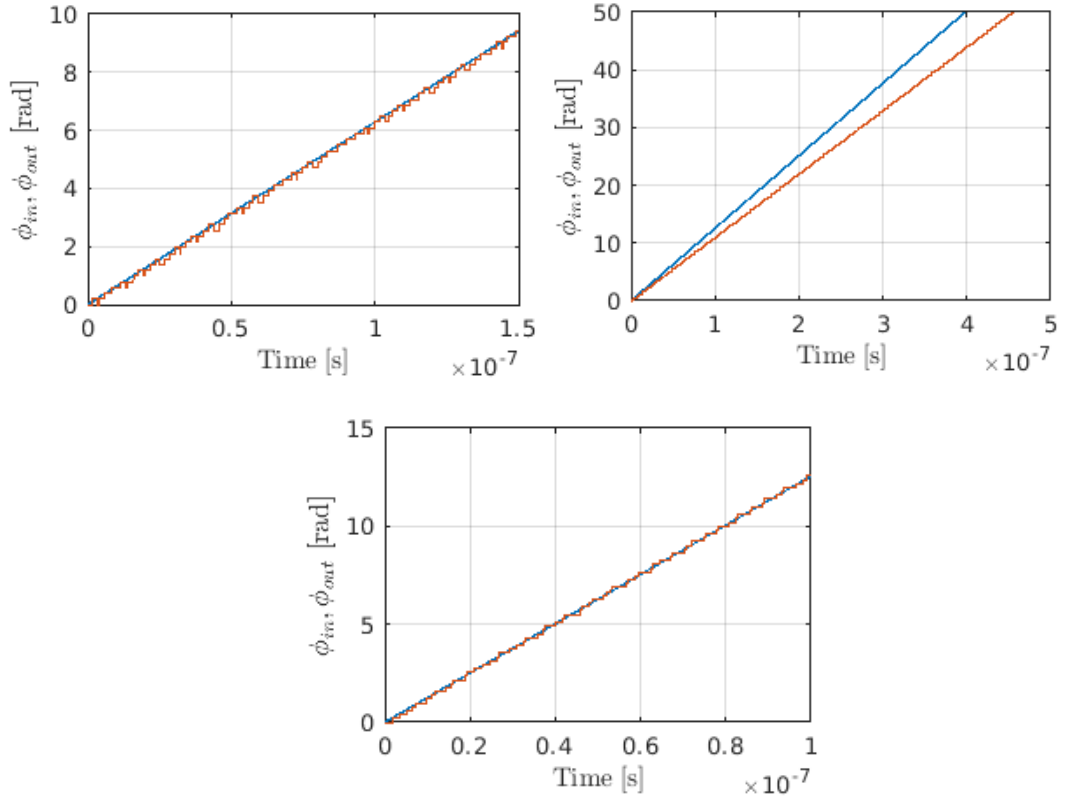


Figure 2.24: The CDR's response to a phase ramp due to the frequency offset Δf between the input and sampling clock, (top, left) type-1 loop tracking the input phase without error while $\Delta f = 10$ MHz, $K_P = 10$ mUI and $\tau_I = \infty$ ($K_I = 0$) (top, right) losing the phase lock for $\Delta f = 20$ MHz, $K_P = 10$ mUI and $\tau_I = \infty$ and (bottom) activating the integration path to track the input with $\tau_I = 32$. $N_d = 1$ for all the cases.

by producing large phase steps, this would result in more jitter generation. Therefore, even with $K_I \neq 0$, the frequency offset range that the loop can tolerate while being properly functional is limited.

Although the addition of K_I enhances the offset frequency tracking of the CDR, increasing it could adversely affect the JTRAN by introducing jitter peaking.

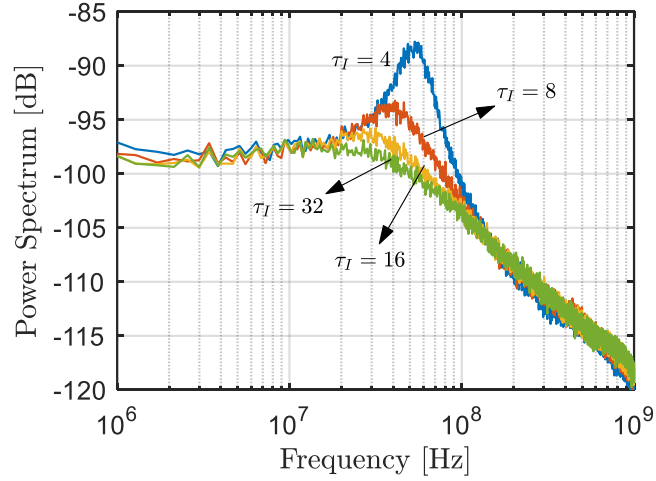


Figure 2.25: PSD of ϕ_{out} for different τ_I ($K_I = K_P/\tau_I$) values with $\phi_{in} = 100$ mUI, the loop parameters are $K_P = 10$ mUI and $N_d = 1$. The over damped response using $\tau_I > 8$, requires that K_I register length to be at least 3-bit wider than the K_P register.

Achieving low jitter peaking requires an overly damped response by maximizing the ratio of K_P to K_I , $\tau_I = K_P/K_I$ (frequency integrator's time constant), analogous to the damping factor in linear CDRs [16]. The immediate result of such a choice is the required accuracy for K_I which mandates increasing the register length in the digital domain. Simulations suggest [Fig. 2.25] that a value of $\tau_I > 8$ is required to reduce the jitter peaking. This, in turn, requires the K_I register's length to be at least 4 bits more than the K_P register length.

Like the previous section it is possible to develop a linear counterpart to simplify the system analysis. In the presence of random jitter, the nonlinear functions of the BBPD and MV blocks can be substituted with the gain and a quantization noise. The BBPD linear model is based on (2.8) in section 2.1.1.3 and for the MV block [35]:

$$K_{MV} = \sqrt{\frac{2}{\pi}} \frac{1}{\sigma_A} \quad (2.40)$$

$$\sigma_{MV} = \sqrt{1 - \frac{2}{\pi}} \quad (2.41)$$

As demonstrated in Fig. 2.26 to Fig. 2.28 the same concept is utilized to attain the linearized version of the CDR. The values for K_{PD} and K_{MV} will be updated as the CDR tries to minimize the difference between the input and output. Using the linearized system, the jitter transfer function H_{JTRAN} can be extracted as shown in Fig. 2.13.

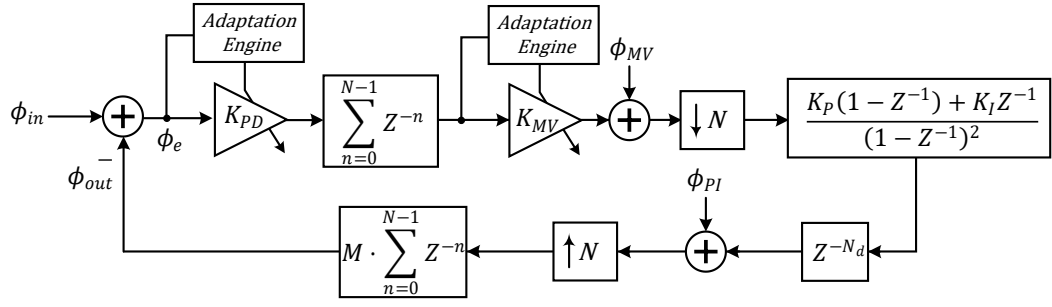


Figure 2.26: The simulation setup to extract the linearized parameters for the BBPD and MV blocks, the quantization noise of BBPD is ignored. This simplification will affect the accuracy of the model for low input jitter values

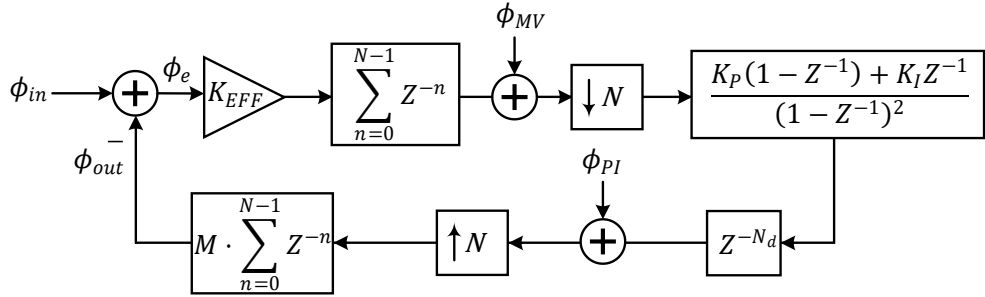


Figure 2.27: The linearized version of the CDR, the BBPD and MV gains are combined: $K_{EFF} = K_{PD} \cdot K_{MV}$, only small and large transitions are considered for PAM4 PD i.e. $\alpha_T = 0.5$. This model is only valid for JTRAN analysis.

A simple example may help to gain an intuitive understanding of the delay's influence. Let the CDR of Fig. 2.20 be in its zero-input state i.e. the data is free of jitter and also assume infinite resolution for the DPC ($\Delta \approx 0$). Now if under the influence of initial state $\phi_{out} \neq \phi_{in}$, then ϕ_e would be reduced by the negative feedback loop until $\phi_e \approx 0$ ¹². Due the loop latency, any decision on the current state of ϕ_e would reach ϕ_{out} after N_d cycles passed. This means by the time that $\phi_{out} \neq \phi_{in}$ the loop still will continue on the previous decided trajectory for N_d cycles which after that the loop will reverse its course. This indicates the existence of a stable oscillation i.e. limit cycle in the loop, causing ϕ_e to dither around ϕ_e with an amplitude and frequency determined by N_d . If we assume $K_I = 0$, depending on ϕ_e 's sign ϕ_{out} would step up/down by an amount of K_P every clock cycle, T_{CLK} . Since any crossing detection takes N_d cycles to be effective then we can approximate it [9] as:

$$\phi_e(t) = N_d K_P \sin\left(\frac{2\pi}{4N_d T_{CLK}} t\right) \quad (2.42)$$

¹²more accurately $|\phi_e| < K_P$.

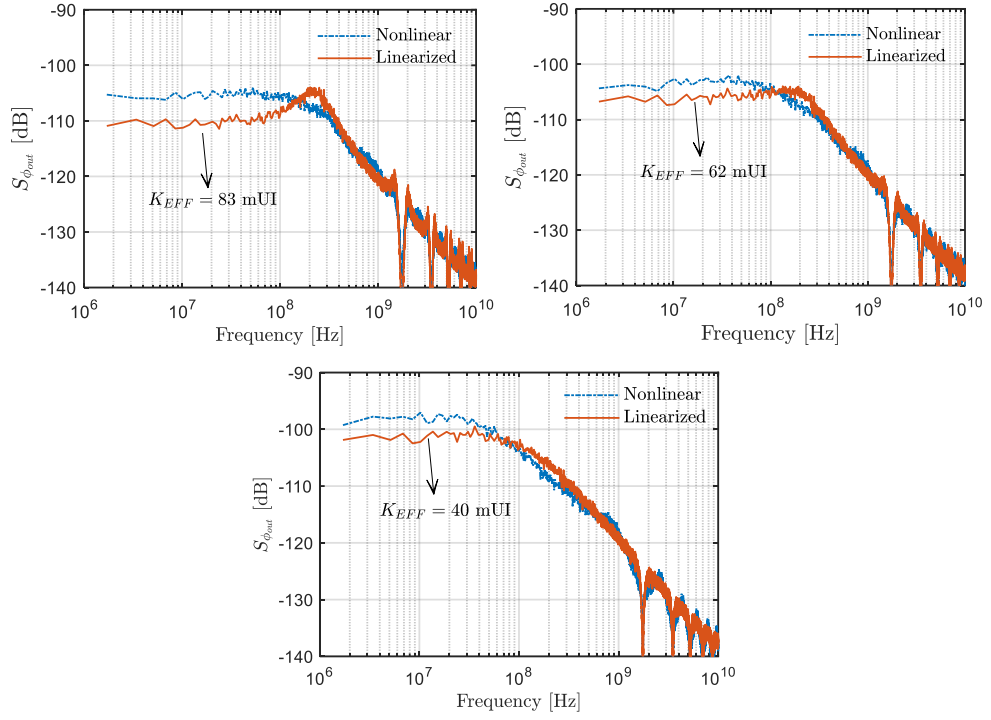


Figure 2.28: Comparison of the linearized and nonlinear CDR, the loop parameters are: $K_P = 10$ mUI, $\tau_I = 32$ and $N_d = 1$. As the input RMS jitter increases the effective gain drops reducing the jitter peaking. The accuracy of the model improves as the input jitter becomes the dominant source of the noise in the system.

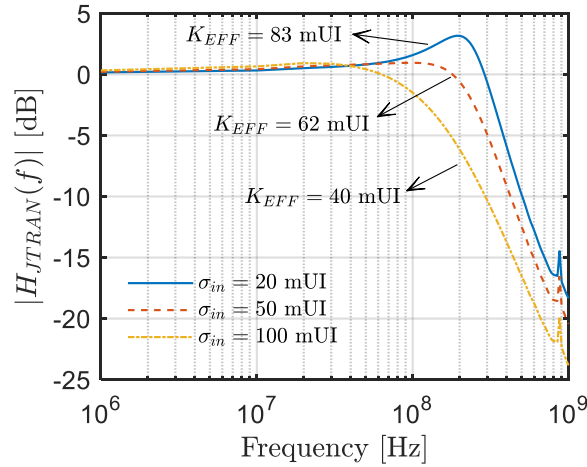


Figure 2.29: The JTRAN obtained from the linearized CDR, calculated using the simulation results from Fig. 2.27

which is the jitter generated by the loop latency, the more the delay the larger the jitter amplitude and the lower its frequency. In Fig. 2.30 the simulation results are illustrated for $N_d = 10$ and $N_d = 20$ while $K_P = 10$ mUI, the jitter amplitude due to the limit cycle is 100 mUI ($= 0.628$ rad) and 200 mUI ($= 1.27$ rad), respectively. This is the main disadvantage associated with the digital

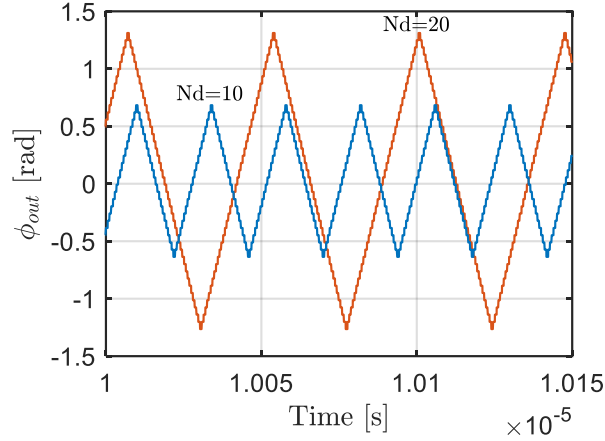


Figure 2.30: A stable oscillation or “limit cycle” is generated in the CDR loop (Fig. 4) due to the long delay $N_d = 10$ and 20. The input is jitter free and the loop parameters are: $K_P = 10$ mUI and $K_I = 0$. The DPC has infinite resolution $\Delta = 0$.

realization of the CDR. In the actual circuit however, the limited DPC resolution would impact this mechanism. If the jitter amplitude $N_d K_P \leq \Delta$ then the quantization noise floor would surpass the jitter. Such a constraint ($N_d K_P \leq \Delta$) sets a maximum value for K_P which translates to the reduction of the CDR's bandwidth with the benefit of less jitter generation due to the long delay.

This condition could be interpreted in another way as well; instead of updating the output value every T_{CLK} the loop waits for $N_d T_{CLK}$ after a decision before the next DPC code change is performed. Consequently, the loop's lower BW impairs the CDR's JTOL performance, minimizes Δf_{max} and increases jitter generation due to the other sources within the loop. Given the fact that Δ (DPC bits) usually is specified at early design stage and could be a predefined parameter, it is crucial to reduce the number of sequential blocks (registers) in the digital section.

The dithering also determines the minimum resolution required for the coefficients in the digital section. For instance if $N_d = 8$ with a 7-bit DPC, to cancel the dithering, the K_P register has to provide at least 3 bits of redundancy i.e. the LF phase accumulator length has to be more than 10 bits.

The foregoing conclusions were drawn upon the assumption of a jitter-free input. The input jitter and the LF order would impact the conditions that initiate the limit cycle. Because of the nonlinear PD, the loop gain is inversely proportional to ϕ_e 's (hence ϕ_{in} 's) amplitude. Therefore, according to the Barkhausen criterion, in frequencies that the required 180° phase shift around the loop is achieved (due to the long delay or the LF's phase response), there exist an

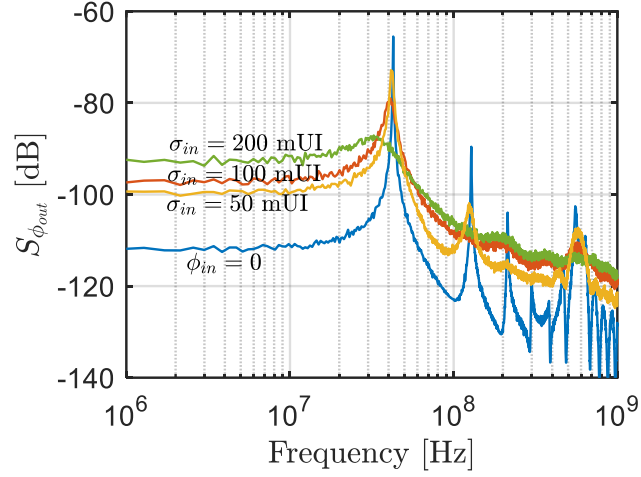


Figure 2.31: The influence of input jitter (incl. 7-bit DPC quantization noise) on the limit cycle. The loop parameters are: $K_P = 10$ mUI, $\tau_I = 32$ and $N_d = 10$

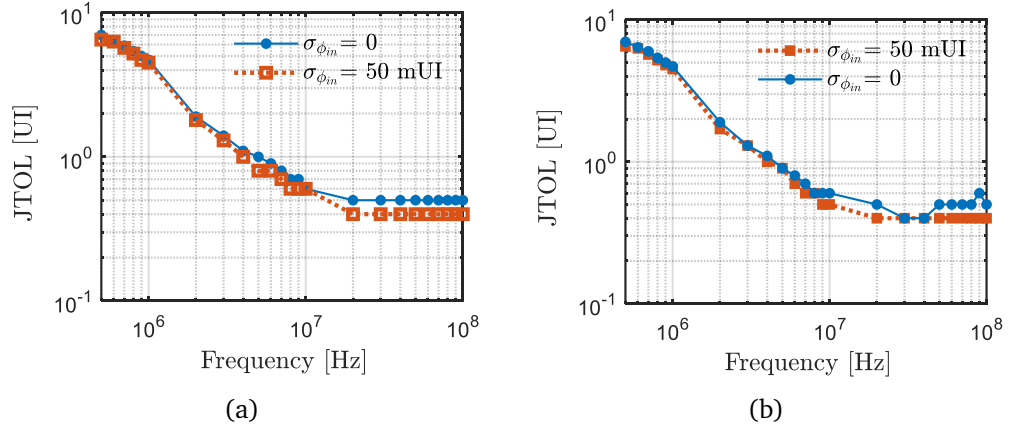


Figure 2.32: JTOL of the CDR (Fig. 4) with and without input random jitter (a) $N_d = 1$ (b) $N_d = 8$ the loop parameters are $K_P = 10$ mUI and $K_I = 0$.

input amplitude which satisfies the conditions for the unity gain magnitude, exhibiting limit cycle behaviour [28]. However, as discussed in a previous section, when random jitter is present in the system, the BBPD characteristic is smoothed out, setting a maximum bound for the variable gain of the PD even when the input amplitude is zero. In other words, random jitter could be useful to quench the limit cycle. As proved in [36], there is a threshold value for the RMS input jitter, $\sigma_{in,th}$, which stops the limit cycle. A larger amplitude of limit cycle requires a larger value of $\sigma_{in,th}$ to quench the limit cycle.

As shown in Fig. 2.31, the simulation results indicate the influence of input jitter on N_d effects, as σ_{in} continues to increase, the limit cycle disappears however the jitter peaking is still evident indicating an underdamped oscillation.

Using the default parameters for our design the CDR's JTOL is shown in Fig.

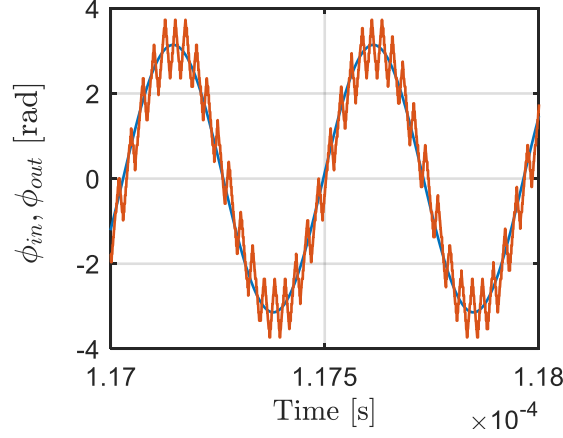


Figure 2.33: The input and output jitter, the loop keeps track of $\phi_{in} = \pi \sin(2\pi \times (2.13\text{MHz}))$ while the limit cycle makes ϕ_{out} dither around ϕ_{in} . Loop parameters are the same as for Fig. 2.32(b)

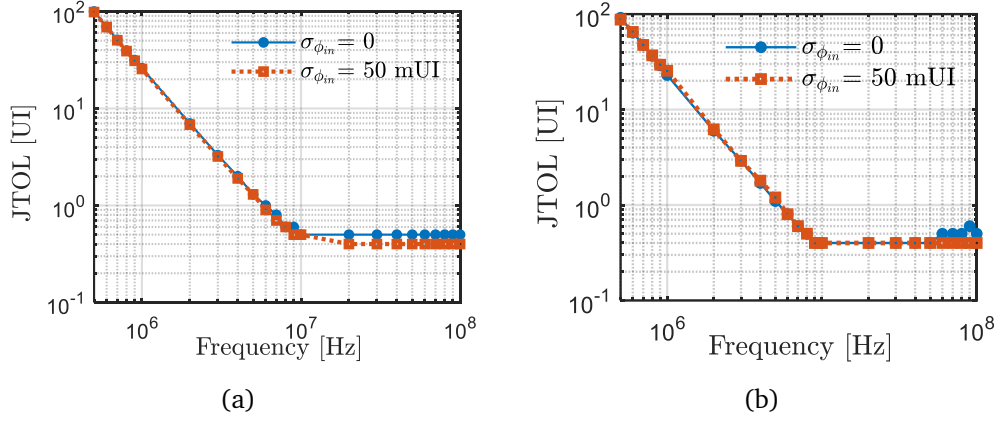


Figure 2.34: JTOL after activating the integration path (a) $N_d = 1$ (b) $N_d = 8$. The loop parameters are: $K_P = 10$ mUI and $\tau_I = 32$.

2.32. Fig. 2.33 plots the output phase for one input jitter's frequency and amplitude point which passes the JTOL criteria i.e. $\phi_e \leq 0.5$ UI. The effect of delay and noise is investigated separately showing how they affect the loop. As it is seen from Fig. 2.34, activating the integration path improves the CDR's phase-rate tracking ability.

2.2 Building Blocks Non-Idealities in CDR

In the previous section we developed the CDR system step by step and analysed it while pointing out the advantages alongside the associated limitations with the chosen architecture. Those limitations are fundamental to the system of the CDR and set the bar for the best achievable performance. However, there

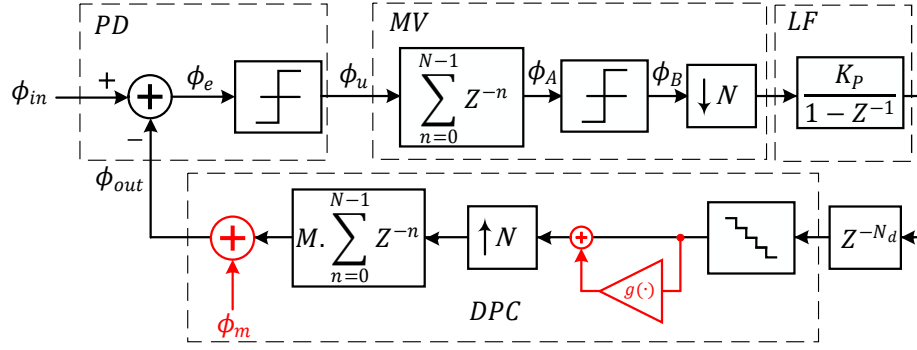


Figure 2.35: Addition of the non-idealities introduced by DPC to CDR's model. Only proportional path is considered in simulations.

are other sources of imperfection that originate from the building blocks at the circuit level that cause further deterioration in the CDR dynamics. In this sense, the critical blocks are the AFE and MPCG (DPC) as they are realized in the analog domain. Among the circuit level non-idealities, of particular interests to us are those that are crucial for true data and clock phase alignment including the output clock phase skews, nonlinearity in the DPC and the voltage offset and phase mismatches between edge sampling channels in the AFE. In the following sections we systematically analyse the aforementioned drawbacks.

2.2.1 Clock Phase Mismatches (Skews) at DPC Output

Fig. 2.35 illustrates the addition of the DPC's nonidealities to the CDR system. As depicted in Fig. 2.36(a)–(b) the multi-phase array of PDs is replaced by a single channel PD operating at frequency of f_s . The skew in clock phases are modeled by the addition of phase error ϕ_m with minimum frequency of f_s/M wherein M is the number of input edge samplers. The amplitude of ϕ_m , represented by $\{\delta\phi_1, \delta\phi_2, \dots, \delta\phi_M\}$ ensemble [Fig. 2.36(c)], depends on the delay variation due to the random mismatches in clock paths, σ_d , and also duty cycle distortion, t_{dcd} .

Supposing that the random delay mismatches are uncorrelated, ϕ_m may be expressed by a periodic waveform as shown in Fig. 2.36(c) where the adjacent levels take a magnitude of $2\pi f_s \sigma_d$ with opposite signs to represent a worst-case condition. The DCD would cause additional deviations by affecting the differential clock phases and can be taken into account by relative shifting of the corresponding levels in ϕ_m with an amount equal to $2\pi f_s t_{dcd}$. In this case with $f_s = 28$ GHz, ϕ_m 's spectrum contains tones at 7 GHz and its harmonics. As the spurs are out-of-band (nullified by the moving average's zero frequencies), the

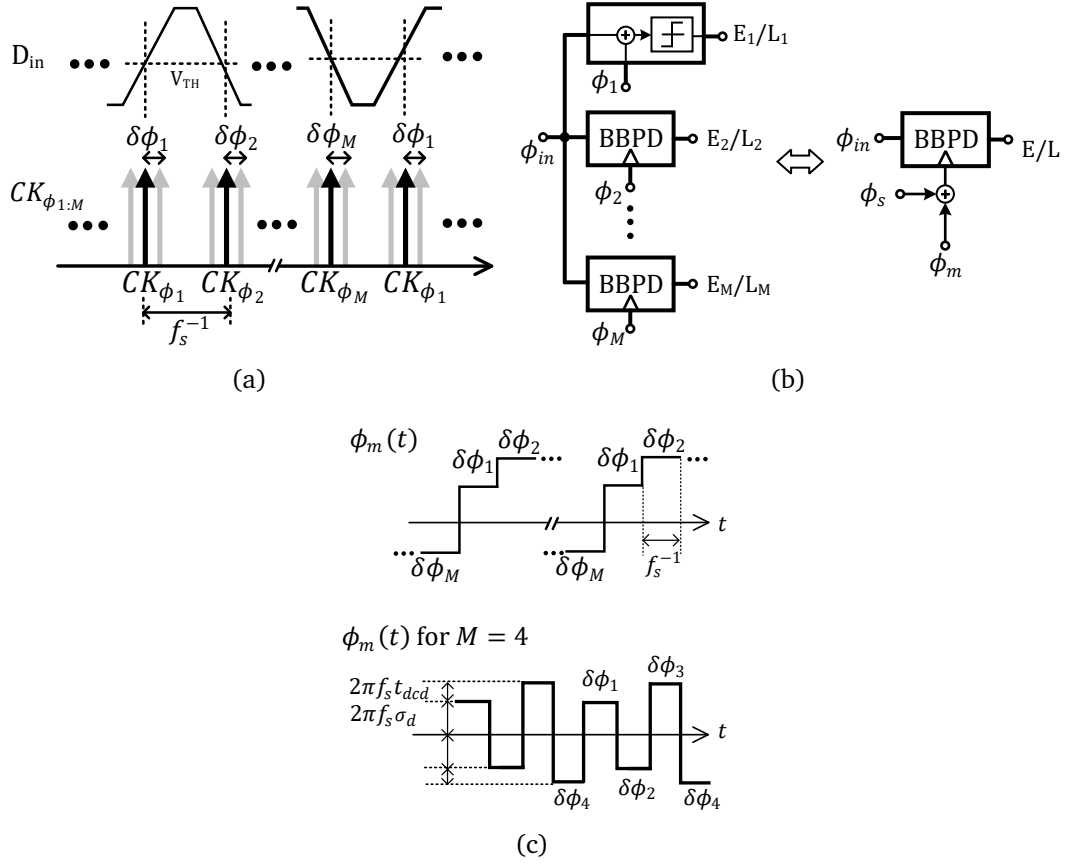
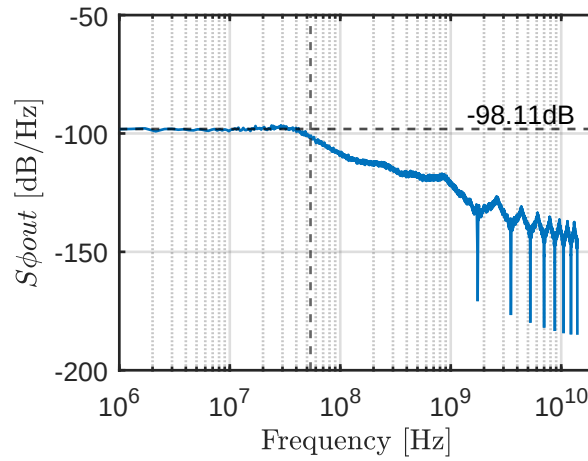


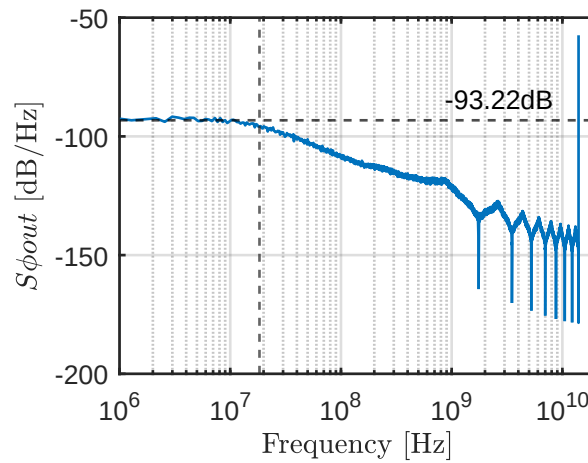
Figure 2.36: (a) sampling of data transitions by edge slicers, the phase skew results in non-uniform sampling (b) modelling of parallel BBPDs operating at f_s/M with a single PD block operating at f_s , addition of ϕ_m to the ideal sampling phase, ϕ_s , to account for the effect of phase skew between clock phases. ϕ_m waveform is periodic with minimum frequency of f_s/M (c) ϕ_m waveform used in our simulations ($M = 4$) and $f_s = 28$ GHz.

loop fails to correct for such errors. Hence the recovered sampling clock, f_s shows strong phase modulation which reduces the available sampling margin to meet certain bit error rates. Fig. 2.37 illustrates $S_{\phi_{out}}$, the spectral density of output phase, ϕ_{out} , for different ϕ_m values.

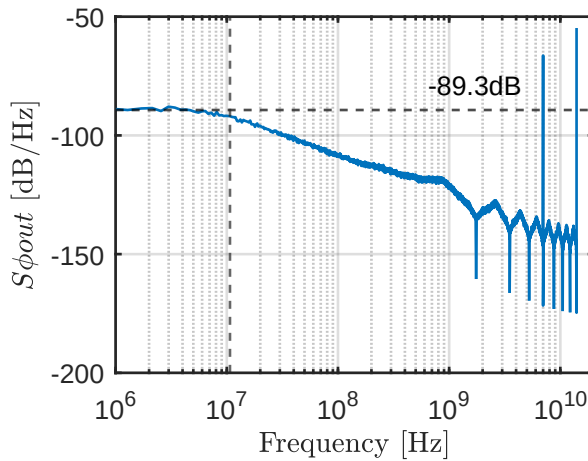
In addition to the generation of out-of-band tones, the overall response at lower frequencies changes drastically. This happens because of the nonlinear nature of the bang-bang loop; ϕ_m minimizes the PD's sensitivity to the random components in ϕ_e and the combined gain of PD and MV, $K_{EFF} = K_{PD} \cdot K_{MV}$, drops as shown in Fig. 2.38. Consequently, the amount of generated jitter inside the loop increases so does the total output rms jitter, $\sigma_{\phi_{out}}$, due to the random components of ϕ_{out} [Fig. 2.38]. In Fig. 2.38 to extract K_{EFF} the following set of expressions from [35], [28] and [32] and has been used in conjunction with



(a)



(b)



(c)

Figure 2.37: ϕ_{out} power spectral density (a) $\sigma_d = 0$, $t_{dcd} = 0$ (b) $\sigma_d = 5$ ps, $t_{dcd} = 0$ thus one spur at 14 GHz (c) $\sigma_d = 5$ ps, $t_{dcd} = 0.025T_{CK}$ ($T_{CK} \approx 142$ ps) resulting in additional spur at 7 GHz. Default parameters are $\sigma_{\phi_{in}} = 100$ mUI (-105 dB/Hz), $K_p = 5$ mUI and $N_d = 8$.

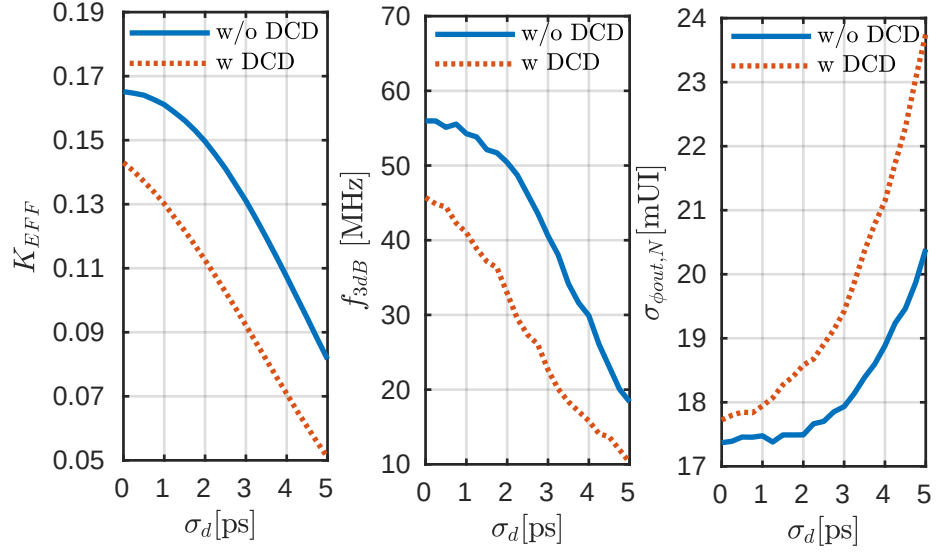


Figure 2.38: Effective gain of PD and MV, the loop's jitter transmission bandwidth and output rms jitter (due to random components) vs σ_d with and without DCD ($t_{dcd} = 0.025T_{CK}$ and $T_{CK} \approx 142$ ps, other loop parameters are based on Fig. 2.37

the nonlinear simulation results:

$$\begin{aligned}
 K_{PD} &= \frac{E[\phi_{e,N}(nT_s)\phi_u(nT_s)]}{E[\phi_{e,N}^2(nT_s)]} \\
 K_{MV} &= \frac{E[\phi_A(nT_s)\phi_B(nT_s)]}{E[\phi_A^2(nT_s)]}
 \end{aligned} \tag{2.43}$$

wherein $T_s = f_s^{-1}$, $\phi_{e,N}$ represents the random jitter in ϕ_e while ϕ_u is the BBPD's output including random and deterministic jitters. ϕ_A and ϕ_B are the input and output of the MV's 1-bit quantizer, respectively. It should be noted that unlike ϕ_e which contains both random and deterministic values, ϕ_A is a pure random signal without spurs. This is expected since N/M is an integer and therefore, the spurs always coincide with the zero frequencies introduced by the moving average filter.

In our analysis we have relied on the simulation results to calculate the required values and have assumed that the input to the MV's nonlinearity is purely random since the moving average filter heavily attenuates the out of band spurs generated by ϕ_m . It should be noted that ϕ_m can also include the phase noise of the input reference but the amount of contributed RMS jitter is negligible when compared with ϕ_{in} .

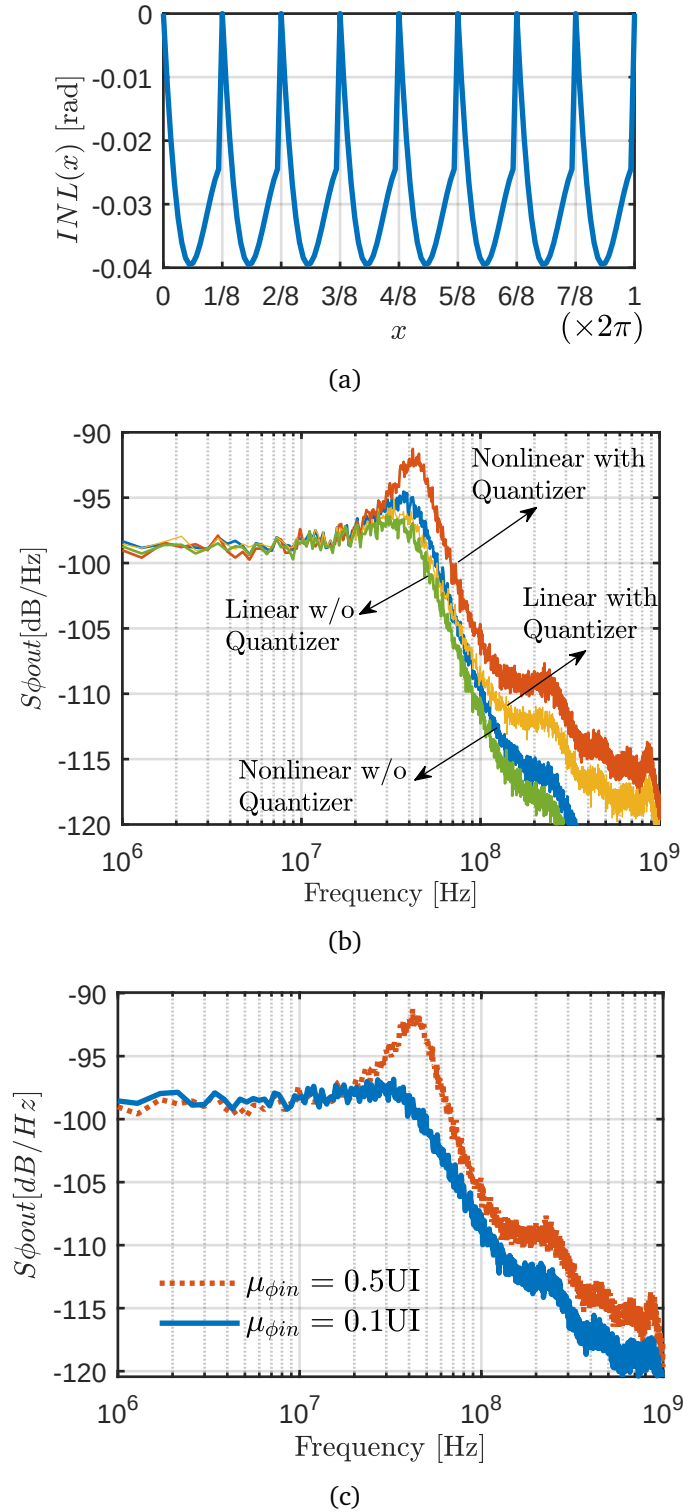


Figure 2.39: (a) INL profile for DPC nonlinearity, (b) changes in ϕ_{out} spectral density due to the INL and DNL effects (by enabling/disabling the quantizer and nonlinearity block) (c) ϕ_{out} spectral density for $\mu_{\phi_{in}} = 0.1UI$ and $0.5UI$ including INL and DNL effects. Default loop parameters are used.

2.2.2 DPC Nonlinearity

In Fig. 2.35 $g(\cdot)$ can be expressed in the form of $g(x) = \epsilon x + INL(x)$, with ϵ representing the gain error. As ϵ is a linear error, it can simply be corrected by adjusting K_P therefore will be ignored here. We use an arbitrary INL profile¹³ as depicted in Fig. 2.39(a). Having its argument received from the quantizer, $g(x)$ produces a non-uniform quantization noise which corresponds to the DNL error. By inserting or removing of the quantizer, we can readily differentiate the INL and DNL effects. Because of the loop's high pass response to DPC's noise, at low frequencies the DNL has little impact in comparison to the large jitter generated by the BBPD and MV blocks whereas at high frequencies it introduces excessive phase dithering, raising the noise floor, Fig. 2.39(b).

Although the impact of the INL is suppressed by the large loop gain, it makes the loop dynamics dependent on static phase shifts in the input, $\mu_{\phi_{in}}$.¹⁴ To explain this we note that since the loop is type one, the steady state error of a step input is zero i.e. $\mu_{\phi_{out}} = \mu_{\phi_{in}}$. To satisfy this constraint, the input of the $g(\cdot)$ block has to settle around a certain value, which alters the effective gain of the DPC as the input code varies, this phenomenon is shown in Fig. 2.39(c).

2.2.3 Voltage Offsets in Edge-Sampling Channels and Slicers (AFE)

Each block of the AFE can contribute some amount of offset voltage e.g. the differential buffers due to the random mismatches, charge injection and clock feedthrough by the switch-cap network, offset of the slicers and the reference voltages. All the offsets can be seen as a threshold voltage's shift which would cause decision errors. As explained in section 2.1.1.1, detection based on a non-centred threshold would cause a dead-zone in the characteristics of the BBPD. The main difference here is that, since the BBPD is the combination of parallel PDs, offset mismatch between channels could create additional errors. As shown in Fig. 2.40 by assuming a single pole frequency response for the input of the slicers, the resulting time difference, Δt , between an ideal threshold

¹³The INL profile is based on Eqn. 3.8 for a unit PI cell with $\phi = \pi/4$ and $\eta = 0.1$.

¹⁴Examples of this scenario could be present during initial lock acquisition at start up or any momentary phase glitch, driving the CDR loop to correct for the offset created by the phase step at the input.

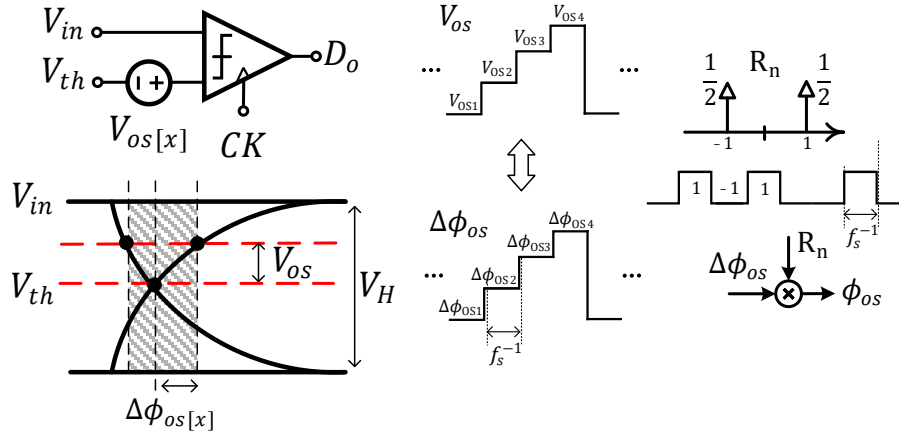


Figure 2.40: Conversion of the voltage offsets from the AFE's sampling channels referred to slicers input (including the offsets from input buffers, switch-capacitor network and slicers) to phase offsets $\Delta\phi_{os}$, R_n is to randomize the effect of edge types. The output, ϕ_{os} , is added to the input of PD.

crossing at V_{th} , and a displaced one by an amount of V_{os} is given by:

$$\Delta t = RC \ln \left(\frac{0.5V_H}{V_{th} - V_{os}} \right) \quad (2.44)$$

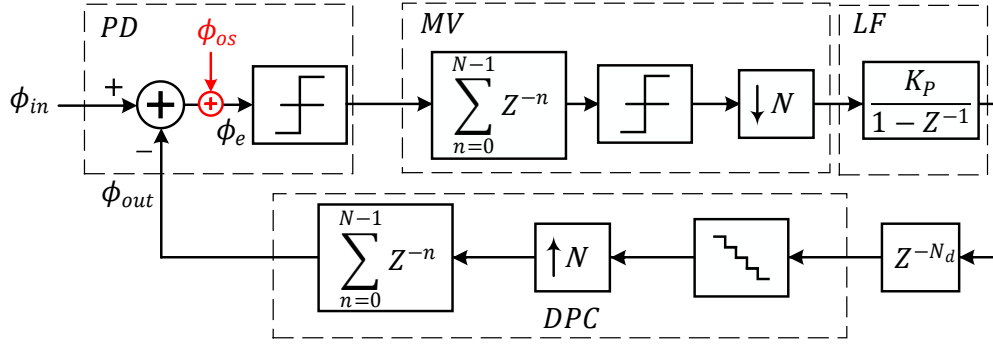
as $V_{th} = V_H/2$ then:

$$\Delta t = RC \ln \left(\frac{1}{1 - \frac{2V_{os}}{V_H}} \right) \quad (2.45)$$

and converting Δt to $\Delta\phi$:

$$\Delta\phi = 2\pi R_b \Delta t = \frac{R_b}{f_{BW}} \ln \left(\frac{1}{1 - \frac{2V_{os}}{V_H}} \right) \quad (2.46)$$

Eqn. 2.46 states that reducing the slicers input's time-constant and increasing the voltage swings (eyes height) would reduce the amount of phase offset. Since $V_{HS} = V_{HL}/3$ in the same conditions, the phase detection based on small eyes is also more prone to offset voltages. For instance by assuming $f_{BW} = 0.7R_b$, as in our design the 28 GBd PAM4 input has differential swings of $V_{HL} = 200$ mVpp and $V_{HS} = 66$ mVpp, therefore an offset of 20 mV, if left uncalibrated, would translate to jitter amplitudes of approximately 50 mUI and 200 mUI if detected by large and small transitions, respectively. Now to model the effect, we can invoke the same approach mentioned in section 2.1.1.3. The only difference here is the mismatch among the four channels' offsets. As shown in Fig. 2.40, ϕ_{os} is a repeating sequence of four offset values calculated by Eqn. 2.46 for every channel. ϕ_{os} would be randomized by the multiplication of a uniformly distributed random sequence, R_n , to include the edge type depen-

Figure 2.41: Addition of the ϕ_{os} to the CDR's system.

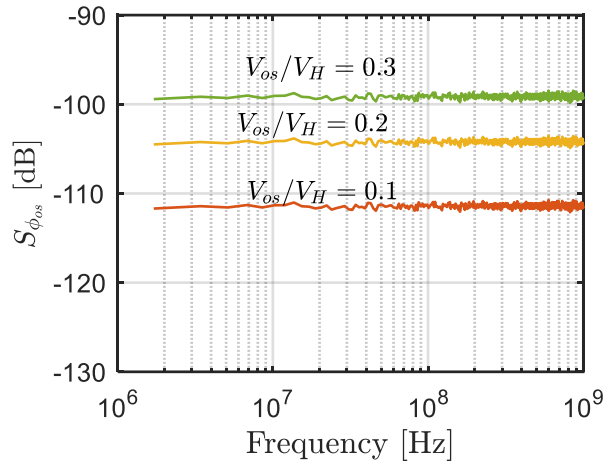
dency. Although Eqn. 2.46 is asymmetrical around the threshold, hence $\Delta\phi$ takes unequal values for rising and falling edges depending on V_{os} polarity, we only use the maximum phase shift in our modelling. Since the four channels are identical and uncorrelated, equal σ_{os} would represent corresponding offset levels in ϕ_{os} . Due to the randomization by R_n , unlike the clock skew in DPC, the signs of the offset values are not important. Therefore, statistically speaking this scenario is equivalent to the case of a single channel with one offset value. The offset error is incorporated in the CDR model, as shown in Fig. 2.41. Fig. 2.42 illustrates the performed simulations for different values of V_{os}/V_H .

2.2.4 Phase Mismatches in Edge-Sampling Channels (AFE)

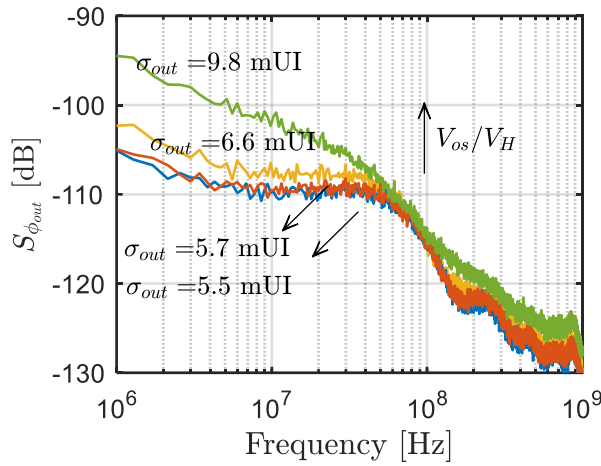
The delay mismatch between channels is due to the RC time variation (random mismatch and layout dependent effects). The effect mechanism for such error is the same as the clock skew's issue (without DCD). This is because the PD measures the relative phase error between the data and clock i.e. ϕ_e , and is incapable of discriminating between the error sources [Fig. 2.43]. The only difference is that the output phase spectrum (clock) in this case would be spurious free.

2.2.5 Jitter due to the Additive Noise in PAM4 (AFE)

Every block of CDR can introduce some amount of random noise which can cause excessive jitter during clock and data transitions. Since the slew rate (SR) in PAM is different for the large, medium and small eyes, the RMS jitter due to the additive noise would be a function of the transitions type as well. Any voltage perturbation dV at the sampling instance of t_s can be converted to



(a)



(b)

Figure 2.42: (a) ϕ_{os} spectrum for different values of V_{os} , (b) ϕ_{out} spectrum for different RMS values of V_{os} relative to V_H while $\phi_{in} = 20$ mUI vs ideal case, only small and large transitions are considered. Loop parameters are: $K_P = 1$ mUI, $K_I = 0$, $N_d = 8$. Only large and small transitions are considered.

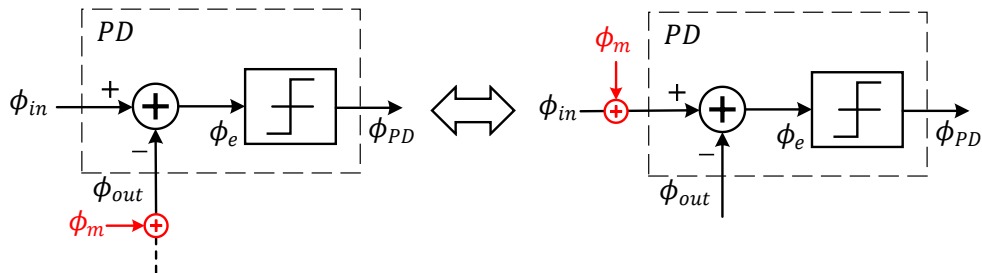


Figure 2.43: The similarity between phase mismatch in data and clock path, the PD cannot discriminate between the source of the errors. Although the effect mechanism is similar, the spectrum of ϕ_{out} for the (right) is spurious-free.

the corresponding jitter value ($d\phi$) using:

$$d\phi(t_s) = 2\pi f_s \frac{dV(t_s)}{SR} \quad (2.47)$$

$$\sigma_j = \left(\frac{2\pi f_s}{SR}\right) \sigma_n \quad (2.48)$$

σ_n and σ_j are the standard deviation of the voltage noise and jitter respectively. Assuming single-pole frequency response for the input channel, the SR expression becomes:

$$V_{out} = V_H(1 - e^{-t/RC}) \rightarrow SR = \frac{dV_{out}}{dt} = \frac{V_H}{RC} e^{-t/RC} \quad (2.49)$$

wherein V_H is the related eye's height. For the large and small eyes the threshold is centered then at the time of crossings $V_{out} = V_H/2$ and $SR = V_H/2RC$. Substituting this in Eqn. 2.48 and, as $f_{BW} = 1/2\pi RC$, it yields:

$$\sigma_j = \left(\frac{f_s}{f_{BW}}\right) \left(\frac{2\sigma_n}{V_H}\right) \quad (2.50)$$

It should be noted that, even though increasing f_{BW} results in steeper transitions, the second term $2\sigma_n/V_H$ would create a direct dependency. In other words, because σ_n is obtained by integrating the noise over the bandwidth ($\sigma_n \propto \sqrt{f_{BW}}$), it follows that ($\sigma_j \propto (\sqrt{f_{BW}})^{-1}$). Since $V_{HS} = V_{HL}/3$ using Eqn. 2.50 yields $\sigma_{jS} = \sqrt{3}\sigma_{jL}$. For the medium transitions however depending on the transition type i.e. falling or rising edge the amount of excessive jitter due to the additive noise is different, we assume the worst case which happens when $V_{out} = 0.75V_H$ and considering $V_{HM} = (2V_{HL})/3$, using Eqn. 2.50 yields $\sigma_{jM} = \sqrt{3/2}\sigma_{jL}$. For instance, with the assumption of $f_{BW} = 0.7f_s$ and $V_{HL} = 200$ mV, a random noise with $\sigma_n = 1$ mV would result in RMS jitter of $\sigma_{jL} \approx 2.3$ mUI(= 82 fs), $\sigma_{jM} \approx 2.8$ mUI(= 100 fs) and $\sigma_{jL} \approx 4$ mUI(= 140 fs) for a 28 GBd PAM4 signal.

2.3 Chapter Summary

In this chapter we laid out the system-level description of the CDR and developed a behavioral model for it. We proposed the Tri-level PD for PAM4 operation which results in better trade-off between the jitter generation in CDR and its bandwidth while dealing with the medium level transitions.

A behavioral model for CDR including the PD, Majority Voting (MV), Loop Filter and DPC is developed. Addition of integral path to increase the loop tracking capability in the presence of frequency offset is covered in details. The relation between proportional path and integral path gains in determining the jitter peaking is studied as well. The impact of long delay because of the digital implementation in CDR's loop dynamics is explained. It was shown that to avoid exciting the limit cycles and hence reducing performance degradation, certain constraints have to be satisfied which affect the maximum proportional path gain.

In addition, the influence of circuit imperfections from AFE and DPC were investigated and the necessity for inclusion of calibration and trimming blocks were outlined. Table 2.1 summarises the effect of different loop parameters and circuit level impairments on the CDR's loop dynamics.

Table 2.1: Summary of the design parameters and impairments with their impact on CDR dynamics

Design parameter/impairment	Description and impact
Input jitter	Due the nonlinear PD the input jitter amplitude affects the gain and BW
K_P	the proportional path gain, increasing K_P increases the loop gain and bandwidth
K_I	the integral path gain, enhances the phase tracking/JTOL in the presence of frequency offset
τ_I	the integral path time constant (K_P/K_I), similar to damping ratio in linear systems, determines the Jitter peaking in JTRAN
N_d	the total delay around the loop, excessive delay can cause stability related issues i.e. limit cycles and jitter peaking
Δ	quantization noise introduced by the DPC, increases the jitter generated in the loop
α_T	transition density, the higher the transition density the higher the PD's gain and the loop BW
Multilevel transitions	imposing a trade-off between the BW and the systematic DDJ generated in the loop
DEMUX ratio	dictated by the number of sampling channels in the AFE and DLC, inversely affects the MV averaging window and the loop BW
Clock skew and DCD	Causes phase modulation of the recovered clock. PD sensitivity is reduced, reducing the gain which increases the jitter generated inside the loop
DPC non-linearity	DNL of the DPC can cause excessive phase dithering at high jitter frequencies increasing the noise floor. INL makes the loop dynamics dependent on static phase shifts in the input
Voltage offsets in AFE	Creates a "dead zone" in the BBPD response which, in turn, causes a reduction in loop gain. Reduced loop gain increases the jitter generated by the control loop
Phase mismatches in edge sampling channels	the effect would be similar to the clock skew and DCD case

Chapter 3

CDR's Circuit Level Design

This chapter presents the circuit-level design of the CDR using 65-nm CMOS technology. The three main building-blocks are designed to meet the specs required for operating with the 28 Gb/s PAM4 input (200 mV differential swing). The three blocks are Analog Front End (AFE), Digital Loop Controller (DLC) and Digital to Phase Converter (DPC or MPCG) as shown in Fig. 1.11. The AFE includes the sample and hold (S&H), input buffers (amplifiers) and comparators array. Most of the related contents for the AFE section (except the comparator and DAC parts) are taken from [20] which was part of a project developed in our group and published prior to this work.

Inside the AFE, the input that is sampled by the (S&H) blocks is converted to full swing voltages representing the NRZ data embedded in the input's multi-level amplitude and also the edge samples containing the phase information necessary for phase detection. The AFE also provides the first 1 : 4 DEMUX for both data and edge samples. The main recovered data is also taken from this part of the circuit (7 Gb/s). The AFE outputs then are fed to DLC part but first they are down-converted further by a 1 : 4 DEMUX to lower data-rates (1.75 Gb/s) which can be handled by the digital section. The DLC's digital part includes BBPD, MV, LF blocks. The 7-bit LF output is encoded into 16-bit thermometer (32 complementary bits for differential switching) and eight one-of-n logic bits. This 40-bit bus encompasses the control signals for the DPC's PR block which decides the polarity and magnitude of the phase steps that the output clock has to make.

Additionally, as discussed previously in chapter 2, circuit imperfections cause a deterioration in the CDR operation, hence some trimming and calibration

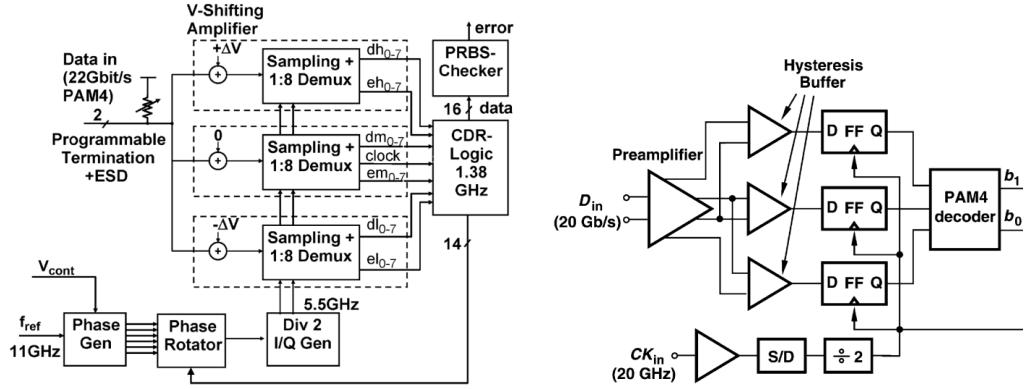


Figure 3.1: Analog Front End sections used in [19] (left) and [37] (right)

procedures are deemed necessary to mitigate those effects. For this reason, the AFE is equipped with the voltage offset calibration block which also sets the reference voltages for the slicers, the DPC(MPCG) is designed with delay trimming capability for de-skewing the multi-phase clocks which are explained in details in the following sections.

3.1 Analog Front End (AFE)

3.1.1 Input sample and hold and buffers

Several analog front-ends for amplifying and detecting PAM constellations have been reported in the literature [19], [37] and [38]. The front-end of the 22 Gb/s PAM-4 CDR from [19] (see Fig. 3.1) used three voltage-shifting amplifiers to generate amplified copies of the input signal, with two copies shifted by an offset $\pm\Delta V$. A second set of 12 amplifiers was then used to implement a half-rate architecture and remove the random dc-offsets due to mismatches in the subsequent current-mode logic (CML) D-flip flops. The D-flip flops and sense amplifiers regenerate the data and edge samples to full logical levels. The half-rate sampling makes it difficult to scale this architecture to 56 Gb/s in 65-nm CMOS. Additionally, note that the voltage shifting amplifiers and 2nd stage amplifiers need to be linear across an extended range equal to the input swing $\pm\Delta V$, which makes the design of these amplifiers difficult.

The authors in [37] implemented a 20 Gb/s PAM-4 receiver by merging the voltage shifting amplifiers into one structure [Fig. 3.1] consisting of two differential pairs thus reducing power consumption. Similar to [19], this structure creates three differential copies of the input, with each copy centred on its own

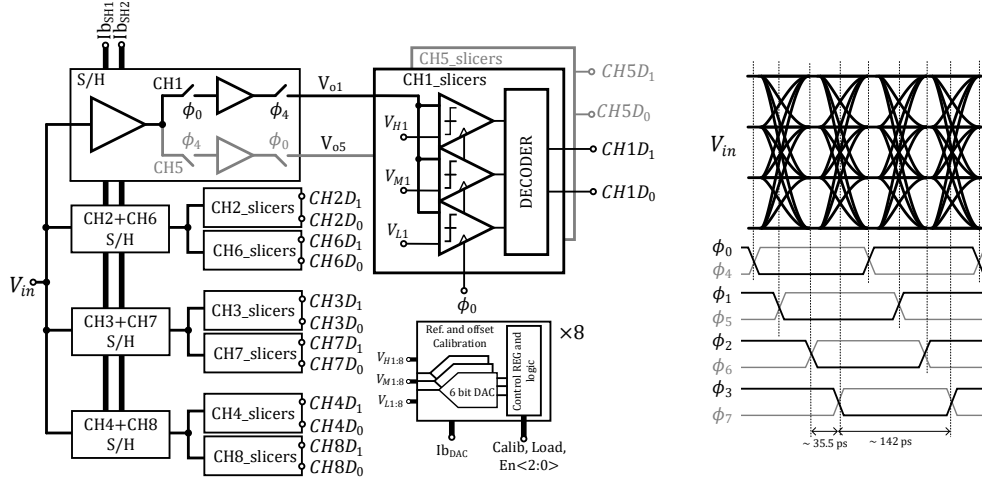


Figure 3.2: The proposed AFE architecture and the timing diagram for the sampling phases

common-mode (CM) voltage. A second set of amplifiers with hysteresis were used to clean up ambiguous transitions prior to regenerating the signal into digital bits using CML D-flip flops. Note that both the 1st and 2nd stage amplifiers need to operate at the full bandwidth. The D-flip flops operated at the full clock rate making it difficult to scale this architecture to 56 Gb/s. Again, the design of the merged amplifier is difficult due to the need for an extended output CM range. A similar approach was used in [38] for a 10 Gb/s capable PAM-4 front-end. In [39], a flash ADC was used for a 2.5 Gbaud, 10 Gb/s dual-mode PAM-10 signal. However, such a full-rate flash ADC does not scale easily to 56 Gb/s due to the time required for the comparators to make a decision on the input level.

To overcome these difficulties, the 1:8 interleaved architectures in Fig. 3.2 is proposed: a 1st stage of four high-speed buffers distributes the differential input signal to pairs of master sample-and-hold (S&H) circuits, each controlled by complementary sampling clocks. The sampling clocks run at 1/8th of the total bitrate (7 GHz for 56 Gb/s). A 2nd set of differential buffers then drives slave S&H circuits, which are driven by the opposite clock phase of the corresponding master S&H circuit's sampling clock. The samples stored by the slave S&H circuits are regenerated to a thermometer code by a set of 3 clocked (differential) dynamic comparators for each of the 8 channels. Two of these comparators have a built-in differential dc offset $+\Delta V$ and $-\Delta V$ respectively, while the middle comparator has no dc-offset. Unavoidable dc-offsets due to mismatches in the buffers and comparators are compensated by calibrating the dc-offsets of the comparators themselves. It can be shown that gain mismatches between buffers can also be removed through calibrating the dc-offsets of the

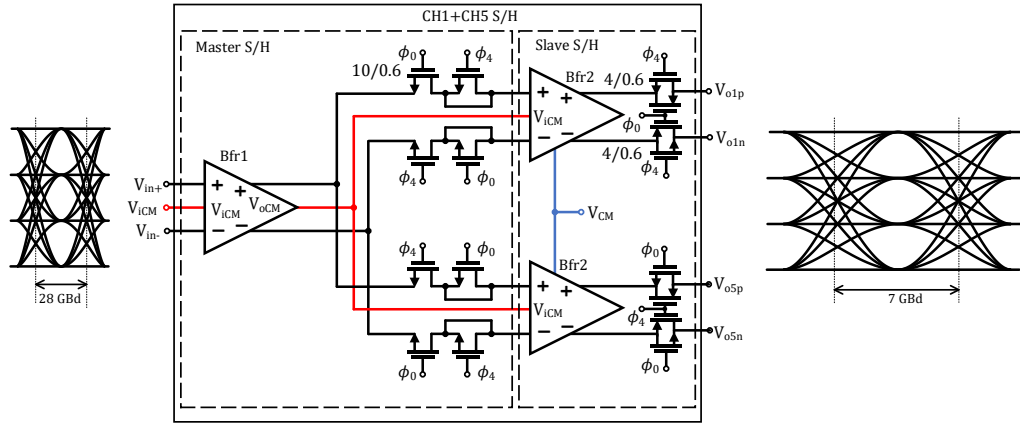


Figure 3.3: detailed schematic of the sample and hold section

comparators. This is explained in section 1.2. Note that the range over which the 1st stage and 2nd stage buffers need to be linear is equal to the input signal swing. This is because the offset is generated in the comparators rather than the buffers/amplifiers thus relaxing the buffer requirements compared to [19], [37].

For a conventional 1:8 interleaved structure, normally 8 buffers would be required to avoid charge sharing during those time intervals where the sampling clocks overlap. However, by grouping the sampling clocks in complementary pairs (ϕ_0 and ϕ_4 , ϕ_1 and ϕ_5 etc. [Fig. 3.2]) one channel will be in sampling mode while the complementary channel will be in hold mode thus avoiding charge sharing. This allows halving the number of input buffers saving power and reducing the capacitive load on the input. Note that by driving two S&H circuits from the same buffer kickback noise from the comparator that is being reset would couple onto the hold capacitor of the other channel. The use of the 2nd stage buffers and slave S&H circuits isolates the channels avoiding kick-back noise from disturbing the sampling operation. Note that as the 2nd stage buffers have relaxed bandwidth requirements (≈ 7 GHz) compared to the 1st stage buffers (which need at least 20 GHz bandwidth¹), their bias current can be substantially reduced.

The main advantages of the master/slave sampling front-end can be understood by considering the sampling circuitry as shown in Fig. 3.3 The first S&H circuit must have sufficient (> 20 GHz) bandwidth to sample the 56 Gb/s PAM-4 signal. Such a wideband S&H circuit can be realized using NMOS switches as long as the input voltage to the NMOS switches is sufficiently near the ground

¹Calculated by using $f_{BW} = 0.7R_b$, for a PAM4 input with symbol rate, R_b , of 28 GBd.

rail to maintain a small on-resistance. However, this conflicts with the CM requirements for the dynamic comparator. Indeed, this comparator uses an input based on an NMOS differential pair to ensure high-speed and hence needs a sufficiently high CM voltage to maintain the input in the saturation region. These conflicting requirements can be broken by the slave S&H circuits: indeed, as the slave S&H circuits sample the signal held by the master S&H circuits, their bandwidth requirements can be relaxed: (≈ 7 GHz) is sufficient, Table 3.1. A parallel combination of an NMOS and PMOS transistor can be used as a sampling switch which can support higher input voltages. Using the 2nd buffer the CM voltage at its output can now be raised and fixed to a given reference: a value equal to half the supply voltage was found to be optimum for the dynamic comparator. Fixing the CM voltage at the input of the comparators to a given reference also helps with the calibration of dc-offsets, as the differential dc-offset of the comparator depends on the input CM voltage.

Table 3.1: Design requirements for the master/slave sample and hold

Requirements	Master S&H	Slave S&H
Bandwidth	> 20 GHz	> 7 GHz
CM Level	Near the GND	$V_{DD}/2$
Sampling Switch	NMOS	NMOS+PMOS
Buffer Config.	Source Follower	Common Source

Finally, note that the master S&H circuit only uses one shorted NMOS transistor in series with the main sampling switch to cancel clock feedthrough and charge injection. This can be done as each output phase of the 1st buffer drives two sampling switches which are controlled by complementary clocks, hence cancelling each other's clock feedthrough and charge injection. The elimination of these transistors reduces the load on the clock generator. Due to the low supply voltage and the linearity requirements for the PAM-4 constellation the design of the two buffers is critical in terms of the dc levels. Additionally, accurate biasing is required to ensure repeatable gain and bandwidth performance across process, supply voltage and temperature (PVT) variations.

Fig. 3.4 shows the 1st buffer which consists of source followers M1 and M2. The output CM voltage V_{oCM} of the 1st buffer is required by the 2nd buffer. Rather than adjusting the output CM voltage V_{oCM} to a known reference using a CM feedback (CMFB) loop, here the input CM voltage of the 1st buffer is set to a fixed V_{iCM} via the $50\ \Omega$ termination resistors at the input. This is done to counter variations in the on-resistance of the switches in the master

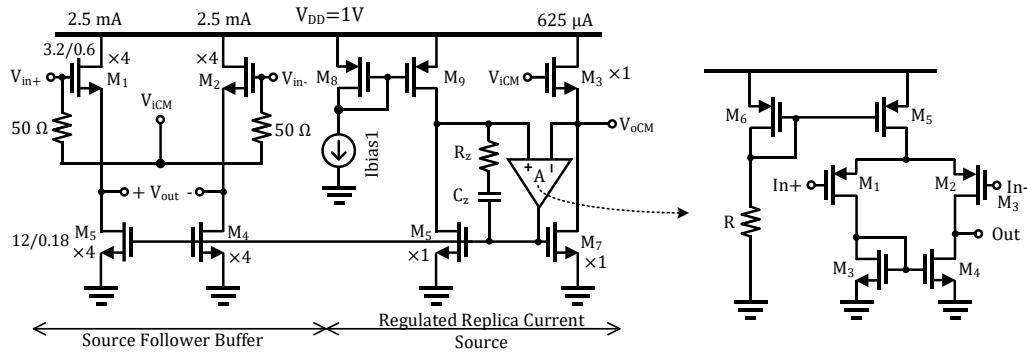


Figure 3.4: Schematic of the first-stage buffer

S&H circuit due to process and temperature related variations of the NMOS's threshold voltage. For example, in the slow corner the threshold voltage of M1 and M2 is higher than its typical value: as the input, CM V_{iCM} , to M1 and M2 is fixed, this will lower the output CM voltage, V_{oCM} . In turn, this lower output CM voltage reduces the on-resistance of the master S&H circuit's switches (see Fig. 3.3), thus compensating for the increase in threshold voltage of the switches themselves.

As the output CM voltage V_{oCM} is unknown, it is reconstructed using a scaled ($\div 4$) replica M3 of the transistors M1 and M2, M3 is biased with the same (again scaled by $\div 4$ to save power) bias current as M1 and M2: hence its output voltage equals the output CM voltage V_{oCM} . To ensure high-speed, current source transistors M4 and M5 use devices with small lengths making accurate current mirroring difficult. Here this is solved by forcing the wanted bias current I_{bias1} through transistor M6. Using operational amplifier, A, the gate voltage of M6 (and hence current source transistors M4, M5 and M7) is adjusted such that its drain voltage equals V_{oCM} . As M4, M5 and M7 now have the same drain ($=V_{oCM}$) and gate voltages, their drain currents are equal to $4 \times I_{bias1}$ neglecting modulation of M4 and M5's bias current due to the high-speed input) and I_{bias1} (for M6 and M7).

To achieve sufficient bandwidth, the bulk connections of source followers M1 and M2 in the 1st stage buffers cannot be connected to their sources. Therefore, the input signal is attenuated: the 2nd stage buffer provides amplification to compensate for this attenuation. Simulations suggest this attenuation has negligible impact on the signal-to-noise (SNR) ratio. The schematic of the 2nd buffer is shown in Fig. 3.5: it consists of a PMOS differential pair M1 and M2 loaded with a differential load resistor R1. A degeneration resistor R2 and capacitor C sets the gain and provide a zero for bandwidth extension. The reconstructed

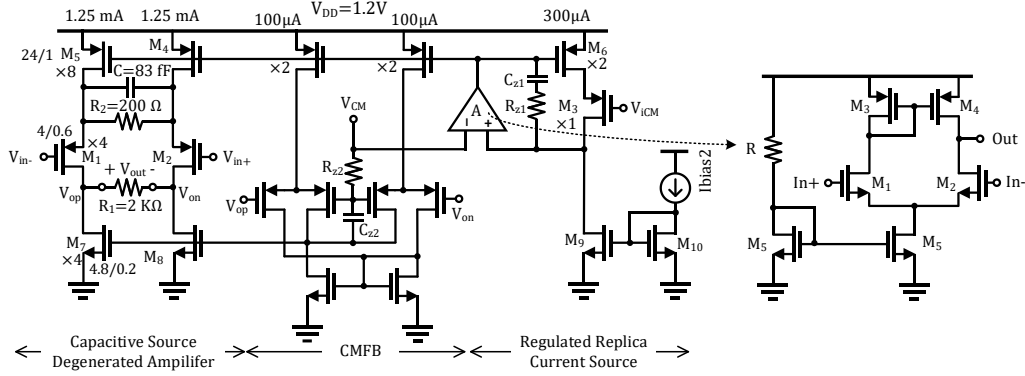


Figure 3.5: Schematic of the second-stage buffer

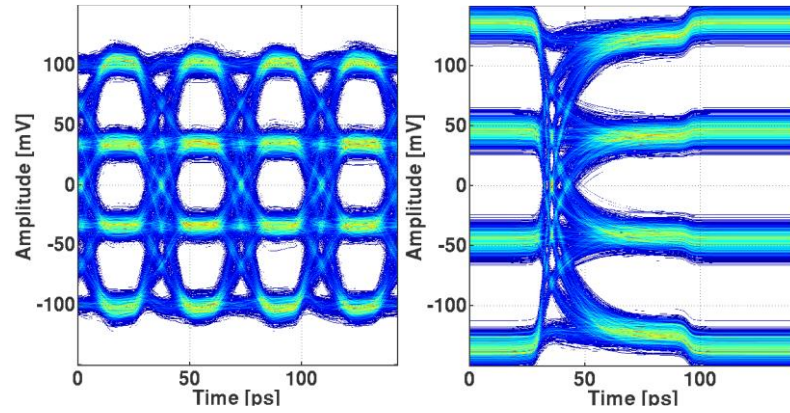


Figure 3.6: Eye diagram of the input (left) and output(right) [3.3]

output CM voltage V_{oCM} from the 1st stage buffer is used to accurately define the bias currents by adjusting the gate voltage of current source transistors M4 and M5. A CMFB loop adjusts the output common-mode voltage to V_{CM} ($\approx$ half the supply voltage, $V_{DD}/2$), which is required for the dynamic comparators. The simulations took into account layout parasitic and were done across process, supply voltage ($\pm 5\%$) and temperature (25°C to 110°C) corners, Table 3.2. The nominal supply was 1.0 V for the 1st stage buffer and 1.2 V for the 2nd stage buffer. Each 1st stage buffer consumed 6.9mA and each 2ndstage buffer used 2.9 mA(each time including the bias circuitry). A transient simulation of sampling a 56 Gb/s input signal is given in Fig. 3.6.

Table 3.2: Simulation results for the first and second stage buffers

	1 st Stage's BW (GHz)		2 nd Stage's BW (GHz)		Total Gain (dB)	
	$T = 25^\circ\text{C}$	$T = 110^\circ\text{C}$	$T = 25^\circ\text{C}$	$T = 110^\circ\text{C}$	$T = 25^\circ\text{C}$	$T = 110^\circ\text{C}$
Typical	30	27	11.8	11	2	0.2
Fast/Fast	34	31	14.7	13.5	1.4	0.1
Slow/Slow	26	23	9.7	8.9	1.8	-0.2

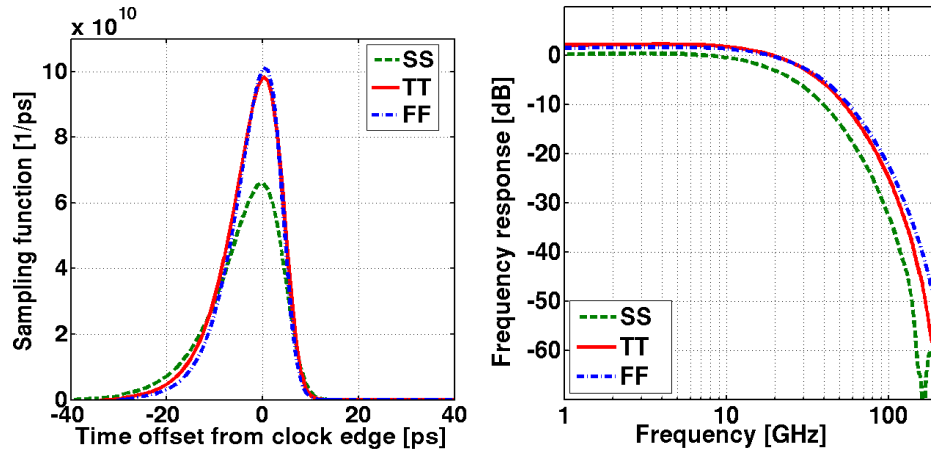


Figure 3.7: SFs and frequency responses for typical and extreme corners

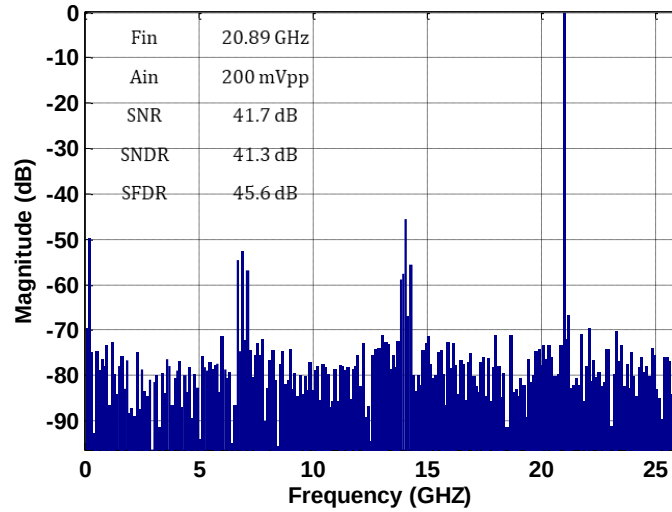


Figure 3.8: Single-tone FFT of S&H output

To quantify the bandwidth and timing resolution of the sampling front-end, the methodology presented in [40] and extended for latching in [19] and [41], is used: the output V_{TH} of a S&H circuit after the switch has been turned off can be expressed as an integral of the input, $V_{in}(t)$, up to the moment where the sample is taken multiplied by a weight function $h(t)$:

$$V_{TH}(t) = \int_{-\infty}^{+\infty} V_{in}(\tau)h(t - \tau)d\tau \quad (3.1)$$

with $h(t)$ known as the ‘‘Sampling Function (SF)’’ [40] or ‘‘Impulse Sensitivity Function (ISF)’’[42]. The aperture time is defined as the time width that bounds 80% of the area under the SF curve, see [19]. The Fourier transform of the SF then gives the frequency response of the S&H circuit from which its 3-dB bandwidth can be obtained, Fig. 3.7. The aperture time and 3-dB bandwidth

(derived from the SFs, Fig. 3.7) are given in Table 3.3 assuming 20 ps clock rise and fall times: the worst-case aperture time is 17 ps which is less than the 35 ps symbol width at 28 Gbaud. The worst-case bandwidth is 18.82 GHz which is somewhat less than the bandwidth of the buffers alone due to the finite fall time of the clock, but still sufficiently large compared to the 14 GHz Nyquist frequency of a 56 Gb/s, 28 Gbaud PAM4 signal.

Table 3.3: The Sampling Function and sampling frequency response of the Master/Slave sample and hold

Sim. Corner	80% Aperture Time (ps)	3-dB Bandwidth (GHz)
Typical ($T = 25^\circ\text{C}$)	14	22.9
Fast/Fast ($T = 25^\circ\text{C}$)	13	25.1
Slow/Slow ($T = 110^\circ\text{C}$)	17	18.8

The linearity of the circuit is tested by applying a single-tone sinusoid (with the frequency of 20.89 GHz) and taking FFT of the output signal as shown in Fig. 3.8. Finally, the cyclostationary sampled noise (including the buffers and kT/C noise) was found (using SpectreRF pss and pnoise simulations) to be 1.42 mV (differentially, at the output of the 2nd S&H circuit). Assuming an optical receiver, the required SNR to receive a PAM-4 signal with a bit-error rate of 10^{-12} is 26.5 dB. The 1.42 mV noise from the sampling front-end then results in a negligible 0.2 dB SNR degradation.

3.1.2 Comparators (Slicers) and offset calibration DACs

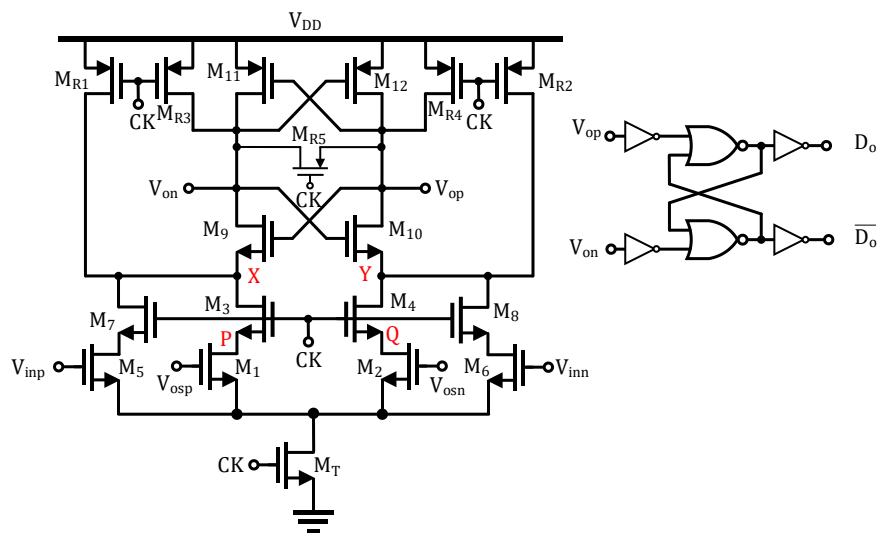


Figure 3.9: Schematic of the comparator

As shown in Fig. 3.9 the design uses dynamic comparators to convert small input differences to full-swing rail to rail outputs. This architecture is preferred over the CML based latch due to its power efficiency (no static power consumption) and short regeneration time [19], [43]. The core circuit is based upon the so-called Strong-Arm architecture [44] which has two phases when the CK is high:

- a) Initial amplification phase: M1 and M2 start to draw current from node P, Q, X and Y. Since the initial voltage in X and Y during the reset time is set to VDD the cross coupled transistors are off until one of the nodes voltage drops to $V_{DD} - V_{TH}$.
- b) Second amplification phase followed by regeneration: As M9 and M10 start to conduct current, output nodes voltages, V_{op} and V_{on} begin to change at different rate as well which eventually enables the positive feedback, causing the cross coupled pairs to enter regeneration mode. The node with higher voltage would increase to V_{DD} while the lower output decreases toward the ground.

The reset transistors (MRx) ensure that no charge from the previous state affects the current decision. Incomplete discharging during the reset phase would cause dynamic offset issues which translates to hysteresis in the comparators characteristic. MR5 shorts the two outputs together during the reset phase which mitigates the initial voltage difference due to mismatches providing further offset reduction .

The major drawback of the Strong-Arm comparator is the kick-back noise injected through the capacitive paths mainly from the outputs. The addition of M3, M4, M7 and M8 provides shielding by isolating the input transistors from the output [45].

The output of the Strong-Arm undergoes reset in every clock cycle. To retain the output states until the next conversion, a latch is added to the output. The connection to the SR latch is through the inverters isolating the two positive feedbacks inside the SR latch and the comparator. The output of the slicers array is thermometer code. It is converted to binary code by a decoder. Intermediate buffering of the slicers outputs with inverters produces asynchronous gain avoiding metastability issues.

Unlike [45], instead of using a shared transistor to isolate the inputs from the outputs, the design splits the reference and signal paths transistors, allocating separated connections to X and Y. The reason for such modification is that the

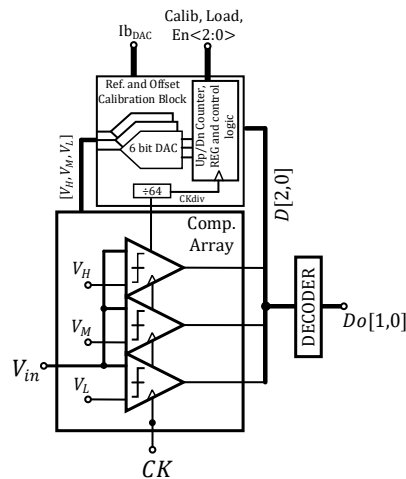


Figure 3.10: Single channel comparators' array and offset calibration block diagram

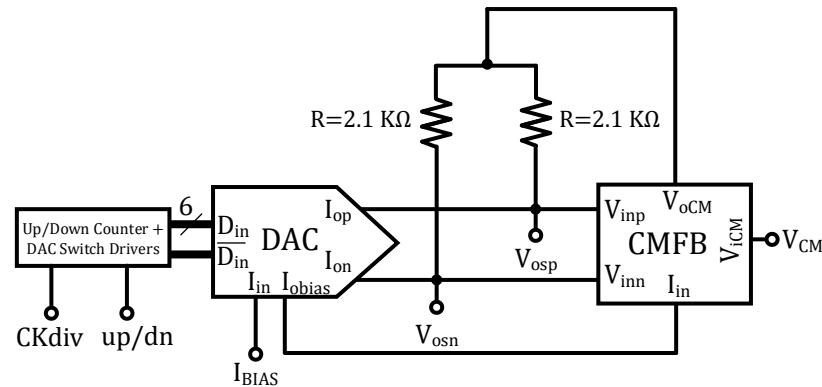


Figure 3.11: Schematic of the Calibration DAC with CMFB

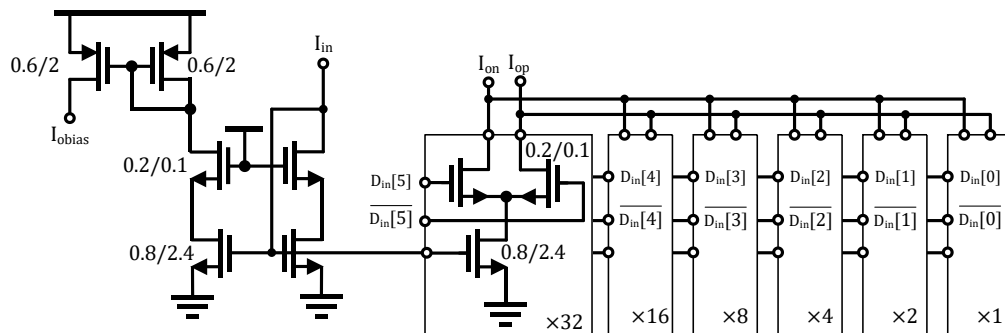


Figure 3.12: Detailed DAC circuitry

reference values (once calibrated) remain constant and would not be changing over the cycles therefore the parasitic capacitance of the reference pairs, M5 and M6, can be excluded from the P and Q nodes. This increases the amplification phase BW for the input difference whereas the overall capacitance seen from X and Y is unchanged. Although such a connection can increase the mismatch effects, this can be corrected by the offset calibration scheme.

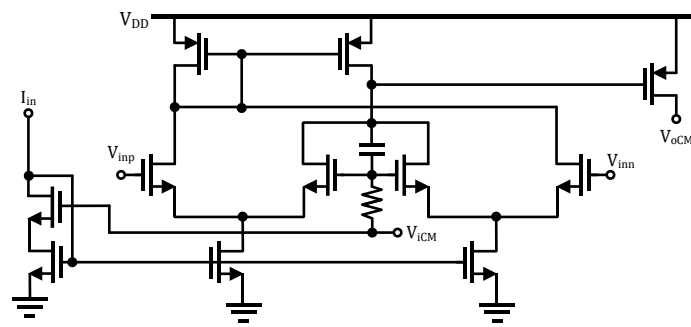


Figure 3.13: Detailed CMFB circuitry

Since the dynamic comparator would suffer from large offset voltage in the presence of mismatches, a calibration method is employed to reduce the input referred offset. A 6-bit DAC² is used to correct the offset through the calibration loop, as shown in Fig. 3.10 and Fig. 3.11. The DAC is based on a current steering topology with binary weighted cells as shown in Fig. 3.12. The resolution of the current cells is set to be $2 \mu A$, which with $R = 2 K\Omega$, the DAC output voltage amplitude is 252 mV. The fully differential operation necessitates a proper CM level control. This is done by the feedback mechanism which senses and compares the CM level with a desired value, V_{CM} , through an amplifier, Fig. 3.13. The current to the DAC cells is mirrored to this section as well to create better control over biasing levels. The CMFB loop frequency response has been compensated by addition of the R_z and C_z at the input, V_{iCM} .

The calibration scheme is foreground which requires it to be performed once at start-up. The procedure is as follows: suppose the differential input to the comparator is set to zero, in the presence of offset the output would prefer to stay in one state as the comparator is clocked. This would drive the up/down counter to increment (or decrement) the input to the DAC which produces a differential voltage at V_{osp} and V_{osn} . The counter keeps changing in one direction until the output state toggles between opposite states indicating that the loop has corrected the offset. At this point the thermal noise is the dominant source for decision errors. It should be noted that the offset calibration block is clocked at lower speed (64 times slower) hence decreasing the amount of power required for this section.

Every channel of the AFE is connected to an array of three comparators resolving the 2-bit information of the input PAM4 signal. The three references re-

²Although simulations suggested that a 5-bit DAC could provide sufficient accuracy by bringing the offset below the required level, a 6-bit DAC is used for actual implementation.

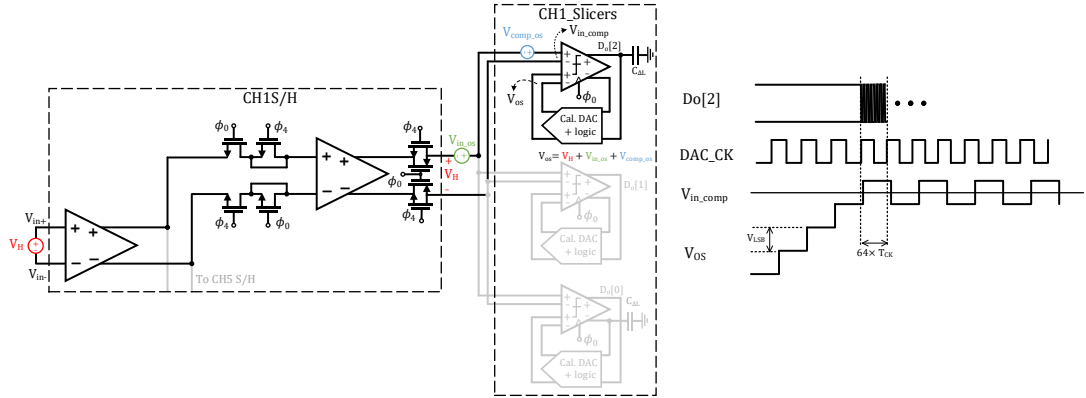


Figure 3.14: The reference setting and calibration process are combined. The procedure, with the signal diagrams, is shown for the setting of V_H . The calibration block is clocked 64 times slower than the comparators block. When the calibration is complete the output of the comparator dithers. This calibration block simultaneously sets all the V_H references for all the 8 channels, the procedure is repeated for the V_M and V_L references

quired for defining the decision thresholds are set during the offset calibration. The main advantage is that the entire offset of the AFE channels, including the input buffers and S&H switches, can be easily corrected as they will be added to the main input and referred to the input of the associated comparators. This means that by setting the input of the AFE to the required reference level i.e. V_H , V_L or 0^3 , $V_{os} = V_{osp} - V_{osn}$ will settle around a value that in addition to the comparators offset, encompasses the effect of all the offset introduced in the path, Fig. 3.14.

In addition to offset mismatch, the gain mismatch between channels could be present. However by means of the same calibration scheme the effect of the gain mismatch will be removed. As shown in Fig. 3.14 the calibration process defines the references at the input of the circuit for all channels, simultaneously. Therefore, during calibration, each channel (depending on the gain and offset) creates a scaled and shifted version of the reference in the input of the corresponding slicer, as depicted in Fig. 3.15. Since both the reference and input experience the same path non-idealities, the results are insensitive to the gain mismatch as well.

Since the high-level-decision and low-level-decision slicers compare the input with the non-zero differential references, V_H and V_L , ideally the corresponding DAC code wouldn't be settled mid-range i.e. its output is unable to cover the available dynamic range symmetrically. To rectify this, the output load of the

³All the inputs are differential

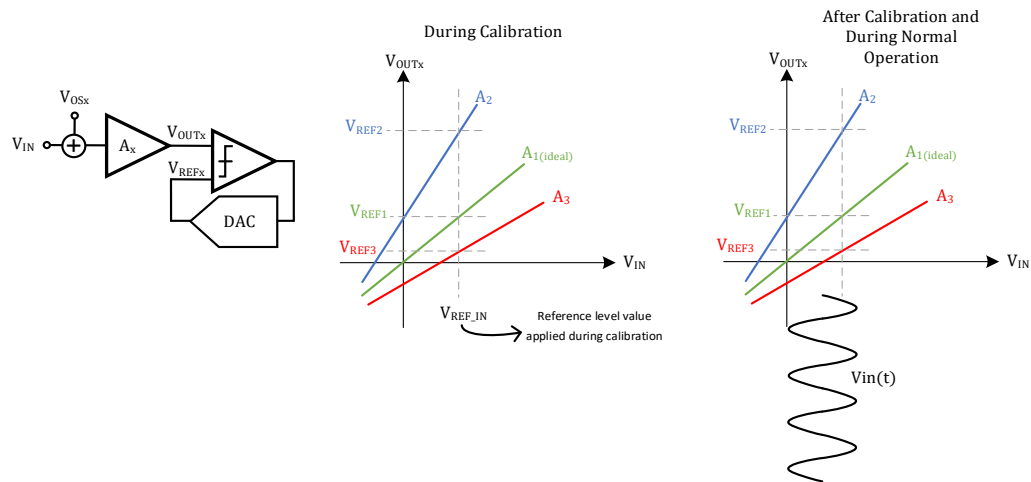


Figure 3.15: The calibration scheme removes the gain mismatch in addition to the offset mismatch between channels: during calibration, channels with different gain and offset would create their version of V_{REF-IN} i.e. V_{REF1} , V_{REF2} , V_{REF3} etc. During normal operation when $V_{in}(t)$ crosses V_{REF-IN} , all the slicers will change their output states, hence the final decision is insensitive to the gain and offset mismatches

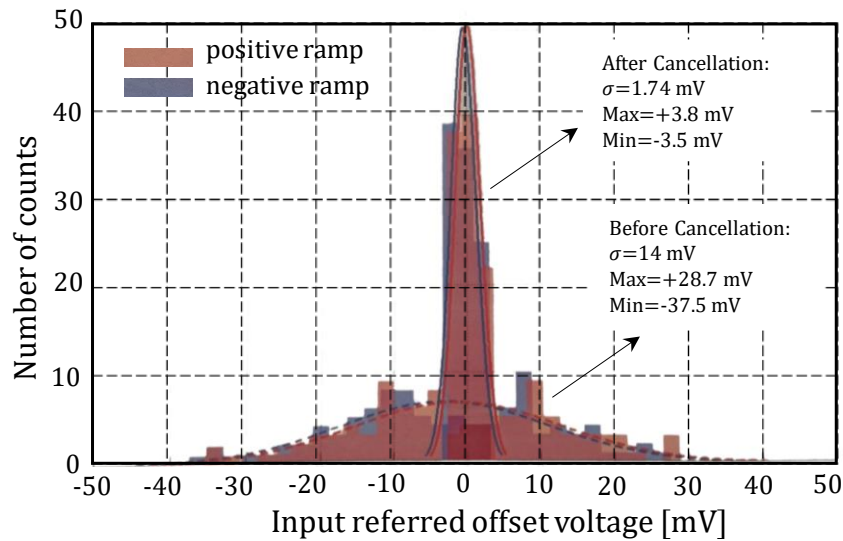


Figure 3.16: Comparator's offset before and after offset cancellation, the offset is shown for two scenarios in which the input is a positive and negative ramp. (for this simulation the DAC resolution is five bits)

slicers is intentionally unbalanced by adding some extra capacitors ($C_{\Delta L}$) as shown in Fig. 3.14, to the related slicers.

Once activated, the calibration engine sets the decision level of similar slicers in all channels simultaneously, in other words all the low-level slicers are enabled together and, once calibrated, the same step would be repeated for the mid-level and high-level slicers as well. External adjustment is also embedded in the design to allow loading of the DAC's input registers without the use of the

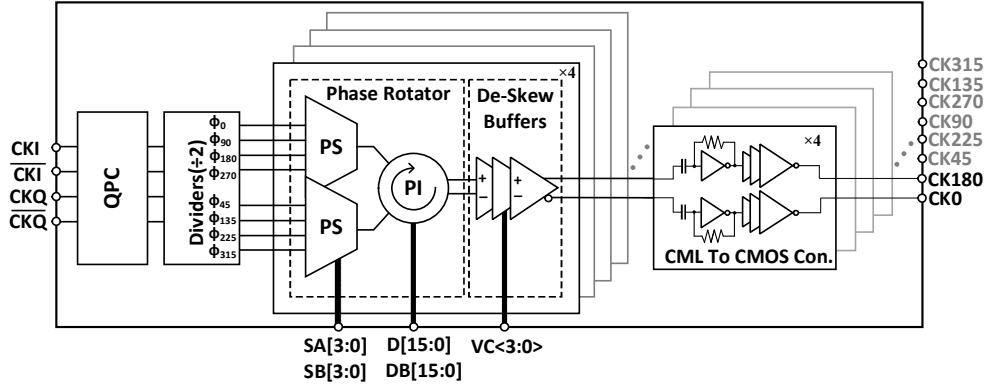


Figure 3.17: DPC block diagram

calibration loop. The simulation results for the comparator's offset before and after offset cancellation using the calibration loop is shown in Fig. 3.16 (excl. S&H and buffers). To simulate the comparator's offset the techniques described in [46] and [47] are employed and the input is set to be a varied ascending or descending ramp (taking into account the hysteresis effect). The comparator is able to resolve 10 mV input while operating at 7-GHz clock frequency and dissipate only 400 μ W of power, including the calibration DAC.

The simulated AFE section consumes 68 mW of power, out of which 56 mW is drawn from 1 V/1.2 V by the S&H and input buffers. The comparator (slicer) bank dissipates 12 mW of power from 1 V power supply.

3.2 Digital to Phase Converter (DPC)

The DPC block diagram is shown in Fig. 3.17. It receives CKI , $\overline{CKI}$, CKQ and $\overline{CKQ}$ as the main references and outputs eight evenly spaced phases from $CK0$ to $CK315$ at half the input rate. The code inputs including SA , SB , D and DB control the phase shifting of the output clocks while the reference voltage, VC , is used for relative phase adjustments.

3.2.1 Phase Rotator (PR)

The PR block consists of two phase selectors (PS)s followed by a phase interpolator (PI). The PSs multiplex and output two adjacent clock phases, $V_\varphi (= V_{PS}e^{j\varphi})$ and $V_\psi (= V_{PS}e^{j\psi})$ based on the input code. Then the PI generates the clock phase, $V_\theta (= V_{PI}e^{j\theta})$, by using the weighted sum of the φ and ψ phases:

$$V_\theta = A_{PI} \cdot (\alpha \cdot V_\varphi + \beta \cdot V_\psi) \quad (3.2)$$

wherein A_{PI} is the PI's voltage gain and the normalized weights α and β are controlled by the digital input code. By assuming φ as the reference phase and $\phi = (\psi - \varphi)$, then the code to phase characteristic function of the PI can be quantified as:

$$\theta = \arctan\left(\frac{\beta \sin \phi}{\alpha + \beta \cos \phi}\right) \quad (3.3)$$

Ideally, θ should sweep the phase difference between the two inputs in uniform steps with $\theta_{LSB} = \phi/2^{N_{PI}}$ in which N_{PI} is the PI's resolution.⁴ The α and β parameters can be estimated using the inverse form of Eqn. 3.3 similar to predistortion techniques, however this complicates the mapping of the digital codes to the weights. By allocating some margin for systematic errors, simpler functions like $\alpha + \beta = 1$, can be used to generate the weights. The resulted error has a code dependency which translates to nonlinearity in the PI's characteristic function. To improve the linearity, ϕ should be decreased which is limited by the number of available clock phases at the PR input. In our design, we use eight phases to cover the 360° phase rotation so $\phi = 45^\circ$. For the PI section $N_{PI} = 4$, which includes 16 steps with a nominal step size of approximately 2.8° and a maximum systematic error of 0.45° .

At multi gigahertz clock frequencies, f_{CK} , the weights α and β usually are implemented by using weighted current sources based on the current-steering topology and are merged with the input phases φ and ψ in a CML structure to synthesize Eqn. 3.2. Due to the amplitude saturation in CML circuits, harmonics of φ and ψ must be considered in Eqn. 3.2 which makes the phase linearity of the PI be dependent on the cell's output time constant τ_{out} . As explained in [48] to suppress such an effect, the input time spacing, $\phi/2\pi f_{CK}$, at most should be equal to τ_{out} . In other words:

$$\frac{\phi}{2\pi f_{CK} \tau_{out}} \leq 1 \quad (3.4)$$

Since $\phi = \pi/4$ and assuming that $f_{BW} = 1/2\pi\tau_{out}$ then following can be derived:

$$f_{CK} \geq \frac{\pi}{4} f_{BW} \quad (3.5)$$

stating that the introduced nonlinearity subsides at higher f_{CK} as long as the harmonics fall beyond the circuit bandwidth, f_{BW} . Therefore, the circuit behavior can still be examined by considering only the fundamental tone. Referred

⁴To simplify the expression, we ignore the offset in θ caused by the frequency dependent phase shift from A_{PI} .

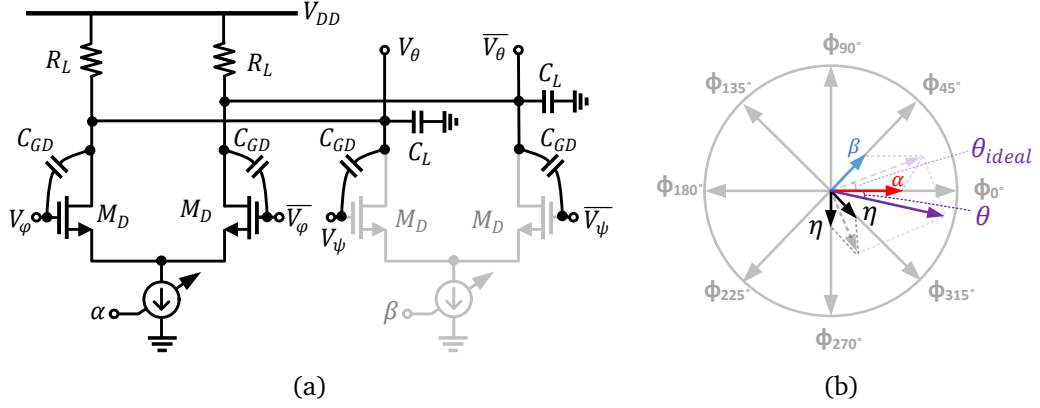


Figure 3.18: (a) PI unit cell's circuit, clock feedthrough by means of C_{GD} results in limited range. (b) addition of $-j\eta$ to the interpolation coefficients to model the effect, the input phases are $\phi = \phi_0^\circ$ and $\psi = \phi_{45^\circ}$

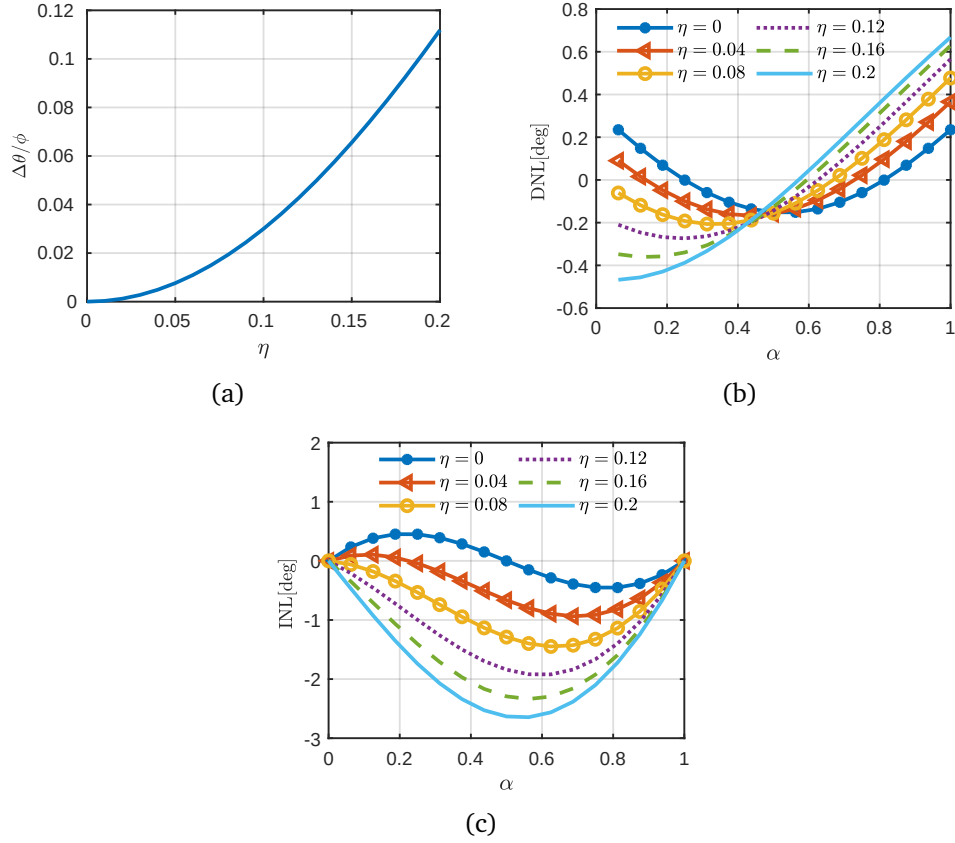


Figure 3.19: The effect of clock feedthrough η on the (a) gain error, (b) DNL and (c) INL of a single PI cell based on equation (8) by assuming $\phi = \pi/4$.

as type-I, the most common CML based PI circuitry is shown in Fig. 3.18(a) which is a dual-input differential amplifier with a current steering DAC as the tail current source. Based on the input code the total amount of available current is divided between the two input pairs. Thermometer coding is preferred

since it guarantees monotonicity in the presence of mismatch inside the unit cells and obviates phase glitches. Symmetrical loading is used to avoid any conversion of common mode noises, coupled from supply and substrate, into differential ones which results in excessive jitter[49]. The main disadvantage of the type-I is the large phase steps during boundary switching which arises from the phase feedthrough due to the gate-drain capacitance C_{GD} [50]. Through these capacitive paths some amount of input phases always appears at the output even though the associated weight is set to zero. This limits the available sweep range in every octant and can be referred as offsets in the main coefficients. By assuming $f_{CK}(= \omega_{CK}/2\pi)$ is close to f_{BW} and neglecting the higher order harmonics, Eqn. 3.2 becomes:

$$V_\theta = A_{PI} \cdot \left(\alpha + \frac{1}{A_{PI}} \cdot \frac{Z_L}{Z_L + Z_{GD}} \right) \cdot V_\varphi + A_{PI} \cdot \left(\beta + \frac{1}{A_{PI}} \cdot \frac{Z_L}{Z_L + Z_{GD}} \right) \cdot V_\psi \quad (3.6)$$

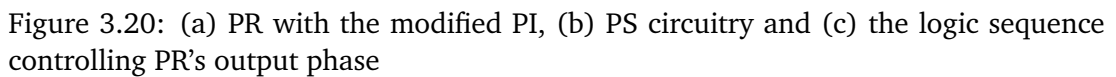
wherein $Z_{GD} = 1/j\omega_{CK}C_{GD}$ and $Z_L = R_L \parallel (1/j\omega_{CK}(C_L + C_{GD}))$. Since $A_{PI} = -G_m(Z_L \parallel Z_{GD})$ represents the main path gain and G_m is the effective input pairs transconductance hence the offset terms become:

$$\frac{1}{A_{PI}} \cdot \frac{Z_L}{Z_L + Z_{GD}} = -\frac{1}{G_m Z_{GD}} = -j \frac{\omega_{CK} C_{GD}}{G_m} \quad (3.7)$$

which implies that the amount of introduced offset is inversely proportional to the ratio of feedthrough path admittance and the input pairs effective transconductance. Note that the offset terms are phasors leading α and β by 90° in phase resulting in excessive deviation of θ as shown in Fig. 3.18(b). Using Eqn. 3.3 if $\eta = \omega_{CK}C_{GD}/G_m$ then:

$$\theta = \arctan\left(\frac{\beta \sin \phi - \eta(1 + \cos \phi)}{\alpha + \beta \cos \phi + \eta \sin \phi}\right) \quad (3.8)$$

Eqn. 3.8 indicates that θ 's sweep range is smaller than ϕ which squeezes the octants at the PI's output. Consequently, the maximum phase step occurs at the boundaries where the octants are switching. Using equation Eqn. 3.8 the gain error and INL/DNL of the PI is plotted for various values of α and η in Fig. 3.19. By ignoring the offsets in θ as η increases so does the amount of nonlinearity which is intensified at higher frequencies. A common solution is to isolate the input from the output as per the alternative architecture, type-II [50], which changes the order of the input transistors forming a cascode struc-



Let us reconsider the architecture of the type-I PI. It appears that the offsets in Eqn. 3.6 can be canceled by adding some negative terms. A feasible approach is to exploit the differential nature of the CML circuits. If the inputs and out-

puts of each differential pair are cross connected using capacitors, as shown in Fig. 3.20(a) the circuit is able to suppress the phase feedthrough. Through performing transient simulations at transistor-level based on Fig. 3.20(a) with clock frequency of 7 GHz, $\Delta\theta = \theta_{max} - 45^\circ \approx 3.5^\circ$ is observed while under the same conditions in the modified circuit $\Delta\theta \approx 2.5^\circ$. It should be noted that during input clock crossings the displacement current due to the large capacitance of the tail current sources causes further distortion of the output phase. Similar analysis can be carried out to model that effect but we skip over it here.

In Fig. 3.20(b) each PS circuit multiplexes eight inputs i.e. four differential clocks and selects the phase based on the input code. The circuit uses “1 of n” logic for the bits in SA and SB registers and the activated switches steer the current to the related differential pair. Asynchronous state changes in SA, SB, D and DB registers should be prevented since it would induce phase glitches.

Dynamic errors could still occur during boundary switching as it prompts momentary phase deviations in V_φ and V_ψ hence in V_θ . To decouple such phase disturbances from V_θ , the PR uses a decoder by which the simultaneous switching of V_φ and V_ψ is avoided. Instead of shifting V_φ and V_ψ by 45° during every octant traversing, only the phase associated with zero coefficient ($\alpha = 0$ or $\beta = 0$) is rotated by 90° while the other phase remains unchanged. To keep the phase rotation in the same direction, the coefficients register, D has to reverse the counting course in every boundary transition. The method is illustrated in Fig. 3.20(c).

The simulation results for the INL of the PR is shown in Fig. 3.21(a). With the residual error of $\Delta\theta \approx 2.5^\circ$ in the single PI cell, the gain error ($\Delta\theta/\phi$) with $\phi = 45^\circ$ is 0.05. By looking for the corresponding η value (≈ 0.125) in Fig. 3.19(a) and using Fig. 3.19(c) the related maximum INL is roughly -2° . Since $\theta_{LSB} = 2.8^\circ$ then the predicted maximum INL of $-0.71 LSB$ is close to the simulation results in Fig. 3.21(a).

3.2.2 Quadrature Phase Corrector (QPC)

The PR uses eight clock phases which are generated by using divided-by-two versions of the quadrature inputs. As Eqn. 3.8 implies, θ is dependent on ϕ and uneven octants in the PR's input cause deviation of ϕ from its nominal value of 45° , which introduces discontinuity in octant boundaries and deteriorates the overall linearity of the PR. One of the main sources of this static error is the

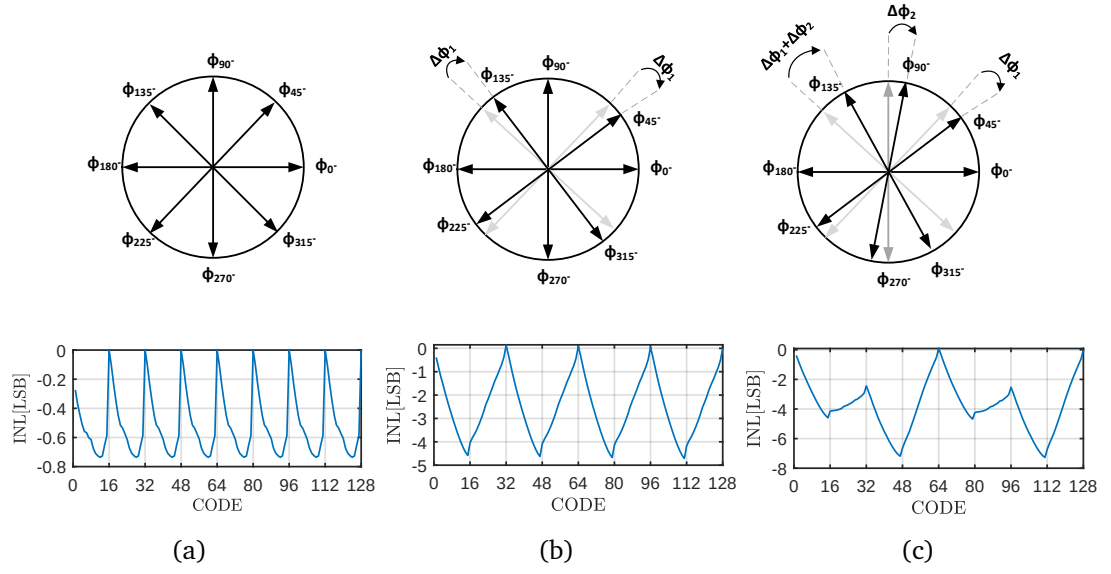


Figure 3.21: PR's INL profiles from the transient simulation with (a) ideal input phase, (b) phase imbalance due to the I/Q mismatch $\Delta\phi_1 = 12.5^\circ$ (@ 7 GHz) (c) phase imbalance due to the I/Q mismatch and duty cycle distortion resulted from preceding stages $\Delta\phi_1 = 12.5^\circ$ and $\Delta\phi_2 = 6.25^\circ$ (@ 7 GHz)

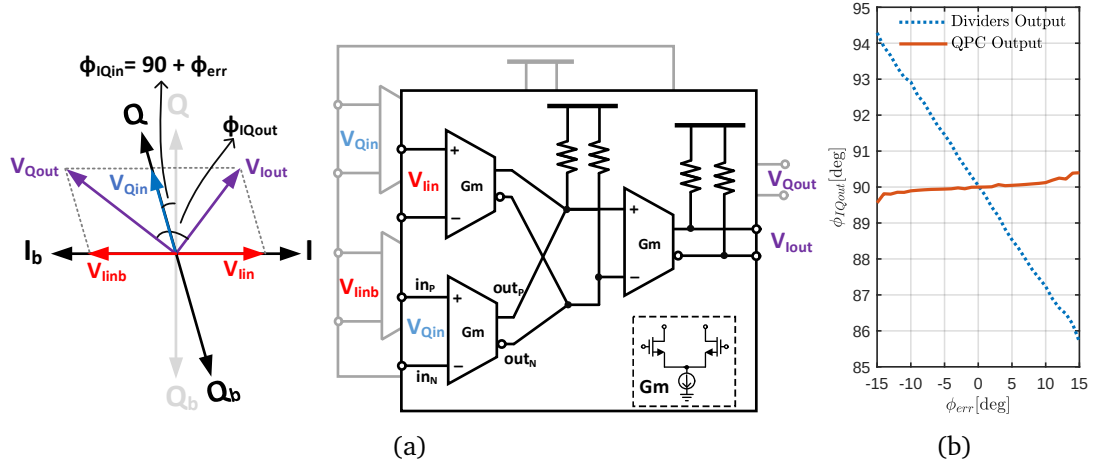


Figure 3.22: (a) Phasor diagram and schematic of the QPC. (b) Transient simulation shows the phase at the output of QPC and dividers vs the amount of input's I/Q mismatch.

I/Q phase mismatch at the input reference[51]. For detailed evaluation of the effects, the transient simulation of PR is repeated by assuming that $\Delta\phi_1$ represents the input I/Q phase mismatch as shown in the phasor diagram of the Fig. 3.21(b). It should be noted that since the reference signals are passing through the dividers, the input I/Q phase mismatch manifests itself as the relative rotation of the two phasor sets of $\{\phi_{0^\circ}, \phi_{90^\circ}, \phi_{180^\circ}, \phi_{270^\circ}\}$ and $\{\phi_{45^\circ}, \phi_{135^\circ}, \phi_{225^\circ}, \phi_{315^\circ}\}$ at the PR input. The resulting INL is plotted for $\Delta\phi_1 = 12.5^\circ$ (5 ps @ 7 GHz).

In addition to I/Q phase mismatch, duty cycle distortion (DCD) may shift the phases inside each of the phasor sets by $\Delta\phi_2$, as illustrated in Fig. 3.21(c), leading to further degradation in the linearity. For this case, the INL profile is computed with $\Delta\phi_1 = 12.5^\circ$ and $\Delta\phi_2 = 6.25^\circ$. To reduce the impact of I/Q phase mismatch, a simple quadrature phase corrector (QPC) with a new approach is presented.

The phasor diagram in Fig. 3.22(a) describes the method. By considering V_{In} as the reference phasor, we let the phase of V_{Qin} , ϕ_{IQin} , deviate from its ideal value, 90° , by an amount of ϕ_{err} . The QPC should generate quadrature signals with the phase of ϕ_{IQout} being independent of ϕ_{err} . We surmise that simultaneous rotation of the related I/Q phasors at the output with respect to ϕ_{err} may correct such error. This functionality can be implemented by blending the phases akin to performing phase interpolation with equal weights. Applying this concept in every quadrant results in a new I/Q constellation composed of V_{Iout} and V_{Qout} . As shown in Fig. 3.22(a) any presence of ϕ_{err} pulls both V_{Iout} and V_{Qout} in the same direction, hence keeping ϕ_{IQout} undisturbed. The relation between ϕ_{IQout} and ϕ_{err} becomes:

$$\begin{aligned}\phi_{IQout} &= \pi - \arctan\left(\frac{k \cos \phi_{err}}{1 + k \sin \phi_{err}}\right) \\ &\quad - \arctan\left(\frac{k \cos \phi_{err}}{1 - k \sin \phi_{err}}\right) \\ &= \pi - \arctan\left(\frac{k \cos \phi_{err}}{1 - k^2}\right)\end{aligned}\tag{3.9}$$

where $k = |V_{Qin}|/|V_{In}|$. If $k = 1$, then $\phi_{IQout} = 90^\circ$, regardless of the ϕ_{err} value, meaning that full desensitization is achieved. This is also evident from Fig. 3.22(a) since $V_{Inb} = -V_{In}$, then V_{Iout} and V_{Qout} resemble the result of addition and subtraction of two vectors (with equal magnitude and an arbitrary angle) which are always perpendicular.

The circuit featuring the QPC is shown in Fig. 3.22(b). The amplitude difference between V_{Iout} and V_{Qout} can influence the subsequent phase interpolation however the dividers preceding the PR restore the amplitudes to the same level.

Based on simulations [Fig. 3.22(b)] the QPC operation follows the predictions made by Eqn. 3.8 though the main limitation comes from the output phase sensitivity to the input swings in the dividers as the amplitude difference between V_{Iout} and V_{Qout} can reach 16%. Despite this drawback, the combination is still capable of attenuating the input phase imbalance.

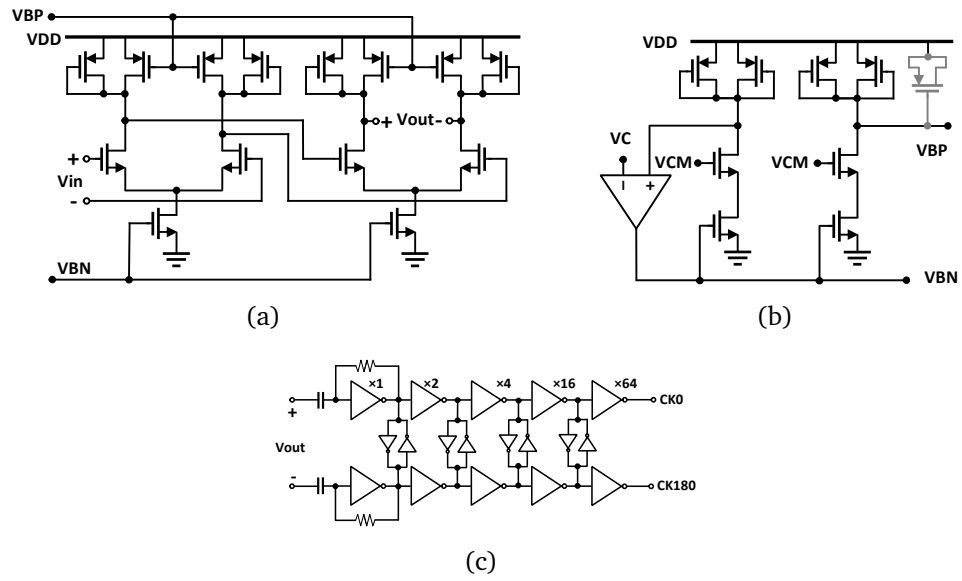


Figure 3.23: (a) de-skew buffers, (b) delay controlling circuit and (c) CML to CMOS converter.

As Eqn. 3.9 suggests, any deviation of k from its ideal value due to the amplitude mismatch between V_{In} and V_{Qin} could result in additional phase errors in ϕ_{IQout} . Validated by simulations, $\pm 5\%$ variations in k offset the ϕ_{IQout} curve by an amount less than $\pm 3^\circ$. In addition, the degradation on the reduced sensitivity of ϕ_{IQout} to ϕ_{err} is negligible with a maximum 1° change in ϕ_{IQout} with ϕ_{err} spanning the range of $\pm 15^\circ$.

The architecture of the QPC indicates that its operation is susceptible to random mismatches. According to Monte Carlo simulations, the standard deviation of ϕ_{IQout} is approximately 4° . Although equipping the QPC with a trimming circuitry could improve the performance, such feature was not considered in this version of the design.

3.2.3 De-skew Buffers and CML to CMOS Converters

To generate rail to rail clocks, CML to CMOS converters have been added to the design, as shown in Fig. 3.23. The CML output DC voltages are removed by the AC coupling capacitors; the CM level is redefined through the feedback resistors and biasing of the first inverters at trip points (self-biased inverters). The following chains of four inverters buffer up the clock signals to gain the required driving strength. Any unequal rise and fall times can shift the clock crossings from the midpoint which can cause DCD. To avoid this DCD, cross coupled inverter pairs are inserted between the two single-ended sides of the differential

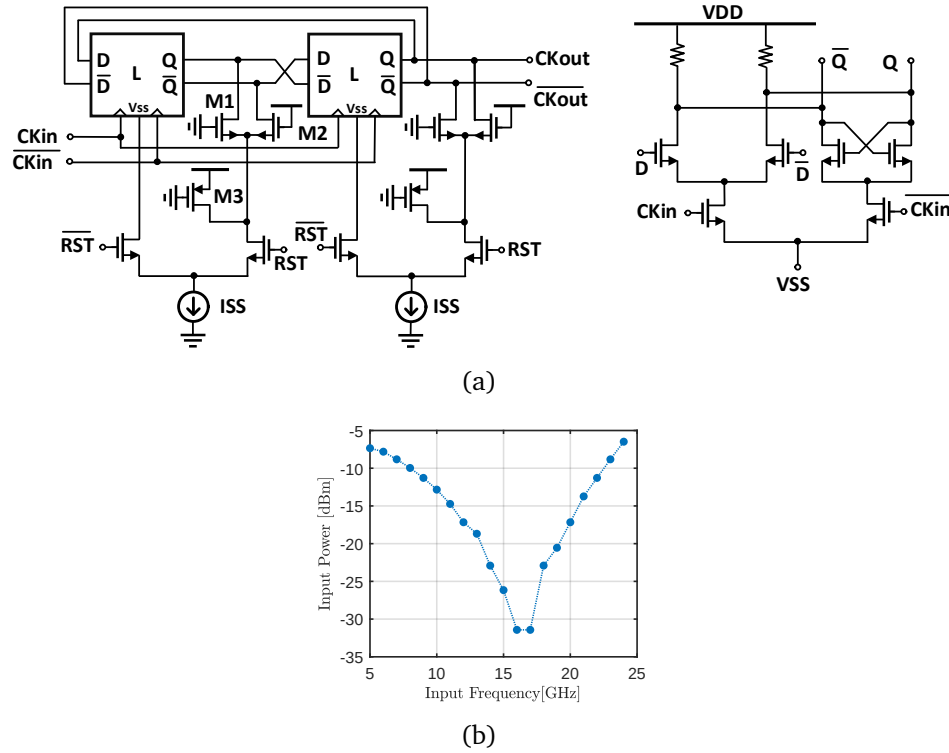


Figure 3.24: (a) frequency divider with synchronous reset and (b) the simulated sensitivity curve.

phases [52]. Altogether the four PR blocks provide eight clock phases with a phase spacing of 45° . Any mismatch can cause phase misalignment at the output. To compensate the skew, buffers are implemented in the form of variable delay lines consisting of two differential stages, hence the independent trimming of the delays in each PR stage can be used to de-skew the relative phase mismatch between the four clock phases.

3.2.4 Dividers

To generate the eight clock phases ($\phi_{0^\circ}, \phi_{45^\circ}, \dots, \phi_{315^\circ}$), differential quadrature inputs with the frequency of $f_{REF} = 2f_{CK}$, are fed to divide-by-two frequency dividers. The frequency divider architecture is based on the static frequency divider in which a single flip-flop, in the form of master-slave CML D latches, is inserted in a negative feedback loop. One of the main requirements for the dividers in this design is to generate a true phase sequence at the output. If the node voltages inside the divider are not defined properly at startup, the divider output can fall out of phase by 180° . Applying a synchronous resetting mechanism guarantees the proper ordering of the output phases. This is accomplished

by using resettable CML latches as shown in Fig. 3.24(a) in which RST initializes the outputs of the master and slave latches with opposite high ($\approx V_{DD}$) and low ($\approx V_{DD} - V_{swing}$) voltage values. Dummy transistor M_1 is added to keep the output nodes balanced. Small sizes for M_1 and M_2 are chosen to avoid extra loading at the output which, with large V_{GS} , can lower the output voltage available for the tail current source I_{SS} during reset operation. For this reason, M_3 is used to source extra current, keeping enough voltage headroom. The simulated sensitivity curve for the dividers is plotted in Fig. 3.24(b).

3.3 Digital Loop Controller (DLC)

The digital loop controller (DLC) consists of DEMUX, bang-bang PDs, majority voting, loop filter and an encoder block. The DEMUX section and related clock distribution network are designed by using the custom analog flow while the remaining blocks are implemented through the digital design flow in which an RTL code is synthesized and mapped to a target technology using standard cell libraries (front end design). In the next step a place and route (PnR) tool is called to generate the final layout of the block using the mapped files. The input to the digital implementation system is a set of design rules and constraints including the frequency of operation, clocks fall and rise time, input-output delay alongside the design and corners (PVT) information. Also, additional data regarding the standard cells timing and physical specifications have to be provided. The ultimate goal is to meet the timing closure which means the design must avoid any setup and hold violations. As our clock speed requirement is high (1.75 GHz), to validate the results of static timing analysis (STA) the most critical timing path was post-layout extracted and simulated separately by the Spectre circuit simulator.

After the successful synthesis, place and routing, in addition to the physical layout, two more files for top-level simulations are generated:

- a) A Verilog HDL code file, describing the gate level information of the synthesized block
- b) A timing file in the form of standard delay format (SDF) containing the actual cell delays (loading effects) in the design plus the interconnects' delay. These two files are annotated back to the analog and mixed signal simulator environment (Spectre AMS Designer) to be used with other analog building blocks. This is the same environment that was used to verify the initial RTL code (Ver-

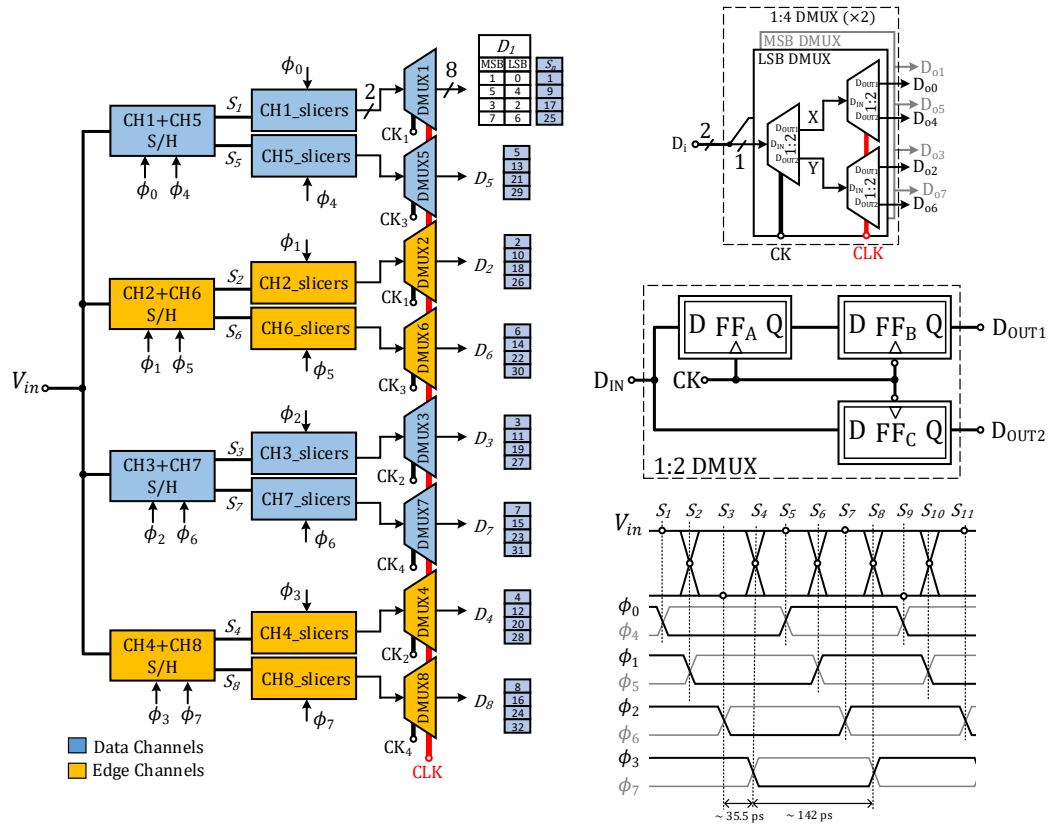


Figure 3.25: Downsampling of AFE's output by DMUX section, the thirty two 2-bit samples (S_n) are aligned to one clock, CLK, at 1.75 GHz. Each DMUX block contains LSB and MSB 1:4 DMUXs. 1:4 DMUXs are built of three 1:2 DMUX cells. Three TSPC flip flops are required per single 1:2 DMUX. The timing diagram shows the sampling sequence of the front end channels.

ilog HDL) i.e. before the physical implementation. In this environment, the AFE and MPCG were modelled by Verilog A and other basic circuit components. For mixed signal simulation an appropriate connect lib was generated to guarantee proper signal conversions between the analog and digital domains.

3.3.1 De-multiplexer (DEMUX)

Each channels slicer's output is a 2-bit 7-Gb/s NRZ signal including the digitized data and edge information as shown in Fig. 3.25. Since the standard-cell-based design with the available library may not be able to operate at such high input speed, the data rate has to be reduced. Using a 1:4 de-multiplexing ratio, the data rate is brought down to 1.75 GS/s. It should be noted that since the slicers are triggered by eight different clock phases with 45° spacing ($= 35.5$ ps) at 7 GHz their respective outputs would also follow the same phase order, hence another critical task is to align all these phases to one phase of the clock, CLK,

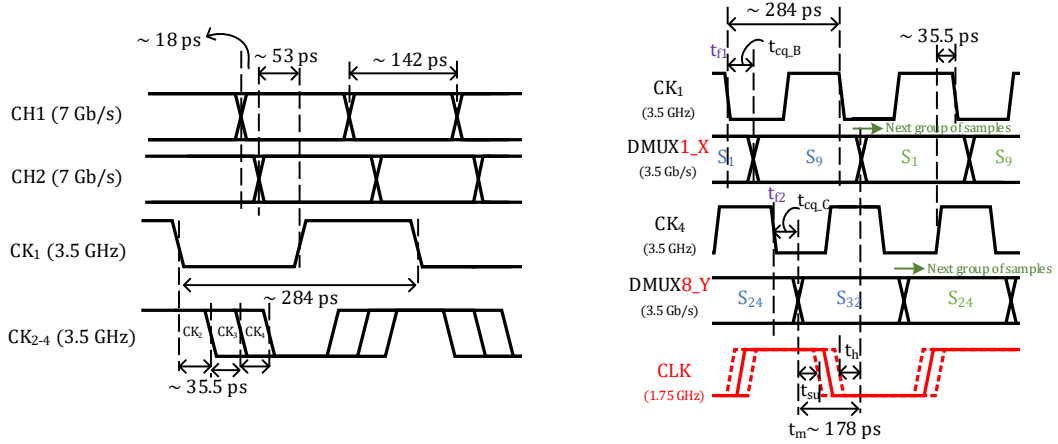


Figure 3.26: the timing diagrams (Left) for the first column of 1:2 DMUXs as in 3.25. The 7 Gb/s data from AFE output is down-sampled by four clock phases at 3.5 GHz. (Right) for the second column of 1:2 DMUXs brings the data rate further down to 1.75 Gb/s and align the data to CLK at 1.75 GHz. To keep the orders of the input to digital section correct, the CLK has to arrive after the data at node X and Y is ready to be sampled by FFB and FFC in DMUX8. Also the arrival of *CLK* has to be before the data change in the same nodes of DMUX1

used by the following digital block. To accomplish this, we perform the first 1:2 de-multiplexing with four clock phases. This means that one of the channel's 2-bit outputs would be sampled at an offset of 18 ps from midpoint, leaving an ample clock phase margin (CPM) of 54 ps, Fig. 3.26. The setup time of the sampling flip flops has to be less than this value. The next column of 1:2 DEMUXs would align these four phases to one clock cycle running at 1.75 GHz.

Since the timing order of the outputs is important for a proper phase detection using 32 consecutive data and edge samples (64 bits), the DEMUX module has to retain the output sequence order w.r.t the digital section input. In other words, DMUX1 and DMUX8 must provide the first and last sampled values in every set of 32 samples, respectively. This is attained by positioning CLK's transitions after one for the first 1:2 DMUX in DMUX8, i.e. CK_4 . Fig. 3.26. Because of the small timing margins, the flip flops (FFs) in the multiplexer section have to provide low delay, setup and hold time to avoid failure due to the PVT variations. For this reason, a true single-phase clock (TSPC) [53] FF was designed, as shown in Fig. 3.27.

The clocks for the DEMUXs can be generated by dividing the required phases from the DPC outputs. The data from the output of the AFE and the clocks from the DPC section would experience different path delays hence their arrival time at respective DEMUX inputs would be skewed considerably, mandating a de-

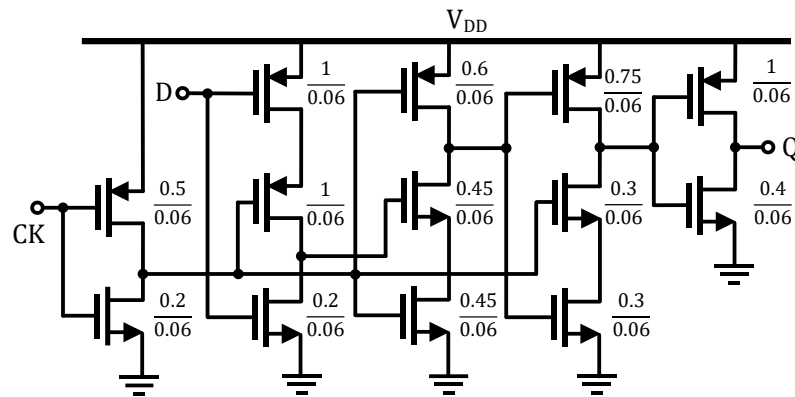


Figure 3.27: The TSPC flip flop's circuit diagrams.

skew mechanism. It should be noted that all the DEMUX blocks have to be properly synchronized with the AFE output to avoid sampling failure. The CDR feedback loop has no control over this part as the main sampling points are within the AFE and the true functionality is only possible when the output data is properly transferred to the digital section. The above observation calls for some means of phase adjusting or delay control to define the sampling phases for the DEMUX section. Although through corner simulations it is possible to match the data and clock path delays against the PVT variations, due to the extensive buffering such an approach may not be reliable and residual timing errors could still cause phase offsets and delay mismatches. Therefore, some means of trimming is necessary. The trimming can be implemented through the use of voltage controlled delay lines (VCDL). However, given the fine tuning, variable and limited delay range of VCDLs, they might not provide an optimum solution over the design corners. In contrast, the requirements can be managed well with a fixed delay range swept by constant and coarse step sizes. This alternative technique is based on using multi-phase clocks spanning the entire clock period realized by frequency divisions and phase inversion.

Since the main clocks are at 7 GHz, after division they would cover half of the clock's phase range as the time spacing is not affected by frequency dividing, to encompass the second half-period an inverting path is added. To equalize the delays between inverting and non-inverting paths, transmission gates are employed. By multiplexing these paths, two clock phase shifter block are built, as shown in Fig. 3.28 and Fig. 3.29. The order of shifting is important for correct edge detection and sequencing of all the DMUX clocks. Addition of the up-counters simplifies the operation and also retains the values for the period of normal operation.

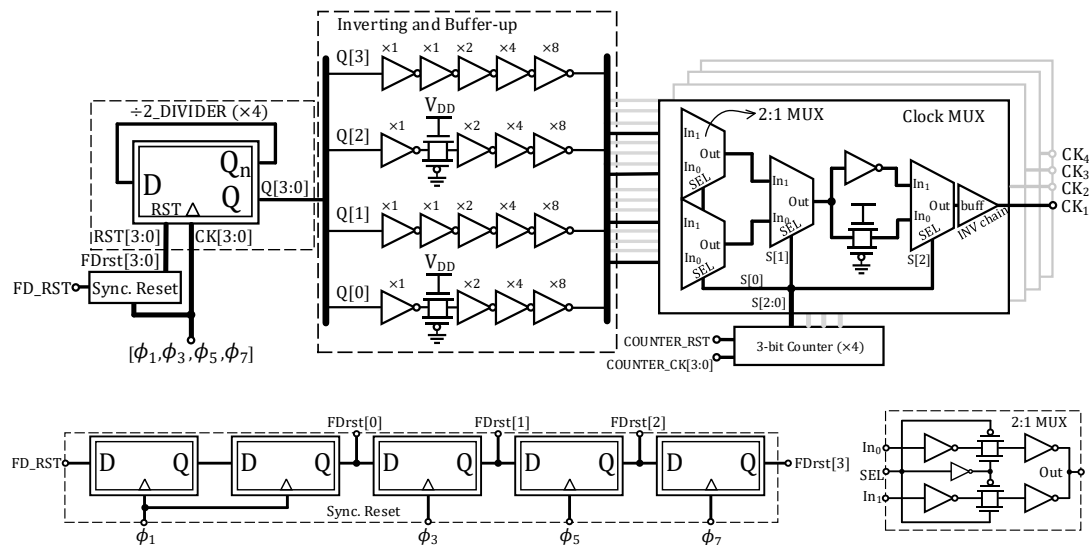


Figure 3.28: The clock divider (outputting 3.5 GHz) and phase shifter used for the first column of DMUXs. Each of the CK_1 to CK_4 can advance by $T_\phi/4$ ($= 35.5$ ps) while covering time span of $2T_\phi$ (≈ 142 ps). The synchronous reset ensures correct phase sequencing for the alignment process.

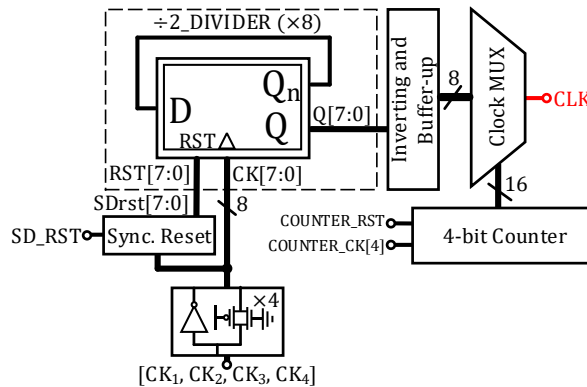


Figure 3.29: The clock dividers (outputting 1.75 GHz) and phase shifter used for aligning the input data and clock of the second column of DEMUXs. CLK is also used by the proceeding digital block. The time steps are $T_\phi/4$ ($= 35.5$ ps) providing complete rotation of $4T_\phi$.

As the four inputs for the clock shifter block are taken directly from the DPC output to evade load unbalancing, dummy inverters have been inserted for unused phases. Using a 7 GHz input, the first dividers output phase can fall out of phase by 180 degrees, which should be avoided; hence a synchronous reset mechanism is applied. The DFF used here are also resettable [Fig. 3.30]. Instead of being placed at the output of the slave latch, the resetting transistors are inserted in the output of master latch to reduce the impact on the DFFs clock-to-output delay, t_{cq} .

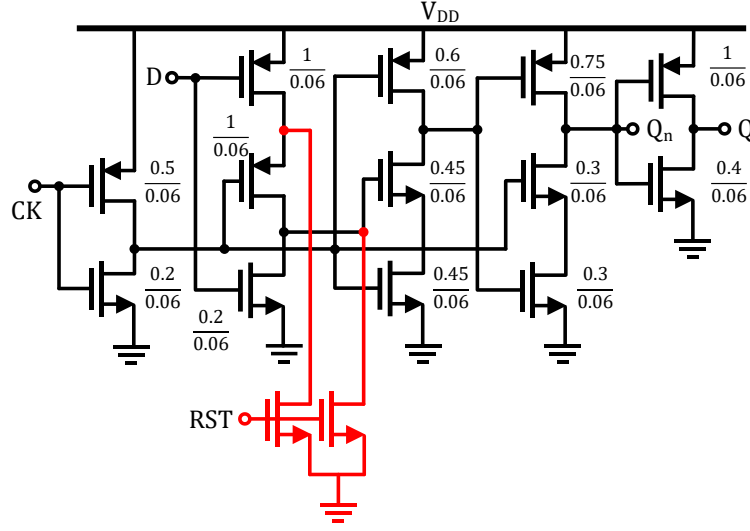


Figure 3.30: Addition of reset transistors to TSPC DFF used as a frequency divider.

To align the AFE data outputs and the sampling clock of the DMUXs, we use the DFFs as simple binary phase detectors⁵. If every DEMUX data input takes a clock-like pattern with the same frequency as the triggering clock then sliding the clock phase creates a horizontal scanning of the DFF input. The moment that the output states change, this indicates that the clock and data are in phase. The procedure would start with the first column of 1:2 de-multiplexers inside 1:4 DMUXs. After alignment of the 3.5 GHz clocks (CK) the 1.75 GHz CLK would be shifted, this has to be done using the DEMUX8 output as it provides the last sampling values in every 32-input set.

The method is illustrated in Fig. 3.31. When the state of DFF output changes, the counter can be clocked by one or two more pulses to ensure near-the-mid-point sampling of D_{in} . The same process is repeated for the second DMUX columns and CLK at 1.75 GHz. However, the input rate has to be halved to 3.5 Gb/s, to match the data rate with the CLK frequency.

The second clock shifter [Fig. 3.29] is almost similar but there is a subtle difference: as the steps still are $T_\phi/4 = 35.5$ ps hence in total 16 steps (4-bit counter) are needed to complete one cycle rotation at 1.75 GHz (≈ 142 ps). Accompanied with their inverted versions at 3.5 GHz, CK_1 to CK_4 cover half of the CLK period, which is extended over the $4T_\phi$ interval by the second frequency division through the following eight dividers.

The DEMUX output is updated every time 32 samples, ($S_n, n = 1, \dots, 32$) have

⁵Prior to the alignment of AFE output and DMUX, proper calibration of the slicers has to be performed.

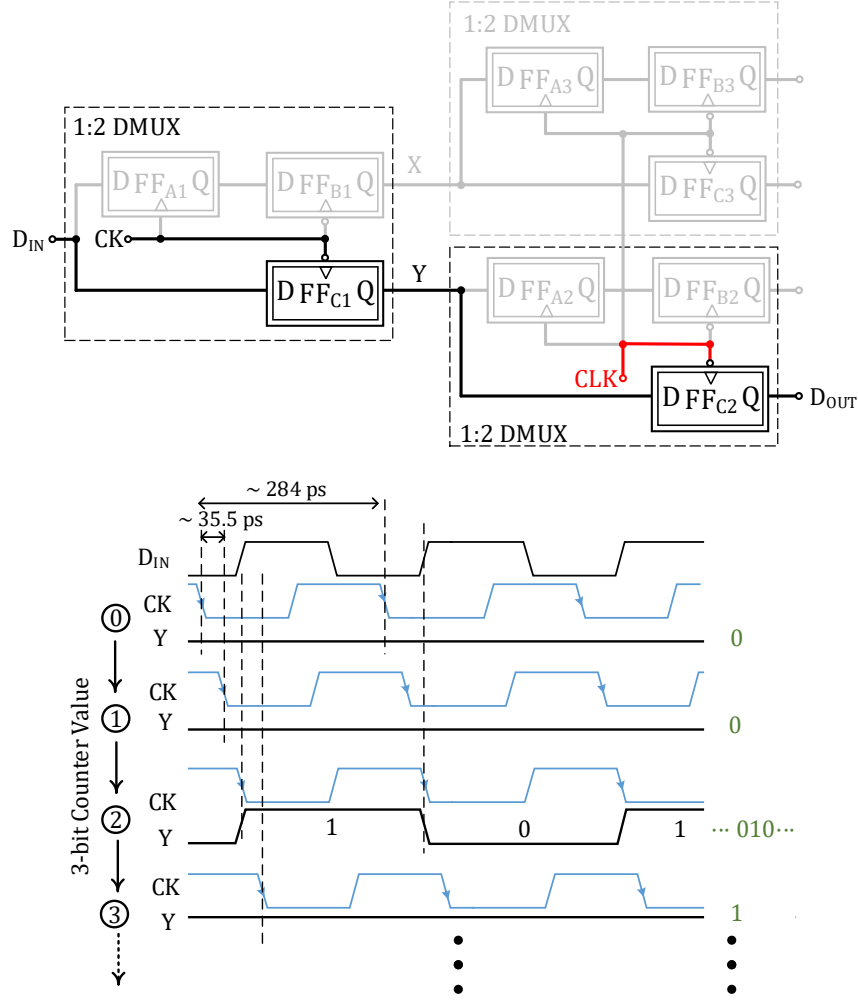


Figure 3.31: The AFE to DMUX alignment procedure, the diagram is shown for the first column of DMUXs, after applying clock-like pattern D_{IN} at 7 Gb/s the 3.5 GHz clock, CK , is horizontally scanning the DMUX input until the output (Y) state is changed from 0 to 1 (here corresponding to 2 at the counter output) which indicates the phase de-skewing is achieved.

been taken. As mentioned, to define the ensembles correctly, the CLK 's falling edge has to be placed after the data transitions in DMUX8's internal nodes of X or Y as shown in Fig. 3.26. The timing window's upper bound is defined by the next data transition in the nodes X and Y of DMUX1. Taking into account t_{cq} of the DFFs driving these nodes i.e. t_{cqB} (t_{cqC}) in DMUX1 (DMUX8), then for the available margin t_m , we can write:

$$t_m = t_{f2} + t_{cqC} - t_{f1} - t_{cqB} \quad (3.10)$$

Assuming that $t_{cqC} = t_{cqB}$ and since $t_{f2} - t_{f1} = 1.25T_\phi$ hence $t_m = 1.25T_\phi \approx 178$ ps. However, the actual sampling window, t_{sw} , is shorter considering the

setup time, t_{su} , and hold time, t_h , of the sampling DFFs in DMUX8, then:

$$t_{sw} = t_m + t_{su} - t_h = 178 \text{ ps} - t_{su} - t_h \quad (3.11)$$

The TSPC dividers have t_{su} and t_h of roughly 30 ps so the CLK could have 118 ps of timing margin. With the time step of 35.5 ps, three steps can cover the required range.

3.3.2 Phase Detectors (PDs), Majority Voting (MV) and Loop Filter (LF)

As discussed in section 2.1.6 the K_P and K_I registers' lengths determine the number of bits required for processing in the design. K_P has to provide some redundant bits for the proportional path gain adjustability and for mitigating limit cycles at least three extra bits have to be allocated⁶. K_I 's length is dictated by the integration path time constant which, to achieve a high damping response, requires four more bits than K_P . We allocate one clock cycle for the PD arrays to output 16 early-late results, the majority voting operation demands 2 clock cycles estimated by early design versions. As the MV output has two bits, to simplify the design, instead of multipliers, MUX blocks can be employed which output K_P (K_I) or 0 or $-K_P$ ($-K_I$) depending on the MV outcome within one clock cycle. By assigning one clock to each of the accumulators the MAC blocks (LF) would need two clock cycles. The LF output passes through an encoder block within the next cycle before being sent to DPC input. In total, to render an output, the digital section demands at least seven clock cycles, therefore having a 7-bit DPC translates to minimum lengths of 10 and 14 bits for K_P and K_I , respectively.

Early design versions with standard cell implementation suggested that the maximum accumulator length that can provide a valid output within one clock cycle is around 16 bits. So to add more redundancy to the design we assign 16 bits of length for all the registers in the loop. After truncation, the encoder section will take the first 7 MSBs to convert it to the required input for the DPC. The complete building block diagrams of the digital section is shown in Fig. 3.32, Fig. 3.33 and Fig. 3.34.

⁶This value is determined by the number of delays in the loop which is already dependent on the number of sequential blocks in the digital section, an initial value can be used and as the design progresses it can be refined by iterations.

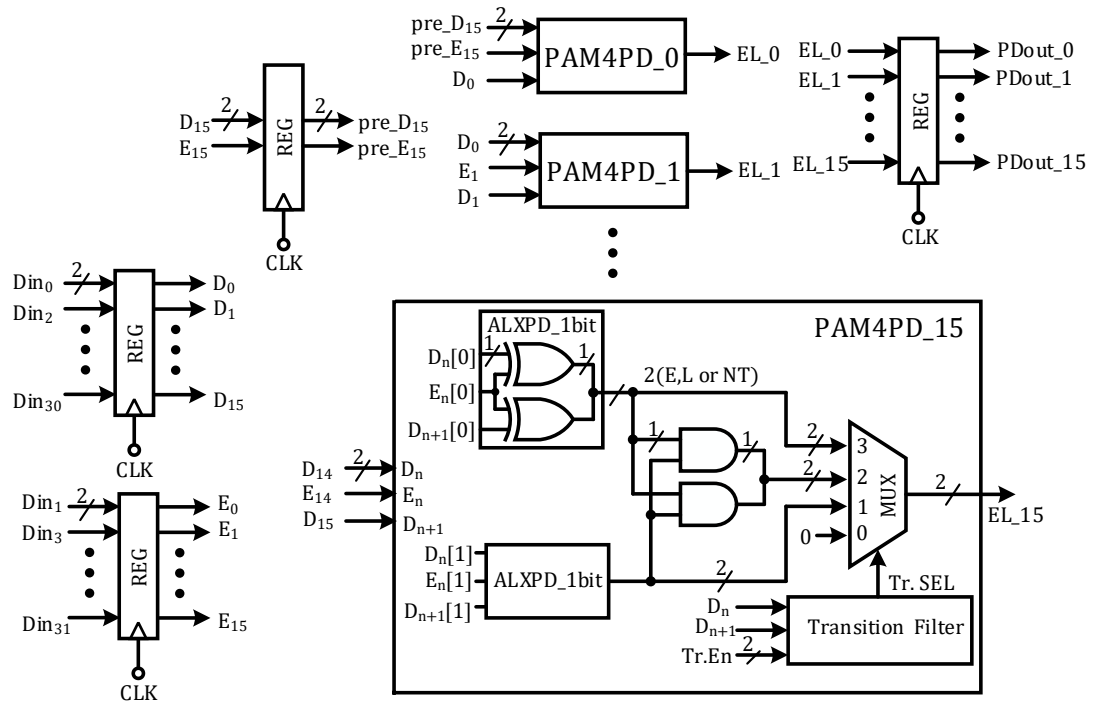


Figure 3.32: block diagram of the PAM4 PD, the 16 parallel PDs performing bang-bang phase detection using 32 samples (64 bits). The sixteen outputs ($PDout_0$ to $PDout_{15}$) will be sent to the MV section. The last data and edge samples (D_{15} and E_{15}) in every group is stored for the phase detection with the next input set i.e. with D_1 . The transition filter is used to enable/disable detection based on middle transitions.

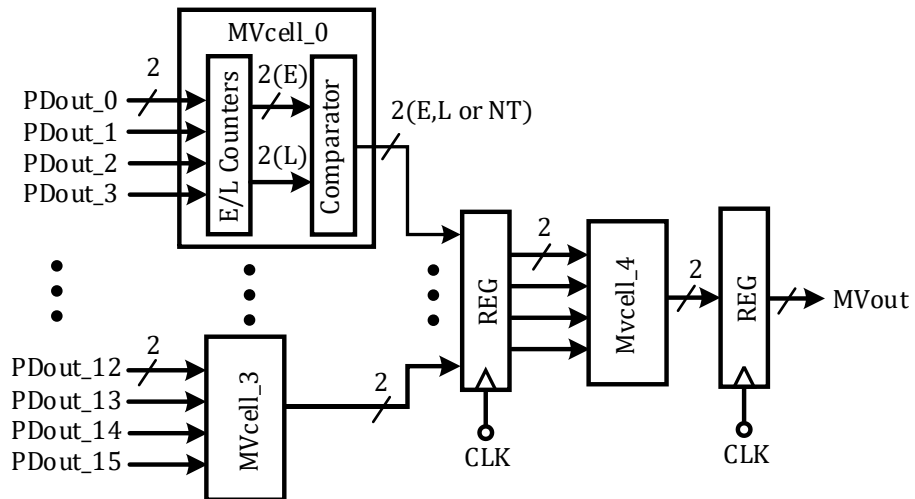


Figure 3.33: block diagram of the majority voting (MV) section, the input is sixteen 2-bit early/late samples produced by the PAM4 PD, the task is completed within two clock cycles.

To account for on chip variations (OCVs) a timing de-rating factor of 5 - 10% is used for the data and clock path during STA analysis. Additionally, 5% of margin is also considered for the clock jitter. The final design has the complexity of

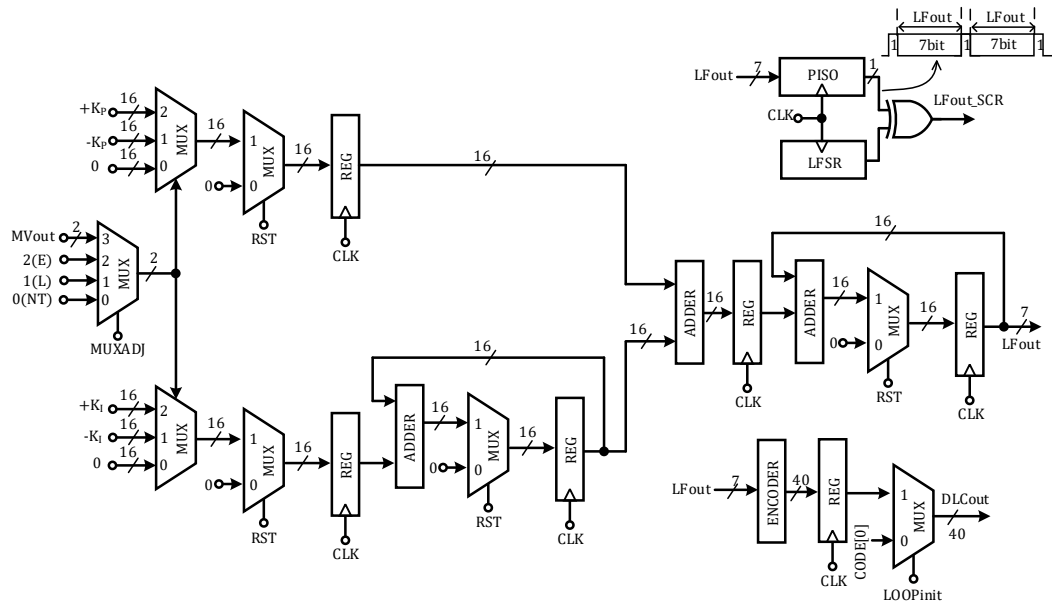


Figure 3.34: The loop filter block diagram including MAC section, Encoder for DPC input and a parallel to serial register with a scrambler as interface circuit for probing during test. The multipliers are implemented using MUX blocks simplifying the gate level complexity. Synchronous reset mechanism is used, the last MUX is used for initializing of the CDR loop, ensuring presence of the clock in system at start up

6000 gates, encompassing an area of $150 \mu\text{m}$ by $150 \mu\text{m}$. The estimated power consumption of the block with 50% flip-flop activity is around 50 mW while operating at 1.75 GHz clock frequency under nominal design scenario.

3.4 Chapter Summary

This chapter presented the core circuitry design for the three main building blocks of the CDR including the AFE, DLC and DPC. The AFE, DPC and part of DLC (DEMUX) are designed through the analog flow while the DLC backend which contains PD, MV, LF and decoders is realized by digital flow.

The AFE employs time interleaving architecture to sample the 28 GBd PAM4 input with the master-slave based sample and hold architecture. The input buffers provide 20 GHz bandwidth while the second buffers have a relaxed bandwidth requirements of 7 GHz. The AFE is also equipped with a new calibration scheme which simultaneously corrects the effect of voltage offset and gain mismatches among the sampling channels.

In the DPC section, the work was focused on improving the linearity of the code to phase characteristic by proposing a modified PI cell and a new QPC circuitry.

To correct for the phase mismatches of the multi-phase outputs the de-skewing block is added to the DPC.

Finally, the implementation of the DLC is explained. In addition, a process-insensitive method to align the AFE output to one clock cycle of the digital clock is demonstrated.

Chapter 4

Experimental Results

This chapter presents the experimental results for the CDR and its building blocks, we begin with the DPC(MPCG) measurements, section 4.1. Because of its critical function, the DPC has been fabricated as a stand-alone chip prior to its integration in CDR. The DPC testing involves the (a) measurement of the phase shifts with respect to the input code to extract the code to phase characteristic. The linearity of this process is examined by extracting the code to phase DNL and INL. The DPC has nominal time resolution of 1.1 ps (while operating on 14 GHz input clock) which demands high sensitivity techniques to be invoked as explained in section 4.1.2. The other DPC performance criteria are the output phase de-skewing and tolerating the input phase I/Q imbalance which are covered in section 4.1.3.

Following the DPC we present the silicon interposer design and validation. Since the packaging of CDR proved to be difficult, due to the high number of I/O pads, a custom packaging method was employed in which a silicon interposer was designed and fabricated in 1.2 μm CMOS. This part is covered in 4.2.

section 4.3, covers the CDR's lab validation and measurement results. For the CDR our ultimate goal is to measure the JTOL as this is the most important parameter for the CDRs used in short reach optical transceivers. However due to its complexity, first each individual block will be tested in open loop mode before closing the feedback loop around the clock and checking the phase recovery as explained in section 4.3.3. After these steps we will perform BER bathtub test followed by JTOL measurement.

4.1 Testing of the DPC (MPCG)

4.1.1 PCB Design Considerations and Test-bench

The DPC has been fabricated in 65nm bulk CMOS process, Fig. 4.1. The active area for the DPC section is 0.062 mm^2 and the chip is mounted directly on a printed circuit board (PCB) using die-on-board wire-bonding. The bonding diagram is illustrated in Fig. 4.1. For the chip to PCB attachment, a non-conductive adhesive is applied thus avoiding the possibility of short circuits between VDD VIAs and GND plain inside the PCB's thermal pad area. A non-transparent glop-top epoxy encapsulates the chip to avoid any mechanical stress during transport and assembly to lab instrumentations. Due to the high number of the pads (89 pads) and the short pad spacing on the chip side ($6 \mu\text{m}$ edge to edge), the packaging process mandated a fine pitch and high-quality finish PCB material in order to shorten the wirebonds' length hence decreasing the high frequency losses. The PCB was fabricated using Thin Flex (A-2005RD) as the insulator material with $75 \mu\text{m}$ dielectric thickness. To reduce the length of the input high speed lines, the chip is placed close to the edge of the PCB. Efforts have been made to keep the input paths symmetrical hence avoiding any mismatches between I/Q phases. The final PCB floorplan is decided based on allowing enough room for the other connections as shown in Fig. 4.2. EM simulations were performed to optimize the width and spacing of the traces. The width of the single ended and differential microstrip lines are $110 \mu\text{m}$ and $110 \mu\text{m}$, respectively, achieving $50 \Omega/100 \Omega$ characteristic impedance and, where necessary, the lines were tapered to minimize the impedance discontinuity effects.

The main PCB includes the DUT, decoupling capacitors for the power supply, reference voltages and resistive dividers which are used as level shifters for the digital controlling signals. Edge mounted GPPO connectors with semi-rigid adapters are used to connect the board to high speed signal generators and instrumentation setups.

The test setup is shown in Fig. 4.2. The input clock is generated using SHF's 78120B clock synthesizer. The IQ signal is generated by applying the clock to the quadrature hybrid which is followed by the delay lines (DLs) to output differential signals. The DLs are used instead of BALUNs to compensate any possible phase mismatch while the first two DLs are added to test the I/Q phase mismatch tolerance of the circuit. For the time and frequency domain measurements Keysight's 86100A digital sampling scope and 8565EC spectrum

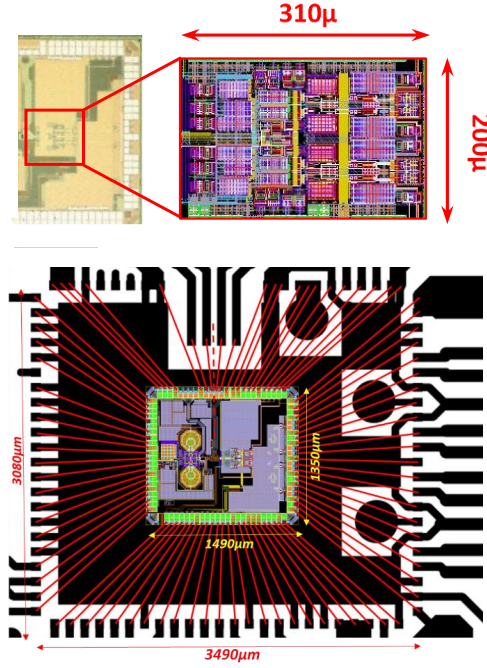


Figure 4.1: micrograph of the DPC chip and its bonding diagram (to PCB pads)

analyzer are utilized respectively. Because of the high number of biases and reference signals and to reduce the clutter on the main board, a separate PCB has been designed which produces the required voltages from a single power supply. Jumper connectors for the digital traces also mounted on the intermediate PCB to isolate the main PCB from any possible mechanical stress during setup preparations. The controlling signals are generated using a μ C unit.

4.1.2 Phase Shift, DNL and INL Measurements

Fig. 4.3 illustrates the output phase range when the codes are shifted from 16 to 32. To measure the small time steps with high sensitivity a frequency domain method based on phase modulation of the clock edges with a periodic signal is used [54]. The resulting spectrum has spurs near the main carrier i.e. the clock frequency, whose relative power, SCR [in dB_C], is proportional to the amount of delay t_d added to the clock, Fig. 4.4. The relation between t_d and SCR can be described as:

$$t_d = \frac{T_{CK}}{2} 10^{SCR/20} \quad (4.1)$$

The SCR is measured as the control signal is pulsed between $\text{CODE}[n]$ and $\text{CODE}[n+1]$ then the code is incremented to $\text{CODE}[n+1]$ and is pulsed between $\text{CODE}[n+1]$ and $\text{CODE}[n+2]$. The task is repeated for 128 consecutive codes.

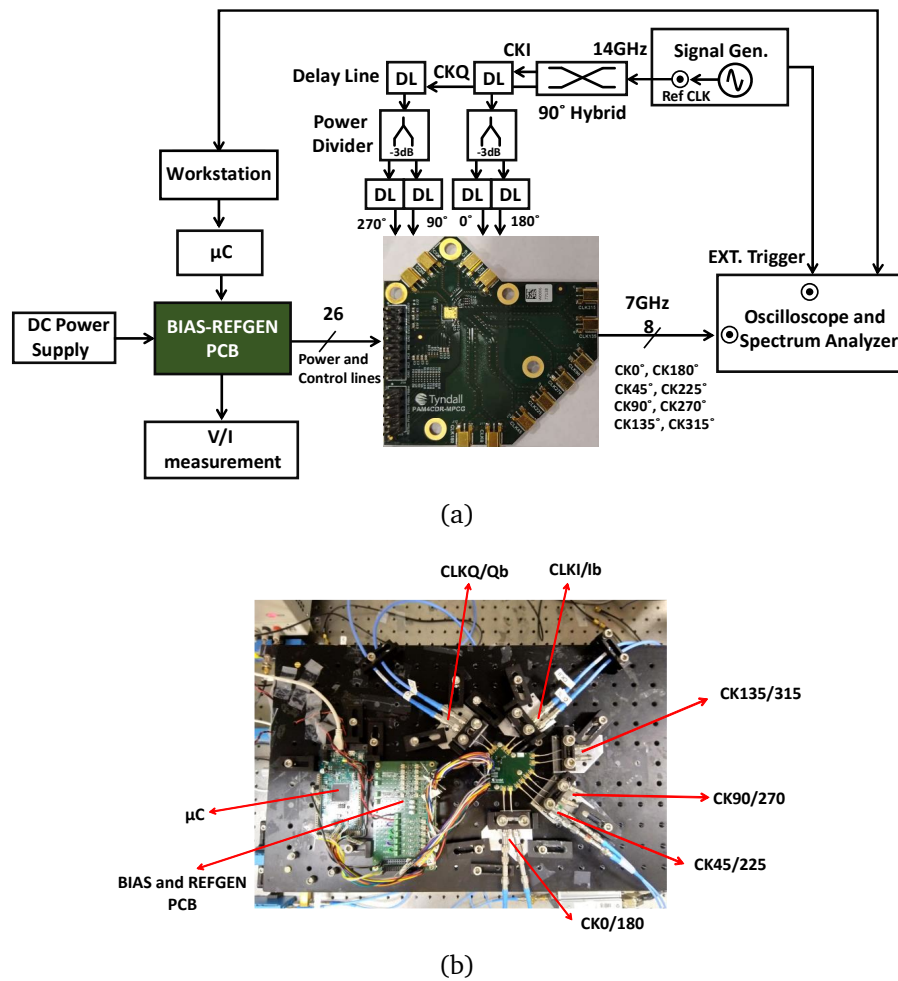


Figure 4.2: (a) block diagram and (b) the view of the measurement setup

Before employing it in the main set-up, a simple test bench was prepared to verify the method, Fig. 4.5. The clock synthesizer's external jitter option is used to modulate the clock edges by using an Arbitrary Waveform Generator (AWG). Then an equivalent time digital sampling scope is used to measure the time steps and cross check the results with the spectrum analyzer's output. It was observed that multiple readings (sweeps) result in 0.5 dB difference in recording spur/side-band power which introduces around 100 fs error. This is well below the accuracy threshold for the DNL measurement, however as INL computation is based on the cumulative sum of DNL samples, then the resulting errors can be perceptible, leading to systematic gain error in the DPC's code to phase transfer. Although averaging of multiple sweeps can reduce this error, there will still be some residual error. Another source of systematic error is the duty cycle distortion (DCD) of the pulsing code which, if strong, will manifest itself in the clock spectrum by producing side-bands in even indices of

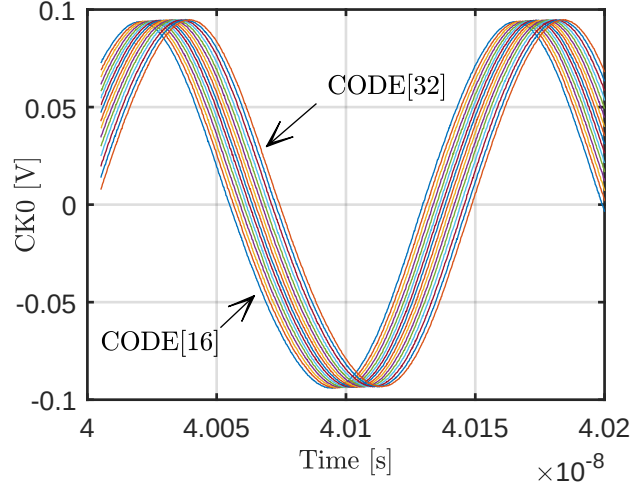


Figure 4.3: Measured CK0 output (taken from the high speed CML PAD drivers) as the code shifted from 16 to 32 covering one octant.

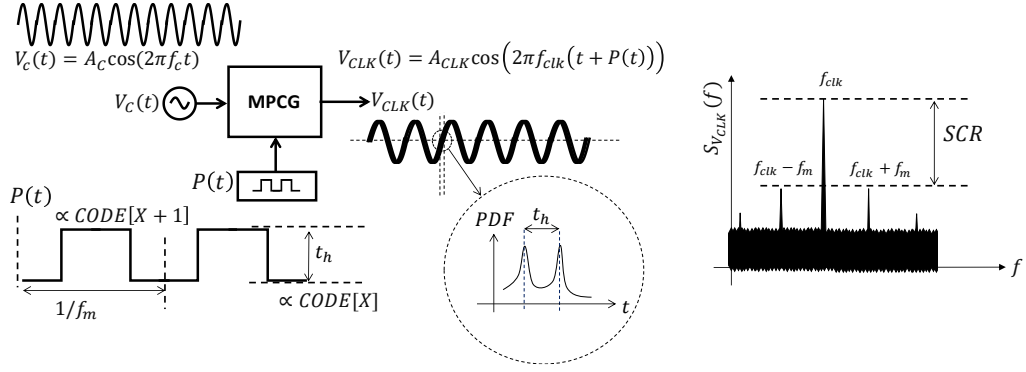


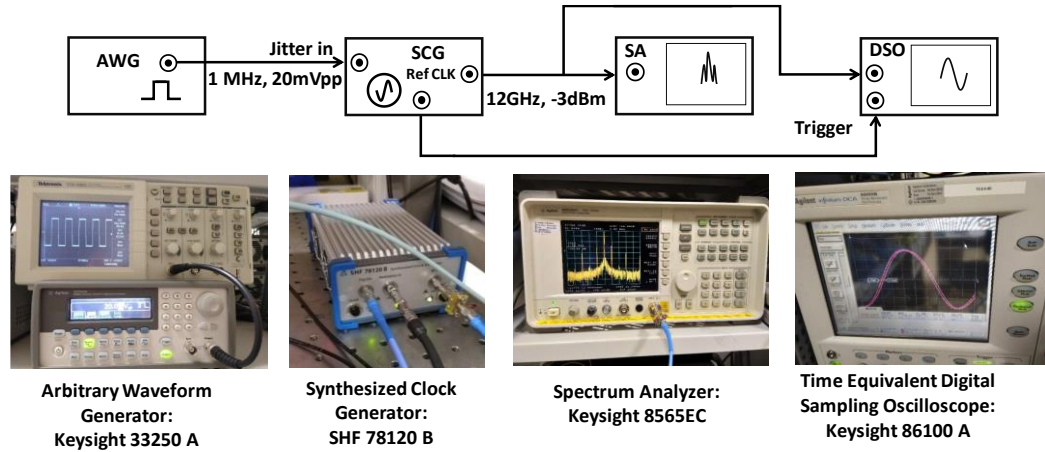
Figure 4.4: Time step measurements in frequency domain using phase modulation technique, here DPC (MPCG) operates like a phase modulator.

the modulating frequency. If the modulating square signal has a duty cycle of d , one can derive the following:

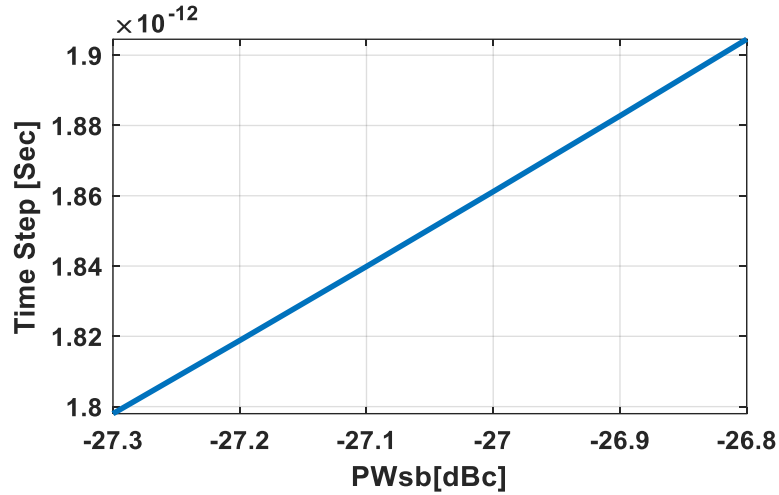
$$t_d = \frac{\sin(\pi d) T_{CK}}{2} 10^{SCR/20} \quad (4.2)$$

which indicates that, for example, a duty cycle of 45%, if ignored, can introduce approximately 2% of error in every step. The impact of the duty cycle distortion can be incorporated into the calculations to increase the accuracy as follows. In Eqn. 4.2, d is found by comparing the third and the first side-bands i.e. $(Psb_3 - Psb_1)$ as in Fourier series expansion:

$$\frac{\sin(\pi d)}{3 \sin(\pi d)} = 10^{(Psb_3 - Psb_1)/20} \quad (4.3)$$



(a)



(b)

Figure 4.5: (a) Validation of the time step measurement technique, in this example the modulating signal's amplitude (AWG output) is set to be 20 mVpp at 1 MHz and the carrier (SGC) frequency is 12 GHz, DSO (equivalent-time sampling scope) recording is 1.88 ps.(b) Multiple readings from SA varies within 0.5 dB range resulting in 100 fs deviations.

with some modifications:

$$d = \frac{1}{\pi} \arccos\left(\frac{\sqrt{1 - 3 \times 10^{(P_{sb3} - P_{sb1})/20}}}{2}\right), \quad \frac{1}{3} < d < \frac{1}{2} \quad (4.4)$$

Now, to evade the effect of vestigial errors in INL calculation, we consider that the DPC's code to phase transfer incurs no gain error after shifting by 128 codes as it outputs the same phase i.e., the outputs for CODE[0] and CODE[128] are exactly one clock period apart. This is valid as long as the overall measurement time is kept short to avoid errors associated with low frequency phase drifts of

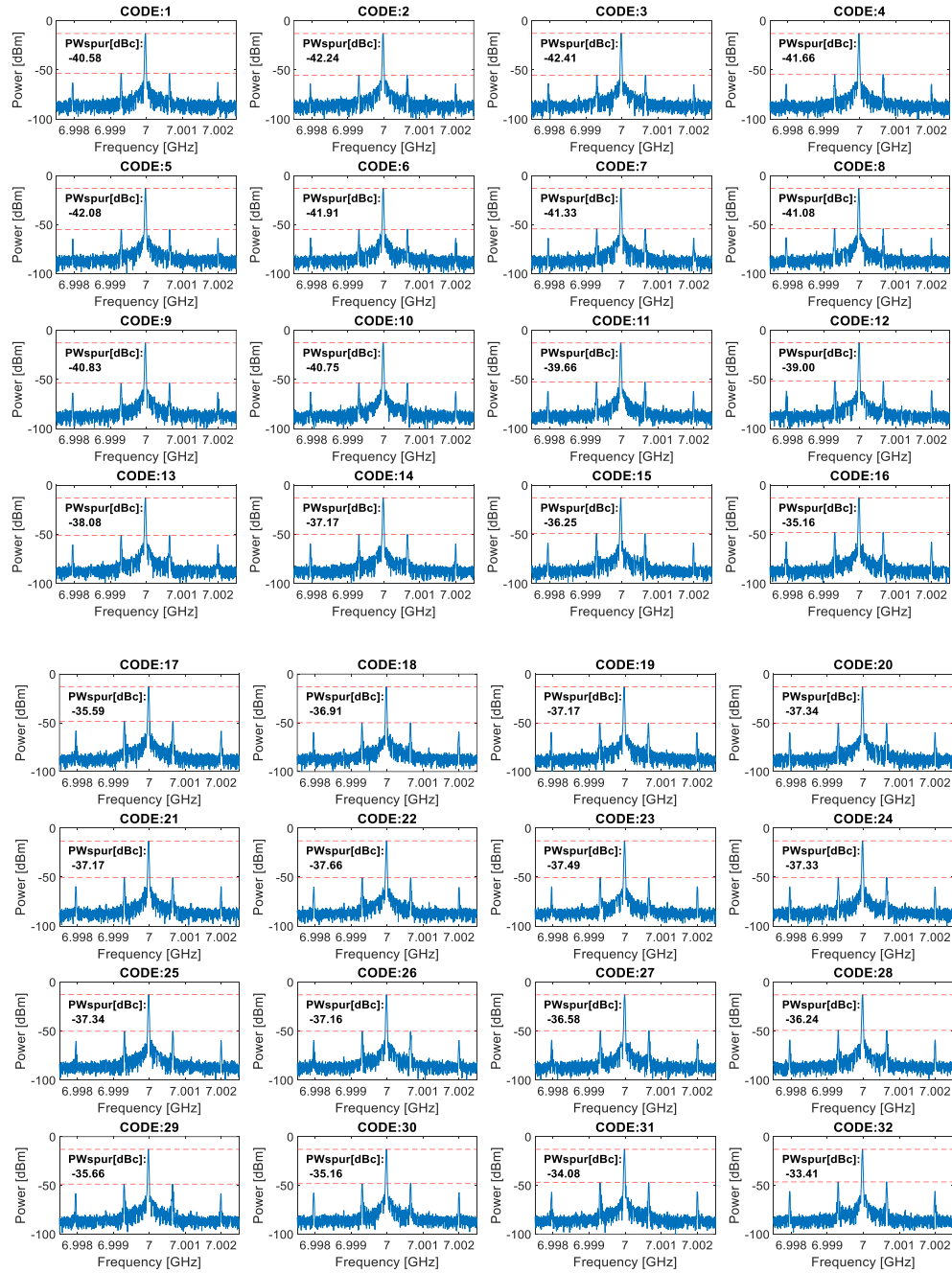


Figure 4.6: Spectrum of the output clock [CK0] for code[1] to code[32] covering the first quarter of the clock phase at 7 GHz, SA settings: RBW and Span are 10 kHz and 5 MHz, respectively.

the input reference clock¹. In addition, the introduced errors are independent of the input codes; hence the average error can be extracted from the measured time steps for the sequence of 128 + 1 consecutive codes. By using this method,

¹This value depends on the equipment type, as an approximation, a total phase drift of less than 0.1 LSB during measurement is sufficient.

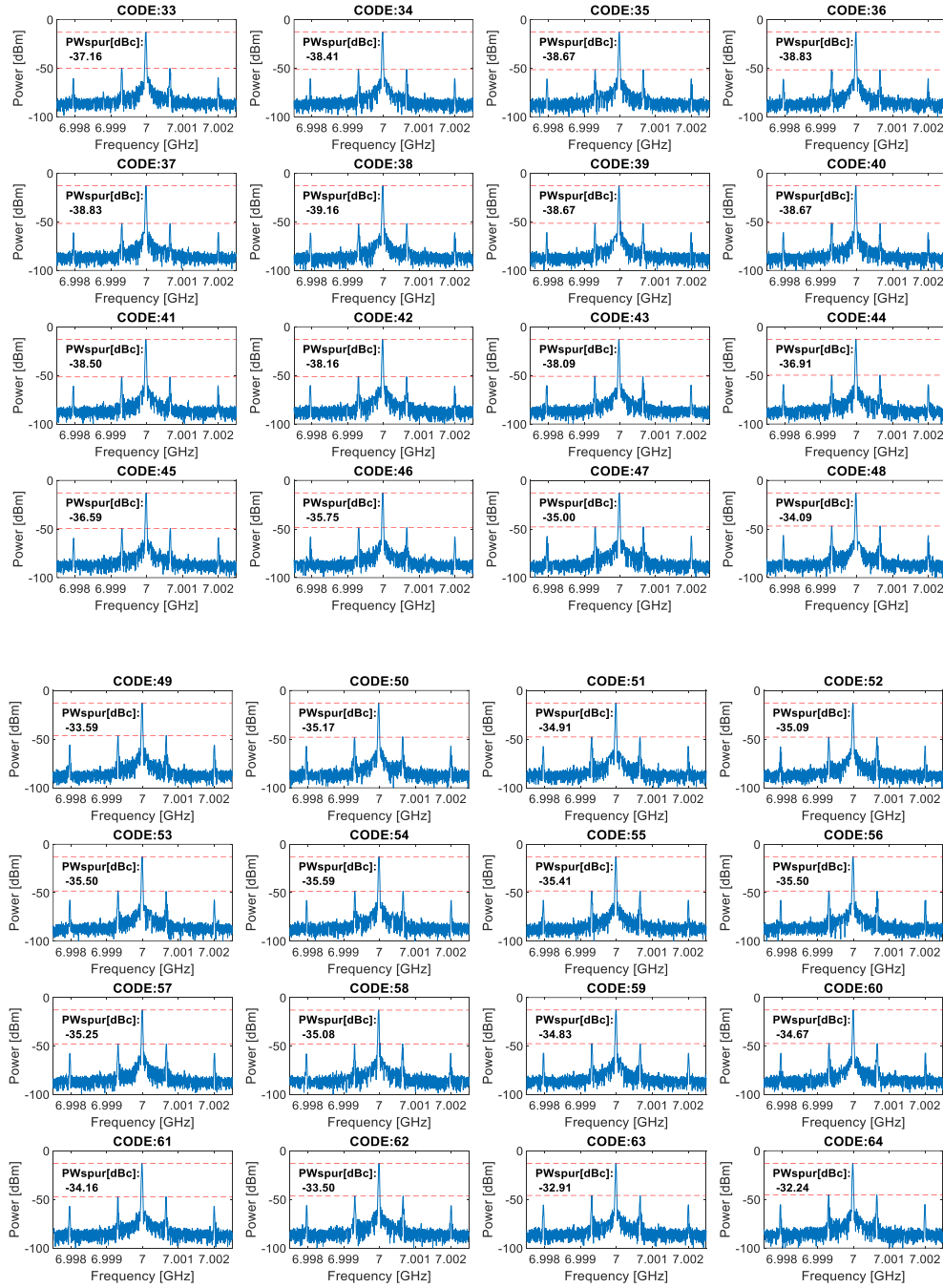


Figure 4.7: Spectrum of the output clock [CK0] for code[33] to code[64] covering the first quarter of the clock phase at 7 GHz, SA settings: RBW and Span are 10 kHz and 5 MHz, respectively.

the induced gain error is removed and the INL can be calculated using:

$$\text{INL}[n] = \sum_{n=1}^{128} (\text{DNL}[n] - \overline{\text{DNL}}) \quad (4.5)$$

wherein $\overline{\text{DNL}}$ is the mean of DNL profile over 129 codes. It is worth mention-

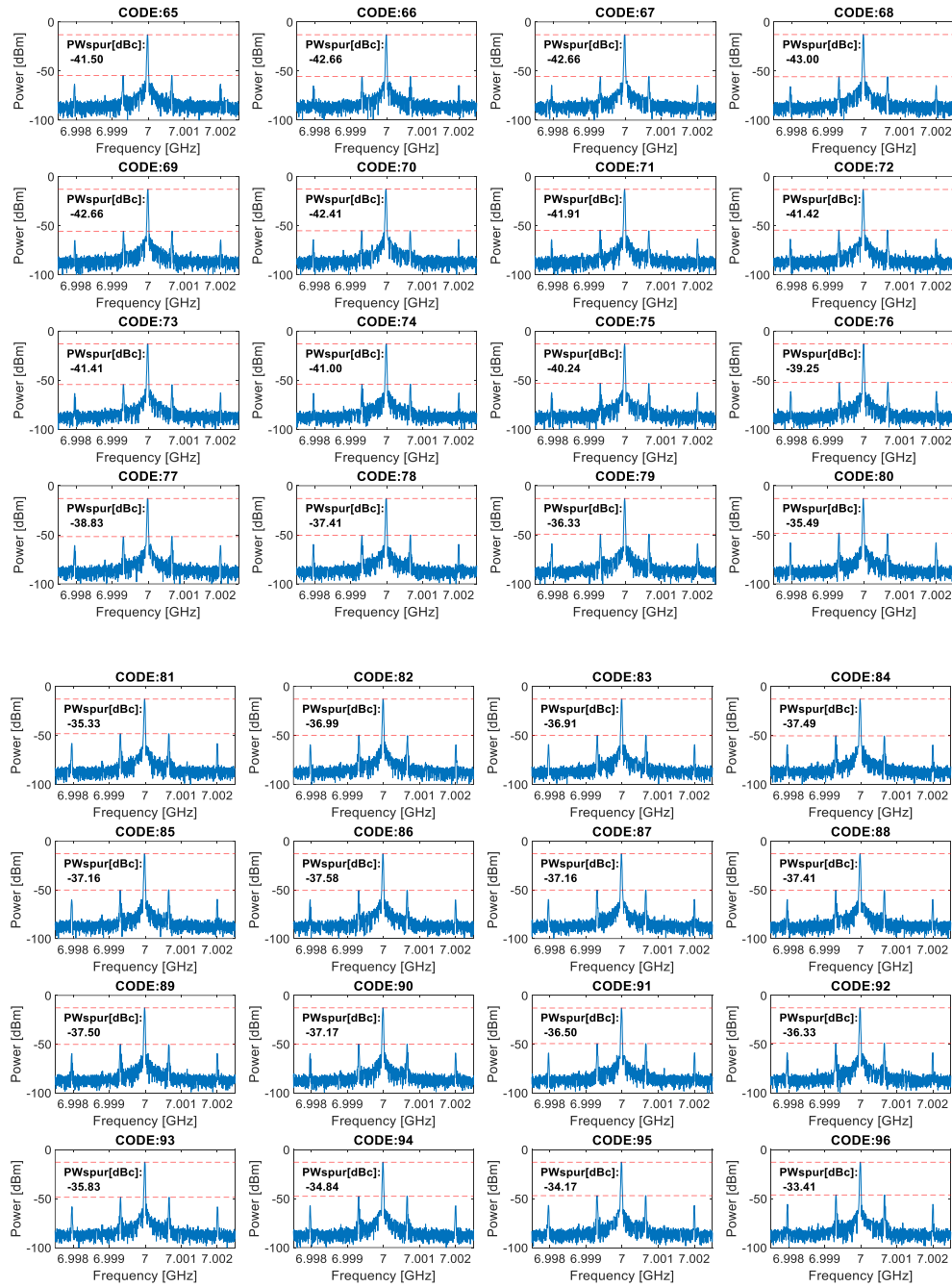


Figure 4.8: Spectrum of the output clock [CK0] for code[65] to code[96] covering the first quarter of the clock phase at 7 GHz, SA settings: RBW and Span are 10 kHz and 5 MHz, respectively.

ing that the choice of modulating frequency is bounded by the minimum offset from the center frequency to distinguish spurs from the clock's phase noise whereas the maximum frequency is limited by the bandwidth of the digital interfaces. Based on this, the pulsing frequency of the controlling code sequence is set between 650 – 700 kHz. To improve the readings sensitivity, the spectrum

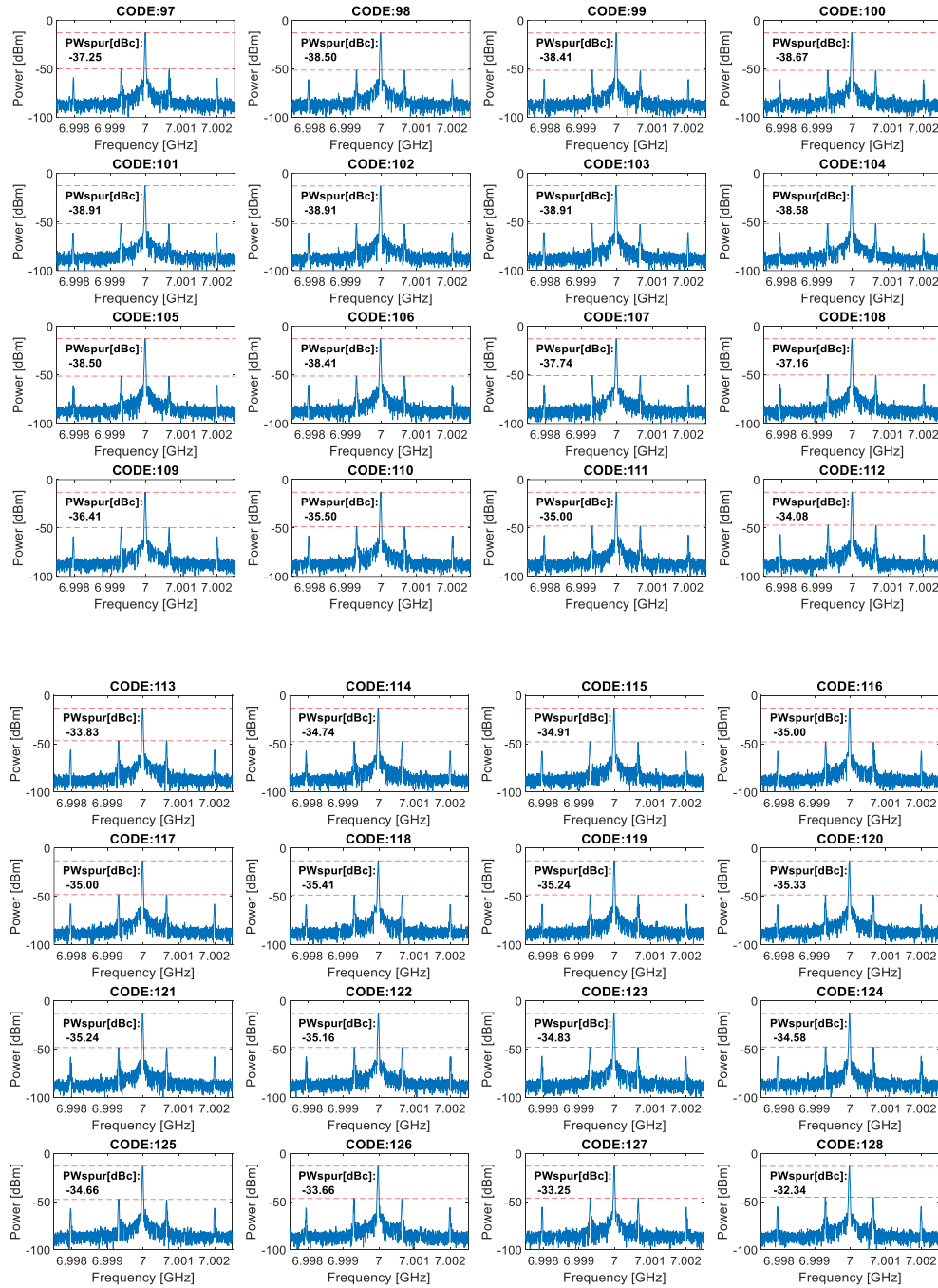


Figure 4.9: Spectrum of the output clock [CK0] for code[97] to code[128] covering the first quarter of the clock phase at 7 GHz, SA settings: RBW and Span are 10 kHz and 5 MHz, respectively.

analyzer's resolution bandwidth (RBW) is adjusted to 10 KHz , which shifts the noise floor well below the spur power level. The spectrum of the modulated clock in every code step in each of the four quadrants is shown in Fig. 4.6, Fig. 4.7, Fig. 4.8 and Fig. 4.9.

The normalized DNL and INL are plotted in Fig. 4.10 for different input fre-

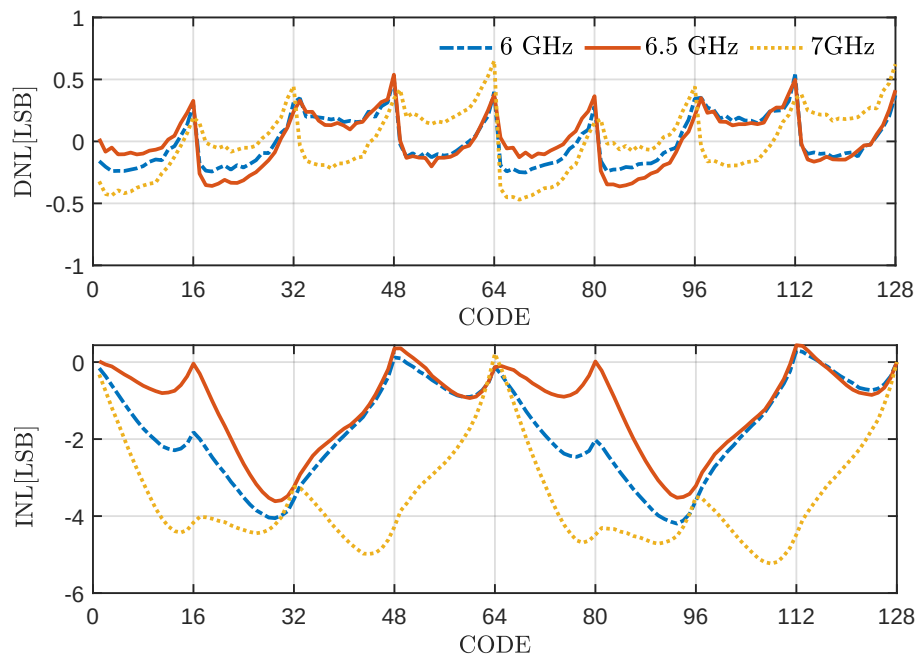


Figure 4.10: Measured DNL and INL profiles for CK0 at different output frequencies. (intentional IQ mismatch is added at the input to correct for the phase imbalance from other sources such as: cables, PCB traces, connectors and etc.)

quencies, indicating a wide frequency range of operation. INL and DNL profiles for the four output clock phases at design frequency of 7 GHz (14 GHz input clock) are illustrated in Fig. 4.11. In all the measurements the output of code 0 is considered to be the reference phase. Comparing the results with the prediction made by the simulation (see chapter 3, Fig. 3.21) reveals that the input to the PR core suffers from phase mismatches due to the residual I/Q imbalances and duty cycle distortion introduced by the preceding blocks, especially the dividers.

4.1.3 QPC and De-Skew Buffers Validation

With no direct access to the output of the QPC block, an indirect approach is employed to measure the I/Q phase mismatch tolerance. The testing is based on the amount of change in the output phase shift with respect to the deliberate phase imbalance at the input while the code is swept one octant, for instance, from CODE[0] to CODE[16] and it is equivalent to the vertical shift in the INL of CODE[16]. The results are shown in Fig. 4.12 for ± 10 ps time mismatch around the nominal I/Q value. The phase change is 6.4 ps, corresponding to 3 : 1 attenuation.

The de-skew buffers can provide delay ranges of 40 ps at the frequency of 7 GHz

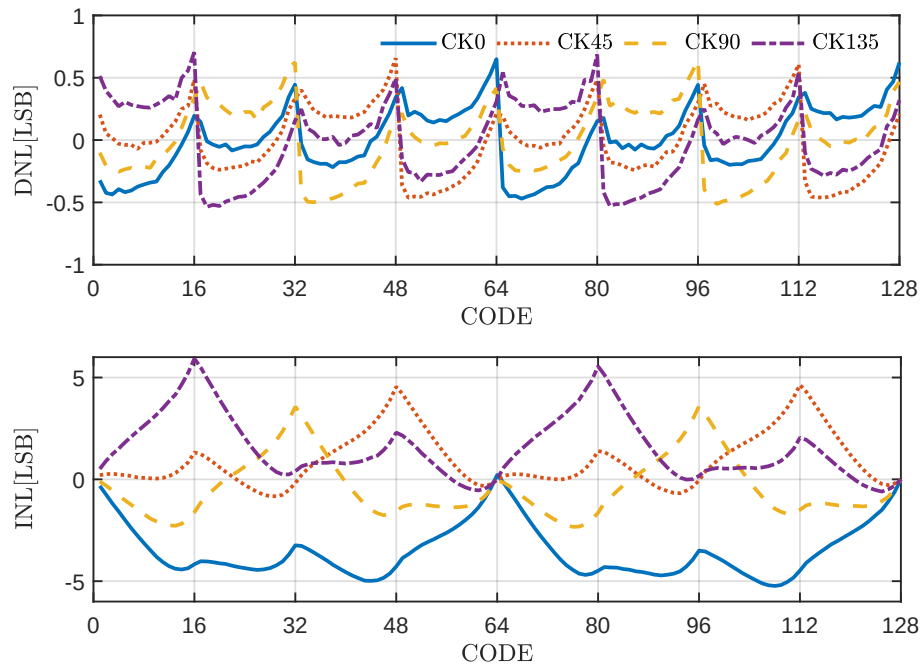


Figure 4.11: measured INL and DNL for the output phases at targeted design frequency (7GHz)

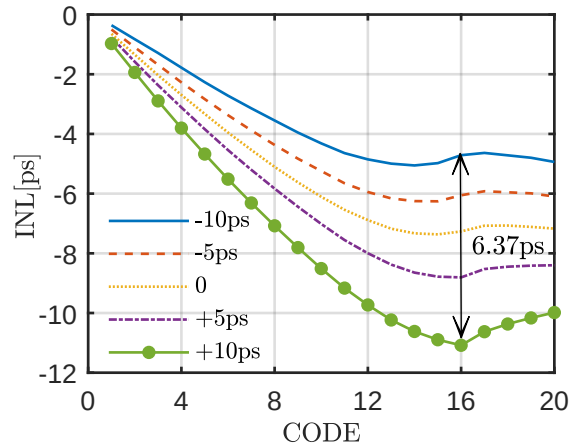


Figure 4.12: The performance of QPC is tested by addition of intentional mismatches at the input while looking at the INL shifts at CODE=16

as the controlling voltage, V_C , varies from 0.3 V to 0.7 V (see Fig. 4.13) The amount of integrated RMS jitter at the input and output of the circuit is 200 fs and 600 fs, respectively. With the output jitter demonstrating Gaussian distribution, the jitter contribution of the block is around 565 fs. Using a spectrum analyzer the dividers output self-oscillation frequency was measured to be approximately 6 GHz.

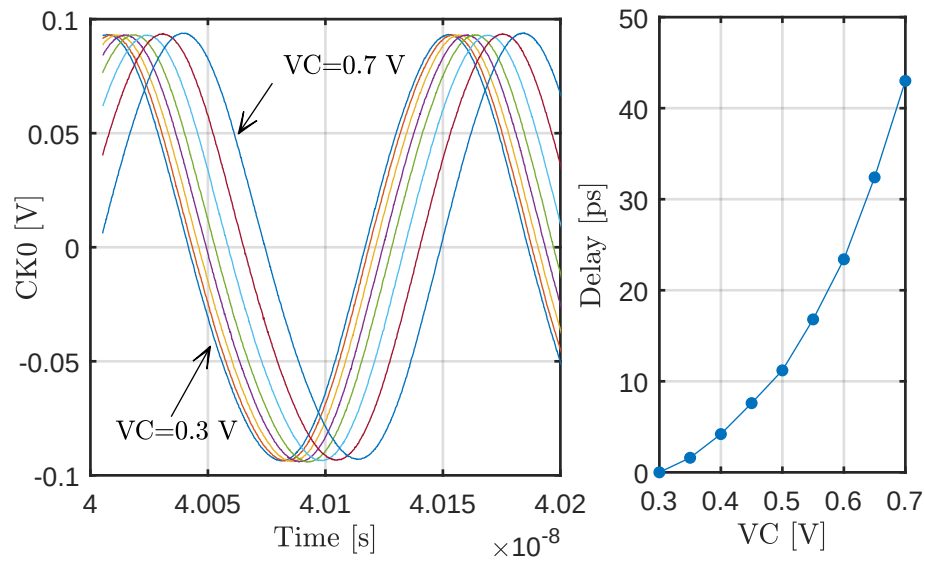


Figure 4.13: adjusting the phase of CK0 using controlling voltage VC, the resulted delay shows the wide de-skewing range of output buffers.

Table 4.1: DPC's Performance Summary and Comparison with Prior Art

	This work	[55]	[56]	[57]	[58]	[59]	[60]
Technology	65 nm	28 nm	65 nm	28 nm	65 nm	65 nm	28 nm FDSOI
Supply	1.05 V	1.1 V	1.2 V	1 V	1.2 V	1.2 V	1.2 V
Frequency	6-7 GHz	2 GHz	0.5-1.5 GHz	0.3 GHz	10 GHz	5-8 GHz	2-11 GHz
Resolution	7 bits	11 bits	8 bits	10 bits	7 bits	7 bits	7 bits
DNL	0.7 LSB	1.25 LSB	0.52 LSB	-	0.3 LSB*	0.77 LSB	0.5 LSB
INL	6 LSB	4.9 LSB	1.33 LSB	1.86 LSB	3 LSB*	1.76 LSB	1.1 LSB
Multi-phase output (#)**	Yes(8)	No	No	No	Yes(4)	Yes(2)	Yes(8)
Output phase de-skew	✓	×	×	×	×	×	×
Power consumption	40.5 mW	19.8 mW	4.3 mW	11.06 mW	N/A mW	22.95mW	< 33.6 mW
Active area	0.062 mm ²	0.009 mm ²	0.06 mm ²	0.047 mm ²	N/A	0.0426 mm ²	0.028 mm ²

*Only simulation results are provided for the phase rotator section.

** power consumption is directly proportional to the number of output phases.

4.1.4 Power Consumption and Performance Summary

At 14 GHz input frequency, the DPC consumes 161 mW power of which 81 mW is drawn by the main core and the rest by the output drivers from 1.05 V and 1.2 V voltage supplies respectively. The CML to CMOS converter contributes 50% to the core power consumption since this circuitry is not part of the main DPC's function, the actual DPC block power dissipation is around 40.5 mW. Table 4.1 summarizes the performance of the DPC and compares it with that of prior art. The power consumption is higher in comparison with [55],[56] and [57] mainly due to the operating frequency and the number of the output phases. In terms of linearity, although the DPC's may not demonstrate favorable INL, the achieved DNL is within the acceptable range.[58], [59] and [60] feature higher clock frequencies, while the last one benefits from more advanced CMOS technology the first two provide fewer number of outputs. Furthermore, the

proposed DPC, offers timing de-skew, allowing relative adjustment of the output phases.

4.2 Silicon Interposer for CDR Packaging

4.2.1 Design Considerations

The CDR chip in total has 146 pins with a staggered PAD orientation. To facilitate the required fan out, a custom- packaging scheme was needed. A silicon interposer was designed to provide intermediate connectivity by matching the PAD pitches to those of the PCB side. The interposer was fabricated using in-house fabrication facility of Tyndall in $1.2\ \mu\text{m}$ CMOS technology. Since at the time of fabrication no TSV (Through Silicon Via) option was available, a full flip chip approach was chosen for both the chip-to-interposer and interposer-to-PCB connections. Because of some technical issues, the first option, as explained later, was not successful. Placing the chip in a cavity faced limitations imposed by PCB manufacturing hence after redoing the PCB, we proceeded with the direct wire-bonding of the interposer to PCB as shown in Fig. 4.14 and Fig. 4.16.

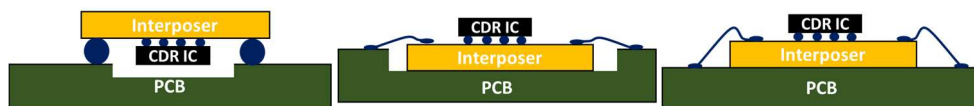


Figure 4.14: The scenarios considered for the packaging of the CDR IC using silicon interposer without TSV option , from left to right: fully flip-chip eliminating bond-wires parasitic, flip chip CDR IC and wire-bonded interposer inside cavity shortening the length of wire bonds, flip chip CDR IC and wire-bonded interposer with no cavity on PCB. The third option is used.

To investigate the signal integrity impairment caused by the interposer's insertion loss, multiple EM (Electromagnetic) simulations were performed during the design phase. Unfortunately, due to the lack of a proper PDK (process design kit), the EM simulations were carried out through an estimated process stack-up which was developed based on the information provided by Tyndall's silicon fab, Fig.4.15. All the values are DC therefore the frequency dependency of the parameters was not modeled and tracked at this stage resulting in an underestimated channel loss calculation. Therefore, for proper high frequency characterizations, a test-chip was designed and the actual channel response after fabrications were measured. The structures encompass multiple transmis-

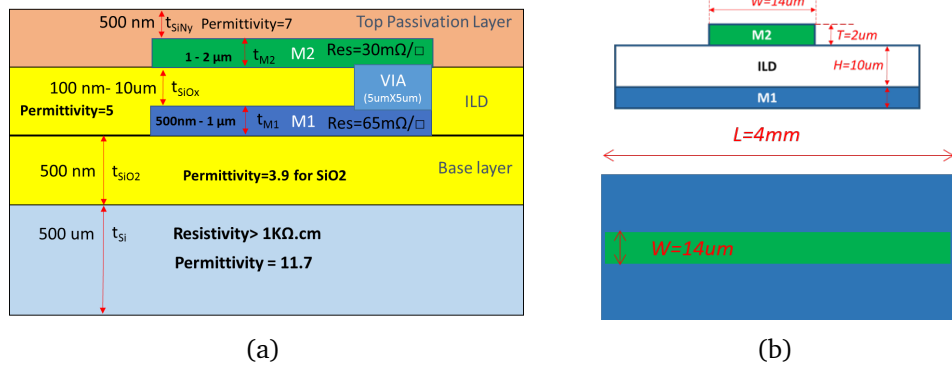


Figure 4.15: (a) Substrate stack-up for 1.2 μm CMOS, Micro-strip line structure to determine the optimal W required for $Z_0 = 50 \Omega$. In the final version after inclusion of the PADS, the width increased to 16 μm to compensate for the effect of additional parasitic capacitance. The dielectric (ILD) thickness is 10 μm .

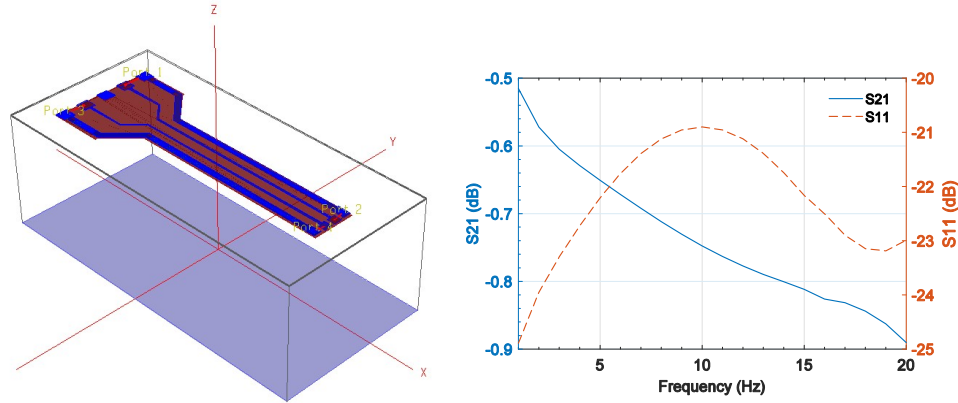


Figure 4.16: Imported layout of the input differential data line in ADS environment, the single-ended S_{11} and S_{21} based on EM simulations with ADS Momentum. The coupling values (S_{31} and S_{41}) are negligible (< -30 dB)

sion lines which are micro-strip T-lines, grounded co-planar wave guides and a replica of the input data and clock routes. Using this method, we could estimate the actual channel response of the main silicon interposer and correct them in the main CDR set-up, if necessary. The PCB and input connectors losses are measured by allocating some space to “calibration traces” on the same board. The PCB type is Rogers based and the manufacturer stack-up information was used to perform EM simulations on PCB tracks as well.

4.2.2 DC and High Frequency Measurements

Due to the large area of the interposer chip, Fig. 4.17, and the difference between the Coefficient of Thermal Expansion (CTE) of the silicon and PCB materials most of the packaged samples failed. After few trials only one safe sample

was produced which allowed us to perform measurements on just the data path related interconnects. At first, DC measurements were carried out which re-

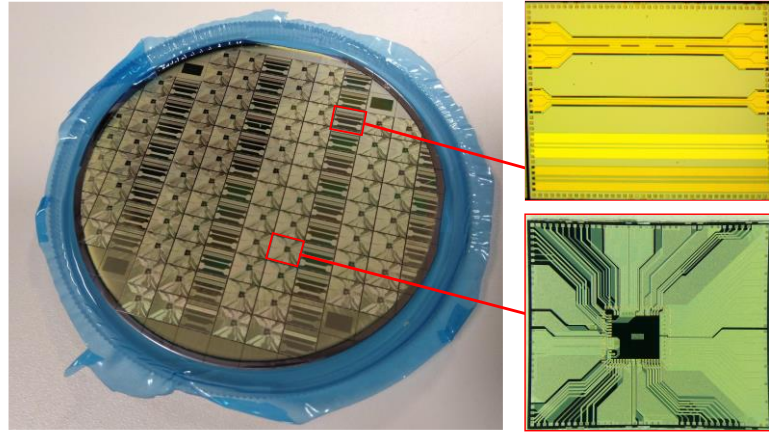


Figure 4.17: The image of a 4" silicon wafer (the photomask reticule contains three chips) and the micrographs of the test structure and CDR interposer in $1.2\ \mu\text{m}$ CMOS. (Size: $8\text{mm} \times 7\text{mm}$).

vealed that each of the signal lines for the calibration and DUT traces has resistivity of $1\ \Omega$ and $9\ \Omega$ respectively. This implies that the combination of the DUT signal lines and C4 (controlled collapse chip connection) bumps account for the DC resistance of $8\ \Omega$. The resulted loss can be a concerning factor when the signal and power integrity are important requirements. Further inspection by using on-die DC probing showed that the issue arises from the quality of the C4 bumps during the packaging process rather than the DUT lines. In the following sections we continue with the high frequency characterization. However, considering both the mechanical and electrical reliability issues, we abandoned the idea of the fully flip chip option and proceeded with the wire-bonding of the silicon interposer to the PCB.²

Since at the time of measurement no BALUNs or four-port vector network analyzer (VNA) were available, single-ended scattering parameters are extracted by repeating two-port measurements. The calibration trace is used to estimate the channel response of the fixture networks. Then the results obtained from this phase are used for “de-embedding” the DUT response from the input PCB connections as follows. Each of the calibration and main PCB lines with DUT can be identified as a four-port network with the following scattering matrix.

²Due to this issue the design and manufacturing processes had to be repeated for the main CDR's PCB.

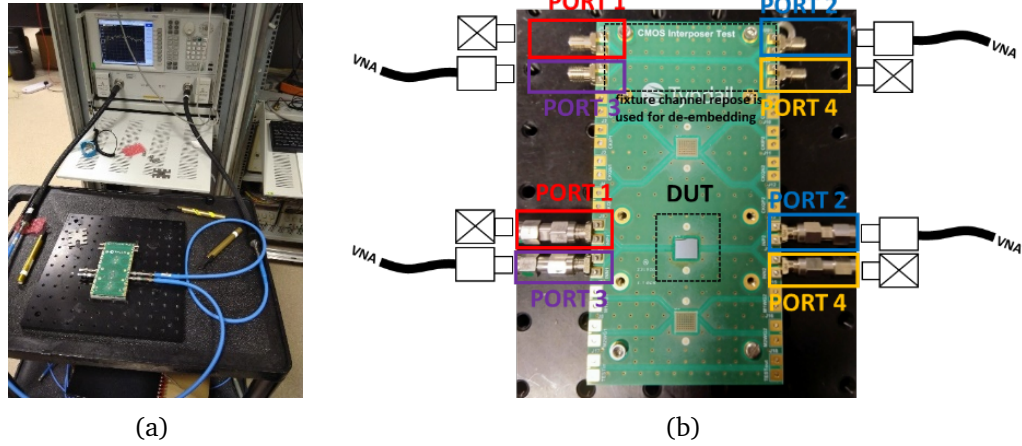


Figure 4.18: (a) Test PCB and (b) the S parameter measurement set-up for calibration board and DUT lines, the set-up measures thru response (S_{21}) of the four-PORT network using PORT1 and PORT2

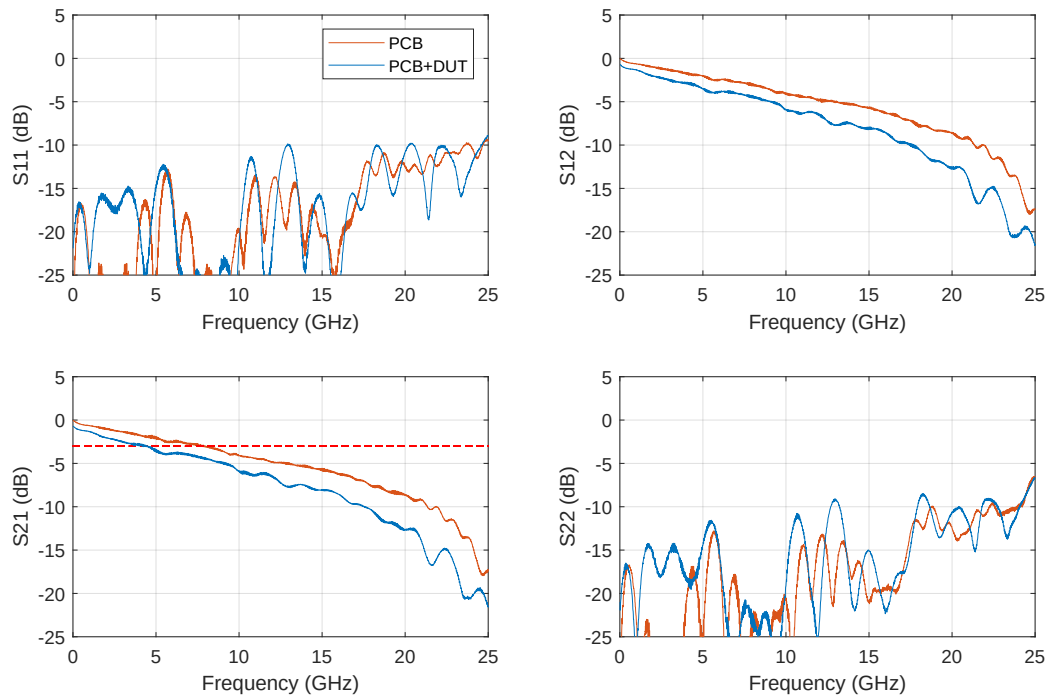


Figure 4.19: Results for the set-up of Fig. 4.18. S_{11} (identical to S_{22} , S_{33} and S_{44}) and S_{21} of the network. Note that here only the amplitude responses are shown however for the calculation the phase responses are used as well.

$$[S] = \begin{pmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{pmatrix} \quad (4.6)$$

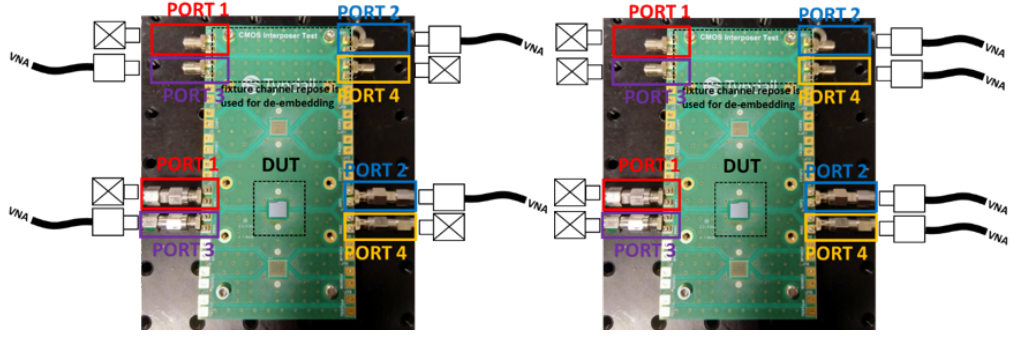


Figure 4.20: setup for measuring the coupling response S_{32} and S_{42} (identical to S_{41} and S_{31}) for near and far PORTS. Since the network is reciprocal and symmetrical any cross connection can be used.

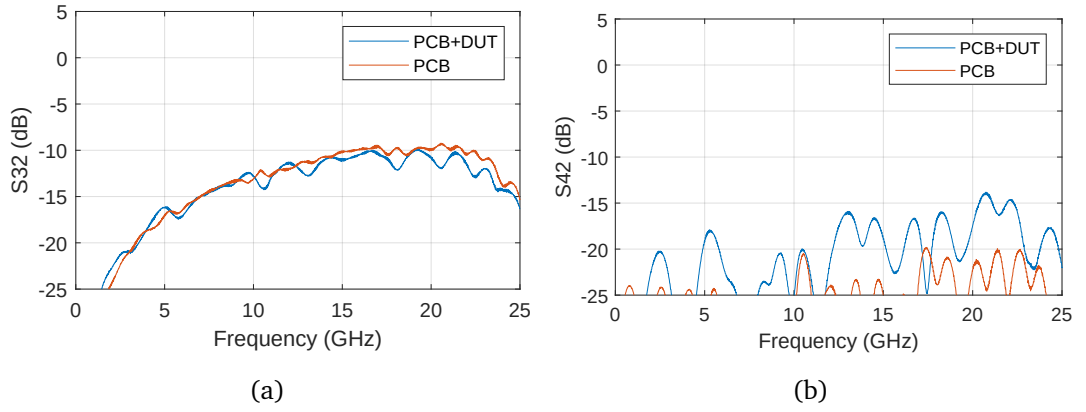


Figure 4.21: Recorded values for S_{32} and S_{42} (identical to S_{41} and S_{31})

Since the connections consist of only passive components and the networks are symmetrical and reciprocal hence $[S]$ can be simplified to:

$$[S] = \begin{pmatrix} S_{11} & S_{21} & S_{31} & S_{41} \\ S_{21} & S_{11} & S_{41} & S_{31} \\ S_{31} & S_{41} & S_{11} & S_{21} \\ S_{41} & S_{31} & S_{21} & S_{11} \end{pmatrix} \quad (4.7)$$

in which S_{21} is the through path response while S_{31} and S_{41} account for the transmission via coupled paths. This reduces the characterization procedure to three two-port-measurement cases. The reflection coefficient, S_{11} , is identical for all the cases. The results for each scenario are shown in Fig. 4.18 to Fig. 4.21.

We can use signal flow graphs [61] to derive the set of equations necessary to find the scattering parameters of the fixture network and DUT as depicted in Fig. 4.22. To avoid confusion in notation we denote the measured scattering

parameters for the calibration traces and the part with DUT as $[S_C]$ and $[S_t]$ matrices while for the fixture network and DUT itself we define $[S_F]$ and $[S_D]$ matrices, respectively. In addition to being identical, we suppose that the individual fixture networks are symmetrical and reciprocal i.e. $[S_{F11}] = [S_{F22}]$ and $[S_{F21}] = [S_{F12}]$, this was confirmed by the EM simulation results. With reference to the calibration section and fixture network, known as “Thru” connection, and by applying Masson’s rule [62], we can derive the following set of equations:

$$S_{C11} = S_{F11} + \frac{S_{F11}S_{F21}^2}{1 - S_{F11}^2} + \frac{S_{F11}S_{F41}^2}{1 - S_{F11}^2} \quad (4.8)$$

$$S_{C21} = \frac{S_{F21}^2}{1 - S_{F11}^2} + \frac{S_{F41}^2}{1 - S_{F11}^2} \quad (4.9)$$

$$S_{C41} = S_{F11} + \frac{2S_{F41}S_{F21}}{1 - S_{F11}^2} \quad (4.10)$$

and for the section including DUT, we have:

$$S_{T11} = S_{F11} + \frac{S_{D11}S_{F21}^2}{\Delta} + \frac{S_{F11}S_{F21}^2S_{D21}^2}{\Delta} + \frac{S_{D11}S_{F41}^2}{\Delta} + \frac{S_{F11}S_{F41}^2S_{D21}^2}{\Delta} \quad (4.11)$$

$$S_{T21} = \frac{S_{D11}S_{F21}^2}{\Delta} + \frac{S_{D11}S_{F41}^2}{\Delta} \quad (4.12)$$

$$\Delta = 1 - S_{F11}^2S_{D21}^2 - 2S_{F11}S_{D11} - S_{F11}^2S_{D11}^2 \quad (4.13)$$

note that these equations are derived upon the assumptions that: a) the ef-

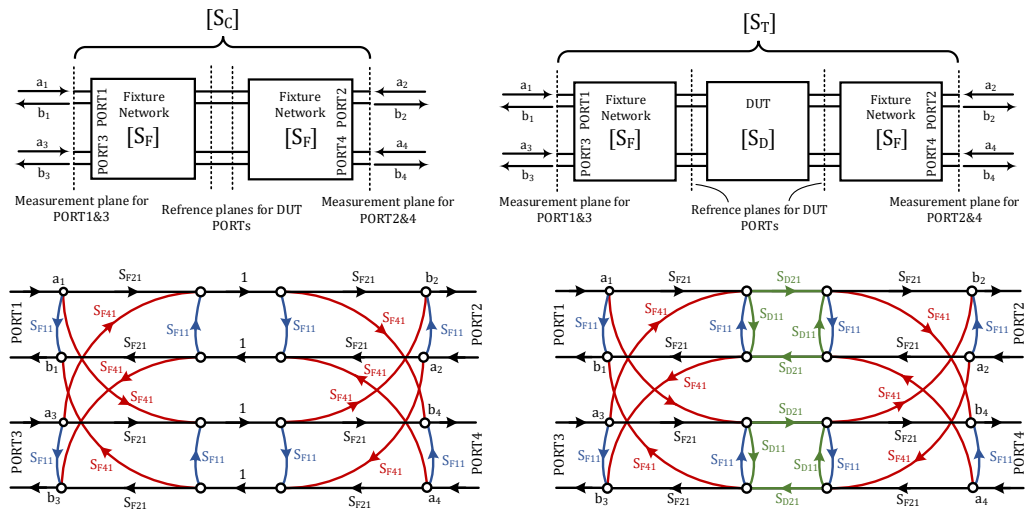


Figure 4.22: Block diagram and SFG of the measurement setup for Thru connection (left) and DUT connection (right)

fect of length mismatch between the fixture networks in the DUT connection

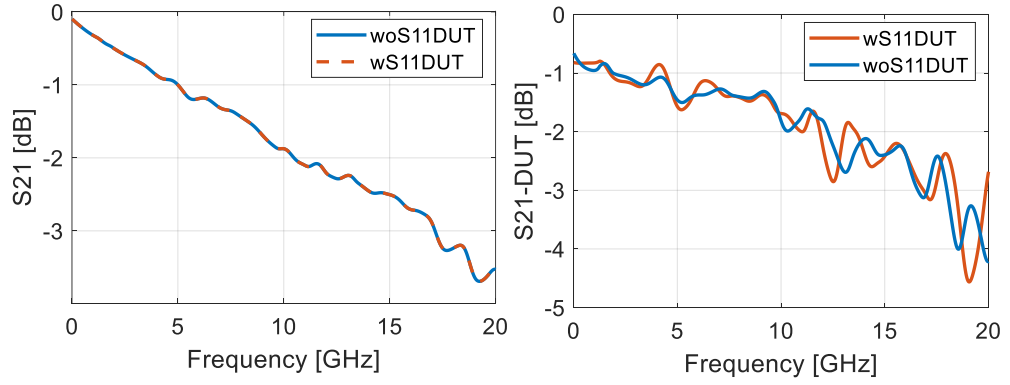


Figure 4.23: Calculated Fixture (left) and DUT (right) insertion losses from measurements with and without DUT S_{11}

and those in the calibration trace, on reflection loss (S_{F11}) is negligible. For the insertion loss however, given that the removed part is roughly $1/7$ of the total trace's length, it can be compensated by subtracting an offset value of $0.07 \times S_{T21}$ (S_{T21} of calibration traces) from S_{F21} . b) since S_{31} is below -15 dB over the bandwidth of interest (≈ 20 GHz) it is not included in the expressions and c) for the DUT only the reflection and insertion losses are considered and the effect of coupling is neglected as the comparison of the results for S_{41} in Fig. 4.21 suggests little differences. The solution to the set of equations gives the scattering parameters for the fixture network and DUT. The calculated frequency responses are shown in Fig. 4.23.

4.3 Testing of the CDR

4.3.1 PCB Design Consideration and Test-bench Preparation

The CDR chip was fabricated in 65nm CMOS bulk technology with the active chip area of 0.67 mm^2 . The micrograph of the chip is shown in Fig. 4.24. For the packaging, as explained earlier, the CDR was flipped chip over the silicon interposer and the whole module is wire-bonded to the test PCB, Fig. 4.25. The chip is placed close to the edges which shortens the length of high speed data and clock traces. Edge mounted GPPO connectors with semi-rigid adapters facilitate connections to K (2.92 mm) cables. The 10 differential outputs are accessible through 20 SMA connectors forming a semi-circle shape. Since the lines are longer, to obviate extra losses their widths are increased. Based on EM simulations the soldering mask was removed over the lines to achieve better impedance matching. The block diagram for the first version of the testing setup

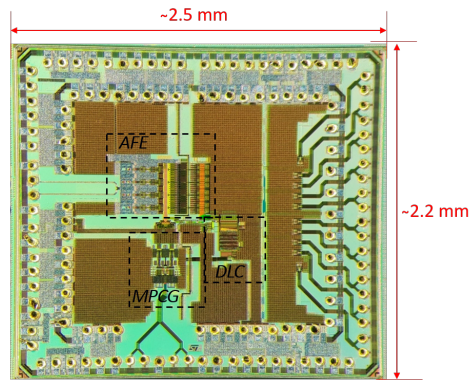


Figure 4.24: PAM4 CDR chip micrograph

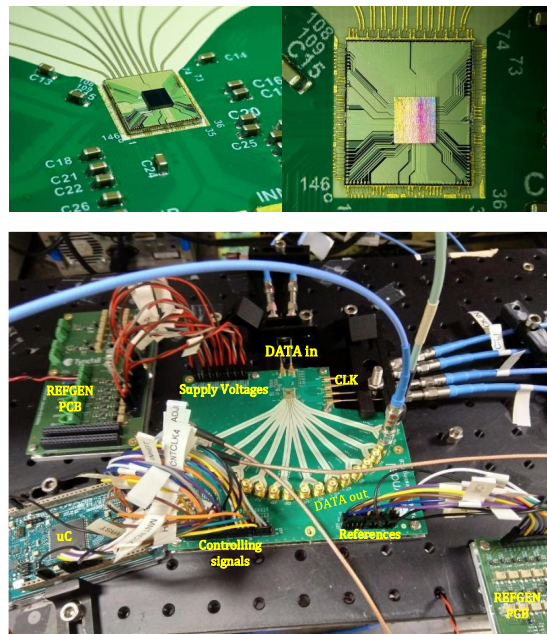


Figure 4.25: The view of the packaged CDR and the testing PCB

(TS1) is illustrated in Fig. 4.25 in which the input clock and data patterns are provided by SHF 78120B and SHF 12124A, respectively. For monitoring the recovered clock, output data and loop filter's output a four-channel real time sampling scope (Tektronix DPO 1254) is connected to the testbed. Similar to DPC testing, the reference generator PCB provides the required bias voltage and currents. The CM levels for both clock and data inputs are provided through bias tees. Communications with μ C unit, to execute required code sequences, are provided within MATLAB environment. Owing to the complex architecture, step by step measurements were carried out to ensure that individual building blocks are functional prior to the top level CDR measurements. As depicted in Fig. 4.27, available TPs (test-points) for probing are:

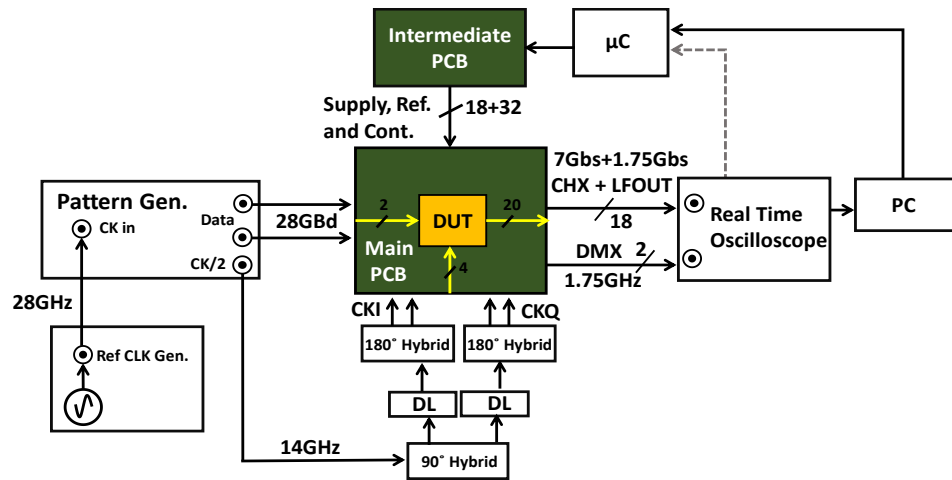


Figure 4.26: Simplified block diagram of the initial setup (TS1) for testing of PAM4-CDR, (bias tees not shown)

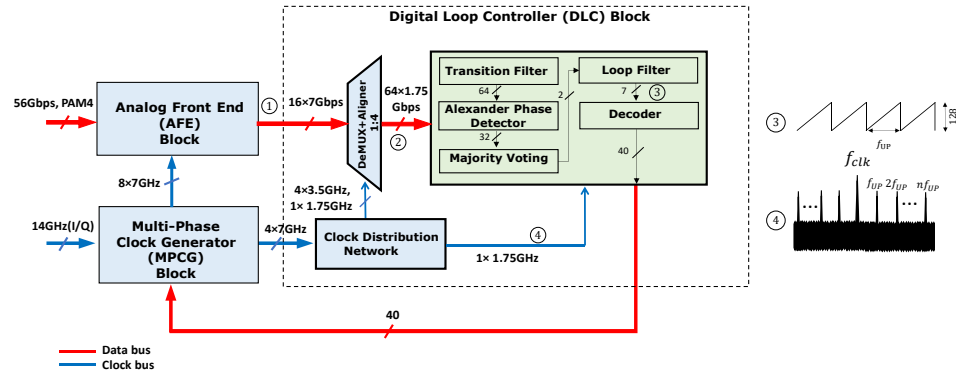


Figure 4.27: available TPs for probing the CDR chip and verification of DLC+MPCG functionality

1) Output channels in AFE section which represent the recovered data for BER measurements. In the circuit design phase, to reduce I/O pad counts, a dedicated multiplexing block is instantiated at the AFE output, providing access to edge samples by means of the same pins. These edge samples are a part of the input for PDs (Phase Detector) inside the DLC block.

2) Outputs of DEMUX block, 16 out of 64 bits are accessible using DMXMNTR output for AFE-DEMUX phase alignment.

3) The serialized output of the loop filter to investigate the phase tracking.

4) The monitoring block outputs the divided-by-four of the recovered clock, the same clock used by the digital section.

The steps for CDR measurements and performance validation are shown in Fig. 4.28 which are explained in detail in the following sections.

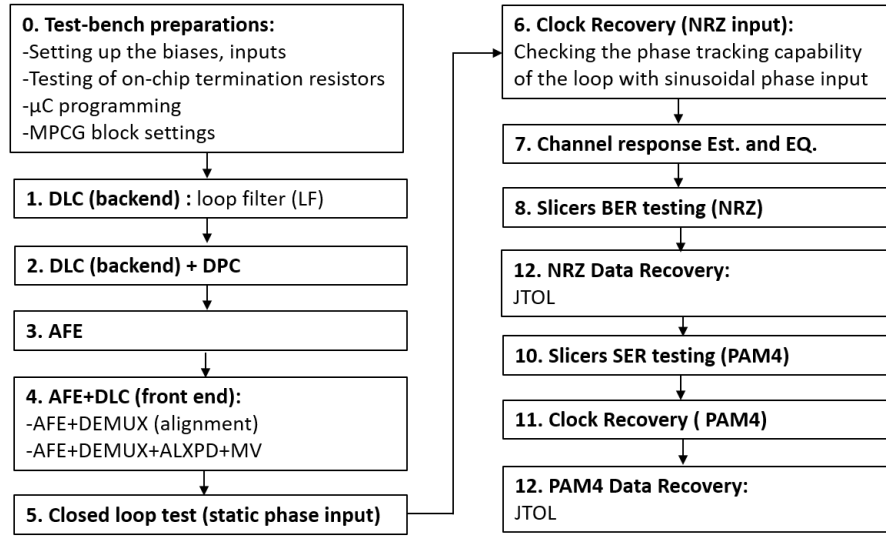


Figure 4.28: CDR's Lab validation steps

4.3.2 Individual Building Block Validation

We begin with the DLC's back-end i.e. the LF section and move around the CDR's feedback loop. As the CDR task is to control the clock, the presence of the system clock at start-up is necessary for the true operation of the CDR. A control signal asserts MPCG input code to 0, initializing the clock phases which at the same time opens the feedback loop. Now, if the coefficient register is loaded with some K_P value while MUXADJ is set to 0 or 2 (making the MUX section output a constant train of early or late signals and ignoring the MV output). A sawtooth signal will be formed at the LF output, as shown in Fig. 4.27. To verify the operation of the decoder block and the connectivity of the DLC's backend to MPCG's code input, one approach is to look at the frequency content of the clock, which is phase modulated by the LF output. As the modulating signal has a full scale amplitude (2π), the spectrum of the clock exhibits sidebands over a wide range of frequencies. Although the power of the sidebands may be estimated by Bessel function, for our quick-check purpose, only the frequency position and spacing of the sidebands are important. It should be noted that the dividers in the path of MPCG to DLC solely down convert the clock frequency from 7 GHz to 1.75 GHz and do not affect the modulating frequency i.e. $\pm f_{UP}$. Using different values for the K_P the recorded offset frequencies are listed in Table 4.2.

In order to test the AFE section, the references for the slicers have to be set by internal DACs. This is realized by enabling the calibration loop and performing the offset cancelation, as explained in section 3.3. For the PAM2 or NRZ data

Table 4.2: measured values for the LF output frequency and clock offset frequencies

LFout frequency (f_{UP}) set by different values of KP	Measured offset with SA
106.8 kHz	108 kHz
213.6 kHz	213 kHz
427 kHz	417-433 kHz

format the slicers references are defined using the same input, 0 V differential voltage, during calibration while for the PAM4 data format, the inputs are adjusted to -0.66 V, 0 V and $+0.66$ V (differential) for bottom, middle and top slicers, respectively. To ensure that the references are set up correctly, a ramp signal is applied using the DC port of the data line bias tees. The slicers' outputs are shown in Fig. 4.29, Fig. 4.30 and Fig. 4.31.

The two-bit-output of the slicers (after thermometer to binary decoders) are demultiplexed by the front-end part of the DLC section. The DEMUX has to align all the sampled data to one clock phase at 1.75 GHz in two steps as discussed in Chapter 3. To accomplish this, first a clock-like data at 3.5 GHz is applied to the input, then the controlling code sequence starts to shift $CK_{1:4}$ through $CNT_clk[3 : 0]$ pins and the numbers on which the state of the respective DEMUX output changes are recorded, Table 4.3. After setting $CK_{1:4}$, the input data pattern frequency is reduced to 1.75 GHz and the CLK phase is adjusted in similar manner via $CNT_clk[4]$ pin. Since these values are dependent more on the fabrication process³, this step is a one-time calibration with no need for repetition at the next start-up.

³Although the temperature and voltage variations may cause shifts, they are both well-controlled parameters within the lab environment.

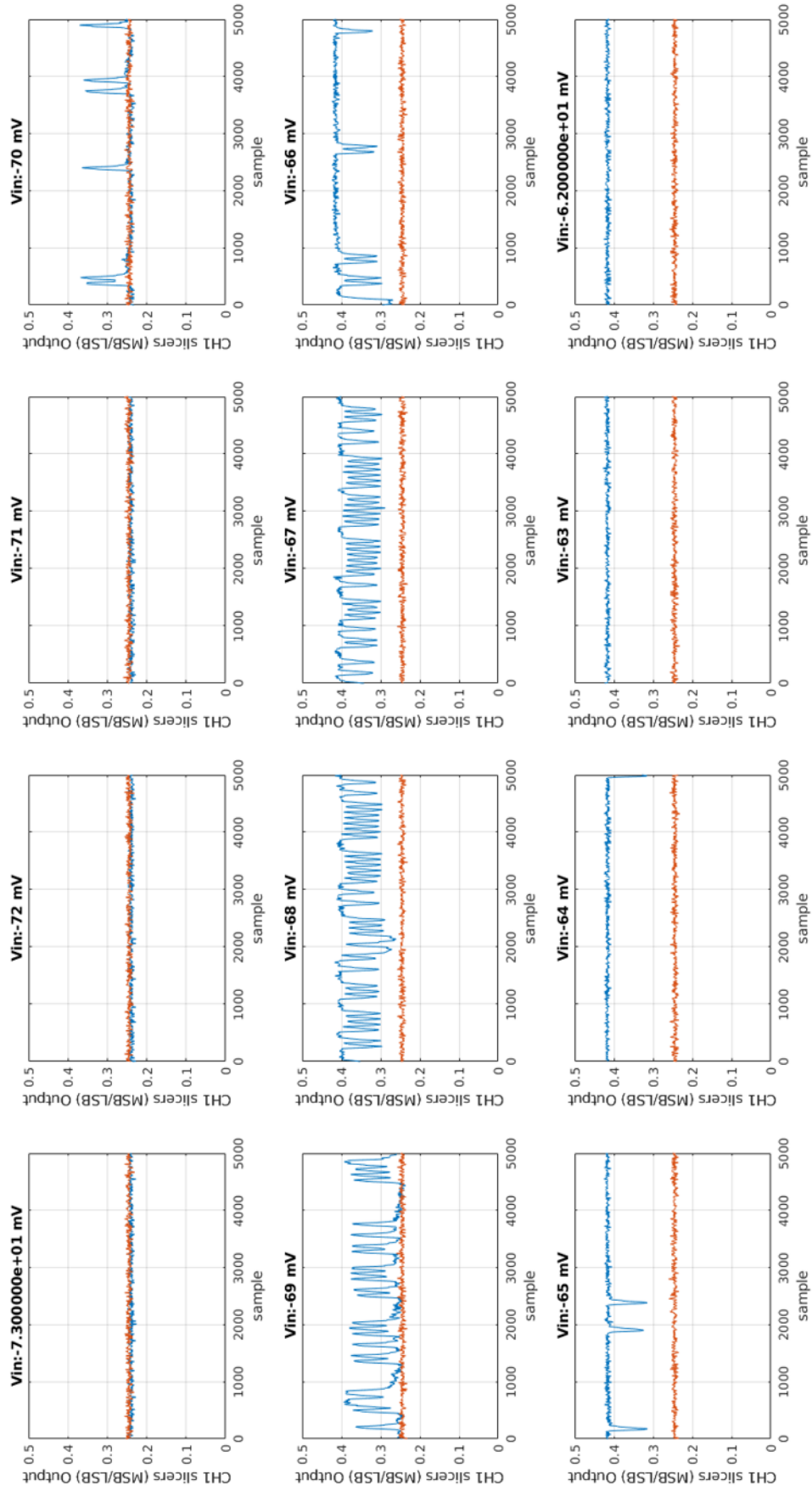


Figure 4.29: Recorded output of the slicers with a 200-mVpp ramp input. The output is shown when the input value is around the threshold of the low-level slicer i.e. $V_L = -66$ mV.

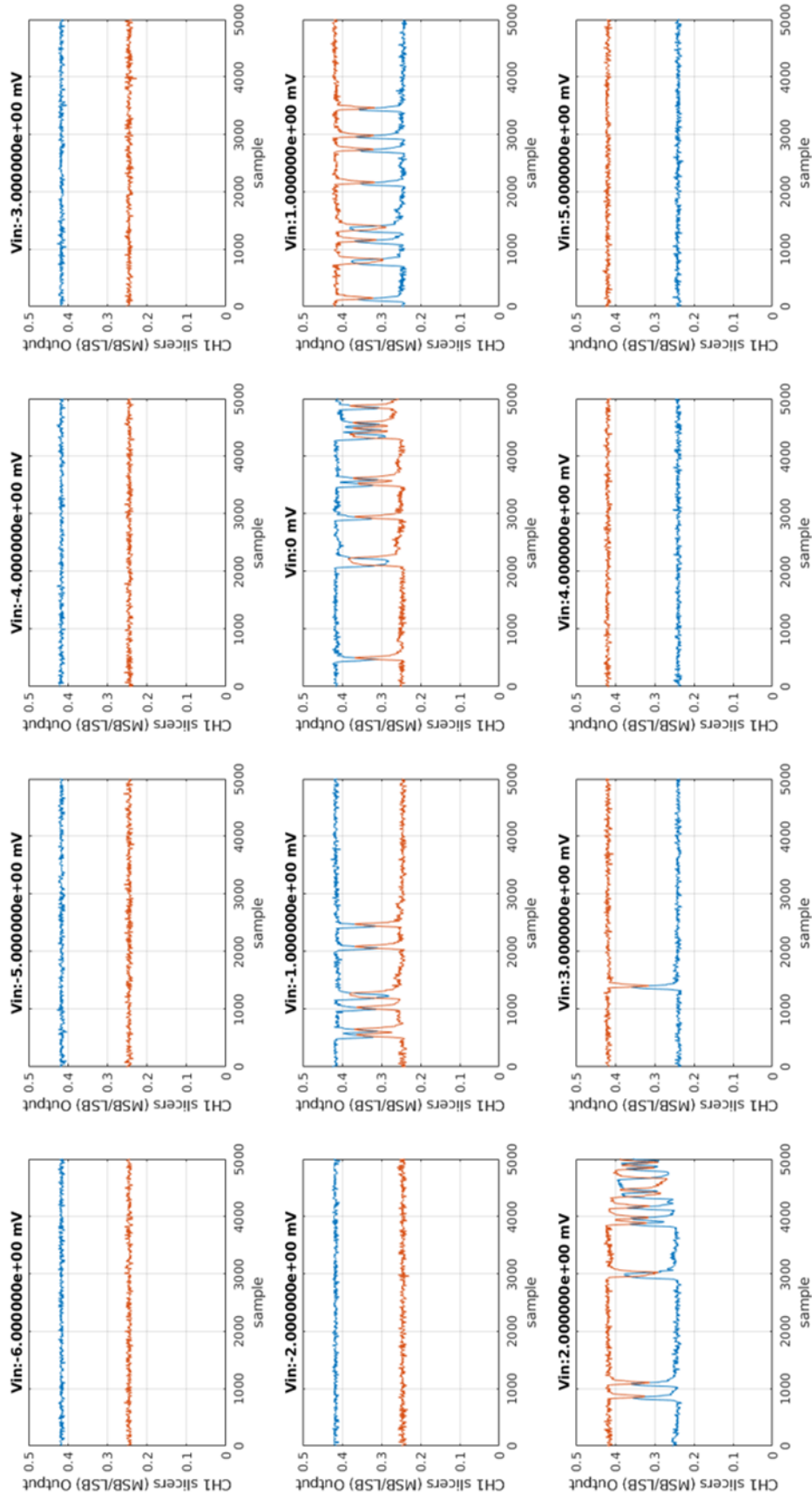


Figure 4.30: Recorded output of the slicers with a 200-mVpp ramp input. The output is shown when the input value is around the threshold of the mid-level slicer i.e. $V_M = 0$ V.

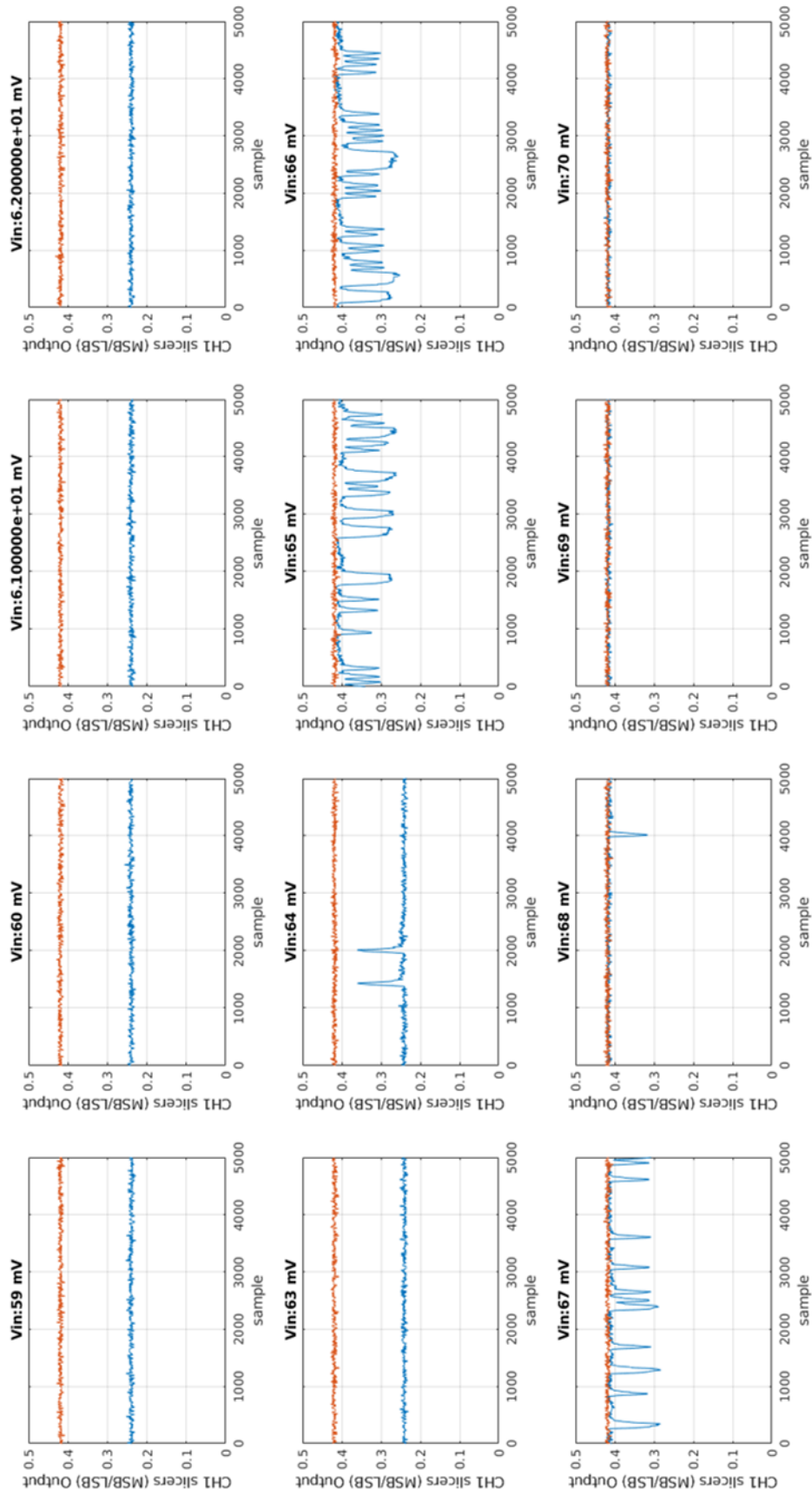


Figure 4.31: Recorded output of the slicers with a 200-mVpp ramp input. The output is shown when the input value is around the threshold of the high-level slicer i.e. $V_H = +66$ mV.

Table 4.3: Measured counters' values for AFE to DEMUX alignment

CNT-clk [n]	0	1	2	3	4
Recorded values*	(1,5)	(2,6)	(3,7)	(4,0)	(2,10)

*the values include rising and falling edges

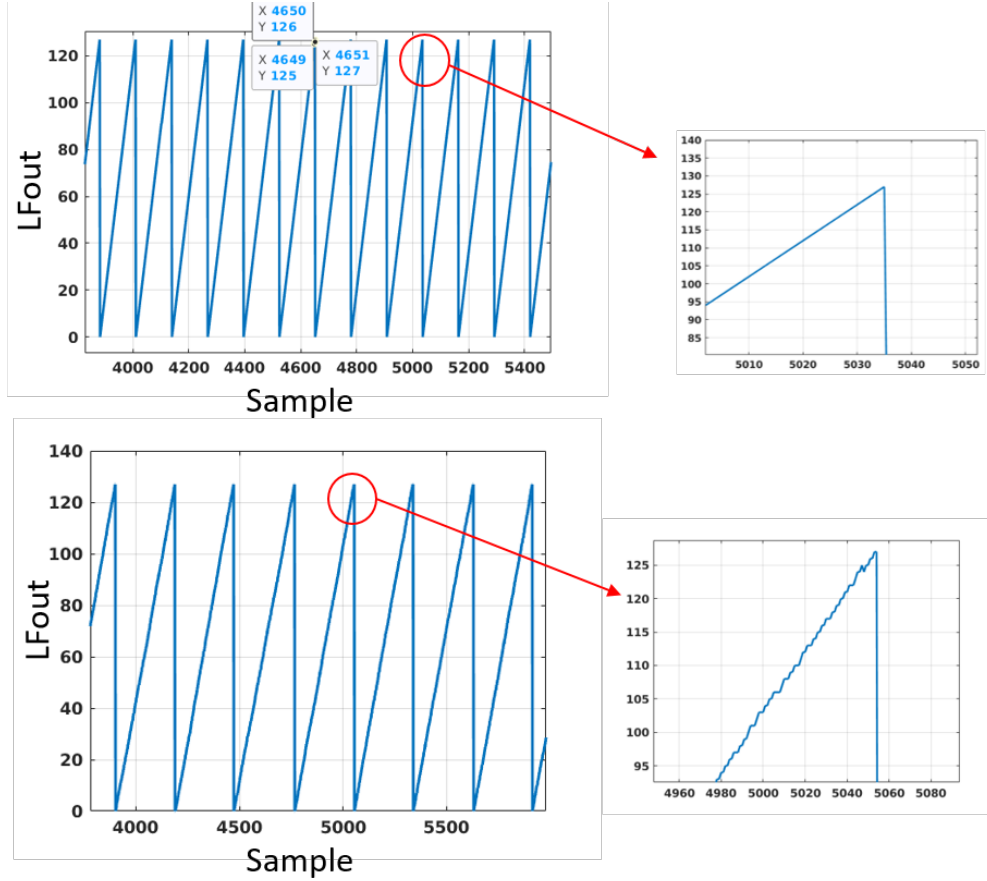


Figure 4.32: Verifying the functionality of the PD and MV, (a) the 7-bit output of LF (Code[0:127]) for the clock-like input signal at $f_{ref}/16$ and (b) PRBS7 input. The reduction in gain of the PD and MV is apparent due to the mismatch among sampling channels. The loop is deactivated.

Validation of the PD arrays and MV blocks is the last part of our journey around the CDR loop. To avert the influence of clock phase skews and possible bandwidth mismatch among multiple channels the input pattern is modified in such a way that data transitions only happen when they are sampled by one channel. In this way, the performance of the ALXPD arrays and MV section can be examined truly. As the CDR feedback is deactivated and the difference between input data and clock phases is constant, the LF would receive constant Early or Late signals from the output of the MV, therefore the accumulator with the gain of K_P would produce a ramp signal as shown in Fig. 4.32. Applying a PRBS7 pattern results in a dithered ramp with a significant reduction in overall gain

due to the phase mismatch of data and clock paths among different channels as seen in Fig. 4.32. Although this would compromise the performance of the CDR in tracking the input phase it would not inhibit the overall functionality.

4.3.3 Phase Tracking Inspection

We have thus far completed checking the operation of the individual blocks in the open loop CDR. The next step is to see whether the CDR is able to track the input phase. It is worth mentioning that, even with a high BER, the CDR loop can still follow the input phase which is changing at a rate far smaller than the data rate. The maximum jitter frequency that we are interested is less than 100 MHz so with a sampling frequency of 7GHz at each channel, it translates to an oversampling ratio (OSR) of 70. Therefore, the CDR will still receive enough information regarding the input jitter. We begin the closed loop measurement with a static phase shift test. Under such conditions the LF output code, after closing the loop, must settle around a certain code with a small dithering. The result is shown in Fig. 4.33.

For the dynamic phase shift, however, the testbed has to be modified (TS2) as shown in Fig. 4.34. Using the modulation function of the clock generator (SHF 78120B) sinusoidal jitter is added to the clock input of the pattern generator (SHF 12124A) and hence data transitions. The clean clock for the CDR is provided by the trigger output of the clock generator. For preliminary tests, sinusoidal jitter with two different frequencies has been used, as shown in Fig. 4.35. As the results indicate, the loop is successfully performing phase locking and the clock recovery part is fully functional.

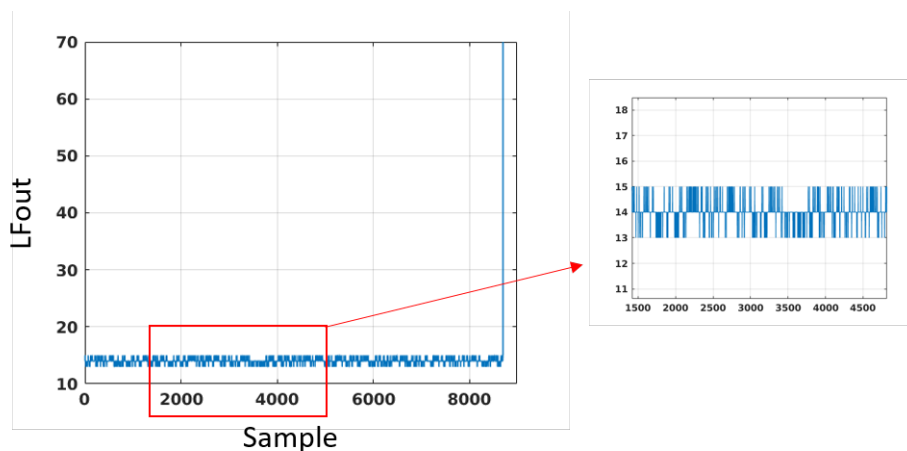


Figure 4.33: the loop filter output when the loop is closed.

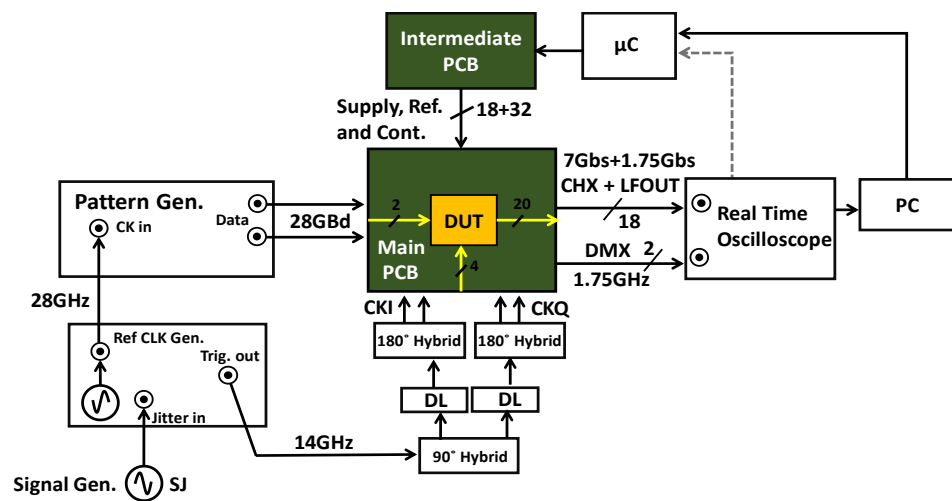


Figure 4.34: phase tracking test setup (TS2) to test clock recovery operation

4.3.4 Channel Equalization and BER Measurements for PAM2 (NRZ)

TS2 lacks the data processing capability required for BER experiments, hence additional changes are made (TS3) as illustrated in Fig. 4.36. Two arbitrary wave generators (Tektronix AWG70001A) are used with one as the clock source and the other one as the pattern generator. The AWGs are synchronized using a synch line. To record the output data another real time scope (DPO 71254B) is connected to the PCB's SMA connectors. Because of the equipment bandwidth limitations, it was decided to reduce the data rate to 25 GBd and hence the clock frequency to 12.5 GHz.

In order to maintain signal integrity for BER measurements, the input channel bandwidth limitation and frequency loss have to be compensated using equalizing techniques. The input channel encompasses all the parts from the output circuitry of the AWG, cables, RF amplifiers, PCB, interposer and packaging parasitic. As there is no direct access for probing the effect of PCB, interposer and the wirebonding losses, at first, the equalization is performed only up to the PCB inputs i.e. until the GPPO connectors. The channel response is estimated based on the method developed in [63], Fig. 4.37. By employing an FIR filter the channel frequency response is equalized wherein the filter coefficients were calculated using IFFT and the inverse of the channel frequency response. The results are shown in Fig. 4.38. It should be noted that the FIR filter sample rate is much higher than the targeted baud rate and the effective bandwidth of equalized channel is restricted to be 20 GHz, evading the BER degradation due

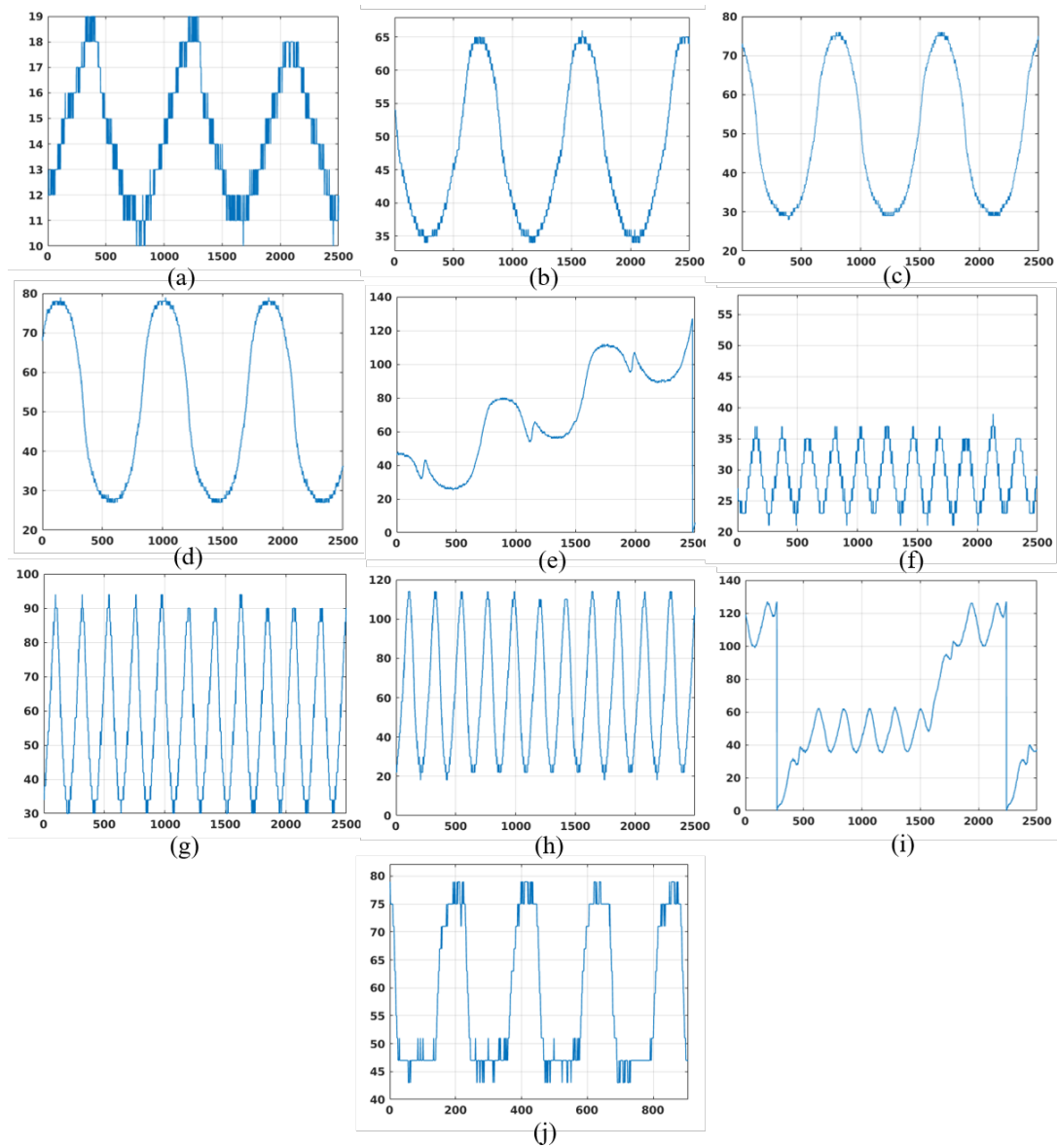
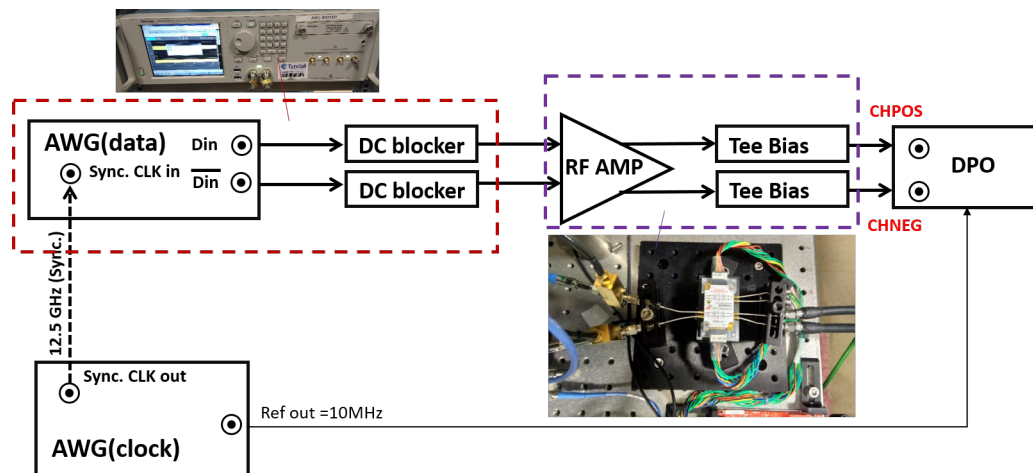
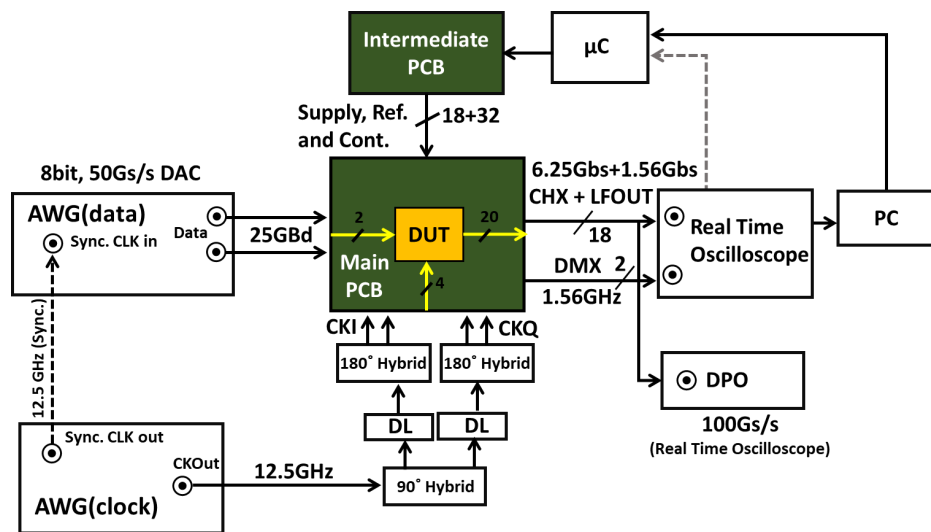


Figure 4.35: LF output as the 28-GBd NRZ input data is phase modulated by sinusoidal jitters: at the jitter frequency of 250 KHz with amplitudes of (a) 100 mVpp (b) 400 mVpp (c) 800 mVpp (d) 1000 mVpp and (e) 1200mVpp, at jitter frequency of 1 MHz with amplitudes of (f) 100 mVpp (g) 200 mVpp (h) 300 mVpp (i) 350 mVpp and (j) a pulse signal with 100 mVpp amplitude, The CDR loses the lock in (e) and (i)

to SNR reduction by thermal noise.

The BER bathtub curve is obtained by skewing the clock phase w.r.t the data transitions and capturing the output of the slicers with a DPO. Using cross correlation of the received bit stream and the transmitted PRBS, the excessive path delay is removed then the number of errors are counted. Considering the length of the captured symbols by DPO (1 Mbits) , our setup can guarantee a confi-



dence level (CL) ⁴ of more than 99% for BER of 10^{-5} . This BER is one order of magnitude less than our targeted BER threshold of 10^{-4} for JTOL.

The results show that in the best case the BER is 10^{-4} . As explained, the input equalizer is compensating the frequency distortion introduced by the channel up to the PCB input. However, the rest of the channel can impact the BER significantly. This part includes the PCB, packaging and input part of the AFE (S/H). To mitigate these imperfections a symbol based FFE with three taps is invoked. The idea is to perform a blind equalization i.e. updating the filter taps based on the gradual decrease in BER. With a few iterative experiments, the values for the normalized taps were found in which the best BER is achieved

⁴Here the calculation of the confidence level for a certain BER is based on: $CL = 1 - e^{(-Nbit \times BER)}$ in which Nbit is the size of an error-free ensemble.

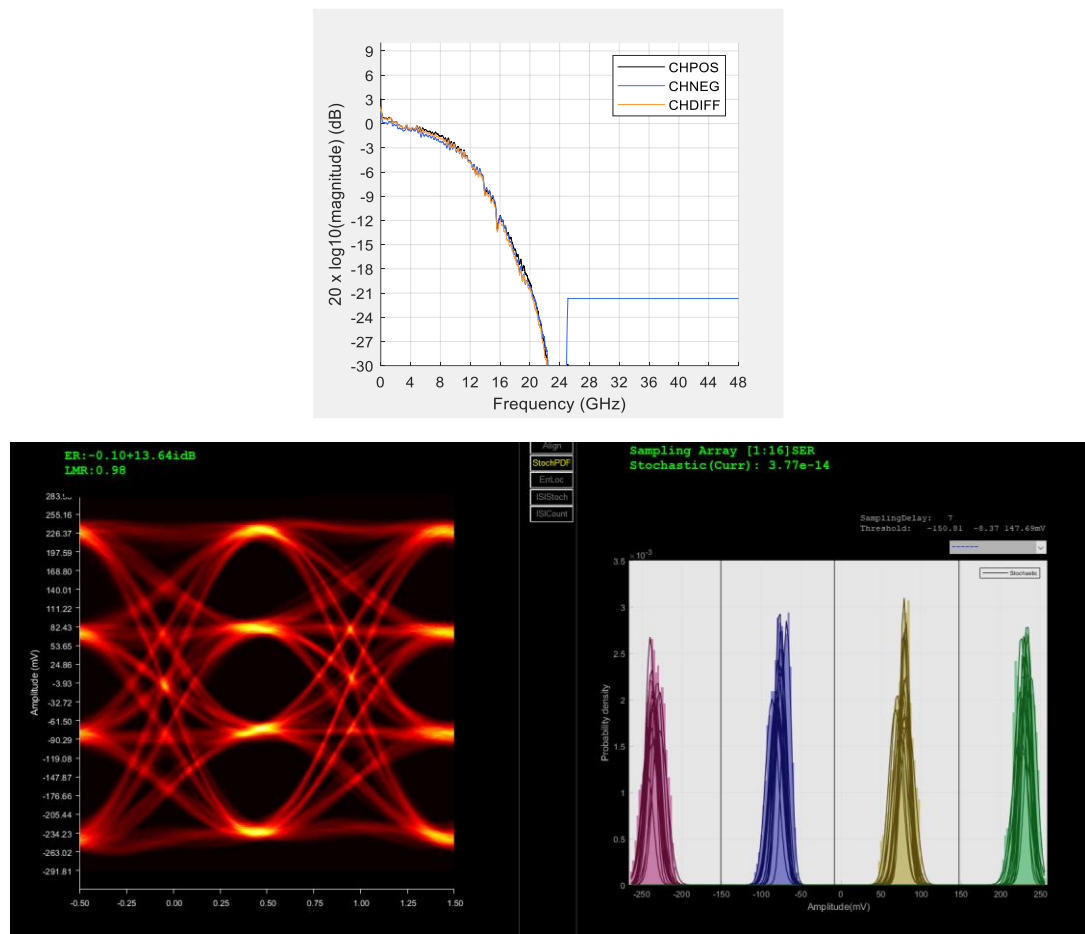


Figure 4.38: channel frequency response and the equalized differential 25 Gb/s PAM4 eye diagram at the output (PRBS7)

Fig. 4.39. More taps also were tried however this did not improve the results considerably.

4.3.5 Jitter Tolerance (JTOL) for PAM2 (NRZ)

Returning to our main objective, now we can investigate the CDR's output BER in the presence of jitter. The results for the static phase shift are shown in Fig. 4.40 in which a phase step (< 1 UI) is applied to the input and the response of the CDR before and after closing the feedback loop is measured. For the dynamic test, the jitter is added to data transitions through the MATLAB workstation code, mandating a dedicated verification testbed. For this reason, a software based code is developed which emulates the CDR hardware using the samples directly taken from the AWG output by the DPO, as shown in Fig. 4.41. The CDR emulator then extracts the jitter and data pattern from the AWG samples. The results for some jittered inputs are shown including the sampled

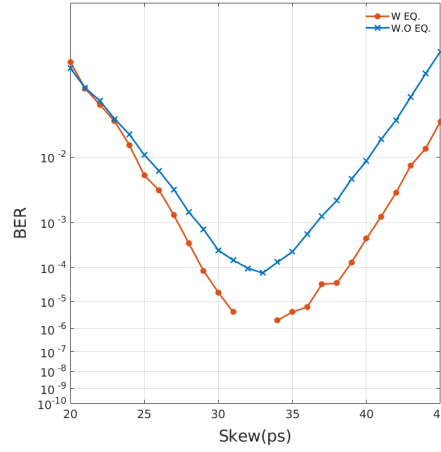


Figure 4.39: the BER curve vs phase skew, with and without 3-tap symbol based FIR. The tap coefficients are $[0, 1, -0.3]$. The input is a 25 GBd, PRBS15 NRZ.

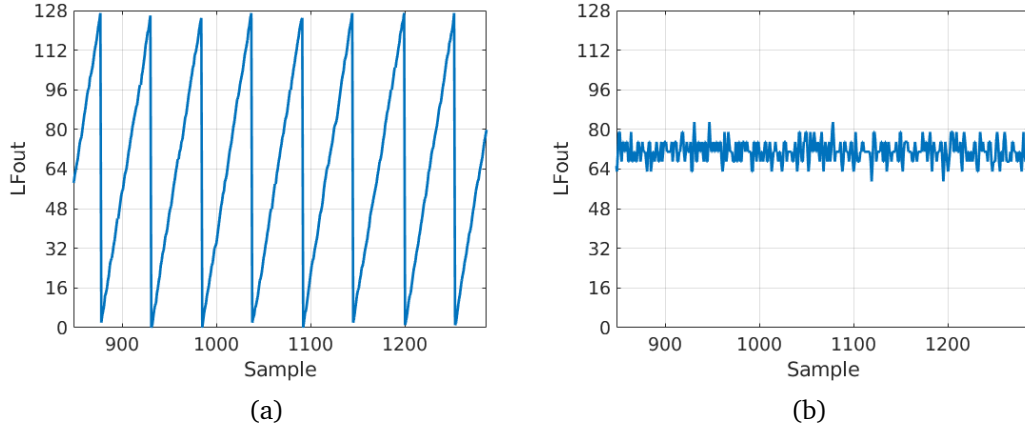


Figure 4.40: The static phase tracking and resulted BER, the CDR input (25 GBd PRBS7 NRZ) is shifted from a sampling point with $BER = 0$ by applying a time step of 15 ps (0.375 UI). The resulted loop filter output is shown before and after closing the feedback loop. the Recorded BER for (a) is 1.83×10^{-1} and for (b) is 0

eyes in Fig. 4.42. As a caveat, we should be attentive to the sampling nature of our jitter generation method; there is a relation between the pattern length, N , with the baud rate of R_b , uploaded to the AWG and the frequency of the jitter, f_j , as:

$$\frac{M}{f_j} = \frac{N}{R_b} \quad (4.14)$$

Eqn. 4.14 is similar to the criterion that is often referred to as coherent sampling which describes the sampling of a periodic signal. In this case, an integer number of sinusoidal jitter cycles, M , fits into a predefined sampling window proportional to N . This is a necessary condition to avoid any phase glitch as the AWG keeps repeating the input pattern after N samples, and its violation could

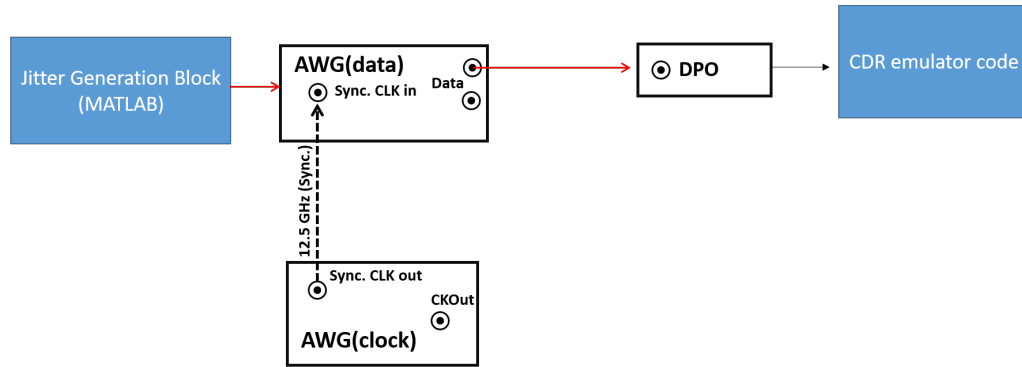


Figure 4.41: test bed used for validation of the jitter generation and CDR emulator functions

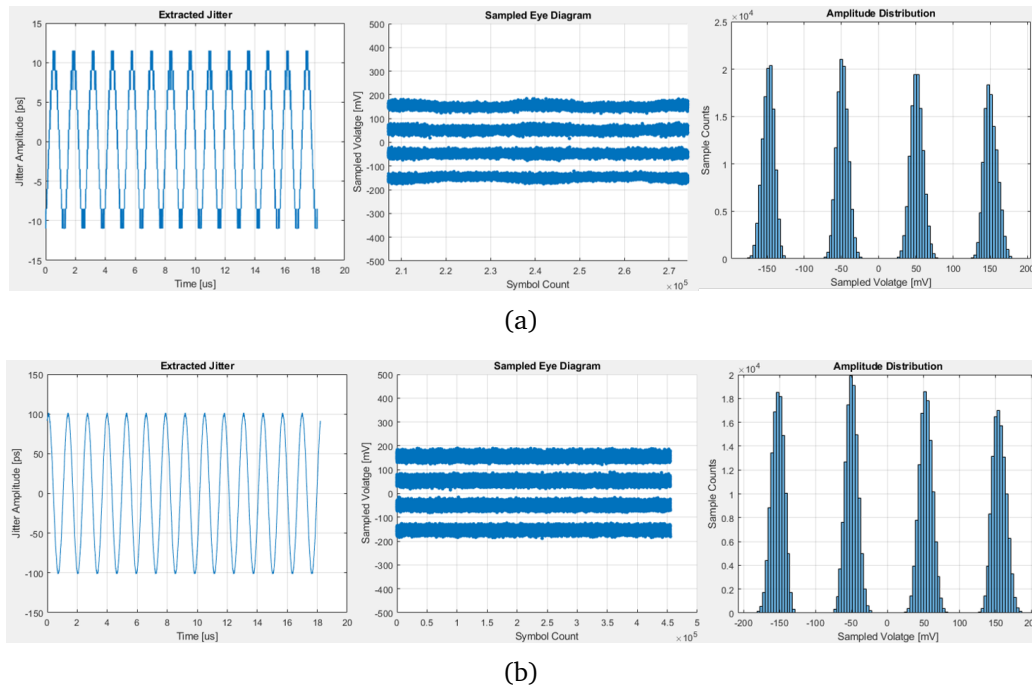


Figure 4.42: Results for the jitter tracking and sampled eyes by CDR emulator. The results are shown for jitter frequency of 0.7689 MHz with jitter amplitude of (a) 10 ps (b) 100 ps

deteriorate the measured BER due to the momentary loss of lock by the CDR.

Due to the asynchronous data acquisition and the fact that the recovered data contains the same amount of jitter as the input, the CDR emulator code is also used at the slicers' outputs for the correct BER testing. Fig. 4.43 compares the jitter at the output data, extracted by the CDR emulator and the CDR's LF output.

For the jitter tolerance, a few jitter frequency points were selected. At each frequency point the BER was measured after every incremental step in jitter

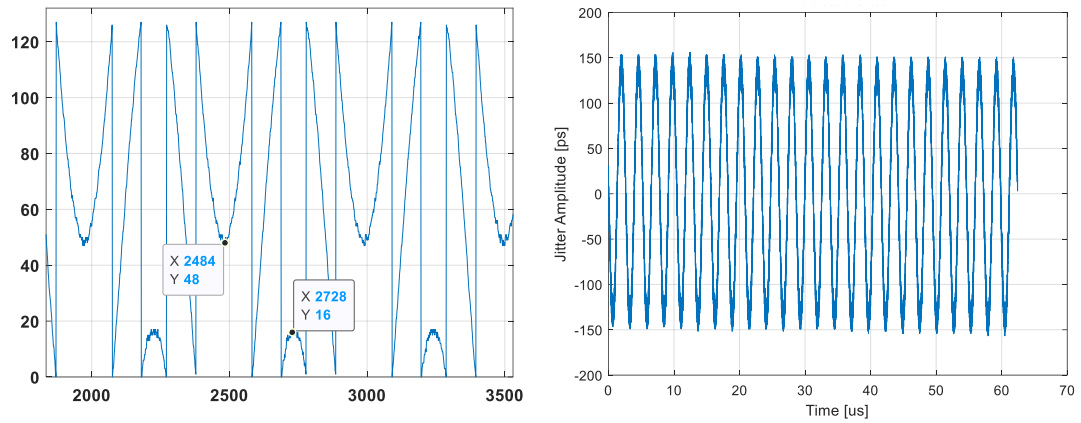


Figure 4.43: comparison of jitter amplitude recorded from LF out (left) and the AFE output data (right), the input jitter amplitude is 140 ps at the jitter frequency of 384 KHz, the code shift at the LF output is 225 translating to $225 \times (1.25 \text{ ps}) \approx 280 \text{ ps}$ peak-to-peak jitter.

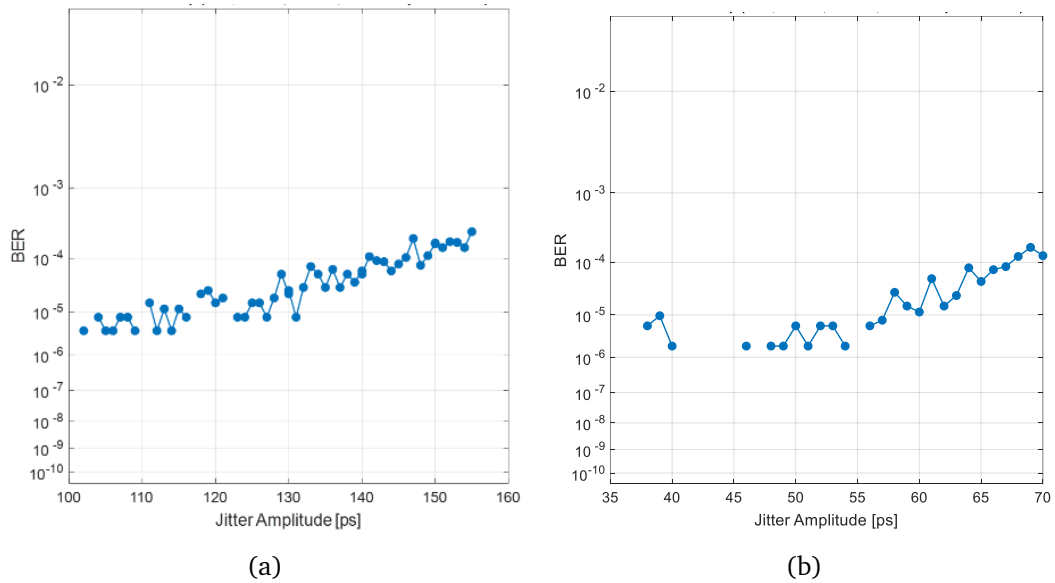


Figure 4.44: BER degradation as the input jitter amplitude increases at jitter frequency of (a) 384 kHz (b) 769 kHz

amplitude. The BER against the jitter amplitude for a few frequency points is shown in Fig. 4.44. As the jitter amplitude increases the BER is degraded, the threshold BER is defined as 10^{-4} . The jitter amplitude at which the BER crosses this threshold is registered as the jitter tolerance value. Fig. 4.45 shows the JTOL for the CDR using PAM2 (NRZ) input. The filter setting is $K_P = 256$ and $K_I = 0$ while all the transitions are activated. The JTOL mask is based on the Optical Internetworking Forum's (OIF) standards for CEI-56G-LR-PAM4 interface [64]. The CDR is able to tolerate 1 UIpp jitter amplitude at 2 MHz frequency. Another parameter of particular interest to us is the loop bandwidth for

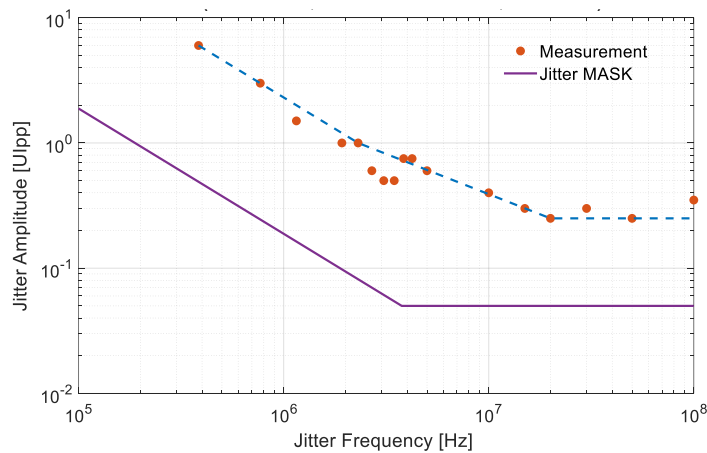


Figure 4.45: JTOL for NRZ (PAM2) input with BER threshold set to be 10^{-4} , The jitter Mask is based on “CEI-56G-LR-PAM4 Long Reach Interface”

jitter transmission. Although direct JTRAN measurements cannot be performed using our current test-bench, JTOL data readily provides the loop bandwidth which is the corner frequency in the JTOL curve and, for this case, it is at around 20 MHz.

4.3.6 BER Measurements for PAM4

Before proceeding with PAM4 JTOL measurements, the BER of the AFE for PAM4 input should be measured. The reason is that, unlike NRZ, the linearity of the AFE is critical for true PAM4 signalling. To generate a PAM4 signal two NRZ patterns are combined while one of the patterns is shifted by one symbol. Following some signal processing the sequence is loaded to the AWG. The jitter generation block is also tested in similar way to the NRZ one. For the slicers outputs the LSB and MSB bits are measured separately. We continued the BER experiments while bearing in mind that the blind equalizer is optimized for NRZ input which inherently is insensitive to nonlinearities so the same FFE configuration and tap values might not be suitable for PAM4. Despite modifying the coefficients and running multiple tests, the results however were not promising and the BER for 25 GBd PAM4 was not satisfactory. To circumvent the issue of bandwidth limitation the input PAM4 sequence is modified in a way that each symbol is duplicated i.e. the effective baud rate is halved and reduced to 12.5 GBd. However, the sampling clock frequency was fixed at 12.5 GHz. The output BER is shown in Fig. 4.46.

To elaborate the issue with 25 GBd input, a diagnostic method was devised in which only small eyes in the PAM4 signal were used to corroborate each slicer’s

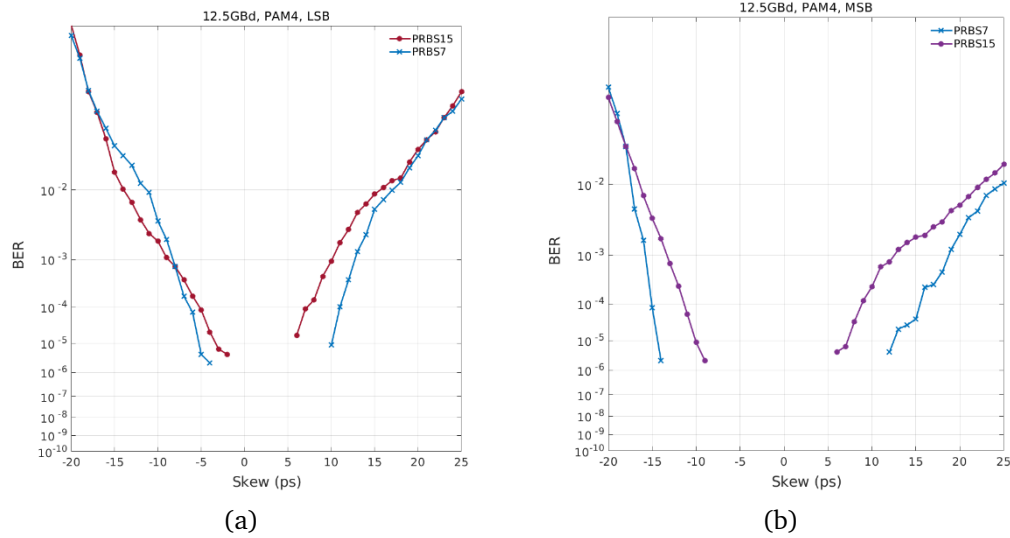


Figure 4.46: BER bathtub curve for 12.5 GBd PRBS7 and PRBS15 PAM4 for LSB and MSB outputs

functionality. Fig. 4.47 illustrates the method in detail. The input swing is kept within the boundaries where the minimum value is determined by AFE's sensitivity while the maximum value does not trigger other slicers even with the FFE enabled. Then a differential DC voltage, V_{IND} , is added to the input to shift the eyes up/down targeting individual LSB or MSB slicers and the BER bathtub curve is extracted. Looking at the results revealed a problem with the lower slicer; increasing the input amplitude and data-clock phase skewing didn't resolve the issue. This observation indicates that the main cause of the failure may not be due the bandwidth limitation imposed by the channel (including AFE's buffers and S/H), rather the problem of the lower slicers and following decoders at resolving the high speed input. Such imperfection given the differential operation of the slicers would not be expected. Possible suspects here are the effect of residual static offset after calibration and the dynamic offset (hysteresis) in comparators while detecting high speed input and depending on their sign, the polarity of V_{IND} with respect to that sign could influence the slicers operation.

4.3.7 Jitter Tolerance (JTOL) for PAM4

Although the AFE did not satisfy the specifications for the PAM4 input with 25 GBd symbol rate, we decided to continue with the modified pattern and investigate the CDR operation. However, the CDR struggled in phase lock acquisition. To examine it carefully we note that in comparison to the functional

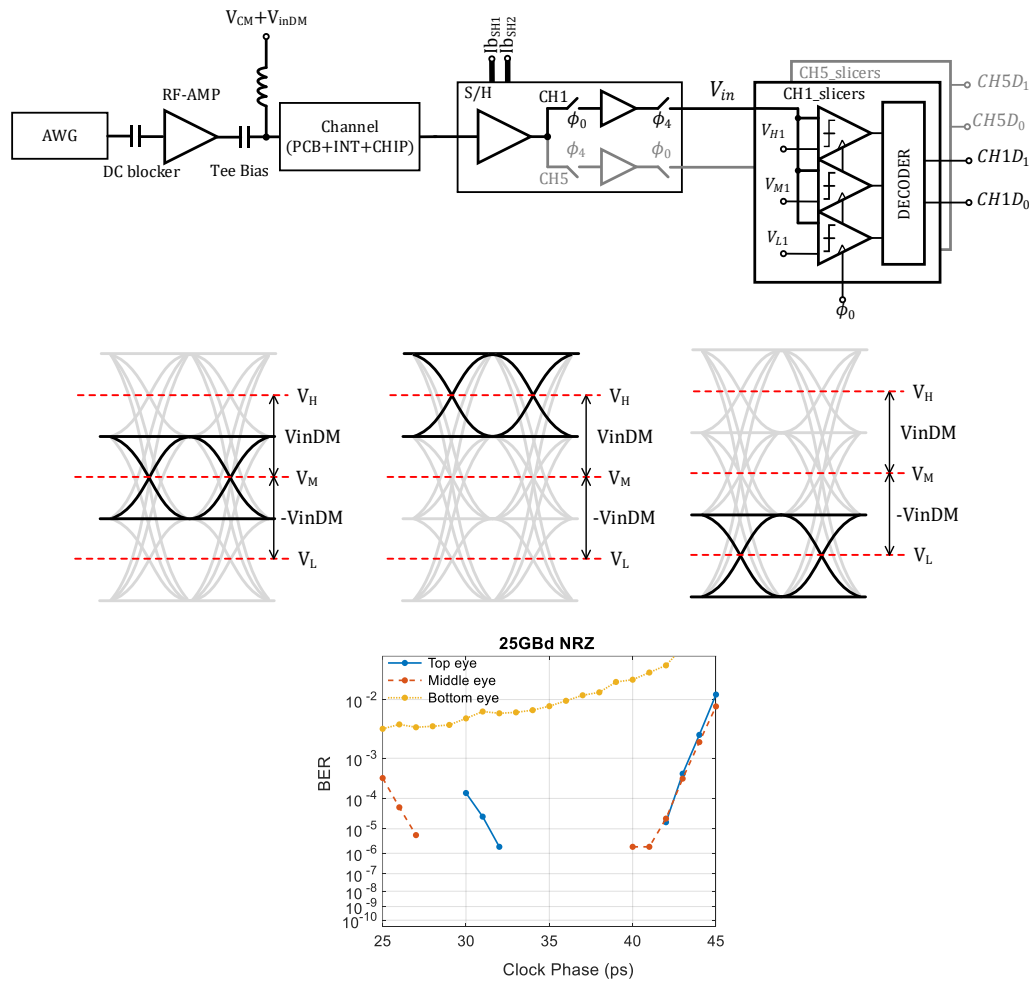


Figure 4.47: The diagnostic method for the AFE failure to operate on 25 GBd PAM4 signal, it revealed the main issue with the bottom-eye sampling part could be from slicers not being able to resolve the input difference at 25 GBd input, the BER is not improving even with increasing the swing and additional data-clock skew

NRZ case, the only difference here is the setting of the slicers reference level by the calibration sections and application of a multilevel signal at the input. Further inspections showed that the calibration circuitry, cannot properly set the reference levels for top and bottom level slicers in some channels. The convergence failure in reference settings proved not to be channel specific as it could occur in different channels after every reset or start-up. This increased the likelihood that the problem stemmed from the calibration circuitry which includes the slicers, DACs and backend logics, rather than the S/H network and input buffers. Regulating the CM levels for the slicers and DACs, modifying DAC's dynamic ranges and initializing the calibration loop offered the most plausible solutions. While for the first two options changing the input current sources and adjusting the bias voltages were used, for the third one manual loading of

the DAC registers was the only alternative approach. However, tweaking the bias conditions didn't resolve the problem and disturbed communications with the ISP registers made it impossible to perform manual reference settings. Unfortunately, Because of these obstructions the PAM4 measurement could not be proceed further and since none of the alternatives were deemed to be viable solutions to tackle this problem, the verification of the CDR with the current test-bed is concluded at this stage. Table 4.4 summarizes the test cases that the CDR has been put through.

Table 4.4: Summary of the CDR's operation

Test Case	BER (bathtub curve results)	JTOL (BER < 10 ⁻⁴)	Failure Mechanism
PAM2 25 GBd	✓ (< 10 ⁻⁶)	✓	-
PAM4 25 GBd	× (> 10 ⁻⁴)	×	one of the slicers operates with high BER
PAM4 12.5 GBd*	✓ (< 10 ⁻⁶)	×	CDR fails to lock (irregular reference settings in slicers)

*Although the input resembles a 12.5Gbd pattern the actual symbol rate is 25Gbd and the CDR operates with 12.5GHz clock, the pattern is generated by symbol repetition of the input PRBS at 25Gbd to alleviate the limited BW issues of the slicers.

Table 4.5: measured values for CDR's building blocks supply voltages and currents

Block	Sub-blocks	Supply Voltage	Supply Current
AFE	2 nd stage buffers + bias blocks	1.16 V	34 mA
	1 st stage buffers+ comparators + DAC	1.06	47.8 mA
DLC	including AFE backend	1 V	55 mA
MPCG	Input dividers + QPC + PR	1.06 V	42.7 mA
	De-skew Buffers + CML to CMOS Con.	1 V	45.5 mA
Output Buffers	-	1.04 V	146 mA

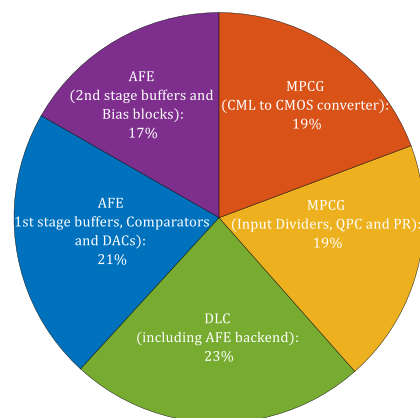


Figure 4.48: CDR's power breakdown, power consumption of the core circuitry = 236 mW (excluding output buffers)

Table 4.6: PAM4 CDR performance comparison

References	[19]	[65]	[66]	This Work*
CDR architecture	PR based	VCO based	VCO based	PR based ^a
Data-Rate	22 Gb/s	56 Gb/s	56 Gb/s	50 Gb/s
Technology	90 nm SOI CMOS	40 nm CMOS	65 nm CMOS	65 nm CMOS
1-UI JTOL bandwidth	1 MHz	2 MHz CMOS	1 MHz	2 MHz
Loop Bandwidth	7 MHz	10 MHz	10 MHz	20 MHz
BER	10^{-12}	$<10^{-12}$	10^{-12}	$<10^{-6}$
Supply	1.1 V	1 V	1.2 V	1-1.2 V
Power	228 mW	382 mW ^b	238 mW ^c	236 mW
Power efficiency	10.4 pJ/bit	6.82 pJ/bit	4.25 pJ/bit	4.27 pJ/bit
Area	0.12 mm ²	0.49 mm ² ^d	0.51 mm ²	0.67 mm ²

*projected performance

^a high frequency external clock source is required

^b including CTLE/DFE as the power break down data is not available

^c excluding CTLE/IIR Summer power for a fair comparison

^d active area is estimated from the chip micrograph

4.3.8 Power Consumption and Performance Summary

Table 4.5 details the supply voltages and currents drawn by each block of the CDR. The voltage values are in the nominal range of 1 V – 1.2 V. Total power consumption of the chip is 388 mW out of which 236 mW is taken by the core circuitry and 152 mW is dissipated by the output buffers driving the I/O pads. Fig. 4.48 summarizes the contribution of individual blocks in percentage of the power consumed by the core circuitry. Although the circuit has issues which prevent complete functionality for the PAM4 signal, the performance for the truly operational version could still be *projected* at 50 Gb/s data rate. Table 4.6 compares the measurement results with some other published works on PAM4 CDR.

4.4 Chapter Summary

This Chapter presented the experimental results for the DPC as a stand alone chip and the CDR chip as the main focus of the work.

The DPC measurements were carried out using frequency domain methods in which phase modulation of the output clock by pulsing the input digital code produces side-bands with the power proportional to the amount of delay corresponding to the input code. Additional experiments assessed the performances of the QPC and de-skewing blocks.

The CDR testing started with the high frequency validation of the silicon in-

terposer which facilitates the packaging of the chip. The CDR had to undergo step-by-step measurements including static and dynamic phase recovery, BER bathtub and the jitter tolerance tests. We started with PAM2 cases and proceed to multilevel PAM4.

The testing with PAM4 proved that there is a functionality issue calling for more investigations. By using different diagnostic methods it was discovered that the LSB slicers cannot resolve the input signal while operating at 25 GBd. Further testing with low speed inputs also showed an issue with reference settings of the CDR. Since these issues were related to the hard core circuitry and there was no work-around techniques available to proceed with the measurements, hence by relying on the NRZ measurement a projected performance was used to compare the results with some prior arts.

Chapter 5

Conclusion

5.1 Work Summary

This work concentrates on the design of CDRs for short-reach optical transceivers which employ PAM4 signalling to achieve the required high speed and density for development of the next generation of scaled interconnects in data centres. A PAM4 CDR was designed in a top-to-bottom flow by introducing enhanced architectures both at the system and circuit levels.

A tri-level PD which improves the performance of PAM4 CDR is presented in Chapter 2. The binary nature of the BBPDs can introduce systematic jitter while dealing with non-adjacent level transitions. Hence most CDR designs avoid using medium transitions which can cause 25% bandwidth reduction. Tri-level PD ameliorates the issue to some extent by conditional use of medium transitions depending on the region of edge samples. Using different techniques, the JTRAN, JG and JTOL of the CDR were analysed and compared against simulation results which proved the effectiveness of the proposed PD.

Next a system level model of the PAM4 CDR is developed and used to investigate the function of each building block. The important design parameters were identified and their effects on the dynamics of the CDR were analysed by using extensive behavioural simulations. We also showed how some circuit imperfections can worsen the performance by back-annotating those non-idealities into the system-level model. This proved that certain trimming or calibration mechanisms are critical to improve the CDR function at the circuit level.

In chapter 3 the circuit level design is discussed. The building blocks, which in-

clude an analog front end (AFE), a digital to phase converter (DPC) and a digital loop controller (DLC), have been designed in 65-nm CMOS technology. The AFE consists of an arrangement of 8 interleaved master and slave sample-and-hold circuits followed by an array of dynamic comparators. Each interleaved channel contains two wideband buffers with accurate bias and common-mode control circuitry to drive the sample-and-hold circuits. The worst-case (across process, temperature and supply voltage corners) aperture time of the sampling front end is 17 ps for a differential input voltage swing of 200 mV, sufficient to resolve a 56 Gb/s (28 Gbaud) PAM-4 signal. For the DPC section, the design introduces a modified phase interpolator (PI) and a quadrature phase corrector (QPC) to reduce the effect of the circuit imperfections on the DPC's resolution and linearity. In addition, de-skew buffers were invoked to correct the possible phase mismatches among different sampling channels. By incorporating the DLC, the CDR benefits from the digital implementation of the loop filter which reduces the area while providing flexibility in terms of parameter adjustments to meet certain specs.

The packaging of the CDR was another challenging part which necessitated a custom design. To provide the required fan-out for the high number of the pins a silicone interposer was designed and fabricated in Tyndall's in-house silicon fab. The technology used is a 1.2 μm CMOS process. After the fabrication the interposer was tested to ensure high speed signal integrity.

Extensive measurements have been performed to validate the operation of the CDR and also the DPC, as a standalone chip, which are fabricated in 65-nm CMOS technology. Employing a 14-GHz quadrature reference clock, the DPC achieves DNL/INL of 0.7/6 LSB respectively while consuming 40.5 mW power from a 1.05 V supply. Although the CDR was able to recover the data for NRZ input at 25-GBd input, it struggled to function for the PAM4 input. The diagnostic methods suggested a few failure mechanisms which are covered in Chapter 4. To demystify the actual cause however, it may require additional measurements especially with more chip samples. This was not possible due the limited time during this project. Despite these issues, it was possible to come up with a "projected" performance for the CDR using NRZ test results and estimate its performance. The 1-UI JTOL bandwidth was around 2 MHz, with the loop bandwidth being around 20 MHz while $\text{BER} < 10^{-4}$. The power consumption is 236 mW which with a 50 Gb/s data rate translates to 4.27 pJ/bit of energy efficiency. Although our treatment of the subject targets a certain category of high speed CDRs, the proposed techniques can be effective in other applications

[67] as well.

5.2 Future Works

The correct plan for the future works may be initiated first by the testing of additional CDR chips available from the first fabrication. This would demystify any failure, that might be caused by packaging/assembling. The packaging can cause bandwidth limitation due the long wire bonding which in return triggers signal integrity issues mainly at the high speed input data lines.

Our experience with the CDR measurements showed the importance of having properly functional auxiliary modules to test the chip's building blocks by employing different methods. For example the operation of the AFE (and the entire input channel including the silicon interposer and packaging) can be easily monitored by using the calibration DAC in conjunction with the DPC. The main idea (similar to the eye-monitoring methods [68], [69]) is to scan the slicers input by using the DPC and calibration DACs. The DPC output would sweep the time interval in small steps while at every time instance the DAC would step up/down the slicers references to resolve the input amplitude. Although the current chip in its ideal form would allow us to perform such measurement, the problem with calibration DACs circuitry in setting the references and also the serial communication issues with the DACs input registers inhibited such approach. Therefore a proper verification of the testing blocks has to be considered prior to any chip re-spin.

In addition, the observations during lab validation suggest embedding of additional test circuitry inside the chip that can increase the measurement accuracy and reduce the costs by avoiding extensive and laborious test-beds. For example an on-chip BERT [70] can be implemented to measure the BER of the CDR directly.

The benefit of having DFE function built-in around the slicers can be substantial in terms of enhancing the frequency response of the AFE and hence improving the BER results. There have been extensive researches in the area the DFEs for PAM4 [71], [72], [73], [74] which can be incorporated in the future version of the design.

The other design improvement could be achieved by merging the S/H network (the salve part) into the slicers' array and performing the sampling directly

through the comparators. To circumvent the kick-back noise issues, different architectures of comparators with pre-amplifier stages could be utilized.

Reconsidering the overall CDR's system level, a significant change could be made by the use of other PD architectures like the Mueller-Muller PD [75] as it allows baud-rate operation. This is beneficial in terms of saving power and achieving higher data rates while operating with the same sampling frequency.

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