CORA Cork Open Research Archive
Cartlann Taighde Oscailte Chorcaí

Title	Design principles for maximizing photovoltage in metal-oxide-protected water-splitting photoanodes
Authors	Scheuermann, Andrew G.;Lawrence, John P.;Kemp, Kyle W.;Ito, T.;Walsh, Adrian;Chidsey, Christopher E. D.;Hurley, Paul K.;McIntyre, Paul C.
Publication date	2016-01-01
Original Citation	Scheuermann, Andrew G.; Lawrence, John P.; Kemp, Kyle W.; Ito, T.; Walsh, Adrian; Chidsey, Christopher E. D.; Hurley, Paul K.; McIntyre, Paul C. (2016) 'Design principles for maximizing photovoltage in metal-oxide-protected water-splitting photoanodes'. Nature Materials, 15, 99-105. doi: 10.1038/NMAT4451
Type of publication	Article (peer-reviewed)
Link to publisher's version	http://www.nature.com/nmat/journal/v15/n1/full/nmat4451.html - 10.1038/NMAT4451
Download date	2026-10-30 08:10:36
Item downloaded from	https://hdl.handle.net/10468/3339

UCC
University College Cork, Ireland
Coláiste na hOllscoile Corcaigh

Design Principles for Maximizing Photovoltage in Metal-Oxide-Protected Water-Splitting Photoanodes

Andrew G. Scheuermann,[a] John P. Lawrence,[a] Kyle W. Kemp,[a] T. Ito,[a,c] Adrian Walsh,[d] Christopher E.D. Chidsey,[b] Paul K. Hurley,[d] and Paul C. McIntyre*[a]

Supplementary Information

Materials and Methods

Silicon substrates

Heavily boron-doped (100) p-type silicon wafers (ρ=0.001-0.002 Ω·cm, thickness 505-545 μm) were used as conductive silicon substrates to study water oxidation in the dark. Moderately phosphorous-doped (100) n-type silicon wafers (ρ=0.14-0.24 Ω·cm, thickness 450 μm) were used for Type I MOS Schottky junction photoanodes. Buried junction devices were made with n-type silicon wafers and were subjected to a standard clean using a Semitool Spray Acid: first the wafers are subjected to ozone and DI water, then NH_4OH (2000:1) is added to help remove particles and organics, and lastly ozone, DI water, and HF (1150:1) are used to etch the chemical oxide and regenerate the surface oxide, also removing any metallic species. The implant is performed with a 4 x 10^{15} cm^2 dose of boron at 15keV. Following the implantation, the samples were annealed at 950°C for 40 minutes. The junction depth was characterized in two ways. First the surface was bevelled at a known angle through the p^+ surface region and the nSi was stained allowing for an optical measurement to determine the depth. This resulted in a calculated depth of 448 nm. Secondly, the p^+ region was preferentially etched using a HNO_3:HF solution and scanning electron microscopy (SEM) was utilized to directly measure a junction depth of ~460 nm.

Wafer Clean and Slot-Plane Antenna (SPA) Oxidation of SiO_2

Before SiO_2 growth, prime grade Si (100) wafers were prepared using a three part clean: 10 minutes at 50°C in 5:1:1 H_2O:H_2O_2:NH_4OH to remove trace organics, 10 minutes at 50°C in 5:1:1 H_2O:H_2O_2:HCl to remove trace metal ions, and then 30 seconds in 2% HF to remove the silicon dioxide layer. Lastly the substrates were spun dry leaving a hydrogen passivated silicon surface for plasma oxide growth. Next the SiO_2 layer is regrown with precise thickness control using the slot plane antenna (SPA) method. A 2.45 GHz microwave is used to generate a uniform high density plasma below the dielectric shower plate with a diameter exceeding 30 cm, capable of uniformly covering large wafers. The deposition temperature was set to 500°C for an actual substrate temperature of approximately 400°C and allowed to equilibrate while argon was purged through the chamber at 100 scccm. Then the argon flow rate was increased to 1500 sccm and oxygen gas was introduced at 400 sccm for 10 seconds. Finally the argon flow was set to 1200 sccm and oxygen held at 40 sccm for 25 seconds at a process pressure of 5 Torr. The microwave power was set to 3000 W and held for the duration of the growth time. After the microwave power is shut off, argon and nitrogen are allowed to flow for an additional 3 seconds to conclude the process. This process was optimized for the thinnest possible oxides; decreasing the process time to 3 to 5 seconds results in depositions around 15 Å in thickness, the approximate minimum for this method. By extending the run length, films of over 100 Å can be grown but they require increasingly long deposition times. More details can be found in previously published work [1].

Atomic Layer Deposition (ALD) of TiO_2

Titanium dioxide layers were deposited by a custom home-built ALD instrument with tetrakis(dimethylamido)titanium (TDMAT) as the metal precursor and water as the oxidant. The

bubbler is kept at 70°C and a gradient is maintained between the bubbler and chamber reaching 120°C at the inlet. The substrate temperature was approximately 170°C for all deposition in accordance with the ALD window reported previously, the TDMAT was pulse time was 0.7s and the H_2O pulse time was 0.5s [2]. The equilibrium purge pressure was approximately 600mTorr. These depositions had stable growth rates of ~0.6Å/cycle over the thickness ranges studied. Details of the ALD system and process have been published previously [3].

Deposition of catalyst and back-contact

Iridium metal catalysts and platinum and aluminium back-contact metals were deposited by electron beam evaporation. The surface catalyst was a 2 nm layer of iridium for all water splitting cells. Previous work has shown that even with these very thin layers, the catalyst is uniform in thickness [4]. MOS capacitors for solid-state analysis had 50 nm or Ir to allow for effective probing of the metal gate. All p^+Si samples had a back-side contact of 20 nm of e-beam Pt deposited and n-Si samples had an e-beam deposited 100 nm Al backside contact to provide an Ohmic contact.

Aqueous solution preparation

As in previous work [1-4], aqueous solutions of pH 0, 7, and 14 were prepared to study performance across the pH range. Solutions were 1 M H_2SO_4, 1 M NaH_2PO_4/Na_2HPO_4 buffer, and 1 M NaOH respectively. All solutions were prepared with MilliQ water and checked against both a bench top glass pH electrode and the reversible hydrogen potential using Pt electrodes. Solution resistance values of 4.3 Ω, 40.0 Ω, and 11.2 Ω for the pH 0, 7, 14 solutions, respectively were used from EIS analysis. All water oxidation overpotential results are corrected by subtracting the product of the measured current and the series resistance from the applied voltage: E_{corr} =

$E_{\text{applied}} - iR_{\text{series}}$. The plotted water oxidation curves are the raw data, not corrected.

Ferri/ferrocyanide preparation

The reversible redox couple ferri/ferrocyanide was prepared to study electronic carrier transport in these anodes. Potassium ferricyanide and potassium ferrocyanide trihydrate were used to make a 1:1 solution containing 10 mM of each species with 1M potassium chloride. MilliQ water was used for these solutions.

Cyclic voltammetry

Electrochemical measurements were carried out using a glass frit isolated Ag/AgCl/saturated KCl reference electrode and a platinum wire counter electrode, as detailed by Chen et al. [4]. The active area of 0.196 cm^2 was defined by a bored Teflon cone pressed down onto the nano-layered anode. All ferri/ferrocyanide CV's were measured at a scan rate of 100 mV/s in a static solution. A peristaltic pump was used during water oxidation to circulate the solution at 1 mL/s; water oxidation current vs. potential data were also collected at a scan rate of 100 mV/s.

MOS capacitor fabrication and capacitance analysis

MOS capacitors were fabricated using stencil lithography. Various gate metals were deposited through a shadow mask defining circular capacitors of diameters ranging from 100 to 250 μm and thicknesses of 50 nm on n-Si. Measurements were taken at room temperature. Scans were taken sweeping from depletion to accumulation with a superimposed 50 mV AC voltage to measure the capacitance between 1 kHz and 1 MHz.

Sentaurus Modeling

Device simulations were performed using Synopsys Sentaurus (Version I-2013.12-SP1). Default material properties, found within the software, were used for both silicon and SiO_2. Doping densities and junction depths were set to the material values reported in the main body of the manuscript and supplementary for the silicon actually used. The material TiO_2 is not found within the Sentaurus default material database and therefore its material properties were added manually. Moderate n type doping of 1×10^{17} cm^{-3} was assumed. For the TiO_2 band structure we assumed an electron affinity of 4.2 eV [5] relative to vacuum and a bandgap of 3.2 eV [6]. Optical constants for TiO_2 were incorporated over the desired spectral range from previous literature values [7]. The default Sentaurus parameters were used for the Shockley-Read-Hall lifetimes of 10 μs and 3 μs for electrons and holes respectively. The front and back contact metals were iridium and aluminum respectively again reflecting the actual devices fabricated in this study. Modelling of the electrodes consisted of defining the work functions of each contact. We assumed a work function of 5.1 eV and 4.1 eV for iridium and aluminum respectively based on ranges for values of 5.0-5.67 eV and 4.06-4.26 reported in the literature [8]. Surface recombination velocities of 2.57×10^6 cm/s and 1.93×10^6 cm/s were assumed for electrons and holes respectively at the iridium-TiO_2 interface. This interface is modeled using the Schottky contact physics model built into Synopsys Sentaurus. For all materials we assume the presence of both SRH and radiative recombination defined by the models present in the Synopsys Sentaurus™ Device User Guide using the specified material properties listed above and those included as default parameters in Synopsys Sentaurus material database. Optical generation was modelled using the Transfer Matrix Method (TMM) using a representative version of the AM1.5G spectrum. Description of optical generation models used by Sentaurus can be found within the Sentaurus™ Device User Guide.

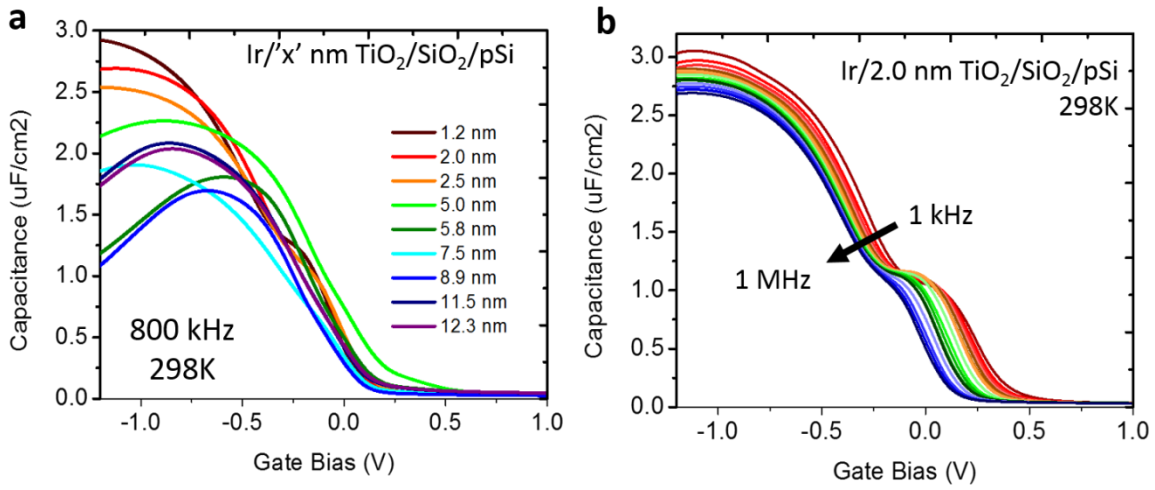


Figure S1 | Photovoltage loss is not due to fixed charge in the insulator. (A) Collection of the 800 kHz CV curves measured in the dark as a function of TiO_2 thickness showing that the flat band voltage is reasonable and does not vary systematically with TiO_2 thickness. The photovoltage loss observed in Figure 2 would require a positive fixed charge, moving the device from inversion to accumulation at zero bias. Charges in insulator layers can be probed by measuring the flat band voltage of MOS capacitors as a function of insulator thickness. In particular, an increasing oxide thickness decreases the oxide capacitance density C_{ox}. If bulk charge density per unit volume, Q_{bulk}, is present, there will be a parabolic relationship between the flat band voltage, V_{fb}, and oxide thickness, t_{ox}, according to equation (S1), where Φ_{metal} is the metal work function, Φ_{Semi} is the silicon Fermi level, and Q_{int} is the interface charge per unit area:

$$V_{fb} = \Phi_{Metal} - \Phi_{Semi} - \frac{Q_{int}}{C_{ox}} - \frac{Q_{bulk} t_{ox}}{2C_{ox}} \qquad (S1)$$

p-type silicon is chosen over n-type silicon for this analysis because the lower leakage current allows for more robust characterization of any shift in flat band voltage. The valence band offset

(VBO) and conduction band offset (CBO) for silicon to titanium dioxide, are 2.56 eV and -0.4 eV, respectively [9-10]. These offsets are responsible for the lower leakage currents obtained from pSi compared to nSi capacitors, despite relatively high, trap-mediated hole currents in TiO_2. As can be clearly seen above, no shift with thickness is observed that could explain the 0.5 to 1V shift in inferred photovoltages. The ALD-TiO_2 layers in this pSi MIS study were deposited side to side with the layers measured for nSi photovoltage loss to ensure consistency. In addition to no thickness-dependence of the flat band voltage, the absolute value is reasonable. Given a p-type doping between 1e15 cm^{-3} and 1e16 cm^{-3} the silicon Fermi level lies between ~4.9 and 5.0 eV. The flat band voltage extracted from these devices around 0 V would suggest an iridium work function of similar value, ~5eV, without any charge component which is reasonable. Since the iridium work function can vary, small charge components are possible, but they are small and not correlated with oxide thickness. **(B)** A multi-frequency capacitance voltage measurement of a 50 nm Ir / 2.0 nm TiO_2 / SiO_2 / p-type Si MOS capacitor showing reasonable dispersion as a result of reasonably low leakage current densities.

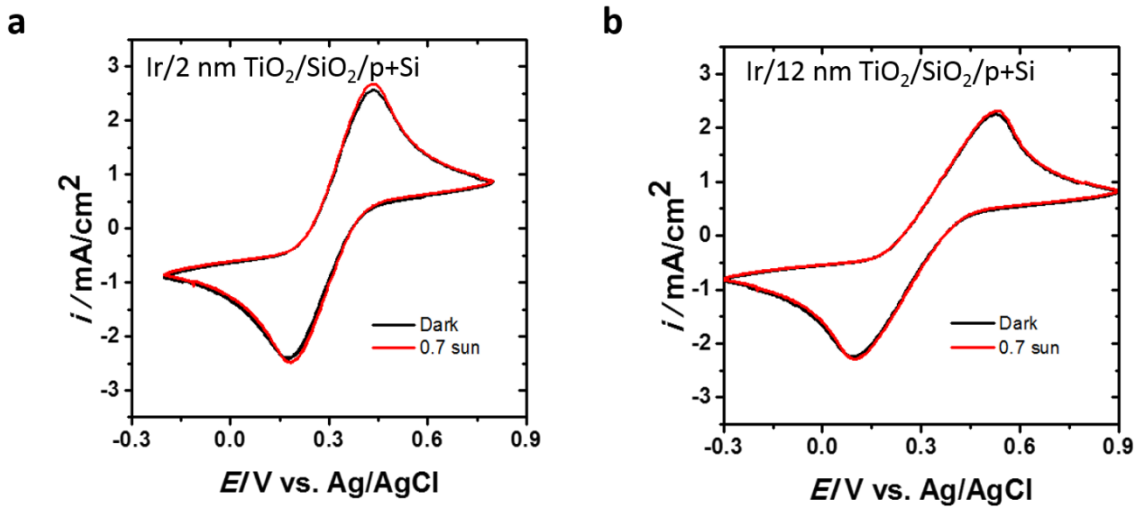


Figure S2 | Photovoltage loss is not due to charging under illumination. (A) 2 nm of ALD-TiO_2 and **(B)** 12 nm of ALD-TiO_2 protecting degenerately doped p^+Si anodes for electrochemistry in ferri/ferrocyanide solution. For both thin and thick films, electrochemistry is performed in the dark and under 0.7 sun illumination. The resulting traces are identical, showing that illumination does not lead to detectable charging of the protection layer. This experiment further shows that calculating the photovoltage in Type I and Type II cells vs the ferri/ferrocyanide reversible redox potential of ~0.3 V vs Ag/AgCl will give the correct value.

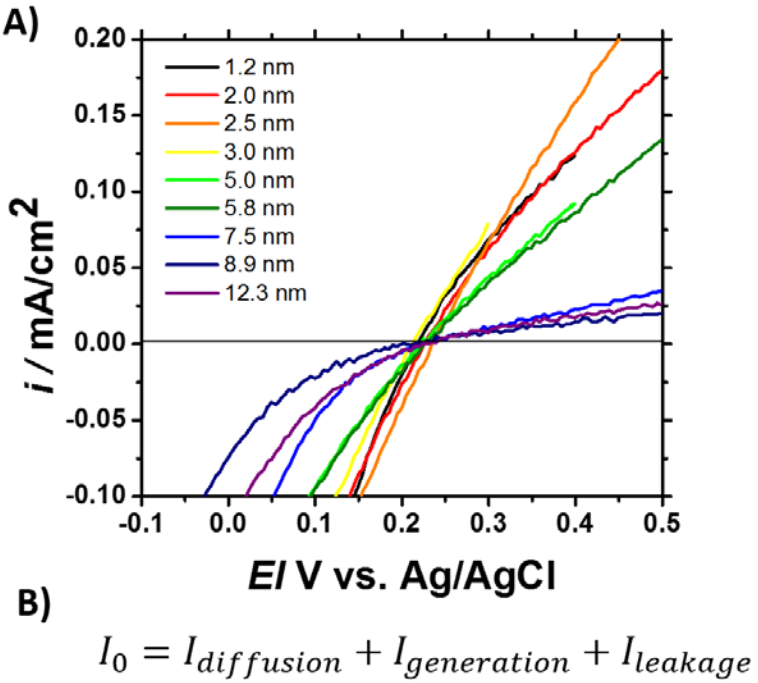


Figure S3 | Photovoltage loss is not due to SRH recombination. (A) The dark current of Type I MIS photoanodes with structure Ir / 'x' nm TiO_2 / SiO_2 / nSi for each thickness. As can be seen, the reverse dark current at positive bias, and at values above the zero current point (~0.2 V vs Ag/AgCl), decreases with thickness. Thus there is no evidence of an increasing density of recombination centers. **(B)** The reverse current is made up of three components; $I_{diffusion}$ based on the band bending, which is not changing; $I_{generation}$ due to recombination-generation (R-G) centers; and $I_{leakage}$ which includes all non-idealities that may lead to Ohmic-type leakage current. In reference to (A), the current appears Ohmic not saturating, showing a strong leakage current as previously shown for these devices and there is no evidence, nor any reason, to expect an increase in R-G centers as a function of TiO_2 thickness. Since voltages as high as 500 – 550 mV are achieved for the thinnest TiO_2 layers, this leakage current does not appear to be detrimental to voltage as a thermal generation current from R-G centers would be.

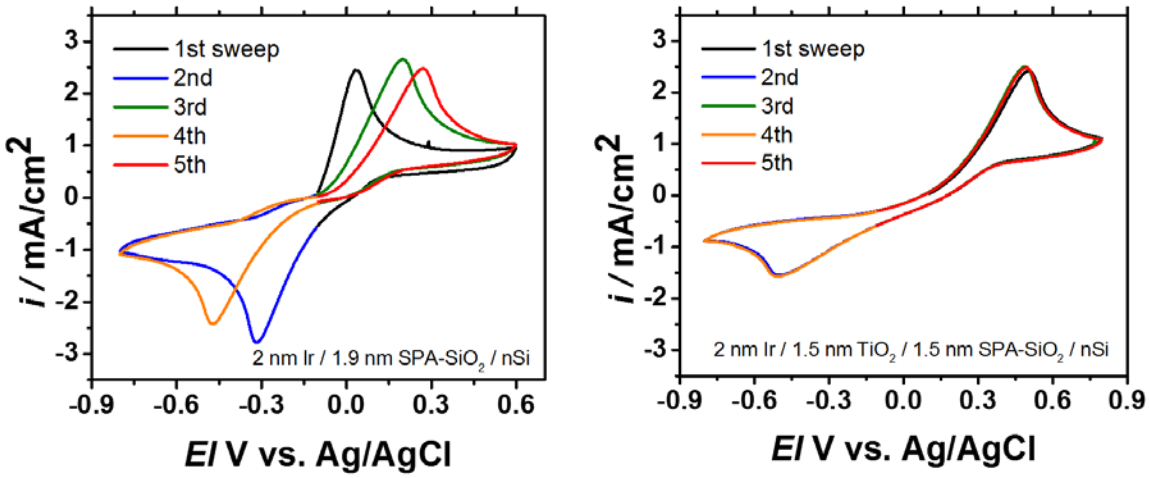


Figure S4 | Samples without ALD-TiO_2 are not stable introducing possible measurement error. Left – 2 nm Ir / 1.9 nm SPA-SiO_2 / nSi photoanode and Right – 2 nm / 1.5 nm TiO_2 / 1.5 nm SPA-SiO_2 / nSi photoanode both measured under 1 sun of AM 1.5 illumination in 10 mM / 10 mM ferri/ferrocyanide 1M KCl at a scan rate of 100 mV/s, surface area 0.196 cm^2. The anode without TiO_2 protection is highly unstable with the peaks expanding with each subsequent sweep indicating that the DC resistance of the sample is increasing. The photovoltage measured from the $E_{1/2}$ position and referenced to the p^+ Si sample at 295 mV vs Ag/AgCl moves from 436 mV to 433 mV between the 1^{st}-2^{nd} and 3^{rd}-4^{th} sweep. The anode with TiO_2 protection shows a consistent peak-to-peak splitting and $E_{1/2}$ position consistent with the greatly enhanced stability afforded by the TiO_2. The instability shown here without TiO_2 is particularly acute for the thinnest SiO_2 layers and thus the reported photovoltage may be subject to error although the magnitude of that error is within a couple percent for the first 5 sweeps shown here.

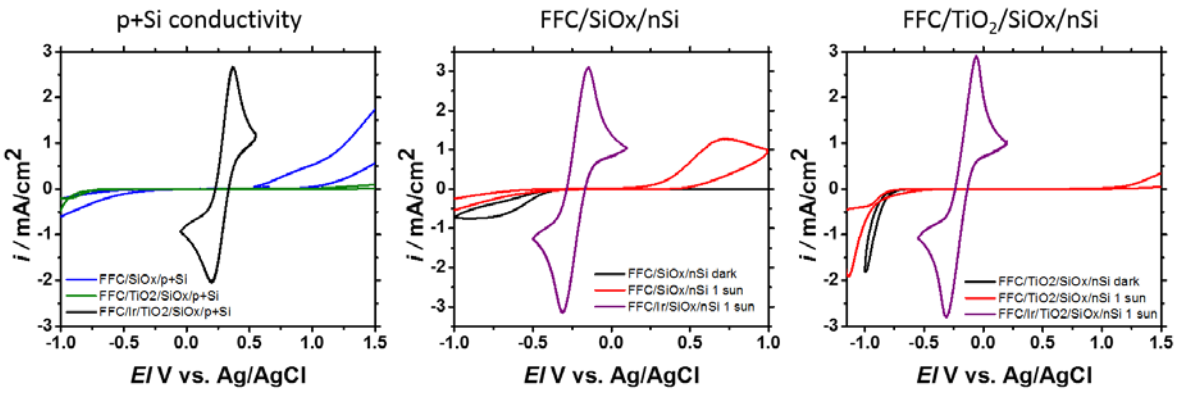


Figure S5 | Type 0 silicon cells show no meaningful photovoltage. Cyclic voltammetry of Type 0 photoelectrochemical cells show first with the p^+Si conductivity measurement that removing the iridium catalyst (black with iridium) removes essentially all of the meaningful conductivity in the oxide bilayer cell (green) and drastically increases charge transfer resistance even for just a thin SiOx layer of presumably ~1.3 nm when the measurement begins (blue). Most of the successful Type 0 cells to date have incorporated schemes that allow the electrolyte to directly contact the semiconductor in some schemes even permanently attaching the first layer of redox molecules to ensure a good electrical connection. This shows how easily even a very thin oxide layer disrupts the charge transfer in Type 0 cells. This paper shows how resistive insulators placed inside the junction create a charge extraction barrier. The low density of states contact in Type 0 cells resulting in poor charge transfer even in the reference p^+Si device with a high hole interface density on the insulators serves only to exacerbate this problem. The ferri/ferrocyanide couple should be capable of providing a sufficient built-in field with n-type Si. As shown in the p^+Si conductivity measurement, ferri/ferrocyanide has a reversible redox potential of ~ 0.3 V vs Ag/AgCl or about 0.5 V vs NHE, which is approximately 5 V vs the vacuum level, given that the SHE absolute voltage vs vacuum is approximately 4.5 V [11]. For n-type silicon with a Fermi level of ~ 4.25 eV, this indicates the existence of a built-in voltage of up to 0.75 V at an nSi-ferri/ferrocyanide

electrochemical junction. In the case of FFC/SiO_x/nSi (middle) and especially FFC/2 nm TiO_2/SiO_x/nSi (right), negligible current is measured at small bias, indicating that essentially all of the photogenerated carriers recombine before being extracted from the device. There is only a slightly increased current at larger applied bias, several hundred millivolts in the SiO_2-only case and over a volt in the TiO_2/SiO_2 case, where the applied voltage is finally capable of driving some of the photogenerated minority carriers out of the device before they recombine. This is in contrast to the result when adding a thin 2 nm metal layer (purple) that facilitates charge transfer. The Type 1 samples derive their voltage from the MIS junction and the charge transfer is sufficient with the very thin oxide layers that a large interface hole accumulation is not necessary to extract charge. In the Type 0 case, even with a high interface hole density, the low density of states contact prevents efficient charge extraction across the insulators and out of the device.

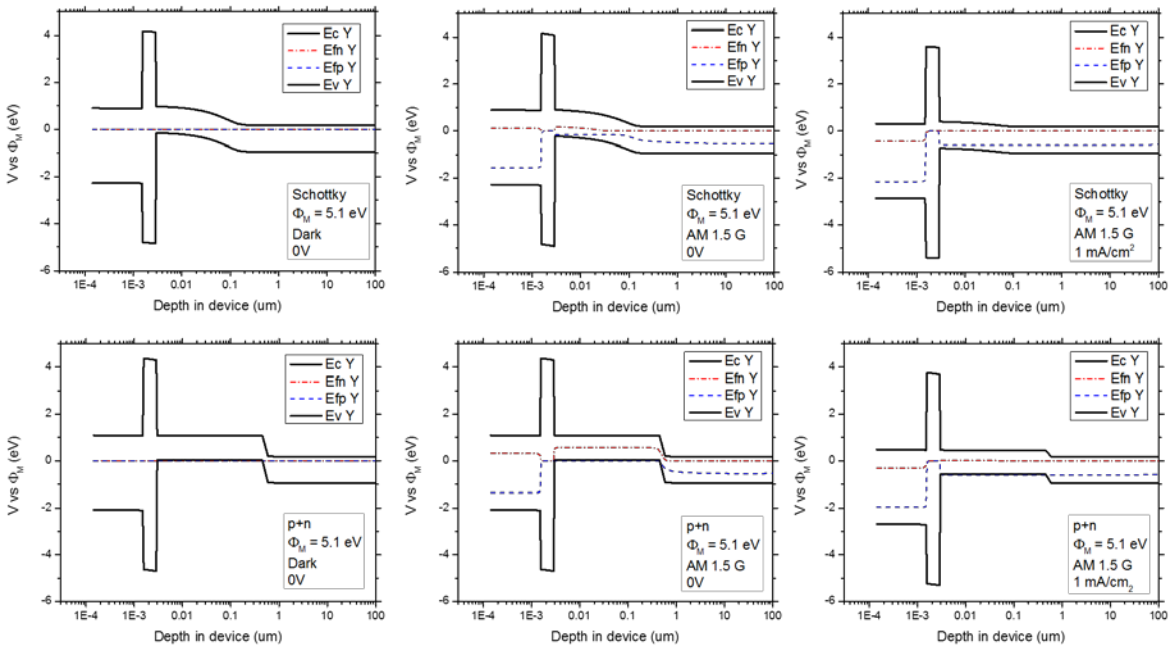


Figure S6 | Band diagrams of Type 1 Schottky and Type 2 p+n junctions under various conditions These band diagrams are for the Type I MIS n-Si anode in the top row and the Type II MIS buried p^+nSi anode on the bottom row. The far right viewgraphs for both junctions here are the same as those in Figure 6 in the main text without the layouts. The far left viewgraphs show the band bending in the dark with no applied bias, and in the middle under illumination with no applied bias. As can be seen on the bottom row, the quasi hole Fermi level is always at the valence band at the interface for the buried junction device. The Type 1 nSi device displays an inversion layer as a result of the iridium-nSi junction, but its depth is markedly less than that of the p^+n junction. The hole concentration at the interface of the illuminated Type 1 nSi structure with surface inversion decreases under the effect of applied bias while that of the Type 2 p^+n structure remains essentially constant. The observation that the photovoltage decreases in the case of the nSi photoanode despite the presence of a hole inversion layer, indicates that surface inversion induced by the metal to semiconductor work function difference is not sufficient to

eliminate the dependence of the photovoltage on the TiO_2 thickness. All band diagrams were generated by Sentaurus modeling and are plotted against the depth in the device in microns on the x-axis and voltage referenced to the metal work function on the y-axis. The iridium work function is taken to be 5.1 eV in this analysis. All materials properties are those of the actual materials used in this study.

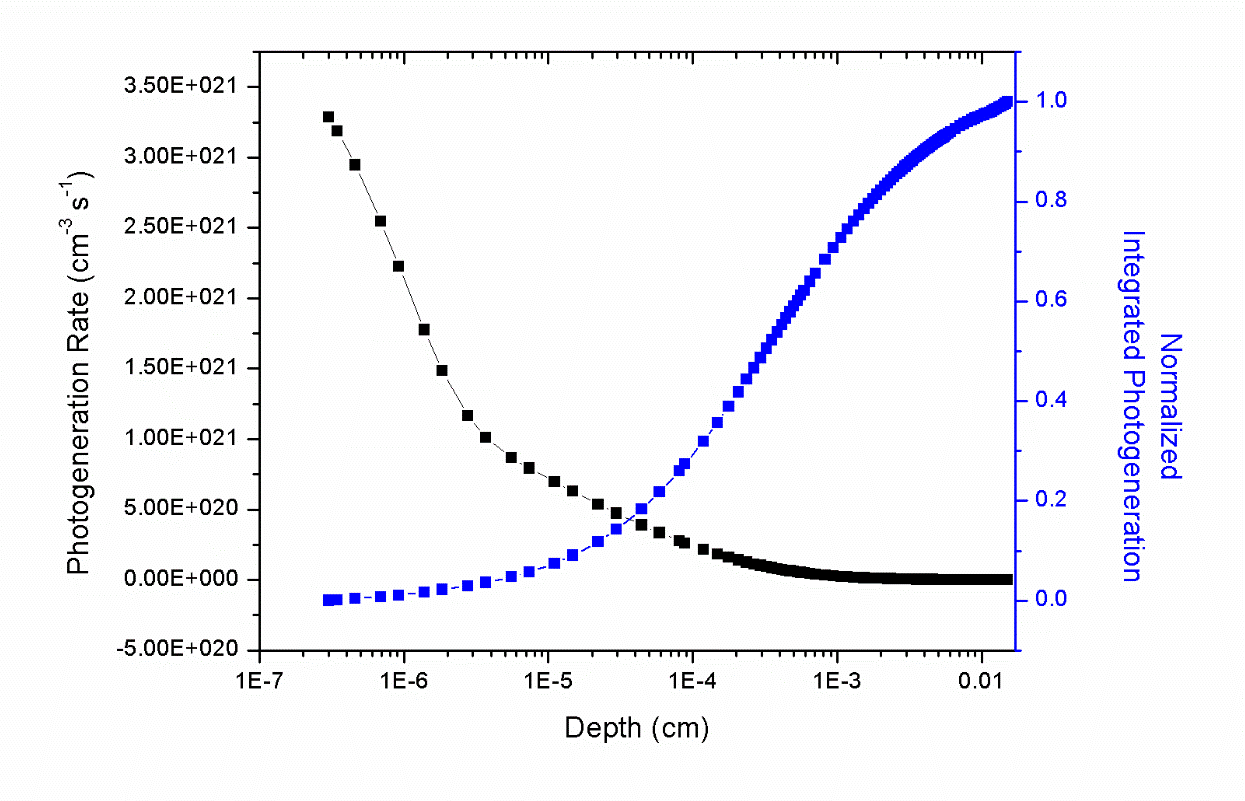


Figure S7 | Photogeneration rate and integrated photogeneration from Sentaurus simulations. The photogeneration (black) is plotted as a function of the depth in the Type 1 and Type 2 MIS structures. The integrated photogeneration is shown here on a normalized scale (blue). This plot shows that about 30% of the photogeneration occurs within the first micron of the silicon sample. While placing the p^+n junction deeper could further decouple interface hole density from current flow and illumination conditions, it is important to ensure that the junction depth is less than the minority carrier diffusion length of heavily boron doped silicon, which is around 1 μm. These competing considerations were used to select the junction depth of around 0.45um.

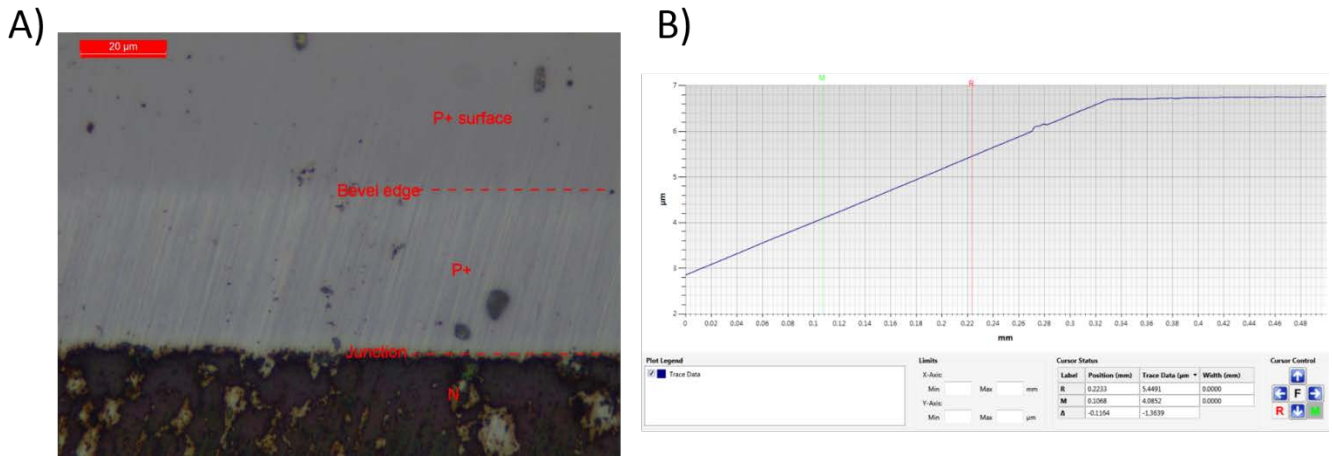


Figure S8 | Junction depth by bevel analysis. Bevel analysis of the p^+ surface region for buried junction depth. A) -- A staining solution is applied to the beveled surface plating the underlying nSi. B) – From the surface profiler the angle of sin θ = 0.0112 and the hypotenuse of 40.0 µm are determined for a calculated junction depth of 0.448 µm.

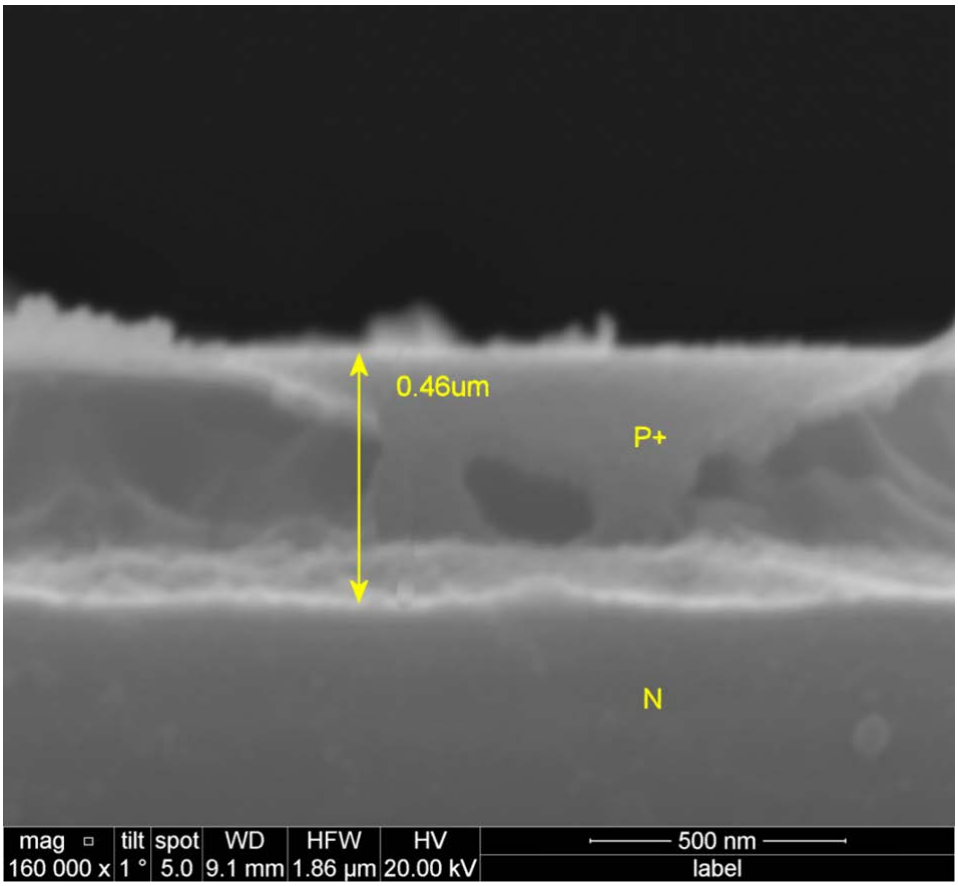


Figure S9 | Junction depth by SEM analysis. SEM analysis of the p^+ surface region for buried junction depth. The wafers were mechanically polished at 90º followed by FIB cleaning sweep to remove artifacts. Then a HNO_3: HF solution is applied to etch the more heavily doped side of junction allowing for the optical determination of the depth by scanning electron microscopy (SEM). A junction depth of approximately 0.46 µm is measured.

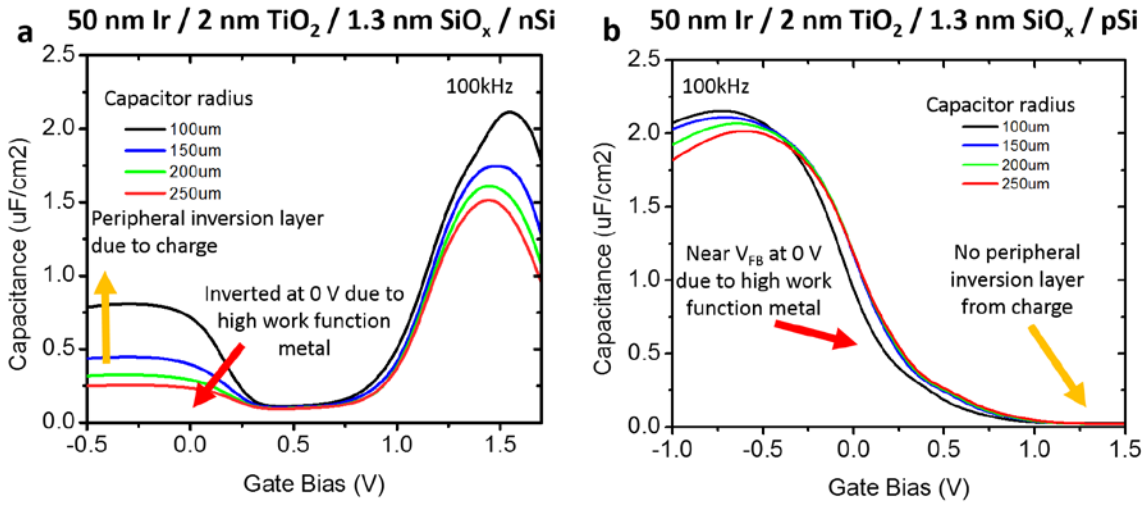


Figure S10 | Capacitance voltage analysis reveals a hole inversion layer in n-type devices. Capacitance voltage analysis in the dark on n-type and p-type Si reveals the presence of a hole inversion layer in the n-type devices. Inversion refers to the situation where the minority carrier population exceeds that of the majority carrier. Ideally, surface inversion occurs when the applied bias causes the Fermi level to pass the mid-gap position and come to an opposite position, about the mid-gap, from the flat band Fermi level position, which is set by the doping. When at such a bias, for example 0 V for the nSi devices above, inversion will still only be typically observed in CV analysis at AC probe frequencies less than 100 Hz allowing minority carrier generation to follow the AC signal. At frequencies above this, for example the 100 kHz used here, no inversion response is typically observed leading to a flat CV curve. Inversion is also illumination dependent [12], so measuring under light will produce a frequency dependent inversion response. These measurements, however, are performed in the dark and do show an inversion response in the nSi near 0 V due to the high work function metal, but also edge effects often called peripheral inversion. The red arrow indicates the fact that the high work function metal causes the nSi to be in the DC inversion bias regime at zero applied bias. The p-type devices should accordingly be

near the flat band condition with a high work function metal at zero applied bias. Thus all of the n-type silicon surface covered by metal will be inverted at 0 V for Type 1 devices. Although this inversion is not typically probed at high AC frequency, it still affects the DC operation of the device. Secondly, there is an inversion capacitance-voltage response (yellow arrows) shown in the nSi devices (left) but not pSi devices (right) in the dark even at very high AC measurement frequencies such as the 100 kHz frequency used for these curves. This inversion response is still observed (although at lower magnitude) even at 1 MHz. This type of inversion is sometimes called peripheral inversion [13] because it is due to minority carriers in the surrounding non-metal-coated material drifting under the gate. The magnitude of that inversion response increases as the gate size decreases since minority carriers have a further distance to travel from the edge to the center of the capacitor in the time dictated by the ac signal frequency. The other key characteristic of peripheral inversion is its presence in one doping type and absence in the other. Without a metal present, the inversion must be caused by either positive or negative charge affecting either p-type or n-type semiconductors, but not both. In this case, that charge is negative. Importantly, while a negative charge would not cause peripheral inversion in p-type capacitors, significant charge under a metal gate would still shift the flat band voltage as probed in S1 previously. For these samples as well, no significant shift in flat band voltage was observed. This can be found by comparing the Fermi levels and flat band voltages of the nSi and pSi MIS capacitors with the same insulators. Assuming no charge component, both the nSi and pSi flat band voltages correspond with metal catalyst work functions around 5.1 – 5.3 eV considering the Fermi levels of 4.25 eV and 5.0 eV of the two device types respectively. This agrees well with the range of work functions reported for iridium as well as those measured previously for these types of devices. Similar to S1, this shows that the flat band voltage is predominantly set by the metal-semiconductor Schottky junction and

not fixed charge and that the fixed charge does not correlate with oxide thickness. Further, the effect of any peripheral charge should be negligible in these studies as blanket metal films are used ensuring the surface is inverted everywhere from the presence of the metal – the metal diameter of the electrochemical pads is two orders of magnitude larger than the largest diode measured here (red curve). Despite the inversion induced by the high workfunction metal, the illuminated Type I device does not maintain the high hole density on the interface with increasing bias as shown in S6 and accordingly experiences a photovoltage loss as compared to Type 2 p^+n devices.

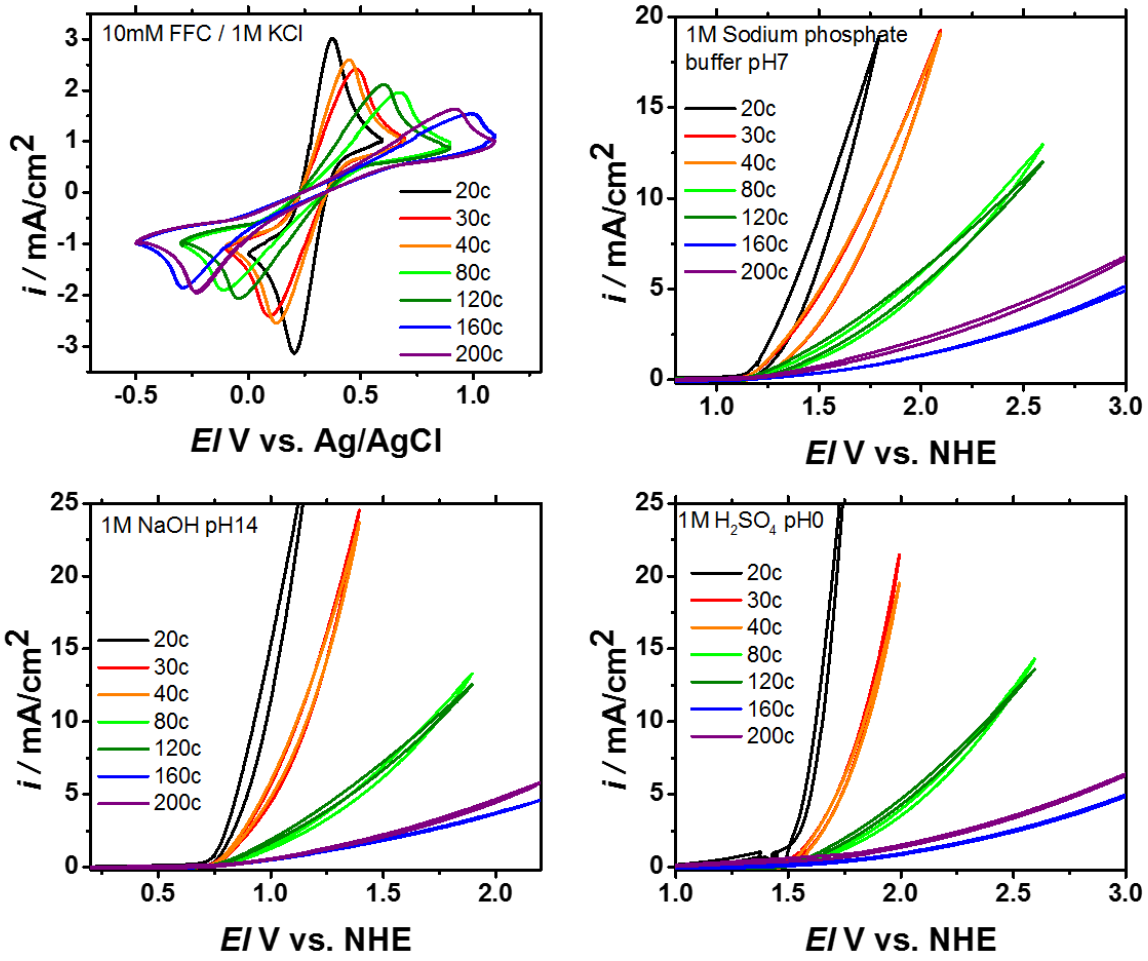


Figure S11 | Cyclic voltammograms for p+Si reference cells Electrochemical results taken in the dark for 2 nm Ir / 'x' cycles of ALD-TiO_2 / ~1.3 nm SiO_2 / p^+Si. The growth rate was approximately 0.4 - 0.5 Å/cycle. The scaling of the DC resistance in the ferri/ferrocyanide cyclic voltammograms corresponds with the overpotential loss in pH 0, 7, and 14 as previously reported.

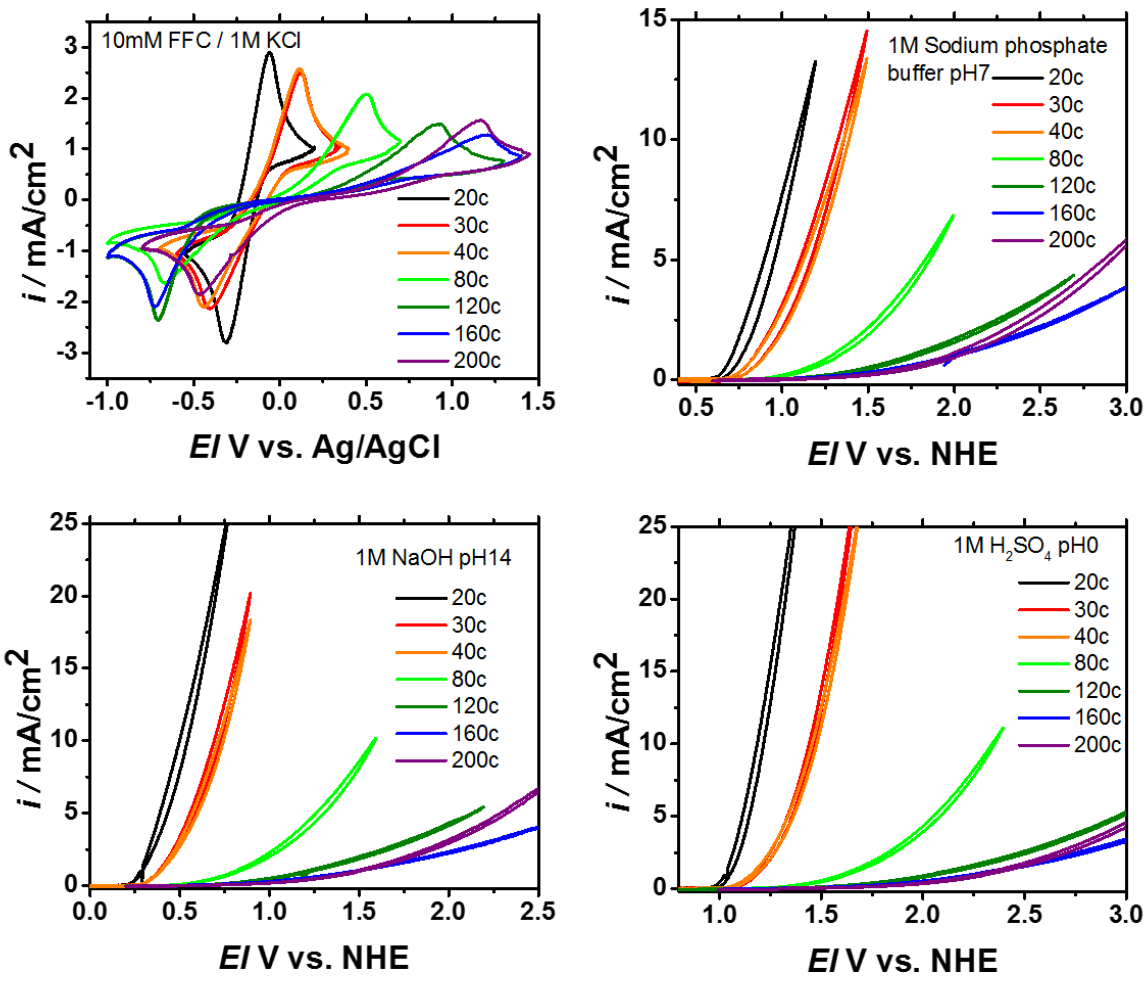


Figure S12 | Cyclic voltammograms for Type I MIS nSi cells. Electrochemical results taken under 1 sun of AM 1.5 illumination for 2 nm Ir / 'x' cycles of ALD-TiO_2 / ~1.3 nm SiO_2 / nSi Schottky junction structure in 10 mM ferri/ferrocyanide in 1M KCl and in pH 14 solution, 1M NaOH, pH 7 solution, 1M sodium phosphate buffer, and pH0 solution, 1M H_2SO_4.

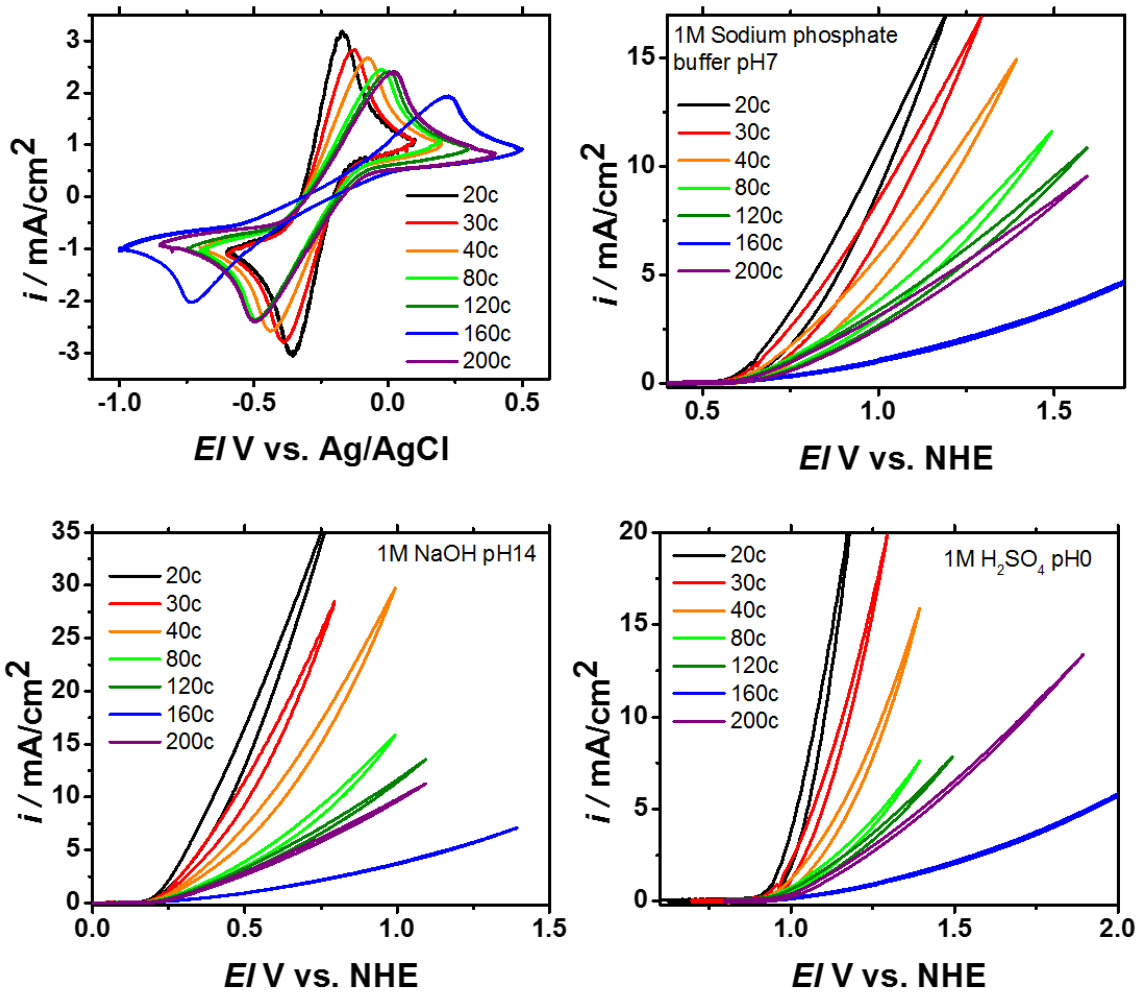
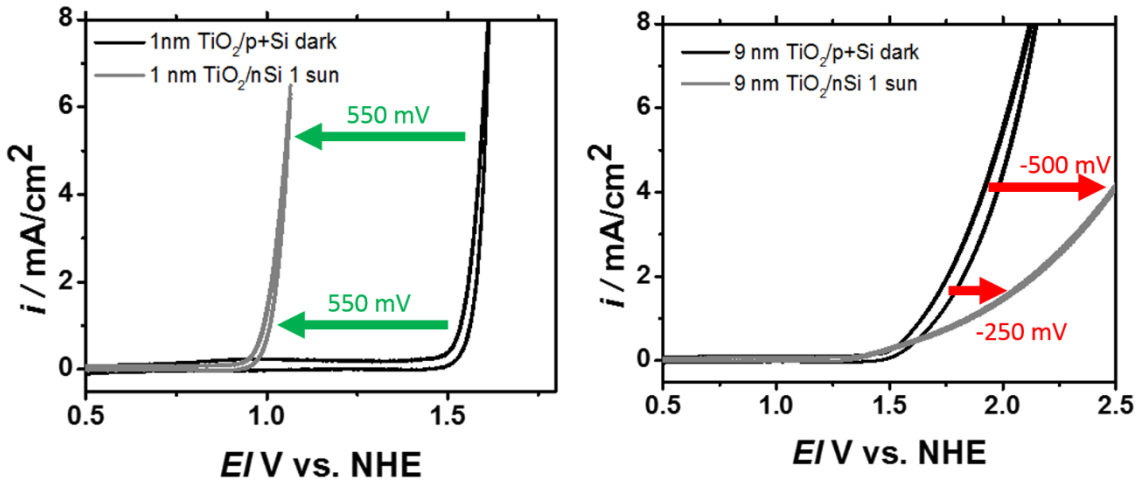


Figure S13 | Cyclic voltammograms for Type 2 p+n buried junction cells. Electrochemical results taken under 1 sun of AM 1.5 illumination for 2 nm Ir / 'x' cycles of ALD-TiO_2 / ~1.3 nm SiO_2 / p^+nSi buried junction structure in 10 mM ferri/ferrocyanide in 1M KCl and in pH 14 solution, 1M NaOH, pH 7 solution, 1M sodium phosphate buffer, and pH0 solution, 1M H_2SO_4.

S14 | Detail on photovoltage calculations. The photovoltage is calculated as the shift between the p^+Si reference and photoanode at a given current density. Our work has typically chosen 1 mA/cm^2 to represent a typical turn-on current. Other works often use $10mA/cm^2$ as a good approximation of the desired max power point. In practice, the performance of the integrated device (particularly taking into account current matching requirements in tandem structures) will dictate the max power point and therefore the most relevant current density at which to measure photovoltage of the half cell. Measuring photovoltage at higher current densities is valuable because it is a better predictor of the ultimate efficiency of the device than an open circuit voltage. However, it can be hard to compare between reports that chose different current values and may have different reference points. The figure below shows that when the TiO_2 is very conductive (left) the shift is constant at all current densities, but when the TiO_2 is thicker in the Type I nSi cell, there is a photovoltage loss associated with recombination leading to a "photovoltage shift" that is a function of current. Here, since the reference does not experience this loss, the shift is worse with higher current. This loss has been the main subject of this paper.



Since this paper focuses mainly on voltage and eliminating charge extraction barriers, as opposed to overall series resistance, it is perhaps most appropriate to pick a low current photovoltage

approximating the open circuit voltage for comparison, although the theory should hold true for any arbitrary chosen current density. It is important to note that since the fill factor is always less than one, any photovoltage choice at positive current is always less than the open circuit voltage by incorporating conductivity losses. Focusing on the zero current voltage is more general and not subject to any current dependence as encountered above. The photovoltage at zero current (the open circuit photovoltage) is calculated in three ways. In ferri/ferrocyanide solution, it is calculated as the $E_{1/2}$, the average of the peak potentials for the photoanodes compared to the $Fe(CN)_6$ Nernstian cell potential, which is also the same as the $E_{1/2}$ value for the p^+Si anode measured in the dark. For the water oxidation curves, such a method is not possible since only the half reaction is studied. The shift can be taken at the lowest possible faradaic current density (above the capacitive current) or extrapolated to zero oxide resistance by fitting with typical kinetic models such as Butler-Volmer kinetics. Both of these methods have been performed for the values shown in S13 and in the main paper and produce the same results within 0.2% of the reported photovoltage-- typically < 2 mV--which is very good agreement and less than the expected error from the measurement itself.

Modeling with a Butler-Volmer (B-V) model is performed as follows:

The typical B-V equation is modified to include relevant terms for this device stack E_{OC}, the open circuit voltage, $E_{applied}$, the voltage applied by the potentiostat, $E_{H2O/O2}$, the thermodynamic potential of water oxidation, η_{Ir}, the turn on overpotential required for the iridium catalyst, and E_{gate}, the voltage dropped over the MOS gate structure. Typical values of η_{Ir} = 300 mV and i_0 = 6×10^{-9} A/cm^2 were used (6) and only the anode half reaction was considered:

$$i_{anode} = i_0 exp\left(\frac{-\alpha F(E_{OC}+E_{applied}- E_{H2O/O2}-\eta_{Ir}-E_{gate}}{RT}\right) \quad \text{(S2)}$$

For the p^+Si anodes measured in the dark, there is no open circuit voltage (Eoc) and the voltage dropped over the gate (Egate) is assumed only due to the series resistance of the oxide. So equation S2 can be simplified:

$$i_{anode} = i_0 exp\left(\frac{-\alpha F(E_{applied}- E_{\frac{H2O}{O2}}-\eta_{Ir}-i_{anode}R_{oxide}(i_{anode})}{RT}\right) \quad \text{(S3)}$$

As shown in equation S3, the voltage dropped across the gate is dependent on current (i.e. the effective resistance is current dependent). This is true for the photovoltage loss associated with recombination in Type I nSi MOS structures (increasing loss with higher current), but it is also true with the series resistance loss measured in the p^+ and p^+nSi structures i.e. the oxide is not a simple Ohmic resistor. This is to be expected from trap-mediating conduction in the TiO_2 in series with a tunneling process through SiO_2. As the Fermi level scans through the energies of the trap distribution, the tunneling probability is not constant. The resistances obtained in this way for a given current density agree quantitatively with those obtained by modeling ferri/ferrocyanide redox with commercial software (also based on B-V kinetics).

Equation S3 can be solved to resolve the functional form of R_{oxide} as a function of each ($E_{applied}$, i_{anode}) point in the cyclic voltammetry measurement. This makes the reasonable assumption that Butler-Volmer kinetics accurately describe the behavior of the photoanode under operation with only a varying R_{oxide} correction.

Finally, the point where $R_{oxide} = 0\ \Omega$ corresponds to the turn-on point where Butler Volmer kinetics describes the cyclic voltammograms without any device resistance. The results of the p^+Si simulation are fed into the p^+nSi and nSi result and iterated to converge on the open circuit voltage value that satisfies Butler Volmer kinetics.

S15 | Tabulated values of the photovoltages for Type 2 p^+nSi cells and Type 1 nSi cells. The open circuit voltage is measured as the shift of the $E_{1/2}$ value from the Nernstian potential of the $Fe(CN)_6$ redox couple for FFC. For water oxidation, the shift of the current onset is taken at the lowest possible current density above the noise, here ~ 0.2 mA/cm^2.

Table 1: Photovoltage values in FFC and during water oxidation for p^+nSi cells

TiO_2 thickness (nm)	FFC $E_{1/2}$ shift (mV)	Water oxidation onset shift pH = 0 (mV)	Water oxidation onset shift pH = 7 (mV)	Water oxidation onset shift pH = 14 (mV)
1	554	584	538	514
1.5	544	565	558	545
2	542	570	549	543
4	536	563.6	574	564
6	527	553	558	540
8	607	606	630	576
10	582	580	579	597

Table 2: Photovoltage values in FFC and during water oxidation for nSi cells

TiO_2 thickness (nm)	FFC $E_{1/2}$ shift (mV)*	Water oxidation onset shift pH = 0 (mV)*	Water oxidation onset shift pH = 7 (mV)*	Water oxidation onset shift pH = 14 (mV)*
1	472	510	491	463
1.5	427	407	433	429
2	447	425	443	439
4	364	164	195	202
6	165	-77	-60	-36
8	118	-74	-40	-54
10	-10	-259	-235	-185

*The photovoltage loss in FFC and water oxidation are different by a constant factor proportional to the IR_{series} loss since the water oxidation shift only accounts for the half reaction.

S16 | Derivation of Equation 4. The photovoltage loss ratio to inverse dielectric constant ratio relationship is derived from the parallel-plate capacitor model:

$$\Delta V = \frac{\Delta Q}{C} = \frac{\Delta Q}{\varepsilon_0 \varepsilon_i A} t_i \qquad (S4)$$

Where ΔV is the voltage loss required to charge the capacitor ΔQ, ε_i is the relative dielectric constant of the insulator, ε_0 the vacuum permittivity, A the plate area, and t_i the insulator thickness. The model is extended by considering changes in the two insulators (TiO_2/SiO_2) that make up the bilayer system:

$$V = \frac{Q}{C_{tot}} = Q\left(\frac{1}{C_{SiO2}} + \frac{1}{C_{TiO2}}\right) = \frac{Q}{\varepsilon_0 \varepsilon_{SiO2} A} t_{SiO2} + \frac{Q}{\varepsilon_0 \varepsilon_{TiO2} A} t_{TiO2} \qquad (S5)$$

Since we are able to independently vary the thicknesses of the two insulator layers and are measuring at a constant current density in all cases, we can take the partial derivate with respect to each insulator:

$$\frac{\partial V}{\partial t_{SiO2}} = \frac{Q}{\varepsilon_0 \varepsilon_{SiO2} A} \qquad (S6)$$

$$\frac{\partial V}{\partial t_{TiO2}} = \frac{Q}{\varepsilon_0 \varepsilon_{TiO2} A} \qquad (S7)$$

The ratio of equation S6 to equation S7 are taken, where the symbol *m* is used to denote the slope of the photovoltage with respect to thickness as also used in Figure 5-D. At the point t_{TiO2} = 1.5

nm and t_{SiO2} = 1.3 nm the two series share the same point—the same actual device--so the value of Q must be equal allowing it to be cancelled out and giving the photovoltage loss ratio for the bilayer structure (Equation 3 in the main text)

$$\frac{m_{SiO2}}{m_{TiO2}} = \frac{\varepsilon_{TiO2}}{\varepsilon_{SiO2}} \qquad (S8)$$

Works cited in supplementary

1) Scheuermann, A.G., Lu, D.Q., Ito, T., Chidsey, C.E.D., McIntyre. P.C. The effect of SPA-SiO_2 tunnel oxide thickness for metal-insulator-silicon photoelectrochemical cells. *ECS Transactions*, **64**, 265-276 (2014).
2) Scheuermann, A.G., Prange, J.D., Gunji, M., Chidsey, C.E.D., McIntyre, P.C. Effects of catalyst material and atomic layer deposited TiO_2 oxide thickness on the water oxidation performance of metal-insulator-silicon anodes. *Energy Environ. Sci.* **6**, 2487–2496 (2013).
3) Scheuermann, A.G., Lawrence, J.P., Gunji, M., Chidsey, C.E.D., McIntyre, P.C. ALD-TiO_2 preparation and characterization for metal-insulator-silicon photoelectrochemical applications. *ECS Transactions*. **58,** 75-86 (2013).
4) Chen, Y. W., Prange, J. D., Duehnen, S., Park, Y., Gunji, M., Chidsey, C. E. D., McIntyre, P. C. Atomic layer-deposited tunnel oxide stabilizes silicon photoanodes for water oxidation. *Nature Mat.* **10**, 539-544 (2011).
5) Fuke, N. *et al.* Influence of TiO_2/electrode interface on electron transport properties in back contact dye-sensitized solar cells. *Solar Energy Materials and Solar Cells* **93,** 720–724 (2009).
6) Pattantyus-Abraham, A. G. *et al.* Depleted-heterojunction colloidal quantum dot solar cells. *ACS Nano* **4,** 3374–3380 (2010).
7) Devore, J.R. Refractive index of rutile and sphalerite. *JOSA* **41**, 416-417 (1951).
8) *CRC Handbook of Chemistry and Physics* (eds. Haynes, W. M., Bruno, T. J. & Lide, D. R.) 95th edition, 12–124 (2014).
9) Perego, M., Seguini, G., Scarel, G., Fanciulli, M., Wallrapp, F. Energy band alignment at TiO_2/Si interface with various interlayers. *J. Appl. Phys.* **103**, 043509-043509 (2008).

10) Mönch, W. Interface-induced gap states and band-structure lineup at TiO_2 heterostructures and Schottky contacts. *J. Appl. Phys.* **107**, 013706 (2010).

11) IUPAC. Compendium of Chemical Terminology, 2 ed. (the “Gold Book”). Compiled by A. D. McNaught and A. Wilkinson. Blackwell Scientific Publications, Oxford (1997).

12) Turner, J. A., Manassen, J. & Nozik, A. J. Photoelectrochemistry with pSi electrodes: Effects of inversion. **37**, 488-491 (1980).

13) O’Connor, É., et al. "Observation of peripheral charge induced low frequency capacitance-voltage behaviour in metal-oxide-semiconductor capacitors on Si and GaAs substrates." *Journal of Applied Physics* **111**, 124104 (2012).