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Investigating vertical charge plasma tunnel field effect transistors beyond semiclassical assumptions

Iman Chahardah Cherik[1], Saeed Mohammadi[1]✉, Paul K. Hurley[2,3], Lida Ansari[2] & Farzan Gity[2]

In this paper, we examine the effects of subband quantization on the efficacy of an L-shaped gate vertical dopingless tunneling field-effect transistor. The proposed architecture leverages an intrinsic tunneling interface that is fully aligned with the gate metal, resulting in enhanced electrostatic control. We utilized a two-step numerical simulation approach grounded in the Schrödinger-Poisson equations to evaluate the performance of our proposed device and accurately calculate the ON-state current. Additionally, we assessed the influence of defects at the heterojunction on the performance of our device. Under quantum mechanical assumptions, parameters such as I_{ON} = 23.8 µA/µm, SS_{AVG} = 12.03 mV/dec, and the I_{ON}/I_{OFF} ratio = 4.88×10^{10} indicate that our structure is a promising candidate for high-performance applications.

Keywords TFET, Dopingless, Quantum confinement, Trap-assisted tunneling, Heterojunction

Short-channel thermionic emission-based transistors experience heightened uncontrollable diffusion currents and direct tunneling of charge carriers when in the OFF state[1]. The deterioration of OFF-state current can significantly impact static power consumption in CMOS technology[2]. To address these non-ideal phenomena, one viable solution is to manipulate the energy bands so that the transport of charge carriers occurs through a thin triangular potential barrier[3,4]. This principle underlies the operation of tunneling field-effect transistors (TFETs). These devices, known as through barrier tunneling transistors, offer advantages such as a sub-60 mV/dec subthreshold swing and reduced OFF-state current in comparison to FinFETs. Nevertheless, the design of low-power, high-performance TFETs remains a complex challenge[5,6].

In 2013, Kumar and Janardhanan introduced an innovative device known as dopingless TFET, which offers advantages such as a reduced thermal budget and mitigation of random-dopant fluctuations[7]. This device operates by utilizing inductive metals to generate holes and electrons within the source and drain regions, respectively. In the past decade, numerous scholars have suggested different approaches to improve the efficiency of dopingless TFETs. For instance, one study introduced a double-gate dopingless TFET utilizing a heterojunction of $In_{0.53}Ga_{0.47}As$-$In_{0.52}Al_{0.48}As$ and achieved an average subthreshold swing (SS_{AVG}) of 36.6 mV/dec[8]. In 2021, Sharma et al. developed the first dopingless tunnel FET based on methyl ammonium lead iodide ($CH_3NH_3PbI_3$), reporting an I_{ON} of 0.44 µA/µm at a gate-source voltage (V_{GS}) of 1 V[9]. The appealing properties of two-dimensional materials led to the design of a double-gate dopingless TFET based on Tungsten ditelluride (WTe_2), achieving an I_{ON} of 222 µA/µm[10]. A critical factor influencing the performance of dopingless TFETs is the reduction of the distance between the inductive metal and the semiconductor region, which can facilitate metal-to-semiconductor tunneling process and the formation of silicide. In 2022, Chahardah Cherik and Mohammadi proposed a scalable, CMOS-compatible solution known as a cladding layer-based TFET to address these non-idealities[11].

In this paper, we introduce a vertical doping-free tunnel field-effect transistor (VD-TFET) that employs a germanium-silicon heterojunction. To improve the device's performance, we have incorporated a 4 nm silicon channel situated between the source region and the gate oxide, facilitating line tunneling of charge carriers within the tunneling interface. Furthermore, we demonstrate that employing a semi-classical approach is inadequate

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for accurately simulating such a device. Consequently, we adopt a two-step simulation method grounded in the Schrödinger-Poisson equations to obtain a more realistic prediction of the device's performance.

Device architecture and simulation methodology

Figure 1 illustrates a three-dimensional representation of the proposed VD-TFET. This device features an inverted intrinsic T-shaped germanium (Ge) source region that is connected to an intrinsic L-shaped silicon (Si) channel. To facilitate the hole generation in the source region, two P^+-doped silicon layers with $N_{Clad} = 3\times10^{19}$ cm^{-3} have been employed, which exhibit a significant valence band offset relative to the source region. This design effectively mitigates unwanted band-to-band tunneling and thermionic emission of charge carriers at the source-cladding layer junctions. Additionally, a 3 nm layer of silicon dioxide (SiO_2) has been incorporated to prevent parasitic tunneling pathways between the highly doped silicon layers and the channel. To simplify the fabrication process and improve the AC/RF performance of the proposed structure, a doping concentration of $N_D = 3\times10^{18}$ cm^{-3} has been selected for the drain region. Furthermore, to improve the electrostatic control and minimize gate leakage current, a 2 nm layer of Hafnium(IV) oxide (HfO_2) has been utilized as the gate oxide. Finally, a gate metal exhibiting a work function of 3.65 eV has been employed to invert the entire tunneling junction, thereby further enhancing the ON-state performance of the VD-TFET.

All the simulations are carried out in Silvaco ATLAS simulation framework. To ensure the accuracy of the simulated results, and as depicted in Fig. 2a, we initially calibrated our simulator using the empirical data from vertical nanowire TFET based on a Ge-Si heterojunction[12]. It is important to note that the parameters of Kane's model are contingent upon doping levels; therefore, they must be individually calibrated for each distinct set of results[13]. For the calibration procedure we have set the following carriers' effective masses: Ge: $m_e = 0.15m_0$, $m_h = 0.22m_0$, Si: $m_e = 0.34m_0$, $m_h = 0.42m_0$. Due to the use of dopingless tunneling junctions and the inefficiency of the bandgap narrowing model for such a device, it is more effective to calibrate the device simulator using a prototype that closely resembles our device. Consequently, we calibrated our simulator using the extracted transfer characteristics of a dopingless TFET, as illustrated in Fig. 2b. In this case the carriers' effective masses are set to $m_e = 0.22m_0$ and $m_h = 0.17m_0$, and three distinct metals possessing the work functions of 5.93 eV, 4.5 eV and 3.9 eV create a P^+-i-N^+ structure from an undoped silicon.

We employed a one-dimensional Schrödinger-Poisson equation solver in the confinement direction to achieve a quantized representation of the density of states within the thin film channel. The confinement direction was specified by setting SP. GEOM = 1DY. We delineated the confinement region using the variables QX and QY. We employed a dynamic non-local BTBT model, which offers greater precision compared to traditional models such as those proposed by Kane or Hurkx. For the mobility model, we implemented the Lombardi (CVT) model,

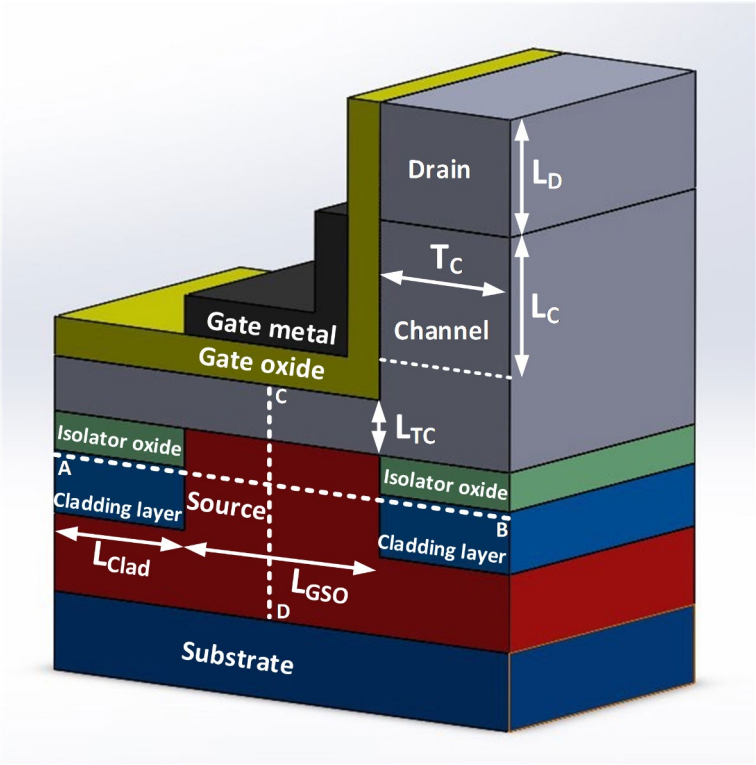


Fig. 1. A three-dimensional representation of the VD-TFET. Different dimensions of the device are exhibited in the figure. The length of the cladding layer (L_{Clad}), the gate-source overlap (L_{GSO}), the drain length (L_D), the channel thickness (T_C), the thickness of thin channel (L_{TC}), and the channel length (L_C) are 10 nm, 15 nm, 45 nm, 10 nm, 4 nm, and 15 nm, respectively.

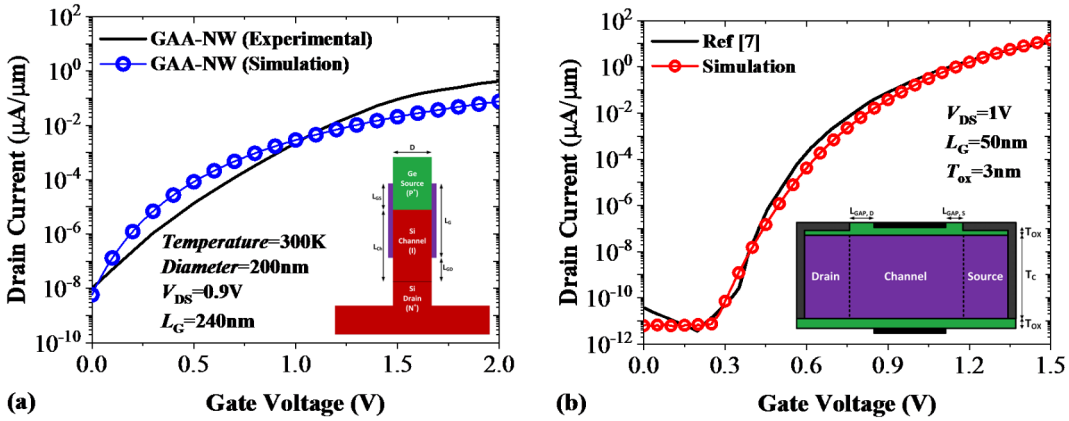


Fig. 2. Replication of the transfer curve of (a) a vertical nanowire TFET [12], and (b) a dopingless TFET [7] (b), utilizing our validated simulation framework.

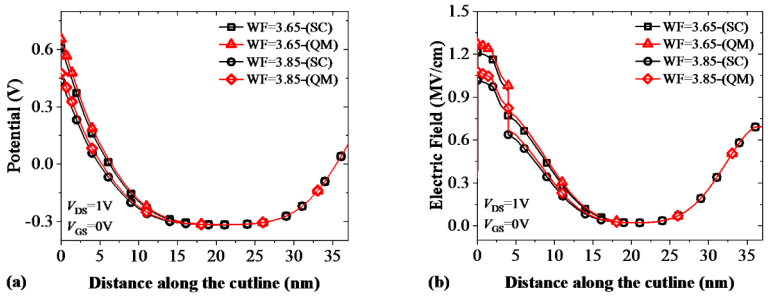


Fig. 3. Semiclassical and quantum mechanical simulation results of (a) the potential and (b) the electric field in VD-TFET. The profiles are along the C-D cutline of Fig. 1.

which evaluates the effects of doping, temperature, and transverse electric fields on charge carrier mobility. In calculating the generation and recombination of charge carriers, we applied the Shockley-Read-Hall (SRH) model. Additionally, the Fermi model was activated to estimate the statistical distribution of charge carriers. Drift-diffusion was selected as the framework for charge transport modeling.

As indicated in[15], the tunneling probability associated with a tunneling field-effect transistor (TFET) can be expressed through the following equation:

$$T(E) \propto \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3|e|\hbar(E_g+\Delta\Phi)}\sqrt{\frac{\varepsilon_c}{\varepsilon_{ox}}t_{ox}t_c}\right)\Delta\Phi$$

Where $\Delta\Phi$ is the tunneling barrier, E_g is the energy bandgap, and m^* is the tunneling effective mass. Incorporating a thin film into the design of our TFET results in the formation of a quantum well within the transistor channel. Consequently, the bulk values for parameters such as the tunneling barrier, energy bandgap, and effective mass are rendered invalid.

In our study, due to the implementation of a very thin channel in the proposed structure, we employed a three-step simulation approach, as outlined in[16]. The initial step involved obtaining the position of the first subband of electrons in the conduction band of the channel through a self-consistent solution of the Schrödinger-Poisson equations. Subsequently, we computed the quantum mechanical bandgap and electron affinity, which differ from their semiclassical counterparts. In the final stage, considering the widening of the bandgap within the channel, we proceeded to calculate the band-to-band tunneling current.

Simulation results

As the first step, we have extracted the potential profiles and the electric field diagrams for two different gate work functions as exhibited in Fig. 3a, b. Since in our proposed structure, the gate electric field and the tunneling path are oriented in the same direction; we have exclusively represented the potential and the electric field along the C-D cutline (plotted on Fig. 1). To have a more insightful representation, both semiclassical and quantum mechanical simulations have been carried out. As expected, when the quantum mechanical effects are considered, the carrier concentration decreases and consequently the absolute value of potential and slope of the potential change increase.

Figure 4a presents the energy bands plot along the A–B segment, as demonstrated in Fig. 1. This diagram substantiates our assertions regarding the reduction of non-ideal tunneling pathways and thermionic current. To facilitate a comparison between the Semiclassical and quantum mechanical methodologies, we have depicted the energy bands along the C–D cutline at the source-channel tunneling junction, under a constant drain-source voltage (V_{DS}) of 1 V and three distinct gate voltages. Figure 4b contrasts these two approaches at a V_{GS} of 0 V. It is evident that a significant tunneling pathway exists between the source region's valence band and the channel's conduction band within the Semiclassical framework. However, upon solving the Schrödinger-Poisson equation, it becomes apparent that the first subband of electrons (E_{e1}) in the channel is considerably elevated above the valence band edge in the source region, indicating that band-to-band tunneling (BTBT) is not feasible. An examination of Fig. 4c reveals that the valence band of the source region is marginally higher than the first electron subband, suggesting that the device is at the 'ON' state for both methodologies. Figure 4d illustrates the energy band diagram for V_{GS} equal to 1 V. Consistent with Fig. 4b and c, the distance and energy overlap at the tunneling junction, when analyzed through the quantum mechanical approach, has degraded in comparison to the Semiclassical approach.

The contour maps of band-to-band tunneling rate of electrons and their current density in the ON-state, depicted in Fig. 5a and b, verify the expected operation mechanism of the proposed device. The obtained results indicate a notable tunneling rate along the thin channel beneath the gate, and migration of charge carriers towards the N^+ drain region. Additionally, it is important to note that the employment of a single L-shaped gate results in a maximum current density at the interface adjacent to the gate metal.

In Fig. 6a, we present a comparison of the transfer curves of the VD-TFET for two distinct gate work functions utilizing both the Semiclassical and quantum mechanical approaches. The results indicate that the Semiclassical approach significantly enhances critical ON-state parameters, including threshold voltage, ON-state current, and the ON/OFF current ratio. Conversely, the quantum mechanical approach yields less favorable outcomes, albeit with greater realism. It is also crucial to emphasize that while a reduction in gate work function strengthens quantization effects within the channel, its impact on improving electrostatic control is more pronounced. Additionally, defects at the heterojunctions represent a non-ideal factor that can considerably impair the performance of the TFET, particularly in the OFF state[17]. In Fig. 6b, we explore a trap-assisted tunneling model incorporating various trap densities (D_t) and trap energy levels (E_t). The findings reveal that the activation of this model results in an OFF-state current of 2.21×10^{-5} μA/μm, and an ON/OFF current ratio of 1.07×10^6 in the worst-case scenario of $D_t = 1 \times 10^{13}$ cm^{-3}, and $E_t = 0.2$ eV.

Finally, a comparative analysis of the performance of our device against other analogous devices is presented in Table 1. The results support the notion that, even with the activation of non-ideal mechanisms such as quantum confinement and trap-assisted tunneling, the VD-TFET remains a high-performance device.

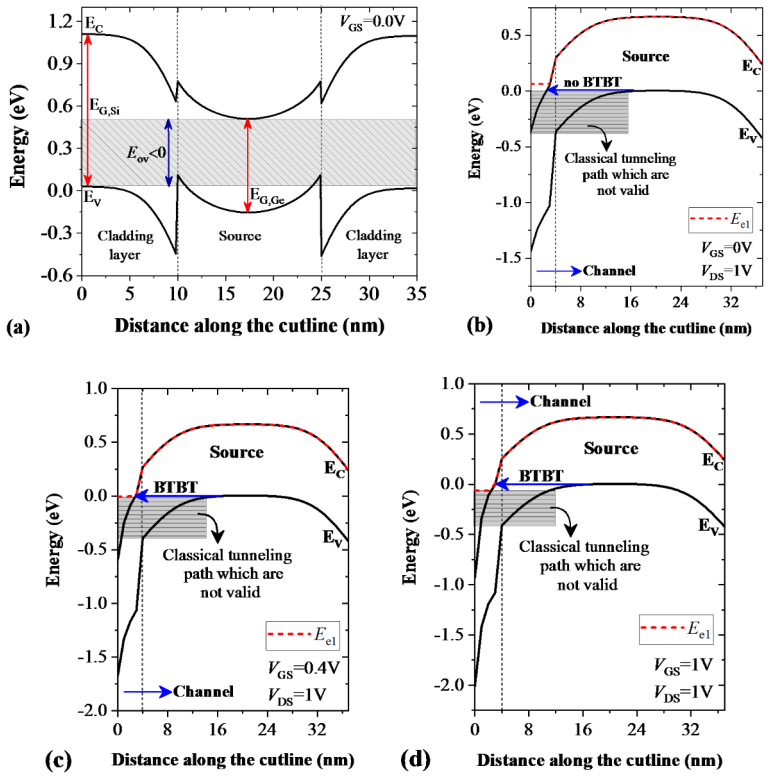


Fig. 4. (a) Energy band structure of the VD-TFET along the A-B cutline, as shown in Fig. 1. Panels (b), (c), and (d) present a comparative analysis of the band structures obtained through Semiclassical and quantum mechanical methodologies at V_{GS} = 0.0 V, V_{GS} = 0.4 V, and V_{GS} = 1 V, respectively.

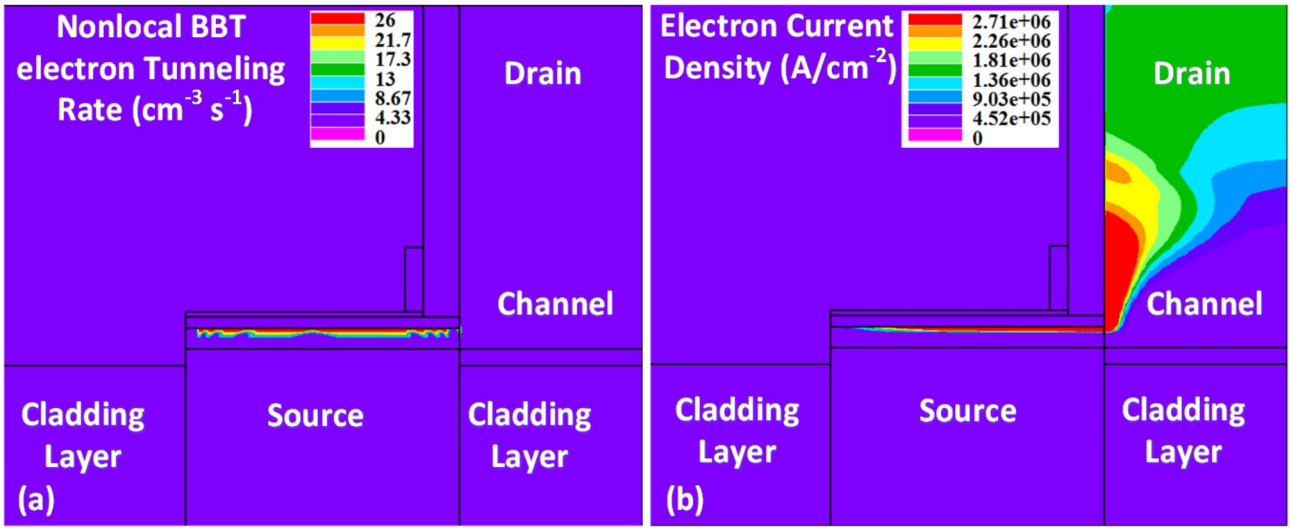


Fig. 5. (a) Band-to-band tunneling rate and (b) current density contour maps at $V_{GS} = V_{DS} = 1$ V.

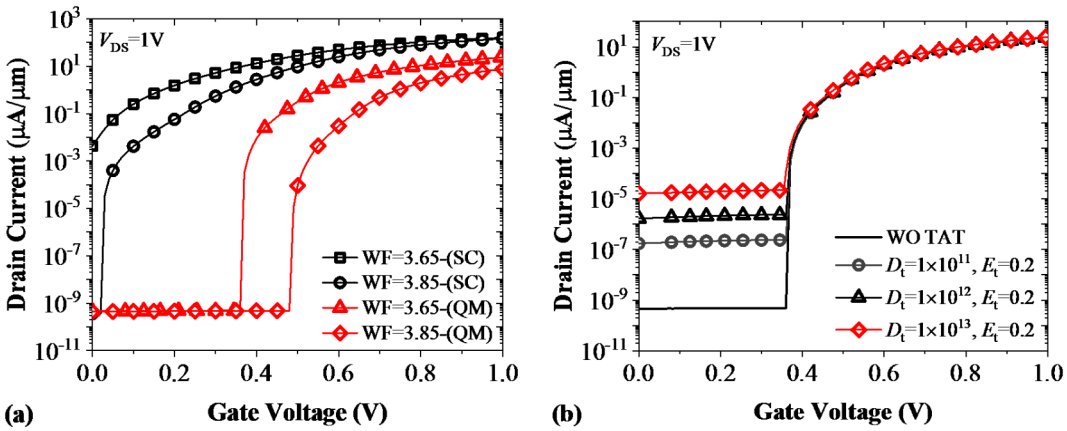


Fig. 6. (a) The influence of variations in the gate work function on the transfer curve of the VD-TFET, analyzed through both Semiclassical (SC) and quantum mechanical (QM) frameworks. (b) The effect of trap-assisted tunneling on the transfer curve of the VD-TFET.

Material	I_{ON} (μA/μm)	SS_{AVG} (mV/dec)	I_{ON}/I_{OFF}	V_{Bias} (V)	Refs.
Si	11	~100	1.1×10^{12}	1.5	[7]
$In_{0.53}Ga_{0.47}As$ -$In_{0.52}Al_{0.48}As$	16.7	36.6	1.96×10^{8}	0.6	[8]
$CH_3NH_3PbI_3$	0.44	27.33	1.85×10^{11}	1	[9]
WTe_2	222	54.15	2.22×10^{5}	0.5	[10]
Ge-Si	4.07	40.26	1.2×10^{10}	0.7	[11]
Si	14.6	19.28	$\sim4.8\times10^{15}$	1.5	[18]
$Si_{0.5}Ge_{0.5}$-Si	16.9	31.38	8.46×10^{11}	1	[19]
Si	~1.35	~72	1.35×10^{10}	1	[20]
Ge-Si	23.08	12.03	4.88×10^{10}	1	This work

Table 1. Evaluation of switching performance for various newly proposed dopingless tunnel field-effect transistors.

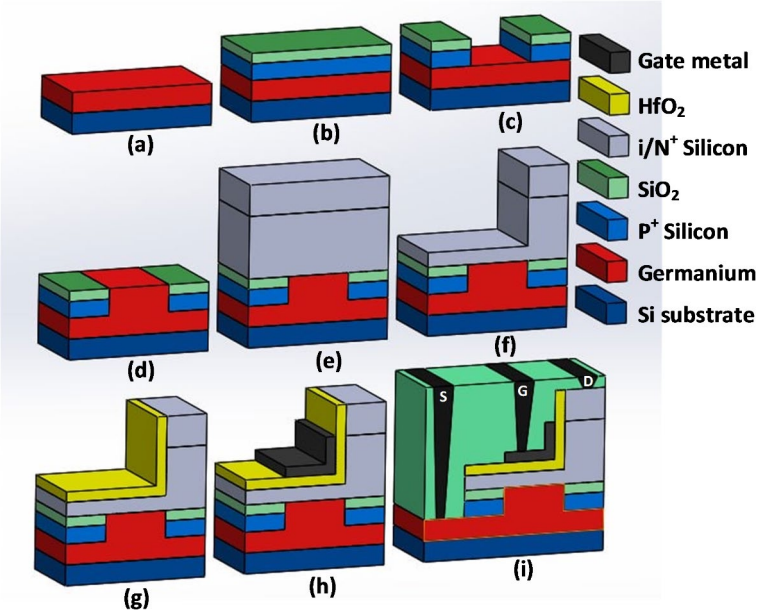


Fig. 7. (a–i) Summarized sequential steps involved in the fabrication of the vertical VD-TFET structure.

Proposed fabrication process

In this section we propose a viable fabrication process for realization of VD-TFET. The process initiates with the deposition of an intrinsic germanium layer onto a P^+-doped silicon substrate (refer to Fig. 7a). Subsequently, an epitaxially grown layer of heavily doped silicon will serve as a cladding layer, followed by the application of a SiO_2 layer, which functions as an isolating oxide (see Fig. 7b). The next phase involves the creation of a U-shaped trench through two sequential etching processes targeting both SiO_2 and silicon (refer to Fig. 7c). In the subsequent step, a layer of germanium will be deposited within the trench to construct an inverted T-shaped source (see Fig. 7d). An intrinsic silicon layer will then be added over the previously formed structure, succeeded by the growth of an N^+-doped silicon layer (see Fig. 7e). After etching the unwanted regions of the silicon layer, a Hafnium oxide layer will be deposited in an L-shaped configuration (refer to Fig. 7f, g). In the next step, gate metal will be applied to fully cover the tunneling interface (see Fig. 7h). The fabrication process concludes with the deposition of SiO_2, which will serve as a spacer and facilitate contact connections (see Fig. 7i).

Conclusion

To enhance the efficiency of tunneling transistors, various strategies, including the reduction of the device's thickness, have been proposed. This approach may result in subband quantization within the channel. In this study, we evaluate the impact of quantum confinement in the channel of vertical dopingless tunneling field-effect transistor (VD-TFET) based on a Ge-Si heterojunction. Our findings indicate that the most effective approach for simulating thin-channel TFETs involves solving the Schrödinger-Poisson equation within the channel, followed by the calculation of the ON-state current using the quantum mechanical bandgap. Additionally, we have taken into account the non-ideal effects of defects at the heterojunction that forms the tunneling interface to further validate the OFF-state performance.

Data availability

The datasets used and/or analyzed during the current study available from the corresponding author on reasonable request.

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Author contributions

Iman Chahardah Cherik: Conceptualization, Methodology, Software, Formal analysis, Investigation, Visualization, Data Curation, Writing - Original Draft Saeed Mohammadi: Conceptualization, Validation, Investigation, Resources, Data Curation, Supervision, Project administration, Writing - Review & Editing Paul K. Hurley: Conceptualization, Investigation, Validation, Resources, Data Curation, Writing - Review & Editing Lida Ansari: Conceptualization, Investigation, Validation, Resources, Data Curation, Writing - Review & Editing Farzan Gity: Conceptualization, Investigation, Validation, Resources, Data Curation, Writing - Review & Editing.

Competing interests

The authors declare no competing interests.

Additional information

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