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Scale Up Of Advanced Packaging And System Integration For Hybrid Technologies

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***Abstract*—This paper presents an overview of challenges in system integration for 2.5D/3D assemblies, including co-packaged optics and electronics, MEMS and microfluidics. It addresses the gap between early-stage prototypes and volume manufacturing that need true advanced packaging and system integration to realize their complex multi-technology devices. This is done by means of a virtual demonstrator that include both 2.5D/3D assemblies of ASICs and integrated photonic devices, as well as MEMS and microfluidics devices. It also addresses lowering the cost barrier for users accessing these technologies for their products, such that it will enable an increased uptake of system integration by the industry at large.**

Keywords—system integration, 2.5/3D integration, photonics packaging, MEMS, microfluidics, MPW runs, cost sharing

I. Introduction

There is a growing demand for advanced packaging and system integration in the semiconductor industry. This trend has been fuelled by the need for better integration of more functionalities in a system-on-chip (SoC) from a wide range of applications, including high-speed datacom, artificial intelligence (AI), Internet of Things (IoT) and bio-medical devices. There has been significant research and development to address the demand for co-packaged microelectronics and optics & photonics, including hybrids such as Micro-Electrical Mechanical Systems (MEMS) and microfluidics. However, such combinations of technologies often requires discrete assembly techniques at component level, which presents challenges to minimise power consumption, reduce footprint, increase data rates, manage thermal and mechanical stresses. Furthermore, there is a need for cost effective and scalable manufacturing processes.

This paper will review the world's first advanced packaging and smart system integration virtual demonstrator developed in the scope of the NEXTS project. The NEXTS project aims to extend the EUROPRACTICE services towards smart system integration [1]. The virtual demonstrator in Figure 1 is a combination of multiple smaller virtual demonstrators combined in a single illustration that showcases key cost cutting building blocks for various technology platforms that make system integration possible between multiple technologies and guides researchers and developers in their process of selecting suitable and industrial available building blocks. This covers a range of technologies; advanced packaging of ASICs, optics & photonics, MEMS and microfluidics, and combinations thereof, which are available for users through EUROPRACTICE. These combinations are made possible through access to a variety of specialised services of key enabling technologies including; pick-and-place, flip-chip, Ball Grid Arrays (BGAs), Cu pillars, wafer-level fan-outs as well as silicon interposers, which facilitate 2.5/3D integration of ASICs and Photonic Integrated Circuits (PICs) through die stacking techniques. Other technologies made possible include hybrid integration of MEMS such as accelerometers and cantilevers, and add-on processes for noble metal finishes and microfluidic building blocks which are prerequisites for many bio-medical sensor devices. Most importantly, all solutions use industry standard processes making them scalable to high volume and typically also more cost effective.

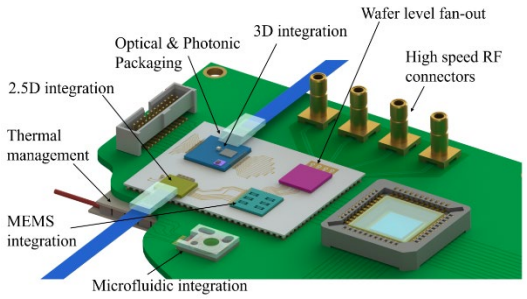


Fig. 1. Virtual demonstrator of scalable advanced packaging and system integration.

II. System Integration and Enabling Process Modules

A. 2.5D/3D System Integration

System Integration is defined in this paper as the methodology used to combine at least two devices stacked and interconnected, or packaged side-by-side on a substrate.

When two or more IC devices are stacked that is called 3D-IC integration or 3D-IC stacking. Individual devices can be the same type such as memories, or can be different devices resulting in heterogeneous integration. The main motivation of such integration is to exploit the 3rd dimension to decrease the footprint of the whole system, and to make tighter interconnections between the sub-circuits. As a result, the system will see a decrease of interconnection parasitics, decreasing the power consumption, while increasing the bandwidth and speed [2].

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Similar to 3D-IC integration, 2.5D consists of integrating two or more devices, however in this case it is side-by-side on a substrate such as an interposer, and the interconnections use bumps or wire bonding.

Figure 2 is a virtual illustration of the 2.5D hybrid integration. Here, system integration is composed of process modules, when combined in a given process flow, allows for packaging different circuits together enabling miniaturization. Such process modules include wire bonding, flip-chip, Under Bump Metallization (UBM), interposers, Through Silicon Via (TSV), and Re-Distribution Layer (RDL) to name a few.

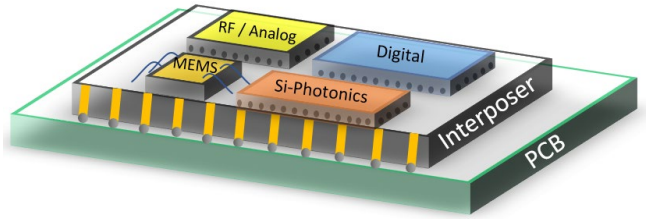


Fig. 2. Schematic of 2.5D hybrid integration

In order to make 2.5/3D system integration accessible to a wide range of users, it is key to drive down the cost of the different process modules and packaging techniques, while preserving the performance and reliability of the system.

The sections below zoom in on specific process modules and/or packaging techniques are used in 2.5/3D integration, namely interposers, bumping, TSVs and Fan-Out Wafer-Level Packaging (FOWLP). In particular, the focus will be on making those technologies more accessible and affordable by cost sharing between users, which improves user uptake of system integration.

B. Interposers

An interposer is a substrate to which individual die(s) can be bonded and connected to each other. As an integration handler, interposers have internal pads and metal routing to allow for intra-chip connections, and periphery pads for the system's primary I/Os. Typically, interposers can be composed of organic, ceramic or silicon material. In the case of Silicon Interposers (Si-Interposers) the minimum width and pitch of interconnections are in the range of microns or even sub-microns, while for organic/ceramic interposers in the order of 100 microns feature size. As such, Si-Interposers are preferred as they enable tighter connections between the separate dies, which in turn, introduces less parasitics, and ensures high density of the system.

Si-Interposers can be passive when a Back-End-of-the-Line (BEOL) metal stack is used, or active when embedded with active devices such as diodes, CMOS, or bipolar devices. Their fabrication can be through a dedicated process, in this case the BEOL metal stack of any CMOS process is sufficient. Figure 3 shows a cross section of Si-Interposer used as an enabler in 2.5/3D system integration.

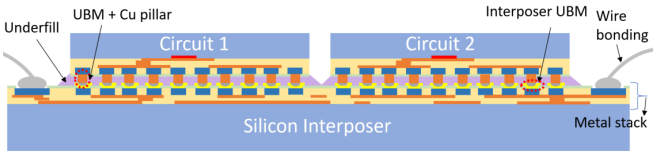


Fig. 3. Illustration of Si-Interposer as an enabler for 2.5/3D system integration

For prototyping and low volume production, an efficient method to reduce the total cost would be to share the mask-set of a CMOS Multi-Project Wafer (MPW) run and fabricate the Si-Interposer together with the other CMOS chips. An alternative method for lowering the fabrication cost for prototyping consists of using a Multi-Layer Mask (MLM) where the mask cost is drastically reduced. Alternatively, one can also think of offering MPW services specifically for Si-interposers. This requires standardization of both technology options and design rules, such that different customer requirements can be served on the same Si-interposer MPW run.

C. Circuit Bumping

In order to achieve a flip-chip process connecting circuits to the interposer, circuits need to have bumps on their pads. These bumps could be solder bumps, Cu pillar bumps, or stud bumps. Figure 4 are magnifications of the bump technologies.

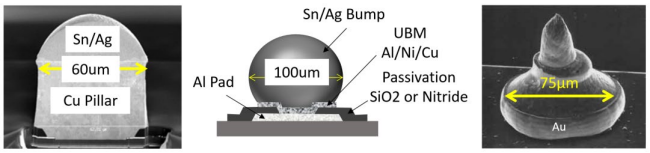


Fig. 4. Bumps technologies: (a) Cu pillar, (b) solder bump, (c) stud bump.

As circuit pads are commonly in Aluminum, they need to have an UBM process before adding the bump. Several types of UBM materials can be used e.g. Ti/Cu/Ni. This material is grown on the Al pad in order to allow the attach of solder bumps or copper pillar bumps. Cu pillar and solder bumps (as shown in Figure 4a and 4b) are grown at wafer level, using lithography masks.

These bumping techniques can be part of the foundry processing, or can be subcontracted to Outsourced Semiconductor Assembly and Test (OSAT) companies. These processes can also be performed on a MPW run where different projects can get the same type of bump. That could be a solution to share the bumping pricing between different customers for the prototyping phase.

Stud bumps shown in Figure 4c are gold bumps obtained by making a thermo-sonic wire-bond, then cutting the wire just after soldering the wire on the circuit's pads. While this process is usually done at chip-level as for wire-bonding, the process is mature and low cost, but has as drawback that the bumps are made one by one in a sequential process, as opposed to the Cu pillar and solder bumps made once in parallel at wafer-level [3].

Stud bumps do not need UBM, the ultrasonic process for soldering the bump allows it to be attached efficiently to the Aluminum pads of the circuit die. Stud bumps are suitable for prototyping or very low volume production as it is affordable and can be accessible to any packaging house that has wire bonding capabilities.

D. Through Silicon Via (TSV)

To connect vertically and exploit the 3rd dimension, the use of TSVs gives the optimal solution interconnections from the face of a chip to its back. TSV consists of drilling holes across the silicon chip and deposit a dielectric / barrier in the hole. This allows for metallization growth in the via. Thus connecting the face of the chip to the backside of the chip. The drilling is done by etching the silicon, the dielectric and

metallization depositions are done using photolithography, all at wafer-level [4].

Since this process is at wafer-level, it is a good candidate for cost sharing using MPW runs. Figure 5 illustrates the TSVs in a chip (circuit 2), and the use of a Si-interposer to connect the primary I/Os of the system as an array at the backside of the interposer.

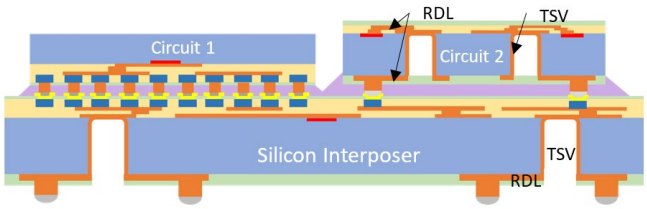


Fig. 5. Both back-to-face and face-to-face assembly on back-bumped silicon interposer using TSVs.

E. Fan-Out Wafer Level Packaging

Wafer level fan-out packaging is a technology where dies from different sources or different technologies with varying thickness and size can be handled and packaged with one integration technology. FOWLP offers a special packaging solution based on the concept of standard Wafer Level Chip Size Packaging (WLCSP) processes. WLCSP processes are a good solution for volume production with high frequency applications because of small packages sizes with very small parasitic effects. The parasitic effects of such a package are low thanks to the small size and no use of bond wires. The main drawback of WLCSP is that the Non-Recurring Engineering (NRE) costs starts at about 50,000 EUR and multiple wafers need to be ordered.

Fraunhofer IZM [5] has been focusing on a solution which can drive down the cost for very small volume and prototyping using a Multi-Project concept similar to the MPWs of semiconductor foundries and offered through EUROPRACTICE. Multi-Project Fan-Out Wafer Level Packaging users share wafer and processing costs, making it more affordable. Figure 6 illustrates the low volume prototyping using multi project fan-out wafer level packaging.

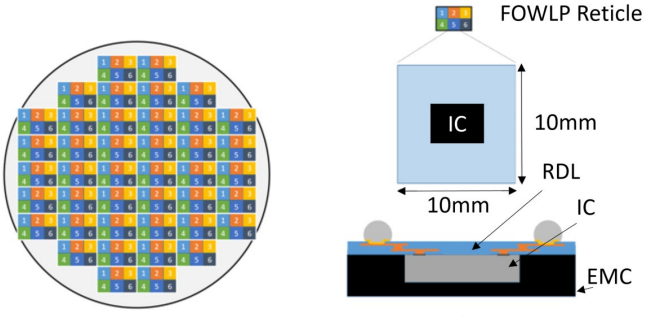


Fig. 6. Wafer Level Fan-Out: (a) Multi project fan-out wafer and (b) FOWLP package (b).

The die could come from different foundries and technologies but should have an edge length of 1.5 to 7 mm and die thickness have to be in a range of 200 – 300 µm. The FOWLP technology use SnAgCu balls with a ball size of 300 µm and a pitch of 500 µm. As a standard for these Multi-Project runs two RDL are fabricated to connect the pad openings of the die with the balls of the package. The RDL layers are useable in integrated antennae or inductors. This possibility to integrate passive structures can reduce the silicon die size and save cost. With the FOWLP technology from Fraunhofer IZM all packages have a size of 10 mm by 10 mm independent on the size of the die. This helps maximize the area on the wafer and avoids any loss of ICs by sawing out the individual devices.

Offering Fan-Out Wafer Level Packaging similar to standard MPW runs makes it possible to package prototypes, reduce the costs per project and include all the positive effects of WLCSP.

III. ADVANCED PHOTONICS PACKAGING

Previously considered specialized functions, PICs and optoelectronics have become much more mainstream due to the rise of 5G and high speed, high-density Datacom transceivers. Typically, photonic packaging and integration requires multiple considerations including the optical interfaces, electrical connections that can be DC or RF in function, thermal management and mechanical housing. These subassembly techniques usually involve surface mount technology such as flip-chip assembly, where the die is mounted on a substrate or an interposer. This technique can be manually carried out or automated for volume prototyping, with sub-micron alignment accuracy. Subsequently, the substrate can be assembled onto a PCB with a pick-and-place tool. Before the subassembly is placed into the housing a fibre attach is carried out.

Another PIC integration technology that opens up affordable volume prototyping opportunities in new areas is the combination of two platforms, low-loss SiN-based TriPleX™ waveguide technology and active InP components [6]. The InP tunable laser covers the C-band, and the TriPleX™ waveguides are designed for single polarization (TE) applications at 1550nm. The high contrast waveguide allows bend radii of 125 micron, which makes large scale integration (VLSI) on chip possible. This VLSI technology allows for low cost integration. Figure 7 shows the design layout rule for users to access this MPW unique technology integration platform with a route to easy assembly and packaging.

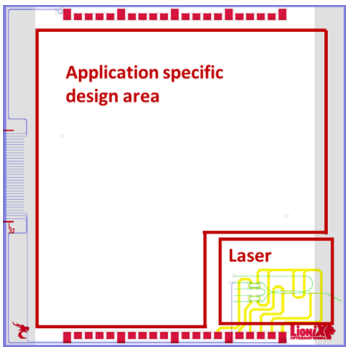


Fig. 7. Design rule for MPW layout of C-band InP tunable laser on SiN

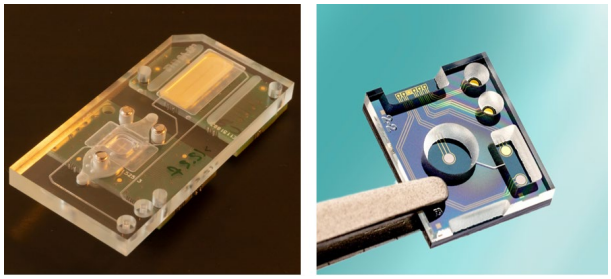
IV. MEMS INTEGRATION

MEMS can be classified either as sensor or an actuator. Both categories use ASICs interface with the outside world to sense the signal or drive the actuator to perform an action. The sensing / actuation mechanism of these devices can be capacitive, piezoelectric, piezoresistive, electrostatic to name a few. It is essential to integrate a MEMS device with an associated peripheral device/circuit to complete a system. System integration of MEMS devices can be on a single wafer (monolithic integration) [7] using the technology of "MEMS

first", where on a single wafer the MEMS (unreleased structure) is fabricated first and then on the same wafer CMOS circuit is fabricated or "CMOS first" where first the CMOS circuit is fabricated on a wafer and then on the same wafer the MEMS device is fabricated. These processes are not cost effective and most researchers and industries go for hybrid packaging where the MEMS and ASICs are discrete components, packaged separately and integrated on a common substrate such as an interposer or PCB. The fact that a properly integrated system can bring down the power consumption, makes it very attractive to industries and researchers to explore different options like Micro Transfer Printing (MTP) for system integration of MEMS devices that are commercially used for system integration of photonic devices. Using such technologies, heterogeneous devices can be system integrated on a single wafer.

V. Microfluidics Integration

While most commercial Si chip packages envision a closed Si surface, this is not the case for many sensors and in particular liquid sensing solutions. Apart from the the typical need for electrical routing, an additional constraint comes from the fluidic access that is needed on top of the Si sensor surface. For reasons of corrosion prevention and surface functionalization purposes, the typical Cu or Al top metallization finishes need a noble metal cover, which is the first deviation from standard CMOS offerings [8].



(a) (b)

Fig. 8. Demonstrator examples of: (a) die-to-die sensor-cartridge bonding and (b) wafer-level Si-to-glass bonding (b).

Two main integration routes for microfluidic devices can be distinguished: wafer level versus die-level. Depending on the level of complexity, the type and required dimensions and resolution of the microfluidic building blocks but also cost and accessibility, one or the other is preferred. For each of the two configurations, an example is shown in Figure 8. Figure 8 (a) illustrates Chip on board (COB) bonding of a sensor ISFET chip and a magnetic coil actuator chip which are both assembled to a plastic (milled) cartridge. A small height compartment is defined at the backside of the cartridge and die-to-die (Si-to-cartridge) adhesive bonding is performed by adhesive dispensing surrounding the compartment walls, followed by alignment and placement. Figure 8 demonstrates the formation of microfluidic functionalities (reservoirs and channels) by wafer-level lithography and glass patterning which is then wafer-to-wafer bonded to a Si sensor wafer. In both cases, special "leave-out" zones are foreseen for access to the wire-bonding pads.

The market uptake of such sensors is strongly dependant on their implementation in a global system solution and therefore, access to scalable and cost-effective integration solutions is of key importance. In terms of product manufacturing scaling potential and dimensional resolution capabilities, wafer-to-wafer bonding is expected to be most promising while die-to-die bonding is advantageous for lower volume solutions. In order to lower the cost barrier for these advanced wafer-level process solutions, noble metal surface finishes can be offered in Multi-Project Wafer (MPW) and Multi-Layer Mask (MLM) mode. Glass cap wafer manufacturing and wafer-to-wafer bonding to Si sensor wafers can be offered through MLM mode.

VI. Conclusion

This paper presented the world's first virtual demonstrator for smart system integration. It showcases key cost cutting building blocks for various technology platforms that make system integration possible between multiple technologies and guides researchers and developers in their process of selecting suitable and industrial available building blocks.

A wide range of technologies were presented; 2.5D/3D assemblies of ASICs and integrated photonic devices, as well as MEMS, microfluidics devices and combinations thereof, which are available for users through EUROPRACTICE. This allows for early stage prototyping and volume manufacturing.

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Abbreviations—BEOL; Back-End-Of-Line, BGA; Ball Grid Array, COB: Chip On Board, FOWLP; Fan-Out Wafer Level Packaging, MLM; Multi-Layer Mask, MPW; Multi-Project Wafer, OSAT; Outsourced Semiconductor Assembly and Test, PIC; Photonic Integrated Circuit, RDL; Redistribution Layer, SoC; System on Chip, TSV; Through Silicon Via, UBM; Under Bump Metallization, WLCSP; Wafer Level Chip Size Packaging.

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