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Title	Flip-chip bonded micro-thermoelectric coolers for on-chip thermal management in integrated photonics
Authors	Kaur, Rajvinder;Tanwar, Amit;O'Brien, Peter;Razeeb, Kafil M.
Publication date	2025-09-26
Original Citation	Kaur, R., Tanwar, A., O'Brien, P. and Razeeb, K. M. (2025) 'Flip-chip bonded micro-thermoelectric coolers for on-chip thermal management of integrated photonic devices', Applied Thermal Engineering, 280(5), 128468 (10pp). https://doi.org/10.1016/j.applthermaleng.2025.128468
Type of publication	Article (peer-reviewed);journal-article
Link to publisher's version	10.1016/j.applthermaleng.2025.128468
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Flip-Chip Bonded Micro-Thermoelectric Coolers for on-chip Thermal Management of Integrated Photonic Devices

Rajvinder Kaur, Amit Tanwar, Peter O'Brien and Kafil M. Razeeb*

Tyndall National Institute, University College Cork, Lee Maltings, Dyke Parade, Cork T12 R5CP, Ireland

*Corresponding author's E-mail address: kafil.mahmood@tyndall.ie

Abstract

Thermal management is a key challenge in high-density photonic integrated circuits, where local hotspots destabilize the wavelength of the photonic device and degrade overall performance. Unlike conventional cooling strategies, micro-thermoelectric coolers (micro-TECs) offer a compact, solid-state, CMOS-compatible solution for localized, on-chip cooling and precise thermal management. In this work, micro-TEC devices are fabricated on Si/SiO_2 substrate using electrodeposited n-type Bi_2Te_3 and p-type CuSbTe thermoelectric materials. The 4.4 × 4.4 mm²-sized devices comprise n- and p-type thermoelectric leg-pairs with a 150 × 150 µm² cross-sectional area and 13 µm height, which are electrically connected by top and bottom Au interconnects via a flip-chip bonding approach. The fabricated devices achieve net cooling of ~1.2 K at 100 mA and 0.71 K at 75 mA at room temperature. Results indicate that high electrical contact resistance at the bonding interfaces limits the cooling performance. Further, COMSOL simulations predict a net cooling of 6.18 K when the leg height is increased to 60 µm and the contact resistivity is reduced to 10^{-11} $\Omega.m^2$. This study provides quantitative design guidelines for micro-TEC interfaces and geometry and demonstrates the feasibility of direct micro-TEC integration onto silicon platforms for on-chip thermal management of photonic components.

Keywords: Micro-thermoelectric cooler, Electrodeposition, Thin film, Flip-chip bonding

Introduction

The growing demand for miniaturized and highly integrated next-generation optoelectronic devices within photonic integrated circuits (PICs) is driving significant advancements in telecommunications technologies. However, it also introduces major challenges and thermal management is one of them [1]. As photonic and electronic device dimensions become smaller, they generate extreme heat flux at the chip and packaging level, which can degrade performance and long-term reliability. This issue is particularly pronounced in temperature-sensitive photonic components such as lasers, semiconductor optical amplifiers (SOAs), and micro-ring resonators, which operate within strict thermal tolerances and are highly susceptible to temperature

fluctuations. These fluctuations can induce wavelength drift and lead to temperature-induced signal degradation [2]. Consequently, localized on-chip thermal control has become crucial to ensure the stable and efficient operation of advanced integrated photonic systems [3, 4].

Traditional cooling strategies, including fans, liquid cooling, and spray cooling, have been widely employed [5-7], but they are impractical for miniaturized and integrated systems. They often create noise and vibration, add system complexity, or require bulky mechanical supporting arrangements. In contrast, thermoelectric cooling, due to its solid-state nature, absence of moving parts, and noise-free operation, offers an efficient thermal management solution for electronic and photonic components [3, 8-10]. A typical thermoelectric cooler (TEC) consists of p-type and n-type thermoelectric materials connected electrically in series and thermally in parallel. When a direct current passes through the TEC, heat is absorbed at one junction and released at the other, a phenomenon known as the Peltier effect, which allows cooling or heating on either side [10]. However, the relatively large size of macro-TECs poses a significant limitation when it comes to direct integration with microscale devices**.** Recent research has focused on developing miniaturized TECs that can address localized hotspots and offer precise on-chip thermal control [11, 12].

Thin film-based micro-TECs are promising for precise thermal management in modern high-density integrated photonic systems due to their compact size and compatibility with CMOS fabrication processes [13, 14]. Their direct integration with photonic devices enables fast thermal response and stabilizes the operating wavelength of lasers [15], thereby mitigating thermally induced drift and maintaining performance and reliability [1, 14]. They open up new possibilities for photonic integrated circuits capable of handling high heat fluxes, up to several hundreds of $W.cm^{-2}$ [16, 17]. Beyond photonics, such micro-TECs also hold promise for hotspot mitigation in advanced microelectronics, high-performance computing, and for providing temperature control in biomedical devices and aerospace applications [18-20].

Various deposition techniques such as sputtering [21], MOCVD [22], co-evaporation [23], and electrodeposition [24] have been employed for fabricating thin-film-based micro-TECs with cross-plane or vertical structures. Among these, electrodeposition stands out for its low cost, compatibility with standard semiconductor manufacturing, and ability to produce thick thermoelectric legs [25]. Several groups have reported electrodeposited micro-TECs on silicon substrates, achieving temperature drops of a few Kelvins [26-28].

However, most reported micro-TECs adopt bridge-like structures, which can limit their ability to provide localized cooling of photonic components on the same substrate at the package level. Flip-chip bonding has therefore been explored to form vertical micro-TEC structures [29]. This approach enables the compact and robust integration of π-shaped leg-pairs of coolers directly over localized hot spots, providing an efficient way of on-chip thermal management. Despite its potential, there are limited studies on the fabrication of the electrodeposited micro-thermoelectric device with flip-chip bonding [30, 31]. Moreover, while these studies highlight the formation of high contact resistance at metal-thermoelectric material interfaces during flip-chip

integration, its effect on cooling performance has not been fully explored. However, Bottner et al. reported a co-sputtered micro-cooler where low contact resistance improved net cooling at room temperature [32]. These findings indicate that high cooling performance in micro-TECs can be achieved through careful optimization of contact resistance and device architecture.

In this work, we demonstrate flip-chip bonded micro-TEC devices on the Si/SiO_2 substrate, comprising electrodeposited n-type Bi_2Te_3 and p-type CuSbTe thermoelectric legs in the vertical π-shaped structure. The legs with a cross-sectional area of 150 × 150 μm^2 are interconnected with Au via Au/In/Au thermo-compression bonding. Systematic measurements are carried out to examine the influence of bonding force on internal resistance and cooling performance. By addressing the critical bottleneck of contact resistivity and providing validated design guidelines for geometry optimization, this work outlines a practical pathway towards enhanced cooling performance for the micro-TEC devices.

Experimental procedures

1. Electrodeposition of thermoelectric materials:

Bi_2Te_3 and CuSbTe are used as n- and p-type thermoelectric (TE) thin film materials, respectively, developed by the electrodeposition method [33]. N-type Bi_2Te_3 electrolyte bath consists of 1 M HNO_3 acid (ACS reagent, 70%), 15 mM Te powder (99.8% trace metals basis) and 10 mM $Bi(NO_3)_3{\cdot}5H_2O$ (ACS reagent, ≥98.0%). First, the Te powder is dissolved in a 1 M HNO_3 solution at 45 °C under constant stirring. Once Te is dissolved, $Bi(NO_3)_3{\cdot}5H_2O$ is added to the solution, followed by the addition of deionized (DI) water to reach the final volume of the electrolyte. P-type CuSbTe electrolyte bath is prepared using 1 M HNO_3, 3.6 mM TeO_2 (≥99%), 2.4 mM Sb_2O_3 (ReagentPlus®, 99%), 50 mM tartaric acid (ACS reagent, ≥99.5%) and 1.0 mM $CuSO_4.5H_2O$ (ACS reagent, ≥98.0%). First, TeO_2 is dissolved in 1 M HNO_3 acid at 45 °C while stirring. The second solution is prepared by dissolving Sb_2O_3 in tartaric acid at 60 °C under stirring. After their complete dissolution, these two solutions are mixed together, and subsequently, $CuSO_4{\cdot}5H_2O$ is added. Finally, DI water is added to achieve the final volume of the bath. The TE electrodepositions are performed in a three-electrode configuration using a CHI660C potentiostat at room temperature. Platinized Ti mesh is used as the counter electrode and Ag/AgCl as the reference electrode. The working electrode is prepared on the silicon (Si) substrate with a 1 µm thick thermally grown SiO_2, followed by the evaporation of a 20 nm of Ti and a 200 nm of Au layer. The substrate is cleaned with acetone, IPA, and DI water before and after each electrodeposition. Both Bi_2Te_3 and CuSbTe films are annealed at 150 °C for 1 hr under an N_2 atmosphere.

2. Device fabrication process:

The micro-TEC device fabrication process combines several electrodeposition and photolithography steps. In our previous work, the geometrical optimization of the height and cross-sectional area of the TE materials as legs was investigated using finite element analysis, which also included the metal interconnect thickness and other parameters [34]. Based on these

COMSOL simulation findings, the photolithographic masks are designed for a 4.4 × 4.4 mm^2-sized micro-TEC device with a cross-sectional area of 150 × 150 μm^2 for both n-type and p-type TE legs. The device process flow is illustrated in Figure 1, comprising 7 photolithography masks. This process involves the flip-chip bonding of the two substrates, where one substrate contains bottom metal interconnects and TE legs, while the other provides the top metal interconnects. After flip-chip bonding, the p- and n-type TE legs are connected electrically in series to form the π-shaped daisy chain of TE leg-pairs.

All electrodepositions during device fabrication are performed in a 1-liter beaker at room temperature on the 4-inch Si/SiO_2 wafer. The wafer is evaporated with 20/200 nm of Ti/Au, serving as a seed layer for the electrodeposition process, as shown in Figure 1(a). The SUSS MA6 mask aligner is used for photolithography steps. The wafer is coated with AZ-10XT photoresist (PR) and baked at 110 °C for 2 min. After the exposure, the PR pattern is attained to define the bottom Au interconnects (Figure 1(b)) with AZ 400K developer. Au electrodeposition is carried out using a commercial Au bath (NB Semiplate Au 100, MicroChemicals) at a constant current density of 1.5 mA cm^{-2} with a platinized Ti mesh counter electrode. After achieving an optimum thickness of Au, the PR is removed in acetone, as shown in Figure 1(c). For the n-type Bi_2Te_3 TE legs, the lithography process is carried out using a 25 µm thick AZ-40XT photoresist, which is coated and soft-baked at 125 °C for 7 min. The desired PR pattern is exposed, then baked at 105 °C for 2 min and developed using the MF-26A developer as shown in Figure 1(d). The PR is removed once the Bi_2Te_3 is electrodeposited on the patterned area (Figure 1(e)). Similarly, in the next lithography step, patterning of PR AZ-40XT (Figure 1(f)) is performed for the electrodeposition of p-type CuSbTe TE legs. After that, the photoresist is removed in acetone. Figure 1(g) illustrates the vertically grown Bi_2Te_3 and CuSbTe legs.

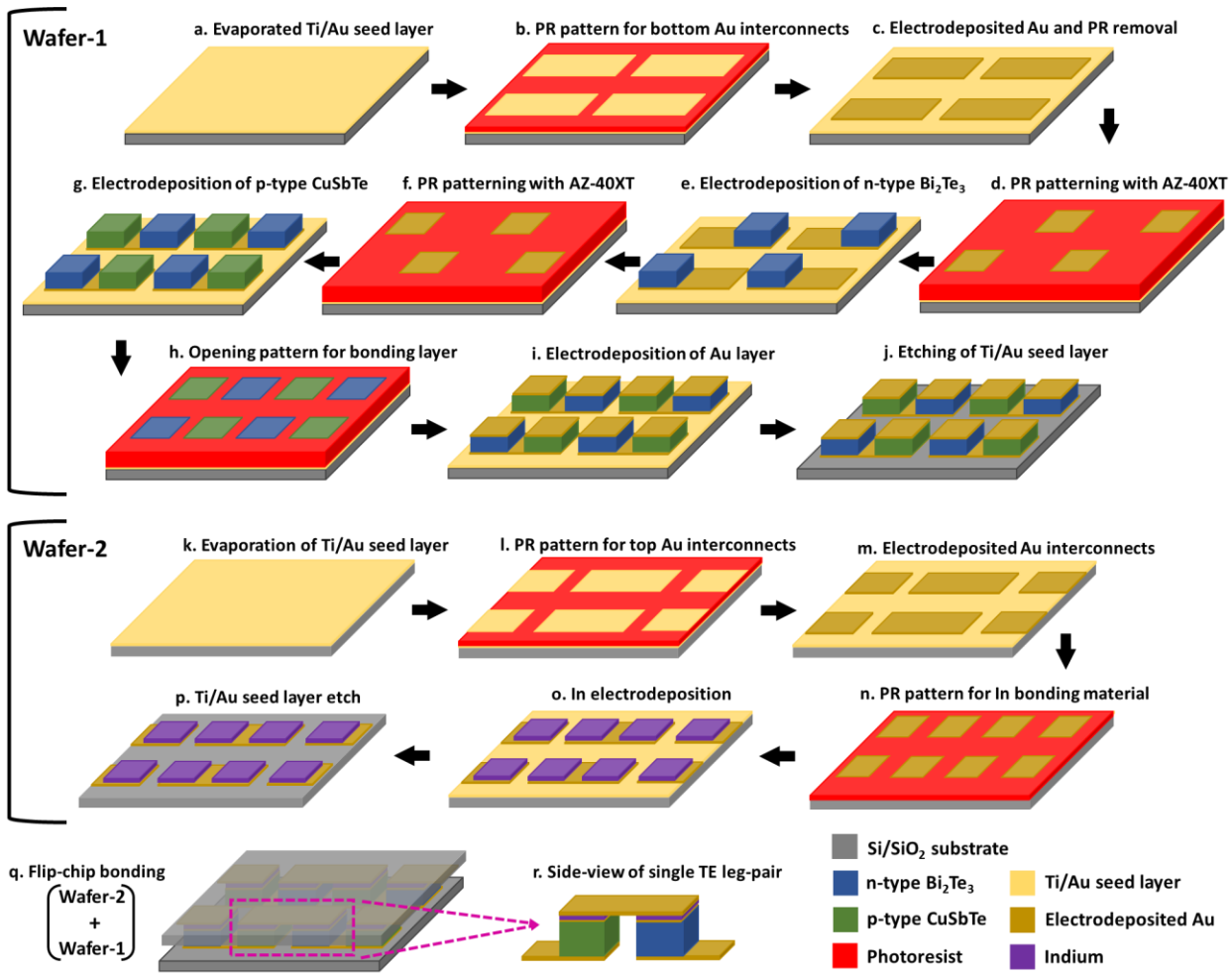

Figure 1. Process flow schematic for the fabrication of micro-TEC device: (a) evaporation of Ti/Au seed layer on wafer-1, (b, c) photoresist (PR) pattern and electrodeposition of bottom Au interconnects, (d, e) PR patterning and electrodeposition of n-type Bi_2Te_3 TE legs, (f, g) PR patterning and electrodeposition of p-type CuSbTe TE legs, (h, i) PR patterning and electrodeposition of Au bonding layer onto n- and p-legs, (j) etching of Ti/Au seed layer on wafer-1, (k) evaporation of Ti/Au seed layer on wafer-2, (l, m) PR patterning and electrodeposition of top Au interconnects, (n, o) PR pattern and electrodeposition of In bonding material, (p) etching of Ti/Au seed layer on wafer-2, (q) final device after flip-chip bonding of bottom and top dies, and (r) schematic of side-view of single leg-pair.

In the next step, a layer of Au is electrodeposited onto both n- and p-legs to serve as a bonding layer in the flip-chip bonding process. This is achieved by using an additional mask to open the target area for Au deposition, as shown in Figures 1(h, i). Finally, one more lithographic step is performed to etch the seed layer of wafer-1. The Au seed layer is then etched using a KI/I_2 solution, followed by the etching of 20 nm of Ti in an HF-based solution (Figure 1(j)).

For the top metal interconnects, the second wafer is fabricated separately. The first three steps (Figures 1(k, l and m)) are similar to Figure 1(a, b and c). First, the Ti/Au seed is evaporated,

followed by the deposition of a thick Au layer after patterning the AZ-10XT photoresist. In the next step, the target area is opened to deposit the bonding material Indium (In), as shown in Figure 1(n), using AZ-10XT photoresist and AZ 400K developer. A commercial indium sulfamate plating bath (Indium Corp.) is used for the electrodeposition of In using an In sheet as the counter electrode. A constant current density of 16 mA cm^{-2} is used to electrodeposit the In layer, and then PR is removed in acetone, as shown in Figure 1(o). Afterwards, one last lithography step is performed to etch the Ti/Au seed layer. Figure 1(p) shows wafer-2 after the seed layer etch.

For the flip-chip bonding process, both wafers are diced into individual device dies. The die-to-die attachment is performed using a FineTech flip-chip bonder, with Au/In/Au bonding, as shown in Figure 1(q). It allows TE legs to form a daisy chain of π-shaped leg-pairs. Figure 1(r) represents the side-view of a single TE leg-pair.

3. Thin film materials and device characterizations:

The morphology of the electrodeposited materials is investigated using a scanning electron microscope (SEM) (Quanta FEG 450) at an accelerating voltage of 20 kV, and their chemical composition is analyzed using an energy-dispersive X-ray spectrometer (EDX) attached to the SEM. XRD patterns of thin films are attained using a PANalytical X'pert Pro with Cu Kα radiation (λ=1.54 Å). The thickness of the materials is measured by a KLA Tencor P-17 stylus profilometer. The Seebeck coefficients of the n-type Bi_2Te_3 and p-type CuSbTe films are measured in the in-plane direction using a laboratory-built system [35]. The electrical conductivity is measured and calculated using the four-point probe method. An infrared camera (FLIR X6540sc) is used to capture surface temperatures to test the device's cooling performance.

Results and discussion

1. Thermoelectric characterization of thin films:

The cyclic voltammetry (CV) is carried out to investigate the reduction potential of Bi_2Te_3 and CuSbTe electrolytes. A standard gold electrode of radius 1 mm is used as the working electrode for the CV study at a scan rate of 10 mVs^{-1}. The CVs of both electrolytes are shown in Figure S1 of the Supplementary Information. According to the CV in Figure S1(a), a reduction peak at -103 mV and an oxidation peak at +450 mV are observed for Bi_2Te_3. For CuSbTe, the CV in Figure S1(b) displays a reduction peak at around -100 mV and three oxidation peaks at +195 mV, +470 mV and +570 mV. Based on these CV studies, a constant-potential of -85 mV and -115 mV is considered for the co-deposition of Bi_2Te_3 and CuSbTe films, respectively. The SEM images of electrodeposited n-type Bi_2Te_3 and p-type CuSbTe thermoelectric films after annealing are shown in Figure 2. High magnification image of Figure 2(a) inset shows a wire-like morphology of the Bi_2Te_3 film with a dense profile. The SEM images in Figure 2(b) and inset display a smooth and dense structure of the CuSbTe film. The EDX spectra for both films are shown in Figure S2 of the Supplementary Information. According to the EDX analysis, the atomic weight percentages (at%) of Bi and Te are 36.65% and 63.35%, respectively, indicating a near-stoichiometric composition of Bi_2Te_3 film [36]. On the other hand, the EDX analysis of the p-type CuSbTe film yields at% values

of 15.16% for Cu, 28.61% for Sb, and 56.23% for Te, indicating their co-deposition [33]. Both electrodeposited films are found to be in a crystalline nature, as analyzed by XRD. The XRD pattern of Bi_2Te_3 in Figure 2(c) displays the main diffraction peaks at 23.56°, 27.74°, 41.18°, and 50.40° for the (1 0 1), (0 1 5), (1 1 0), and (2 0 5) planes, respectively. The peaks match well with the Bi_2Te_3 rhombohedral phase (JCPDS#08-0027). It reveals that the crystalline structure is highly oriented in the direction of the (1 1 0) plane [35]. In the case of CuSbTe, the XRD diffraction peaks (Figure 2(d)) are visible at 17.38°, 28.33°, 42.62°, and 52°, corresponding to (0 0 6), (0 1 5), (1 1 0), and (2 0 5) planes. The peaks are indexed to the standard rhombohedral crystal structure of Sb_2Te_3, with the $R\bar{3}m$ space group (JCPDS#01-072-1990). The diffraction peak at around 38° corresponds to the Au seed layer in both films.

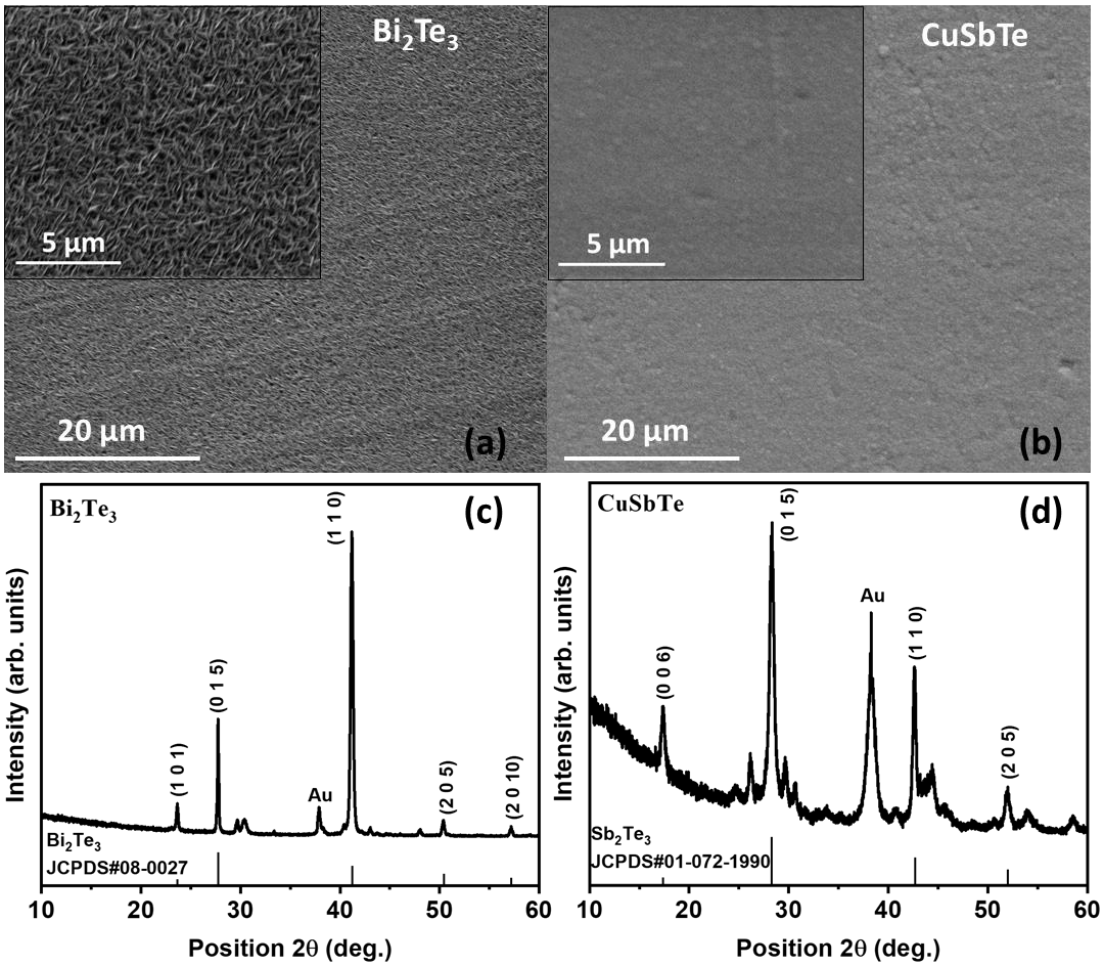

Figure 2. SEM images of the electrodeposited and annealed (a) Bi_2Te_3, (b) CuSbTe films, XRD pattern of (c) Bi_2Te_3, and (d) CuSbTe films.

The thermoelectric properties of both n- and p-type materials are measured at near room temperature. The Bi_2Te_3 and CuSbTe TE films exhibit Seebeck coefficients (S) of -50.6 μVK^{-1} and 29.8 μVK^{-1}, respectively, while their electrical conductivities (σ) are 4.9×10^4 and 9.5×10^4 Sm^{-1}, respectively. The power factor is derived from the $S^2\sigma$ relation, yielding values of 126 and 84

$\mu Wm^{-1}K^{-2}$ for n- and p-type materials. While the n-type Bi_2Te_3 material's performance is reasonable, the CuSbTe power factor is modest as compared to other electrodeposited p-type options, which are compatible with CMOS fabrication processes, as shown in Table S1 of the Supplementary Information. It indicates the requirement of further enhancing the thermoelectric properties of CuSbTe.

2. Micro-TEC device fabrication:

The device fabrication process follows the steps outlined in Figure 1. As discussed earlier, the Si/SiO_2 substrate with an evaporated 20/200 nm Ti/Au seed layer is used for wafer-1. The electrodeposited bottom Au interconnects, with a thickness of around 3 µm, along with their contact pads for electrical connection, are grown. This results in a bottom die size of 4.4 × 4.4 mm^2, as shown in the SEM image in Figure 3(a). With the next two lithographic steps, a 150 × 150 μm^2 area is exposed and developed for the sequential deposition of Bi_2Te_3 and CuSbTe. Before TE leg electrodepositions, the substrate is cleaned with oxygen plasma to remove any remaining photoresist residue and to provide better adhesion of TE materials. The grown TE legs are shown in Figure 3(b). It can be seen that the profile of both electrodeposited legs is not equal in height. This is due to the different growth rates of Bi_2Te_3 and CuSbTe. Not only that, the profile is not uniform across both legs, and the height is lower in the center compared to the edges and corners, as evident from the SEM images in Figure S3 of the Supplementary Information. This occurs due to edge effects during the electrodeposition process, where the current density is higher at the edges than in the center, resulting in rapid growth of the pillars at the edges [28]. Therefore, the wafer has undergone a chemical mechanical polishing (CMP) process to planarize both the TE legs. Before CMP, the wafer is coated with AZ-40XT photoresist to protect the TE legs during the CMP process, which is then removed after the CMP. Figure 3(c) shows the smooth and equal height of Bi_2Te_3 and CuSbTe, which is around 13 µm. Before processing the wafer for the next step, it is annealed at 150 °C for 1 hr in the N_2 atmosphere with a temperature ramp rate of 5 °C per min. Then the wafer is cooled down naturally. A 1 µm thick Au layer is then electrodeposited onto the TE legs, as shown in Figure 3(d), to form the flip-chip Au/In/Au bond in the last step.

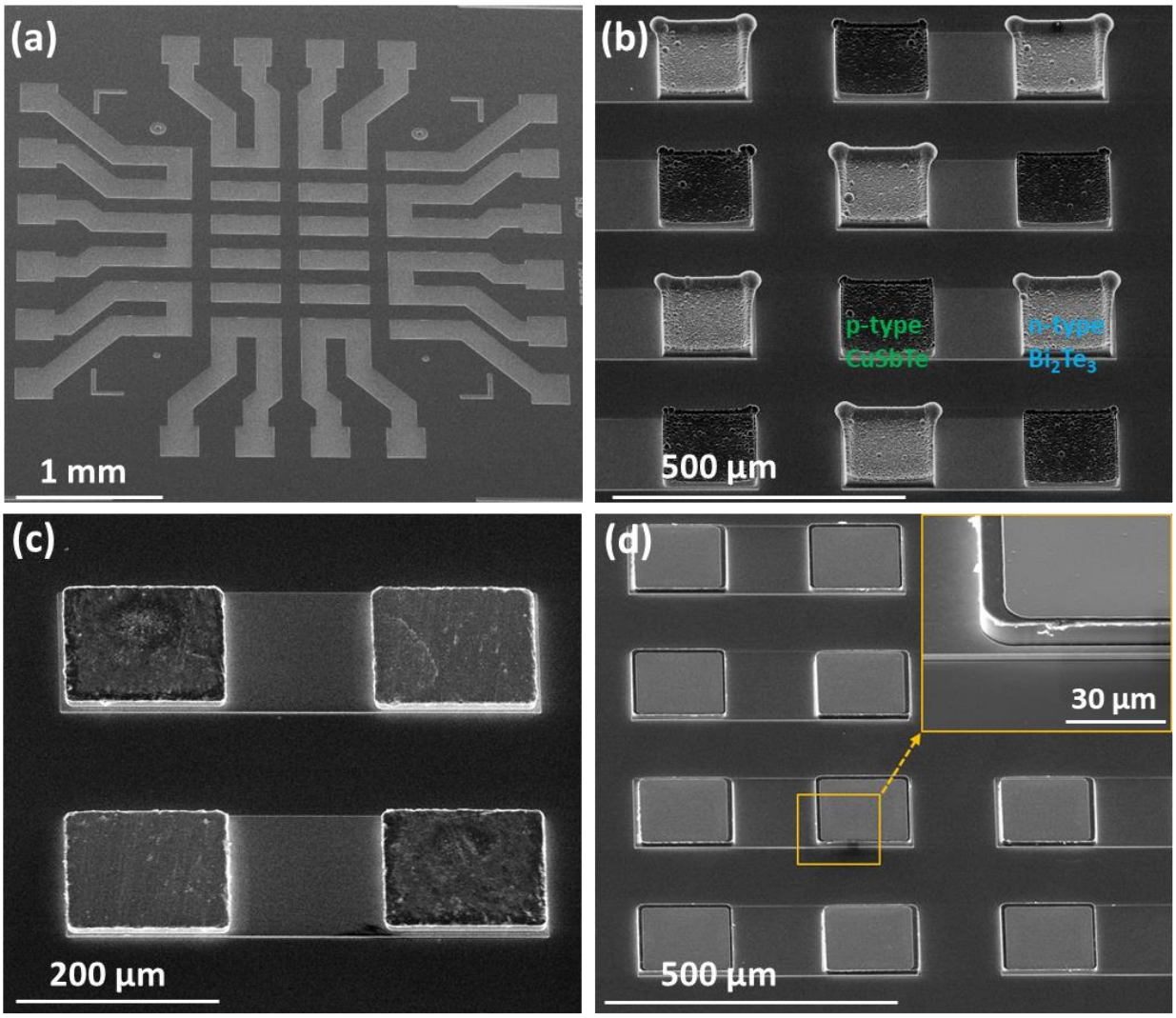

Figure 3. SEM images of (a) electrodeposited Au bottom interconnects and connection pads, (b) electrodeposition of n- and p-type thermoelectric legs, (c) planarized legs after the CMP process, and (d) electrodeposited Au layer on both TE legs, and the inset is a magnified view of a single leg.

The top interconnect for Au/In/Au bonding of the micro-TEC device is fabricated on wafer-2. First, 3 µm thick Au interconnects are electrodeposited, followed by the electrodeposition of In as the bonding material. A thickness of 3±1 µm is achieved for the In electrodeposition. Immediately after that, a thin Au layer of about 50 nm thickness is electrodeposited to prevent the oxidation of In. Figure 4 represents the SEM image of electrodeposited Au and In layers on wafer-2.

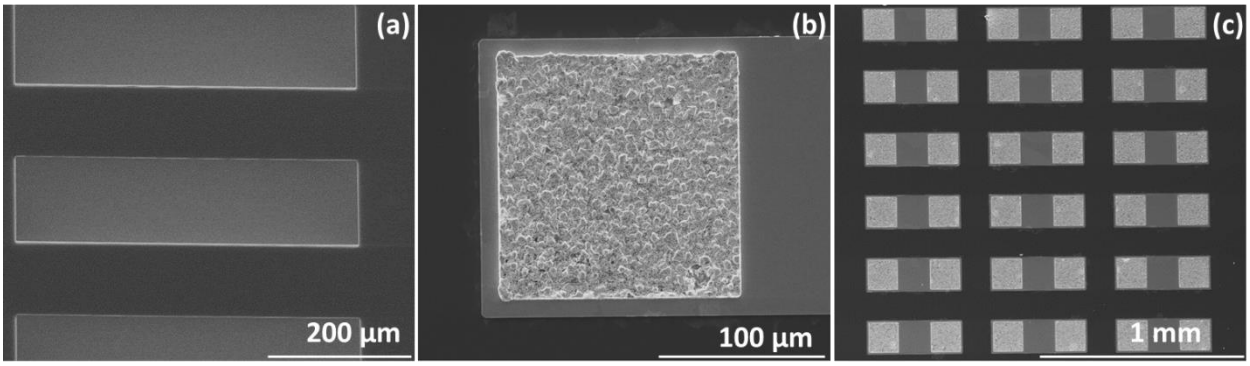

Figure 4. (a) Au electrodeposition for top interconnects, and (b, c) electrodeposition of In bonding material on top Au interconnects.

Both wafers are diced into individual dies before the flip-chip bonding. The area of the top chip is 2.65 × 2.65 mm², which is smaller than the area of the bottom chip (4.4 × 4.4 mm²). During the thermo-compression bonding process, a bonding force of 2.5 N is applied for 120 sec. The bonding occurs at a temperature of 220 °C under a nitrogen (N_2) flow to prevent oxidation of the In bonding material. Figure 5(a) shows the final micro-TEC device after the flip-chip bonding. The X-ray image is taken to visualize the electrical connection beneath the substrate and identify any overflow of In, which is not visible, as shown in Figure 5(b). The fabricated device consists of a total of 18 leg-pairs made of n- and p-type TE materials. Since each leg-pair is connected electrically in series, the connection pads are designed to allow testing of several single leg-pairs, individual 6 rows, and the full device using the corresponding connection pads, as needed.

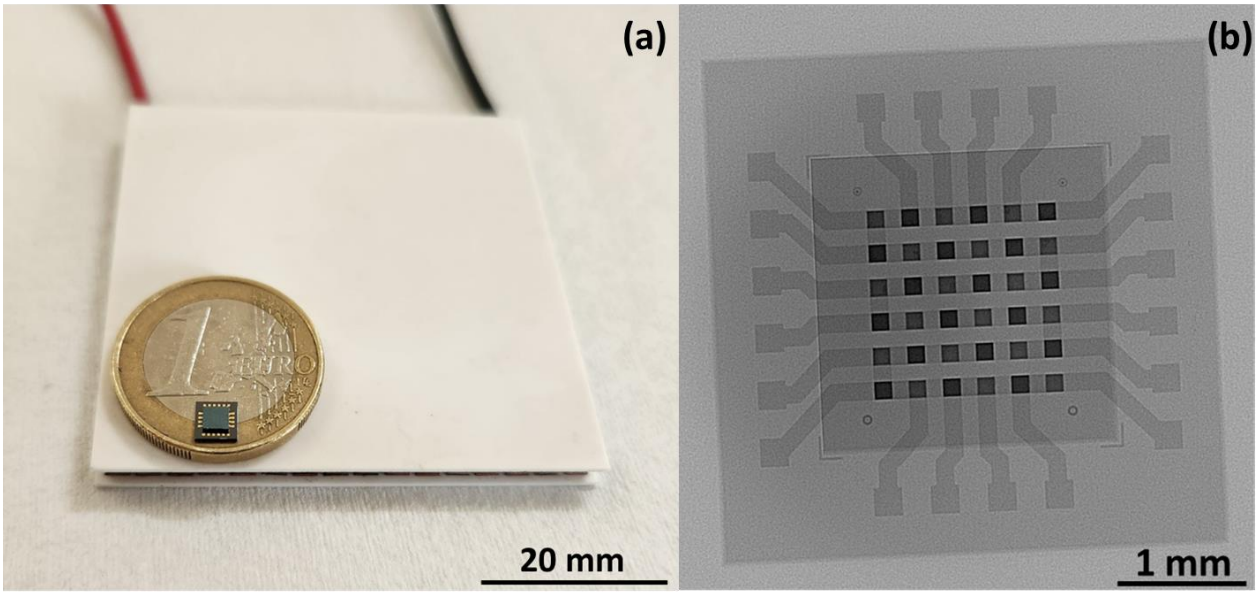

Figure 5. (a) Optical image, and (b) X-ray image of the flip-chip bonded device.

To observe the bonding interfaces, a flip-chip bonded micro-TEC is vertically mounted in a polymer as shown in Figure S4 of the Supplementary Information. The sample is polished for cross-sectional imaging. Figure 6 shows a cross-sectional SEM image of a π-shaped TE leg-pair connected with top and bottom Au interconnects. The inset image is finely polished, highlighting the appearance of a few voids at the Au/In/Au bonding interface formed during the thermo-compression bonding process. These voids are consistent with the Au-In solid-liquid interdiffusion bonding phenomenon. As intermetallic phases ($AuIn_2$/AuIn) form and grow during bonding, uneven merging of the reacting interfaces can leave some voids or gaps [37]. Also, native oxidation on the In bonding material, prior to bonding, can reduce wettability and further promote interfacial voids [38]. The presence of such interfacial voids affects the devices' contact resistance, and thus their performance, which is discussed in the next section.

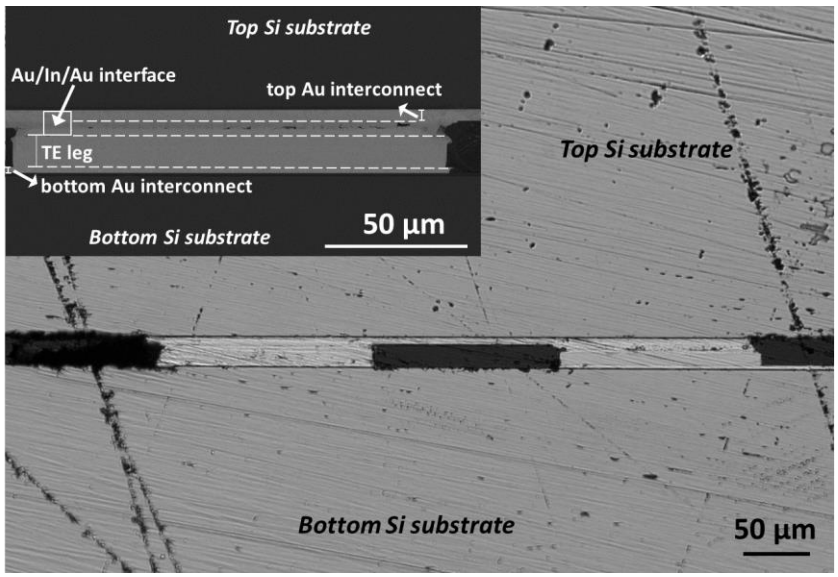

Figure 6. Cross-sectional SEM image of a thermoelectric leg-pair in the flip-chip bonded micro-TEC, and the inset is a magnified view of the Au/In/Au bonding interface of one TE leg.

3. Device characterization:

3.1. Experimental results

To evaluate the thermoelectric cooling performance of the flip-chip bonded device, it is wire-bonded after mounting on a designed PCB board (size: 36.2 × 36.2 mm²), as shown in Figure 7(a). The connecting wires are soldered to supply the current to the micro-TEC device from a DC Power analyzer (Agilent Technologies N6705B). Since the silicon substrate is transparent in the FLIR camera's spectral range (1.5-5.5 µm), black carbon markers are placed on the devices' top and bottom surfaces to provide reliable spatial referencing during infrared thermography. Figure 7(b) shows the connected device placed under the FLIR camera to observe the temperature profile, with the inset showing the carbon markers in place. The entire measurement setup is illustrated in Figure S5 of the Supplementary Information.

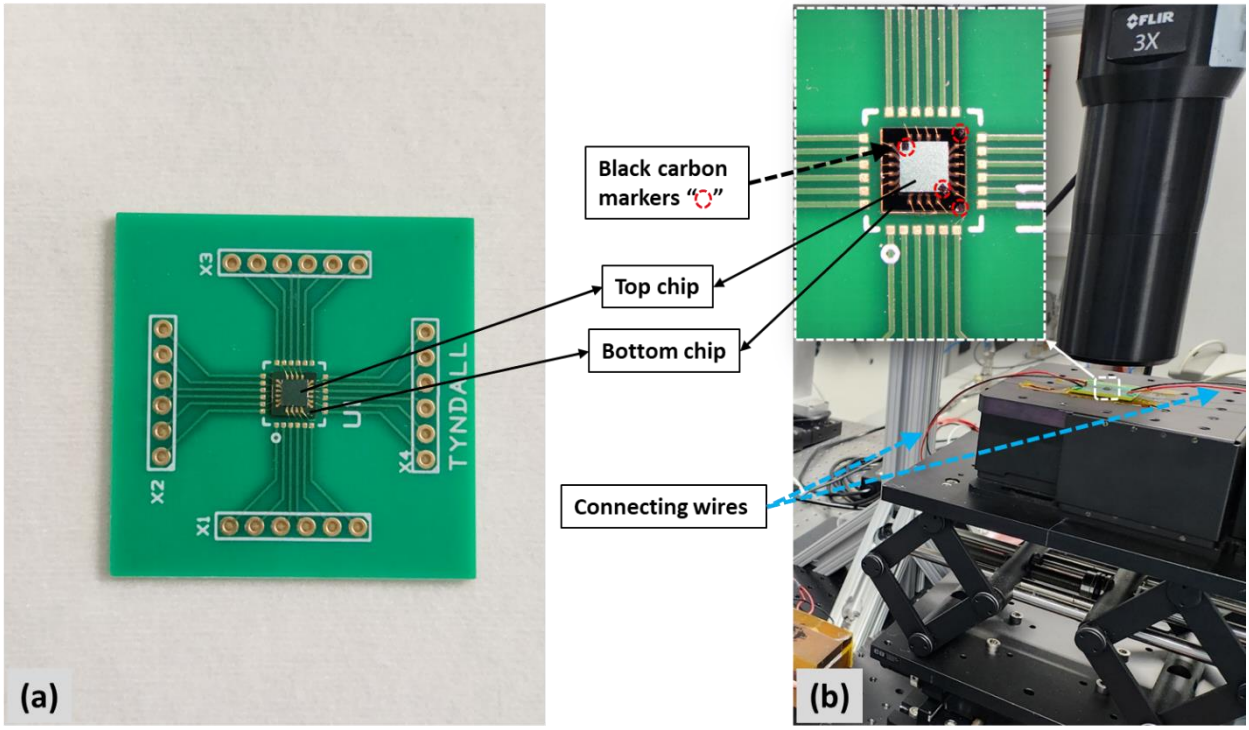

Figure 7. (a) Wire-bonding of a flip-chip bonded device on a PCB board, and (b) device placed under the FLIR camera.

The cooling performance is characterized under zero external heat load at room temperature when a range of currents is applied through the connected wires. Here, the net cooling *(ΔT)* is defined as the average temperature difference between the bottom and top surfaces of the device, as shown schematically in Figure 8(a). During device testing, the hot side is exposed to ambient air, and no additional heat sink is used. Out of a total of 18 TE leg-pairs, only 16 leg-pairs are functioning in this fabricated device, and the device is named Device_1. A second device, i.e., Device_2, is fabricated following the same fabrication process as outlined in Figure 1, but with a higher bonding force of 3.5 N applied during the flip-chip bonding step. Device_2 has 12 working leg-pairs. The measured *ΔT* at different applied currents for both devices is shown in Figure 8(b), represented by solid lines. In both cases, the measured *ΔT* initially increases with current and then decreases as the current is further applied. This behavior is attributed to Joule heating, which becomes significant at higher currents and offsets the Peltier cooling effect, thereby decreasing the *ΔT* [34]. A maximum *ΔT* of 1.2 K is achieved at 100 mA for Device_1 and 0.71 K at 75 mA for Device_2. Figure S6 of the Supplementary Information shows the thermal profile of Device_2 with an applied current of 20 mA. Interestingly, Device_2 is showing lower *ΔT* values than Device_1. The electrical characterization reveals that 16 working leg-pairs of Device_1 give an internal resistance of around 2.06 Ω (average per leg-pair = 0.13 Ω), whereas it is measured to be 0.22 Ω for a single leg-pair in Device_2. Given that both devices have been fabricated using the same TE materials, geometry, and leg dimensions, the calculated electrical resistance of a single leg-pair (based on the material's properties) is around 0.07 Ω. It is therefore inferred that

the remaining resistance arises from contact resistance at the interfaces between the metal interconnects and the TE legs. Based on these values, the contact resistance is estimated to be around 0.06 Ω per leg-pair in Device_1 and 0.15 Ω in Device_2, which is nearly 3 times higher than that of Device_1. Table 1 presents a summary of the results of the two fabricated devices. We hypothesize that this elevated contact resistance in Device_2 contributes to additional Joule heating, which in turn leads to the observed reduction in ΔT compared to Device_1 [39]. Such high contact resistivity is often a result of interfacial defects, such as the formation of native oxide, voids, and cracks, as seen in cross-sectional SEM images (Figure 6). Device_2 is bonded with a higher bonding force, which may have introduced mechanical stress or cracking in the structure, thereby increasing the device's internal electrical resistance. These results underscore the importance of bonding environment and parameters in ensuring the robustness and performance of the micro-TECs.

Table 1. Summary of the obtained results of the fabricated micro-TEC devices.

	Bonding force	Working Leg-pairs (out of 18)	Measured ΔT (K)	Measured average resistance of single leg-pair (Ω)	Calculated resistance of single leg-pair (based on materials properties & dimensions) (Ω)	Estimated contact resistance (Ω)
Device_1	2.5 N	16	1.2	0.13	~0.07	~0.06
Device_2	3.5 N	12	0.71	0.22	~0.07	~0.15

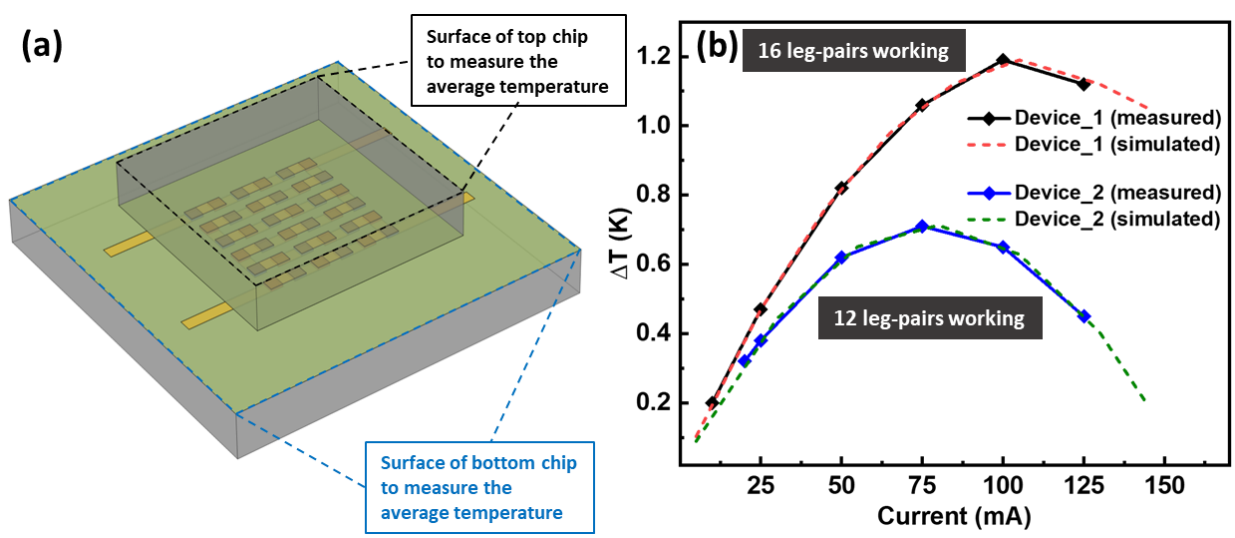

Figure 8. (a) Schematic of a flip-chip bonded device, representing the surfaces to measure the temperature, and (b) ΔT of Device_1 and Device_2 on applying different currents at room temperature.

3.2. Simulation analysis

A thermoelectric model using COMSOL Multiphysics is developed to investigate the performance limitations of the fabricated micro-TEC devices. The three-dimensional governing equations for coupled thermal-electrical relations in steady state are given by [40, 41]:

$$\nabla(\kappa\nabla T) + \rho J^2 - TJ.\left[\left(\frac{\partial S}{\partial T}\right)\nabla T + (\nabla S)_T\right] = 0 \qquad (1)$$

$$\nabla.J = 0 \qquad (2)$$

where, T is the absolute temperature, S is the Seebeck coefficient, ρ is the electrical resistivity, and κ is the thermal conductivity of the thermoelectric materials. J represents the current density vector, expressed as:

$$J = -\sigma(\nabla V + S\nabla T) \qquad (3)$$

where, V is the electrostatic potential. The cooling power (Q_c) at the cold side is described by the standard equation, which is the result of Peltier cooling counter balanced by Joule heating and Fourier heat conduction [40]:

$$Q_c = n\left[ST_cI - \frac{1}{2}I^2R - K\Delta T\right] \qquad (4)$$

where, n is the number of TE leg-pairs, S (=S_p-S_n) is the net Seebeck coefficient (with S_p and S_n for p- and n-type TE legs), T_c is the cold side temperature, and ΔT is the temperature difference. I is the applied electrical current, R (=$\rho L/A$) is the internal electrical resistance, K (=$\kappa A/L$) is the thermal conductance of the device, where L and A are the length and cross-sectional area of the materials, respectively.

For simulations, the model uses the same footprint, 4.4 × 4.4 mm², with TE legs having a cross-sectional area of 150 × 150 µm², which is consistent with the fabricated flip-chip bonded device. Room temperature thermoelectric properties of n-type Bi_2Te_3 and p-type CuSbTe measured in this work are used. The boundary conditions assume the model is thermally isolated except for the hot side of the substrate (fixed at 293 K) and the cold side. Heat loss and thermal contact resistance are neglected, and an extra fine mesh with 6512 elements is employed. Based on governing equations, the simulations indicate that the experimentally obtained ΔT values for Device_1 and Device_2 are only possible when the electrical contact resistivity between the metal interconnects and the TE legs is on the order of 10^{-10} Ω.m². The simulated cooling curves in dotted lines in Figure 8(b) agree well with the measurements and fit the data closely, yielding R^2 = 0.9989 for Device_1 and R^2 = 0.9998 for Device_2. Residuals for both devices are provided in Figure S7 of the Supplementary Information. The residuals vs. current are centred at zero, show no visible trend, and have a small spread. These results demonstrate that the model is consistent with the measured behaviour, confirming its adequacy. However, previous studies have reported ΔT values of 4.4 K [17] and 6 K [42] for micro-TECs with a very low contact resistivity of 10^{-11} Ω.m². These findings confirm that the main limiting factor in the cooling performance of

our micro-devices is higher contact resistivity at the metal-TE material interface. In addition, Table 2 summarizes a comparison of different micro-TECs with our fabricated one based on their aspect ratios (defined as thermoelectric leg height/width) and ΔT values. Since the aspect ratio of our current devices is around 0.09, with square-shaped legs of 13 µm height and of 150 µm side width, we infer that the ΔT of our device can be further improved by increasing the aspect ratio of the thermoelectric legs while simultaneously minimizing the contact resistances.

Table 2. Comparison of measured ΔT of micro-thermoelectric coolers at different aspect ratios.

Ref.	Height of Leg (µm)	Width or Diameter of Leg (µm)	Aspect Ratio (height/width)	Measured ΔT (K)
[43]	4.5	40	0.11	~1.3
[25]	20	60	0.33	2
[44]	5	30	0.17	0.7
This work	13	150	0.09	1.2 & 0.71

To explore geometrical optimization, further simulations are performed on a fully functional micro-TEC device comprising a total of 18 leg-pairs, varying the leg height from 13 to 60 µm, with a constant cross-sectional area of 150 × 150 µm². A low electrical contact resistivity on the order of 10^{-11} Ω.m^2 is considered. The simulated net cooling is plotted in Figure 9(a), which shows an improvement with increasing leg height. Results indicate that ΔT for the 13 µm leg height is improved to 1.83 K, exceeding the measured ΔT of 1.2 K of Device_1, due to the one order of magnitude lower contact resistivity considered in the model. A maximum ΔT of 6.18 K is predicated at a leg height of 60 µm (aspect ratio 0.4), which is higher than the previously reported values for electrodeposited micro-TECs at room temperature [42]. Figure 9(b) illustrates the temperature distribution along the TE legs at a height of 60 µm. As the leg height increases, the thermal conductance, K ($=\kappa_p A_p/L_p + \kappa_n A_n/L_n$; where the indices p and n refer to p-type and n-type TE legs), decreases. It minimizes heat flow from the hot side back to the cold side and thereby improves the ΔT [27]. At the same time, longer legs also introduce higher electrical resistance, R ($=\rho_p L_p/A_p + \rho_n L_n/A_n$), leading to higher Joule heating ($=I^2R$), which offsets the device's net cooling. Hence, an optimal aspect ratio is crucial for balancing thermal conduction and electrical resistance to achieve maximum cooling performance.

A mesh sensitivity analysis is also carried out to ensure that the 3D modeling results are independent of mesh resolution and free from numerical artifacts. In this study, three mesh sizes are considered: fine, extra fine, and extremely fine with numbers of elements 2112, 6512, and 28889, respectively. The effect of mesh size on ΔT values for leg heights ranging from 13 to 60 µm is shown in Figure S8 of the Supplementary Information. The results show that ΔT remains nearly unchanged across the different mesh sizes, confirming that the simulation outcomes are stable and not significantly influenced by mesh resolution. While thermal contact resistance is not considered in the main simulations, it can also influence the performance of thin film cooling

devices, though typically to a lesser extent than electrical contact resistance [45, 46]. To assess its impact, we performed additional simulations for a leg height of 60 µm, considering literature values of thermal contact resistance at interfaces ranging from 1×10^{-10} to 5×10^{-5} $m^2.K.W^{-1}$ [46, 47]. As shown in Figure 9(c), simulated ΔT is greatly unaffected when the thermal contact resistance is below 1×10^{-7} $m^2.K.W^{-1}$, but higher values significantly reduce the net cooling. Therefore, for practical micro-TEC applications, the thermal contact resistance should be maintained below ~10^{-7} $m^2.K.W^{-1}$ to achieve high cooling performance, which is consistent with previously reported values [17].

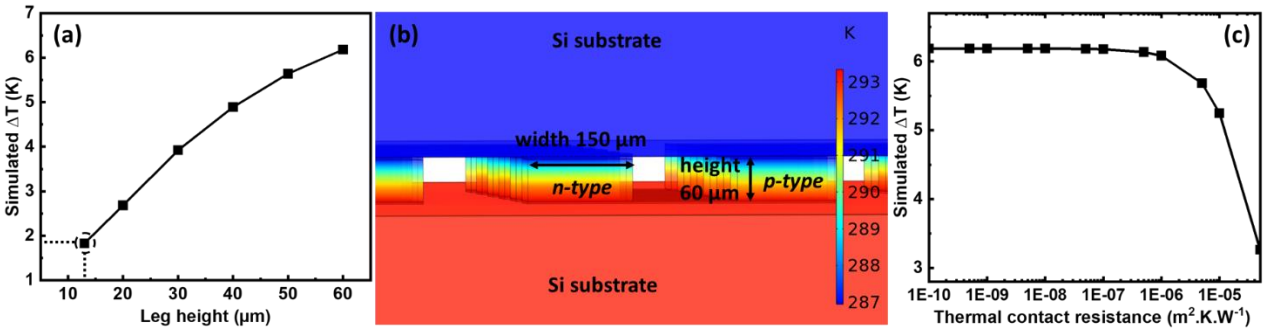

Figure 9. (a) Simulated net cooling of the full device with variation of thermoelectric leg height, (b) temperature distribution at leg height of 60 µm, and (c) simulated net cooling of 60 µm leg height with varying the thermal contact resistance at interfaces.

4. Future work:

Future development of micro-TEC will focus on two main directions: improving interface quality to minimize contact resistance and ensuring long-term device reliability.

i. First, minimizing contact resistance at the bonding interface remains a critical challenge. Previous studies have shown that incorporating contact layers such as Ti or Co can effectively reduce the electrical contact resistance in Bi_2Te_3 thin films [48, 49]. Additionally, Sn-based solder bumps have been successfully utilized in flip-chip bonding to enhance electrical performance [50]. On the other hand, as shown in Figure S3 of the Supplementary Information, constant-potential electrodeposition to grow thick thermoelectric legs can lead to increased surface roughness, which may degrade the quality of bonding contacts. Pulsed-electrodeposition has emerged as a promising approach to grow thicker (hundreds of microns), uniform, and smoother thermoelectric films [51, 52]. Furthermore, recent studies demonstrate that surfactants or additives (CTAB, SLS, etc.) can also play a key role in controlling morphology [53, 54]. Incorporating such approaches, either individually or in combination, offers a promising pathway to reduce roughness, improve bonding quality, and lower contact resistance in future device fabrication.

ii. Second, while this study focused on room temperature performance, future work will also involve systematic reliability testing, including long-term stability and durability under varying operating temperatures. These evaluations are essential for determining the practical applicability of micro-TECs, particularly in high-density integrated photonic systems where continuous operation and thermal cycling can significantly influence device lifetime.

Overall, future efforts combining advanced fabrication strategies with reliability testing will enable the realization of fully functional micro-TEC devices with lower contact resistance, optimized aspect ratios, and robust stability for on-chip thermal management in next-generation integrated photonic systems.

Conclusions

In this study, flip-chip bonded micro-TEC devices were fabricated on Si/SiO_2 using standard microfabrication techniques. Electrodeposited Bi_2Te_3 and CuSbTe thermoelectric materials were used as n- and p-type legs, respectively, which were connected via Au/In/Au thermo-compression bonding. The 4.4 × 4.4 mm^2-sized devices achieved net cooling of 1.2 K and 0.71 K at room temperature. Also, the impact of contact resistance at the bonding interfaces on cooling performance was investigated. COMSOL-based simulations indicate that increasing the thermoelectric leg height from 13 µm to 60 µm, with low contact resistivity on the order of 10^{-11} $\Omega.m^2$, can improve the net cooling to 6.18 K. The findings suggest that flip-chip bonded micro-TECs with optimized geometry and interfaces are promising for on-chip thermal management of integrated photonic devices.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

This work received funding from Research Ireland and is co-funded under the European Regional Development Fund under Grant Number 12/RC/2276. This work also received funding from the European Union's Horizon Europe research and innovation programme under the grant agreement 101160642. The authors would like to thank Jun Su Lee for the flip-chip bonding, Noreen Nudds for the wire-bonding of devices, Finbarr Waldron for the device's X-ray imaging, and Kamil Gradkowski and Xiuyun He for the IR thermal measurements at the Tyndall National Institute.

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