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Multiphysics design and fabrication of 3D electroplated VIA materials topographies for next generation energy and sensor technologies

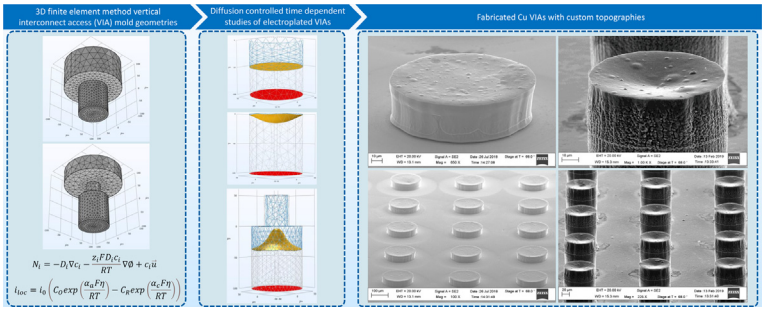
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HIGHLIGHTS

- Novel 3D multiphysics simulations were used to model electroplated Cu vertical interconnect access (VIA) topographies.
- The simulation results revealed that diffusion-controlled mass transport conditions can enable flat, concave and convex Cu VIA topography design options.
- The simulations were validated by a comparative study with fabricated Cu VIA arrays showing a highly positive correlation.
- Flat and concave topographies were achieved at Cu VIA to VIA mold thickness ratios of $\leq$0.5 and $\geq$0.8, respectively.
- Tailored convex topographies enabled by altering the dual layer VIA mold system layer 2/layer 1 width/diameter ratio at values <1.

GRAPHICAL ABSTRACT



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ABSTRACT

3D micro and nanoconductors have emerged as essential components of next generation energy and sensor technologies. This work investigates novel methods to tailor the topography of electroplated 3D conductive components, such as VIAs, using the FEM in COMSOL Multiphysics. This enables meeting the design specifications of flat, convex, or concave substrate-distal electroactive surfaces. Flat conductor surfaces are ideal for microbump soldering and flip-chip fabrication methods and concave/convex designs increase the number of available electrode reaction sites for sensor applications. 2D/3D multiphysics simulations are performed comprising: (1) electrochemistry modeling with the Nernst-Planck and Butler-Volmer formulations for mass transfer and reaction kinetics, and (2) a deformed geometry physics module to track the growing electrode during electrodeposition. Simulation results are compared to directly corresponding experimental work, with positive correlation. Our findings enable tailored and scalable electroactive surface processing options, which can be readily integrated into pre-existing research and industry standard operating procedures.

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1. Introduction

Electroplating enables materials deposition onto or into a substrate with tight control over various parameters such as surface functionalization (e.g., electrical, thermal and magnetic properties), specified deposit thicknesses (e.g., micro–macro scale) and tailored design topologies (e.g., by selective deposition) [1,2,3,4,5,6,7]. In addition to its versatility, electroplating is high-throughput and often entails inexpensive process requirements, qualities which have made it an indispensable component of modern R&D and industry processing lines [8]. This has significantly broadened the design space of materials engineering for energy and sensor technologies in domains ranging from power electronics to quantum computing, neurotechnology, space and the internet of things (IoT). Example applications include integrated voltage regulators [9], superconductors [10], neural implants [11], thermoelectric generators [12] and various devices in micro/-nanoelectromechanical systems (MEMS/NEMS) [13].

As demand increases for next generation micro/nano-devices with reduced form factors, enhanced efficiency and improved power density, effective predictive modeling of the electroplating process is needed to enable key technological advancements in this area [14]. Unlocking the potential of next generation devices requires effective implementation of electroplated 3D conductors, otherwise known as vertical interconnect access points (VIAs) [15,16]. VIAs use the z-axis to minimize device footprint and thereby enable unprecedented metrics for performance and versatility through increased granularity and point-of-load (PoL) power delivery, all of which are key longstanding goals of integrated magnetics research [9,17,18,19,20,21,22,23,24,25]. For example, researchers at Intel Corporation (CA, USA) recently reported microinductors with magnetically enhanced VIAs that achieve best in class: performance (e.g., quality factor), energy and current density, and saturation current [26]. Additionally, VIAs are essential for wafer level vacuum packaging (WLVP), wherein they are used as input/output (I/O) interconnects that reduce the packaging cost and footprint of various vacuum sealed MEMS/NEMS devices by as much as 10x [13].

VIA topography specification is expected to become an increasingly important design option in emerging next generation micro/-nano devices. Flat conductor topographies are needed for interlayer matching in advanced 2.5D and 3D flip-chip architectures [13] and concave and convex designs increase much-needed electrode surface area for sensor applications [27]. For example, the surface area of micropillar area electrodes (μAEs) was shown to be proportional to their voltammetric response (e.g., current density) [28,29] and the sensitivity of μAEs was reported to be 1.5× greater than a competing planar electrode, notwithstanding a 40% smaller footprint [27]. Moreover, HAR nano-pillars can significantly increase the mass loading effect in surface acoustic wave (SAW) sensors [30].

Porous electrode designs hold promise to significantly increase the electrode surface area, however several technical challenges need to be addressed such as process development for uniform pore size/distribution, defect-free lattice filling/electroplating and the development of novel porous materials by, for example, implementation of advanced lithographic techniques to pattern 3D materials [31,32,33]. Flat electrode topographies can be produced with chemical mechanical polishing (CMP), a post processing technique wherein an electroplated overburden is planarized with a corrosive slurry and an abrasive polishing pad. CMP is known to have many process constraints however, such as introducing radial etch gradients (nonuniformity), limited sample size/geometry (due to sample slotting), incompatibility with island-like device topologies (due to edge lapping), incompatibility with high aspect ratio (HAR) features (due to sheer forces), inducing bulk film stress (due to compressive/sheer forces) and introducing contaminants into complementary metal oxide semiconductor (CMOS) compatible process flows (e.g., metal ions) [34].

We identify that mathematical modeling of 3D electroplated VIA topographies could potentially reveal a new simple method to enable the flat, concave and convex topography design options. This new method would be inexpensive, high-throughput and easily integrated into standard electroplating procedures. Furthermore, it would increase the design space for next generation micro/nano devices and emerging 2.5D/3D advanced electronics packaging architectures. Therefore in this study, we investigate predictive modeling of electroplated 3D conductors with a focus on electroformed VIA topographies (surface profiles). Cu was selected as the material of focus in this study as it is the most common VIA material due to its low resistivity (only the more costly Au and Ag have a lower resistivity), resistance to electromigration and high heat transfer coefficient [13,35,36,37]. Furthermore, Cu is known to be mechanically robust with an elastic modulus of 130 GPa, which adds to its compatibility with emerging advanced packaging architectures [38,39].

Ubiquitous in the semiconductor industry, electroplating Cu into wafer scale photoresist (PR) molds is a high-throughput technique that can be readily utilized to fabricate VIA arrays. In the effort to advance understanding of the complex VIA electroplating process, various Cu electrodeposition simulation methods have been reported in the literature. Simulations fall into two main categories: (1) continuum models that use partial differential equations to express physical quantities (e.g., charge, concentration, momentum) as continuous variables (e.g., using mesh boundaries) [40,41,42,43,44,45] and (2) molecular resolution models that implement ions and molecules as discrete particles or groupings of particles in a stochastic process (e.g., the kinetic Monte Carlo (KMC) method) [46,47,48,49,50]. Due to the large amount of computational resources required, many KMC methods include elements of continuum theory to enable multiscale modeling (e.g., angstrom to microscale) with a realistic time frame [51].

Superconformal electroplating is a key focus in the literature, wherein the dynamic interaction of accelerators, suppressors and levelers is investigated to enable void-free plating of Cu trenches and VIAs [46,47,52,53,54,55,56,57,58,59]. This type of plating simulation has gained popularity due to (1) the well-known damascene process that uses a conformal seed layer on topographically complex substrates and (2) the difficulty of plating HAR through substrate (or silicon) via (TSV) molds comprising a significant differential in the localized electroactive species concentration along the TSV axial length [60].

Much less attention has been given to bottom-up electroplating simulations of Cu trenches and VIAs, wherein the sidewalls are electrically insulated [60,61,62,63,64]. This processing option is emerging as an essential feature of various advanced electronics packaging architectures, in part due to the significant added benefit of circumventing current crowding at the trench/VIA entrance and thereby negating the "pinch-off" effect that results in plating voids [60,64]. Reported bottom-up simulations use 2D geometries to (1) demonstrate void-free electroplating of Cu VIAs [60,63], (2) explore the deposition rate as a function of accelerator concentration [64], and (3) investigate electroformed Cu VIA topographies (e.g., roughness and gradient) as a function of AR [62], leveling agent concentration and the mold wall to substrate angle [61]. The Cu VIA topography was shown to progress from flat to concave as a result of an increasing VIA to mold thickness ratio [61,62]. This is due to vertically collimated Cu^{2+} diffusion streamlines combining with radial Cu^{2+} diffusion streamlines as the electrodeposit approaches the mold boundary, wherein the concavity can be reduced or even somewhat inverted by increasing the leveler

concentration or changing the mold wall to substrate angle [61] or AR [62].

Herein we propose for first time, 3D bottom-up electroplating simulations, inclusive of experimental verification, to enable an effective methodology to achieve flat, concave and convex topography design options for circular VIA geometries, the most common VIA shape [13,35,65]. We implement an additive-free continuum model in COMSOL Multiphysics using the finite element method (FEM) to enable fast-converging (non-axisymmetric compatible), μm scale 2D and 3D DC simulations (e.g., 200 × 200 × 200 = 6,2 80,000 μm^3), wherein the dimensional size was selected to align with the typical interposer thickness in emerging 2.5D advanced packaging architectures [13]. We investigate the influence of various diffusion-controlled mass transport conditions (no advection) and we fix the VIA mold AR at 1 (e.g., thickness/diameter) and the mold wall to substrate angle at 90° to focus on simple processing options for flat and concave topographies. Whilst we fix the VIA mold AR at 1, we present the herein discussed electroformed topography trends as dimensionless quantities for broad application to various mold geometries. Finally, we propose a novel mold geometry to produce highly convex Cu VIA topographies and provide a suitable corresponding fabrication method. In this work, we propose a simple electroplating methodology to enable tailored surface topography processing options, which can be readily integrated into research and industry standard operating procedures (SOPs).

2. Experimental

2.1. The copper sulfate electrolytic cell

Continuum electroplating models comprise two main fundamental equations for mass transfer and reaction kinetics. Mass transfer entails physically moving the electroactive species from anode to cathode, whereupon the reaction kinetics take over to form an electrodeposit. This is depicted in the copper sulfate electrolytic cell in Fig. 1 and the corresponding equations are discussed in section 2.2.

When electroplating Cu VIAs for example, the cathode can comprise from the bottom upwards: a Si substrate (e.g., thickness (T) = 525 μm for a standard 100 mm diameter wafer), a thermally grown $Si0_2$ layer that functions as a diffusion barrier (e.g., T = 250 nm), a Ti adhesion layer (e.g., T = 20 nm), a sputtered electroactive Cu seed (e.g., T = 100 nm) and a photoresist patterned with a VIA mold array (e.g., T = 100 μm). Example anodes are Cu pellets housed in an inert electrically conducting mesh receptacle or a solid Cu substrate with dimensions similar to the cathode. Electroplating begins when the patterned cathode is placed in a wafer holder and submerged into the copper sulfate electrolyte, whereupon an external voltage should be immediately applied to ensure a sufficient overpotential so that the Cu seed does not etch. Reduction of Cu^{2+} occurs at the cathode, which creates a faradaic current that corresponds to electrons moving in the external circuit. To avoid rough plating topographies and discontinuous VIA cross-sections, it is essential to specify a sufficient electrochemical cell current to establish a reasonable electroplating current density. For example, the Cu electroplating current density in a sulfuric acid electrolyte is typically in the range of 2–8 $A{\cdot}dm^{-2}$, wherein the plateable surface area may be calculated from the photomask layout [66].

2.2. Fundamental equations

2.2.1. Nernst-Planck mass transport

As shown above, mass transfer entails components for diffusion, migration and advection. Diffusion occurs when a substance moves along a concentration gradient. Migration occurs when an electroactive species moves in response to an electric field and advection results from pumping, stirring or otherwise agitating the

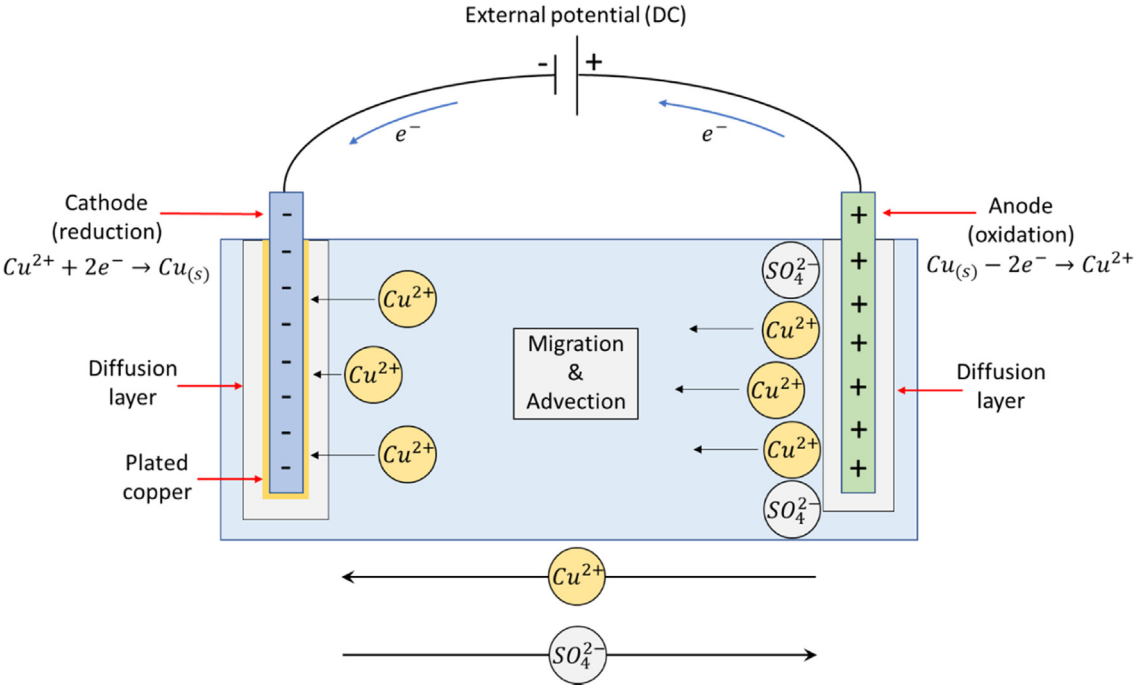


Fig. 1. Copper sulfate electrolytic cell. An external potential is applied across the electrodes to induce oxidation at the anode and reduction at the cathode. Once ionized to Cu^{2+}, the electroactive species first traverses the anode diffusion layer, then the bulk solution via migration and advection, and then finally the cathode diffusion layer. The reaction is 1:1 for reactants to products and requires a two-electron transfer.

electrolyte. A formula that accounts for these factors is the Nernst-Planck equation for mass transport, as shown in (1) [67].

$$N_i = -D_i \nabla c_i - \frac{z_i F D_i c_i}{RT} \nabla \varnothing + c_i \overrightarrow{u} \quad (1)$$

N_i is the overall transport vector for the ith electroactive species in units mol·m^{-2}·s^{-1}. The first factor describes diffusion, which entails D_i, the diffusion coefficient in m^2·s^{-1} and ∇c_i, the concentration gradient with units of mol·m^{-4}. The second factor accounts for migration, where z_i is the unitless ionic species charge, F is Faraday's constant in C·mol^{-1}, R is the ideal gas constant in J·mol^{-1}·K^{-1}, T is in K and $\nabla \varnothing$ is the field potential gradient in V·m^{-1}. The last factor comprises a flow term, $\overrightarrow{u}$ in m·s^{-1}, for the advection condition. The corresponding physics module in COMSOL Multiphysics that accounts for all three mass transport mechanisms is the Tertiary Current Distribution (TCD) module, which is later described.

2.2.2. Butler-Volmer electrochemical kinetics

The governing redox kinetics equation is the Butler-Volmer formula (2) [67].

$$i_{loc} = i_0 \left(C_O exp\left(\frac{\alpha_a F \eta}{RT}\right) - C_R exp\left(\frac{\alpha_c F \eta}{RT}\right) \right) \quad (2)$$

The localized electrode current density, i_{loc} in units of A·m^{-2}, is local in the sense that it varies across the electrode topography. This is an essential quality, as it enables simulating complex 2D and 3D electrode growth by factoring in local deviations in the reaction kinetics with a resolution proportional to the geometry mesh size. As this is a redox equation, it comprises two parts, one for oxidation at the anode (left) and another for reduction at the cathode (right). The exchange current density coefficient, i_0 in A·m^{-2}, is the electrochemical cell current density at zero overpotential. The dimensionless factors C_O and C_R are fractions of the time-sensitive oxidized and reduced electroactive species concentrations to the respective reference concentrations at t = 0. The dimensionless anodic and cathodic transfer coefficients are α_a and α_c, respectively. The overpotential is η in V $(E - E_{eq})$, and all other parameters are as previously described.

Inserting C_O and C_R into this equation is optional, but doing so forces concentration dependent kinetics, which is essential to accurately model VIA electroplating. This is true even in the case of a perfectly stirred bulk electrolyte providing a quasi-infinite number of electroactive specie at the diffusion layer due to a two-part mass transport mechanism comprising: (1) advection streamlines being unable to penetrate deep into VIA molds, forcing diffusion-controlled mass transport [43,68], as shown in Fig. 2a, and (2) electroactive specie with low diffusion coefficients traversing elongated streamlines inside HAR VIA molds, as shown in Fig. 2b. This results an ion scarcity at the electrode–electrolyte interface, which must be accounted for in the corresponding kinetics equation.

2.3. Solver settings

COMSOL Multiphysics FEM simulations first require drawing a geometry, then inputting numbers and settings into a set of discrete physics modules, and then finally performing a multiphysics study, which is typically either stationary (steady-state) or time-dependent. The simulation VIA mold geometry and the physics modules are presented in Sections 2.3.1 and 2.3.2–2.3.3, respectively. A summary of the simulation parameters is given in Section 2.3.4.

2.3.1. VIA mold geometry

Using 2D geometry is a great starting point for 3D simulations, as it simplifies troubleshooting in complex 3D meshes and establishes a reference point to which 3D results can be compared. Several meshed geometries are shown in Fig. 3.

As shown in Fig. 3, the FEM breaks up a simulation geometry into a continuous set of discrete areas (pixels) in 2D and volumes (voxels) in 3D, each of which is demarcated by a set of boundaries. The boundaries are fitted to a fundamental shape, which is typically a triangle in 2D and a tetrahedron in 3D. As an example, and for these shapes, each discrete finite element has three boundaries in 2D and four in 3D. The simulation is computed by solving a set of physics equations at each of the demarcated boundaries in the FEM mesh. The triangle (2D) and the tetrahedron (3D) were selected as the fundamental mesh elements for this work, as these shapes minimize the degrees of freedom (DoF) per finite element and they have been demonstrated to be suitable for standard use with COMSOL's electrodeposition module, wherein a significant amount of literature has been reported [40,41,69].

A key feature of an optimized FEM simulation is a refined mesh, which refers to a control area/volume (e.g., a geometry) filled with appropriately sized finite elements [70]. For example, the simplest mesh comprises finite elements that are similar in size to the geometry, wherein the corresponding simulation would likely be very fast but highly inaccurate. Alternatively, the most complex mesh comprises finite elements that are infinitely small, which in reality is limited by hardware/software capabilities, wherein the corresponding simulation would likely be highly accurate but very slow. Therefore, care must be taken to ensure a sufficiently complex mesh that comprises enough discrete area or volume nodes to accurately model the real-world process with an acceptable margin of error. This is because solver time is a function of the system's DoF, which is proportional to the pixel/voxel count and the magnitude/complexity of the physics equation set. Due to this, accuracy and solver speed are diametrically opposed, wherein effective simulations must find a pragmatic compromise.

Several refined meshes are depicted in Fig. 3, wherein the finite element size is highly variable throughout the geometry, which is due to a significant differential in the level of complexity throughout the control area/volume. In Fig. 3, no significant chemical reaction takes place in the bulk electrolyte and mass transport is relatively simple (e.g., no walls, no advection), therefore it can be filled with the largest finite elements. Conversely, a significant chemical reaction takes place at the cathode and mass transport is relatively complicated (e.g., diffusion along a growing and topographically complex electrode), therefore it should be fitted with the smallest finite elements.

Arriving at a refined mesh entails iteration from a starting point. To produce a refined mesh, one approach is to first use the smallest finite elements possible throughout the entire geometry to arrive at the most accurate solution, and then gradually increase the element size in select locations until the solver is sufficiently fast while remaining highly accurate. This approach is often impractical however, since performing simulations with the maximum DoF could take days, weeks or more depending on the hardware/software and the physics modules being used. Alternatively, a more realistic approach is to first use large finite elements with a fast solving time and then gradually decrease their size in select locations until the solution no longer changes, whereupon experimental work should be performed to verify the result.

When using the refined meshes as shown in Fig. 3a–c, our simulation time was on the scale of minutes. Therefore, the need for cloud or cluster computing can be circumvented with a refined mesh and a suitable up-to-date computer. With regards to hardware, the RAM builds the FEM mesh, the CPU solves the equations and the GPU displays the geometry and enables orientation

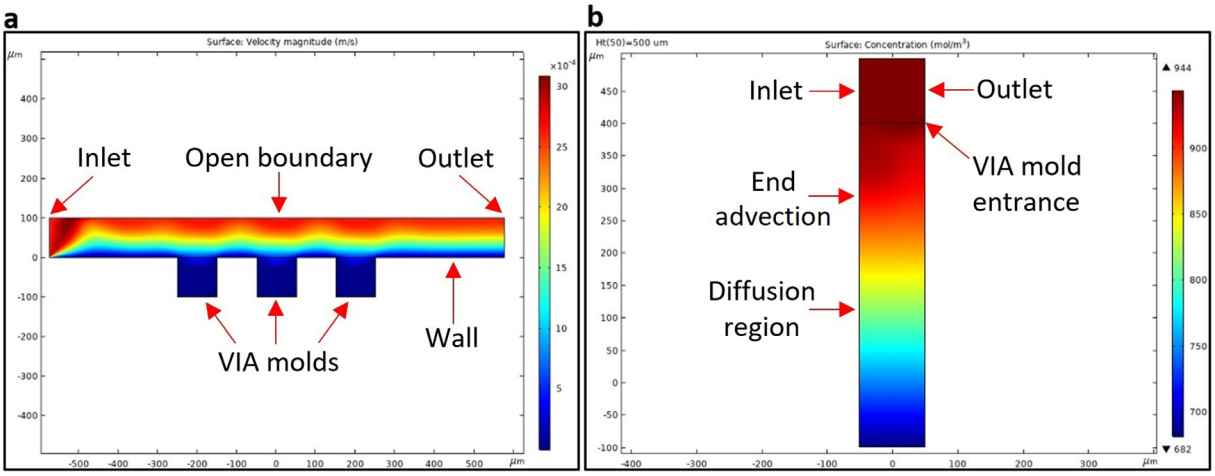


Fig. 2. VIA flow dynamics. a 2D cross-section of three VIA molds, each with an AR of 1, submerged in an aqueous electrolyte (Newtonian) where bulk flow is introduced from the left. The electrolyte is color-mapped according to velocity. The inlet flow speed is 2.62 mm·s^{-1}, which corresponds to a reference half radial point on a 100 mm diameter Si wafer rotating at 1 rpm, as corresponds to our experiments. The flow profile is laminar due to a low Reynolds number (e.g., <5 × 10^5 for a flat plate), where $Re = \rho uL/\mu$ and ρ is the density in kg·m^{-3}, u is the flow rate in m·s^{-1}, L is the characteristic length in m and μ is the fluid kinematic viscosity in m^2·s^{-1} [78]. The flow is pinched on the left boundary due to the inlet boundary condition, which then quickly separates from the substrate due to the fluid's viscosity. The key takeaway is that the flow does not penetrate deep into the VIA molds, whereby mass transport inside the molds does not include an advection term. **b** 2D cross-section of a HAR VIA mold (5:1) with an inlet on the left, an outlet on the right and an open boundary on top. The electrolyte is color-mapped according to concentration and the reference value, 944 mol·m^{-3}, corresponds to our experiments. The horizontal wall was removed from the geometry to induce maximum flow into the VIA mold. The key takeaway is that even in the ideal case wherein the horizontal viscosity component is entirely removed, all advection halts inside the VIA mold around 100 μm down. Beyond this point, elongated diffusion streamlines are present, which significantly reduces the electrolyte concentration at the electrode surface as a function of the diffusion coefficient magnitude.

manipulation (rotating, zooming, etc.). The computer used for this work comprised 16 GB Corsair Vengeance DDR4 2666 MHz RAM, an Intel Core i5-9400F CPU @ 2.9 GHz (6 cores/threads), an Nvidia GeForce GTX1660 Super 6 GB GPU and a Samsung 970 EVO Plus 500 GB SSD (NVMe M.2 form factor).

2.3.2. Physics module 1: Tertiary Current Distribution (TCD)

As previously mentioned, this physics module is compatible with the full Nernst-Planck equation for mass transport. It also supports the Butler-Volmer equation for electrochemical reaction kinetics. As such, the following presents the relevant parameters for these equations as well as the boundary conditions for the corresponding study.

The supporting electrolyte setting was used, whereby the quasi-infinite bulk electroactive species condition was enabled by a small bath loading factor (electroplating area to electrolyte volume ratio) along with excess anode material. This enabled simplification of the redox process to a half-cell reaction comprising the Cu^{2+} reduction alone. The Cu^{2+} ion reduction entails two steps, as shown in (3) and (4) [43,45,71,72].

$$Cu^{2+} + e^- \rightarrow Cu^+ \quad (3)$$

$$Cu^+ + e^- \rightarrow Cu \quad (4)$$

The first step (3) is the rate determining step, which is 1000 times slower than (4) [43,45]. Due to this, the kinetics can be further simplified by using a one electron transfer process.

The Cu^{2+} ion diffusion coefficient in a copper sulfate electrolyte is provided in the literature [71,73] and was also calculated with the Warburg coefficient equation [74] to be 4.12 × 10^{-11} m^2·s^{-1}. The manufacturer's specification sheet was used to calculate the Cu^{2+} ion concentration (944 mol·m^{-3}), which was set as the initial electrolyte concentration as well as the inlet and open boundary conditions. A no flux/insulation boundary condition was specified for all walls.

The electrolyte conductivity of several copper sulfate baths is provided in the literature [44,71,73,75]. The range is highly variable between 5 and 50 S·m^{-1}, implying this parameter is hugely dependent upon the unique composition of the electrochemical bath. To ensure accuracy for this parameter, cyclic voltammetry was utilized to generate impedance plots (Z′ vs. Z″) for 12 test samples from which the average y-intercept was taken as the resistance metric (2.72 Ω), as shown in Fig. 4. Pouillet's law was then used to determine the resistivity, where $r = \rho l/A$ and r is the cell resistance in Ω, ρ is the resistivity Ω·m, l is the length in m and A is the cross-sectional area in m^2, which was then inverted to arrive at the electrolyte conductivity of 5.60 S·m^{-1} [76].

The exchange current density and the cathodic transfer coefficients were taken from the literature, which are 0.5 A·m^{-2} [45,75,77] and 0.5 [45,73], respectively. The bulk electrolyte potential was specified as 0 V vs. the electrode potential of −0.346 V, a common experimental value. Standard temperature and pressure (STP) were used for the temperature and pressure settings and the fluid velocity was zero in all directions to specify diffusion-controlled conditions.

2.3.3. Physics module 2: Deformed Geometry (DG)

The Deformed Geometry (DG) physics module enables specifying a normal mesh velocity on the cathode, and once coupled to the TCD physics module, it can use the local electrode current density as an input to simulate electrode growth. Prescribed mesh displacement was specified as zero in all directions for the substrate and bulk electrolyte geometry boundaries. The vertical walls of the VIA mold were free to deform in the axial direction but not in the normal direction, which was set to zero, as corresponds to electrically insulating PR walls.

After setting up and successfully coupling the TCD and DG physics modules, an electrode growth study could be configured. The main study type was time dependent, however due to the complexity of the multiphysics couple, initial values were established in a stationary (steady state) sub-study comprising a current distribution initialization step for the TCD module.

Once the initial values were established, the time dependent electrode growth simulation could be performed. For the study to converge, it is critically important to enable automatic remeshing

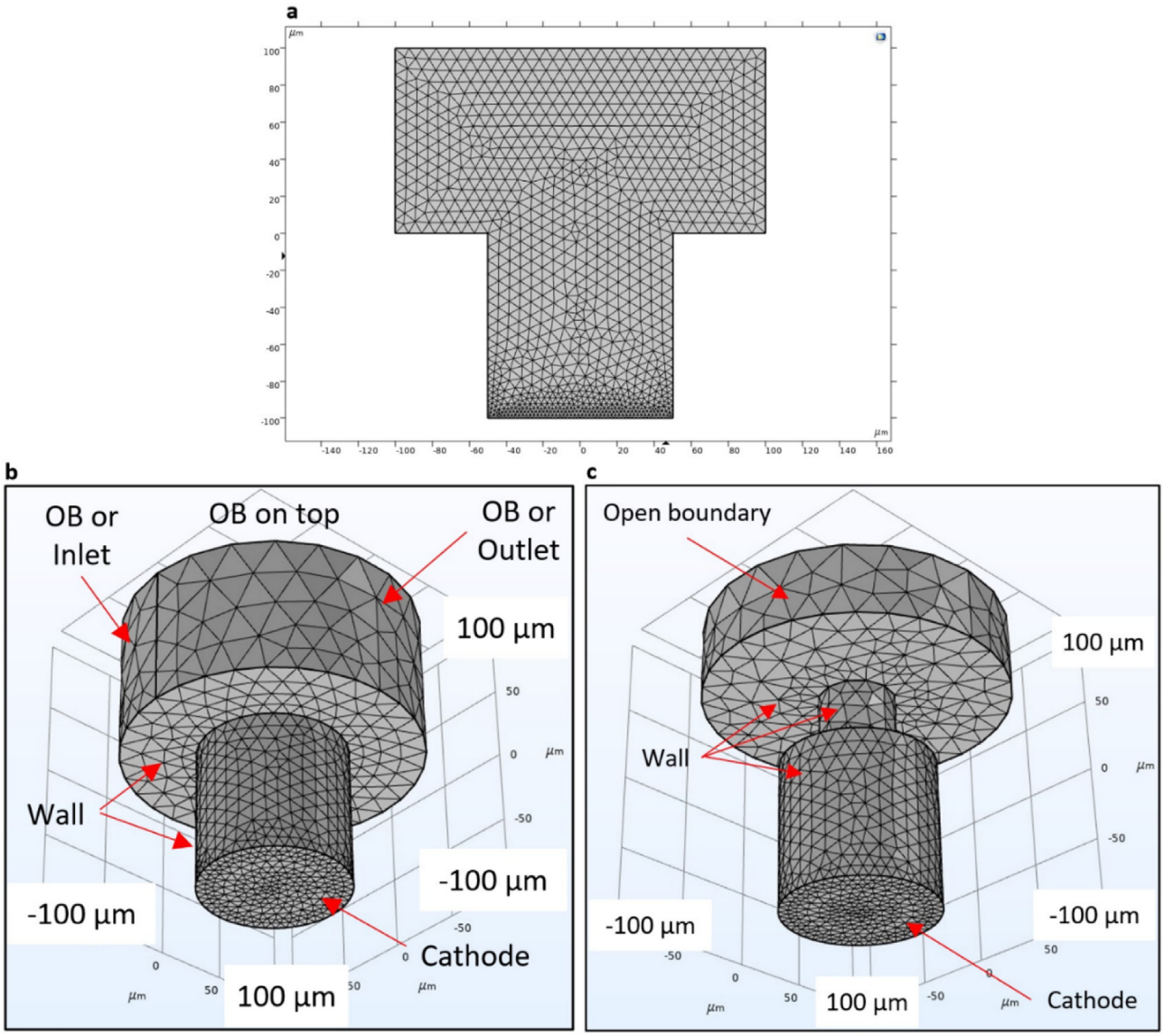


Fig. 3. Solver geometries and FEM meshes. a 2D VIA mold (bottom rectangle, AR = 1) and bulk electrolyte (top rectangle) joined at the internal boundary by COMSOL's Union function. The wall and electrode locations are as previously labeled in Fig. 2. The mesh size is finer everywhere except for the electrode (cathode) boundary, which is extremely fine to enable small local topography changes during electrode growth. **b** 3D version of **a** with a z-axis axis of rotation at (0,0), where OB stands for open boundary. The mesh resolution from the top-down is coarse at the OB (maximum element size (MaES) = 30 µm, minimum element size (MiES) = 5.6 µm), normal at the horizontal PR wall (MaES = 20 µm, MiES = 3.6 µm), finer at the vertical PR wall (MaES = 11 µm, MiES = 0.8 µm) and extra fine at the cathode (MaES = 7 µm, MiES = 0.3 µm). **c** The same as **b**, but with a vertical cylindrical wall added on top of the VIA mold. This forces current crowding at the electrode center, which is demonstrated in section 3.

under the study extension section. This setting monitors the mesh quality as the electrode grows and automatically remeshes the geometry once the mesh quality drops below a user specified value (an example mesh quality expression is provided below). The mesh quality setting is specified under the study → solver configurations → time-dependent solver → automatic remeshing input node. A default mesh quality expression exists in COMSOL, which is a good reference point, however this equation often needs to be optimized to fit each simulation.

A poorly optimized remesh condition results in inverted mesh elements that quickly diverge and terminate the solver. Inverted mesh elements are the result of severe local topographical differences across the cathode that cause the discrete finite elements to not fit together correctly. Specifically, the constitutive equations that are solved on the boundary of the finite elements must not overlap. Typical equations for flow and electroplating simulations are quadratic along the boundary, which results in inverted mesh elements once the mesh becomes sufficiently distorted so that the constitutive equations begin to overlap. Once this happens, the continuity condition across adjacent boundaries is violated and the solver fails. Even with linear constitutive equations, inverted mesh elements still occur on badly deformed meshes.

Arriving at the correct mesh quality expression entails running a simulation on repeat and monitoring when and where it fails, and each time adding or subtracting from the previous mesh quality expression to eventually arrive at a suitable remesh condition. As an example, the optimized mesh quality expression for one of our 3D simulations was comp1.material.minqual-0.03 (the default minus 0.03). This method works best for 3D simulations, however for 2D, the following equation worked best, which is described in an example file in the COMSOL model library: min(comp1.material.minqual-0.2,min(comp1.material.minqual-0.4,min(comp1.material.minqual-0.4,min(comp1.material.minqual-0.4,min(comp1.material.minqual-0.4,min(comp1.material.minqual-0.4,comp1.material.minqual-0.4))))))).

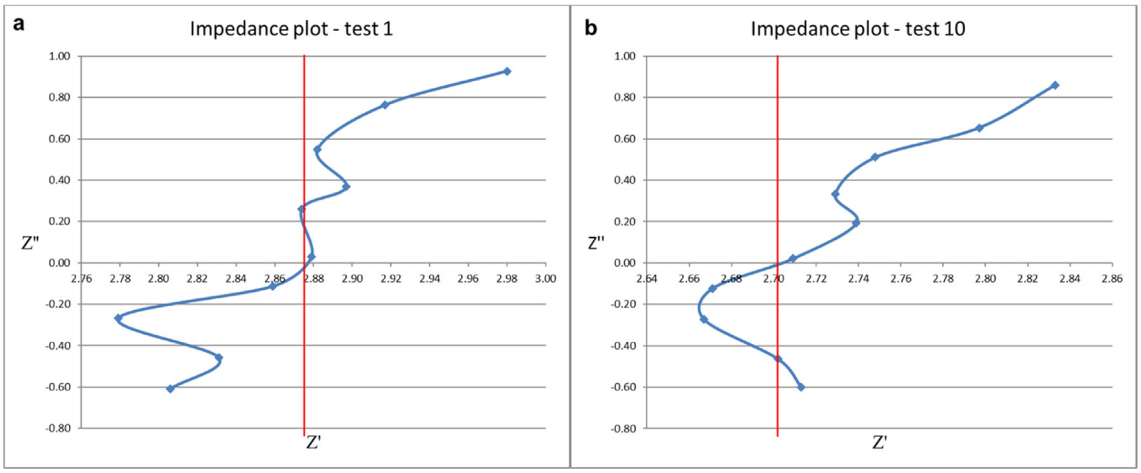


Fig. 4. Example impedance plots for electrolyte resistance determination. a Test 1 of 12, where $Z'' = 0$ is the real part, as marked by the vertical red line. **b** Test 10 of 12. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

In addition to optimizing the mesh quality expression, inverted mesh elements can be reduced by enabling moving boundary smoothing in the prescribed normal mesh velocity node of the DG module. As remeshing is performed, this setting decreases the gradient between adjacent finite elements to lessen their skew. The overall effect is a smoother and more gradual gradient across the growing electrode, which greatly assists in circumventing time consuming remeshing and aids in optimizing new meshes. The default smoothing value is 0.5, which we have reduced by an order of magnitude or more in some cases to increase the effect.

2.3.4. Consolidated simulation parameters

A summary of our simulation parameters is provided in Table 1 below. In addition to the TCD and DG physics modules, these parameters are also compatible with the laminar flow (LF) and moving mesh (MM) physics modules, which can be used to add a unidirectional and a rotating electrolyte crossflow over the VIA mold, respectively, in non-axisymmetric simulations. Furthermore, we expect these simulation parameters could also be suitable for an electro-dissolution study, wherein the opposite of our electrolytic cell voltage could be used.

3. Results and discussion

Simulations were performed with the TCD and DG multiphysics couple, wherein the advection and oxidation terms were omitted from (1) and (2), as corresponds to diffusion-controlled and supporting electrolyte plating conditions, respectively. Flat and concave Cu VIA topographies were first investigated. 3D simulation results were therein compared to 2D results for consistency and then validated with corresponding experimental work, as shown in Fig. 5.

In simulation Fig. 5a and b, the Cu VIA topography is virtually flat at a low VIA to PR thickness ratio (e.g., 0.4–0.5). This result is consistent with the flow streamline analysis in Fig. 2, whereby vertically oriented (e.g., horizontally isotropic) diffusion streamlines deep inside the VIA mold cavity produce a flat electroplated topography. Fig. 5c shows corresponding experimental work that demonstrates a highly positive correlation with Fig. 5a and b, wherein a Cu VIA plated to a similar fraction of the PR thickness (0.40) displays a flat topography (e.g., apparent VIA thickness ≈ 37.27 μm and 37.27/sin(68°) = 40.2 μm vs. 100 μm for the PR).

A limitation of our simulations is sensitivity to minor surface roughness. This is due to use of the moving boundary smoothing setting in the DG physics module, which decreases the gradient between adjacent finite elements to lessen their skew and greatly assists in reducing inverted mesh elements during the simulation process, as previously discussed. The surface roughness in Fig. 5c is due to use of a moderate electroplating current density (e.g., 2.5 $A{\cdot}dm^{-2}$), whereby columns of densely packed diffusion streamlines delivered excess electroactive Cu^{2+} to discrete cathode surface locations, which resulted in localized spherical plating growth inside the VIA mold. This mechanism corresponds to the well-known x-y-z spherical plating growth dynamic that is characteristic of over-plated Cu VIAs protruding into a bulk electrolyte [51]. Notwithstanding minor surface roughness, it is evident that simulation Fig. 5a and b demonstrate a highly positive correlation

Table 1
Multiphysics simulation parameters.

Parameter	Value	Source
Participating electrons, stoichiometric coefficient, chemical species number (half-cell)	1	[43,45,71,72]
Cu^{2+} ion diffusion coefficient	4.12×10^{-11} $m^2{\cdot}s^{-1}$	[71,73,74]
Bulk electrolyte Cu^{2+} ion concentration	944 $mol{\cdot}m^{-3}$	Manufacturer data sheet
Electrolyte conductivity	5.60 $S{\cdot}m^{-1}$	Lab measurements
Exchange current density	0.5 $A{\cdot}m^{-2}$	[45,75,77]
Cathodic transfer coefficient	0.5	[45,73]
Bulk electrolyte potential	0 V	Experiments
Cathode potential	−0.346 V	Experiments
Electrolyte temperature and pressure	STP (293.15 K & 101,325 Pa)	Experiments
Electrolyte density	2286 $kg{\cdot}m^{-3}$	[79]
Electrolyte dynamic viscosity	0.00089 Pa·s	[79]
Bulk electrolyte flow rate	0 or 0.0026 $m{\cdot}s^{-1}$	Experiments
Substrate rotation rate	1 rpm	Experiments

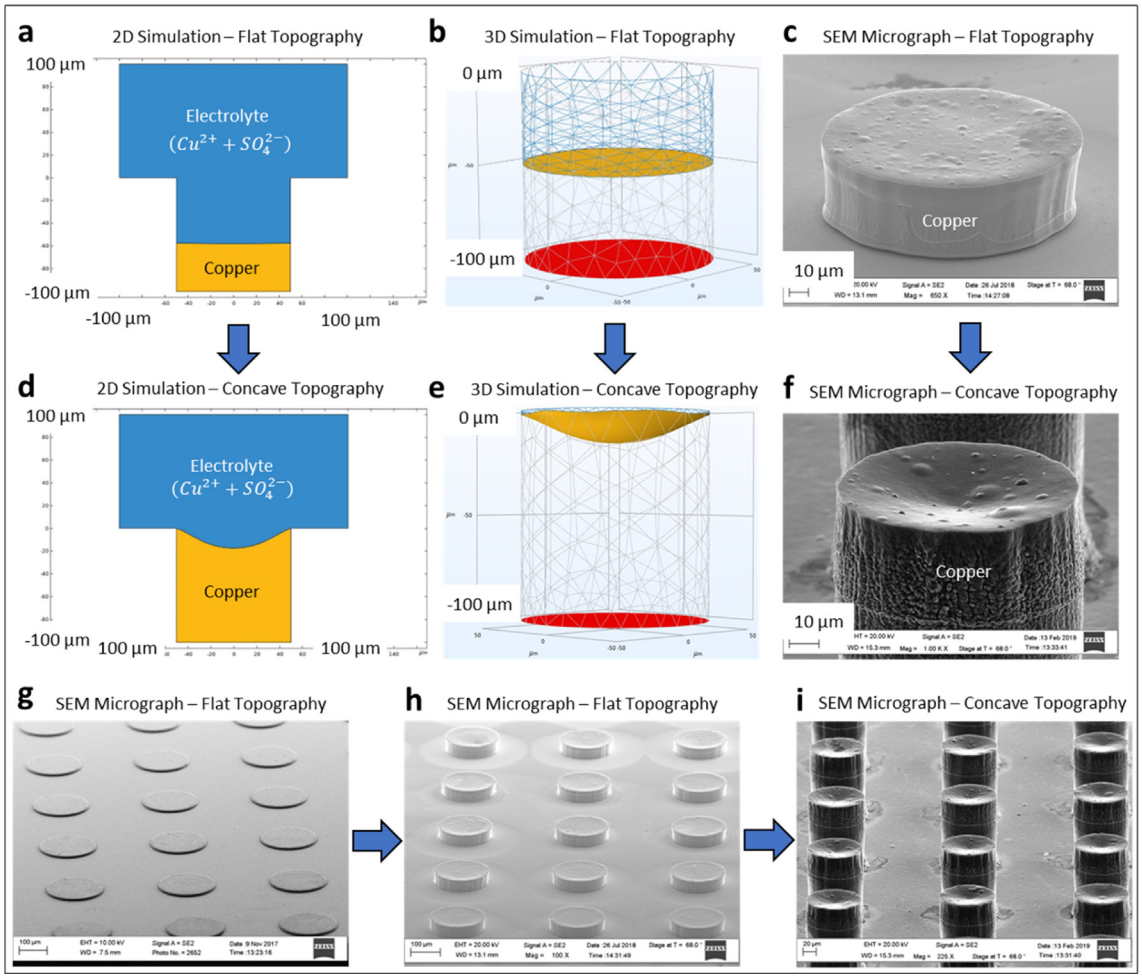


Fig. 5. 2D and 3D simulations with corresponding experimental work for flat and concave VIA topographies. a 2D VIA mold cross-section with an AR of 1. **b** 3D version of **a**, wherein from the bottom-upwards, the red base is the electroplating start point, the grey mesh is electroplated Cu, the gold surface is the Cu VIA topography, and the blue mesh is the copper sulfate electrolyte. **c** SEM micrograph corresponding to simulations **a** and **b**. **d** The same simulation as **a**, but at a later time stamp, wherein the electroplated Cu has just reached the top of the mold cavity. **e** 3D version of **d**. **f** SEM micrograph corresponding to simulations **d** and **e**. **g** Cu VIA array displaying a flat topography, wherein the plating to photoresist thickness ratio was 0.13. **h** Cu VIA array displaying a flat topography, corresponding to **c**, wherein the plating to photoresist thickness ratio was 0.40. **i** Cu VIA array displaying a concave topography, corresponding to **f**, wherein the plating to photoresist thickness ratio was 0.88. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

with the experimental work in Fig. 5c. Therefore, a flat VIA topography is achievable by limiting the electroplated VIA to PR mold thickness ratio.

In simulation Fig. 5d and e, the Cu VIA topography is concave at a high VIA to PR thickness ratio (e.g., 0.8–1). This occurs because very near to the PR mold surface, the electroactive species transport is purely by diffusion, whereby as the electroplated VIA advances toward the VIA mold entrance (see Fig. 2), new horizontal diffusion streamlines add to the pre-existing vertically oriented diffusion streamlines which causes a localized increase in the plating rate at outer radial points of the electroplated VIA. This result is consistent with previous 2D simulations [61,62]. Fig. 5f shows corresponding experimental work that demonstrates a highly positive correlation with Fig. 5d and e, notwithstanding minor surface roughness, wherein a Cu VIA plated to a similar fraction of the PR thickness (0.88) displays a concave topography. Therefore, a concave VIA topography is achievable when the electroplated VIA to PR mold thickness ratio approaches unity.

Fig. 5g–i demonstrate the flat to concave topography transition as the VIA to PR thickness ratio approaches unity (e.g., from 0.13 to 0.88). A specific VIA to PR thickness ratio cutoff metric for the flat to concave topography transition is not herein provided since it is a gradual process that is a multivariable function of the electrolyte composition, plating parameters and the PR mold geometry.

To provide a fabrication processing option for convex electroplated topographies, a smaller columnar VIA mold (PR layer 2) was superimposed on top of the original mold (PR layer 1), as shown in Fig. 6. This mold geometry could be fabricated by modulated exposure of a second thin film after exposing the bottom VIA mold pattern. A single or a dual development process could then be utilized, depending on developer selectivity.

As shown in Fig. 6, the electroplated topography is highly convex at an increasing electroplated VIA to PR mold thickness ratio (e.g., with respect to PR layer 1). This design exploits the result of Fig. 5a–c, wherein an elongated mold geometry forces vertically oriented diffusion streamlines that result in current crowding at the superimposed VIA mold exit (PR layer 2, exit on bottom). Due to this phenomenon, it is expected that the convex electroplated radial height differential could be tailored by altering the PR layer 2 to PR layer 1 width/diameter ratio (ratio < 1). This would enable selection of the electroplated convex slope as a design option. Furthermore, a PR layer 2 to PR layer 1 width/diameter ratio of 1 would enable virtually flat topographies at high electroplated VIA to PR layer 1 thickness ratios, wherein this design

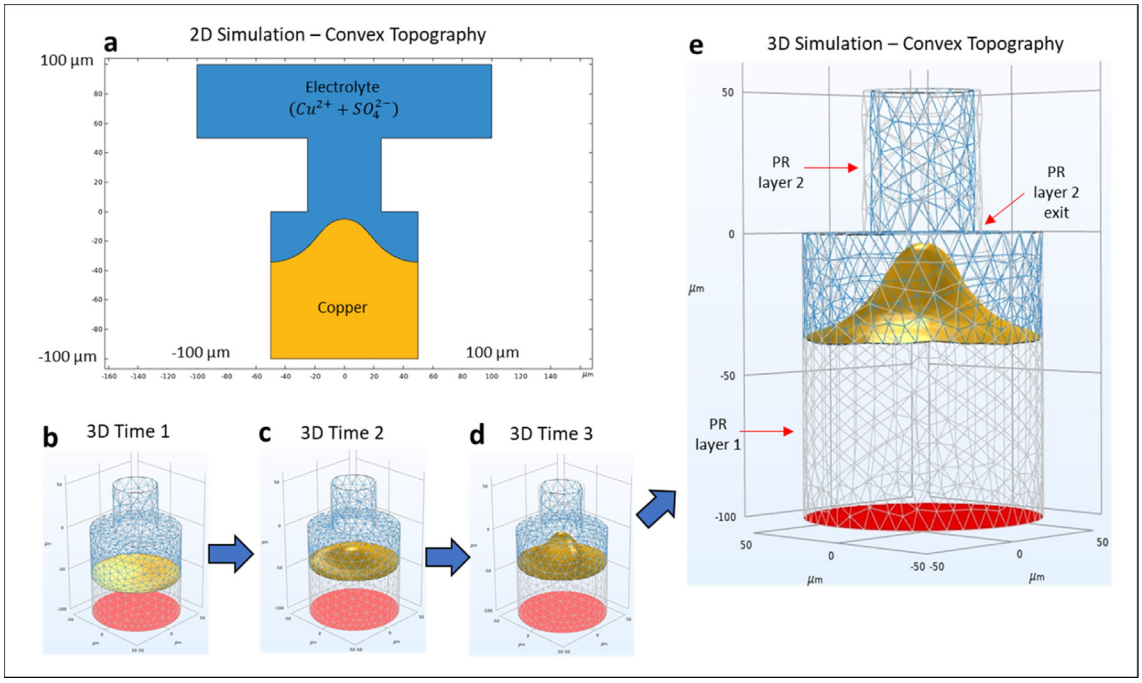


Fig. 6. 2D and 3D simulations for convex topographies with a superimposed PR mold design. a 2D VIA mold cross-section with a columnar VIA mold superimposed on top. **b** 3D version of **a** at an earlier time stamp, where the topography is virtually flat. **c** A subsequent time stamp from **b** displaying a moderately convex topography. **d** 3D version of **a** displaying a highly convex topography. This is the final time stamp just before the growing electrode enters the superimposed VIA mold. **e** Enlarged version of **d**.

option is equivalent to increasing the AR of PR layer 1 by utilizing a dual layer mold process.

4. Conclusions

As demand increases for micro/nano-devices with improved performance and enhanced functionality, VIAs have emerged as a key component of next generation 3D device architectures. Among this landscape, tailored VIA topographies are expected to become an increasingly important design option. Herein, we proposed a simple electroplating methodology that enables tailored electroformed VIA topographies, including flat, concave and convex design options. Flat topographies are essential for emerging 2.5D/3D flip chip architectures and concave/convex designs increase much-needed electrode surface area for sensing applications.

2D/3D FEM electroplating simulations were performed with COMSOL Multiphysics comprising two physics modules coupled in a multiphysics format: (1) tertiary current distribution and (2) deformed geometry. We have shown that diffusion-controlled mass transport conditions can be used to enable flat, concave and convex substrate-distal electrode topographies. Directly corresponding experimental work was used to validate flat and concave electroplated 2D/3D VIA topography simulations, which were then extended to convex electroplated VIA topographies. It was found that flat and concave electroplated VIA topographies are achievable at low and high VIA to PR mold thickness ratios, respectively (e.g., $\leq$0.5 and $\geq$0.8). This is due to elongated VIA mold cavities forcing diffusion streamlines to become vertically oriented at a significant depth into the PR mold cavity, wherein horizontally oriented diffusion streamlines are increasingly present as the electroplated mold approaches the PR mold/electrolyte boundary. Additionally, a novel dual layer PR mold was proposed as a design option to enable convex electroplated VIA topographies. By altering the dual PR layer mold width or diameter dimensional ratio (layer 2/layer 1), the convex slope can be selectively tailored, wherein a ratio of 1 can be used to enable flat electroplated VIA topographies at a high electroplated VIA to PR mold 1 thickness ratio.

To conclude, our methodology augments the electroplating design space by increasing its degrees of freedom to encompass VIA topographies, wherein tailored and scalable surface processing becomes an accessible design option that can be readily integrated into pre-existing research and industry electroplating SOPs.

5. Data availability

The raw data required to reproduce these findings are available within the paper. The processed data required to reproduce these findings are available within the paper.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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