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Authors	Cussen, Teresa;Majeed, Bivragh;Delaney, Kieran;Ó Mathúna, S. Cian
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Thin Silicon in a Novel 3-D Format for Implementation in Distributed Autonomous Micro Modules

Teresa Cussen, Bivragh Majeed, Kieran Delaney and Cian O'Mathuna
National Microelectronics Research Centre
Lee Maltings, Prospect Row, Cork, Ireland
353 21 4904088
{tcussen, bmajeed, kdelaney, cian.omathuna} @nmrc.ie

ABSTRACT
Silicon thinning, interconnection and packaging are key innovative hardware technologies that can be used to realise distributed autonomous micro-modules (DAMM) for future ad-hoc networks in ambient systems and intelligent environments. These would interact, respond and learn from their surroundings making integration of engineering, computer science and human intelligence a reality**.** This paper investigates thinning silicon sensors and packaging these sensors in a tetrahedral format. This form was chosen because it is vastly expandable and when miniaturised can be used as a building block for DAMM's, which can be designed to physically integrate into materials from which artefacts are fabricated.

Keywords
Thin silicon, 3-D packaging, flip chip, micro-modules.

INTRODUCTION
Ubiquitous computing represents the continuous trend in computing and communication technology towards smaller and more integrated information technology devices. The demand for smaller size, higher performance and increased functionality, means that interconnection and packaging technology has to improve significantly. The success of this integrated technology is dependent on the ability to embed DAMM's into our everyday surroundings. The optimal approach is to integrate DAMM's into an artifact in a manner coherent with its manufacture rather than adding it on after manufacture. These DAMM's will have computational power along with sensing and actuating abilities. The interface between the "real world" and the micro-nodes is established through sensor data. Interconnection and packaging technology has a key role to play in making these systems a reality. Advances in the packaging of sensors, in particular, strengthens this "real world" interface and facilitates the realisation of these DAMM's.
The most recent development in packaging to meet the growing demand for small highly integrated system has been chip scale packaging. These miniaturised packages combined the benefits of flip chip technology, i.e. shorter interconnection and area connection, with the considerable benefits of the package itself i.e. physical protection and easier assembly. But these technologies have lagged behind the growing demand for smaller and higher functionality devices. 3-D packaging has now emerged, as an innovative way to meet market requirements for the next generation of electronic products [5].
By using stacked thin chip packages it is possible to increase system integration while also reducing the length of the wire connects between the die thus reducing noise, increasing speed and reducing power. Many of the benefits of thin silicon packages contribute to the viability of distributed autonomous systems, such as those needed in ubiquitous computing, as these thin packages allow for easier integration of intelligent modules into artefacts.
Since standard silicon die thickness is in the order of 500 microns, reducing the height of a stacked package can be achieved by thinning the individual layers of the package [3]. Also, when silicon is thinned to below 50 microns it becomes flexible [1], [4], combined with a flexible substrate it can be a major advantage in the areas of wearable computing and embedded artefacts. One of the biggest advantages of 3-D packaging technology is that it increases silicon efficiency, which is the ratio of active silicon area to footprint area, an efficiency of greater than 100% is possible.
One of the earliest stacked chip scale packages consisted of bare die Flash memory and SRAM for use in mobile phones [3]. Today however industry has advanced to the point where it is considered feasible to stack 48 layers containing a total of 52 chips. The finished product would contain a processor, interface chips, DRAM, and 32 layers of flash memory [2].
There are three methods of 3-D stacking, which can be classified as follows: 1) wafer level stacking, which involves stacking thinned wafers on top of each other and interconnection is made through wafers via-holes, 2) chip level stacking, which involves stacking chips on top of each other and 3) package level stacking where packaged IC's are stacked to increase the silicon efficiency.

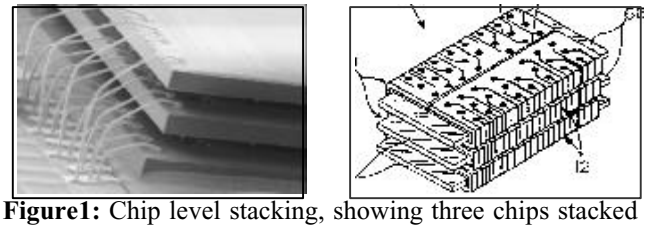


Figure1: Chip level stacking, showing three chips stacked and interconnected via wire bonding

This project deals with innovative chip level packaging. It employs thin silicon micro-sensors, which are packaged into a new shape using a flexible substrate. The aim is to produce the most efficient surface to volume ratio package, which can then be integrated with other similar packages to build DAMM's. The concept of packaging micro-sensors into tetrahedral shapes is very novel and has not been investigated before. This work has been done as a feasibility study for DAMM's at millimetre scale before moving to a highly miniaturised level.

SILICON THINNING

There are three main techniques used to thin silicon: wet etching, plasma etching and back grinding. For this experiment back grinding was chosen, as it is the most efficient method of removing the bulk of unwanted silicon. Back grinding refers to a mechanical process of removing silicon using an aluminium oxide powder (Al_2O_3). Al_2O_3 powder is mixed with water to make a slurry, which is released onto a grinding plate. Pressure is applied to the sample as it rotates on the surface of the grinding plate and the Al_2O_3 and H_20 slurry removes the excess silicon.

The test chip used consists of a heating element and diodes. The diodes act as temperature sensors where their forward voltage drop varies with changes in temperature. These changes in temperature are produced by applying a voltage to the on-chip heating element [6].

The electrical properties of a 225micron and an 80micron chip were compared to those of a regular 525micron chip to determine the effect of the thinning process. The result of this experiment is shown in figure2.

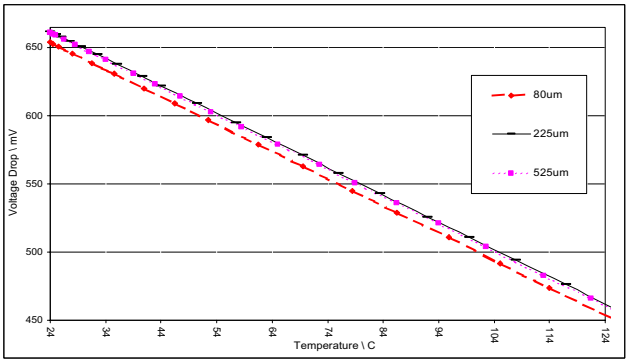


Figure 2: Forward voltage drop across diodes of varying substrate thickness as a function of temperature.

As the silicon substrate is reduced, figure3, so too is the chips ability to dissipate heat. This means that for the same heater voltage the thinner chips are much hotter than the regular chips. However, as shown in figure2, the voltage drop across each of the diodes is the same for the same temperature. This means that the thinning process does not adversely affect the operation of these temperature sensors.



Figure 3: Comparative profile of thin chip to regular chip.

PACKAGING

The packaging step starts with thinned silicon bonded onto a flexible substrate (flex). After etching of single sided flex the thin die are attached to the substrate using flip chip technology. Through holes, made by mechanical drilling, are necessary to access both sides of the flex. These holes are filled either with isotropic conductive paste or solder to obtain the connections. After testing, the packaging step is completed by forming the flexible substrate into a shape of a tetrahedron.

The tetrahedron is the simplest of the polyhedrons with four equilateral triangles for faces. This is the least number of faces required to enclose a portion of three-dimensional space. The tetrahedron is the most stable structure when force is applied [7]. At the current size, it is possible to assemble tetrahedrons at a prototype level, and to validate their robustness and reliability. Repeatability at high volume is in question as nature of assembly technique will not scale easily, however, it is speculated that at the target level of miniaturisation, techniques such as self-assembly could solve the problem. Table 1 shows some of the important properties of a tetrahedron in comparison with other regular polyhedrons and some shapes into which tetrahedrons can be formed. Four tetrahedrons form another tetrahedron with a central space occupied by an octahedron, 5 tetrahedrons make a flying saucer structure and 20 tetrahedrons form a complex near spherical structure. These shapes are investigated for possible physical integration into an artefact. The most important property is surface to volume ratio, which this project plans to exploit in 3-dimensional packaging.

Properties	Tetra	Octa	Icosa	Cube	Sphere
Surface Area	1.73 a^2	3.46a^2	8.660 a^2	6 a^2	12.5 a^2
Volume (vol)	0.117a^3	0.471a^3	2.357 a^3	a^3	4.2 a^3
SA/Vol ratio	14.8/a	7.35/a	3.97/a	6/a	3/a

Shapes into which tetrahedron can be formed			
Properties	Tetra with an Octa centre	Flying saucer	Icosahedron
Surface Area	1.73 a^2	4.330 a^2	8.660 a^2
Volume (vol)	0.117a^3	0.5890 a^3	2.357 a^3
SA/Vol ratio	14.8/a	7.35/a	3.97/a

Table 1:Compartive properties of different polyhedrons

CONCLUSION AND FUTURE WORK

In order to develop and integrate DAMM's into every day surroundings a novel packaging technique is being explored in this current work. Future investigation will be directed at thinning and reducing the chip dimensions of more complex sensors including accelerometers. A comparative investigation will be carried out into heat transfer, connectivity reliability and stress analysis on different shapes and the effect on these properties, when thinned chips are packaged. The ultimate goal will be to miniaturize the dimensions of the DAMM to micron level so that they blend into typical materials used for manufacturing artifacts.

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