CORA Cork Open Research Archive
Cartlann Taighde Oscailte Chorcaí

Title	Study of glass interposers for co-packaging electronic and photonic chips
Authors	Gupta, Parnika
Publication date	2025
Original Citation	Gupta, P. 2025. Study of glass interposers for co-packaging electronic and photonic chips. PhD Thesis, University College Cork.
Type of publication	Doctoral thesis
Rights	© 2025, Parnika Gupta. - https://creativecommons.org/licenses/by-nc-sa/4.0/
Download date	2026-10-25 14:05:20
Item downloaded from	https://hdl.handle.net/10468/18485



UCC
University College Cork, Ireland
Coláiste na hOllscoile Corcaigh

Ollscoil na hÉireann, Corcaigh

National University of Ireland, Cork



Study of Glass Interposers for Co-Packaging Electronic and Photonic Chips

Thesis presented by

Parnika Gupta

for the degree of

Doctor of Philosophy

University College Cork

[Tyndall National Institute]

Supervisor: Prof. Peter O' Brien

Co-Supervisor: Dr. Padraic Morrissey

February 2025

Declaration

This dissertation is the result of the work carried out in Photonic Packaging and Systems Integration Group at Tyndall National Institute from January 2020 to February 2025.

This is to certify that the work I am submitting is my own and has not been submitted for another degree, either at University College Cork or elsewhere. All external references and sources are clearly acknowledged and identified within the contents. Except where otherwise stated this dissertation is the result of my own work and is not substantially the same as any I have already submitted, or that I am in the process of submitting, for any degree either at University College Cork or elsewhere.

Parnika Gupta

Tyndall National Institute,

University College Cork,

February 2025

Acknowledgement

I would like to express my deepest gratitude to my supervisor, Prof. Peter O' Brien, for his invaluable guidance, support, and encouragement throughout this research. His expertise and insights have been instrumental in shaping this thesis.

I am also profoundly grateful to my co-supervisor, Dr. Padraic Morrissey, whose dedication and commitment have been a constant source of inspiration. His meticulous attention to detail and unwavering support have significantly contributed to the completion of this work.

My heartfelt thanks go to my colleagues in the lab Kamil, Arun, How Yuan, Jun Su, Marc, Sean, Noreen, Das, Sharon and Matt whose collaboration and assistance have been crucial. Your willingness to help and share knowledge has made this journey smoother and more enjoyable. I would also like to thank my PhD buddies Robert and Saif, I have got to learn a lot by working with them.

I owe a special debt of gratitude to my parents and my brother for their unwavering strength and support. Your belief in me has been a pillar of strength, and your encouragement has kept me going through the toughest times.

To my friends, thank you for your kind support and for sharing laughter during challenging moments. Your companionship has been a source of joy and relief, making this journey more enriching.

Lastly, I would like to extend my deepest thanks to my husband Amit, for his incessant advice and suggestions to better my thesis. Your constant support and belief in my abilities have been invaluable.

Abstract

In recent years, glass interposers have received significant attention within the microelectronics industry. This interest is primarily driven by their potential for scaling to panel-level packaging, which can reduce the cost of advanced packages. This ability to scale, coupled with excellent thermal dissipation, high optical quality, and superior electrical performance, makes glass interposers especially advantageous for photonic package integration, representing an exciting opportunity in the industry. This thesis presents a comprehensive thermal and electrical analysis of glass interposers for 2.5D electronic-photonic packages. It explores various thermal management strategies aimed at enabling the co-packaging of electronic and photonic chips within glass interposer-based packages. Additionally, the thesis investigates the electrical losses associated with different elements, including transmission lines, through-glass vias (TGVs), microvias, and ball grid array (BGA) structures.

Firstly, the efficacy of thermal Through-Glass Vias (TGVs) in dissipating heat from a laser chip bonded to a glass interposer is demonstrated by achieving a temperature reduction of approximately 120°C. This significant cooling effect is evident due to the laser chip's high heat flux density. This cooling efficiency can be further enhanced by optimizing the copper filling within the TGVs. Secondly, reference thermal chips are introduced as cost-effective and widely available heat sources for evaluating heat dissipation through glass interposers. These reference chips are utilized to assess the impact of TGV pitch variation on the thermal performance of the glass interposer. The influence of design parameters of TGVs, microvias, and BGAs on the electrical losses through glass interposers is also examined.

Furthermore, the author further discusses the thermal stabilization of photonic packages, which can be achieved through a novel structure called Substrate Integrated Micro-TEC (SimTEC). This structure features TGVs partially filled with copper and thermoelectric materials, with interconnects on the top and bottom of the glass interposer acting as the hot and cold sides of the SimTEC device. The impact of TGV design variations on the cooling capability of SimTEC is analyzed through simulations. Besides TGVs and SimTEC as thermal management strategies, which facilitate heat dissipation through the glass interposer, heat removal from the topside of electronic chips bonded to the glass interposer is demonstrated using copper clips.

These clips spread heat away from the electronic chip, emphasizing the importance of a heat dissipation pathway to establish contact between the copper clip and the heat sink. Finally, design rules are formulated which are aimed at enabling effective thermal management and electrical transmission in glass interposers.

Further investigation is needed to determine the optimal method for integrating package-level cooling solutions, such as heat sinks and micro-TECs, with system-level cooling solutions. Research aimed at facilitating seamless interaction between these cooling solutions with minimal thermal resistance is encouraged. The author also recommends conducting reliability analyses of glass interposers from both thermo-mechanical and photonic perspectives.

List of Publications

1. **Parnika Gupta**, Amit Tanwar, Xiuyun He, Kamil Gradkowski, Kafil M. Razeeb, Padraic E. Morrissey, Peter O'Brien, "Substrate integrated micro-thermoelectric coolers in glass substrate for next-generation photonic packages," J. Optical Microsystems 4(1) 011006 (5 January 2024). https://doi.org/10.1117/1.JOM.4.1.011006.
2. **Parnika Gupta**, Arun Kumar Mallik, Kevin Krohnert, Sylwester Latkowski, Chigo Okonkwo, Saif Alomari, Das Soumitra Kumar, Kamil Gradkowski, Padraic E. Morrissey, Peter O' Brien, "Thermal and Electrical Study of Glass Interposers in Co-Packaged Electronic-Photonic Systems," in IEEE Transactions on Components, Packaging and Manufacturing Technology, doi: 10.1109/TCPMT.2025.3533388.
3. Luigi Ranno, **Parnika Gupta**, Kamil Gradkowski, Robert Bernson, Drew Weninger, Samuel Serna, Anuradha Murthy Agarwal, Lionel C. Kimerling, Juejun Hu, and Peter Obrien; "Integrated Photonics Packaging: Challenges and Opportunities", ACS Photonics 2022 9 (11), 3467-3485; DOI: 10.1021/acsphotonics.2c00891.
4. **Parnika Gupta** et al., "Impact of Through Glass Vias Filling on the Performance of Passive Thermal Cooling in Photonic Packages," 2022 IEEE 9th Electronics System-Integration Technology Conference (ESTC), Sibiu, Romania, 2022, pp. 391-397, doi: 10.1109/ESTC55720.2022.9939531.
5. **Parnika Gupta** et al., "Reference Thermal Chips for 2D and 3D Co-packaging Process Development," 2023 IEEE 73rd Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 2023, pp. 2160-2165, doi: 10.1109/ECTC51909.2023.00372.
6. K. Kröhnert, **Parnika Gupta** et al., "High Aspect Ratio Through-Glass Vias as Heat Conductive Element," 2022 IMAPS Nordic Conference on Microelectronics Packaging (NordPac), Gothenburg, Sweden, 2022, pp. 1-6.
7. **Parnika Gupta** et al., "Thermal Management Strategies for Co-Packaged Optics on Glass Interposers in Next-Generation Photonic Packaging," Conference Proceedings, 2023 IEEE International 3D Systems Integration Conference (3DIC), Cork, Ireland, 2023, pp. 1-65, doi: 10.1109/3DIC57175.2023.10155106. [Oral Presentation]

List of Acronyms

AI	Artificial Intelligence
ASIC	Application-Specific Integrated Circuit
BEOL	Back End of Line
BGA	Ball Grid Array
C4	Controlled Collapse Chip Connection
CMP	Chemical Mechanical Polishing
CPO	Co-Packaged Optics
CPW	Co-Planar Waveguide
CTE	Coefficient of Thermal Expansion
DUT	Device Under Test
EIC	Electronic Integrated Circuit
FAU	Fiber Array Unit
FEM	Finite Element Method
FEOL	Front End of Line
FMCW	Frequency Modulated Continuous Wave
GSG	Ground-Signal-Ground
I/O	Input/Output
IHS	Integrated Heat Spreader
IR	Infrared
LIDAR	Light Detection and Ranging
LIDE	Laser Induced Deep Etching
MCP	Multi Chip Package
ML	Machine Learning
PCB	Printed Circuit Board
PIC	Photonic Integrated Circuit
RDL	Redistribution Layers
RTD	Resistance Temperature Detector
SIMTEC	Substrate Integrated Micro Thermoelectric Cooler
SiP	System-in-Package
TCT	Thermal Cycling Test
TEC	Thermoelectric Cooler

TEG	Thermoelectric Generator
TGV	Through Glass Vias
TIA	Trans-Impedance Amplifier
TIM	Thermal Interface Material
TSV	Through Silicon Via
UBM	Under Bump Metallization
VNA	Vector Network Analyzer
WDM	Wavelength Division Multiplexing

Nomenclature

k_{xy}	Effective in-plane thermal conductivity (W/m.K)
k_z	Effective out-of-plane thermal conductivity (W/m.K)
Ω	Electrical Resistance/ Characteristic Impedance (Ohm)
$k\Omega$	Electrical Resistance (kilo-Ohm)
S_{21}	Insertion Loss (dB)
S_{11}	Return Loss (dB)
T_c	Temperature at Cold End of Thermoelectric Cooler (K)
T_H	Temperature at Hot End of Thermoelectric Cooler (K)
J	Electric Current Density
V	Voltage (V)
S	Seebeck Coefficient (μV/K)
κ	Thermal Conductivity (W/m.K)
q	Heat Flux (W/m^2)
Q_c	Cooling power (mW)
I	Current (mA)
zT	Thermoelectric figure-of-merit
σ	Electrical conductivity (S/m)
∇	Gradient or Vector differential operator
Δ	Change in Variable

Table of Contents

Declaration ii
Acknowledgement iii
Abstract iv
List of Publications vi
List of Acronyms vii
Nomenclature ix
Table of Contents x
List of Figures xiv
List of Tables xxxiv
Chapter 1: Introduction 1
1.1 Photonic Packaging 1
1.1.1 2.5D integration of electronic and photonic chips 3
1.1.2 Glass Interposer: An enabler for 2.5D photonic packages 5
1.1.3 Focus of the Thesis 5
1.2 Background and Motivation 6
1.2.1 Need for co-packaging EIC and PIC 6
1.2.2 Motivation for study of glass interposers 8
1.3 State of the Art 10
1.3.1 Fabrication of Glass Interposers 10
1.4 Objectives and Highlights of the Thesis 16
1.5 Thesis Organization 18
1.6 References 21
Chapter 2: Thermal Management with Through Glass Vias for Next Generation Photonic Packages 27
2.1 Introduction 27
2.2 Experimental Results 29
2.2.1 Experimental Setup 29
2.2.2 Measurements using an IR Microscope 29
2.3 Simulation Results 33
2.3.1 Comparison of Simulation and Experimental Results 34
2.3.2 Sensitivity Analysis of Copper filling in TGVs 36

2.4 Conclusion 38
2.5 References 39
Chapter 3: Reference Thermal Chips for 2D and 3D Co-packaging Process Development 40
3.1 Introduction 40
3.2 Methodology and Analysis 42
3.2.1 Thermal Characterization of First-Generation Reference Thermal Chips 42
3.2.2 Thermal Characterization of Co-packaged Reference Thermal Chip and Reference Photonic Chip 48
3.2.3 Optical Characterization of Co-packaged Reference Thermal Chip and Reference Photonic Chip 51
3.3 Conclusion and Future Work 54
3.4 References 55
Chapter 4: Thermal and Electrical Study of Glass Interposers in Co-Packaged Electronic-Photonic Systems 57
4.1 Introduction 57
4.2 Design of Glass Interposer for Thermal and Electrical Characterization ..60
4.2.1 Design of Glass Interposer for Thermal Characterization 60
4.2.2 Design of Glass Interposer for Electrical Characterization 62
4.3 Assembly and Characterization of Thermal Test Vehicle 63
4.3.1 Assembly of Thermal Test Vehicle 63
4.3.2 Characterization of Thermal Test Vehicle 65
4.4 Assembly and characterization of electrical test vehicle 73
4.4.1 Assembly of Electrical Test Vehicle 73
4.4.2 Characterization of Transmission Lines on Glass 74
4.4.3 Characterization of Glass Interposer 77
4.4.4 Characterization of Electrical Test Vehicle 80
4.5 Conclusion 83
4.6 References 85
Chapter 5: Substrate Integrated Micro-Thermoelectric Coolers in Glass Substrate for Next-Generation Photonic Packages 90
5.1 Introduction 90
5.2 Simulation Approach 96
5.3 Results and Discussions 99

5.3.1 Substrate Integrated Micro-TEC 99
5.3.2 Effect of SimTEC via diameter 103
5.3.3 Effect of SimTEC via height 104
5.3.4 Effect of SimTEC via pitch 106
5.3.5 Effect of SimTEC fill factor 107
5.4 Optimization Analysis for SimTEC 109
5.5 Conclusion 113
5.6 References 115
Chapter 6: Copper Clip as Heat Spreaders for Glass Interposers 119
6.1 Introduction 119
6.2 Copper Clip for Heat Dissipation 121
6.3 Parametric study of components 126
6.3.1 Impact of Electronic Chip Thickness 126
6.3.2 Impact of Spacing between EIC and PIC 128
6.3.3 Impact of TIM Thickness 129
6.3.4 Impact of Copper Clip Thickness 130
6.3.5 Impact of Copper Clip Length 131
6.4 Requirement of a heat sink 133
6.4.1 TGVs under Copper Clip 133
6.4.2 Heat Sink integrated in PCB 138
6.5 Extended Copper Clip 145
6.6 Conclusion 153
6.7 References 155
Chapter 7: Design guidelines for co-packaging electronic and photonic chips on glass interposers for next-generation photonic packages 157
7.1 Introduction 157
7.2 Arrangement of thermal TGVs 158
7.3 Thermal TGV parameters and Requirement of Heat Sink 167
7.3.1 Effective Thermal Conductivities used in simulation model 167
7.3.2 EIC and PIC packaged on Glass Interposer and PCB 169
7.3.3 EIC and PIC packaged on Glass Interposer with heat sink integrated into the PCB 172
7.3.4 EIC and PIC packaged on Glass Interposer with heat sink attached directly under thermal TGVs 176

7.3.5 EIC and PIC packaged on Glass Interposer with heat sink attached directly under the thermal TGVs (only for EIC) 178
7.4 Hotspot Management 181
7.5 Electrical Design of TGVs 191
7.5.1 Diameter and Pitch of TGVs 191
7.5.2 Height and Shape of TGVs 197
7.6 Conclusion 201
7.7 References 203
Chapter 8: Conclusions and Future Work 205
8.1 Contributions and Highlights 205
8.2 Future Work 209
Appendix A 212
Appendix B 222

List of Figures

Figure 1.1: Examples of packaged photonic modules; (a) Single-channel PIC with side-by-side electronic integration; (b) Optical Network Unit (ONU) of the FP7-FABULOUS project; (c) Single-channel in/out photonic module with vertically integrated electronic chip; (d) 8-Channel Transceiver for the FP7-PLAT4M project [7]. 2

Figure 1.2: Illustration of Large-Scale Integration (LSI) silicon photonic systems capturing current and future technologies. (a) WDM Transceiver: A semiconductor mode-locked laser (SMLL) provides multi-wavelength continuous-wave (CW) light to an array of compact, WDM-capable modulators and filters. Reflection control circuits limit back reflections into the laser. High-speed photodetectors (PDs) carry out the O/E conversion. (b) The electrical current is then amplified by transimpedance amplifiers (TIAs) and limiting amplifiers. Analog-to-digital converters (ADCs) are used to digitize the signal for further digital signal processing (DSP). Monitoring PDs are used for control and stabilization of wavelength, phase shift, and temperature. Digital-to-analog converters (DACs) and drivers are used for E/O modulation of the digital signal. Dynamic random-access memory (DRAM) provides large memory access. Micro-controllers (μC) may be used to offload some of the digital processing as well. (c) LIDAR: A tunable laser provides frequency chirped light to a network of phase shifters, circulators/duplexers and coherent frontend for homodyne/ heterodyne frequency-modulated CW (FMCW) ranging and detection. Beam steering is done using optical phase arrays (OPAs) or focal-plane arrays (FPAs). Delay line interferometers aid in calibrating the received beat frequencies and support chirp linearization by directly controlling the tunable laser or a modulator and various forms of error correction through DSP [3]. 4

Figure 1.3: Generations of optics and the evolution of co-packaging technologies used in data center applications. The generational progression drives tighter integration between network switching and optical I/O that will probably culminate with 3D co-packaged optics with integrated lasers on chip [23]. 7

Figure 1.4: Electronic chip and photonic chip co-packaged on glass interposer with Through Glass Vias (TGVs) under the chips for heat dissipation. The low thermal conductivity of glass enables low thermal crosstalk between electronic and photonic chips. 8

Figure 1.5: Transmission performance comparison of TGV in Borofloat® Schott 33 glass substrate and TSV in silicon substrate (with 0.5µm oxide liner along the TSV). The diameter and pitch of the vias (TGVs and TSVs) is 100µm and 150µm respectively. The thickness of the substrate (glass and silicon) is 300µm. 9

Figure 1.6: Different processing flows, depending on the wafer thickness (A: glass thickness<300µm; B: glass thickness>300µm) [41]. 12

Figure 1.7: Customized Integrated Heat Spreader (IHS) with 2 cut-out windows for Fiber-Array-Unit (FAU) attachment [44]. 13

Figure 1.8: (a) TGV unit cell for effective out-of-plane thermal conductivity calculation with its boundary conditions to be applied in the FEM simulation software (b) detailed simulation model turned into a simplified simulation model with the use of effective thermal conductivity calculated from (a) [52]. 14

Figure 1.9: Overview of different elements of the glass interposer as well as heat removal mechanisms studied in the thesis. 16

Figure 2.1: Test Vehicles packaged for thermal IR measurements with laser soldered on (a) glass interposer (b) glass interposer with unfilled TGVs and (c) glass interposer with copper filled TGVs. 29

Figure 2.2: Measurement setup for IR imaging of the surface temperature of the laser packaged in the test vehicles. 30

Figure 2.3: Measurement results of the maximum surface temperature of the laser chip soldered on the test vehicles with (a) glass interposer assembly (b) glass interposer with unfilled TGVs assembly and (c) glass interposer with copper filled TGVs assembly. 32

Figure 2.4: Simulated results for the maximum surface temperature of the laser chip assembled on the test vehicles with (a) glass interposer (b) glass interposer with unfilled TGVs and (c) glass interposer with copper filled TGVs. 34

Figure 2.5: Comparison of the simulated and measured results in the three test vehicles with (a) glass interposer (b) glass interposer with unfilled TGVs and (c) glass interposer with copper filled TGVs. 35

Figure 2.6: Sensitivity analysis of the impact of copper filling on the effective thermal conductivity of a copper filled TGV with (a) simulation model of the cavity in copper-filled TGV and (b) showing the simulated results. 37

Figure 2.7: SEM Micrograph showing the cavities in the copper filling that were simulated in the sensitivity analysis. 37

Figure 3.1: An illustration showing the concept of Reference Chips for Co-packaging process development using 2.5D co-packaged reference thermal chip, reference RF chip and reference photonic chip. 41

Figure 3.2: Reference Thermal chips with heater line length of (a) 4450 µm in Chip 1, (b) 2450 µm in Chip 2 and (c) 1450 µm in Chip 3. 43

Figure 3.3: Measurement setup for recording the surface temperature of the reference thermal chip using IR thermal microscope on the top. 44

Figure 3.4: Measured data representing the increase in maximum surface temperature across the cross-sectional direction of the central heater loopback in (a) Chip 1, (b) Chip 2 and (c) Chip 3 respectively. 46

Figure 3.5: Comparison of the increase in surface temperature of different reference thermal chips with the error bars representing the measurements for each of the five heater loopbacks in each chip. 47

Figure 3.6: Measurement setup for recording the surface temperature of the reference thermal chip and reference PIC in (a) 2D stacked configuration with the reference chips placed side by side and (b) 3D stacked configuration with the reference PIC bonded on top of the reference thermal chip. The reference PIC has a region of interest (ROI) which is covered with a black solution for the IR thermal measurements across that area. 48

Figure 3.7: (a) 2D stacked reference PIC and reference thermal chip with the (b) surface temperature measurement of ROI on the reference PIC using thermal camera (c) and the recorded data highlighting the variation in the maximum surface temperature of the reference PIC as different heaters (H1-H5) on the reference thermal chip are switched on consecutively. 49

Figure 3.8: (a) 3D stacked reference PIC and reference thermal chip with the (b) surface temperature measurement of ROI on the reference PIC using thermal

camera (c) and the recorded data highlighting the variation in the maximum surface temperature of the reference PIC as different heaters (H1-H5) on the reference thermal chip are switched on consecutively. 50

Figure 3.9: Comparison between the maximum surface temperature of the reference thermal chip (Ref. TC) and reference PIC at different power levels, where the error bars represent the measurements recorded for the operation of each heater loopback (H1-H5). 51

Figure 3.10: Measurement setup for the optical characterization of the reference PIC when different heaters on the reference thermal chip are switched on. The fiber array is used for coupling in/out of the grating coupler loopback structure on the reference PIC. 52

Figure 3.11: Optical Spectrum analyser results for the input SLD source and the light coupled out of the (a) 2D stacked reference PIC and (b) 3D stacked reference PIC when H4 on the reference thermal chip is operated at increasing powers ranging from 237 mW to 2100 mW. The central wavelength is red-shifted in the case of 2D and 3D stacked architectures respectively. 53

Figure 4.1: A 2.5D glass interposer package consisting of co-packaged electronic (EIC) and photonic (PIC) chips bonded on the glass interposer (first-level interconnections); which is subsequently bonded on the PCB (second-level interconnections). 59

Figure 4.2: Details of the glass interposer stackup for (a) thermal characterization with different components such as BGA pads, thermal and DC connection TGVs, microvias, RDL wiring and UBM; (b) electrical characterization with different components such as RDL wiring, signal and ground TGVs, microvias and BGA pads. 62

Figure 4.3: Perspective view of the fabricated glass interposer for (a) thermal characterization with 100 μm pitch thermal TGVs in the interposer; (b) electrical characterization which includes CPW transmission lines on top and bottom of the glass surface which is interconnected through TGVs. 64

Figure 4.4: (a) Perspective view of the subassembly containing flip-chip bonded reference thermal chip on glass interposer. (b) Top view of the thermal test vehicle showing assembled reference thermal chip and glass interposer (thermal TGV pitch of 100 μm) on PCB, with underfill between the reference thermal chip-glass interposer and glass interposer-PCB interfaces.

The cross-sectional lines are specified in the figure. (c) Cross-sectional view of the thermal test vehicle along cross-sectional line 1. (d) Cross-sectional view of the thermal test vehicle along cross-sectional line 2. 66

Figure 4.5: Infrared thermal measurement showing surface temperature of the flip-chip bonded reference thermal chip on the glass interposer in thermal test vehicle exhibiting thermal TGV pitches of 200, 300 and 400 µm. 67

Figure 4.6: Maximum surface temperature measurement across the topside of the flip-chip attached reference thermal chip (along the horizontal axis shown as dashed lines in the inset for (a)100 µm and (b) 400 µm pitch TGVs with increasing input powers of the heater loopback (P_{in}). The heater loopback at the corner of the chip is being operated in both (a) and (b). 69

Figure 4.7: Comparison of the (a) simulated and (b) measured maximum surface temperatures of the backside of the flip-chip attached reference chip in the thermal test vehicle using different TGV pitches in the glass interposer with increasing input power of the heater loopback in the chip. 70

Figure 4.8: Simulated variation in the chip's maximum surface temperature with the change in out-of-plane effective thermal conductivity of TGVs and bumps between glass interposer and PCB (with underfill) when the glass thickness/TGV height is (a) 460 µm and (b) 110 µm respectively. PCB (with underfill). 71

Figure 4.9: Variation of the chip's maximum surface temperature with variation in the TGV pitch (100 µm, 200 µm, 300 µm and 400 µm). The figure also shows a significant decrease in maximum surface temperature with a heat sink embedded in the PCB, where the heat sink is the same size as that of the chip. 72

Figure 4.10: (a) Side view of the electrical test vehicle showing the Bi-Sn solder balls bonding the glass interposer on the PCB for RF characterization. This side view is pictured after the Bi-Sn solder reflow and before epoxy underfilling. (b) X-ray imaging analysis of the electrical test vehicle. 74

Figure 4.11: (a) Schematic showing CPW transmission line on glass. (b) Simulated and (c) measured insertion loss for the CPW transmission line (RDL1) with varying lengths on glass. (d) Simulated and (e) measured return loss for CPW transmission lines on glass with varying lengths. 76

Figure 4.12: (a) Variation of characteristic impedance with frequency for the CPW transmission line on glass, conductor backed CPW transmission line (CBCPW) and CBCPW transmission line with via fence connecting the side grounds to the backside ground on top and bottom of the glass interposer with their respective electric field distributions at 20 GHz. (b) shows the top view of the fabricated CPW transmission line on the glass interposer with no backside ground and TGVs and (c) shows the top view of the fabricated CBCPW transmission line with TGVs in the glass interposer. 77

Figure 4.13: (a) Schematic showing glass interposer for electrical characterization. Simulated and measured insertion loss results for the glass interposer with different lengths of the RDL1 line on top (b) 3 mm, (c) 4 mm, (d) 5 mm and (e) 6 mm. 78

Figure 4.14: Schematic showing glass interposer for electrical characterization. Simulated and measured return loss results for the glass interposer with different lengths of the RDL1 line on top (b) 3 mm, (c) 4 mm, (d) 5 mm and (e) 6 mm. 79

Figure 4.15: Schematic showing the electrical test vehicle for characterization (with de-embedded PCB losses). Simulated and measured insertion loss results for the de-embedded test vehicle with different lengths of the RDL1 line (b) 3 mm, (c) 4 mm, (d) 5 mm and (e) 6 mm. 82

Figure 4.16: Simulated insertion loss and return loss for the electrical test vehicle in (a) current design and (b) optimized design. (c) shows the optimized structure where the pitch of the ground fence TGV, microvias, BGA pads and solder are reduced to 250 μm, the microvia, BGA pad and solder diameter are reduced to 100 μm and the TGV diameter is increased to 70 μm to reduce impedance discontinuity along the signal path. 83

Figure 5.1 Schematic showing different approaches of thermoelectric cooler integration in a photonic package where Photonic Integrated Chip (PIC) and Electronic Integrated Chip (EIC) are co-packaged together on a Glass substrate where the implementation of (a) Macro-Thermoelectric Cooler (Macro-TEC) ; (b) Micro-TEC (μ-TEC) and (c) Substrate integrated micro-TEC (SimTEC) in photonic packages is highlighted. 92

Figure 5.2: Diagram showing the SimTEC architecture in Glass substrate with the SimTEC vias operating in the central region of the electronic chips (EIC)

and photonic chip (PIC) with the chip's peripheral I/Os dedicated for electrical connection in the photonic package. 94

Figure 5.3: Simulation model for (a) Free-standing micro-TEC leg pair and (b) SimTEC via pair. 99

Figure 5.4: Graphs showing the change in temperature gradient in the case of a Substrate integrated micro-TEC (SimTEC) when the substrate is varied between glass, silicon and the case where the micro-TEC pillars are free-standing (no substrate). This variation in cooling capability is highlighted in both conditions when the vias/pillars are (a) fully-filled with thermoelectric material and (b) when they are segmented i.e. half-filled with thermoelectric material and half-filled with copper. 100

Figure 5.5: Simulation results showing the temperature gradient across the top and bottom interconnects in the case of (a) Free-standing micro-TEC pillars (b) SimTEC vias in glass Substrate and (c) SimTEC vias in silicon Substrate, showing the thermal losses silicon contributing to the decrease in maximum temperature gradient across the TEC. 102

Figure 5.6: Graphs showing the change in temperature gradient in the case of (a) Free-standing micro-TEC pillars and (b) SimTEC vias in glass when the diameter of the vias/pillars partially filled with copper/thermoelectric material is varied from 30 μm to 50 μm, when the pitch and height of the vias/pillars is kept constant. 103

Figure 5.7: Graphs showing the change in temperature gradient in the case of (a) Free-standing micro-TEC pillars and (b) SimTEC vias when the height of the vias/pillars partially filled with copper/thermoelectric material is varied from 50 μm to 100 μm, when the pitch and diameter of the vias/pillars are kept constant. 105

Figure 5.8: Graphs showing the change in temperature gradient in the case of (a) Free-standing micro-TEC pillars and (b) SimTEC vias when the pitch of the vias/pillars partially filled with copper/thermoelectric material is varied from 40 μm to 60 μm, when the diameter and height of the vias/pillars is kept constant. 106

Figure 5.9: Graphs showing the change in temperature gradient in case of (a) Free-standing micro-TEC pillars and (b) SimTEC vias when the fill-factor (filling ratio of thermoelectric material and copper in vias/pillars) is varied

from 25% (1/4th of the cylinder filled with thermoelectric material and 3/4th of the cylinder is filled with copper) to 100% (the whole cylinder is filled with thermoelectric material), when the diameter, pitch and height of the vias/pillars is kept constant. 108

Figure 5.10: Graphs showing the change in the maximum temperature gradient of (a) Free-standing micro-TEC pillars and (b) SimTEC vias when the diameter, height and pitch of the vias/pillars are varied simultaneously where the fill-factor if the via/pillar is kept constant at 50%. 112

Figure 6.1: Schematic illustrating the heat dissipation pathways for the heat sources on the active region of the electronic chip (EIC). The heat dissipation towards the glass interposer forms a secondary heat flow path due to the solder microbumps and underfill introducing thermal resistance to heat conduction. The heat dissipation towards the topside of the chip and subsequently to the copper clip through the thermal interface material (TIM) forms the primary heat flow path due to its lower thermal resistance. 119

Figure 6.2: Simulation results of the FEM simulation showing the maximum temperature of the co-packaged EICs and PIC with (a) no TGVs under the EICs for heat dissipation and (b) TGVs under the EICs for heat dissipation. The presence of TGVs under the EICs lowers the maximum temperature of the EICs. 123

Figure 6.3: Top view schematic showing co-packaged electronic chips (EIC1, EIC2 and EIC3) and photonic chip (PIC) when there is (a) no copper clip in the assembly, (b) segregated copper clips which denotes separate copper clip on each EIC and (c) single copper clip which is covering all the three EICs. 124

Figure 6.4: Simulation results of the FEM simulation showing the maximum temperature of the co-packaged EICs and PIC with (a) no copper clip, (b) segregated copper clips and (c) single copper clip. The segregated copper clips allow for individual copper clips to be attached to the different EICs and the single copper clip allows for a single copper clip which is larger in size to be attached to the EICs. 125

Figure 6.5: Side view schematic of the co-packaged EIC and PIC with copper clip attached on top of the flip-chip bonded EIC. The schematic shows the various components (such as EIC chip thickness, spacing between EIC and

PIC, TIM thickness, copper clip thickness and length of the copper clip on the glass interposer) in the primary heat flow path which are parametrically studied in section 6.4. 126

Figure 6.6: Maximum temperature of the EICs (EIC1, EIC2, EIC3) and PIC with varying thickness of the electronic chips in case of (a) no copper clip, (b) segregated copper clips and (c) single copper clip. The increase in EIC thickness reduces the EIC and PIC temperature because of the increased chip volume for thermal spreading. 128

Figure 6.7: Maximum temperature of the EICs (EIC1, EIC2, EIC3) and PIC with varying spacing between electronic and photonic chips in case of (a) no copper clip, (b) segregated copper clips and (c) single copper clip. The increase in spacing between the EIC and PIC leads to an increase in the EIC temperature and a decrease in the PIC temperature due to lowered thermal crosstalk. 129

Figure 6.8: Maximum temperature of the EICs (EIC1, EIC2, EIC3) and PIC with varying TIM thickness in case of (a) segregated copper clips and (b) single copper clip. The increase in TIM thickness leads to an increase in the EIC temperature and minimal change in the PIC temperature respectively. It is explained due to the thermal resistance offered by the TIM and low lateral thermal conduction between EIC and PIC on glass interposer respectively. 130

Figure 6.9: Maximum temperature of the EICs (EIC1, EIC2, EIC3) and PIC with varying copper clip thickness in case of (a) segregated copper clips and (b) single copper clip. The increase in copper clip thickness leads to a decrease in the maximum temperature of EIC and PIC due to improved conduction and heat spreading with increased clip thickness. 131

Figure 6.10: Maximum temperature of the EICs (EIC1, EIC2, EIC3) and PIC with varying copper clip length in case of (a) segregated copper clips and (b) single copper clip. The increase in copper clip length on the glass interposer leads to a decrease in the maximum temperature of EIC and PIC as it allows larger area for heat spreading. 132

Figure 6.11: Simulation results of the FEM simulation showing the maximum temperature of the co-packaged EICs and PIC with (a) segregated copper

clips and (b) single copper clip with TGVs in glass interposer under the clip length on the interposer as seen through the schematic (c). 134

Figure 6.12: Variation in the maximum temperature of (a) EIC1, (b) EIC2, (c) EIC3 and (d) PIC with change in effective out-of-plane thermal conductivity (1.2 W/m.K-400 W/m.K) of the TIM, TGVs under the copper clip and bumps between the TGVs in glass interposer and PCB. This figure represents the case with segregated copper clips and the impact of change in thermal conductivity is studied through the magnitude of change in temperature of the chips. 136

Figure 6.13: Variation in the maximum temperature of (a) EIC1, (b) EIC2, (c) EIC3 and (d) PIC with change in effective out-of-plane thermal conductivity (1.2 W/m.K-400 W/m.K) of the TIM, TGVs under the copper clip and bumps between the TGVs in glass interposer and PCB. This figure represents the case with single copper clip and the impact of change in thermal conductivity is studied through the magnitude of change in temperature of the chips. 137

Figure 6.14: Variation in the maximum temperature of EIC1 with change in effective out-of-plane thermal conductivity (1.2W/m.K-400 W/m.K) of TIM, TGVs under the copper clip and bumps between the TGVs in glass interposer and PCB, when the interposer (and TGV) height is (a) 460µm, (b) 230µm and (c) 110µm. Note that TIM remains the dominant impact factor across (a), (b) and (c) but the impact of TGVs is overshadowed by the bumps as the interposer height is decreased. Additionally, the EIC temperature decreases with the decrease in interposer height due to lowering thermal resistance. 138

Figure 6.15: Variation in the maximum temperature of PIC with change in effective out-of-plane thermal conductivity (1.2 W/m.K-400 W/m.K) of TIM, TGVs under the copper clip and bumps between the TGVs in glass interposer and PCB, when the interposer (and TGV) height is (a) 460µm, (b) 230µm and (c) 110µm. Note that the impact of TGVs is overshadowed by the bumps as the interposer height is decreased. Additionally, the PIC temperature decreases with the decrease in interposer height due to lowering thermal resistance (with presence of TGVs under PIC for heat conduction). 138

Figure 6.16: Side view schematic of the co-packaged EIC and PIC with a copper clip attached on top of the flip-chip bonded EIC and TGVs are present under the copper clip. In addition to this, there is a heat sink integrated into the PCB region under the copper clip for effective heat dissipation. 139

Figure 6.17: Variation in the maximum temperature of (a) EIC1, (b) EIC2, (c) EIC3 and (d) PIC with change in effective out-of-plane thermal conductivity (1.2W/m.K-400 W/m.K) of the TIM, TGVs under the copper clip, bumps between the TGVs in glass interposer-PCB and heat sink embedded in PCB. This figure represents the case with segregated copper clips and the impact of change in thermal conductivity is studied through the magnitude of change in temperature of the chips. 141

Figure 6.18: Variation in the maximum temperature of (a) EIC1, (b) EIC2, (c) EIC3 and (d) PIC with change in effective out-of-plane thermal conductivity (1.2W/m.K-400 W/m.K) of the TIM, TGVs under the copper clip, bumps between the TGVs in glass interposer-PCB and heat sink embedded in PCB. This figure represents the case with single copper clip and the impact of change in thermal conductivity is studied through the magnitude of change in temperature of the chips. 142

Figure 6.19: Simulation results of the FEM simulation showing the maximum temperature of the co-packaged EICs and PIC with (a) segregated copper clips and (b) single copper clip with heat sink embedded in the PCB as well as TGVs in glass interposer under the clip length on the interposer as seen through the schematic (c). 144

Figure 6.20: Side view schematic of the co-packaged EIC and PIC with copper clip attached on top of the flip-chip bonded EIC with no TGVs present under the copper clip. The length of the copper clip is extended towards the end of the interposer and is directly attached to the heat sink integrated in the PCB. 145

Figure 6.21: Simulation results of the FEM simulation showing the maximum temperature of the co-packaged EICs and PIC with (a) extended segregated copper clips and (b) extended single copper clip where the copper clip is extended to be directly attached to the heat sink in the PCB. 146

Figure 6.22: Characterization setup for infrared thermal measurement of (a) reference thermal chip on glass interposer, (b) reference thermal chip on glass

interposer with copper clip attached on top of the flip-chip bonded chip (using thermal grease) and (c) reference thermal chip on glass interposer with an extended copper clip bonded on top of the chip (using thermal grease) and the extended copper clip is attached to the heat sink (copper plate maintained at 20ºC). Note that there are no TGVs in the glass interposer and the top surface of the chip, copper clip and extended copper clip are painted black to increase emissivity for infrared thermal measurement. 148

Figure 6.23: Infrared thermal images at maximum input power of a heater loopback in the reference thermal chip and maximum surface temperature profile along the horizontal direction (marked with a red dotted line) in case of (a) reference thermal chip flip-chip bonded on the glass interposer, (b) copper clip attached on top of the chip in the assembly (reference thermal chip flip-chip bonded on the glass interposer) and (c) extended copper clip attached on top of the chip in the assembly with the extended copper clip contacting the heat sink. 149

Figure 6.24: Comparison between the maximum junction temperature on the thermally active surface of the reference thermal chip when it is bonded to the glass interposer with no copper clip, copper clip only extending till the glass interposer and extended copper clip where its length is elongated to contact the heat sink surface. Note that only one heater loopback is operational in this case. 150

Figure 6.25: Infrared thermal images at maximum input power of heater loopbacks (two heater loopbacks are simultaneously operated) in the reference thermal chip and maximum surface temperature profile along the horizontal direction (marked with a red dotted line) in case of (a) reference thermal chip flip-chip bonded on the glass interposer, (b) copper clip attached on top of the chip in the assembly (reference thermal chip flip-chip bonded on the glass interposer) and (c) extended copper clip attached on top of the chip in the assembly with the extended copper clip contacting the heat sink. 152

Figure 6.26: Comparison between the maximum junction temperature on the thermally active surface of the reference thermal chip when it is bonded to the glass interposer with no copper clip, copper clip only extending till the glass interposer and extended copper clip where it's length is elongated to

contact the heat sink surface. Note that two heater loopbacks are simultaneously operational in this case. 153

Figure 7.1: The arrangement of TGVs in (a) Pattern 1 or uniform pattern and (b) Pattern 2 or honeycomb pattern. Uniform pattern shows that the TGVs are arranged in a uniform pitch across all rows and columns whereas the honeycomb pattern shows that the TGVs are placed at half-pitch distances across alternating rows; where pitch signifies the distance between the center of two vias. 158

Figure 7.2: The change in normalized thermal resistance with change in TGV diameter for fully filled vias in (a) Pattern 1 and (b) Pattern 2. The decrease in the normalized thermal resistance in (b) as compared to (a) is high with the lowest diameter (50µm) and highest spacing (300µm). 162

Figure 7.3: The change in normalized thermal resistance with change in TGV diameter and spacing for conformal coated vias with changing conformal coated copper thickness in (a) Pattern 1 and (b) Pattern 2. The decrease in normalized thermal resistance in the case of (b) honeycomb pattern as compared to (a) uniform pattern is more prominent in the case of the lowest diameter (50µm), highest spacing (300µm) and lowest thickness of the conformal coating of copper (5µm). 162

Figure 7.4: The simulation results of a 3.1mm×3.1mm chip bonded on the glass interposer with TGVs arranged in (a) Pattern 1 and (c) Pattern 2. The arrangement of TGVs in the simulation model is shown in (b) Pattern 1 and (d) Pattern 2. 164

Figure 7.5: The increase in peak temperature of the chip with increasing power generated by the chip for Pattern 1 and Pattern 2 for different chip sizes such as (a) $3.1\times3.1mm^2$ (b) $1.5\times1.5mm^2$ and (c) $0.5\times0.5mm^2$. 166

Figure 7.6: The electronic chip (EIC) and photonic chip (PIC) co-packaged on the glass interposer with TGVs under the chips. The spacing between the EIC and PIC varies which varies the volume of glass present between the chips. The TGVs connect the chips on top to the PCB board. 169

Figure 7.7: Scatter plot showing the maximum temperatures of the EIC and PIC when they are co-packaged on the glass interposer with TGVs. The volume under the EIC and PIC signifying the effective thermal conductivity of the TGVs

is changed across glass (Case 1), TGVs with different diameter and pitches (Case 2-21) and copper in glass interposer (Case 22). 171

Figure 7.8: The electronic chip and photonic chip co-packaged on the glass interposer with TGVs and heat sink embedded in the PCB. The heat sink is a copper block embedded in the PCB to allow for the heat removal from the EIC and PIC and it connects to the backside of the PCB maintained at 20ºC. 173

Figure 7.9: Scatter plot showing the maximum temperatures of the EIC and PIC when they are co-packaged on the glass interposer with TGVs and heat sink integrated in the PCB. The volume under the EIC and PIC signifying the effective thermal conductivity of the TGVs is changed across glass (Case 1), TGVs with different diameter and pitches (Case 2-21) and copper in glass interposer (Case 22). The heat sink embedded in the PCB reduces the temperature variation for different spacings across all cases when compared to **Figure 7.7**. 175

Figure 7.10: The electronic chip and photonic chip co-packaged on the glass interposer with TGVs and heat sink embedded in the PCB right under the thermal TGVs. The height of the copper block embedded in the PCB is increased to make contact with the thermal TGVs under EIC and PIC. This is done because the replacement of the bumps layer with copper reduces thermal resistance, and it is feasible to include it in the package architecture and packaging process flow. 176

Figure 7.11: Scatter plot showing the maximum temperatures of the EIC and PIC when they are co-packaged on the glass interposer with TGVs and heat sink integrated in the PCB right under the thermal TGVs. The volume under the EIC and PIC signifying the effective thermal conductivity of the TGVs is changed across glass (Case 1), TGVs with different diameter and pitches (Case 2-21) and copper in glass interposer (Case 22). The heat sink embedded in the PCB under the thermal TGVs further reduces the temperature variation for different spacings across all cases for the PIC, as compared to **Figure 7.9**. 177

Figure 7.12: The electronic chip and photonic chip co-packaged on the glass interposer with TGVs and heat sink embedded in the PCB right under the thermal TGVs only for EIC. The height of the copper block embedded in the PCB is increased to make contact with the thermal TGVs only under the

EIC. This is done to remove heat effectively from the EIC and allows for less lateral heat conduction to the thermally passive PIC. 178

Figure 7.13: Scatter plot showing the maximum temperatures of the EIC and PIC when they are co-packaged on the glass interposer with TGVs and heat sink integrated in the PCB right under the thermal TGVs of the EIC only. The volume under the EIC and PIC signifying the effective thermal conductivity of the TGVs is changed across glass (Case 1), TGVs with different diameter and pitches (Case 2-21) and copper in glass interposer (Case 22). The heat sink embedded in the PCB under the thermal TGVs of the EIC reduces the temperature variation for different spacings across all cases for both the EIC and PIC, as compared to **Figure 7.7**. 179

Figure 7.14: Design of the glass interposer with different components for co-packaging reference chips on the glass interposer. These components such as UBM, microvia, RDL2, RDL1, TGVs, Backside RDL and BGA facilitate the electrical and thermal connections from the top to the bottom of the glass interposer. The glass interposer also consists of two polyimide layers on the top and one polyimide layer on the bottom, this architecture is explained in detail earlier (refer Chapter 4). 183

Figure 7.15: Design of the glass interposer with the positions of the reference PIC, reference thermal chip and reference RF chip bonded on the glass interposer, with reference PIC positioned at the edge of the interposer. The reference thermal chip is thermally active as it is powered through the heater loopbacks on the chip, marked as H1-H10 in the figure. 183

Figure 7.16: Subassembly consisting of the reference PIC, reference thermal chip and reference RF chip bonded on the glass interposer using simultaneous SAC solder reflow for all the chips, with reference PIC positioned at the edge of the interposer. 184

Figure 7.17: Assembly consisting of the reference PIC, reference thermal chip and reference RF chip bonded on the glass interposer, which is then bonded on the PCB using BiSn solder reflow to connect the subassembly to the PCB, with the reference PIC positioned at the edge of the interposer. 185

Figure 7.18: Final assembly of the co-packaged reference chips, with reference PIC positioned at the edge of the interposer. This assembly is used for thermal

characterization to see the impact of the TGVs in glass interposer on thermal crosstalk between the reference chips. 186

Figure 7.19: The steady-state IR thermal measurement of the co-packaged reference chips along the horizontal axis marked for reference thermal chip, reference RF chip and reference PIC; when the heater loopback H6 is powered to 903.3 mW, with reference PIC positioned at the edge of the interposer. The variation in temperature across the horizontal marked lines for the reference thermal chip, reference RF chip and reference PIC is dependent on the position of the operational heater loopback (on reference thermal chip). 187

Figure 7.20: The transient IR thermal measurement of the co-packaged reference chips along the horizontal axis when the heater loopback H6 is powered to 903.3 mW, with reference PIC positioned at the edge of the interposer. The presence of TGVs in the glass interposer led to low thermal crosstalk with the difference in maximum temperatures of the reference chips ranging from approximately 28ºC to 36ºC. 188

Figure 7.21: The dependence of the maximum surface temperatures of the reference PIC at the edge of the interposer and reference RF chip on the different heater loopbacks in the reference thermal chip (H1-H10) being operated at different powers generated by the heaters (a) 81.33mW, (b) 375.4mW and (c) 903.3mW. The thermal crosstalk between the reference thermal chip, reference RF chip and reference PIC is highlighted with the same temperature variation trend across all input powers. 189

Figure 7.22: The simulation model of the CPW transmission line loopback with three cylindrical TGVs (Ground-Signal-Ground) connecting the ground and signal lines. 191

Figure 7.23: The variation of insertion loss of the CPW transmission line loopback with changing signal and ground TGV diameters (a) 50µm, (b) 60µm, (c) 70µm, (d) 80µm and (e) 90µm and changing pitch (150µm-500µm) for each of these TGV diameters. As the TGV diameter increased from (A) 50µ to € 90µm, the variation of the insertion loss at higher frequency starts getting lower and shows a trade-off when choosing the appropriate pitch for the maximum diameter. 193

Figure 7.24: The contour plots showcasing the insertion loss of the CPW transmission line for varying TGV diameters and pitches at different frequencies like

1GHz, 10 GHz, 20 GHz, 30 GHz and 40 GHz. The challenge which arises with increased mutual capacitance and mutual inductance of the signal and ground TGVs is highlighted in the contour plot for insertion loss at 40 GHz. 194

Figure 7.25: The contour plots showcasing the change in effective out-of--plane and in-plane thermal conductivities of the TGV with changing diameter and pitch of the TGVs. 194

Figure 7.26: The simulation model of the CBCPW transmission line loopback with cylindrical TGVs connecting the ground and signal lines.The ground TGV fence along the loopback connects the continuous ground planes on top and bottom of the glass interposer. 195

Figure 7.27: The variation of insertion loss of the CBCPW transmission line loopback with TGV ground fence with changing signal and ground TGV diameters (a) 50µm, (b) 60µm, (c) 70µm, (d) 80µm and (e) 90µm and changing pitch (150µm-500µm) for each of these TGV diameters showing a trade-off when choosing the appropriate pitch for the maximum diameter. The variation in the insertion loss at higher frequencies for increasing diameter from (a) 50µm to (e) 90µm with different pitches gets lower and the trade-off between maximum diameter and pitch exists to achieve low-loss transmission. 196

Figure 7.28: (a) Insertion loss of CBCPW transmission line loopback with ground fence when the TGV and glass substrate height is changed from 100µm to 500µm, (b) showing the change in maximum temperature of a chip bonded on the glass interposer (with PCB underneath) and (c) showing the change in maximum temperature of a chip bonded on the glass interposer (with copper heat sink underneath) when the chip size and the corresponding number of TGVs under the chip is changed. The TGVs are assumed to be cylindrical in these cases. 198

Figure 7.29: (a) Insertion loss of CPW transmission line loopback with no backside ground and no ground fence for increasing taper angle of the signal/ground TGVs, (b) Insertion loss of CBCPW transmission line loopback with backside ground and via ground fence for increasing via taper angles and (c) showing the change in maximum chip temperature when the chip size,

number of TGVs under the chip are changing for different TGV taper angles. 200

Figure 8.1: Maximum Temperature of (a) electronic chip and (b) photonic chip when the effective out-of-plane thermal conductivity of the TGV volume under the chips is varied from 1.2 W/m.K (glass) to 400 W/m.K (Copper). The variation in maximum temperature is simulated for different thickness of the TGVs/glass interposer 100, 250 and 500 µm. The simulation model is derived from Section 2 (Chapter 7). 209

Figure 8.2: Thermal Cycling Test (TCT) was conducted on a set of samples with hyperbolic TGV structures in glass. The TCT was performed from -40˚C to 125˚C with a dwell time of 15 minutes for the maximum and minimum temperature. The rate of temperature change was fixed at 4˚C/minute. The results of the TCT samples before thermal cycling and samples after 100 and 200 thermal cycles. 211

Figure A.1: Reflow profile for SAC305 solder bonding between reference thermal chip and glass interposer with the bonded subassembly shown in the inset. 214

Figure A.2: (a) Reflow profile for BiSn solder bonding between the reference thermal chip subassembly and PCB with the (b) bonded assembly and magnified view of the bonded sample. 214

Figure A.3: Assembly process of the thermal test vehicle. 215

Figure A.4: Top view of reference thermal chip assembly showing heat spreading across the chip's top surface when the reference thermal chip is bonded on (a) glass interposer which is then bonded on PCB; (b) glass interposer with 100µm pitch thermal TGVs which is then bonded on PCB and (c) glass interposer with 100µm pitch thermal TGVs which is then bonded on PCB with heat sink embedded in it. The figure clearly shows the improved lateral thermal spreading by incorporating thermal TGVs and the improvement in the downward heat dissipation (through interposer and PCB) with incorporation of thermal TGVs and heat sink in PCB. 217

Figure A.5: Assembly process of the electrical test vehicle. 218

Figure A.6: Insertion loss of the CPW transmission line in glass (RDL1=3mm in length) displaying monotonic decay in the signal upto 10 GHz. The slope of

this insertion loss is useful for computing the dielectric loss of the glass interposer, which is calculated as 0.0435 dB/GHz/cm. 219

Figure A.7: SAM image displaying the uneven spread of the underfill between glass interposer and PCB, with the area under the signal transmission structures marked through a red dotted box. 219

Figure A.8: Image displaying reflections of the ultrasonic signal being (a) 57% in the region of evenly spread underfill and (b) 100% in the region with no underfill. This means that the underfill is unevenly spread and the process of underfill dispension through capillary mechanism needs optimization. 220

Figure A.9: Simulation and measurement of return loss results for the de-embedded electrical test vehicle. This includes the losses incurred in the glass interposer with solder and underfill beneath it. The measured return loss is lower as compared to the simulated return loss due to the presence of air pockets due to the uneven spread of the underfill between glass interposer and PCB. 221

Figure B.1: Design of the glass interposer with the reference PIC, reference thermal chip and reference RF chip bonded on the glass interposer, with reference PIC positioned near the center of the interposer. 230

Figure B.2: Subassembly consisting of the reference PIC, reference thermal chip and reference RF chip bonded on the glass interposer using simultaneous SAC solder reflow for all the chips, with reference PIC positioned near the center of the interposer. 230

Figure B.3: Assembly consisting of the reference PIC, reference thermal chip and reference RF chip bonded on the glass interposer, which is then bonded on the PCB using BiSn solder reflow to connect the subassembly to the PCB, with reference PIC positioned near the center of the interposer . 231

Figure B.4: Final assembly of the co-packaged reference chips, with reference PIC positioned near the center of the interposer. 232

Figure B.5: The steady-state IR thermal measurement of the co-packaged reference chips along the horizontal axis when the heater loopback H6 is powered to 903.3 mW, with reference PIC positioned near the center of the interposer. 234

Figure B.6: The transient IR thermal measurement of the co-packaged reference chips along the horizontal axis when the heater loopback H6 is powered to 903.3 mW, with reference PIC positioned near the center of the interposer 234

Figure B.7: The dependence of the maximum surface temperatures of the reference PIC near the center of the interposer and reference RF chip on the different heater loopbacks in the reference thermal chip (H1-H10) being operated at different powers generated by the heaters (a) 81.33mW, (b) 375.4mW and (c) 903.3mW. 235

Figure B.8: SAM image of the package consisting of the reference chips bonded on the glass interposer and PCB with PIC positioned at the edge of the interposer. 236

Figure B.9: SAM image of the package consisting of the reference chips bonded on the glass interposer and PCB with PIC positioned near the center of the interposer. 236

List of Tables

Table 2.1: Table showcasing the effective in-plane and effective out-of-plane thermal conductivities of the test vehicles with laser chip bonded on glass, glass with unfilled TGVs and glass with copper filled TGVs. 33

Table 3.1. Electrical resistance measurements for the heater line loopbacks on different reference thermal chips 43

Table 4.1: Table detailing the number of TGVs and the corresponding volume of copper in the glass interposer when the TGV pitch is increased from 100 µm to 400 µm) 68

Table 5.1: Table highlighting the features of a centimetre scale TEC (Macro-TEC), Free-standing micro-TEC device and Substrate integrated micro-TEC (SimTEC). 95

Table 5.2: Thermoelectric properties of the materials measured at room temperature. 98

Table 5.3: Table showing the cooling capacity of Fully-Filled and Segmented pillars/vias in Free-standing and SimTEC configurations when $\Delta T=\Delta T_{max}$. 101

Table 5.4: Table showing the cooling capacity of Free-standing micro-TEC pillars and SimTEC vias configurations when $\Delta T=\Delta T_{max}$ for different pillar/via diameter. 104

Table 5.5: Cooling capacity of Free-standing micro-TEC pillars and SimTEC vias configurations when $\Delta T=\Delta T_{max}$ for different pillar/via height. 105

Table 5.6: The cooling capacity of Free-standing micro-TEC pillars and SimTEC vias when $\Delta T=\Delta T_{max}$ for different pillar/via pitch. 106

Table 5.7: Cooling capacity of Free-standing micro-TEC pillars and SimTEC vias configurations when $\Delta T=\Delta T_{max}$ for different fill factor. 108

Table 5.8: Design of Experiment (DOE) for the three geometrical factors (Diameter, Height and Pitch) of the free-standing micro-TEC pillars and SimTEC vias showing their impact on the temperature gradient and cooling power of free-standing micro-TEC and SimTEC device. 109

Table 6.1: Geometrical parameters (length, width and height) of the different components in the FEM simulation 122

Table 6.2: Effective in-plane and out-of-plane thermal conductivities of different components in the FEM simulation 123

Table 6.3: Maximum temperature of the EICs (EIC1, EIC2 and EIC3) and PIC derived from the FEM simulation with no TGVs under the EICs and with TGVs under the EICs 124

Table 6.4: Maximum temperature of the EICs (EIC1, EIC2 and EIC3) and PIC derived from the FEM simulation with no copper clip, segregated copper clips and single copper clip attached on top of the EICs. Note that in these cases, there are no TGVs in the glass interposer under the EICs. 125

Table 6.5: Maximum temperature of the EICs (EIC1, EIC2 and EIC3) and PIC derived from the FEM simulation with segregated copper clips and single copper clip attached on top of the EICs with TGVs in the glass interposer under the clip length on the interposer 135

Table 6.6: Effective in-plane and out-of-plane thermal conductivities of different components in the FEM simulation for segregated and single copper clip with heat sink integrated in the PCB in addition to the TGVs in the glass interposer under the copper clip area on the interposer. 143

Table 6.7: Maximum temperature of the EICs (EIC1, EIC2 and EIC3) and PIC derived from the FEM simulation with segregated copper clips and single copper clip attached on top of the EICs with TGVs in the glass interposer under the clip length on the interposer and heat sink integrated in the PCB. The area of the heat sink in PCB is kept the same as the area of the copper clip on glass interposer 144

Table 6.8: Maximum temperature of the EICs (EIC1, EIC2 and EIC3) and PIC derived from the FEM simulation with extended segregated copper clips and extended single copper clip attached on top of the EICs. The length of the clip is extended over the surface of the glass interposer to be directly attached to the heat sink integrated in the PCB 146

Table 6.9: Maximum Temperatures of EIC1, EIC2, EIC3 and PIC in different configurations 153

Table 7.1: Parameters used in the simulation model for analyzing heat dissipation in Pattern 1 and Pattern 2. 164

Table 7.2: Table detailing the number of thermal TGVs used in the simulation model for Pattern 1 and Pattern 2 with varying chip sizes. 165

Table 7.3: Simulation Parameters for the electronic chip and photonic chip co-packaged on the glass interposer 167

Table 7.4: The effective in-plane (k_{xy}) and out-of-plane (k_z) thermal conductivities for the different components used in the simulation model 167

Table 7.5: The effective in-plane (k_{xy}) and out-of-plane (k_z) thermal conductivities for the different diameter and pitch of the thermal TGVs. The table also contains the cases 1 and 22 when there are no thermal TGVs present (glass in Case 1) and when the TGVs are replaced with an equivalent copper block in the glass interposer (Copper in Case 22). 168

Table A.1: Glass Interposer Design for Thermal Test 212

Table A.2: Glass Interposer Design for Electrical Test 213

Table A.3: Effective Thermal Conductivities Used in Simulation Model 216

Table B.1: The maximum temperature of the EIC when the EIC and PIC are co-packaged together on the glass interposer with TGVs. 222

Table B.2: The maximum temperature of the PIC when the EIC and PIC are co-packaged together on the glass interposer with TGVs. 223

Table B.3: The maximum temperature of the EIC when the EIC and PIC are co-packaged together on the glass interposer with TGVs and heat sink integrated in the PCB. 224

Table B.4: The maximum temperature of the PIC when the EIC and PIC are co-packaged together on the glass interposer with TGVs and heat sink integrated in the PCB. 225

Table B.5: The maximum temperature of the EIC when the EIC and PIC are co-packaged together on the glass interposer with TGVs and heat sink integrated in the PCB right under the thermal TGVs, with no C4 bumps in between. 226

Table B.6: The maximum temperature of the PIC when the EIC and PIC are co-packaged together on the glass interposer with TGVs and heat sink integrated in the PCB right under the thermal TGVs, with no C4 bumps in between. 227

Table B.7: The maximum temperature of the EIC when the EIC and PIC are co-packaged together on the glass interposer with TGVs and heat sink integrated in the PCB right under the thermal TGVs of the EIC only, with no C4 bumps in between. 228

Table B.8: The maximum temperature of the PIC when the EIC and PIC are co-packaged together on the glass interposer with TGVs and heat sink integrated in the PCB right under the thermal TGVs of the EIC only, with no C4 bumps in between. 229

Chapter 1: Introduction

1.1 Photonic Packaging

The rapid rise of numerous machine learning (ML) models, each containing trillions of parameters, underscores the demand for high-performance compute systems that utilize Artificial Intelligence (AI) accelerators with disaggregated memory [1]. As data volumes increase exponentially, electrical interconnects (copper-based) face limitations in terms of bandwidth and speed [2]. Given the stringent requirements for bandwidth, density, energy efficiency, and low latency, silicon photonics has emerged as the preferred technology for implementing such architectures [1]. Silicon photonics has already emerged as a dominant technology in the field of communication for intra-, and inter-datacenter interconnects [3]. Photonic interconnects are more energy-efficient, reducing power consumption and enabling longer reach [4]. Packaging of these integrated photonic devices presents numerous technological, manufacturing, and cost challenges. Historically, packaging has been accepted to be a high-cost step in the overall manufacturing process, often consuming more than 80% of the total manufacturing cost [4,5]. As the field of integrated photonics continues to advance, efficient and reliable photonic packaging solutions are crucial for ensuring optimal performance and widespread adoption.

Photonic packaging involves the design, assembly, and integration of photonic components into functional modules or systems [5]. These components may include optical waveguides, fiber-chip couplings, RF lines, and more. Examples of packaged photonic modules can be seen in **Figure 1.1**.

Photonic packaging presents several challenges that impact the performance, reliability, and cost-effectiveness of photonic devices. These challenges include:

- Optical Coupling Efficiencies:
    - Achieving efficient light coupling between optical components (e.g., lasers, waveguides, detectors) is crucial. Challenges include alignment precision, mode matching, and minimizing losses at interfaces [6].
- Bonding Technologies and Hermeticity:

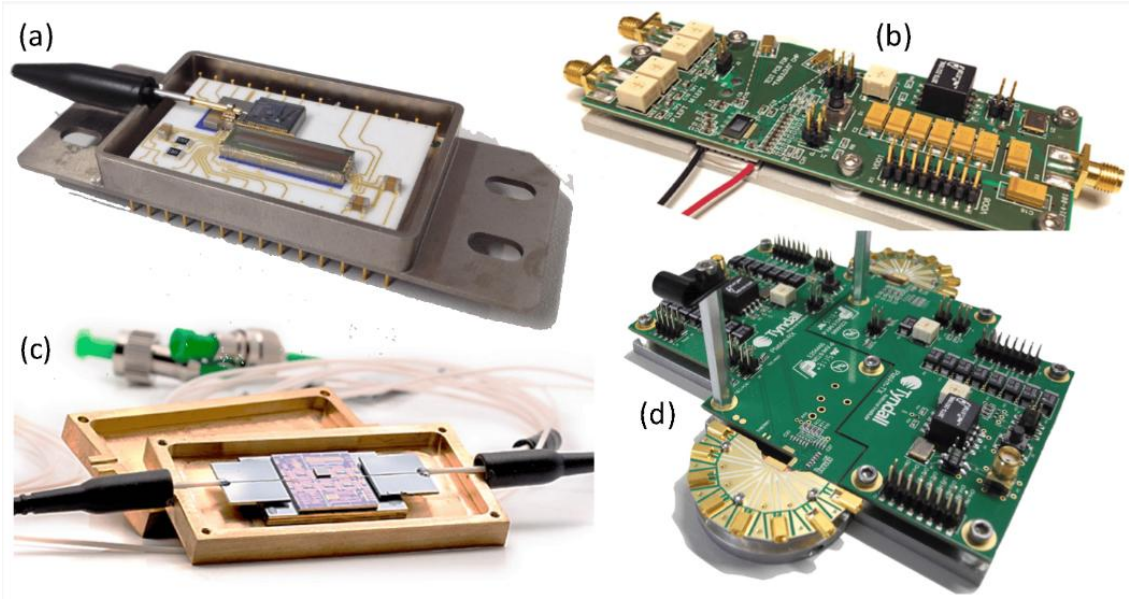


Figure 1.1: Examples of packaged photonic modules; (a) Single-channel PIC with side-by-side electronic integration; (b) Optical Network Unit (ONU) of the FP7-FABULOUS project; (c) Single-channel in/out photonic module with vertically integrated electronic chip; (d) 8-Channel Transceiver for the FP7-PLAT4M project [7].

- Reliable bonding techniques are essential for assembling photonic devices. Ensuring hermetic seals prevents moisture ingress, which can degrade performance [8].
- Challenges involve selecting suitable materials, achieving strong bonds, and maintaining long-term stability [8].

- Thermal Management:
  - Electronic and photonic devices generate heat during operation. Efficient heat dissipation is critical to prevent performance degradation and ensure reliability [8].
  - Challenges include designing effective heat sinks, managing temperature gradients, and avoiding thermal-induced stress [8].
- Electrical Performance:
  - Co-packaged optics (CPO) involves integrating electronics and photonics. Ensuring low electrical losses and high-speed signal transmission is challenging [6].
  - Addressing impedance matching, signal integrity, and power distribution is essential [6].

- Manufacturability and Automation:
    - Scalable, cost-effective manufacturing processes are vital. Challenges include automated assembly, yield optimization, and reducing production costs [6].
    - Collaboration across research fields needed to accelerate CPO technology development [6].

The goal is to mitigate these packaging challenges and create reliable packages that protect delicate photonic devices while maintaining their performance characteristics. In addition to the optical interconnects, electrical interconnects are required to co-package electronic and photonic chips for a multitude of functions in photonic packages such as drivers for modulators, Trans-Impedance Amplifiers (TIA) for photodiodes, control circuitry for ring resonators, thermal stabilization circuits etc. This is illustrated in **Figure 1.2**. The design learning obtained by optimizing the package architecture will contribute to the creation of the Assembly Design Kit (ADKs) that support electronic-photonic co-design.

1.1.1 2.5D integration of electronic and photonic chips

The 2.5D packaging approach in photonics involves integrating photonic integrated circuits (PICs) with electronic integrated circuits (EICs) on an interposer substrate (**Figure 1.4**). An interposer serves as an optical or electrical interface routing between chips in 2.5D configuration. The interposer also facilitates spreading the electrical/optical connection to a wider pitch (from chip to package substrate) or reroute it to a different connection [9]. By co-locating electronics and photonics on an interposer, the electrical link length is reduced, leading to higher interconnecting bandwidth density. Shorter signal paths enable faster data transfer, critical for applications like data centers, AI, and 5G [6]. Compact packages experience thermal interactions between electronic and photonic chips and managing heat dissipation in EICs without compromising the optical performance of the PICs is crucial [7]. A temperature change of approximately 20 °C can often cause a PIC to deviate from its intended operational range [8,9]. To ensure reliable performance of PICs in field testing, global thermal stabilization using a thermo-electric cooler (TEC) has been proposed in **Figure 1.1(b)** [10].

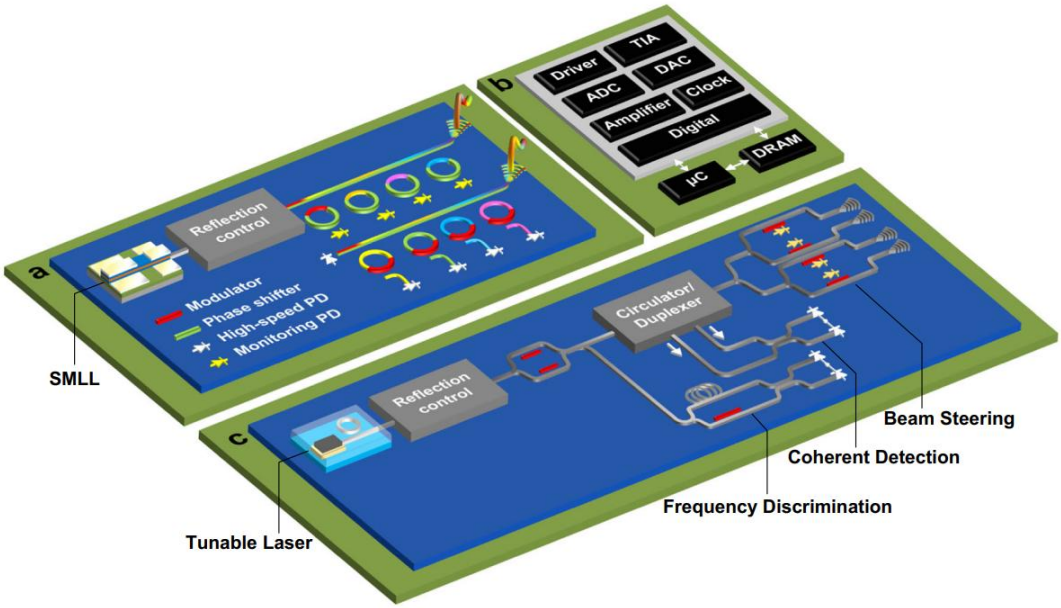


Figure 1.2: Illustration of Large-Scale Integration (LSI) silicon photonic systems showcasing current and future technologies. (a) WDM Transceiver: A semiconductor mode-locked laser (SMLL) provides multi-wavelength CW light to WDM-capable modulators and filters. Reflection control circuits limit back reflections, and high-speed photodetectors (PDs) perform O/E conversion. (b) Electrical current is amplified by transimpedance amplifiers (TIAs) and limiting amplifiers. ADCs digitize the signal for DSP. Monitoring PDs control wavelength, phase shift, and temperature. DACs and drivers modulate the digital signal, with DRAM for memory access and micro-controllers (µC) for digital processing. (c) LIDAR: A tunable laser provides frequency-chirped light to phase shifters, circulators/duplexers, and a coherent frontend for FMCW ranging and detection. Beam steering is done using optical phase arrays (OPAs) or focal-plane arrays (FPAs). Delay line interferometers calibrate beat frequencies and support chirp linearization through DSP [3].

The TEC provides stability against seasonal temperature variations of ±10 °C, enhancing reproducibility when tuning individual photonic elements (such as micro-ring resonators and thermo-optic phase-shifters) on the PIC [10].

However, utilizing such global cooling techniques in the photonic package means that the EICs in the package are operating at temperatures lower than their actual limitations due to the temperature-sensitive PIC present in the package. In addition to this, the variation in temperature across the TEC leads to a temperature variation in the whole package, including the PIC, which can impact the PIC-fiber coupling due to warpage. This thermo-mechanical impact on PIC-fiber coupling efficiency highlights

the use of TEC as an inefficient thermal management scheme [11]. Thermal decoupling is therefore needed between EICs and PICs such that the heat dissipated by the EIC does not negatively impact the optical functionalities of the PIC and temperature stabilization on the PIC can be separated.

1.1.2 Glass Interposer: An enabler for 2.5D photonic packages

A glass interposer is a thin, flat substrate made of glass that serves as an electrical bridge between different components within a 2.5D package (shown in **Figure 1.4**). Glass interposers in 2.5D packages presents itself as a viable platform for photonic packaging as the low thermal conductivity of glass prevents lateral thermal crosstalk between electronic and photonic chips [12]. Glass interposers also offer additional advantages such as optical transparency [13], dimensional stability [13], high resistivity, low loss electrical channels [14] and cost efficiency [15] for high density photonic packages [16]. Apart from the low thermal crosstalk between EICs and PIC, glass interposer also permits heat dissipation with copper filled Through Glass Vias (TGVs) [17]. TGVs are vertical vias that pass through a glass substrate, connecting different layers of a package. Research shows that TGVs play a significant role in heat dissipation within 2.5D integrated circuits (ICs) [18,19]. Hence, the glass interposer permits low thermal crosstalk between EICs and PICs while allowing heat dissipation from EICs through TGVs.

1.1.3 Focus of the Thesis

This work directly contributes to solving some of the core thermal packaging design challenges around using glass interposer for co-packaging of electronics and photonics together, which sets the groundwork for future developments in the field and more sophisticated and complex photonics systems to be implemented. Firstly, we study thermal management techniques that can be employed in 2.5D glass interposer-based packages with co-packaged EICs and PICs.

The effectiveness of TGVs for heat dissipation is studied in Chapter 2 where laser chips are bonded on glass interposer test vehicles and the maximum temperature of the laser chip is compared across the test vehicles with and without TGVs. Since lasers are small-sized, active light sources, they do not form a reliable heat source for studying heat dissipation in 2.5D packaged EIC and PIC system. Reference thermal chips are introduced in Chapter 3, which are an inexpensive solution to emulate the

thermal performance (hotspots) in EICs. These reference chips are easy to fabricate and available in large quantities for testing the heat dissipation and crosstalk in glass interposer based photonic packages. The heat dissipation through the glass interposer with TGVs is further studied by varying the pitch of the TGVs in Chapter 4. The glass interposers are also electrically characterized through coplanar transmission line structures in the glass interposer in Chapter 4. The thermal decoupling between EICs and PICs and the thermal stabilization of PICs can be improved further through the partial filling of thermoelectric materials in glass vias. This approach is termed "Substrate integrated micro-TEC" or SimTEC by the author and is detailed in Chapter 5. In addition to the heat flow path through the glass interposer, the heat flow path through the top of the chip is also studied through copper clip attachment on top of the flip-chip bonded reference thermal chip on the glass interposer in Chapter 6. Chapter 7 then details the design rules attained as a result of the thermal and electrical study of the TGVs in glass-based photonic packages. The author then presents a conclusion and future outlook that opens up a path to new research tasks.

1.2 Background and Motivation

1.2.1 Need for co-packaging EIC and PIC

Due to the rise of 5G, Internet of Things (IoT), AI, and high-performance computing applications, data center traffic has surged at a compound annual growth rate of nearly 30%. However, conventional pluggable optics (such as transceivers) have not kept pace with this growth, leading to a widening gap between application requirements and their capabilities [20,21]. CPO aims to bridge this gap by significantly shortening the electrical link length between electronic components and photonic devices as seen in **Figure 1.3**. It achieves this by integrating optics (such as lasers, modulators, and detectors) directly onto the same package as the switch ASIC (Application-Specific Integrated Circuit). By bringing optics closer to the switch ASIC, CPO increases interconnecting bandwidth density [18,19,20,21,22]. CPO involves co-optimization of electronics and photonics, enabling efficient integration. As data rates increase, power dissipation becomes a limiting factor and consequently, heat generated by densely packed components can impact performance [20,21]. The electronic and photonic components need to be integrated in close proximity to achieve reduced latency, increased bandwidth, energy efficiency and compact form factor.

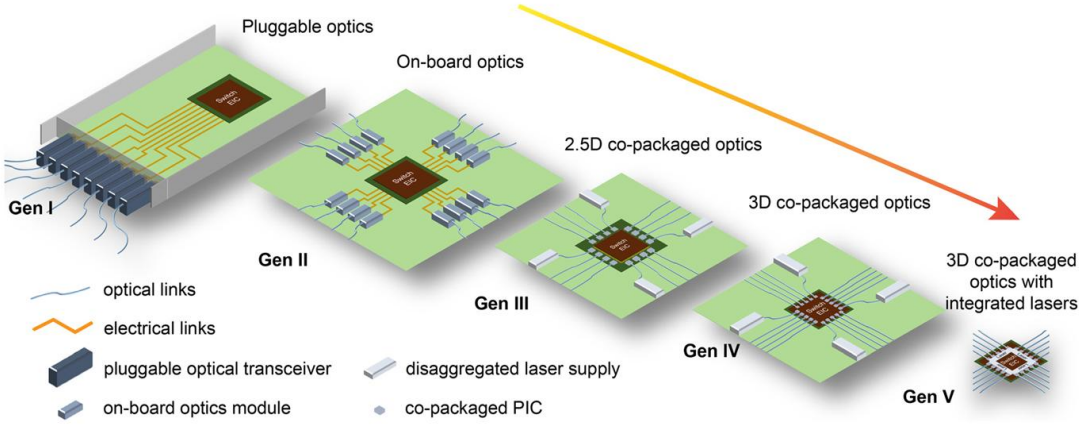


Figure 1.3: Generations of optics and the evolution of co-packaging technologies used in data center applications. The generational progression drives tighter integration between network switching and optical I/O that will probably culminate with 3D co-packaged optics with integrated lasers on chip [59].

Co-packaging can leverage existing packaging technologies such as flip-chip bonding, copper pillar bumps, interposers, vias etc [23]. It employs these techniques to reduce the interconnection length between EICs and PICs. The placement of electronic and photonic chips in close proximity for low-loss electrical transmission can also lead to thermal crosstalk between EICs and PIC. Glass interposers can offer a unique advantage in this regard as the low thermal conductivity of glass decreases lateral thermal conduction and TGVs allows effective heat dissipation in glass interposers [12] as seen in **Figure 1.4**.

A detailed view of the glass interposer structure is shown in Figure 1.4, highlighting key components such as the electronic and photonic chips, solder bumps, micro-vias, underfill, polyimide layers, through-glass vias (TGVs), and the printed circuit board (PCB). The design of the glass interposer in this work was based on manufacturable parameters from IZM Fraunhofer. The TGVs were hyperbolic in structure with a minimum diameter and pitch of 50 µm and 60 µm respectively; consistent with current fabrication capabilities. The interposer thickness was kept constant across all simulations and reported results, with a representative value of 460 µm. Copper filling within the TGVs was considered to be uniform and void-free throughout the study except for the initial results in Chapter 2; no variation in fill level was introduced across the other chapters. The figure also serves to identify and locate important structural elements referenced throughout the document, such as polyimide layers

used for passivation and supporting metal traces or RDLs (Redistribution Lines), solder bumps providing electrical and mechanical interconnection, micro-vias in the polyimide layers and redistribution layers for signal routing, and the underfill material that enhances mechanical integrity and thermal conduction between chip and interposer. The PCB forms the base of the assembly, interfacing with the interposer through standard BGA connections.

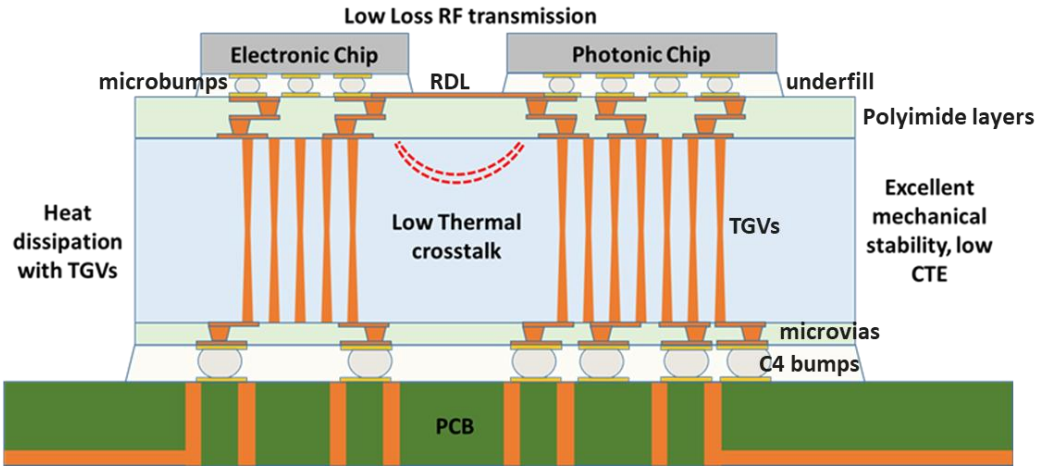


Figure 1.4: Electronic chip and photonic chip co-packaged on glass interposer with Through Glass Vias (TGVs) under the chips for heat dissipation. The low thermal conductivity of glass enables low thermal crosstalk between electronic and photonic chips.

1.2.2 Motivation for study of glass interposers

The study of heat dissipation in co-packaged EIC and PIC on glass interposers is primarily motivated by the following reasons:

1. **Cost-Effectiveness:** Glass interposers offer a potential low-cost alternative to silicon interposers [24,25]. By leveraging glass as an interposer material, manufacturers can simplify processes and significantly reduce manufacturing costs through scaling from wafer-level to panel-level packaging, which is especially important for system-in-package (SiP) designs [26].
2. **High I/O Density:** As chips continue to increase in I/O density, 2D package technology becomes insufficient. Glass interposers, part of the 2.5D package technology, allow for fine-pitch redistribution layers (RDL) and micro-bump connections, improving electrical performance and reducing power consumption [26].

3. **Reliability and Performance:** Understanding heat dissipation ensures the reliability of 2.5D packages. By managing thermal behavior, glass interposers can withstand temperature cycling and maintain long-term performance [26].
4. **Low Loss and High Bandwidth:** Optical waveguides within the glass substrate allow efficient light propagation, enabling close proximity between electronic and photonic chiplets.

Glass waveguides exhibit low optical loss, ensuring minimal signal attenuation. High bandwidth transmission is achievable due to low dispersion and low material absorption in glass [27,28].

5. **Excellent RF Performance:** Glass-based interposers exhibit low insertion loss in high-frequency RF applications. This makes them suitable for low-loss electrical interconnects between EIC and PIC [29]. TGVs also exhibit better electrical performance as compared to TSVs (**Figure 1.5**) due to the electrical insulation properties of TGVs.

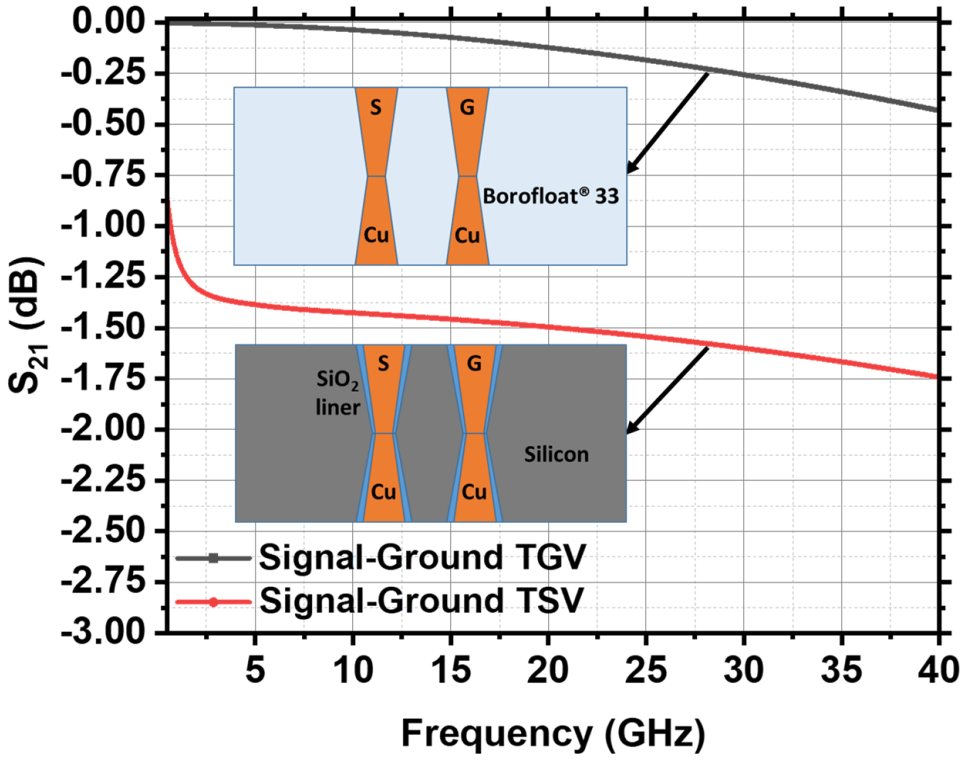


Figure 1.5: Transmission performance comparison of TGV in Borofloat® Schott 33 glass substrate and TSV in silicon substrate (with 0.5µm oxide liner along the TSV). The diameter and pitch of the vias (TGVs and TSVs) is 100µm and 150µm respectively. The thickness of the substrate (glass and silicon) is 300µm.

The different thermal management techniques that can be employed for enabling co-packaged electronic and photonic chips on glass interposers are studied through this thesis.

1.3 State of the Art

In this section, we explore the existing research on fabricating glass interposers and thermal management techniques for efficient heat dissipation in glass interposer packages. The fabrication process of the glass interposer is divided into two parts- fabrication of TGVs and fabrication of the RDLs on top and bottom of the glass core interposers. The thermal management approaches for glass interposers specified in this section are broadly divided into three parts, namely: heat spreaders, TGVs and micro-thermoelectric coolers.

1.3.1 Fabrication of Glass Interposers

1.3.1.1 Fabrication of Through Glass Vias

Research has demonstrated that 300mm semiconductor manufacturing tools can effectively process glass interposers. These tools enable the fabrication of copper wiring levels on one side of the interposer and the creation of Under Bump Metallization (UBM) and C4 (Controlled Collapse Chip Connection) bumps on the opposite side of the interposer [30]. The electrical connection from the top surface of the glass interposer to the bottom surface of the glass interposer is enabled through TGVs. The TGV formation technology that is used for the fabrication of wafer-level glass interposer in this thesis is Laser Induced Deep Etching (LIDE®) by LPKF Laser & Electronics [31].

LIDE is a selective etching process used to create TGVs in borosilicate glass substrates. The process involves modifying the glass substrate using a picosecond laser and then selectively etching the modified area with hydrofluoric acid (HF) solution [32]. At the laser-affected zone (LAZ), recombination of chemical bonds [33,34], nanostructure formation (such as nanovoids form along the laser beam path) and increased internal stress [35,36] can enhance the etch ability when immersed in HF solution. Key factors affecting TGV profile include laser pulses, HF solution concentration, and glass composition [32]. The LIDE technology showcases high throughput since it only utilizes one single laser pulse to create a TGV and the processed glass is defect-free [37].

High aspect ratio TGVs (1:10) with a taper angle of approximately 2º are formed in the Corning SGW3 glass through single picosecond laser pulse modification [38].

The glass substrate modification is caused due to the nonlinear multiphoton excitation effect prompted by the laser pulse [38]. LPKF also employs spatial and temporal beam shaping, leveraging nonlinear optical processes to extend the modified region in glass substrates [31]. Hydrofluoric acid (HF) is utilized to etch the borosilicate glass substrate, and the primary reaction is depicted as [39]:

$$SiO_2 + 6HF = H_2SiF_6 + 2H_2O$$

As the length of the etched channel extends, the etchant loses its mobility and the etch rate declines, leading to a taper or an hourglass shape in the glass substrate [39]. The angle of these hourglass shaped TGVs increases with decreasing HF concentration and appropriate levels of ultrasound energy, ultimately leading to vertical sidewalls [39]. It is seen through [40] that the femtosecond laser irradiation on borosilicate glass can lead to the formation of color centers and these centers display a higher level of reactivity, when etched with HF solution.

The formation of TGVs is followed by the metallization of the TGVs. It starts with the deposition of an adhesion layer and copper seed layer, which is dependent on the wafer thickness and via geometry. This is followed by electrodeposition of copper in TGVs which includes conformal coating, hermetic filling and complete via filling [41].

1.3.1.2 Fabrication of RDL for glass-core interposers

After the Chemical Mechanical Polishing (CMP) process to remove the copper overburden, a dielectric polymer layer is applied to the wafer as a RDL passivation film for metallization. This layer is created using photosensitive polyimide and cured at a low temperature. Following this, a copper (Cu) seed layer is deposited. Positive photoresist is used to pattern the redistribution lines. Finally, the Cu RDL lines are electroplated onto the wafer, followed by the removal of the photoresist and Cu seed layer [42]. This is followed by subsequent patterning and formation of the second layer of RDL and bond pads on the interposer. The RDLs on the different polyimide layers are connected through microvias patterned in the polyimide layers. The fabrication process flow for the glass interposer is shown in **Figure 1.6**, where **Figure 1.6(A)** denotes the process flow for an interposer with thickness below 300µm where a carrier

wafer is required and **Figure 1.6(B)** denotes the process flow for an interposer with thickness above 300µm [41].

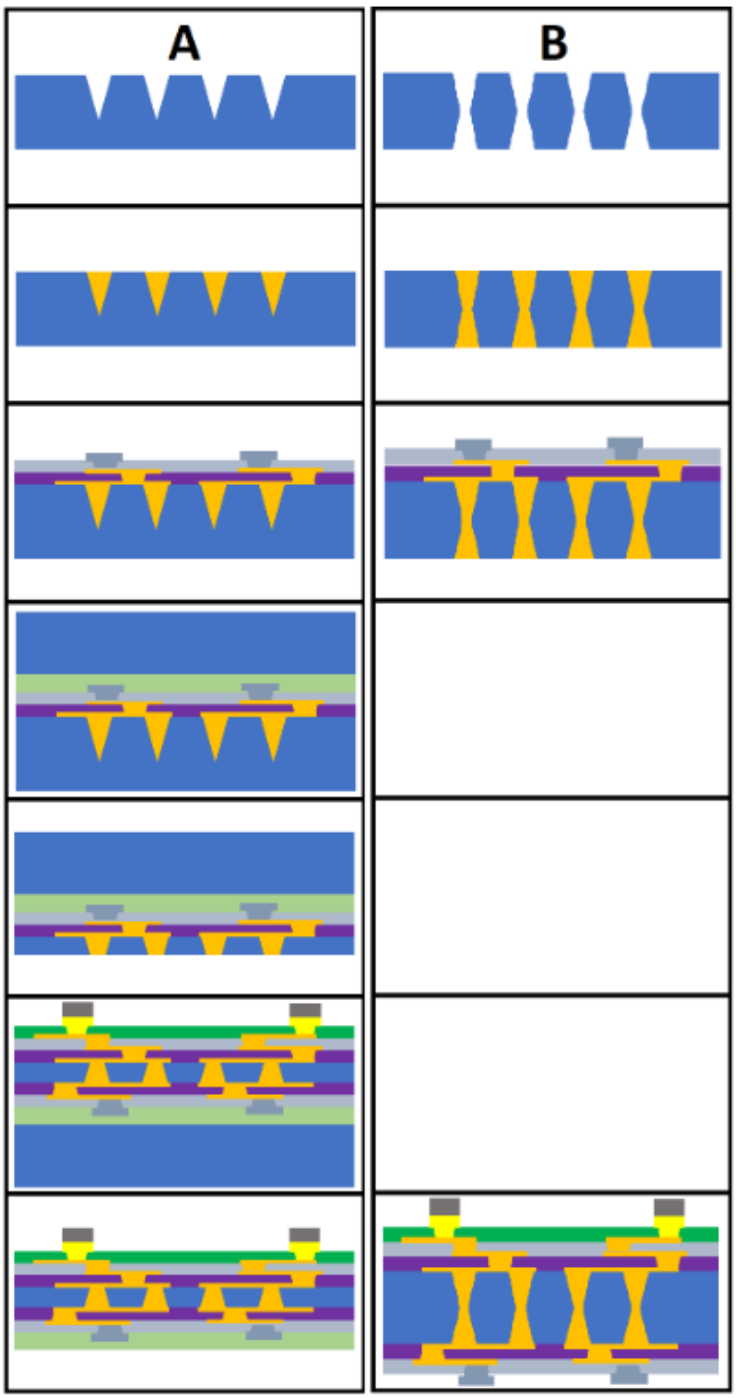


Figure 1.6: Different processing flows, depending on the wafer thickness (A: glass thickness<300µm; B: glass thickness>300µm) [41].

These glass interposers can enable high-density interconnections between electronic and photonic chips and act as an electrical/thermal/mechanical medium connecting the

chips and the PCB. Hence, it is essential to study the thermal management approaches that can be instrumental for the optimum functionality of glass interposer-based photonic packages.

1.3.2 Thermal Management Approaches for Glass Interposers

1.3.2.1 Heat Spreaders

Heat spreaders have been utilized for dissipating heat from the optical chiplet in [43] and [44], where thermal interface materials act as the contact between the optical chiplet and integrated heat spreader. In [43], different thermal interface materials andchanges in the die preparation steps are considered for effectively managing thermal dissipation using the heat spreader in the multi-chip package (MCP). This MCP consists of Silicon Photonics I/O chiplets packaged with a high-performance Intel FPGA chiplet. [45] and [46] also propose the use of integrated heat spreaders (IHS) and cold plates for effective heat dissipation in photonic engines. A 28.5% reduction in junction-to-ambient thermal resistance is shown in [47] with the integration of polycrystalline diamond as heat spreaders to the back-side of silicon chips as compared to the package without diamond integration.

The heat dissipation methods mentioned above involve integrating heat spreaders onto bonded electronic and photonic chips. However, these heat spreaders require cutouts to accommodate fiber-optic attachments to the PIC (as shown in **Figure 1.7**). Additionally, integrating a heat sink and fan directly onto the bonded PIC can introduce additional thermal resistance [48] and vibrations [49]. This in turn impacts heat dissipation in the package and alignment accuracy between the PIC and the fiber. Chapter 6 elaborates on the localized cooling of EICs and PICs through the primary heat flow path, which originates from the top of the flip-chip bonded integrated circuit.

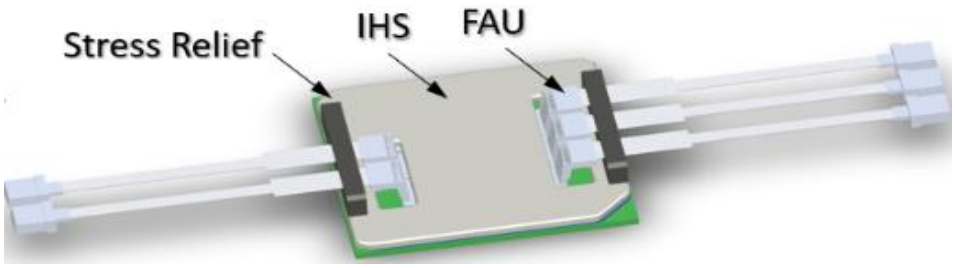


Figure 1.7: Customized Integrated Heat Spreader (IHS) with 2 cut-out windows for Fiber-Array-Unit (FAU) attachment [44].

1.3.2.2 Through Glass Vias

In addition to the primary heat flow path the secondary heat flow path with TGVs in the glass interposer for electronic-photonic co-packaging is also explored in this thesis. Previous research on thermal analysis of glass packages has shown that fully-filled copper TGVs offer a heat dissipation pathway for power amplifier chips and the steady state temperature of the power amplifier chip reduces with increasing number of blind vias [50]. Thus, TGVs can alleviate the heat dissipation challenge in the glass interposer [51]. As compared to the silicon interposer, copper TGVs in glass provide a thermal pathway for heat dissipation as well as thermal isolation between chips packaged side-by-side on the glass interposer [52,53]. The decrease in pitch of the TGVs leads to an increase in the effective out-of-plane thermal conductivity (**Figure 1.8**) [54]. However, this increase in the effective out-of-plane thermal conductivity of glass with the decrease in pitch of TGVs surpasses the increase in the in-plane effective thermal conductivity of glass [54]. The decrease in junction-to-board thermal resistance becomes insignificant with the increase in effective out-of-plane thermal conductivity of glass interposer beyond 100 W/m.K [54]. This is also specified in [55], where the improvement in peak temperature of the glass interposer gradually saturated with increasing TGV density. The integration of an adequate thermal path design outside the glass interposer architecture has been specified in [52] as it makes the thermal performance of the glass interposer equivalent to that of the silicon interposer. The reason for the saturation in peak temperature improvement and the need for the thermal path outside the glass interposer is specified in Chapter 4.

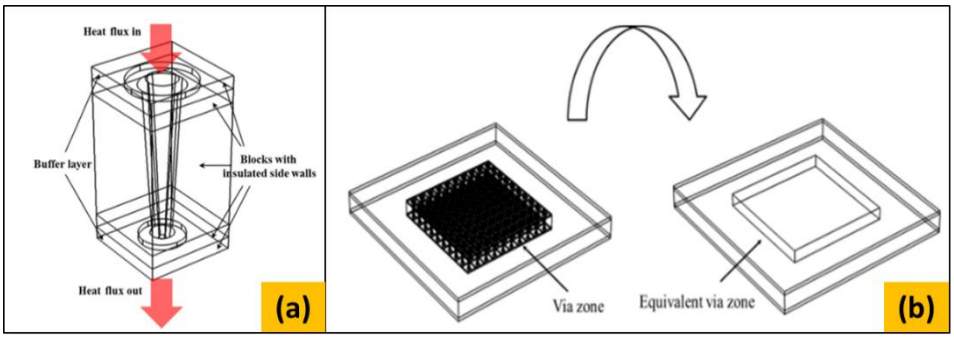


Figure 1.8: (a) TGV unit cell for effective out-of-plane thermal conductivity calculation with its boundary conditions to be applied in the FEM simulation software (b) detailed simulation model turned into a simplified simulation model with the use of effective thermal conductivity calculated from (a) [52].

The impact of the change in effective out-of-plane thermal conductivity of the bumps (connecting the glass interposer and PCB) on the decrease in temperature of the chips bonded on the glass interposer is shown to be superior to that of the TGVs in [54] and [55]. However, this analysis is mostly carried out for the thin glass interposers (100-200µm thickness). The impact of the change in effective out-of-plane thermal conductivity of the TGVs supersedes that of the bumps in the case of thicker glass interposers (when the thickness of the glass interposer is greater than the thickness of the bumps layer). This analysis is carried out in detail in Chapter 4.

1.3.2.3 Micro-Thermoelectric Coolers

Localized cooling for integrated electronic and photonic devices can be attained through micro-thermoelectric coolers (micro-TECs) [56]. Traditional macro thermoelectric coolers (TECs) are often inefficient for the thermal management of devices generating high heat flux levels (around 10kW/cm^2), especially with high-density integration in compact packages [57]. The design of these micro-TECs is optimized through Finite Element Method (FEM) simulations in [58] to improve the coefficient of performance (COP) of the micro-TEC device. However, the integration of micro-TECs (and heat sink) on the flip-chipped PIC leads to thermal resistance (offered by the bottom oxide layer in the chip) and mechanical stresses respectively.

Thus, the micro-thermoelectric cooling is integrated into the glass package by partially filling the TGVs with thermoelectric materials and this approach is termed a "Substrate integrated micro-thermoelectric cooler" or SimTEC. The design optimization of the SimTEC is detailed in Chapter 5.

1.4 Objectives and Highlights of the Thesis

The objective of this work is to study the electrical and thermal aspects of a glass interposer for electronic-photonic co-packaging with different elements as seen in **Figure 1.4**. This study is done step-by-step through thermal and electrical analysis of TGVs, CPW RDLs and reference chips. Different heat removal mechanisms for chips bonded on the glass interposer is also studied. Once the different elements are studied, these are studied as a part of the full-flow interposer. As a result of this, thermal and electrical design rules for the full-flow glass interposer are formulated. An overview picture is also shown in **Figure 1.9**.

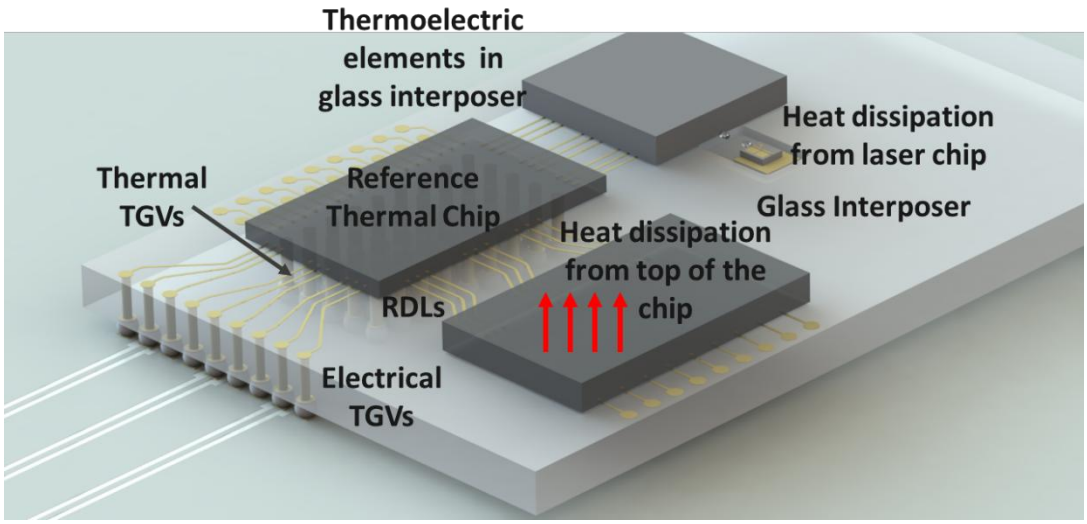


Figure 1.9: Overview of different elements of the glass interposer as well as heat removal mechanisms studied in the thesis.

This work aims to solve the thermal management challenge for co-packaged electronic and photonic chips on glass interposers. Previous research on this topic has mainly been based on the packaging of logic and memory dies on the glass interposer [51,52,53,54], where the SiP packages are mechanically robust for the placement of a large heat spreader encompassing all dies followed by the placement of the heat sink. However, in the case of co-packaged electronic and photonic chips, the popularity of the glass interposer arises out of the thermal decoupling between EIC and PIC provided by the low thermal conductivity of glass. The thermal management strategies need to be formulated such that the different aspects of photonic packaging are taken into account, such as:

1. Delicate optical facet of the PIC in case of edge coupler

2. Additional thermal resistance between junction and ambient environment through placement of a heat sink
3. Fan (in heat sink) vibrations that could lead to decrease in coupling efficiency of PIC-fiber interface
4. Close proximity between EIC and PIC
5. Thermally sensitive components on PIC such as ring resonators, modulators etc.
6. Thin EICs and PICs (100-300 μm), where the warpage could lead to ineffective thermal contact between top chip surface and heat sink

Based on these considerations, this thesis contributes to the thermal management strategies for glass interposers specifically catered to co-packaging electronic and photonic chips. Key highlighted contributions of the thesis include:

1. The efficacy of TGVs for heat dissipation, especially from heat sources with small areas such as laser chip is shown where the incorporation of TGVs in the glass interposer leads to a decrease in temperature of approximately 120ºC.
2. The reference thermal chips with heater loopbacks are devised to act as hotspot sources, emulating the thermal functionality of an EIC, which can be used to characterize the glass interposer. The glass interposer is thermally characterized by changing the dimensional parameters such as pitch of the TGVs with the reference thermal chip bonded on the glass interposer.
3. The decrease in pitch of the TGVs from 400 μm to 100 μm leads to a temperature decrease of approximately 2.9ºC.
4. A further decrease in the pitch of the TGVs (below 100 μm) leads to no significant change (lower than 1.5ºC) in the maximum temperature of the reference thermal chip because of the thermal impedance offered by the PCB.
5. The thesis also explores the importance of impedance matching when designing the microvias and Ball Grid Array (BGA) pads in the glass interposer to reduce insertion loss in the coplanar transmission line structures interconnected with TGVs, microvias and BGA.
6. Localized temperature control of the EIC and PIC is facilitated through the incorporation of thermoelectric materials in TGVs, termed as SimTEC which offers a thermal tuning capability of $\Delta T = \pm 9.3$ K (or 18.6K) with variation in dimensions of the TGVs partially filled with thermoelectric materials.

7. The heat spreading from the topside of the flip-chip attached reference thermal chip bonded on the glass interposer (without TGVs) through a copper clip is demonstrated. The integration of a copper clip reduces the maximum reference thermal chip temperature by approximately 9ºC, and is further reduced by 15ºC with the extended copper clip making direct contact with the heat sink.
8. Design rules are devised which illustrate the arrangement of the copper filled TGVs in a honeycomb pattern, optimization of the TGV dimensional parameters (diameter and pitch), requirement of heat sink or micro-TEC integrated in the PCB, hotspot management in co-packaged reference chips on glass interposer for effective thermal management of the assembly.

The analysis through the above-mentioned studies will prove to be useful for interposer designers and package designers for the thermal/electrical optimization of the chip-interposer-PCB stackup. This is eventually aimed at the design rules being incorporated as Assembly Design Kit (ADK) for package designers.

1.5 Thesis Organization

The thesis is organized as follows:

- **Chapter 1:** Introduction to the relevance of glass interposers as a platform for co-packaging electronic and photonic chips. The motivation to study different elements of the glass interposer as well as thermal management strategies is highlighted.

Study of elements of Glass Interposer Assembly

- **Chapter 2:** The effectiveness of TGVs for heat dissipation from a laser chip is studied through test vehicles with laser chip bonded on glass, glass with unfilled TGVs and glass with copper filled TGVs. The chapter highlights the usefulness of thermal TGVs for heat removal from laser chips as compared to the glass without thermal TGVs. The copper filling of the TGVs plays a major role in contributing towards heat dissipation.
- **Chapter 3:** The introduction of reference thermal chips which emulate thermal operation of an EIC (driver, TIA etc) and can be used for thermal characterization of glass interposers. Three different reference thermal chips are compared with varying heater lengths to analyze the differences in heat

dissipation. In addition to this, the impact of the heat dissipated by the reference thermal chip on the optical performance of the reference PIC is studied.

- **Chapter 4:** Thermal characterization of glass interposer using reference thermal chip bonded on the glass interposer with varying TGV pitches. Electrical characterization of the glass interposer through measurement and simulation of coplanar transmission line structures in glass interposer. The impact of changing TGV pitch on the maximum temperature of the reference thermal chip is studied. In addition to this, the electrical performance of TGVs, RDLs, microvias and bumps is also studied through insertion loss measurements.

Study of Thermal Management Strategies Glass Interposer Assembly

- **Chapter 5:** In addition to thermal TGVs, an alternative heat dissipation mechanism is studied where active cooling is involved. This incorporates the use of micro-thermoelectric elements in the glass interposer. FEM simulations comparing the SimTEC architecture with the free-standing micro-TEC architecture followed by a Design of Experiments (DOE) highlighting the variation in temperature difference (ΔT) across the top and bottom interconnects of the SimTEC device.
- **Chapter 6:** A second alternative is to remove the heat from the chips bonded on the glass interposer through its topside. Copper clips as a thermal management mechanism for heat removal from topside of the flip-chip attached ICs on glass interposer as a primary heat dissipation pathway. These copper clips are quite effective in heat dissipation from the reference thermal chips. When operated in conjunction with thermal TGVs, this bidirectional heat removal strategy can be highly useful.
- **Chapter 7:** Design rules to aid in the effective thermal design and electrical layout of the glass interposer for co-packaging electronic and photonic chips. The different glass interposer elements are studied in more detail (arrangement, diameter, pitch, taper and height of TGVs, location of hotspots etc.) to reach design guidelines which can aid manufacturability decisions at foundry services.

- **Chapter 8:** The conclusions derived from different chapters as well as various thermal management strategies in glass interposers presented in the thesis are presented in a concise manner along with providing directions for future work.

1.6 References

[1] Ramachandra, S. (2023). “Packaging Photonics for AI/ML Systems.” IEEE Photonics Technology Letters, 35(4), 1347-1350. DOI: 10.1364/OME.12.001347.

[2] Chipmakers Getting Serious About Integrated Photonics.

[3] Shekhar, S., Bogaerts, W., Chrostowski, L. et al. Roadmapping the next generation of silicon photonics. Nat Commun 15, 751 (2024). https://doi.org/10.1038/s41467-024-44750-0.

[4] Integrated Photonics Systems Roadmap: IPSR

[5] Guerber, S., et al. (2021). “Development, calibration, and characterization of silicon photonics-based optical phased arrays.” Presented at Smart Photonic and Optoelectronic Integrated Circuits XXIII.

[6] Tan, M., Xu, J., Liu, S., Feng, J., Zhang, H., & others. (2023). “Co-packaged optics (CPO): status, challenges, and solutions.” Frontiers of Optoelectronics, 16(1), 1-15.

[7] Carroll, L.; Lee, J.-S.; Scarcella, C.; Gradkowski, K.; Duperron, M.; Lu, H.; Zhao, Y.; Eason, C.; Morrissey, P.; Rensing, M.; et al. Photonic Packaging: Transforming Silicon Photonic Integrated Circuits into Photonic Devices. Appl. Sci. 2016, 6, 426. https://doi.org/10.3390/app6120426.

[8] M. F. Dautartas, J. Fisher, Hui Luo, P. Datta and A. Jeantilus, "Hybrid optical packaging, challenges and opportunities," *52nd Electronic Components and Technology Conference 2002. (Cat. No.02CH37345)*, San Diego, CA, USA, 2002, pp. 787-793, doi: 10.1109/ECTC.2002.1008189.

[9] Interposers - Semiconductor Engineering (semiengineering.com).

[10] Researchers look at thermal stabilization in photonic packages

[11] Baehr-Jones, T., Pinguet, T., Lo Guo-Qiang, P., Danziger, S., Prather, D., & Hochberg, M. (2012). Myths and rumours of silicon photonics. Nature Photonics, 6(4), 206-208.

[12] Kaspar, P.; Brenot, R.; Le liepvre, A.; Accard, A.; Make, D.; Levaufre, G.; Girard, N.; Lelarge, F.; Dan, G.-H.; Pavarelli, N.; et al. Packaged hybrid III-V/silicon SOA. In Proceedings of the European Conference on Optical Communication (ECOC), Cannes, France, 21–25 September 2014; pp. 1–3.

[13] Yuruker, S. U., Mandel, R. K., Bae, D. G., Gektin, V., & Ohadi, M. M. (2018, May). Packaging and Thermal Decoupling of an Optical Array using a Thermoelectric

Cooler. In 2018 17th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm) (pp. 695-700). IEEE.

[14] K. Kröhnert et al., "High Aspect Ratio Through-Glass Vias as Heat Conductive Element," 2022 IMAPS Nordic Conference on Microelectronics Packaging (NordPac), Gothenburg, Sweden, 2022, pp. 1-6.

[15] Aric Shorey, Shelby Nelson, David Levy, Paul Ballentine; Thin Glass Substrates with Through-Glass Vias.. International Symposium on Microelectronics 1 October 2019; 2019 (1): 000147–000151. doi: https://doi.org/10.4071/2380-4505-2019.1.000147.

[16] Charles Woychik, John Lauffer, David Bajkowski, Michael Gaige, Robert Edwards, Gordon Benninger, William Wilson; Processing Through Glass Via (TGV) Interposers for Advanced Packaging. International Symposium on Microelectronics 1 October 2018; 2018 (1): 000264–000269. doi: https://doi.org/10.4071/2380-4505-2018.1.000264.

[17] Frost & Sullivan. “Overview of the Interposer Technology in Packaging Applications.” Link

[18] Brusberg, L., et al. (2022). “Glass Interposer for High-Density Photonic Packaging.” DOI: 10.1364/OFC.2022.Tu3A.3.

[19] Heng-Chieh Chien, Chun-Hsien Chien, Ming-Ji Dai, Ra-Min Tain, Wei-Chung Lo, Yung-Jean Rachel Lu; Thermal Characteristic and Performance of the Glass Interposer with TGVs (Through-Glass Via). International Symposium on Microelectronics 1 January 2013; 2013 (1): 000611–000617. doi: https://doi.org/10.4071/isom-2013-WP11.

[20] https://www.keysight.com/blogs/en/inds/2023/02/14/co-packaged-optics-promises-and-challenges

[21] https://www.yolegroup.com/strategy-insights/global-insights-into-the-co-packaged-optics-technology-platform/

[22] M. Vallo, P. Mukish, "Global insights into the co-packaged technology platforms enabling transceivers with capacities of 1.6 Tbps and higher," Proc. SPIE 12027, Metro and Data Center Optical Networks and Short-Reach Links V, 120270R (3 March 2022); https://doi.org/10.1117/12.2608690.

[23] Tan, M., Xu, J., Liu, S. et al. Co-packaged optics (CPO): status, challenges, and solutions. Front. Optoelectron. 16, 1 (2023). https://doi.org/10.1007/s12200-022-00055-y.

[24] A. Ivankovic, T. Buisson, S. Kumar, A. Pizzagalli, J. Azemar, R. Beica; 2.5D Interposers and Advanced Organic Substrates Landscape: Technology and Market Trends. International Symposium on Microelectronics 1 October 2015; 2015 (1): 000041–000045. doi: https://doi.org/10.4071/isom-2015-TP22.

[25] Overview of the Interposer Technology in Packaging Applications (frost.com).

[26] Zhao, J., Chen, Z., Qin, F. et al. Development of high performance 2.5D packaging using glass interposer with through glass vias. J Mater Sci: Mater Electron 34, 1790 (2023). https://doi.org/10.1007/s10854-023-11185-0.

[27] Lars Brusberg, Aramais R. Zakharian, Şükrü Ekin Kocabaş, Lucas W. Yeary, Jason R. Grenier, Chad C. Terwilliger, and Robert A. Bellman, "Glass Substrate With Integrated Waveguides for Surface Mount Photonic Packaging," J. Lightwave Technol. 39, 912-919 (2021).

[28] L. Brusberg, J. R. Grenier, Ş. E. Kocabaş, A. R. Zakharian, L. W. Yeary, D. W. Levesque, B. J. Paddock, R. A. Bellman, R. M. Force, C. C. Terwilliger, C. G. Sutton, J. S. Clark, and K. Rousseva, "Glass Interposer for High-Density Photonic Packaging," in Optical Fiber Communication Conference (OFC) 2022, S. Matsuo, D. Plant, J. Shan Wey, C. Fludger, R. Ryf, and D. Simeonidou, eds., Technical Digest Series (Optica Publishing Group, 2022), paper Tu3A.3.

[29] Chien, Chun-Hsien, Ching-Kuan Lee, Hsun Yu, Chang-Chih Liu, Peng-Shu Chen, Heng-Chieh Chien, Jen-Hau Cheng, et al. 2013. “Performance and Process Comparison between Glass and Si Interposer for 3D-IC Integration.” IMAPSource Proceedings 2013 (1): 618–24. https://doi.org/10.4071/isom-2013-WP12.

[30] B. Hedrick et al., "End-to-End Integration of a Multi-die Glass Interposer for System Scaling Applications," 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, USA, 2016, pp. 283-288, doi: 10.1109/ECTC.2016.261.

[31] R. Ostholt, N. Ambrosius and R. A. Krüger, "High speed through glass via manufacturing technology for interposer," Proceedings of the 5th Electronics System-integration Technology Conference (ESTC), Helsinki, Finland, 2014, pp. 1-3, doi: 10.1109/ESTC.2014.6962711.

[32] Chen, L., & Yu, D. (2021). Investigation of low-cost through glass vias formation on borosilicate glass by picosecond laser-induced selective etching. Journal of Materials Science: Materials in Electronics, 32(21), 16481–16493.

[33] J. W. Chan, T. Huser, S. Risbud, and D. Krol, “Structural changes in fused silica after exposure to focused femtosecond laser pulses,” Optics letters, vol. 26, no. 21, pp. 1726-1728, 2001.

[34] K. Awazu and H. Kawazoe, “Strained Si–O–Si bonds in amorphous SiO 2 materials: A family member of active centers in radio, photo, and chemical responses,” Journal of Applied physics, vol. 94, no. 10, pp. 6243-6262, 2003.

[35] S. Rajesh and Y. Bellouard, “Towards fast femtosecond laser microma chining of fused silica: The effect of deposited energy,” Optics Express, vol. 18, no. 20, pp. 21490-21497, 2010.

[36] Y. Bellouard, T. Colomb, C. Depeursinge, M. Dugan, A. A. Said, and P. Bado, “Nanoindentation and birefringence measurements on fused silica specimen exposed to low-energy femtosecond pulses,” Optics express, vol. 14, no. 18, pp. 8360-8366, 2006.

[37] R. Santos, N. Ambrosius, R. Ostholt and J. -P. Delrue, "Bringing New Life To Glass For Wafer-Level Packaging Applications," 2020 International Wafer Level Packaging Conference (IWLPC), San Jose, CA, USA, 2020, pp. 1-7, doi: 10.23919/IWLPC52010.2020.9375851.

[38] Min-Kai Lee, Jyun-Zong Yu, Hsin-Yu Chang, Chia-Yuan Chang, Chien-Sheng Liu, Pai-Chen Lin; Nonlinear multiphoton modification of glass substrates for fabrication of high aspect ratio through-glass vias. AIP Advances 1 May 2022; 12 (5): 055011.

[39] Zhan, Y., Yin, K., Nie, M., & Dou, G. (2023, August). Selective Laser-induced Etching of Borosilicate Glass In Hydrofluoric Acid. In 2023 24th International Conference on Electronic Packaging Technology (ICEPT) (pp. 1-6). IEEE.

[40] A A Serkov and H V Snelling 2020 J. Phys. D: Appl. Phys. 53 135306, DOI 10.1088/1361-6463/ab6515.

[41] K. Kröhnert et al., "High Aspect Ratio Through-Glass Vias as Heat Conductive Element," 2022 IMAPS Nordic Conference on Microelectronics Packaging (NordPac), Gothenburg, Sweden, 2022, pp. 1-6.

[42] Kuramochi, Satoru, Sumio Koiwa, Takamasa Takano, Miyuki Akazawa, Hiroshi Mawatari, Kousuke Suzuki, and Yoshitaka Fukuoka. 2014. “Comparison of Fabrication Process Capability and Electrical Performance with Silicon and Glass Interposers.” IMAPSource Proceedings 2014 (1): 376–81. https://doi.org/10.4071/isom-WA11.

[43] K. Hosseini et al., "5.12 Tbps Co-Packaged FPGA and Silicon Photonics Interconnect I/O," 2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Honolulu, HI, USA, 2022, pp. 260-261, doi: 10.1109/VLSITechnologyandCir46769.2022.9830221.

[44] Hosseini, K., Kok, E., Shumarayev, S. Y., Chiu, C. P., Sarkar, A., Toda, A., ... & Wade, M. (2021, June). 8 Tbps co-packaged FPGA and silicon photonics optical IO. In 2021 Optical Fiber Communications Conference and Exhibition (OFC) (pp. 1-3). IEEE.

[45] S. Fathololoumi et al., "1.6 Tbps Silicon Photonics Integrated Circuit and 800 Gbps Photonic Engine for Switch Co-Packaging Demonstration," in Journal of Lightwave Technology, vol. 39, no. 4, pp. 1155-1161, 15 Feb.15, 2021, doi: 10.1109/JLT.2020.3039218.

[46] R. Mahajan et al., "Co-Packaged Photonics For High Performance Computing: Status, Challenges And Opportunities," in Journal of Lightwave Technology, vol. 40, no. 2, pp. 379-392, 15 Jan.15, 2022, doi: 10.1109/JLT.2021.3104725.

[47] Y. Zhong et al., "Heterogeneous Integration of Diamond-on-Chip-on-Glass Interposer for Efficient Thermal Management," in IEEE Electron Device Letters, vol. 45, no. 3, pp. 448-451, March 2024, doi: 10.1109/LED.2024.3351990.

[48] H. Oprins, Y. Ban, V. Cherman and J. V. Campenhout, "Thermal Aspects of Silicon Photonic Interposer Packages," 2020 21st International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE), Cracow, Poland, 2020, pp. 1-6, doi: 10.1109/EuroSimE48426.2020.9152630.

[49] H. Ronge, S. Krishnan and S. Ramamoorthy, "Evaluation of Stochastic and Periodic Cellular Materials for Combined Heat Dissipation and Noise Reduction: Experiments and Modeling," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 10, no. 7, pp. 1185-1203, July 2020, doi: 10.1109/TCPMT.2020.2998078.

[50] M. S. Kim et al., "Modeling, design and demonstration of ultra-miniaturized glass PA modules with efficient thermal dissipation," 2015 IEEE 65th Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2015, pp. 1163-1167, doi: 10.1109/ECTC.2015.7159742.

[51] S. Cho, Y. Sato, V. Sundaram, Y. Joshi and R. Tummala, "Experimental demonstration of the effect of copper TPVs (Through package vias) on thermal performance of glass interposers," 2014 IEEE 64th Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 2014, pp. 1247-1252, doi: 10.1109/ECTC.2014.6897451.

[52] S. Cho, Y. Joshi, V. Sundaram, Y. Sato and R. Tummala, "Comparison of thermal performance between glass and silicon interposers," 2013 IEEE 63rd Electronic Components and Technology Conference, Las Vegas, NV, USA, 2013, pp. 1480-1487, doi: 10.1109/ECTC.2013.6575767.

[53] H. Oprins and E. Beyne, "Generic thermal modeling study of the impact of 3D - interposer material and thickness options on the thermal performance and die-to-die thermal coupling," Fourteenth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm), Orlando, FL, USA, 2014, pp. 72-78, doi: 10.1109/ITHERM.2014.6892266.

[54] S. Cho, V. Sundaram, R. R. Tummala and Y. K. Joshi, "Impact of Copper Through-Package Vias on Thermal Performance of Glass Interposers," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 5, no. 8, pp. 1075-1084, Aug. 2015, doi: 10.1109/TCPMT.2015.2450731.

[55] L. Qian, Y. Xia, G. Shi, J. Wang, Y. Ye and S. Du, "Electrical–Thermal Characterization of Through Packaging Vias in Glass Interposer," in IEEE Transactions on Nanotechnology, vol. 16, no. 6, pp. 901-908, Nov. 2017, doi: 10.1109/TNANO.2017.2722686.

[56] R. Enright et al 2017 ECS J. Solid State Sci. Technol. 6 N3103.

[57] Lal, S. 2020. Development of thermoelectric materials and micro-devices for cooling and power generation. PhD Thesis, University College Cork.

[58] R. Kaur, A. Tanwar, P. Gupta, N. Padmanathan, P. O'Brien and K. M. Razeeb, "Design Optimization of Micro-Thermoelectric Cooler for Thermal Management using Finite Element Simulations," 2022 28th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC), Dublin, Ireland, 2022, pp. 1-6, doi: 10.1109/THERMINIC57263.2022.9950684.

[59] Near Margalit, Chao Xiang, Steven M. Bowers, Alexis Bjorlin, Robert Blum, John E. Bowers; Perspective on the future of silicon photonics and electronics. Appl. Phys. Lett. 31 May 2021; 118 (22): 220501. https://doi.org/10.1063/5.0050117.

Chapter 2: Thermal Management with Through Glass Vias for Next Generation Photonic Packages

2.1 Introduction

The move towards co-packaging of photonic and electronic chips in data centre transceivers has gained momentum to reduce the losses incurred by the pluggable optical modules.

This is done by reducing the length of the lossy copper lines running from the ASIC switch to the front-plate optical modules. In the case of co-packaged optics, the ASIC switch and the photonic chiplets are packaged close together in a heterogeneously integrated module [1]. One of the main challenges in this effort is the integration of light sources in the co-packaged module. The usage of external laser source has been studied but it leads to higher losses to interface the light source to the photonic module using an optical fibre and it is also limited by the number of fibers that can be attached to the photonic chip due to the limited shoreline density. The integration of laser sources inside the co-packaged module offers a power-efficient solution [2].

However, the integration of lasers inside the co-packaged module leads to thermal management challenges as the heat generated by the laser can lead to laser failure and the thermal crosstalk between the ASIC switch and photonic module further worsens this situation. The heat generated by the integrated laser source can also affect the temperature sensitive components on the photonic chip. The reliability of this packaged module is hence dependent on solving the thermal management challenge of integrated light source inside a co-packaged module [3]. The co-packaged module also requires high-speed electrical connection between the switch and the photonic module to reduce the power consumption and improve the transmission bandwidth. The use of glass as an interposer material has been proposed for low-loss co-packaged assembly of electronic switch and photonic chips because of its superior electrical and mechanical characteristics [4]. Low-loss optical coupling of high-density fiber and glass waveguide has also been demonstrated [5]. The main drawback is the low thermal conductivity of the glass interposer which can be solved by the incorporation of copper filled vias in glass [6]. These vias are termed as Through Glass Vias (TGVs)

and they can locallly increase the thermal dissipation characteristics of the glass interposer [7] while glass can prevent the lateral thermal crosstalk between chips. This can enable the use of glass interposers as an efficient electro-thermo-mechanical-optical board to support the co-packaging of electronic and photonic chips with an integrated laser source.

Thermal resistance measures a material's opposition to the flow of heat. A solid glass substrate has a high thermal resistance due to its inherently low thermal conductivity. This means it resists the flow of heat, acting as a thermal barrier. This can lead to hot spots and reduced device performance. The introduction of TGVs, typically filled with copper, fundamentally changes the thermal resistance. The copper vias provide a highly conductive pathway for heat to flow through the glass, effectively creating a "thermal short circuit." This dramatically lowers the overall thermal resistance of the substrate system, allowing heat to be transferred away from the chip and dissipated by a heat sink on the other side. Heat capacity is a measure of how much heat energy a material can store. Glass has a specific heat capacity of about 800 J/kg·K. The heat capacity of a different glass substrates is determined by the material properties of these substrates itself. When TGVs are added, the overall heat capacity of the substrate changes based on the combined volume and specific heat of both the glass and the via material. The change is often minimal in a practical sense, as the volume of the vias is small compared to the overall volume of the glass substrate. The primary thermal benefit of TGVs is not in changing the heat capacity, but in reducing the thermal resistance and minimizing the hotspot temperature to facilitate the removal of heat. The TGVs help move the heat out, not store it.

In this chapter, we have demonstrated this improvement in thermal performance of glass interposers with TGVs. In Section 2.2, the construction of three test vehicles with laser packaged on glass interposer, glass interposer with unfilled TGVs and glass interposer with copper filled TGVs has been explained in detail. The packages are tested using an infrared microscope and the results are recorded.

In Section 2.3, the simulation is setup using the same parameters and the results are compared with the measured results. The analysis showed that there is a challenge in the copper filling of TGVs and an analysis is carried out to quantify the impact of via filling on the thermal performance of the copper filled TGV.

2.2 Experimental Results

2.2.1 Experimental Setup

In order to test the heat dissipation characteristics of a glass interposer, three test vehicles are constructed and packaged. The test vehicles include a 1550nm laser soldered on a glass interposer, glass interposer with unfilled TGVs and glass interposer with copper filled TGVs. These three test vehicles will be compared. The TGVs are hourglass shaped with a top and bottom radius of 20µm, middle radius of 10µm and the thickness of the TGVs was the same as that of the glass interposer (460µm) in all the three test vehicles. The glass interposers have a 500nm gold layer deposited on the top and bottom. The TGV diameter and pitches are 40µm and 50µm in the test vehicle with unfilled TGVs and copper filled TGVs. The 150×150 μm^2 solder preform is picked and placed on top of the glass interposer followed by the placement of the laser chip. The laser is soldered on the interposers using a thin gold tin (9µm thick AuSn) solder preform using a flip-chip bonder. This sub-assembly is then bonded to the PCB using silver epoxy. Once the silver epoxy is cured, the laser chip is wire-bonded to the PCB pad for power delivery. The packaged test vehicles are shown in **Figure 2.1**.

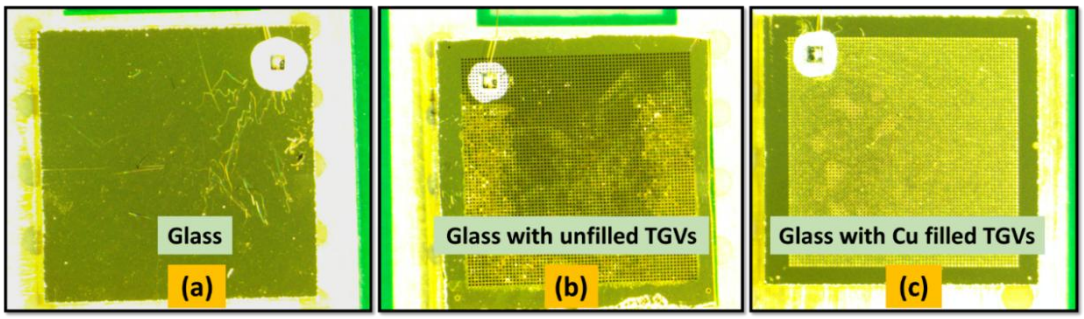


Figure 2.1: Test Vehicles packaged for thermal IR measurements with laser soldered on (a) glass interposer (b) glass interposer with unfilled TGVs and (c) glass interposer with copper filled TGVs.

2.2.2 Measurements using an IR Microscope

Several methods exist for reliably measuring temperature on a chip. These typically involve the placement of a thermistor in close proximity to the device under test (DUT) or the integration of an RTD (resistance-temperature detector) layer beneath it. Both of these techniques have inherent imprecisions. A thermistor, for instance, only measures the surface temperature of its specific location, offering only an approximation of the DUT's actual temperature. The use of a fabricated RTD requires

a small current, which can generate internal heat, potentially affecting the accuracy of the surface temperature measurement and increasing chip fabrication expenses. An external NTC (Negative Temperature Coefficient) thermistor cannot be attached to the laser chip easily due to the comparable size and complexity of solder/wire attached for output reading of the thermistor. In addition to this, the use of an external NTC on the substrate will give an incorrect reading due to the low lateral heat spreading on glass. An alternative method, one employed in our measurements, uses a thermal camera to provide a distinct advantage through contactless, high-speed surface temperature mapping.

The package is placed on a large copper block (8x8x1 cm^3) which has four 4x4 cm^2 TECs embedded at the bottom. The TEC controller was used to maintain the temperature of 20ºC on the surface of the copper block. A FLIR© infrared imaging camera is used to measure the surface temperature of the laser chip in the three test vehicles. The experimental setup is shown in **Figure 2.2**.

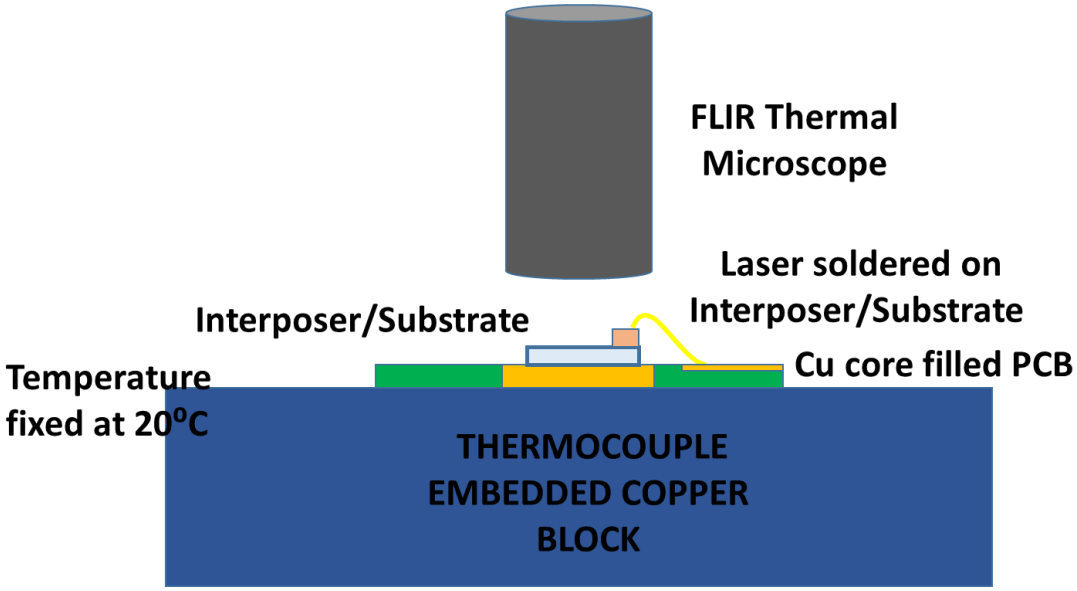


Figure 2.2: Measurement setup for IR imaging of the surface temperature of the laser packaged in the test vehicles.

The topside of the laser opposite to the wire-bonded contact pad is painted black to increase the emissivity and get precise infrared thermal measurements. The laser is powered up using a current source and the input current is varied from 10 mA to 100 mA. The maximum surface temperature of the laser is recorded, and the measurements are shown in **Figure 2.3**. The figure illustrates the experimental results regarding the

maximum temperature reached by a laser chip soldered on glass, glass with unfilled Through Glass Vias (TGVs), and glass with copper-filled TGVs. The input current to the laser was increased incrementally from 10 mA to 100 mA, leading to a corresponding rise in the heat generated by the laser chip. It was observed that the highest temperature increase occurred with unfilled/air-filled TGVs, while the lowest temperature increase was noted in the case of copper-filled TGVs. This underscores the effectiveness of copper-filled TGVs in facilitating heat dissipation.

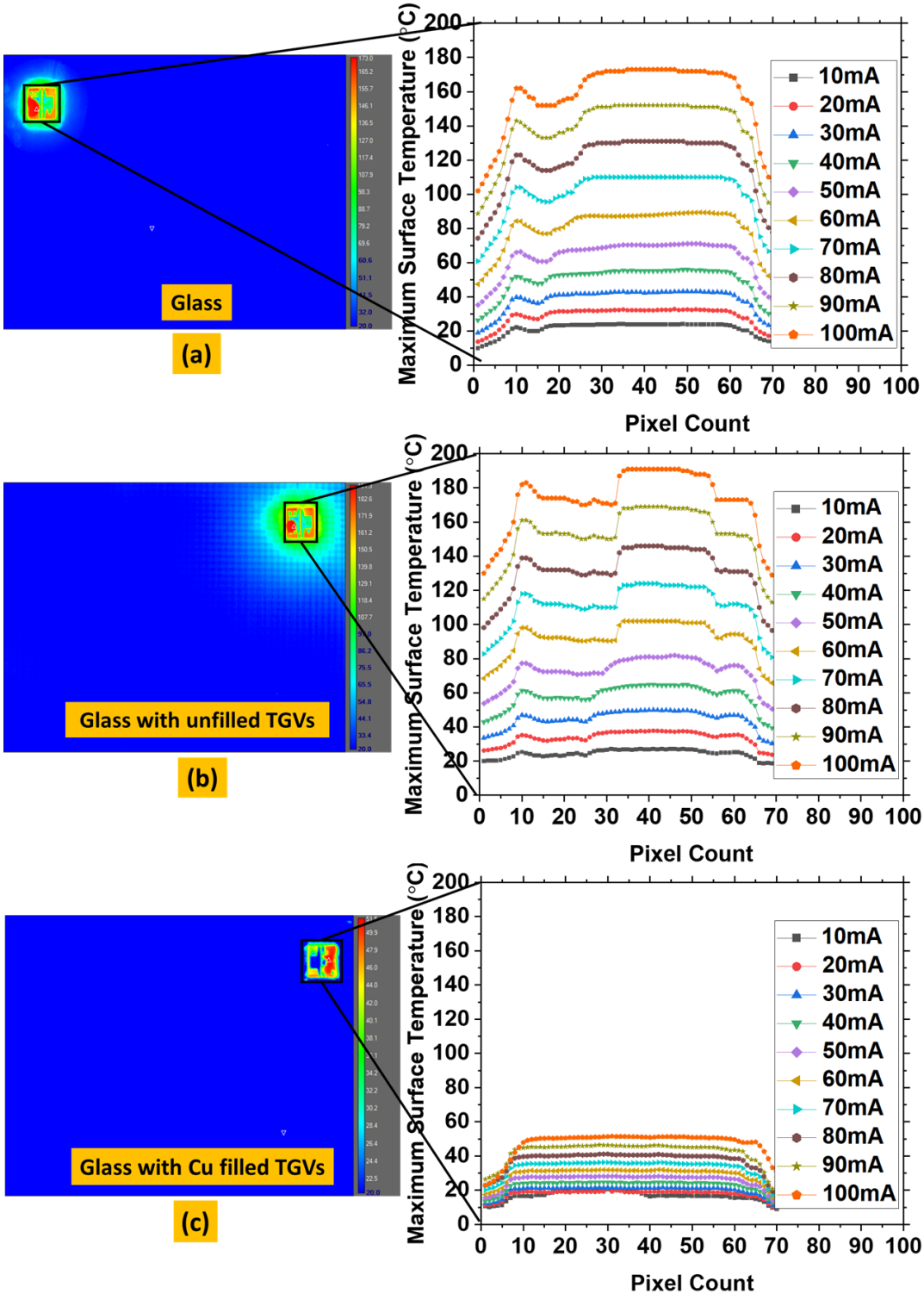


Figure 2.3: Measurement results of the maximum surface temperature of the laser chip soldered on the test vehicles with (a) glass interposer assembly (b) glass interposer with unfilled TGVs assembly and (c) glass interposer with copper filled TGVs assembly.

2.3 Simulation Results

A Finite-Element Method (FEM) simulation is setup in COMSOL© where the active waveguide in the indium phosphide laser is set as the heat source. The laser chip has a 4μm solder layer (thermal conductivity = 57 W/m.K), glass interposers and 1.61 mm thick copper (PCB thickness) underneath it. The bottom temperature of the copper was set at 20ºC. The input power of the laser chip is varied from 9.055 mW to 194.275 mW for glass interposer, 9.0074 mW to 188.689 mW for glass interposer with unfilled TGVs and from 9.0697mW to 190.7895mW for glass interposer with copper filled TGVs. These input powers are calculated from the experimental input currents and voltages. The glass interposer has a thermal conductivity of 1.2 W/m.K. The effective out-of-plane thermal conductivity is simulated for an unfilled via and a copper filled via. The effective k_z for glass with unfilled via and copper filled via is 0.8 W/m.K and 94.78 W/m.K respectively (**Table 2.1**). The in-plane thermal conductivity is 0.6 W/m.K and 2.324 W/m.K (**Table 2.1**). This demonstrates approximately 80 times increase in the out-of-plane thermal conductivity when the copper vias are incorporated in the glass interposer. The simulation results for the three test vehicles for an input current of 100 mA is shown in **Figure 2.4**.

Table 2.1: Table showcasing the effective in-plane and effective out-of-plane thermal conductivities of the test vehicles with laser chip bonded on glass, glass with unfilled TGVs and glass with copper filled TGVs.

Test Vehicles	**Effective in-plane thermal conductivity k_{xy} (W/m.K)**	**Effective out-of-plane thermal conductivity k_z (W/m.K)**
Glass	1.20	1.20
Glass with unfilled TGVs	0.60	0.80
Glass with Cu filled TGVs	2.32	94.78

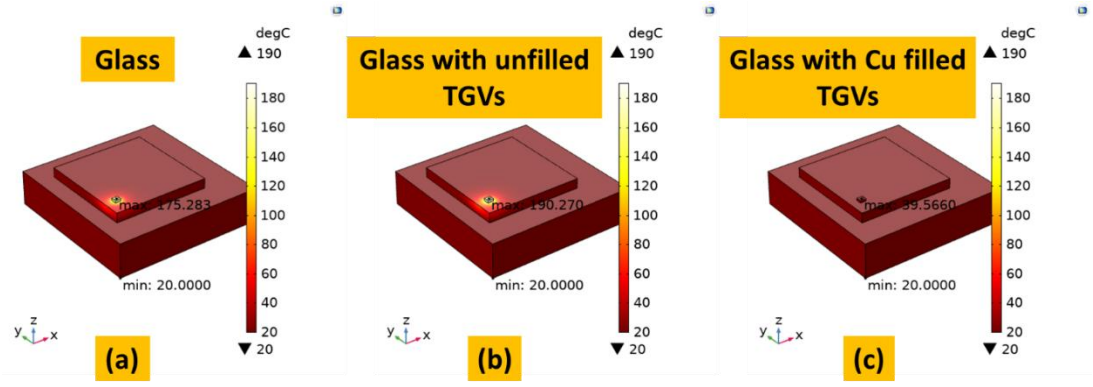


Figure 2.4: Simulated results for the maximum surface temperature of the laser chip assembled on the test vehicles with (a) glass interposer (b) glass interposer with unfilled TGVs and (c) glass interposer with copper filled TGVs.

2.3.1 Comparison of Simulation and Experimental Results

The maximum surface temperature of the laser chip is compared for the simulated and measured results. The results are shown in **Figure 2.5**. In the case of the first test vehicle with laser soldered on glass interposer, the measured and simulated results match closely, and the maximum surface temperature of the laser chip increases to a maximum of 173ºC at an input current of 100mA. Similarly, the second test vehicle where the laser chip is soldered on glass with unfilled TGVs, the measured and simulated results match very closely. The maximum surface temperature of the laser chip is increased to 191.3ºC. This is because of the low thermal conductivity of air (0.03 W/m.K) in the unfilled TGVs. However, in the third test vehicle where the laser chip is soldered on the glass interposer with copper filled TGVs, the measured and simulated results did not match well, especially at input powers above 75 mW (above 50 mA input current). There is a temperature difference of approximately 12.88ºC between the measured and simulated results at an input power of 190.7895 mW (100 mA input current). The glass interposer with copper filled TGVs is analysed further and the copper filling challenge is identified. The analysis describing the impact of copper filling on the effective thermal conductivity of a unit TGV has been detailed in the next section.

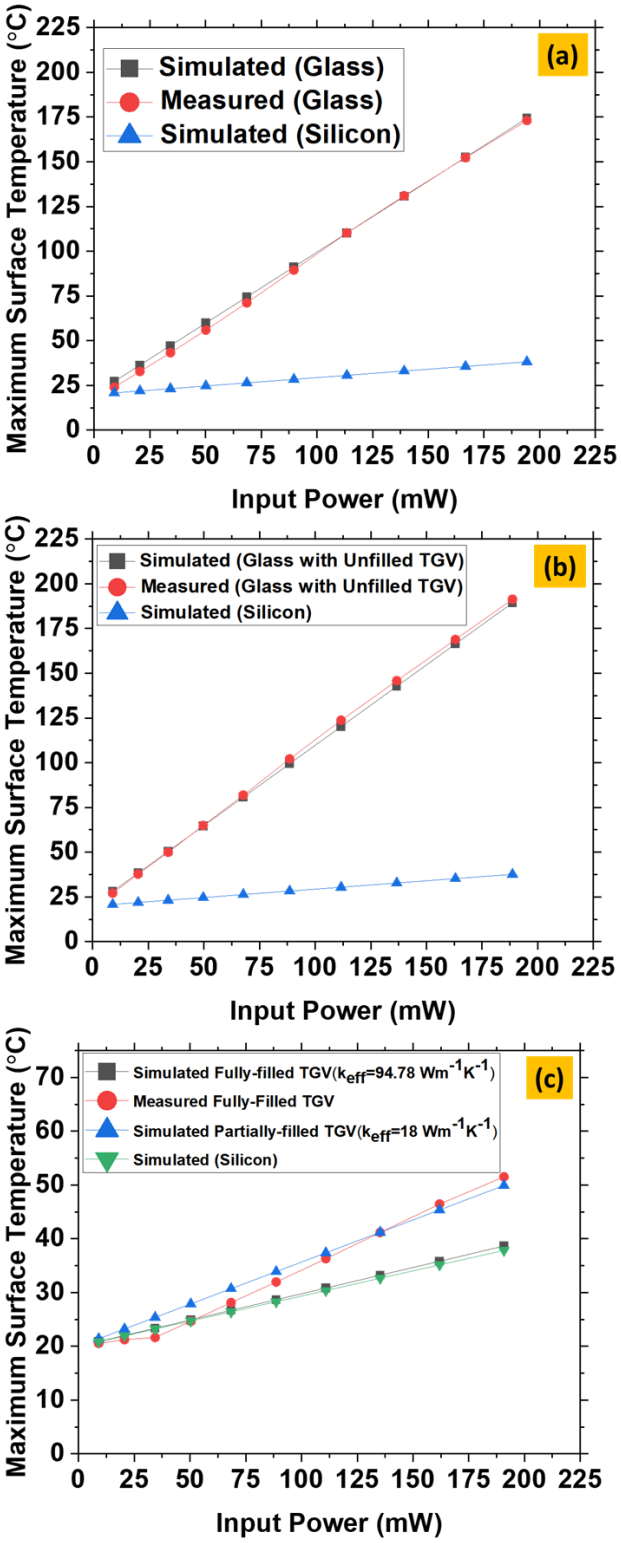


Figure 2.5: Comparison of the simulated and measured results in the three test vehicles with (a) glass interposer (b) glass interposer with unfilled TGVs and (c) glass interposer with copper filled TGVs.

Although the copper filled TGVs are instrumental in reducing the maximum temperature of the laser chip by approximately 120ºC (as compared to the case with laser chip bonded on glass interposer) the partial filling of the TGVs with copper reduces the effective out-of-plane thermal conductivity of the unit TGV from 94.78 W/m.K to 18 W/m.K. This analysis also shows that the ideal simulated results for this glass interposer with copper filled TGVs matched the thermal performance of a silicon interposer. Hence, the copper filling of the TGVs play a crucial part in heat conduction through the TGVs.

2.3.2 Sensitivity Analysis of Copper filling in TGVs

The copper filling in the TGV is identified as a challenge as the partial-filling of the via lead to inefficient heat dissipation. The conical cavity which represented the partial filling of a unit TGV is modelled. The height and bottom radius of the conical cavity in the TGV is increased from 0-425µm and 0-20µm respectively. The impact of the cavity on the effective out-of-plane thermal conductivity of glass with copper filled TGV is shown in **Figure 2.6**. This analysis shows that the partial via filling in TGVs decreased the effective thermal conductivity of the glass with TGV by approximately 10 times. The via filling in the case of the measured samples decreased the effective thermal conductivity of the glass with copper filled TGV to 18 W/m.K based on the quantitative analysis of the cross-sectioned micrograph shown in **Figure 2.7**. Note that when the input current to the laser chip is increased from 10mA to 100mA, the measured voltage incurred changes depending on the temperature of the laser chip. This then leads to minor changes in the output power of the laser chip across the three test vehicles. Although these changes in the output power are incorporated in the FEM simulation model, but the laser chip does not form a reliable heat source for thermal characterization of the TGVs due to its self-heating characteristics. In addition to this, the commercially available laser chips as discrete heat sources are expensive. Thus, a cost-effective solution to emulate the heating characteristics of electronic chips such as driver or trans-impedance amplifier (TIA) chip is needed to characterize the thermal performance of co-packaged electronic and photonic chips on the glass interposer with TGVs. This is realized through the concept of reference thermal chips which is introduced in the next chapter.

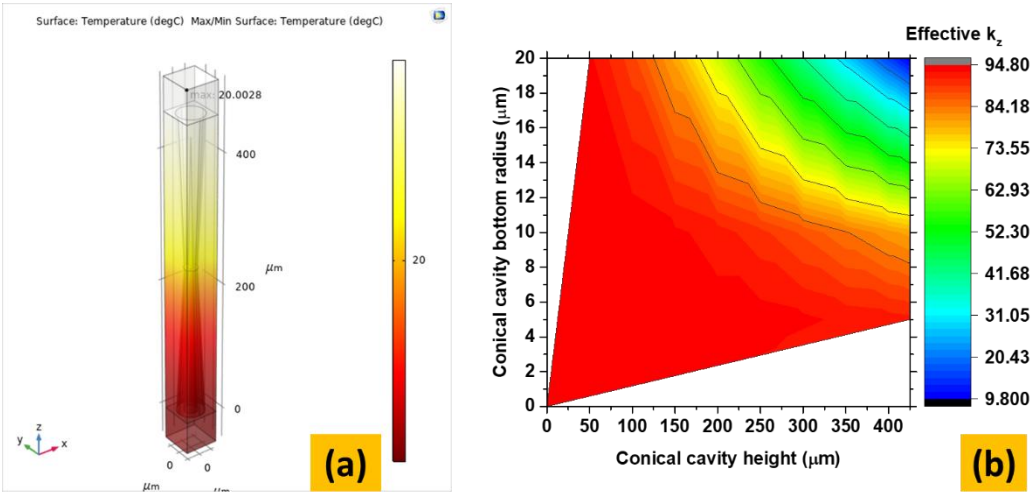


Figure 2.6: Sensitivity analysis of the impact of copper filling on the effective thermal conductivity of a copper filled TGV with (a) simulation model of the cavity in copper-filled TGV and (b) showing the simulated results.

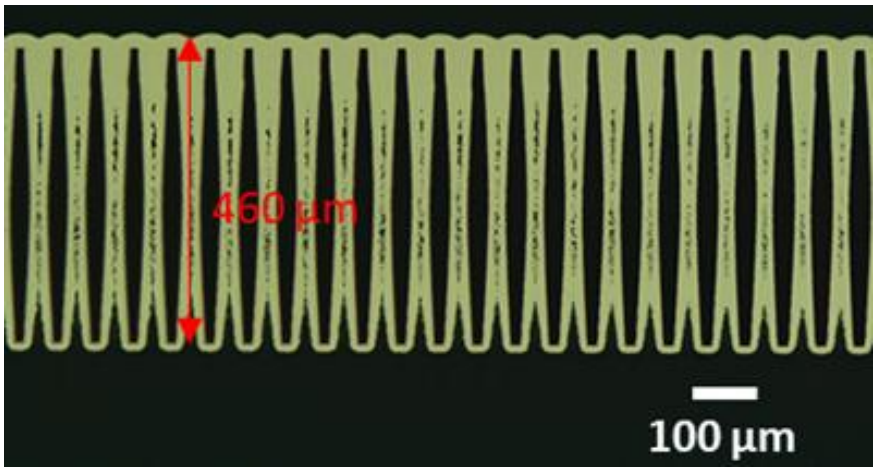


Figure 2.7: SEM Micrograph showing the cavities in the copper filling that were simulated in the sensitivity analysis.

2.4 Conclusion

The thermal dissipation performance of glass with TGVs is studied where three test vehicles with laser chips bonded on the test vehicles are analyzed. The test vehicles consist of laser chip soldered on glass interposer, glass interposer will unfilled TGVs and glass interposer with copper filled TGVs. The third test vehicle demonstrated the best cooling effect, and the maximum surface temperature of the laser chip is measured to be 51.5ºC at an input current of 100 mA. However, this performance is not matched well to the simulated results as there is a difference of approximately 12.88ºC. This was then investigated, and it was found that the via filling had a significant impact on the cooling performance of the glass interposer with copper filled TGVs. The impact of via filling on thermal conductivity of glass with copper filled TGVs is analysed using a simulated model with varying conical cavity parameters in a copper filled TGV. This analysis provides solid proof that glass with fully-filled copper TGVs can be an ideal candidate for integrated light source packaging in a co-packaged transceiver module. Apart from the light source, we need low-cost and abundant heat sources to reliably characterize the thermal performance of co-packaged electronic and photonic chips on glass interposer with TGVs. This is realized through reference thermal chips detailed in the next chapter.

2.5 References

[1] N. Margalit, C. Xiang, S. M. Bowers, A. Bjorlin, R. Blum, and J. E. Bowers, "Perspective on the future of silicon photonics and electronics," Applied Physics Letters, vol. 118, no. 22, p. 220501, 2021, doi: 10.1063/5.0050117.

[2] B. Buscaino, E. Chen, J. W. Stewart, T. Pham, and J. M. Kahn, "External vs. Integrated Light Sources for Intra-Data Center Co-Packaged Optical Interfaces," Journal of Lightwave Technology, vol. 39, no. 7, pp. 1984-1996, 2021, doi: 10.1109/JLT.2020.3043653.

[3] C. Minkenberg, R. Krishnaswamy, A. Zilkie, and D. Nelson, "Co-packaged datacenter optics: Opportunities and challenges," IET Optoelectronics, vol. 15, no. 2, pp. 77-91, 2021, doi: https://doi.org/10.1049/ote2.12020.

[4] K. Kröhnert et al., "Through Glass Vias for hermetically sealed High Frequency Application," Additional Conferences (Device Packaging, HiTEC, HiTEN, and CICMT), vol. 2019, no. DPC, pp. 000125-000140, 2019, doi: 10.4071/2380-4491-2019-DPC-Presentation_TA1_011.

[5] L. Brusberg et al., "Glass Interposer for High-Density Photonic Packaging," in Optical Fiber Communication Conference (OFC) 2022, San Diego, California, S. P. D. S. W. J. F. C. R. R. Matsuo and D. Simeonidou, Eds., 2022/03/06 2022: Optica Publishing Group, in Technical Digest Series, p. Tu3A.3, doi: 10.1364/OFC.2022.Tu3A.3. [Online]. Available: http://opg.optica.org/abstract.cfm?URI=OFC-2022-Tu3A.3.

[6] R. Ostholt, N. Ambrosius, and R. A. Krüger, "High speed through glass via manufacturing technology for interposer," in Proceedings of the 5th Electronics System-integration Technology Conference (ESTC), 16-18 Sept. 2014 2014, pp. 1-3, doi: 10.1109/ESTC.2014.6962711.

[7] S. Cho, V. Sundaram, R. R. Tummala, and Y. K. Joshi, "Impact of Copper Through-Package Vias on Thermal Performance of Glass Interposers," IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 5, no. 8, pp. 1075-1084, 2015, doi: 10.1109/TCPMT.2015.2450731.

Chapter 3: Reference Thermal Chips for 2D and 3D Co-packaging Process Development

This chapter is based on the following publication- **Parnika Gupta**, Robert Bernson, Noreen Nudds, Sean Collins, Kamil Gradkowski, Padraic E. Morrissey, and Peter O'Brien. "Reference thermal chips for 2D and 3D Co-packaging process development." In *2023 IEEE 73rd Electronic Components and Technology Conference (ECTC)*, pp. 2160-2165. IEEE, 2023.

Credit authorship contribution statement

Parnika Gupta: Writing-original draft, Experimentation, Conceptualization, Visualization, Methodology, Investigation, Formal analysis. **Robert Bernson, Noreen Nudds:** Experimentation, **Sean Collins:** 3D SolidWorks Design of Interposer , **Kamil Gradkowski:** Writing – review & editing, Supervision, **Padraic E. Morrissey and Peter O'Brien:** Writing – review & editing, Supervision, Conceptualization, Project administration, Funding acquisition.

3.1 Introduction

Co-packaged optics (CPO) offer a sophisticated solution to increased transceiver bandwidth demands by bringing the photonic engines near the ASIC switch. This enables high-density integration of electronic and photonic components, improves energy efficiency and offers cost reduction [1]. The CPO architecture adds complexity in terms of the cost associated with packaging, assembly and testing of integrated electronic and photonic modules due to high levels of integration. The low throughput and yield of photonic packaged modules has a significant negative financial impact which prevents the widespread adoption of CPO in the burgeoning high speed transceiver market [2]. The photonic packaging processes for CPO requires optimization across various domains such as thermal management, electrical I/O channel bandwidth, optical I/O coupling and mechanical stability of the package [3, 4]. The results of this optimization can then be translated to design rules which can enable standardization, resulting in improved automation capabilities which can overcome the packaging cost barrier for widespread market deployment. The

packaging process optimization is dependent on numerous factors, including chip design, fabrication timeframe, device yield, chip packaging compatibility, substrate/interposer design modifications, testing different packaging materials, process iterations and automation. These cost-decisive factors can be managed in a parallel fashion through the adoption of reference chips.

Reference chips are designed to emulate the thermal, electrical and optical packaging functionalities of the chips that are used in the final product. For example, the reference photonic chip shown in **Figure 3.1** includes all the optical components provided by a given foundry supplier on a single chip, the reference RF chip (Reference RF EIC) contains transmission line loopbacks for impedance matching; and the reference thermal chip (Reference Thermal EIC) includes heater line loopbacks to generate a heat map/load that mimics that of an electrical driver circuity. The packaging process optimization challenges are addressed as these structures are easy to design, cheaper and faster to produce, flexible in operation and reconfigurable for design iterations. These chips act as building blocks for optimizing the packaging process and testing of the thermal, electrical, optical and mechanical aspects of the co-packaged module simultaneously, in a cost-effective method.

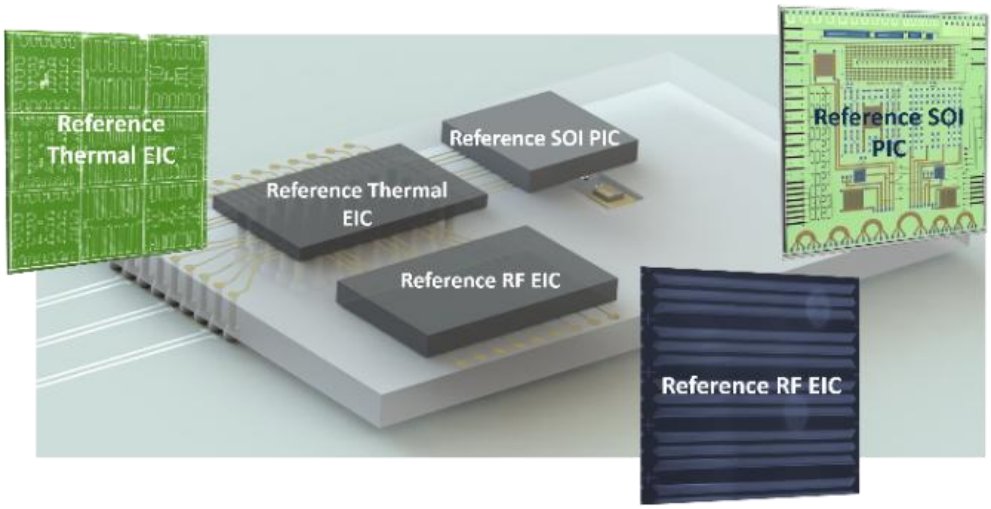


Figure 3.1: An illustration showing the concept of Reference Chips for Co-packaging process development using 2.5D co-packaged reference thermal chip, reference RF chip and reference photonic chip.

The thermal analysis of a co-packaged module becomes critical as the photonic components on the PICs are wavelength-sensitive to variation in temperature, requiring a low thermal crosstalk between the electronic and photonic chips [5, 6].

This thermal coupling challenge is escalated when the light source (e.g. a laser which is a source of heat) is integrated in the package and a thermal stabilization scheme is required to maintain the optimum operation [6, 7]. Thus, electronic components as well as optically active light sources both contribute to the thermal coupling challenge. In this chapter, we develop the concept of a reference thermal chip, evaluate its performance, and demonstrate its operation in a co-packaged configuration. We highlight how such reference PICs provide a cost-effective means for rapid development of co-packaging assembly process. They are critical in order to analyse the flow of heat between the various components of the module in order to design optimal thermal management mechanisms to be employed in the package and subsequently lead to the development of thermally-aware substrate floorplans. The gold bond pads on the reference thermal chip also allow for wire-bond/flip-chip interconnections to test bonding capability, warpage, interface materials such as TIM/underfill used in development of advanced packaging platforms.

3.2 Methodology and Analysis

3.2.1 Thermal Characterization of First-Generation Reference Thermal Chips

The first-generation reference thermal chips are designed on a 5mm × 5mm × 0.5mm silicon chip as tungsten alloy heater line loopbacks with 200µm width and varying lengths as shown in **Figure 3.2**. **Table 3.1** shows that the electrical resistance of the heater lines (as averaged for five heater loopbacks on each chip) increased with the length of the heater line across the three reference chips in a linear fashion as expected. The cross-sectional area of the heater line remains constant for the three reference chips. The Joule heating effect generated by the change in electrical resistance (and current) with the change in heater line length results in heat generated by the heater loopback ($P=I^2R$). Here, P denotes the generated Joule heat, R denotes the electrical resistance of the heater line and I denotes the current passing through the heater line loopback.

Table 3.1. Electrical resistance measurements for the heater line loopbacks on different reference thermal chips

Chip	Length of heater line (µm)	Width of heater line (µm)	Thickness of heater line (µm)	Average electrical resistance of heater loopback (kΩ)
1	4450	200	0.086	0.73±0.026
2	2450	200	0.086	0.404±0.018
3	1450	200	0.086	0.270±0.031

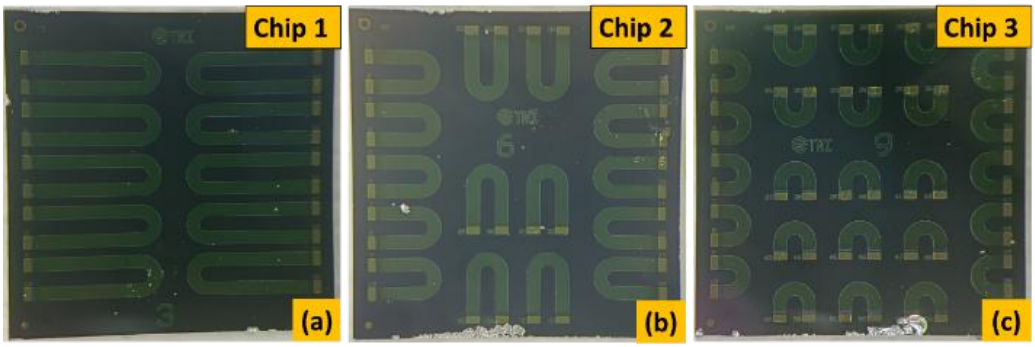


Figure 3.2: Reference Thermal chips with heater line length of (a) 4450 µm in Chip 1, (b) 2450 µm in Chip 2 and (c) 1450 µm in Chip 3.

There are several other methods of reliably measuring temperature on a silicon chip. These include either placement of a thermistor in close proximity of the DUT (device under test) or integration of an RTD (resistance-temperature detector) layer under DUT [8-10]. These methods present certain imprecisions, for example, the thermistor gives the surface temperature measurement of the area where it is surface mounted near the DUT (and an approximate surface measurement of the DUT). The measurement using RTD fabricated on the chip requires a small current to pass through the RTD that in turn generates internal heat that can affect the surface temperature measurement of the DUT (or sensitivity of the sensor), while also adding to the chip fabrication costs. The thermal calibration diodes designed as part of the chip can also be used to monitor the temperature of thermal test chips relying on its temperature sensitive behaviour. This adds fabrication complexities and cost to the chip but when carefully calibrated, can be very precise.

Another method, one which is employed in our measurements, utilizes a thermal camera, which offers a benefit of a contactless, high-speed surface temperature

mapping. The camera (FLIR© X6540sc) has an indium antimonide (InSb) sensor material, resolution of 5 µm across a pixel array of 640 × 512 pixels and a temperature accuracy of ±1°C. Since high emissivity material (approaching unity) is required for this measurement and tungsten had low emissivity (0.03), the reference chips are covered with a thin layer of graphite coating in order to approximate the blackbody conditions necessary for the surface temperature measurement. The measurement setup is shown in **Figure 3.3**.

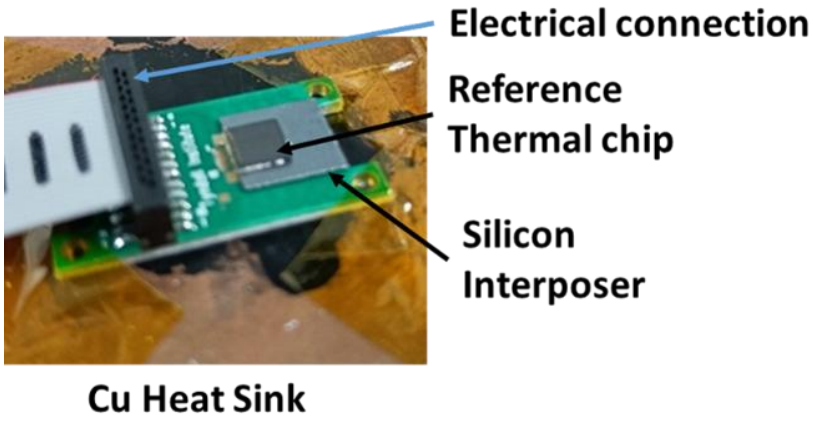


Figure 3.3: Measurement setup for recording the surface temperature of the reference thermal chip using IR thermal microscope on the top.

During the measurement, the reference thermal chip is epoxy-bonded to a 10mm x 10mm x 0.5mm silicon interposer for heat dissipation. This subassembly is then epoxy-bonded to a large copper pad on the PCB. A conductive silver epoxy (Chemtronics CW2400) was used as an adhesive for bonded interfaces throughout this chapter. The bottom of the PCB is integrated with an aluminium heat spreader that improved thermal contact with the heat sink underneath. The bond pads at the ends of the loopback structures on the reference thermal chip are wire bonded to the PCB bond pads and a Keithley 2400 source is used to input voltage levels varying from 10V-30V in the heater loopbacks. This assembly is then placed on an 8cm × 8cm × 1cm copper block which was kept constant at 20°C during the entire experiment to provide ideal heat-sinking conditions, i.e. ensure only intrinsic effects of Joule heating were analysed without the influence of the environment. The thermal measurements were performed subsequently for each of the five heater loopbacks on one side of the chip (east side on **Figure 3.2**).

The thermal camera measurements for the central heater loopback on the three chips is shown in **Figure 3.4**. It shows the temperature cross-section for a selected heater loopback on the chip surface (as presented in the inset **Figure 3.4**) on each of the three reference chip designs. The heat generated by the tungsten heater line was also dissipated in the lateral direction on the chips around the heater loopback. This lateral heat spreading on the silicon reference thermal chip can be seen by the increased temperature plane around the heater lines in **Figure 3.4**. The maximum surface temperature of each heater loopback is measured in isolation for all the reference chips.

he data in **Figure 3.4** is presented for the central heaters. Performing the same measurement on heaters further towards the edge of the chip, there is observed an increase in the maximum surface temperature of the heater loopback due to the proximity to the chip edge. However, as this difference is quite small (maximum increase of 5.8% in Chip 1, 3.7% in Chip 2, 2.89% in Chip 3), the metric of maximum surface temperature is used as a suitable performance indicator for the reference thermal chip. This metric can be used for matching the hot-spot design of reference thermal chip closer to that of the electronic chip used in the final assembly.

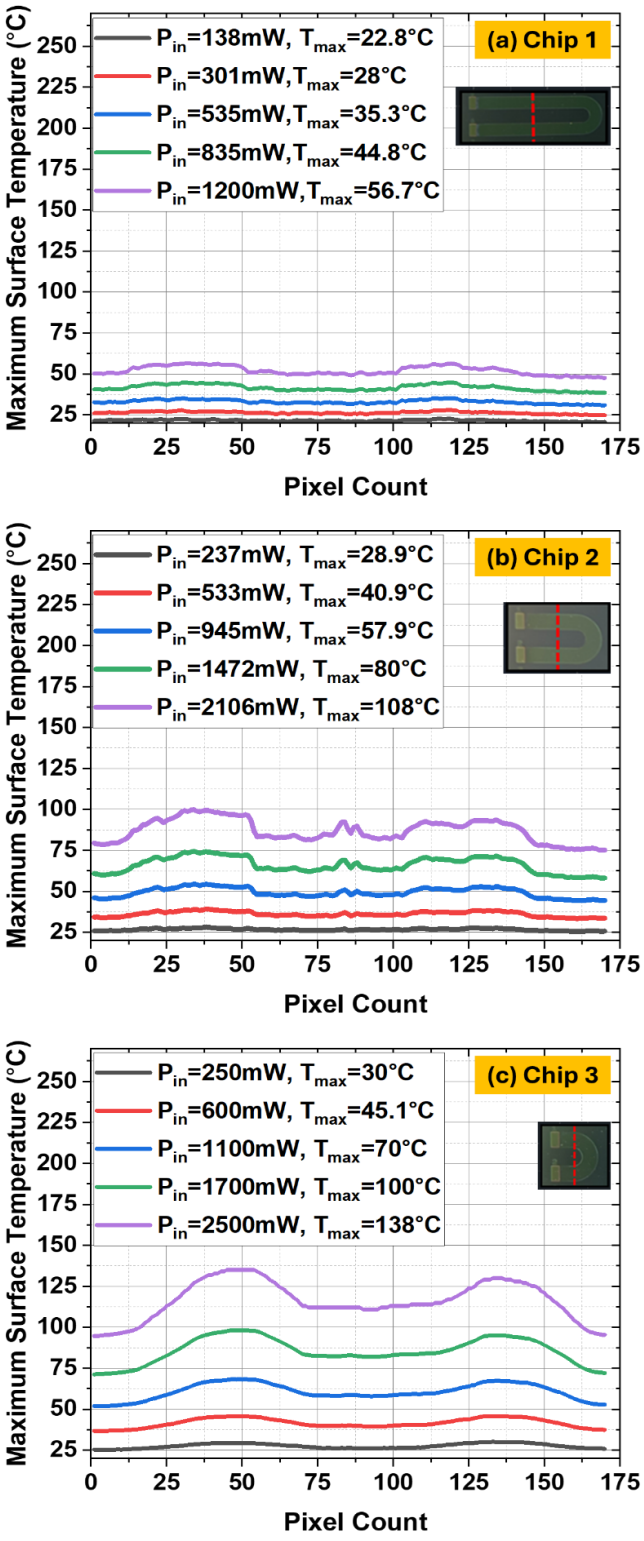


Figure 3.4: Measured data representing the increase in maximum surface temperature across the cross-sectional direction of the central heater loopback in (a) Chip 1, (b) Chip 2 and (c) Chip 3 respectively.

Figure 3.5 shows the maximum surface temperature as a function of the total thermal power generated by the heater for each Chip. The error bars show variance across all the five measured loopbacks. As the power generated by the heater loopbacks was increased, the maximum surface temperature follows in a linear fashion. The increasing surface temperature from Chip 1 to Chip 3, despite similar heat loads, is due to the shorter length of the heater loopback. This shorter length reduces electrical resistance, which in turn increases the current flowing through the heater line. The increased current results in a rise in Joule heat generated by the loopback, causing the higher temperatures.

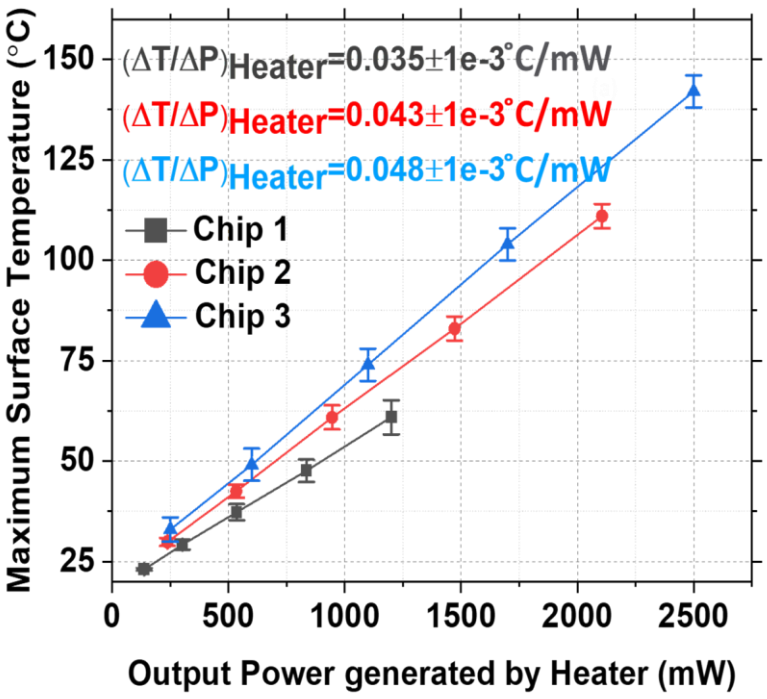


Figure 3.5: Comparison of the increase in surface temperature of different reference thermal chips with the error bars representing the measurements for each of the five heater loopbacks in each chip.

Reference thermal Chip 2 is selected for further analysis of co-packaged architectures along with the reference PIC in the next section because of its operating temperature range, which closely resembles the operating temperature range of a driver chip for photonic packages.

3.2.2 Thermal Characterization of Co-packaged Reference Thermal Chip and Reference Photonic Chip

In order to understand the thermal effects of Joule heating of the reference thermal chip on the reference PIC in different packaging architectures, the reference chips that constitute the package are assembled in either 2D or 3D configurations. The reference PIC is shown in **Figure 3.1**, where it consists of different electrical and optical elements such as DC loopbacks, edge couplers, grating couplers and microring resonators. The reference PIC is thermally inactive and optically passive; used as a test vehicle for this study. In the first case (2D), the reference thermal chip is epoxy-bonded next to (approximately 20 µm away from) the reference PIC on the silicon interposer. In the second case (3D), a reference PIC is attached to the top of the reference thermal chip. In both cases, the reference chips have the same size of 5mm × 5mm × 0.5mm. The bonding method and measurement setup is kept the same as that used in the characterization of individual reference thermal chips. The thermal camera is used for characterization of these packaging architectures by recording the maximum surface temperature of both chips, as detailed in Section 3.2.1. In this case, each of the five heaters on the thermal chip are numbered from H1 to H5. The thermal measurement setup is shown in **Figure 3.6**.

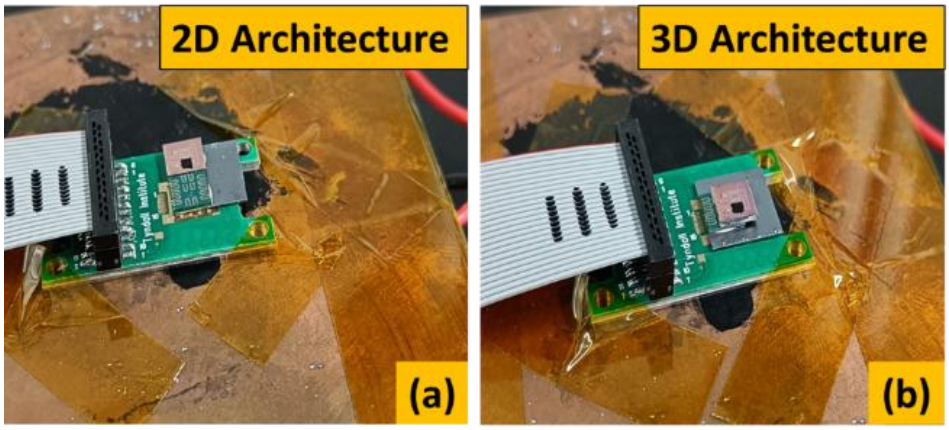


Figure 3.6: Measurement setup for recording the surface temperature of the reference thermal chip and reference PIC in (a) 2D stacked configuration with the reference chips placed side by side and (b) 3D stacked configuration with the reference PIC bonded on top of the reference thermal chip. The reference PIC has a region of interest (ROI) which is covered with a black solution for the IR thermal measurements across that area.

In order to accurately measure the surface temperature on the reference PIC, an area of approximately 1.5mm × 1.5mm is coated with a black solution as shown in **Figure**

3.6 to maximize the surface emissivity. In the first set of characterization experiments, the maximum surface temperature of this area/region of interest (ROI) on the reference PIC is recorded as the different heaters (H1-H5) are powered on consecutively. This is done so that the impact of the different spatial locations of the five different heater line structures on the reference PIC can be measured. **Figure 3.7** and **Figure 3.8** show a picture and thermal measurements performed for 2D and 3D configuration respectively for a constant thermal load about 2100 mW.

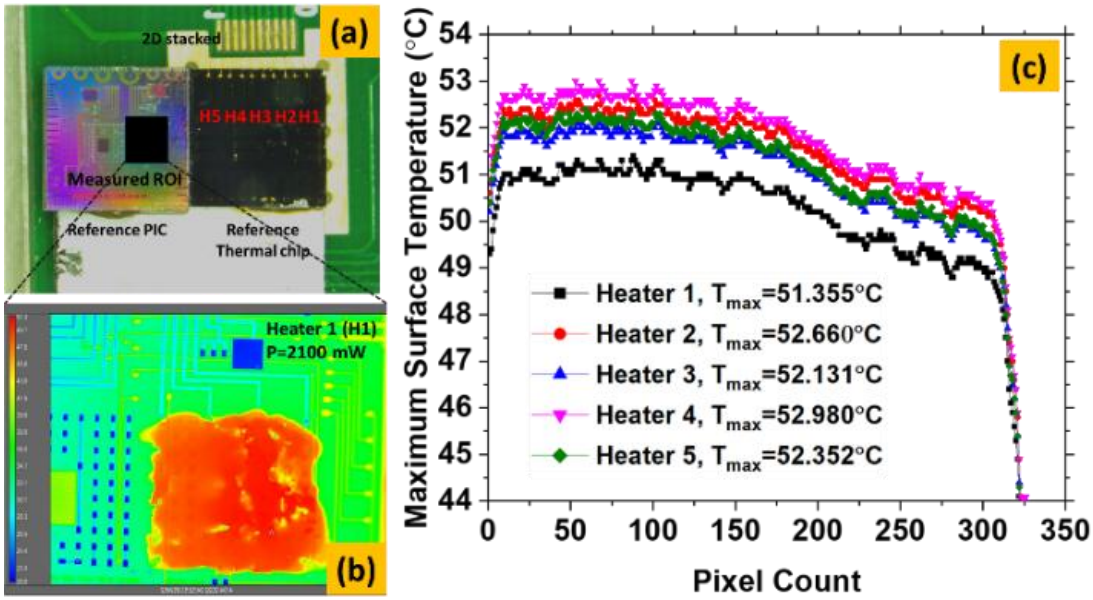


Figure 3.7: (a) 2D stacked reference PIC and reference thermal chip with the (b) surface temperature measurement of ROI on the reference PIC using thermal camera (c) and the recorded data highlighting the variation in the maximum surface temperature of the reference PIC as different heaters (H1-H5) on the reference thermal chip are switched on consecutively.

We observe that in the case of 3D stacked architecture, the maximum surface temperature at equilibrium is on average 10° higher than for the 2D case. This is a result of the shorter heat flow path between the two chips in 3D configuration (i.e. lower thermal resistance) as compared to the longer heat flow path through the silicon interposer in the case of 2D configuration (i.e. corresponding to higher thermal resistance).

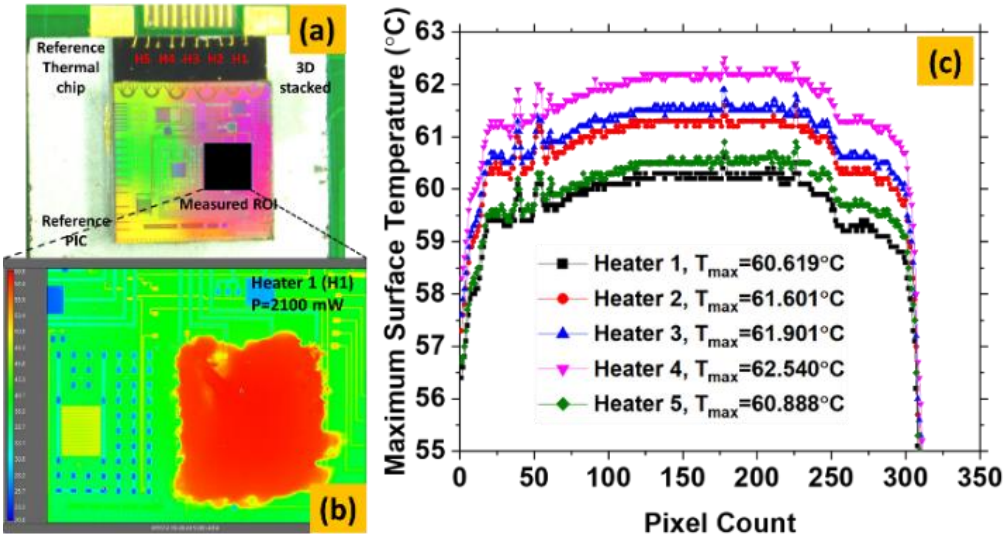


Figure 3.8: (a) 3D stacked reference PIC and reference thermal chip with the (b) surface temperature measurement of ROI on the reference PIC using thermal camera (c) and the recorded data highlighting the variation in the maximum surface temperature of the reference PIC as different heaters (H1-H5) on the reference thermal chip are switched on consecutively.

The variation is within ±1°C range that is the same as the accuracy range of the thermal camera. This can be attributed to the high thermal conductivity of silicon, which flattens the temperature gradient in equilibrium conditions.

Consequently, **Figure 3.9** shows average maximum temperature of the reference chips as a function of thermal load. The temperature variation of the Reference PIC is small across the entire range of thermal loads, meaning that, owing to the high thermal conductivity of the substrate, there is minimal dependence of the temperature on position of the heat source relative to the reference PIC for the distance scales employed in the experiment. The impact of the small difference in distances between the reference thermal chip and the reference PIC can be observed when calculating $\Delta T/\Delta P$. This value is higher for the 3D stacked configuration, showing that it is more susceptible to heat sources. No such difference is seen in the slope of the temperature of individual heaters of the reference thermal chip. Larger variations in the case of reference thermal chips are due to proximity to the edge – as the heaters are closer to the edge of the chip, their temperature will be higher than for those located centrally. It can be foreseen that the spatial positions of the heaters would have more pronounced effect on the temperature of the PIC in case where a low thermal conductivity material was used as an interposer/substrate.

It would also lead to a larger temperature difference between the architectures in 3D stacked architecture as compared to the 2D architecture. Thus, the analysis of ΔT/ΔP using the reference thermal chips is essential for selection of the right substrate materials for thermal management in photonic packages.

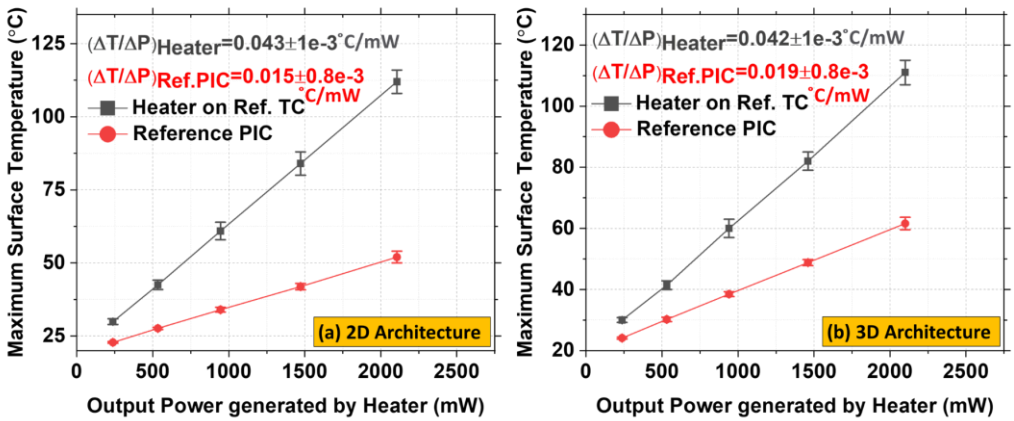


Figure 3.9: Comparison between the maximum surface temperature of the reference thermal chip (Ref. TC) and reference PIC at different power levels, where the error bars represent the measurements recorded for the operation of each heater loopback (H1-H5).

3.2.3 Optical Characterization of Co-packaged Reference Thermal Chip and Reference Photonic Chip

As mentioned previously, many passive and active optical components in a PIC are sensitive to changes of temperature. The reference chips allow for a quick way of analysing the optical impact of Joule heating on these structures in conditions they will observe during normal operation of the module. In the previous section, we assembled a co-packaged system of reference thermal chip and reference PIC in two different configurations. Using the same system, we can now directly measure the impact of thermal heating on the optical performance of grating couplers on the reference PIC.

The optical measurement is carried out by coupling light from a fiber array into the reference PIC and then from the reference PIC back into the fiber array through loopback structures on the PIC, when the reference thermal chip is powered using different heat loads. The grating coupler (GC) loopbacks with a 10° insertion angle are used as the I/O structures in the reference PIC. A micro-ring resonator is also present near the waveguide loopback connecting the input GC and output GC.

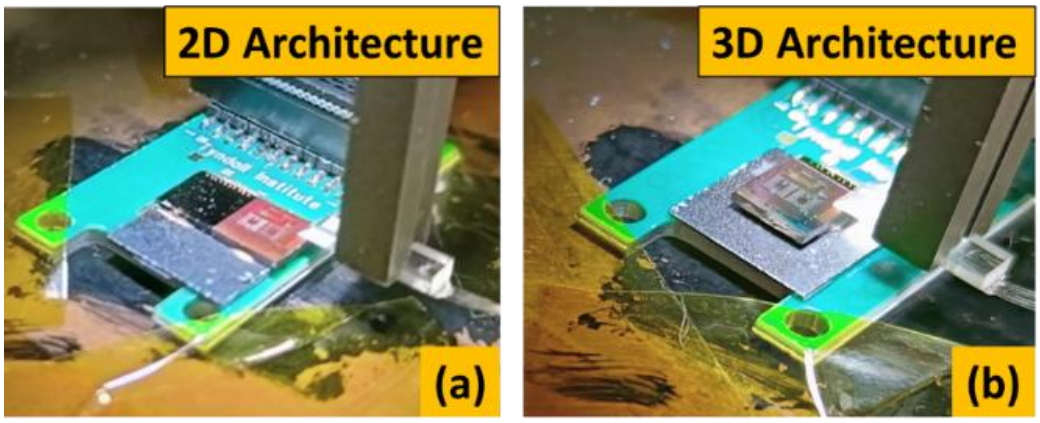


Figure 3.10: Measurement setup for the optical characterization of the reference PIC when different heaters on the reference thermal chip are switched on. The fiber array is used for coupling in/out of the grating coupler loopback structure on the reference PIC.

A 1310nm SLD source is used as the input and an optical spectrum analyser is used to measure the (normalized to the input) transmitted light spectrum. The fiber-chip coupling setup for 2D and 3D stacked configurations is shown in **Figure 3.10** where the fiber array is coupled to the grating coupler loopback near the edge of the reference PIC.

The recorded data for 2D and 3D architectures is shown in **Figure 3.11(a)** and **Figure 3.11(b)** respectively, which highlights a red-shift in the central wavelength of the coupled light with rising Joule heating effect due to the thermo-optic effect of silicon in both cases [11]. This red-shift is approximately 2nm for 2D stacked architecture which was due to the higher reference PIC temperature. There is a shift in central wavelength for the 3D stacked architecture, however the shift is not quantifiable due to the degraded ring performance. The spikes seen in **Figure 3.11(a)** are due to the presence of a MRR (micro-ring resonator) next to the waveguide connecting grating couplers in the loopback.

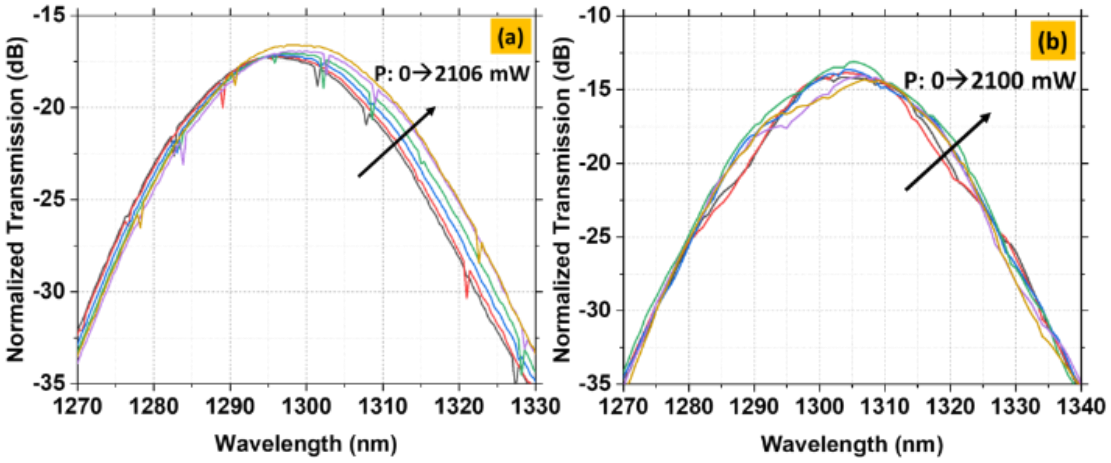


Figure 3.11: Optical Spectrum analyser results for the input SLD source and the light coupled out of the (a) 2D stacked reference PIC and (b) 3D stacked reference PIC when H4 on the reference thermal chip is operated at increasing powers ranging from 237 mW to 2100 mW. The central wavelength is red-shifted in the case of 2D and 3D stacked architectures respectively.

This result helps us get an insight into the optical effect of the higher reference PIC surface temperature in the case of 3D stacked architecture as compared to the 2D stacked architecture (coupled central wavelength red-shifted by approximately 0.359 nm/^{o}C). This red-shift can be detrimental to the wavelength-specific operational capability of photonic circuitry in the package. In order to prevent this wavelength change, either the temperature-sensitive optical components on the reference PIC should be placed at a sufficient distance from the hot spot or certain spot-cooling solutions must be employed to dissipate heat from the reference thermal chip. These tests employing the reference chips can help with design decisions where the thermal coupling between the chips does not severely affect the package performance.

3.3 Conclusion and Future Work

In this chapter the concept of reference thermal chips has been introduced and the characterisation of the first-generation devices has been experimentally evaluated. Heater loop back lines on the thermal reference chips were designed to mimic the hotspots on an electronic chip and were used to demonstrate the suitability of such devices to make advanced CPO architectures in 2.5D and 3D configurations.

The heat dissipated by the reference thermal chips also lead to an increase in the surface temperature of the reference PIC in both 2D and 3D stacked configurations. The reference PIC surface temperature in the 3D stacked architecture increased by approximately 19% higher as compared to the 2D stacked architecture, which is an indicator of the package architecture effects. The $\Delta T/\Delta P$ parameter derived from the thermal measurements can act as a figure of merit for the selection of a packaging platform, which allows for less thermal coupling between the electronic and photonic chips. The temperature rise is also reflected in the optical characterization of the reference PIC where the coupled central wavelength red-shifted for the 2D and 3D stacked packages respectively. This pre-emptive testing can further lead to thermally-aware substrate floor planning in photonic packages. Further work and analysis is required for optimized design of the reference thermal chip to enable closer resemblance to the thermal profile of hot spots on a driver chip. These reference chips will also enable design rule development for glass interposers through thermal, optical and RF testing. For example, the reference thermal chip, reference PIC and reference RF chip can be used to test the bonding capability of a glass interposer as the first test towards assembly process optimization. The next step is to evaluate the minimum spacing between the reference thermal chip and reference PIC on this interposer where we have low thermal crosstalk and effective heat dissipation using through glass vias. This would then result in a design rule for photonic packages developed on the glass interposer platform.

3.4 References

[1] C. Minkenberg, R. Krishnaswamy, A. Zilkie, and D. Nelson, "Co-packaged datacenter optics: Opportunities and challenges," IET Optoelectronics, vol. 15, no. 2, pp. 77-91, 2021, doi: https://doi.org/10.1049/ote2.12020.

[2] N. Margalit, C. Xiang, S. M. Bowers, A. Bjorlin, R. Blum, and J. E. Bowers, "Perspective on the future of silicon photonics and electronics," Applied Physics Letters, vol. 118, no. 22, p. 220501, 2021, doi: 10.1063/5.0050117.

[3] R. Mahajan et al., "Co-Packaged Photonics For High Performance Computing: Status, Challenges And Opportunities," Journal of Lightwave Technology, vol. 40, no. 2, pp. 379-392, 2022, doi: 10.1109/JLT.2021.3104725.

[4] K. Hosseini et al., "8 Tbps Co-Packaged FPGA and Silicon Photonics Optical IO," in 2021 Optical Fiber Communications Conference and Exhibition (OFC), 6-10 June 2021 2021, pp. 1-3.

[5] K. Gradkowski et al., "Thermal challenges for packaging integrated photonic devices," in 2016 6th Electronic System-Integration Technology Conference (ESTC), 13-15 Sept. 2016 2016, pp. 1-5, doi: 10.1109/ESTC.2016.7764516.

[6] L. Ranno et al., "Integrated Photonics Packaging: Challenges and Opportunities," ACS Photonics, vol. 9, no. 11, pp. 3467-3485, 2022.

[7] B. Buscaino, E. Chen, J. W. Stewart, T. Pham, and J. M. Kahn, "External vs. Integrated Light Sources for Intra-Data Center Co-Packaged Optical Interfaces," Journal of Lightwave Technology, vol. 39, no. 7, pp. 1984-1996, 2021, doi: 10.1109/JLT.2020.3043653.

[8] R. Sattari, H. van Zeijl, and G. Zhang, "Design and Fabrication of a Multi-Functional Programmable Thermal Test Chip," in 2021 23rd European Microelectronics and Packaging Conference & Exhibition (EMPC), 2021: IEEE, pp. 1-7.

[9] B. Siegal and J. Galloway, "Thermal test chip design and performance considerations," in 2008 Twenty-fourth Annual IEEE Semiconductor Thermal Measurement and Management Symposium, 2008: IEEE, pp. 59-62.

[10] H. Oprins et al., "Experimental thermal characterization and thermal model validation of 3D packages using a programmable thermal test chip," in 2015

IEEE 65th Electronic Components and Technology Conference (ECTC), 2015: IEEE, pp. 1134-1141.

[11] L. Liu, B. Zhu, and H. ki Tsang, "Thermo-optic tunable silicon grating coupler," in Conference on Lasers and Electro-Optics/Pacific Rim, 2015: Optical Society of America, p. 27P_8

Chapter 4: Thermal and Electrical Study of Glass Interposers in Co-Packaged Electronic-Photonic Systems

---

This chapter is based on the following publication- **Parnika Gupta**, Arun Kumar Mallik, Kevin Krohnert, Sylwester Latkowski, Chigo Okonkwo, Saif Alomari, Das Soumitra Kumar, Kamil Gradkowski, Padraic E. Morrissey, and Peter O'Brien. "Thermal and Electrical Study of Glass Interposers in Co-Packaged Electronic-Photonic Systems." *IEEE Transactions on Components, Packaging and Manufacturing Technology* (2025).

Credit authorship contribution statement

Parnika Gupta: Writing-original draft, Experimentation, Conceptualization, Visualization, Methodology, Investigation, Formal analysis. **Arun Kumar Mallik:** Experimentation. **Kevin Krohnert:** Glass Interposer Fabrication, **Saif Almoari**: RF testing, **Kamil Gradkowski:** Writing – review & editing, Supervision, **Das Soumitra Kumar**- Project Management, **Sylwester Latkowski, Chigo Okonkwo**, **Padraic E. Morrissey and Peter O'Brien:** Writing – review & editing, Supervision, Conceptualization, Project administration, Funding acquisition.

4.1 Introduction

Due to the escalating performance demands of data centers and HPC (High-Performance Computing) systems, traditional pluggable optical transceivers face challenges in keeping up with the rapidly increasing bandwidth density and energy efficiency requirements [1]. Co-packaged optics (CPO) emerges as a solution by integrating photonic devices in close proximity with high-performance electronics on the same package substrate through advanced integration schemes. CPO significantly reduces SerDes (Serializer/Deserializer) distances, thereby substantially reducing power consumption [2].

Various integration schemes for transceivers exist, including monolithic, 2D, 2.5D, or 3D integration approaches [3], involving either permanently attached transceivers

(e.g., solder reflow assembly) or those inserted into electrical sockets. These methods offer diverse strategies for effectively combining electronic and photonic components to meet the evolving demands of data center architectures [1, 4].

In scenarios involving hundreds of channels or more, the utilization of interposers for 2D or 3D integration facilitates the combination of driving electronic integrated circuits (EICs) with photonic ICs (PICs), thereby enhancing power efficiency. The integration of EICs and PICs through such interposers helps alleviate electrical interconnect loss by minimizing the required reach and the number of electrical transition points [5].

This co-packaging approach involves bringing optical and electrical chips into close proximity using 2.5D interposers, enabling the realization of ultra-high bandwidth channels with reduced power consumption compared to conventional packages assembled on boards [6, 7]. However, thermal crosstalk between EICs and PICs in such co-packaged systems can impact the optical functionality of thermally sensitive components on the PIC (such as micro-ring resonators, amplifiers etc.) [8-10].

The thermal isolation feature of glass interposers for co-packaging EICs and PICs can be leveraged for targeted thermal management [9-12].

Through Glass Vias (TGVs) in these glass interposers aid in dissipating heat generated by electronic chips locally, while the low thermal conductivity of glass prevents thermal crosstalk between electronic and photonic chips. TGVs and redistribution layers (RDLs) within the glass interposer facilitate electrical connections between assembled integrated circuits and the PCB [13], as illustrated in **Figure 4.1**.

The literature discusses the enhancement in thermal performance of glass interposers with the implementation of TGVs [12, 14]. Cho et al., also highlight that increasing the effective thermal conductivity of the TGVs and interconnects beyond 100 W/m.K leads to an insignificant change in the out-of-plane thermal resistance of a glass interposer assembly [12]. However, the value of this effective thermal conductivity, beyond which the heat dissipation through the TGVs stagnates, is dependent on the interposer's volume for heat conduction, as discussed through this chapter. This study seeks to address the gap between the constrained heat dissipation capabilities of

Through Glass Vias (TGVs) and the necessity for integrating vapor chambers into Printed Circuit Boards (PCBs) (as denoted by reference [14]).

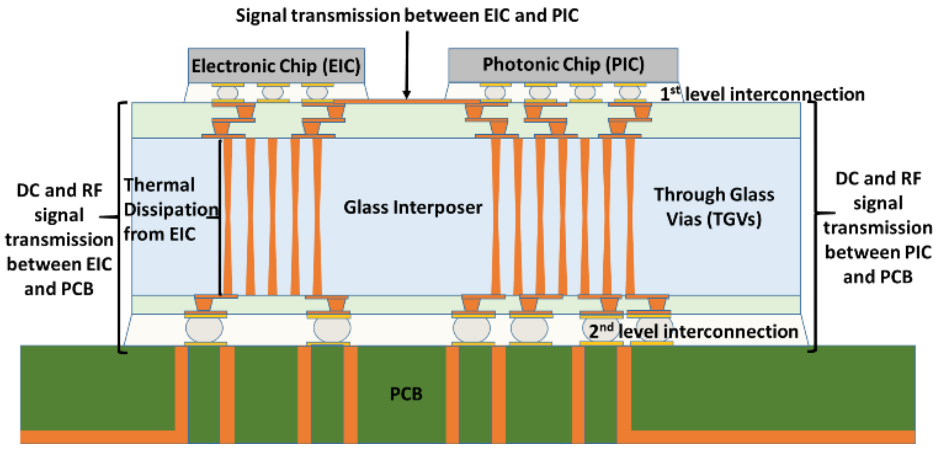


Figure 4.1: A 2.5D glass interposer package consisting of co-packaged electronic (EIC) and photonic (PIC) chips bonded on the glass interposer (first-level interconnections); which is subsequently bonded on the PCB (second-level interconnections).

This chapter involves design, assembly and characterization of the glass interposer for thermal analysis. The assembled glass interposer is referred to as a "thermal test vehicle", which undergoes thermal characterization.

The TGVs also play a critical role in reducing channel losses compared to Through Silicon Vias (TSVs) [15]. In this research, the focus lies on investigating the insertion loss and return loss associated with co-packaging EICs and PICs on a glass interposer. The investigation involves three design scenarios:

1. Transmission Lines on Glass: The electrical transmission between EIC and PIC on the glass interposer is characterized using co-planar waveguide (CPW) transmission lines on the glass substrate.
2. Glass Interposer: The study examines signal transmission through CPW transmission lines, TGVs, microvias, and Ball Grid Array (BGA) pads on the glass interposer.
3. Electrical Test Vehicle: The effect of packaging on signal transmission through the glass interposer is analyzed by characterizing a glass interposer packaged on the PCB, referred to as an "electrical test vehicle".

The design of glass interposer (both thermal and electrical) is discussed in section 4.2. The assembly process and characterization of the thermal test vehicle is discussed in

section 4.3. Section 4.3 also analyzes the impact of variation in TGV pitch on heat dissipation performance of the glass interposer. Similarly, the assembly process and characterization of the electrical test vehicle is discussed in section 4.4. This section also includes the characterization and analysis of the three design scenarios mentioned above.

4.2 Design of Glass Interposer for Thermal and Electrical Characterization

The test vehicles for thermal and electrical characterization of the glass interposer are constructed with a 460 µm thick Borofloat® Schott 33 glass core featuring hourglass-shaped copper-filled TGVs [8]. This core is stacked between polyimide layers both above and below, as depicted in **Figure 4.2**, with a single polyimide layer on the bottom and two polyimide layers on top of the core. The metal wiring on top of the glass surface and polyimide layer (1st polyimide layer) on the upper side is denoted as RDL1 and RDL2 (redistribution layers 1 and 2), while that on the lower side is termed as Backside RDL (BRDL). These copper lines are 3 µm thick.

To mitigate stress in the polyimide layers, the pads are designed with rounded corners, and the microvias are arranged in a staggered configuration (**Figure 4.2(a)**).

The larger pads (exceeding 300×300 µm²) incorporate holes to prevent cracks resulting from outgassing during fabrication and soldering. The Under Bump Metallization (UBM) pads on the glass interposer corresponding to the pads on the chip intended for soldering comprises a material stack including gold, copper and nickel, aimed at enhancing solder adhesion during chip bonding onto the glass interposer. The fabrication process of the glass interposers is detailed in our previous work [8].

4.2.1 Design of Glass Interposer for Thermal Characterization

The thermal characterization of the glass interposer requires a heat source, such as a reference thermal chip that has tungsten heater loopbacks acting as hotspots [16]. The glass interposer for thermal characterization comprises of UBM pads and a sizable gold pad atop the second polyimide layer, as seen in **Figure 4.2(a)**. These components serve two different purposes: facilitating the soldering of reference thermal chip pads to corresponding UBM pads and aiding in the thermal spreading of heat generated by

the reference thermal chip respectively. The microvias establish the connection between the UBM pad/gold pad and RDL2 on the 1st polyimide layer. RDL2, in turn, is connected to RDL1 situated atop the glass core via microvias. TGVs within the glass interposer core establish the connectivity between RDL1 and the BRDL on the lower surface of the glass core, as detailed in **Figure 4.2(a)**. The diameter of the TGVs is 50 µm. The pitch of the TGVs under the reference thermal chip is varied from 100 µm to 400 µm. Uniform TGV pitch distribution is preferred here for comparing heat dissipation. Non-uniform TGV pitch distribution in the interposer is also feasible.

Subsequently, on the lower surface of the glass core, microvias within the backside polyimide layer connect the BRDL to the Ball Grid Array (BGA) pads. These circular BGA pads on top of the backside polyimide layer feature a diameter of 250 µm and a pitch of 500 µm (refer to **Table A.1** in Appendix A). Thus, the DC connections follow a path, commencing from the UBM pads (bonded to the chip pads through solder) on the 2nd polyimide layer. These connections then fan out on both sides of the large gold pad, as seen in **Figure 4.3(a)**. The thermal connection starts with a large gold bond pad atop the 2nd polyimide layer, designated for thermal spreading, connecting to a network comprising several RDL2 pads and a large RDL1 pad through a matrix of microvias. The RDL1 pad is then linked to the same sized (4.5×5 mm^2) backside RDL pad through thermal TGVs featuring different pitches (100 µm, 200 µm, 300 µm, and 400 µm).

Subsequently, the backside RDL pad connects to the BGA pads through microvias, establishing the thermal link to the PCB (**Figure 4.2(a)**). Appendix A (**Table A.1**) provides details about the sizes of the different components in the glass interposer used for thermal characterization.

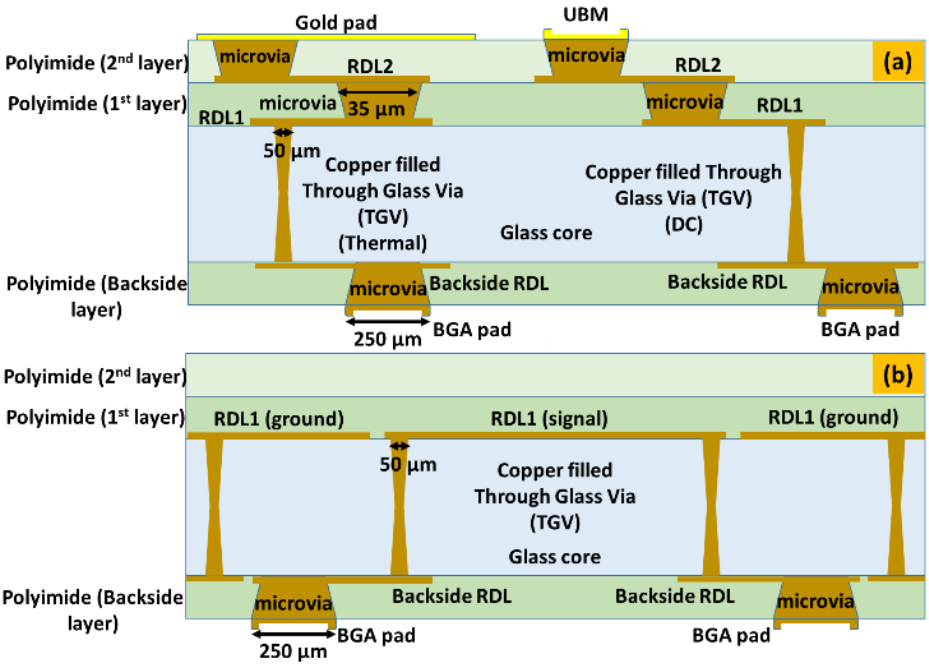


Figure 4.2: Details of the glass interposer stackup for (a) thermal characterization with different components such as BGA pads, thermal and DC connection TGVs, microvias, RDL wiring and UBM; (b) electrical characterization with different components such as RDL wiring, signal and ground TGVs, microvias and BGA pads.

4.2.2 Design of Glass Interposer for Electrical Characterization

The stackup of the glass interposer for electrical characterization mirrors that of the thermal characterization stackup, excluding the utilization of UBM, RDL2, and microvias connecting RDL2 to RDL1 (**Figure 4.2(b)**). The Ground-Signal-Ground (GSG) conductor-backed coplanar waveguide (CBCPW) transmission lines on the top and bottom of the glass core (RDL1 and backside RDL) are interconnected through TGVs, as seen in **Figure 4.2(b)**.

These CBCPW transmission line traces, measuring 100 µm in width, are positioned alongside coplanar ground plates on both top and bottom of the glass core (RDL1 and backside RDL), maintaining a spacing of 18 µm. TGVs establish connections between the signal lines on top and bottom of the glass core. A mesh of TGVs (pitch of 500 µm) also facilitates ground stitching between the ground plates on top and bottom of the glass core, as seen in **Figure 4.3(b)**.

Subsequently, the signal lines and ground plate constituting the backside RDL are linked to the BGA pads through microvias. These BGA pads are then soldered onto

the PCB to enable the electrical characterization of the glass interposer. The glass interposer for electrical characterization consists of RDL1, TGVs, BRDL, microvias connecting BRDL-BGA pads and BGA pads. The length (L) of RDL1 transmission line in the glass interposer is varied (3 mm, 4 mm, 5 mm, and 6 mm). Appendix A (**Table A.2**) provides details about the sizes of the different components in the glass interposer used for electrical characterization.

4.3 Assembly and Characterization of Thermal Test Vehicle

4.3.1 Assembly of Thermal Test Vehicle

The assembly of the thermal test vehicle includes the reference thermal chip, SAC 305 microbumps, glass interposer, Bi-Sn bumps, underfill and PCB. The glass interposer utilized measures 13×7 mm^2 and accommodates 25×14 BGA pads on the backside. Thermal performance analysis of the TGVs within the glass interposer is conducted using a reference thermal silicon chip measuring 5×5×0.5 mm^3 as the heat source as discussed in chapter 3 [16].

To establish thermal/electrical contact between the reference thermal chip and the glass interposer, fifty SAC 305 solder balls (comprising 96.5% tin, 3% silver, and 0.5% copper) with a diameter of 50 μm are deposited onto the gold pads (measuring 100×200 μm^2) of the reference thermal chip using the SB^2 Pactech jet machine.

Following solder jetting; the subsequent step involves flip-chip bonding of the reference thermal chip to the glass interposer. The reflow process for this bonding is conducted at 250°C for 10 seconds, as elaborated in Appendix A (**Figure A.1**). **Figure 4.4(a)** depicts the top view of the flip-chipped reference thermal chip on the glass interposer. Subsequently, this glass interposer subassembly shown in **Figure 4.4(a)** is prepared for bonding onto the PCB.

To facilitate DC electrical connection to the heater loopbacks on the reference thermal chip, a custom PCB is designed and manufactured using FR4 material with a thickness of 1.6 mm and featuring four routing layers. The BGA pads on the top side of the PCB are precisely aligned with those on the bottom of the interposer. Among these pads, 10 pairs of BGA pads (each with a diameter of 250 μm) are linked to the pads of the reference thermal chip for DC connection, while the remaining pads serve to provide thermal spreading and mechanical stability to the entire package.

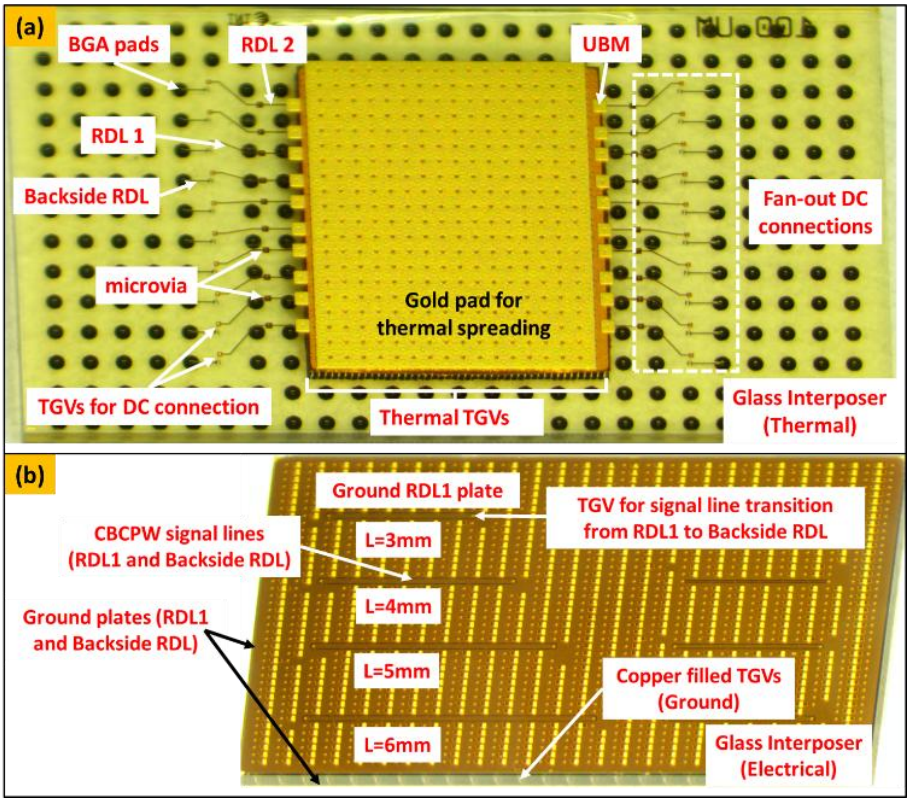


Figure 4.3: Perspective view of the fabricated glass interposer for (a) thermal characterization with 100 µm pitch thermal TGVs in the interposer; (b) electrical characterization which includes CPW transmission lines on top and bottom of the glass surface which is interconnected through TGVs.

The connection between the interposer and the PCB is established using low-temperature-melting 250 µm diameter Bi-Sn solder balls, which are deposited onto the 250 µm diameter gold pads of the PCB using a stencil and tacky solder flux. This lower melting point solder is essential because the reflow temperature must be lower than that used for the flip-chip bonding of the reference chip onto the interposer earlier (**Figure 4.4(a)**). These solder balls undergo a primary reflow process to ensure a uniform solder surface for precise placement of the glass interposer subassembly.

Following the attachment of Bi–Sn solder balls on the PCB, a second reflow process enables the bonding of the subassembly (consisting of reference thermal chip and glass interposer) with the PCB. The same temperature reflow profile utilized for solder ball attachment on the PCB is applied (refer to **Figure A.2** in Appendix A).

The Bi-Sn solder balls on the PCB start to melt when the temperature reaches 155 °C, bonding to the glass interposer BGA pads during N_2 cooling. The set temperature is

maintained higher than the actual melting temperature of Bi-Sn solder balls due to the temperature difference between the surface of the interposer and inside the oven temperature.

To further alleviate mechanical stress, an underfill epoxy (EPOTEK 301-2) is applied between the chip and glass interposer, as well as between the glass interposer and the PCB. This final assembly is cured for 36 hours at room temperature. **Figure 4.4(b)** illustrates the top view of the cured final assembly of the thermal test vehicle, while the cross-section of this test vehicle is depicted in **Figure 4.4(c&d)**. This cross-section shows the hourglass shaped thermal TGVs in **Figure 4.4(c)** and the bonding of the reference thermal chip, glass interposer and PCB in **Figure 4.4(d).** The assembly process of the thermal test vehicle is also summarized in Appendix A (**Figure A.3**).

The FR4 PCB utilized for thermal characterization is 1.6 mm thick with a tolerance of ±10% and incorporates BGA bond pads with a pitch of 500 µm on the topside, aligning with the BGA pads at the bottom of the glass interposer.

4.3.2 Characterization of Thermal Test Vehicle

The heater loopbacks fabricated on the reference thermal chip serve as localized heat sources, generating hotspots on the chip's active surface. This chip is bonded onto the glass interposer, featuring varied pitches of the 50 µm diameter thermal TGVs at 100 µm, 200 µm, 300 µm and 400 µm. Activation of the heater loopbacks positioned along the two edges, as depicted in reference [16], facilitates the assessment of thermal characteristics across the glass interposer structure with distinct TGV pitches.

The heat generated by the heater loopback situated on the active surface of the chip is measured by infrared microscopy (FLIR X6540sc) at the topside of the flip-chip bonded reference thermal chip. This assessment involves the assembly described in **Figure 4.4(b)** situated on a copper block that remains at a consistent temperature of 20 ºC using a thermoelectric cooler (TEC).

The reference thermal chip, featuring heater loopbacks along its edges, is powered through DC connectors at varying power levels (130 mW, 298 mW, and 500 mW). **Figure 4.5** illustrates the temperature recorded at the topside of the chip for glass interposers with TGV pitches of 200 µm, 300 µm and 400 µm for a constant power of 500 mW. Temperature fluctuations correspond to the positioning of the heater

loopbacks, with those at the chip edges generating higher temperatures compared to those at the chip center.

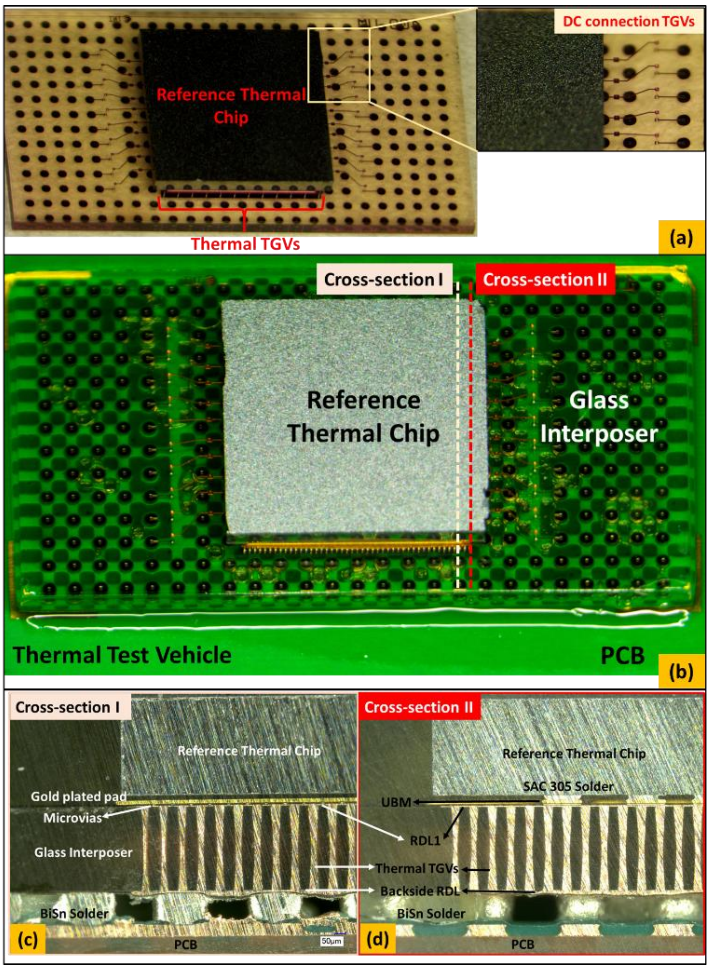


Figure 4.4: (a) Perspective view of the subassembly containing flip-chip bonded reference thermal chip on glass interposer. (b) Top view of the thermal test vehicle showing assembled reference thermal chip and glass interposer (thermal TGV pitch of 100 μm) on PCB, with underfill between the reference thermal chip-glass interposer and glass interposer-PCB interfaces. The cross-sectional lines are specified in the figure. (c) Cross-sectional view of the thermal test vehicle along cross-sectional line 1. (d) Cross-sectional view of the thermal test vehicle along cross-sectional line 2.

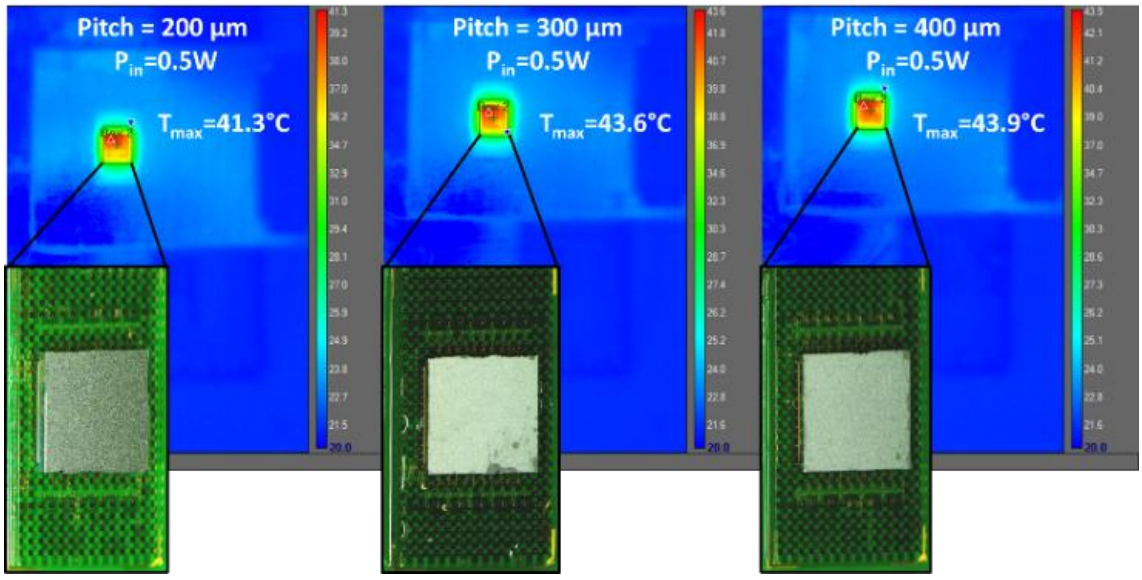


Figure 4.5: Infrared thermal measurement showing surface temperature of the flip-chip bonded reference thermal chip on the glass interposer in thermal test vehicle exhibiting thermal TGV pitches of 200, 300 and 400 µm.

At elevated power levels, this disparity in maximum surface temperature between the corner of the chip's edge and the center of the chip's edge increases (±1ºC), attributed to edge effects as discussed in our previous work [16]. **Figure 4.6 (a & b)** present measurements of the maximum surface temperature registered by a heater loopback situated at the chip's corner, showing a 2.9 ºC increase in temperature as the thermal TGV pitch is changed from 100 µm to 400 µm (at 0.5 W power). This increase in temperature is due to the decrease in the volume of copper in the region occupied by thermal TGVs (**Table 4.1**). The reduction in copper volume results in elevated thermal resistance of the glass interposer. Consequently, the majority of heat disperses toward the top surface of the flip-chip attached reference thermal chip (**Figure 4.6**).

Table 4.1: Table detailing the number of TGVs and the corresponding volume of copper in the glass interposer when the TGV pitch is increased from 100 μm to 400 μm)

Pitch of Thermal TGVs (μm)	Number of TGVs	Volume of Copper in Thermal TGVs under Chip (m^3)
100	2250	4.74×10^{-9}
200	575	1.21×10^{-9}
300	255	0.54×10^{-9}
400	156	0.33×10^{-9}

Moreover, the maximum surface temperature of the heater loopback positioned at the chip's corner is then simulated using Comsol Multiphysics®. The simulation parameters along with simulation results is provided in Appendix A (**Table A.3** and **Figure A.4**). The simulation outcomes closely agree with experimental measurements, as shown in **Figure 4.7**. Despite a substantial 93% reduction in the number of thermal vias (as TGV pitch escalates from 100 μm to 400 μm), there is only a 2.9 °C increase in the surface temperature of the reference thermal chip. This observation is explained through simulations where the effective out-of-plane thermal conductivity of the volume occupied by the thermal TGVs and Bi-Sn solder bumps (with underfill) is varied from 1.2 W/m.K (glass) to 400 W/m.K (copper). The simulation results show that there is a notable practical advantage in utilizing thermal TGVs as compared to glass alone, evidenced by the steep decline in the chip's surface temperature with the incorporation of TGVs in **Figure 4.8** and a 7% reduction in maximum temperature (at 0.5 W power) when a TGV pitch of 400 μm is integrated into the glass interposer (**Figure 4.9**). However, the change in chip's surface temperature becomes minimal (maximum temperature decrease of 1.5 °C) when the TGV pitch of 100 μm is substituted with copper (400 W/m.K). The stagnation in thermal performance observed in TGVs (as shown in **Figure 4.8 (a&b)**) is due to the low thermal conductivity and the larger volume of the PCB, which hinders efficient heat flow.

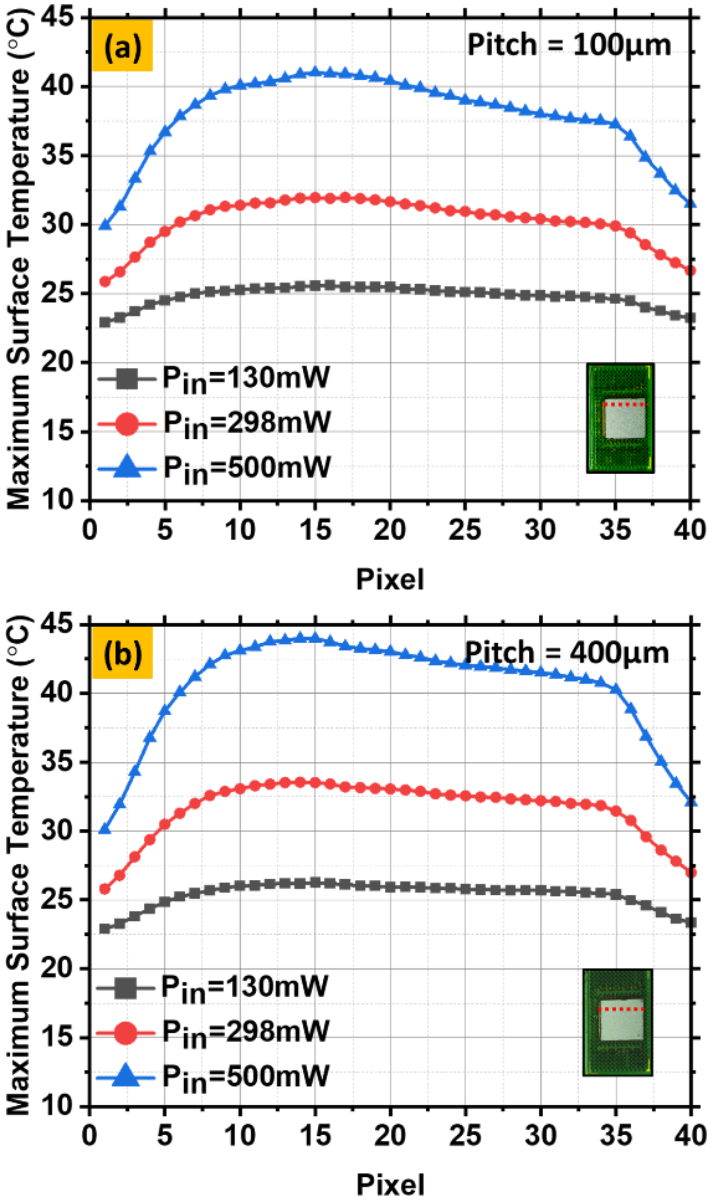


Figure 4.6: Maximum surface temperature measurement across the topside of the flip-chip attached reference thermal chip (along the horizontal axis shown as dashed lines in the inset for (a)100 µm and (b) 400 µm pitch TGVs with increasing input powers of the heater loopback (P_{in}). The heater loopback at the corner of the chip is being operated in both (a) and (b).

This is also seen when the thickness of the glass interposer (with TGVs) is reduced from 460 µm to 110 µm in **Figure 4.8**. Existing studies indicate that variations in the thermal conductivity of the bump layer significantly impacts the overall thermal performance of the interposer, more so than the TGVs [12].

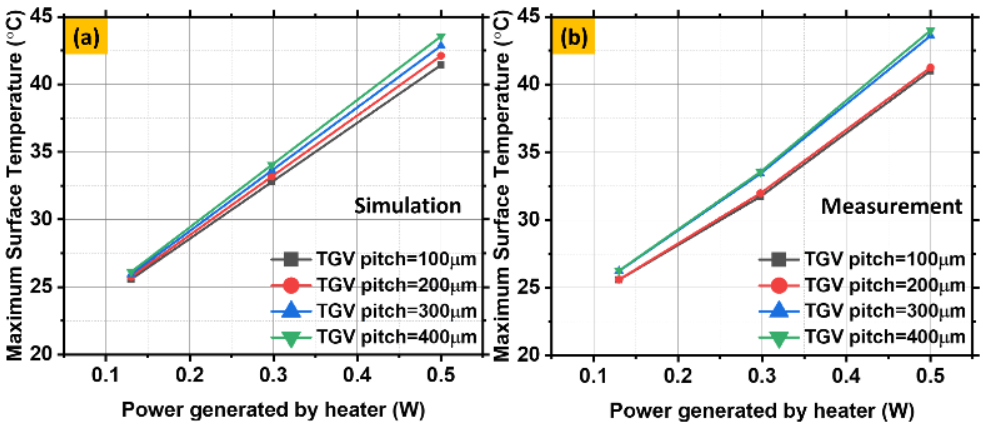


Figure 4.7: Comparison of the (a) simulated and (b) measured maximum surface temperatures of the backside of the flip-chip attached reference chip in the thermal test vehicle using different TGV pitches in the glass interposer with increasing input power of the heater loopback in the chip.

While this holds true for **Figure 4.8(b)**, this trend reverses when the volume of TGVs in the interposer is larger than that of the bumps (as seen in **Figure 4.8(a)**). In our case, the volume of TGVs (height=460 µm) is larger than that of the Bi-Sn solder bumps layer (diameter=250 µm), hence displaying a larger dip in temperature of the chip as compared to the bumps. The chip's surface temperature is also lower in the case of TGVs for the 460 µm thick glass interposer as compared to the 110 µm thick glass interposer due to increased heat spreading. In order to achieve stagnation in thermal performance of TGVs, a 460 µm thick glass interposer requires a slightly higher effective thermal conductivity value for TGVs as compared to the 110 µm thick interposer.

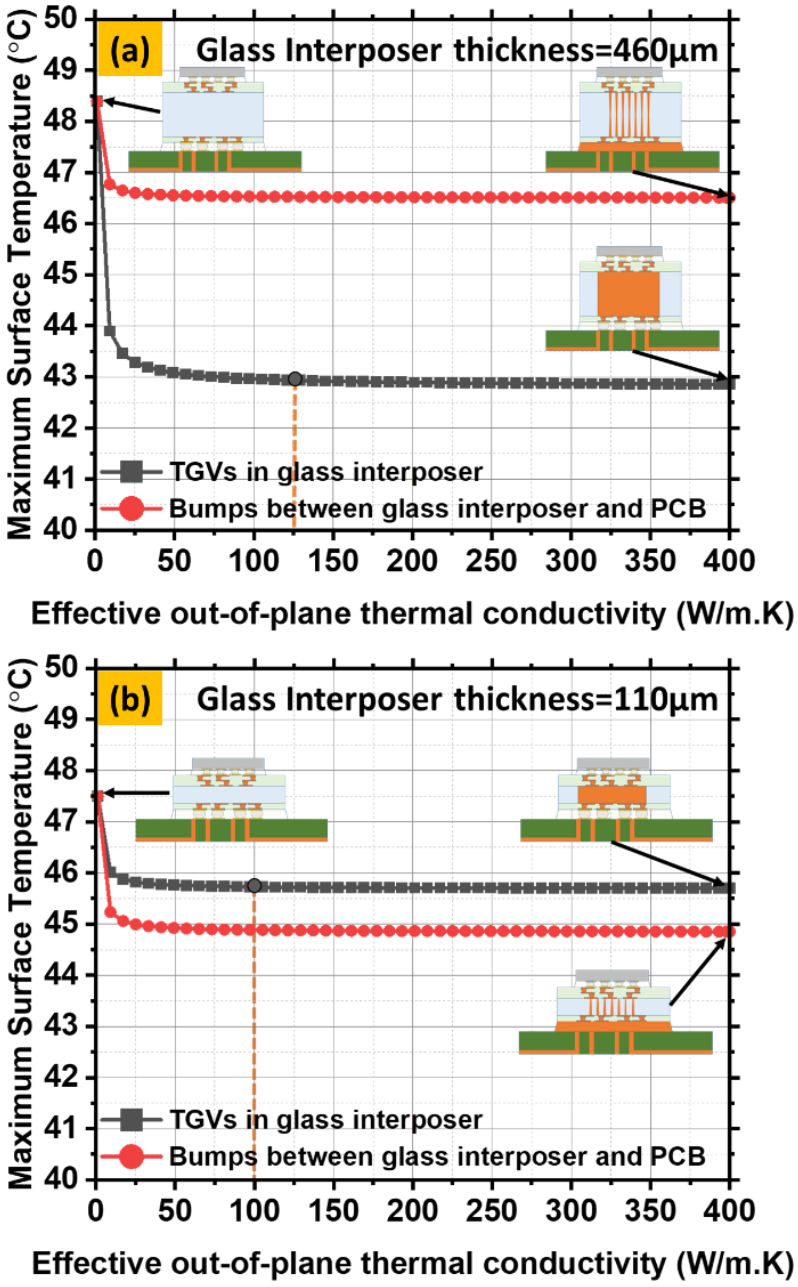


Figure 4.8: Simulated variation in the chip's maximum surface temperature with the change in out-of-plane effective thermal conductivity of TGVs and bumps between glass interposer and PCB (with underfill) when the glass thickness/TGV height is (a) 460 µm and (b) 110 µm respectively. PCB (with underfill).

Thus, the incorporation of TGVs is crucial for establishing an effective thermal pathway, although increasing the TGV density (beyond the 100 µm pitch) and further enhancing the effective out-of-plane thermal conductivity of the glass interposer yields negligible impact on the chip temperature. This pitch relaxation of the thermal TGVs can also reduce the thermal stress in the TGVs [17].

The solution hence relies on improving the thermal conduction through the whole test vehicle stack, by incorporating a heat dissipation mechanism in the PCB. For example, a copper heat sink in PCB offers a high thermal conductivity pathway through the PCB (it offers higher volume than TGVs and Bi-Sn bumps; because the PCB thickness is 1.6 mm). This is evident with an approximately 15 °C decrease in the chip's temperature with the incorporation of a heat sink contacting the TEC surface maintained at 20 ºC beneath the PCB (**Figure 4.9**). Consequently, integrating a heat sink or micro-thermoelectric cooler in the PCB can lead to efficient cooling of the chip within the package.

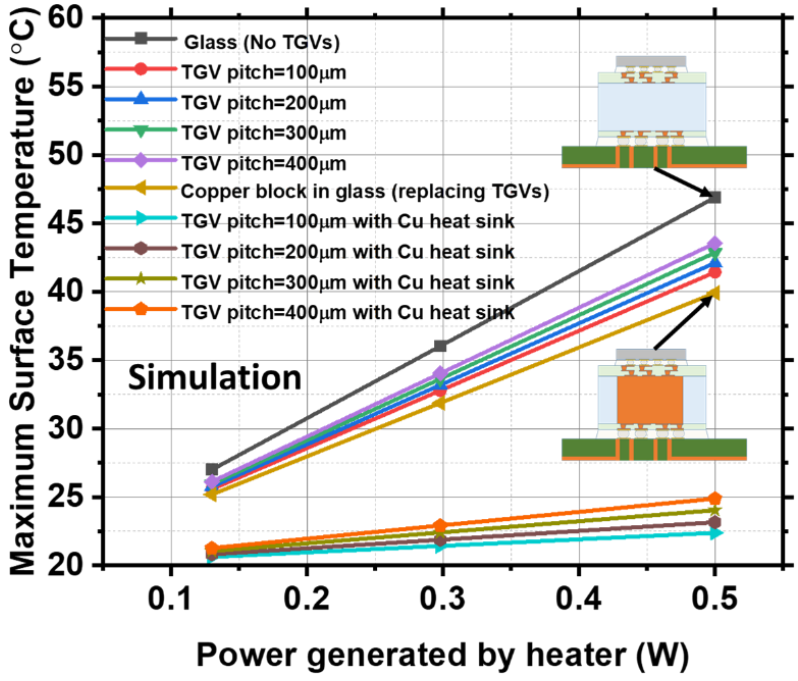


Figure 4.9: Variation of the chip's maximum surface temperature with variation in the TGV pitch (100 µm, 200 µm, 300 µm and 400 µm). The figure also shows a significant decrease in maximum surface temperature with a heat sink embedded in the PCB, where the heat sink is the same size as that of the chip.

4.4 Assembly and characterization of electrical test vehicle

4.4.1 Assembly of Electrical Test Vehicle

The electrical test vehicle is tailored for characterizing a packaged glass interposer and targeting a single-ended 50 Ω characteristic impedance. The assembly consists of four components: glass interposer, Bi-Sn solder bumps, underfill and PCB.

The assembly process starts with the attachment of 250 μm diameter Bi-Sn solder balls onto the BGA pads of the PCB, facilitated by flux and stencil. Subsequently, the glass interposer is carefully positioned over the Bi-Sn solder balls, and alignment adjustment between the interposer and the PCB is conducted under a high-resolution microscope. The attachment of glass interposer to the PCB follows the same temperature reflow profile as the one used in the assembly of the thermal test vehicle. The underfill epoxy (EPOEK 301-2) is applied between the interposer and PCB and cured at room temperature for 36 hours.

Figure 4.10(a) presents a side-view image of the Bi-Sn solder bonding between the interposer and the PCB (without underfill). To validate the attachment further, the entire assembly undergoes a high-resolution X-ray. The X-ray image in **Figure 4.10(b)** depicts precise alignment and attachment of the BGA pads on the glass interposer to the corresponding bond pads of the PCB through the low-melting temperature solder balls (Bi-Sn), with no missing balls and no solder bridging observed in this process. The assembly process of the electrical test vehicle is also summarized in Appendix A (**Figure A.5**).

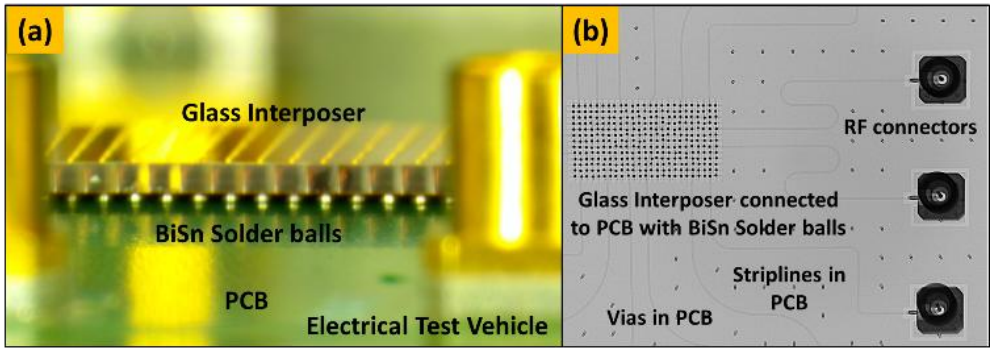


Figure 4.10: (a) Side view of the electrical test vehicle showing the Bi-Sn solder balls bonding the glass interposer on the PCB for RF characterization. This side view is pictured after the Bi-Sn solder reflow and before epoxy underfilling. (b) X-ray imaging analysis of the electrical test vehicle.

A 1.6 mm±10% thick PCB for RF characterization is chosen, comprising a Rogers 4350B core, 4450F prepreg, and FR4 stack-up with plated through-hole vias and 50Ω impedance single-ended striplines. The Rogers 4350B PCB substrate has a dielectric constant (ϵr) of 3.66 (8 to 40 GHz) and a loss tangent of 0.0037 (10 GHz) [18]. The design of the BGA pads on the bottom side of the interposer is replicated on the top side of the PCB. The SMP connectors on the PCB enable electrical characterization of the electrical test vehicle.

4.4.2 Characterization of Transmission Lines on Glass

The interconnects between EIC and PIC is studied through electrical characterization of CPW transmission line with varying lengths (3 mm, 4 mm, 5 mm, and 6 mm) of RDL1 lines on glass, without any backside ground (refer to **Figure 4.12(b)**). These CPW transmission line traces exhibit a width of 100 µm and signal-ground spacing of 18 µm. The characterization includes measurements of CPW transmission lines using a Vector Network Analyzer (VNA) employing 100 µm pitch GSG probes. Additionally, 3D simulations are executed in ANSYS High-Frequency Structure Simulator (HFSS).

For the CPWs, the S parameters are measured using two GSG air-coplanar probes (ACP) from Cascade (currently FormFactor), with a bandwidth up to 67 GHz [19]. In order to de-embed the probes, a calibration is performed using an Impedance Standard Substrate (IIS) substrate.

The one specific to these probes is the FormFactor 101-190D, which allows for calibration using the Short, Open, Load, Through (SOLT) standard [20].

The simulation outcomes closely correspond to the characterization results, except for the case of L=4 mm, where deviations may be attributed to surface irregularities, such as scratches on the sample. Losses in the CPW transmission line structure are primarily attributed to slight deviations in characteristic impedance (approximately 51.5 **Ω**). The variation of characteristic impedance with frequency is depicted in **Figure 4.12** for the CPW transmission line, CPW transmission line with backside ground (CBCPW), and CBCPW transmission line with backside ground and ground fence vias. The incorporation of backside ground and via fence surrounding the CPW transmission line serves to mitigate crosstalk and enhance suppression of higher-order modes, as detailed in [21].

The simulated and measured reflections for the transmission lines consistently remain below -15 dB for all lengths up to 40 GHz, as depicted in **Figure 4.11**. At 20 GHz, the simulated insertion loss for CPW lengths of 3 mm, 4 mm, 5 mm, and 6 mm is -0.242 dB, -0.325 dB, -0.404 dB, and -0.464 dB respectively. Correspondingly, the measured insertion loss is -0.55 dB, -0.812 dB, -0.665 dB, and -0.632 dB respectively. The slope of the S21 plot where the decay is monotonic, when normalized to the frequency and the length of the line, represents the dielectric loss from the glass substrate. For instance, for the 3 mm RDL1 line up to 10 GHz, the dielectric loss is around 0.0435 dB/GHz/cm which is very close to the values obtained with FR4 material [22] (refer to **Figure A.6** in Appendix A). The slightly elevated insertion loss, especially at frequencies greater than 10 GHz observed in the measured samples compared to the simulated scenarios can be attributed to surface irregularities and the roughness of the copper on glass as the RMS surface roughness of copper is measured to be 12.7±0.3 nm [23].

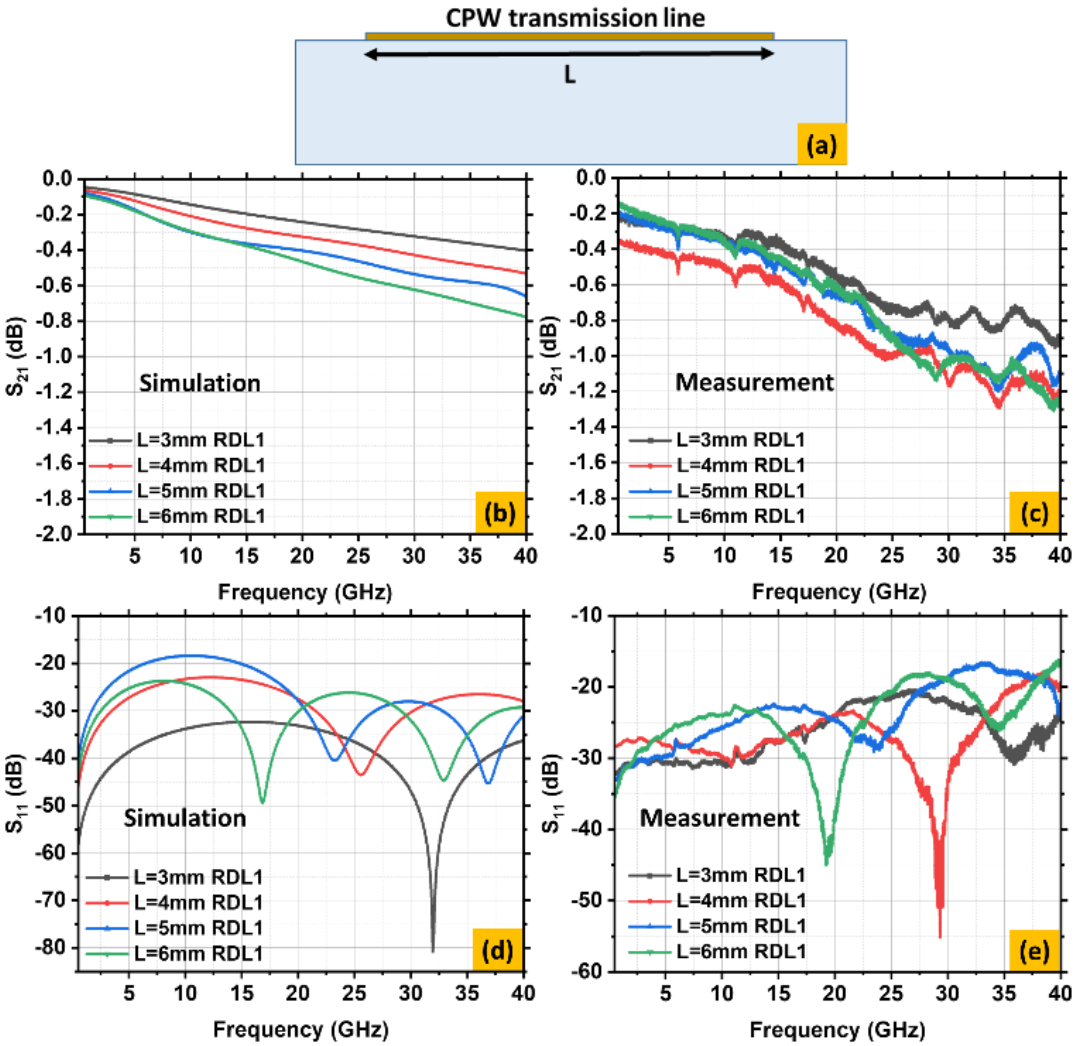


Figure 4.11: (a) Schematic showing CPW transmission line on glass. (b) Simulated and (c) measured insertion loss for the CPW transmission line (RDL1) with varying lengths on glass. (d) Simulated and (e) measured return loss for CPW transmission lines on glass with varying lengths.

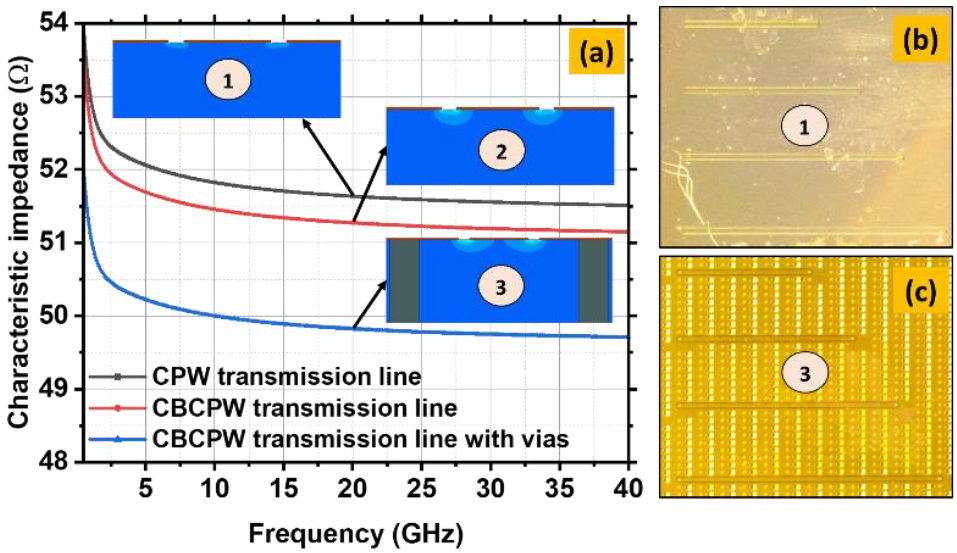


Figure 4.12: (a) Variation of characteristic impedance with frequency for the CPW transmission line on glass, conductor backed CPW transmission line (CBCPW) and CBCPW transmission line with via fence connecting the side grounds to the backside ground on top and bottom of the glass interposer with their respective electric field distributions at 20 GHz. (b) shows the top view of the fabricated CPW transmission lines of different lengths (3 mm, 4 mm, 5 mm and 6 mm) on the glass interposer with no backside ground and TGVs and (c) shows the top view of the fabricated CBCPW transmission line with TGVs in the glass interposer with different lengths.

4.4.3 Characterization of Glass Interposer

In addition to the interconnects on the glass interposer, we need to characterize the signal transmission through different components in the glass interposer. Thus, the glass interposer is characterized (**Figure 4.13** & **Figure 4.14**). A ground via fence encircles the signal transmission lines and signal TGVs with a ground via pitch of 500 µm. The characteristic impedance of the CBCPW structure with vias aligns well with 50 Ω, as evidenced in **Figure 4.12**.

For characterization of the glass interposer, the same setup used for the previous sample is employed. The S parameters for the transmission lines are measured using two GSG |Z| probes from FromFactor with a bandwidth up to 40 GHz [24]. In order to de-embed the probes, a calibration is made using an Impedance Standard Substrate (ISS) substrate. The one specific to these probes is the FormFactor CSR-4, which allows for calibration using the Short, Open, Load, Through (SOLT) standard [25].

Increased insertion losses in this structure as compared to that in **Figure 4.11** is attributed primarily to the geometrical dimensions of the TGVs, microvias and BGA pads. It also represents a collective impact of several factors: the roughness of the conductor surface between the copper-glass and copper-polyimide interface and sidewall roughness of the TGVs [26, 27]. The change in the dielectric constant due to the polyimide layer atop the transmission line [28], and impedance discontinuities at the CPW-TGVs, TGV-microvias, and microvia-BGA pad structures [29-31] is included in the simulation model. Both simulation and measurement results demonstrate good correlation in terms of insertion loss and return loss in the glass interposer structure (**Figure 4.13** and **Figure 4.14**. The simulated 3 dB bandwidth for the glass interposer, where RDL1=3 mm, 4 mm, 5 mm, and 6 mm, is 24.7 GHz, 21.9 GHz, 20.05 GHz, and 24.9 GHz respectively. Meanwhile, the measured 3 dB bandwidth is 25.55 GHz, 21.63 GHz, 19.56 GHz, and 19.79 GHz respectively.

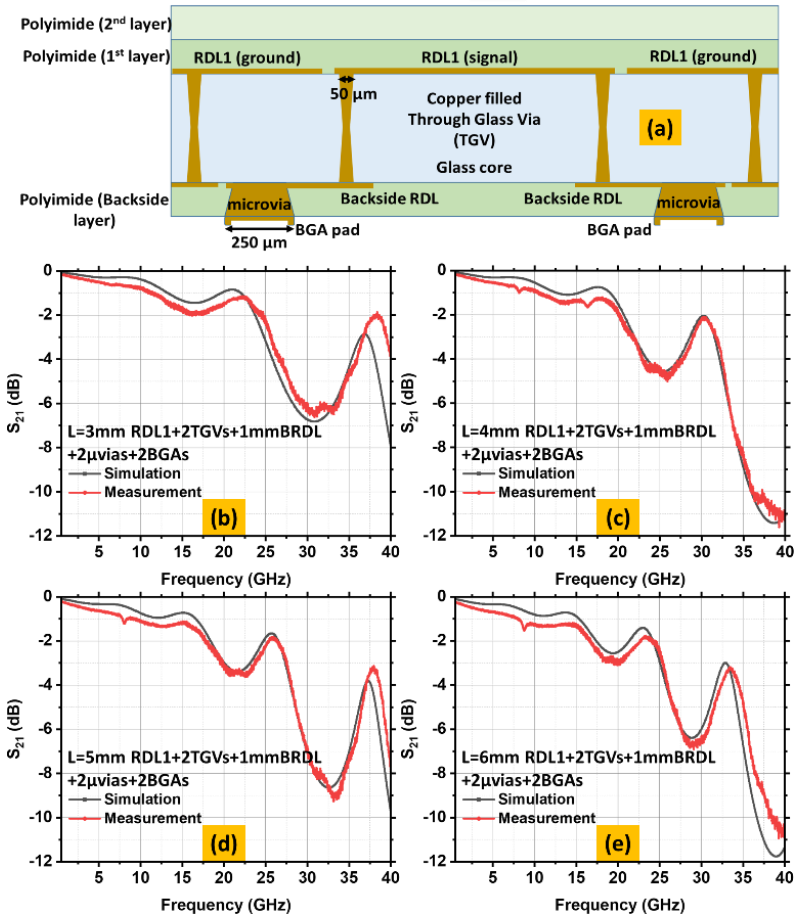


Figure 4.13: (a) Schematic showing glass interposer for electrical characterization. Simulated and measured insertion loss results for the glass interposer with different lengths of the RDL1 line on top (b) 3 mm, (c) 4 mm, (d) 5 mm and (e) 6 mm.

Likewise, the simulated return loss for the glass interposer is -1.964 dB, -0.867 dB, -1.485 dB, and -0.935 dB respectively at 40 GHz. Meanwhile, the measured return loss is -5.16 dB, -0.962 dB, -2.22 dB, and -0.883 dB respectively at 40 GHz. The return loss values and trends exhibit a close match, as demonstrated in **Figure 4.14**.

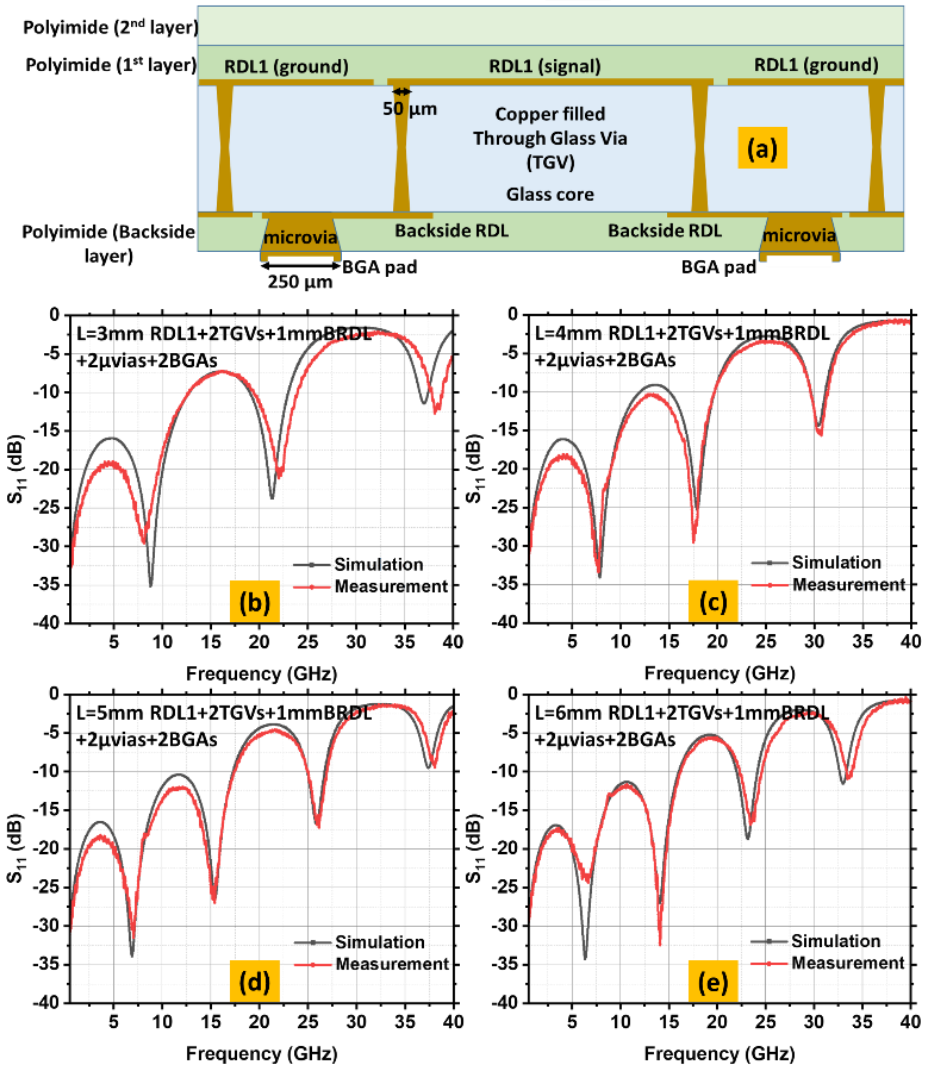


Figure 4.14: Schematic showing glass interposer for electrical characterization. Simulated and measured return loss results for the glass interposer with different lengths of the RDL1 line on top (b) 3 mm, (c) 4 mm, (d) 5 mm and (e) 6 mm.

4.4.4 Characterization of Electrical Test Vehicle

Thirdly, we characterize the packaged glass interposer test vehicle, illustrated in **Figure 4.10(a)**. To measure the S parameters, the VNA needs to be calibrated first in order to transfer the reference plane to the ends of the cables coming out of the VNA. This is done using the electronic calibration kit specific for this VNA (ECAL) [32]. The ECAL module is connected between the ends of the VNA cables at ports 1 and 2, and we run the calibration routine. The results show a flat response up to 67 GHz, indicating good calibration. For the samples mounted on a PCB, the measurement does not need to use RF probes as the PCB is already equipped with miniature SMP connectors [33] with a bandwidth of 40 GHz. The measurements are conducted using RF connectors on the PCB connected to a 2.4 mm 3" cable, which is then linked to the coaxial cable of the VNA. The PCB also has a 2xTHRU [34, 35] structure which is used to de-embed the effect of the launches and PCB transmission lines. The software used for de-embedding is called In Situ De-embedding by AtaiTec. By de-embedding the losses of the PCB from the losses of the electrical test vehicle, we determine the measured insertion loss for the packaged glass interposer with solder and underfill (**Figure 4.15(a)**). The simulation and measurement results follow a similar trends (refer to **Figure 4.15**); however, the degradation in the measurements stems from the uneven spread of the underfill between glass interposer and PCB, which is leading to the resonances in the insertion loss measurements beyond 20 GHz (refer to **Figure A.7** & **Figure A.8** in Appendix A). This is further confirmed by the measured return loss, which is lower as compared to the simulated return loss due to the presence of air pockets in the unevenly spread underfill layer (refer to **Figure A.9** in Appendix A).

As compared to the electrical losses in the glass interposer (**Figure 4.13** & **Figure 4.14**), the additional losses in the packaged glass interposer are attributed to impedance discontinuities induced by the inductive and capacitive parasitic effects of solder and underfill in the package. The EPO-TEK 301-2 underfill utilized between the interposer and PCB in this case features a dielectric constant and loss tangent of 3.8 and 0.012 respectively at 1 kHz. The Bi-Sn solder balls are cylindrical in shape with a diameter of 250 µm in the simulation model, leading to the underfill thickness between the glass interposer and PCB also being 250 µm in the simulation model.

To mitigate the impact of packaging losses on the glass interposer, especially at high frequencies, improvements in the design of TGVs and microvias are essential for impedance matching. Effective design changes would involve optimizing the diameter and pitch of TGVs, microvias, and BGA pads in the Ground-Signal-Ground (GSG) configuration, along with selecting underfill materials with lower dielectric constants and loss tangents [36, 37].

Hence, the next step is to optimize the electrical design for packaging. The design optimization is conducted for the loopback in the glass interposer, as the simulation and measurement results shown in **Figure 4.15(a)** exhibit very high losses. Several changes are implemented: the TGV, microvia, and BGA diameter are adjusted to 70 µm, 100 µm, and 100 µm respectively. Additionally, the Bi-Sn solder ball diameter is reduced to 100 µm, and the grounding TGV/microvia/BGA pitch is modified to 250 µm. Consequently, the reduction in the Bi-Sn solder ball diameter results in a decrease in the underfill thickness to 100 µm. These alterations aim to minimize impedance discontinuity along the signal path, leading to a significant improvement in the electrical performance of the glass interposer, as demonstrated in **Figure 4.16**.

The insertion loss of the optimized design is notably reduced by approximately 11.83 dB (at 40 GHz) compared to the current design featuring the 3 mm long RDL1 line, along with TGVs, microvias, BGA pads, BRDL, solder, and underfill (as depicted in **Figure 4.16(a)**). Furthermore, the return loss for the optimized structure remains below -10 dB up to 40 GHz (**Figure 4.16(b)**). It is important to note that these improvements are achieved solely through geometrical parameter optimization, while the material properties remain unchanged.

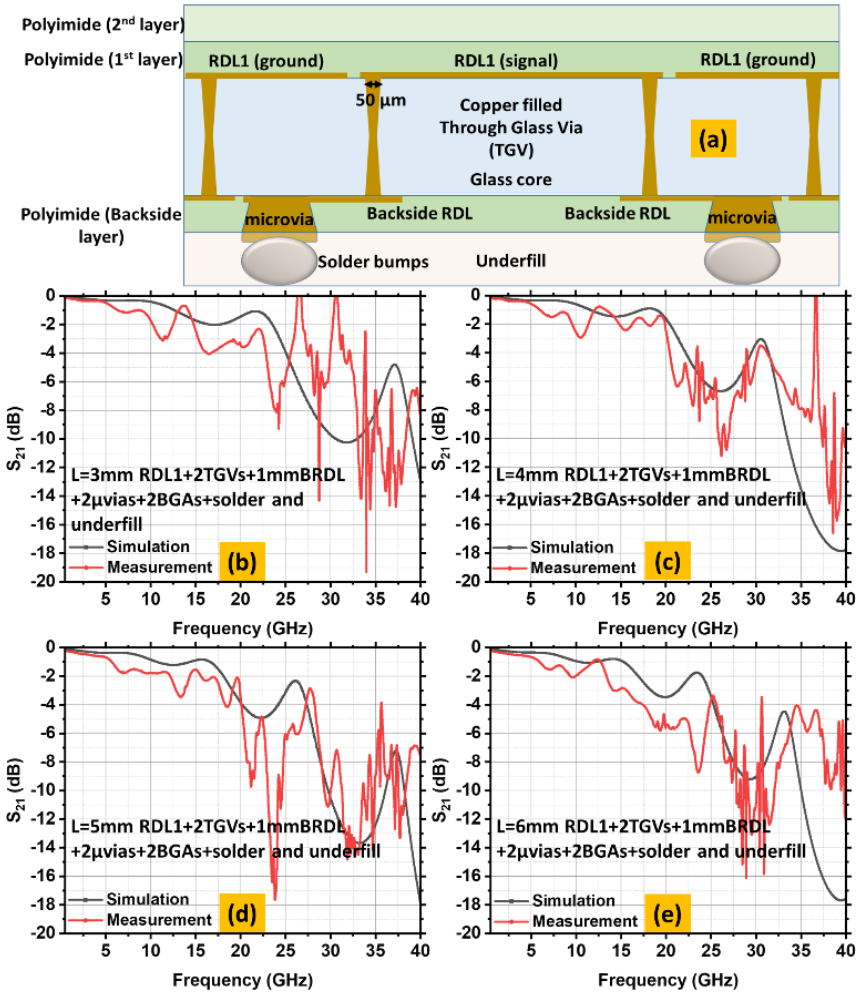


Figure 4.15: Schematic showing the electrical test vehicle for characterization (with de-embedded PCB losses). Simulated and measured insertion loss results for the de-embedded test vehicle with different lengths of the RDL1 line (b) 3 mm, (c) 4 mm, (d) 5 mm and (e) 6 mm.

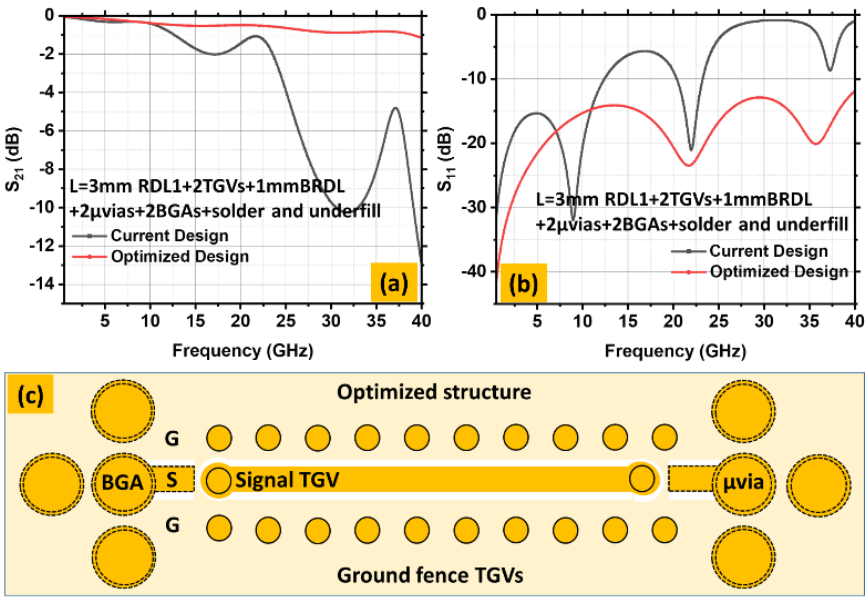


Figure 4.16: Simulated insertion loss and return loss for the electrical test vehicle in (a) current design and (b) optimized design. (c) shows the optimized structure where the pitch of the ground fence TGV, microvias, BGA pads and solder are reduced to 250 µm, the microvia, BGA pad and solder diameter are reduced to 100 µm and the TGV diameter is increased to 70 µm to reduce impedance discontinuity along the signal path.

4.5 Conclusion

This chapter examines the heat dissipation and electrical performance in glass interposers, a vital technology for high-density electronic-photonic packaging. We investigated the effect of varying TGV pitch on thermal performance of glass interposers and identified its impact on overall functionality. Furthermore, we investigated the electrical losses related to various interconnects in 2.5D glass interposer-based packages.

The heat dissipation in glass interposers is studied by varying the thermal TGV pitch from 100 µm to 400 µm in the thermal test vehicle. Thermal characterization with increasing TGV pitch from 100 µm to 400 µm reveals an increase of 2.9ºC in the chip's maximum surface temperature. The FEM simulation indicates that the incorporation of TGVs in glass interposer leads to an improvement in its thermal performance but the variation of TGV pitch lower than 100 µm has minimal impact on the heat dissipation of the reference thermal chip packaged on the glass interposer.

This is because of the presence of the highly thermal resistant PCB, which occupies a large volume impeding heat conduction through it. Thus, the integration of heat sink or micro-TEC in the PCB can reduce the thermal resistance incurred through the PCB.

Furthermore, electrical characterization of the packaged glass interposer reveals significant losses induced by impedance discontinuities along the signal path, including TGVs, microvias, BGA pads, solder, and underfill. Optimizing the design of TGVs, microvias and BGA pads can result in lower electrical loss in the glass interposer. By minimizing impedance discontinuity, the signal transition from the narrower line/spacing of the glass interposer to the wider line/spacing of the PCB achieves an impressive reduction in insertion loss, bringing it closer to the performance of transmission lines on glass.

The understanding of thermal management and signal transmission challenges related to electronic-photonic packaging using glass interposers can help in establishment of practical recommendations to improve performance and reliability in the future.

4.6 References

[1] J. H. Lau, "Co-Packaged Optics—Heterogeneous Integration of Photonic Integrated Circuits and Electronic Integrated Circuits," Journal of Electronic Packaging, vol. 147, no. 1, 2024, doi: 10.1115/1.4065667.

[2] M. Tan et al., "Co-packaged optics (CPO): status, challenges, and solutions," Frontiers of Optoelectronics, vol. 16, no. 1, p. 1, 2023/03/20 2023, doi: 10.1007/s12200-022-00055-y.

[3] A. V. Krishnamoorthy et al., "From Chip to Cloud: Optical Interconnects in Engineered Systems," Journal of Lightwave Technology, vol. 35, no. 15, pp. 3103-3115, 2017, doi: 10.1109/JLT.2016.2642822.

[4] N. C. Abrams et al., "Silicon Photonic 2.5D Multi-Chip Module Transceiver for High-Performance Data Centers," Journal of Lightwave Technology, vol. 38, no. 13, pp. 3346-3357, 2020, doi: 10.1109/JLT.2020.2967235.

[5] L. Brusberg et al., "Glass Platform for Co-Packaged Optics," IEEE Journal of Selected Topics in Quantum Electronics, vol. 29, no. 3: Photon. Elec. Co-Inte. and Adv. Trans. Print., pp. 1-10, 2023, doi: 10.1109/JSTQE.2023.3247245.

[6] C. Minkenberg, R. Krishnaswamy, A. Zilkie, and D. Nelson, "Co-packaged datacenter optics: Opportunities and challenges," IET Optoelectronics, vol. 15, no. 2, pp. 77-91, 2021, doi: https://doi.org/10.1049/ote2.12020.

[7] B. Sawyer, B. C. Chou, S. Gandhi, J. Mateosky, V. Sundaram, and R. Tummala, "Modeling, design, and demonstration of 2.5D glass interposers for 16-channel 28 Gbps signaling applications," in 2015 IEEE 65th Electronic Components and Technology Conference (ECTC), 26-29 May 2015 2015, pp. 2188-2192, doi: 10.1109/ECTC.2015.7159906.

[8] K. Kröhnert et al., "High Aspect Ratio Through-Glass Vias as Heat Conductive Element," in 2022 IMAPS Nordic Conference on Microelectronics Packaging (NordPac), 12-14 June 2022 2022, pp. 1-6.

[9] P. Gupta et al., "Impact of Through Glass Vias Filling on the Performance of Passive Thermal Cooling in Photonic Packages," in 2022 IEEE 9th Electronics System-Integration Technology Conference (ESTC), 13-16 Sept. 2022 2022, pp. 391-397, doi: 10.1109/ESTC55720.2022.9939531.

[10] P. Gupta et al., "Substrate integrated micro-thermoelectric coolers in glass substrate for next-generation photonic packages," Journal of Optical Microsystems, vol. 4, no. 1, p. 011006, 2024. [Online]. Available: https://doi.org/10.1117/1.JOM.4.1.011006.

[11] B. Chou et al., "Co-Design and Demonstration of a Fully Integrated Optical Transceiver Package Featuring Optical, Electrical, and Thermal Interconnects in Glass Substrate," International Symposium on Microelectronics, vol. 2016, no. 1, pp. 000007-000012, 2016, doi: 10.4071/isom-2016-TP12.

[12] S. Cho, V. Sundaram, R. R. Tummala, and Y. K. Joshi, "Impact of Copper Through-Package Vias on Thermal Performance of Glass Interposers," IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 5, no. 8, pp. 1075-1084, 2015, doi: 10.1109/TCPMT.2015.2450731.

[13] L. Ranno et al., "Integrated Photonics Packaging: Challenges and Opportunities," ACS Photonics, vol. 9, no. 11, pp. 3467-3485, 2022/11/16 2022, doi: 10.1021/acsphotonics.2c00891.

[14] S. Cho and Y. K. Joshi, "Thermal Performance Enhancement of Glass Interposer," in ASME 2015 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems collocated with the ASME 2015 13th International Conference on Nanochannels, Microchannels, and Minichannels, 2015, vol. Volume 3: Advanced Fabrication and Manufacturing; Emerging Technology Frontiers; Energy, Health and Water- Applications of Nano-, Micro- and Mini-Scale Devices; MEMS and NEMS; Technology Update Talks; Thermal Management Using Micro Channels, Jets, Sprays, V003T04A021, doi: 10.1115/ipack2015-48563. [Online]. Available: https://doi.org/10.1115/IPACK2015-48563

[15] B. Sawyer et al., "Design and Demonstration of 2.5D Glass Interposers as a Superior Alternative to Silicon Interposers for 28 Gbps Signal Transmission," in 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), 31 May-3 June 2016 2016, pp. 972-977, doi: 10.1109/ECTC.2016.321.

[16] P. Gupta, "Reference Thermal Chips for 2D and 3D Co-packaging Process Development," In 2023 IEEE 73rd Electronic Components and Technology Conference (ECTC), pp. 2160-2165. IEEE, 2023.

[17] A. Benali, M. Bouya, M. Faqir, A. E. Amrani, M. Ghogho, and A. Benabdellah, "Through glass via thermomechanical analysis: Geometrical parameters effect on

thermal stress," in 2013 8th IEEE Design and Test Symposium, 16-18 Dec. 2013 2013, pp. 1-5, doi: 10.1109/IDT.2013.6727093.

[18] Rogers Corporation. "RO4000 Laminates RO4003C and RO4350B - Data Sheet," R04350B datasheet, 2022. [Online]. Available: https://www.rogerscorp.com/advanced-electronics-solutions/ro4000-series-laminates/ro4350b-laminate.

[19] FormFactor Inc. "ACP Probe-Coaxial," 2024. [Online]. Available: https://www.formfactor.com/product/probes/acp/acp-probe-coaxial/.

[20] FormFactor Inc. "Impedance Standard Substrates," 114-456 GSG datasheet, 2024 [Online]. Available: https://www.formfactor.com/product/probes/calibration-tools-probes/impedance-standard-substrates/.

[21] A. Sain and K. L. Melde, "Impact of Ground via Placement in Grounded Coplanar Waveguide Interconnects," IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 6, no. 1, pp. 136-144, 2016, doi: 10.1109/TCPMT.2015.2507121.

[22] L. Annie and L. Eric, "Base material consideration for high speed printed circuit boards," in 2009 4th International Microsystems, Packaging, Assembly and Circuits Technology Conference, 21-23 Oct. 2009 2009, pp. 478-480, doi: 10.1109/IMPACT.2009.5382223.

[23] H. Cai et al., "Design, fabrication, and radio frequency property evaluation of a through-glass-via interposer for 2.5D radio frequency integration," Journal of Micromechanics and Microengineering, vol. 29, no. 7, p. 075002, 2019/05/22 2019, doi: 10.1088/1361-6439/ab1d30.

[24] FormFactor Inc. "|Z| Probe – Coaxial," |Z| Probe 67 GHz datasheet, 2020 [Online]. Available:https://www.formfactor.com/product/probes/z-probe/z-probe-coaxial/#downloads.

[25] FormFactor Inc. "CSR Cal Substrates," CSR-4 datasheet, 2018. [Online]. Available: https://www.formfactor.com/product/probes/calibration-tools-probes/csr-cal-substrates/.

[26] Z. Fang et al., "Analysis and Optimization of Sidewall Roughness on Microwave Performance of Through-Glass Vias in 3-D Integrated Circuits," IEEE Transactions on Microwave Theory and Techniques, vol. 72, no. 1, pp. 54-63, 2024, doi: 10.1109/TMTT.2023.3280945.

[27] A. O. Watanabe, K. Kanno, H. Ito, R. R. Tummala, and M. Swaminathan, "High-density low-loss millimeter-wave package interconnects with the impact of dielectric-material surface roughness," Applied Physics Letters, vol. 119, no. 13, 2021, doi: 10.1063/5.0055637.

[28] Y. Lamy et al., "mmW characterization of wafer level passivation for 3D silicon interposer," in 2013 IEEE 63rd Electronic Components and Technology Conference, 28-31 May 2013 2013, pp. 1887-1891, doi: 10.1109/ECTC.2013.6575835.

[29] M. Woehrmann et al., "Glass based interposers for RF applications up to 100GHz," in 2016 6th Electronic System-Integration Technology Conference (ESTC), 13-15 Sept. 2016 2016, pp. 1-7, doi: 10.1109/ESTC.2016.7764695.

[30] J. Kim et al., "Electrical characteristics analysis and comparison between through silicon via(TSV) and through glass via(TGV)," in 2015 IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS), 14-16 Dec. 2015 2015, pp. 93-96, doi: 10.1109/EDAPS.2015.7383676.

[31] A. O. Watanabe, H. Ito, R. P. Markondeya, R. R. Tummala, and M. Swaminathan, "Low-Loss Impedance-Matched Sub-25-μm Vias in 3-D Millimeter-Wave Packages," IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 10, no. 5, pp. 870-877, 2020, doi: 10.1109/TCPMT.2020.2982294.

[32] Keysight. “N4694A Electronic Calibration Module (ECal), 10 MHz to 67 GHz, 1.85 mm, 2-port [Discontinued],”. [Online]. Available: https://www.keysight.com/nl/en/product/N4694A/electronic-calibration-module-ecal-10-mhz-to-67-ghz-185-mm-2port.html.

[33] Rosenberger. “Mini-SMP connector 18S143-40ML5,” 18S143-40ML5 datasheet, 2024. [Online]. Available: https://products.rosenberger.com/_ocassets/db/18S143-40ML5.pdf.

[34] J. Y. Ye, J. Fan, X. Cao, Q. M. Cai, Y. Zhu, and Y. Zhu, "A 2x-Thru Standard De-embedding Method of Surface Components in High-Speed PCBs," in 2022 IEEE USNC-URSI Radio Science Meeting (Joint with AP-S Symposium), 10-15 July 2022 2022, pp. 58-59, doi: 10.23919/USNC-URSI52669.2022.9887402.

[35] M. Tsiklauri, "P370:Electrical Characterization of Printed Circuit Board and Related Interconnects at Frequencies up to 50 GHz," in 2017 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI), 7-11 Aug. 2017 2017, pp. 1-15, doi: 10.1109/ISEMC.2017.8078138.

[36] H. Xia et al., "Effects of underfill on wideband flip-chip packaging for 5G millimeter-wave applications," IEICE Electronics Express, vol. advpub, 2023, Art no. 20.20230094, doi: 10.1587/elex.20.20230094.

[37] A. Chandrasekhar, S. Brebels, S. Stoukatch, E. Beyne, W. De Raedt, and B. Nauwelaers, "The influence of packaging materials on RF performance," Microelectronics Reliability, vol. 43, no. 3, pp. 351-357, 2003/03/01/ 2003, doi: https://doi.org/10.1016/S0026-2714(02)00342-6.

Chapter 5: Substrate Integrated Micro-Thermoelectric Coolers in Glass Substrate for Next-Generation Photonic Packages

This chapter is based on the following publication- **Parnika Gupta**, Amit Tanwar, Xiuyun He, Kamil Gradkowski, Kafil M. Razeeb, Padraic E. Morrissey, and Peter O'Brien. "Substrate integrated micro-thermoelectric coolers in glass substrate for next-generation photonic packages." *Journal of Optical Microsystems* 4, no. 1 (2024): 011006.

Credit authorship contribution statement

Parnika Gupta: Writing-original draft, Conceptualization, Visualization, Methodology, Investigation, Formal analysis. **Amit Tanwar and Kamil M. Razeeb:** Investigation, validation. **Xiuyun He:** Image generation, **Kamil Gradkowski:** Writing – review & editing, Supervision, **Padraic E. Morrissey and Peter O'Brien:** Writing – review & editing, Supervision, Conceptualization, Project administration, Funding acquisition.

5.1 Introduction

As we progress towards high-bandwidth communication networks, the succeeding generation of photonic packages demands enhanced levels of integration between electronics and photonics within a System-in-Package (SiP) architecture [1, 2]. With closely packed electronic and photonic elements, there arises a thermal interplay between the electronic and photonic chips, potentially impacting temperature-sensitive optical functionalities within the photonic chip. To counteract this thermal interaction and uphold mechanical stability, glass substrates (low coefficient of thermal expansion (CTE) 3.25 x 10^{-6} K^{-1}) have emerged as a viable solution due to their limited lateral heat propagation [3]. Glass substrates also exhibit favorable electrical and optical routing characteristics, featuring a low loss tangent and the suitability for optical waveguide/micro-optical integration [4]. High-density electrical connections can be created within glass through the use of redistribution layers (RDLs), Microvias, and Through Glass Vias (TGVs) [3, 5]. This dense electrical routing facilitates the close integration of electronic and photonic chips, leading to

minimal electrical transmission loss between these components [6]. However, this also introduces another challenge in thermal management – the heat generated by electronic chips must be dissipated within the glass package. Through Glass Vias filled with copper serve as a passive cooling solution to manage the heat generated by electronic chips [7-9].

For photonic chips, specific optical elements like ring resonator filters, modulators, and semiconductor optical amplifiers are sensitive to changes in temperature, as they operate at specific wavelengths. As a result, the temperature sensitive components on the photonic chips necessitate thermal control capabilities to counteract the impact of temperature fluctuations in the operating environment, thereby maintaining optimal performance [10]. One solution for thermal stabilization involves the integration of centimeter-scale thermoelectric coolers (Macro-TEC) at the bottom of the package, as illustrated in **Figure 5.1(a)**. Nonetheless, variations in temperature by the macro-TEC can cause different package components and materials – such as electronic chips, photonic chips, solder bumps, underfill, and epoxies – to deform in distinct ways, potentially affecting the optical coupling between the photonic chip and the fiber [1, 10]. An alternate approach involves achieving precise thermal control of photonic components through the use of Free-standing Micro-Thermoelectric Coolers (micro-TEC). These micro-TECs are compact, lightweight, compatible with CMOS fabrication, and result in lower material consumption. They allow for direct on-chip cooling when the chip is bonded face-up on a substrate [2, 11]. However, this requires additional packaging steps, including the bonding of the micro-TEC module onto the chip and attaching a heat sink to the hot side junction of the micro-TEC.

When the electronic/photonic chips are flip-chip bonded (face-down) onto the glass substrate, integrating a micro-TEC on the chip involves adhering the micro-TEC device to the backside of the photonic/electronic chips. This introduces parasitic thermal resistance due to the chip's thickness, as depicted in **Figure 5.1(b)**. Recent discussions by P. Zhang *et al.* have delved into the optimization of a micro-TEC embedded within a cavity etched in the thermal interface material (TIM) layer atop a 3D integrated architecture and this setup connects to a heat spreader layer [12]. Nevertheless, challenges emerge when photonic and electronic chips within a 2.5D configuration possess different thicknesses, leading to varying thicknesses of the TIM layer connected to the heat spreader [13]. This necessitates the redesign and fabrication

of the micro-TEC with distinct thicknesses for effective thermal control of the photonic and electronic chips. One strategy to mitigate this challenge involves embedding the micro-TEC within a cavity in the substrate. However, this approach introduces additional complexities like die shifting, costs related to precise trench fabrication, precision in die embedding, and integration of the heat sink mechanism connected to the embedded micro-TEC's hot end.

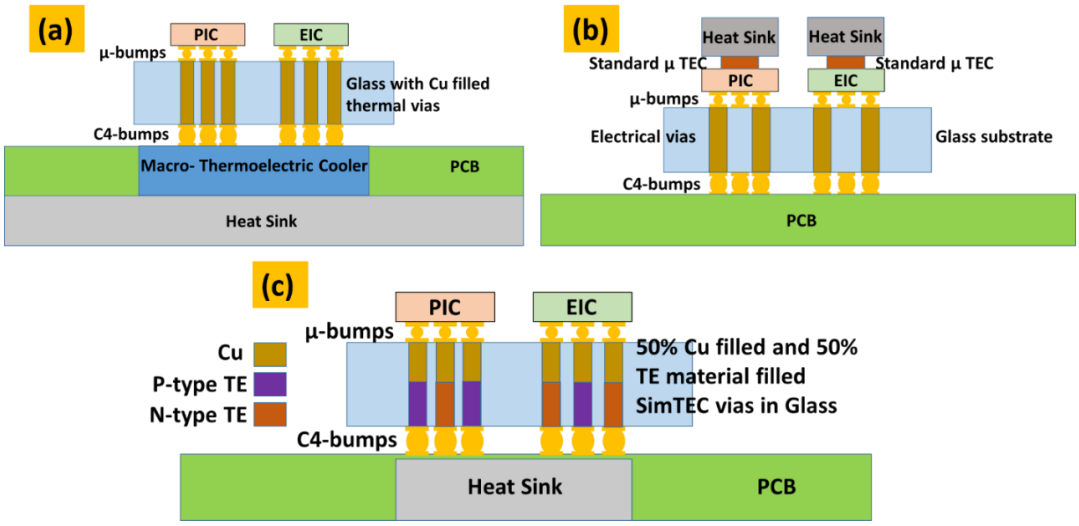


Figure 5.1 Schematic showing different approaches of thermoelectric cooler integration in a photonic package where Photonic Integrated Chip (PIC) and Electronic Integrated Chip (EIC) are co-packaged together on a Glass substrate where the implementation of (a) Macro-Thermoelectric Cooler (Macro-TEC) ; (b) Micro-TEC (µ-TEC) and (c) Substrate integrated micro-TEC (SimTEC) in photonic packages is highlighted.

Thereby, in this chapter, we propose a novel strategy that involves employing Through Glass Vias (TGVs) as Thermoelectric Cooler (TEC) pillars. In this approach, the vias are filled with copper and thermoelectric materials through electroplating. This innovative method is referred to as Substrate integrated micro-TEC (SimTEC), highlighted in **Figure 5.1(c)**. SimTEC facilitates targeted and precise thermal management of photonic chips, enhancing thermal connectivity with the surface of the photonic chip (which is bonded face-down onto the substrate) and maintaining a compact form factor for the glass package. Further reduction in thermal resistance at the chip surface and the cold-side TEC interface can be achieved by transitioning from microbump and underfill based bonding to Copper-Copper (Cu-Cu) hybrid bonding. In this case, the heat sink can be integrated with the Printed Circuit Board (PCB), similar to the architecture of macro-TECs as shown in **Figure 5.2**. The thermal design

is intricately linked with the substrate design, wherein the glass substrate can be divided into domains for signal transmission, power transmission, passive and active thermal management. Notably, this approach eliminates the additional fabrication cost associated with micro-TECs, offering designers greater flexibility in customizing substrate thermal design to accommodate variations in areas corresponding to chip regions requiring thermal adjustment.

As described by Mahajan et al. [14], the maximum temperature limits for the photonic and electronic chips within a photonic engine are delineated distinctly along with changing ambient temperature of the package. This distinction renders the SimTEC approach a viable method for precisely adjusting the chip temperature, complementing broader system-level thermal management techniques. A parallel scenario arises in the neuromorphic photonic accelerator module [15], where specific components, including the core photonic processor, DFB lasers, and SOAs, are susceptible to thermal fluctuations. This susceptibility presents an opportunity for the SimTEC device to provide a temperature stabilization solution seamlessly integrated into the module. Furthermore, SimTEC can be applied to achieve thermal stabilization in quantum photonic devices with exceptional accuracy during prototype development [16]. While this integrated architecture enables localized temperature control, the presence of a glass substrate around segmented vias increases the thermal response time due to the heightened thermal mass of the device [17].

Earlier efforts by researchers have demonstrated the application of polymer-embedded micro-TECs, showing a net cooling temperature (9.6 K), serving as a chemically-stable packaging technique for thermoelectric pillars [17]. However, the compatibility of these embedded micro-TECs with solder reflow processes has not been explored. Liu *et al.* have also examined the fabrication and performance analysis of a Thermoelectric Generator (TEG) based on through glass pillars for the recovery of low-grade waste heat. This setup generated a maximum output voltage of 40.89 mV under a temperature difference of 138 K [18]. The advantages attributed to thermoelectric legs integrated into glass pillars, including increased leg height of the thermoelectric pillars, operation resistant to oxidation and moisture, established manufacturing processes for creating through holes, and cost-effectiveness of glass compared to photoresist, have been elaborated upon [18, 19]. These advantages also

extend to the SimTEC approach, where the focus is on achieving controlled temperature operations of the TEC.

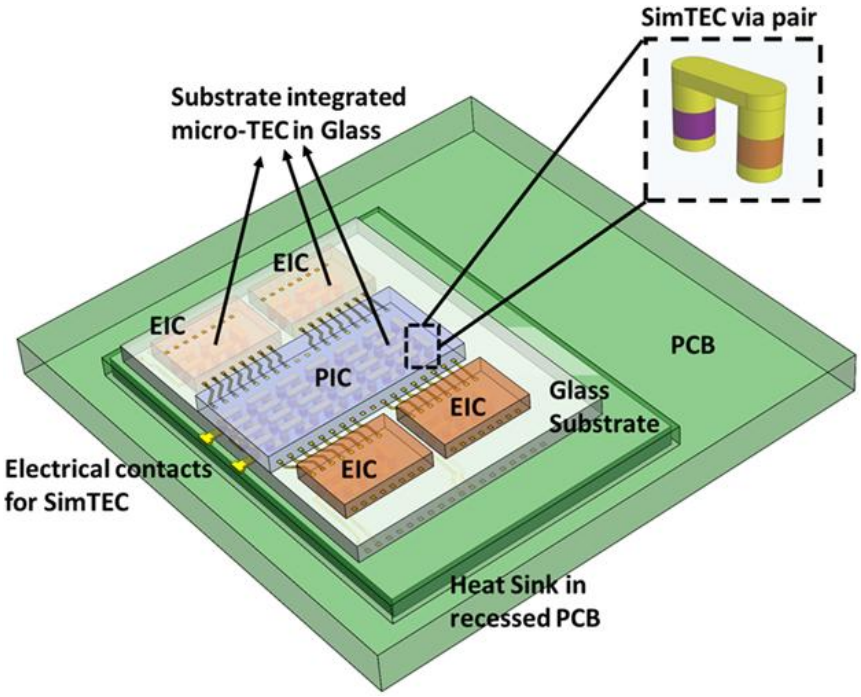


Figure 5.2: Diagram showing the SimTEC architecture in Glass substrate with the SimTEC vias operating in the central region of the electronic chips (EIC) and photonic chip (PIC) with the chip's peripheral I/Os dedicated for electrical connection in the photonic package.

The performance of a thermoelectric module is based on the efficiency of the thermoelectric materials and the design parameters for the TEC. The performance of the thermoelectric materials is measured by $zT = S^2\sigma\kappa^{-1}$, where S is the Seebeck coefficient, σ is the electrical conductivity, κ is the thermal conductivity and T is the absolute temperature [11, 19]. As discussed in the literature, the electroplating technique is considered for the deposition of thermoelectric materials in unfilled TGVs [2, 11, 19]. There are various techniques for the formation of TGVs that can be considered for the fabrication of SimTEC such as mechanical drilling, wet drilling, laser drilling, sandblasting, inductively coupled plasma (ICP) etching, discharge methods, glass reflow methods, etc. [20]. The formation of TGVs is then followed by electrodeposition of the copper and thermoelectric materials in the TGVs and the formation of copper interconnects on the top and bottom of the glass substrate [18]. The performance of the TEC module is also impacted by the design parameters of the thermoelectric legs or the TGV parameters in the case of SimTEC.

In this work, we have theoretically investigated the impact of variation of via parameters such as via diameter, via height, via pitch, fill-factor and order of deposition of copper and thermoelectric materials in the via on the cooling performance of SimTEC. This cooling performance is simulated as the surface temperature difference between the hot side interconnect (where heat is dissipated from the bottom of the glass substrate) and the cold side interconnect (where heat is absorbed from the top of the glass substrate) with the application of a current. This cooling mode can also be converted to the heating mode when we reverse the polarity of the applied current, thus enabling localized thermal tuning of the photonic chips. We have simulated a thermoelectric via pair using Finite Element Method analysis in COMSOL Multiphysics® software. The thermoelectric via pair in SimTEC is also compared with the free-standing thermoelectric leg pair with the same parameter variations to highlight the impact of the glass substrate on the thermoelectric performance. A further optimization analysis for the diameter, height and pitch of the TGVs has been done to see the cooling performance of the SimTEC and free-standing thermoelectric leg pair. **Table 5.1** tabulates the features of a macro-TEC, micro-TEC and SimTEC for briefly differentiating the feasibility of the three thermal tuning approaches in photonic packaging [21].

Table 5.1: Table highlighting the features of a centimetre scale TEC (Macro-TEC), Free-standing micro-TEC device and Substrate integrated micro-TEC (SimTEC).

	Macro-TEC	**Micro-TEC**	**SimTEC**
Temperature Cooled	60-80 K	10-20 K	Approximately 10 K
Size	Centimeter	Micrometer	Micrometer
Fabrication Complexity	Low	High	High
Device Stability	High	Low	High
Flip-Chip Compatibility	Low	High	High
Thermal resistance between chip surface and TEC cold-side surface	High	Moderate	Low

5.2 Simulation Approach

A thermoelectric module consists of p-type and n-type leg pairs which are arranged alternatively, such that they are electrically connected in a series configuration and thermally connected in a parallel configuration [22]. SimTEC consists of a via pair in glass, where one via is filled with copper and p-type thermoelectric material and the other via is filled with copper and n-type thermoelectric material. A DC current is applied to the copper interconnect connected to the n-type via side and the interconnect on the p-type via side is connected to ground. This current flow gives rise to a temperature difference between the top and bottom copper interconnects of the glass with vias because of the Peltier effect [11].

Considering the isotropic properties of the materials, the continuity equation for the electric current density in a thermoelectric module is given by [23]:

$$\nabla \cdot J = 0 \tag{5.1}$$

Where, J is the electric current density.

This current density in the TEC is dependent on the Ohm's law and the Seebeck effect, which is given by [23, 24]:

$$J = -\sigma(\nabla V + S\nabla T) \tag{5.2}$$

$$E = \frac{J}{\sigma} + S\nabla T \tag{5.3}$$

Similarly, the heat flux generated in the TEC can be divided into the effect of the Joule heating and the Seebeck effect, which is translated as [11, 24]:

$$q = STJ - \kappa\nabla T \tag{5.4}$$

Where, σ is the thermoelectric material's electrical conductivity, S is the Seebeck coefficient and κ is the thermal conductivity of the thermoelectric material and T is the absolute temperature.

The steady state equation for heat transfer is given by [11, 23]:

$$-\nabla \cdot q + q' = 0 \tag{5.5}$$

$$q' = J \times E = \frac{J^2}{\sigma} + J \cdot ST \tag{5.6}$$

Thus, the three-dimensional model that governs the thermoelectric effects in the simulation model is expressed as [11, 24]:

$$\nabla(\kappa\nabla T) + \frac{J^2}{\sigma} - TJ \cdot [\left(\frac{\partial S}{\partial T}\right)\nabla T + (\nabla S)_T] = 0 \qquad (5.7)$$

Where, the first term on the left-hand side denotes Fourier heat conduction due to temperature difference, the second term stands for the Joule heat and the third term represents the temperature dependent effects of thermoelectric materials (Thomson effect). Assuming a steady-state condition, where the Thomson effect of thermoelectric materials, contact resistances, heat losses by conduction and convection are not taken into account; the cooling power (Qc) for a single thermoelectric leg pair is given as [11, 24]:

$$Q_c = \left(S_p - S_n\right)T_c I - \frac{1}{2}I^2 R - K(T_H - T_c) \qquad (5.8)$$

Where, S_p and S_n denote the Seebeck coefficient for p and n-type materials respectively; T_H and T_C denote the temperature on the hot side and cold side, respectively, I is the applied current, R is the electrical resistance of the leg pair ($R=\rho L/A$) and K denotes the thermal conductance of the leg pair ($K=\kappa A/L$). The symbols ρ, κ, L and A denote the electrical resistivity, thermal conductivity, length of leg pair and cross-sectional area of the leg pair, respectively. In the equation for cooling power, the second term which stands for the Joule heat and the third term which stands for the Fourier heat conduction play a significant part and are affected by the geometric parameters of the thermoelectric leg pair [11]. Hence, the thermoelectric leg geometry parametrization and its impact on a free-standing thermoelectric leg pair and a SimTEC via pair integrated in the glass substrate are investigated in the next section.

The simulation model for a free-standing TEC leg pair consists of a p-type leg and an n-type leg half filled with copper and half filled with thermoelectric materials. Electrodeposited BiSbTe and Bi_2Te_3 are considered as the p-type and n-type thermoelectric materials respectively in the simulation. The top and bottom interconnect is considered as 3 µm thick copper traces. An aluminium heat sink is connected to the hot side of the TEC, which is electrically isolated from the bottom traces with a thin layer of aluminium dioxide.

Table 5.2: Thermoelectric properties of the materials measured at room temperature.

	Thermoelectric Properties			
Materials	**Seebeck Coefficient (μV/K)**	**Electrical Conductivity (S/m × 10^6)**	**Thermal Conductivity (W/m.K)**	**Ref.**
BiSbTe (p-type TE)	90.50	0.026	0.60	[25]
Bi_2Te_3 (n-type TE)	-121	0.052	0.85	[26]
Copper	1.50	59.60	398	
Glass	Electrically isolated	Electrically isolated	1.20	
Aluminium Dioxide	Electrically isolated	Electrically isolated	30	
Aluminium	Electrically isolated	Electrically isolated	237	

Electrical contact resistance (R_c) at the copper and thermoelectric material interfaces is considered as 1×10-11 Ωm^2 [26, 27]. Thermal contact resistance and heat losses by convection and radiation are not included in the simulation model for simplification. In the case of SimTEC, the simulation model remains the same with the addition of glass substrate around the p-type and n-type vias, such that glass is thermally connected to the vias but electrically isolated from the current flowing through the vias and the copper interconnects. The initial parameters in the simulation model are 30 μm diameter, 60 μm pitch and 100 μm height of the cylindrical leg pair/via pair. The fabrication of free-standing micro-TEC pillars with height >20 μm becomes extremely difficult and we are using the simulation models of the free-standing micro-TEC pillars in this chapter for an equivalent comparison with SimTEC device performance. The height of the glass substrate is kept the same as the via height. Simulation parameters in a single via pair such as via diameter, via height, via pitch, and fill-factor (filling ratio of thermoelectric material and copper) are investigated in the case of SimTEC and compared with the equivalent free-standing micro-TEC leg pair case. The simulation model for Free-standing micro-TEC pillars and SimTEC vias is shown in **Figure 5.3**.

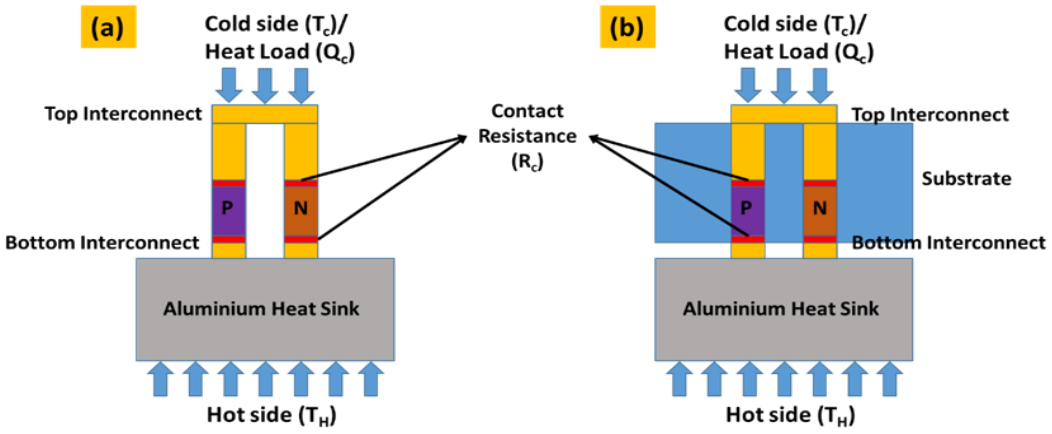


Figure 5.3: Simulation model for (a) Free-standing micro-TEC leg pair and (b) SimTEC via pair.

5.3 Results and Discussions

5.3.1 Substrate Integrated Micro-TEC

In this study, three different substrates glass, silicon and air with their thermal conductivities 1.2, 148 and 0.02 W/m.K respectively, are chosen in order to see the influence on cooling performance of the thermoelectric cooler. **Figure 5.4** shows the temperature gradient (ΔT) of free-standing TEC and segmented TEC for three different substrate materials. In this case for both SimTEC and free-standing micro-TEC pillars, the via diameter, via pitch and via height are considered as 30 µm, 60 µm and 100 µm respectively. These geometric characteristics are made possible by employing thin glass manufacturing, laser-assisted via creation within the glass, and successful electroplating of both copper and thermoelectric material. These combined efforts ultimately play a role in reducing the overall package size [28-30]. As the input current is increased **Figure 5.4(a)** and **(b)**, the temperature gradient of fully-filled and partially-filled segmented SimTEC in glass substrate increases to a maximum value of 3.314 K and 3.629 K respectively due to the combined Peltier and Fourier effects, followed by ΔT starts decreasing due to the overpowering joule heating effect (I^2R). In the case of both segmented and fully-filled devices, the ΔT across the SimTEC device is significantly less than that of the free-standing micro-TEC. For example, the ΔT in the case of segmented free-standing micro-TEC is 20.45 K whereas the ΔT in the case of segmented SimTEC vias is only 3.629 K (approximately six times lesser than 20.45 K).

This is because of the substrate material, which is in physical contact with the pillars and provides an additional heat dissipation path. In other words, the substrate allows a part of the heat to be transferred through heat conduction and decreases the temperature difference between the top and bottom copper interconnects on the substrate. As expected, the increase in thermal conductivity of the substrate material leads to a further decrease in thermal resistance and lends a thermal shunt path through the substrate. As a result, the ΔT keeps decreasing as thermal conductivity of the substrate material increases, with approximately no cooling for the silicon substrate because of the high thermal conductivity of silicon substrate (148 W/m.K). The simulation results highlighting the temperature distribution across the free-standing micro-TEC pillars, SimTEC vias in glass substrate and SimTEC vias in silicon substrate are shown in **Figure 5.5**. This figure also clearly shows the decrease in the temperature gradient across the top and bottom interconnects of the TEC from **Figure 5.5(a)** to **Figure 5.5(c)**, which is perpetuated due to the thermal losses in glass and silicon substrates.

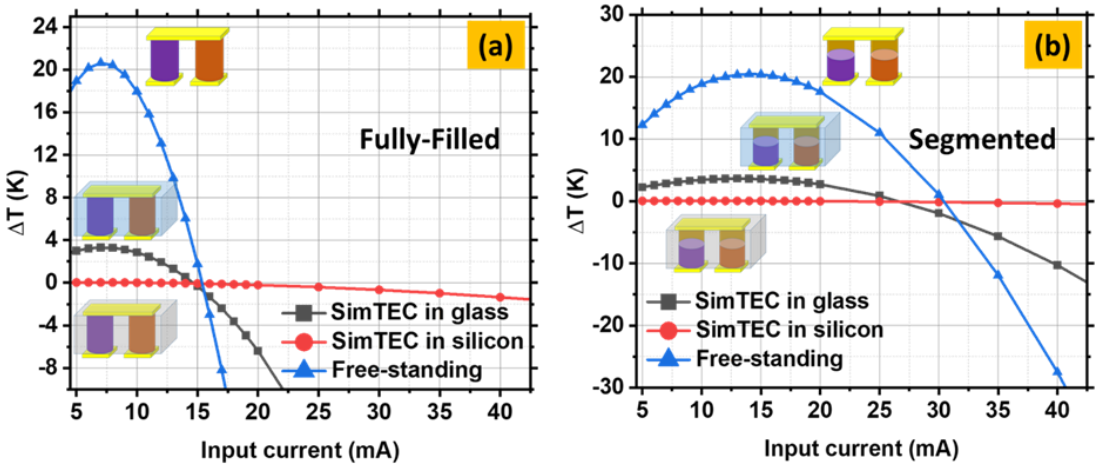


Figure 5.4: Graphs showing the change in temperature gradient in the case of a Substrate integrated micro-TEC (SimTEC) when the substrate is varied between glass, silicon and the case where the micro-TEC pillars are free-standing (no substrate). This variation in cooling capability is highlighted in both conditions when the vias/pillars are (a) fully-filled with thermoelectric material and (b) when they are segmented i.e. half-filled with thermoelectric material and half-filled with copper.

Table 5.3: Table showing the cooling capacity of Fully-Filled and Segmented pillars/vias in Free-standing and SimTEC configurations when $\Delta T=\Delta T_{max}$.

	Q_c (mW)	
	Fully-Filled	**Segmented**
SimTEC in Glass	0.2036	0.3898
SimTEC in Silicon	0.2321	0.4019
Free-standing micro-TEC	0.000504	0.002652

The input current corresponding to maximum ΔT in the case of fully-filled vias is lower (approximately halved) as compared to that of the segmented vias in the case of both SimTEC and free-standing micro-TEC pillars. This is due to the increased electrical resistance and thermal resistance for the vias fully-filled with thermoelectric material as compared to the segmented vias half-filled with copper and half-filled with thermoelectric material. The input optimum current in **Figure 5.4(a)** corresponding to maximum ΔT increases from 6 mA in the case of SimTEC with silicon substrate to 7 mA in case of both SimTEC with glass and free-standing micro-TEC. Similarly, the input current in **Figure 5.4(b)** and **Figure 5.5** corresponding to maximum ΔT increases from 9 mA in the case of SimTEC with silicon substrate to 13 mA in case of SimTEC with glass to 14 mA in the case of free-standing micro-TEC. Based on the results, glass is a superior material for SimTEC as compared to silicon. It allows the temperature control of the micro-TEC over a broader range of input currents. The cooling capacity Q_c which is the maximum heat that can be effectively dissipated from the surface of a thermoelectric device is calculated in **Table 5.3**. As shown in **Table 5.3**, the cooling power (also mentioned in Section 5.2) of the segmented pillars/vias is higher than that of the fully-filled thermoelectric material filled pillars/vias (for approximately similar ΔT_{max}) because of the increase in operating current corresponding to maximum cooling. The cooling capacity in the case of fully-filled free-standing micro-TEC pillars is the smallest (approaching zero) as it is operating at maximum ΔT.

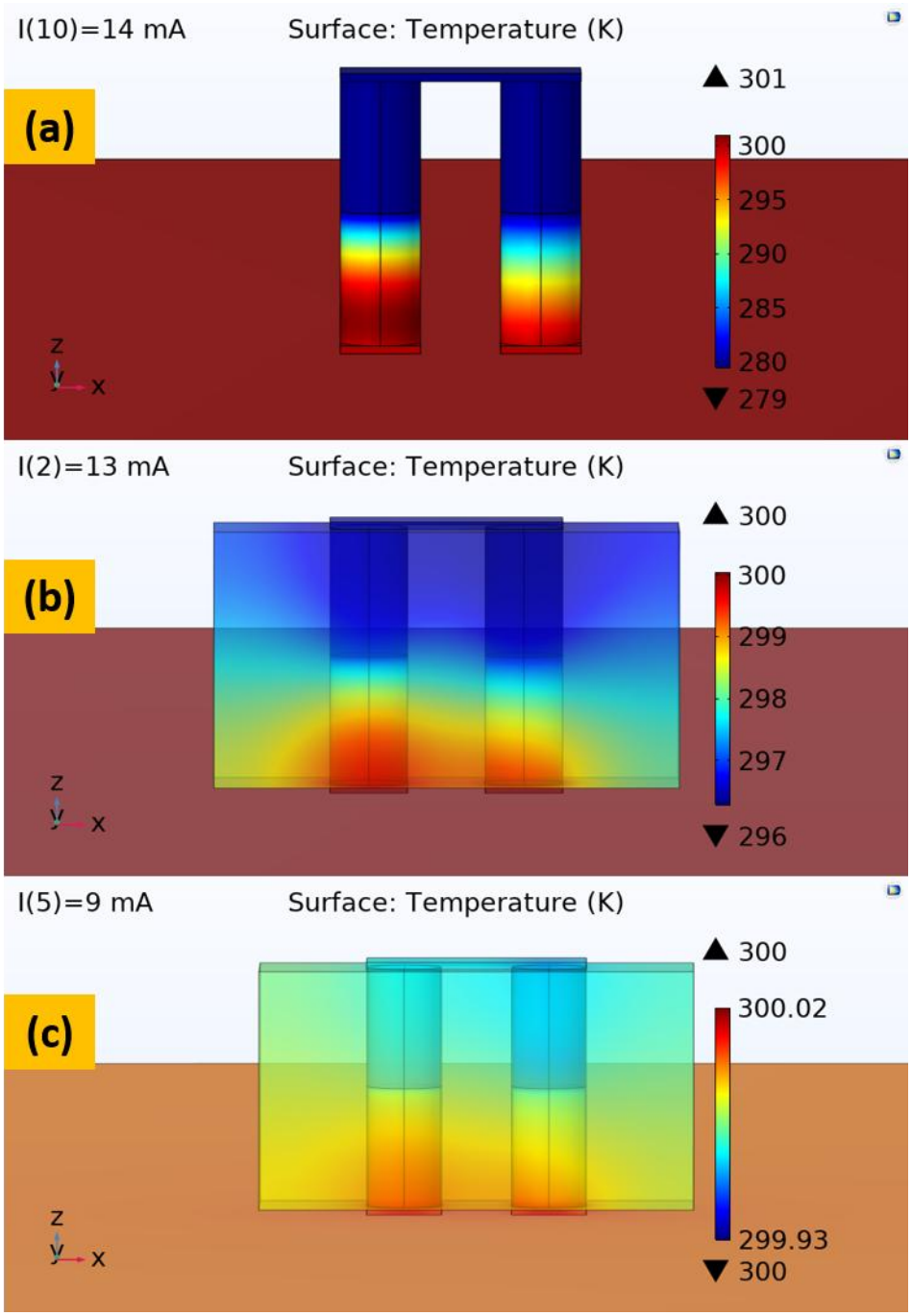


Figure 5.5: Simulation results showing the temperature gradient across the top and bottom interconnects in the case of (a) Free-standing micro-TEC pillars (b) SimTEC vias in glass Substrate and (c) SimTEC vias in silicon Substrate, showing the thermal losses silicon contributing to the decrease in maximum temperature gradient across the TEC.

5.3.2 Effect of SimTEC via diameter

In the case of both free-standing micro-TEC pillars and SimTEC in glass substrate, the via/pillar diameter is increased from 30 to 50 µm, whereas the pitch and via/pillar height is kept constant at 60 µm and 100 µm, respectively. **Figure 5.6 (a)** and **(b)** show the effect of increasing leg diameter in free-standing micro-TEC and increasing via diameter in SimTEC on temperature gradient. As discussed in the last section 5.3.1, the temperature gradient initially goes up and then goes down with applied current because of the combined effects of the Peltier effect, Fourier heat and Joule heating. The increase in pillars diameter in the case of free-standing micro-TEC leads to a decrease in electrical resistance but it also implies that the thermal conductance of the device would increase. These two opposing phenomena lead to a drop in ΔT. However, in the case of glass SimTEC as the via diameter increases, the temperature gradient across the device increases steadily. The SimTEC with diameter 50 µm shows the maximum ΔT of 7.96 K, which is approximately double as compared to that of the SimTEC with the diameter of 30 µm. As the diameter of the vias is increasing, the gap between the vias becomes smaller which means that there is smaller volume of glass between the vias. This decreasing volume of glass between the vias limits the thermal leakage in the glass substrate between the vias and hence an increase in device cooling performance.

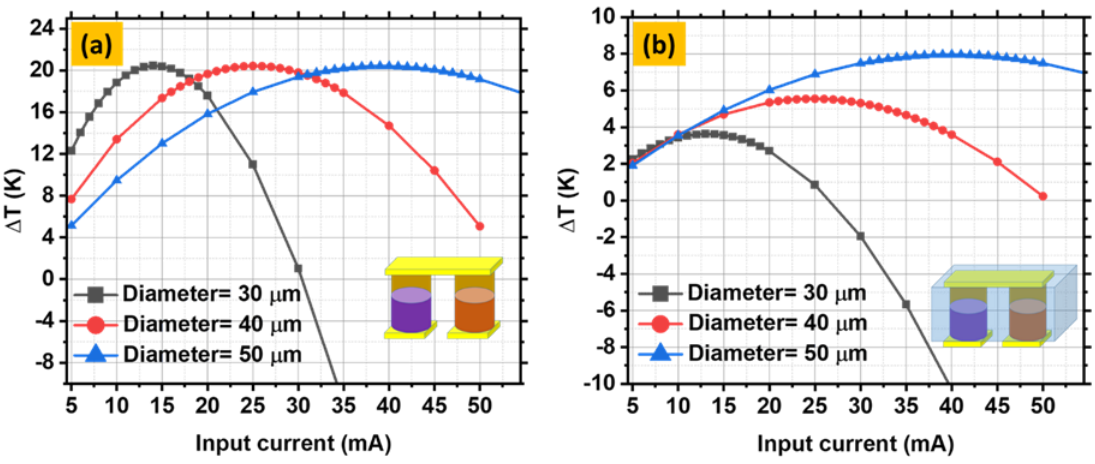


Figure 5.6: Graphs showing the change in temperature gradient in the case of (a) Free-standing micro-TEC pillars and (b) SimTEC vias in glass when the diameter of the vias/pillars partially filled with copper/thermoelectric material is varied from 30 µm to 50 µm, when the pitch and height of the vias/pillars is kept constant.

Table 5.4: Table showing the cooling capacity of Free-standing micro-TEC pillars and SimTEC vias configurations when $\Delta T=\Delta T_{max}$ for different pillar/via diameter.

	Q_c (mW)	
Diameter (µm)	**Free-standing micro-TEC**	**SimTEC in Glass**
30	0.002652	0.3898
40	0.004917	0.6248
50	0.007419	0.8207

The cooling performance of the free-standing micro-TEC is better as compared to SimTEC because of no thermal losses (thermal shunt) in the glass substrate. In both **Figure 5.6 (a)** and **(b)**, the input current corresponding to the maximum cooling of the TEC increases with increasing diameter because of the decreasing overall electrical resistance of the device. The current values for the corresponding maximum ΔT remain approximately same in both free-standing micro-TEC and SimTEC, because of the same electrical resistance of the device. The cooling capacity, as shown in **Table 5.4**, in both cases increase with the increase in diameter of pillars/vias due to the decrease in both electrical and thermal resistance of the device. The reduced electrical resistance leads to a decrease in the joule heat (I^2R) distribution to the cold end.

5.3.3 Effect of SimTEC via height

In this study, both free-standing micro-TEC pillars and the segmented via/pillar height of the SimTEC in glass is increased from 50 to 100 µm, whereas the segmented via/pillar diameter, pitch and fill factor is kept constant at 30 µm, 60 µm and 0.5 respectively. The height of the pillars is a crucial factor for the cooling performance of the TEC device, as the height influences both the electrical resistance and thermal conductance of the device. In case of segmented free-standing micro-TEC, as the pillar height increases, the electrical resistance increases between the top and bottom copper interconnects and the current flowing through the device decreases. At the same time, the increase in height also leads to a decrease in thermal conductance, which in turn causes an increase in the maximum ΔT from 20.1 K to 20.45 K as shown in **Figure 5.7(a)**. However, an interesting phenomenon is observed in the case of segmented SimTEC, as the via height increases, both the optimum current and ΔT decreases as shown in **Figure 5.7(b)**. As the height of the pillars increases, the volume of glass surrounding the vias also increases.

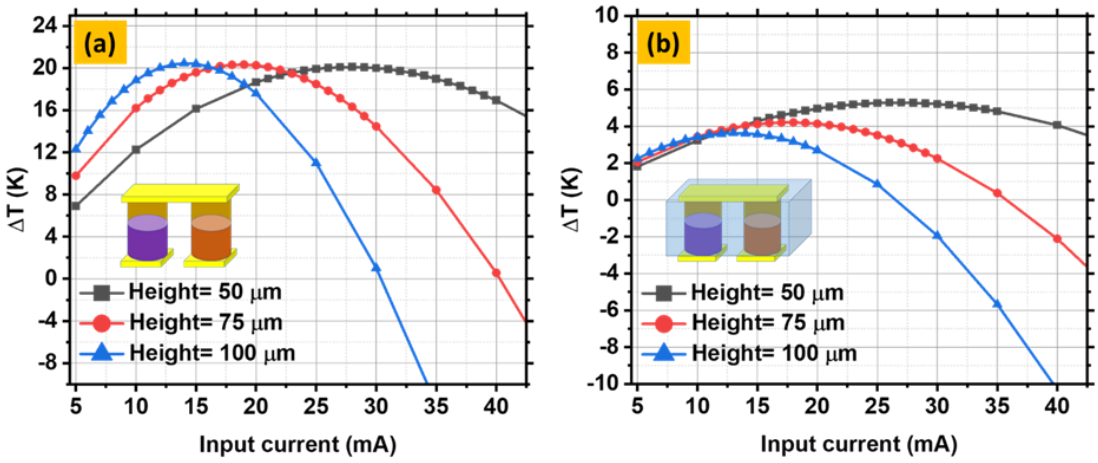


Figure 5.7: Graphs showing the change in temperature gradient in the case of (a) Free-standing micro-TEC pillars and (b) SimTEC vias when the height of the vias/pillars partially filled with copper/thermoelectric material is varied from 50 µm to 100 µm, when the pitch and diameter of the vias/pillars are kept constant.

Table 5.5: Cooling capacity of Free-standing micro-TEC pillars and SimTEC vias configurations when $\Delta T = \Delta T_{max}$ for different pillar/via height.

	Q_c (mW)	
Height (µm)	**Free-standing micro-TEC**	**SimTEC in Glass**
50	0.008074	0.6977
75	0.004257	0.5041
100	0.002652	0.3898

This increasing volume of glass increases the thermal leakage through the substrate (increased thermal losses) and eventually leading to a decrease in device cooling performance. In both cases, the current corresponding to the maximum cooling remains approximately same for varying height and this current decreases with increasing height due to the increasing electrical resistance of the device. The change in ΔT with increasing height is more pronounced in the case of SimTECs as compared to free-standing micro-TECs. In case of SimTEC, the maximum ΔT is 5.28 K, 4.2 K and 3.62 K for the via heights 50 µm, 75 µm and 100 µm, respectively. Hence, larger height of vias deteriorate the cooling performance in the case of SimTEC. As shown in **Table 5.5**, the cooling capacity for both free-standing micro-TEC pillars and the SimTEC vias decreases with increasing height due to the increase in both electrical and thermal resistance of the device.

5.3.4 Effect of SimTEC via pitch

In case of both free-standing micro-TEC pillars and SimTEC vias in glass substrate, the via/pillar height and diameter is kept constant at 100 µm and 30 µm, respectively. The via/pillar pitch is increased from 40 µm to 60 µm in SimTEC and free-standing micro-TEC and its effect on the cooling performance is analysed in each case. In both cases (**Figure 5.8 (a)** and **(b)**) as the pitch is increased, the cooling performance of the device is decreased. In the case of free-standing micro-TEC, the small decrease in ΔT can be attributed to the small increase in the device electrical resistance. The decrease of the maximum ΔT in the case of SimTEC is more pronounced as compared to that of the free-standing micro-TEC.

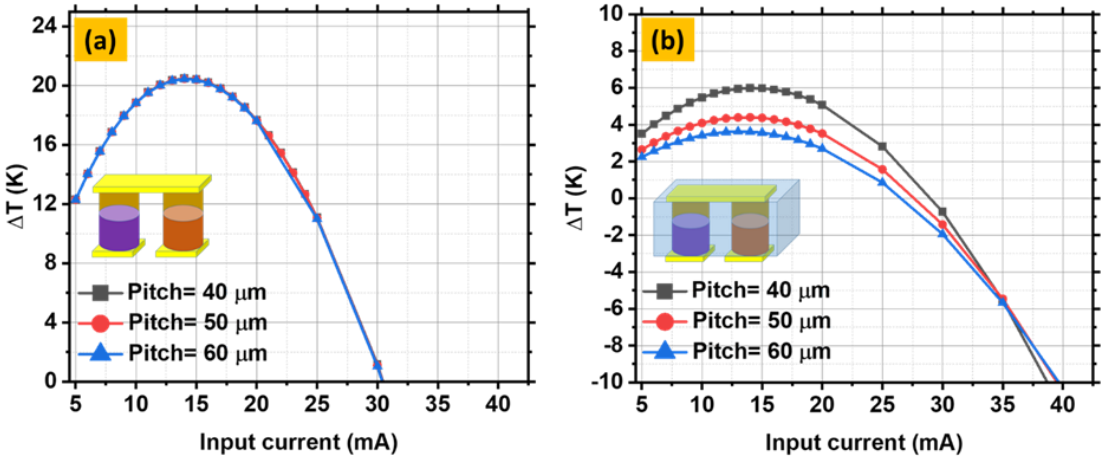


Figure 5.8: Graphs showing the change in temperature gradient in the case of (a) Free-standing micro-TEC pillars and (b) SimTEC vias when the pitch of the vias/pillars partially filled with copper/thermoelectric material is varied from 40 µm to 60 µm, when the diameter and height of the vias/pillars is kept constant.

Table 5.6: The cooling capacity of Free-standing micro-TEC pillars and SimTEC vias when $\Delta T=\Delta T_{max}$ for different pillar/via pitch.

	Q_c (mW)	
Pitch (µm)	**Free-standing micro-TEC**	**SimTEC in Glass**
40	0.002252	0.3415
50	0.002447	0.3785
60	0.002652	0.3898

This significant decrease in maximum (ΔT) is because of the increasing glass volume between the vias as the pitch increases, leading to an increasing parallel thermal

conductance path between the top and bottom copper interconnects on the glass substrate. The maximum ΔT achieved is 5.99 K, 4.4 K and 3.63 K for 40, 50 and 60 µm pitches respectively. Interestingly, the current corresponding to the maximum device cooling performance remains the same at approximately 14 mA in both cases because the via dimensions remain unchanged [31]. The cooling capacity for both the cases (free-standing micro-TEC pillars and SimTEC vias) increase with an increase in the pillar/via pitch mainly due to the decrease in ΔT_{max}, as the current corresponding to maximum cooling remains the same.

5.3.5 Effect of SimTEC fill factor

In case of both segmented free-standing micro-TEC pillars and segmented SimTEC in glass substrate, the via/pillar height, diameter and pitch is fixed as 100, 30, 60 µm, respectively. The volume of the thermoelectric material is increased from 25% to 100% in the vias/pillars. This filling ratio of thermoelectric material in the via/pillar is denoted as fill-factor, which is changed from 0.25 (a quarter filled with thermoelectric material) to 1 (fully-filled with thermoelectric material). In case of free-standing micro-TEC, as the fill-factor of the thermoelectric material increases, the maximum temperature gradient of the device increases by a small proportion as shown in **Figure 5.9 (a)**. This is due to the increment in the volume of thermoelectric material between the copper interconnects on the top and bottom of the pillars which enhances the contribution of the Peltier effect.

Conversely, in case of SimTEC vias as the volume of the thermoelectric material increases, the maximum ΔT decreases. The reason behind this is change of the primary heat flow path from the thermoelectric material filled vias to glass substrate (as the thermal conductivity of glass substrate is higher than the thermal conductivity of the thermoelectric materials) leading to an increased thermal conductance between the top and bottom copper interconnects. When the fill factor is varied from 0.25 to 1, the maximum ΔT falls from 5.15 K to 3.31 K. The decrease in maximum ΔT for SimTEC is more pronounced as compared to the increase in ΔT for the free-standing micro-TEC.

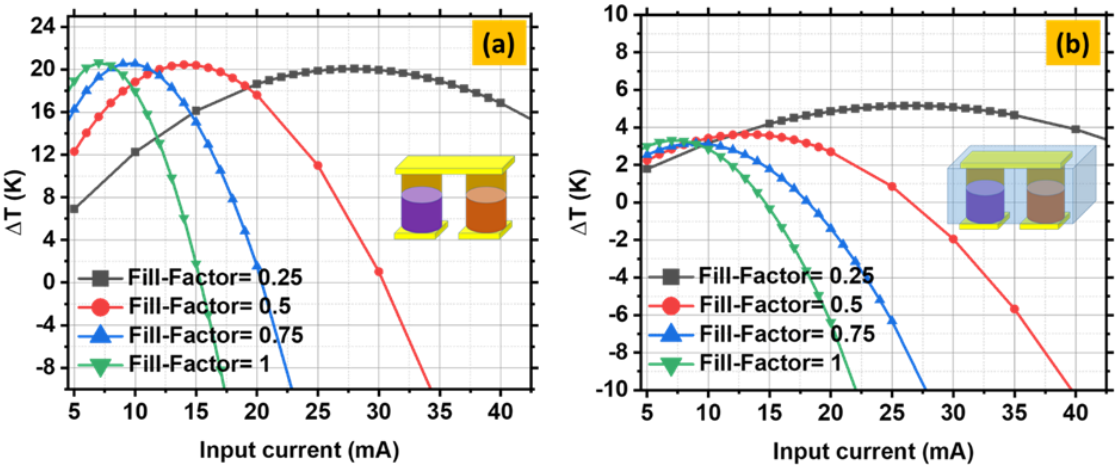


Figure 5.9: Graphs showing the change in temperature gradient in case of (a) Free-standing micro-TEC pillars and (b) SimTEC vias when the fill-factor (filling ratio of thermoelectric material and copper in vias/pillars) is varied from 25% ($1/4^{th}$ of the cylinder filled with thermoelectric material and $3/4^{th}$ of the cylinder is filled with copper) to 100% (the whole cylinder is filled with thermoelectric material), when the diameter, pitch and height of the vias/pillars is kept constant.

Table 5.7: Cooling capacity of Free-standing micro-TEC pillars and SimTEC vias configurations when $\Delta T=\Delta T_{max}$ for different fill factor.

	Q_c (mW)	
Fill-Factor of TE material	**Free-standing micro-TEC**	**SimTEC in Glass**
0.25	0.012321	0.7039
0.5	0.002652	0.3898
0.75	0.001088	0.2713
1	0.000504	0.2036

The different current values corresponding to the maximum ΔT of the device as the fill-factor is increased remains approximately same in the case of SimTEC vias and free-standing micro-TEC pillars. The electrical resistance of the vias/pillars increases with increasing volume of thermoelectric material and decreasing copper volume. This explains the trend of decreasing optimum current value with increasing fill-factor. The decreasing cooling capacity of the free-standing micro-TEC pillars and SimTEC vias with increasing fill-factor (of thermoelectric material) is accounted due to the increase in electrical and thermal resistance of the device.

5.4 Optimization Analysis for SimTEC

Design of Experiments (DOE) is an established method to highlight the effect of multiple factors on the response of the resultant parameter [32]. In our case, the independent factors such as diameter, height and pitch of the vias in SimTEC and the pillars in free-standing micro-TEC are varied and the resulting effect on the variation of maximum temperature gradient across the device is analysed. The diameter, height and pitch of the vias/pillars are all varied among three values. The diameter is varied between 30 µm, 40 µm and 50 µm; height is varied between 50 µm, 75 µm and 100 µm and the pitch is varied between 60 µm, 80 µm and 100 µm. In addition, the pitch is varied such that it is twice the diameter values. The resulting maximum temperature gradient and cooling power in this 3×3×3 factorial design is also tabulated for both cases of SimTEC and free-standing micro-TEC, where the fill-factor is kept constant at 0.5.

Table 5.8: Design of Experiment (DOE) for the three geometrical factors (Diameter, Height and Pitch) of the free-standing micro-TEC pillars and SimTEC vias showing their impact on the temperature gradient and cooling power of free-standing micro-TEC and SimTEC device.

Number	Diameter (µm)	Height (µm)	Pitch (µm)	max(ΔT) Free-standing	Q_c Free-standing micro-TEC (mW)	max (ΔT) SimTEC	Q_c SimTEC (mW)
1	30	50	60	20.1067	0.008074462	5.2848	0.697759
2	30	75	80	20.2882	0.005066396	3.6226	0.513925
3	40	50	60	20.0673	0.014681976	7.1296	1.089483
4	40	75	60	20.3092	0.007614643	6.1392	0.793398
5	40	50	80	19.9796	0.018598842	6.2246	1.156967
6	40	75	80	20.2497	0.009387806	4.9708	0.851657
7	30	50	100	19.9685	0.011643759	4.6711	0.717313
8	50	50	100	19.8263	0.037062469	7.0281	1.692721
9	30	100	60	20.4514	0.002651843	3.6294	0.389838
10	50	50	60	20.0467	0.022090723	9.3069	1.421228
11	50	100	60	20.4226	0.007418645	7.9608	0.820746

12	30	100	100	20.3825	0.003538767	2.6737	0.400488
13	50	100	100	20.309	0.011386614	4.8139	1.00867
14	30	75	100	20.2403	0.005896732	3.3898	0.520577
15	40	100	60	20.4336	0.004917396	5.5472	0.624838
16	40	50	100	19.8902	0.022671149	5.9362	1.172181
17	50	50	80	19.9367	0.02985582	7.5244	1.642173
18	50	75	60	20.297	0.011625882	8.5025	1.037028
19	30	100	80	20.4172	0.003089285	2.9448	0.405407
20	40	100	80	20.3882	0.005933945	4.2368	0.67331
21	40	100	100	20.3419	0.006987212	3.7337	0.685747
22	50	75	80	20.2219	0.015031876	6.3777	1.212063
23	50	100	80	20.3664	0.009330016	5.658	0.961647
24	50	75	100	20.1455	0.018691193	5.6683	1.265605
25	30	50	80	20.0382	0.009833355	4.8414	0.710663
26	30	75	60	20.3354	0.004257387	4.2092	0.504128
27	40	75	100	20.1891	0.011226951	4.5552	0.866411

Figure 5.10 shows the change in maximum temperature gradient (ΔT) across all three parameters (Diameter, Height and Pitch); where the trends $(\Delta T/\Delta D)_{P,H}$ observed in the SimTEC is opposite to that observed in the equivalent free-standing micro-TEC structure. The influence of the geometrical parameters of the pillars in terms of thermal resistance and electrical resistance of the device in turn affects the maximum temperature gradient and cooling power. In addition to this, the thermal losses in the glass substrate impacts the opposing trend of maximum temperature gradient with changes in diameter and height of SimTEC as compared to the free-standing micro-TEC.

Moreover, these thermal losses due to the glass substrate are mainly responsible for the decrease in maximum temperature gradient (ΔT=9.3 K) for SimTEC as compared to the maximum temperature gradient (ΔT=20.45 K) for free-standing micro-TEC, amounting to a decrease of approximately 54%.

In case of free-standing micro-TEC, averaging the impact of diameter, height and pitch of TEC pillars on the change in maximum temperature gradient shows that the order of this impact is Height > Pitch > Diameter. However, for the SimTEC vias, parametric impact on change in maximum temperature gradient (ΔT) across the TEC follows the order of Diameter > Height > Pitch.

This parameter variation also allows the maximum temperature gradient (ΔT) in SimTEC, which varies from a minimum of 2.67 K to a maximum of 9.3 K, amounting to a total variation of 6.63 K. Whereas, in micro-TEC, it only allows for the variation of a maximum cooling range from 19.82 K to 20.45 K (total variation of 0.63 K). Interestingly, this ΔT variation in case of free-standing micro-TEC pillars (19.82 K to 20.45 K) leads to a decrease in cooling capacity from 0.037 to 0.002 mW, which then leads to a trade-off between ΔT_{max} and Q_c(at ΔT_{max}). The ΔT variation in case of SimTEC vias (2.67 K to 9.3 K) allows for a corresponding increase in cooling capacity from 0.4004 to 1.42 mW.

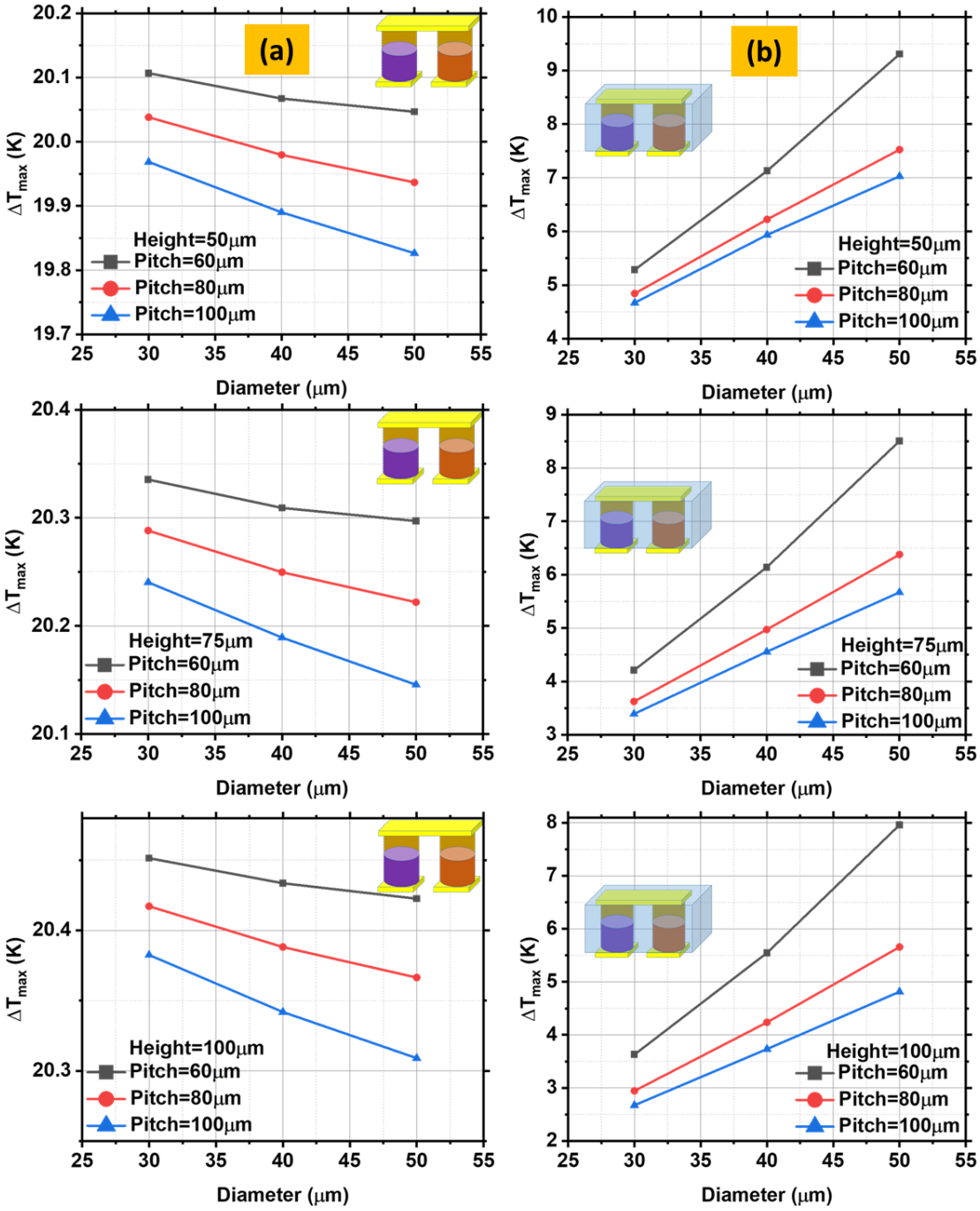


Figure 5.10: Graphs showing the change in the maximum temperature gradient of (a) Free-standing micro-TEC pillars and (b) SimTEC vias when the diameter, height and pitch of the vias/pillars are varied simultaneously where the fill-factor if the via/pillar is kept constant at 50%.

5.5 Conclusion

The integration of TEC capabilities in glass substrates through the SimTEC approach provides a highly attractive thermal management solution for next generation highly integrated electronic-photonic packaged systems. It addresses the need for thermal isolation and control between package components, while maintaining a compact form factor. This work has presented a theoretical analysis of the cooling capability of SimTEC and compared its cooling performance to similarly sized free-standing micro-TEC device. The glass platform in this novel design provides structural rigidity and allows the fabrication processes to be relaxed for embedded micro scale thermoelectric coolers. As discussed in this work, the disadvantage of the SimTEC approach is that higher thermal conductivity of the glass compared to the thermoelectric materials acts to diminish the overall cooling potential. As a result, the maximum temperature gradient of SimTEC decreases by approximately six times as compared to the maximum temperature gradient of free-standing micro-TEC device, which is discussed in Section 5.3.1. This discrepancy primarily arises due to the thermal losses in the glass substrate.

Notably, the range of variation in maximum ΔT resulting from changes in via parameters (diameter, height, and pitch altered concurrently) in SimTEC is 6.63 K, as compared to a mere 0.63 K in the equivalent free-standing micro-TEC device. This range illustrates that increasing the via diameter, decreasing the via height, and reducing the via pitch enhances the cooling performance in SimTEC, with a peak improvement of ΔT = 9.3 K achieved when the fill-factor ratio of thermoelectric material and copper in the pillar/via is maintained constant at 0.5. Moreover, within the simulated range of via parameters, the thermal tuning capability of SimTEC stands at 18.6 K (2×9.3 K). This allows for both heating and cooling of the top via interconnect and photonic chips through the reversal of input current polarity based on environmental thermal fluctuations.

However, it is important to acknowledge that despite its advantages, the cooling capability of SimTEC remains inferior to that of the free-standing micro-TEC device. As a result, SimTEC is better suited for thermal stabilization rather than specialized cooling applications.

Nevertheless, the potential for enhancing SimTEC thermal tuning and cooling efficiency lies in optimizing the performance of the thermoelectric material (zT), which would facilitate a more efficient thermoelectric conversion process and consequently increase the temperature gradient across the top and bottom interconnects of SimTEC vias.

Future Work

The next steps for this work are to include the simulation of complete SimTEC devices in the glass interposer underneath the electronic chips (EICs) and photonic chips (PICs) and analyse the active temperature control of the PIC/EIC. The authors also envision that the SimTEC architecture can be expanded to a multi-layered glass substrate [33], where the thin glass substrate layer with SimTEC can be stacked on top of the glass substrate layer with SimTEG (substrate integrated micro-thermoelectric generator). This will enable the heat load pumped out from the hot side of the SimTEC layer to be used as an input by the SimTEG layer [34] for power generation in the package.

5.6 References

[1] L. Carroll et al., "Photonic Packaging: Transforming Silicon Photonic Integrated Circuits into Photonic Devices," Applied Sciences, vol. 6, no. 12, p. 426, 2016. [Online]. Available: https://www.mdpi.com/2076-3417/6/12/426.

[2] R. Enright, S. Lei, G. Cunningham, I. Mathews, R. Frizzell, and A. Shen, "Integrated Thermoelectric Cooling for Silicon Photonics," ECS Journal of Solid State Science and Technology, vol. 6, no. 3, p. N3103, 2017/02/16 2017, doi: 10.1149/2.0151703jss.

[3] H. Schröder, L. Brusberg, and G. Böttger, "Strategies for glass based photonic system integration," in Proceedings of the 5th Electronics System-integration Technology Conference (ESTC), 16-18 Sept. 2014 2014, pp. 1-7, doi: 10.1109/ESTC.2014.6962732.

[4] B. Chou et al., "Co-Design and Demonstration of a Fully Integrated Optical Transceiver Package Featuring Optical, Electrical, and Thermal Interconnects in Glass Substrate," International Symposium on Microelectronics, vol. 2016, no. 1, pp. 000007-000012, 2016, doi: 10.4071/isom-2016-TP12.

[5] L. Brusberg et al., "Glass Substrate With Integrated Waveguides for Surface Mount Photonic Packaging," Journal of Lightwave Technology, vol. 39, no. 4, pp. 912-919, 2021, doi: 10.1109/JLT.2020.3033295.

[6] H. Schroder, L. Brusberg, N. Arndt-Staufenbiel, J. D.-I. Hofmann, and S. Marx, "Glass panel processing for electrical and optical packaging," 2011 IEEE 61st Electronic Components and Technology Conference (ECTC), pp. 625-633, 2011.

[7] S. Cho, V. Sundaram, R. R. Tummala, and Y. K. Joshi, "Impact of Copper Through-Package Vias on Thermal Performance of Glass Interposers," IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 5, no. 8, pp. 1075-1084, 2015, doi: 10.1109/TCPMT.2015.2450731.

[8] K. Kröhnert et al., "High Aspect Ratio Through-Glass Vias as Heat Conductive Element," in 2022 IMAPS Nordic Conference on Microelectronics Packaging (NordPac), 12-14 June 2022 2022, pp. 1-6.

[9] P. Gupta et al., "Impact of Through Glass Vias Filling on the Performance of Passive Thermal Cooling in Photonic Packages," in 2022 IEEE 9th Electronics

System-Integration Technology Conference (ESTC), 13-16 Sept. 2022 2022, pp. 391-397, doi: 10.1109/ESTC55720.2022.9939531.

[10] K. Padmaraju and K. Bergman, "Resolving the thermal challenges for silicon microring resonator devices," Nanophotonics, vol. 3, no. 4-5, pp. 269-281, 2014, doi: doi:10.1515/nanoph-2013-0013.

[11] R. Kaur, A. Tanwar, P. Gupta, N. Padmanathan, P. O. Brien, and K. M. Razeeb, "Design Optimization of Micro-Thermoelectric Cooler for Thermal Management using Finite Element Simulations," in 2022 28th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC), 28-30 Sept. 2022 2022, pp. 1-6, doi: 10.1109/THERMINIC57263.2022.9950684.

[12] P. Zhang et al., "Intelligent Design and Tuning Method for Embedded Thermoelectric Cooler (TEC) in 3-D Integrated Microsystems," IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 13, no. 6, pp. 788-797, 2023, doi: 10.1109/TCPMT.2023.3292185.

[13] G. Bognár, G. Takács, and P. G. Szabó, "A novel approach for cooling chiplets in heterogeneously integrated 2.5D packages applying microchannel heatsink embedded in the interposer," IEEE Transactions on Components, Packaging and Manufacturing Technology, pp. 1-1, 2023, doi: 10.1109/TCPMT.2023.3298378.

[14] R. Mahajan et al., "Co-Packaged Photonics For High Performance Computing: Status, Challenges And Opportunities," Journal of Lightwave Technology, vol. 40, no. 2, pp. 379-392, 2022, doi: 10.1109/JLT.2021.3104725.

[15] M. S. Nezami et al., "Packaging and Interconnect Considerations in Neuromorphic Photonic Accelerators," IEEE Journal of Selected Topics in Quantum Electronics, vol. 29, no. 2: Optical Computing, pp. 1-11, 2023, doi: 10.1109/JSTQE.2022.3200604.

[16] W. Luo et al., "Recent progress in quantum photonic chips for quantum communication and internet," Light: Science & Applications, vol. 12, no. 1, p. 175, 2023/07/14 2023, doi: 10.1038/s41377-023-01173-8.

[17] A. S. Dutt et al., "Geometric Study of Polymer Embedded Micro Thermoelectric Cooler with Optimized Contact Resistance," Advanced Electronic Materials, vol. 8, no. 7, p. 2101042, 2022/07/01 2022, doi: https://doi.org/10.1002/aelm.202101042.

[18] S. Liu et al., "Micro-thermoelectric generators based on through glass pillars with high output voltage enabled by large temperature difference," Applied Energy, vol. 225, pp. 600-610, 2018.

[19] W.-Y. Chen, X.-L. Shi, J. Zou, and Z.-G. Chen, "Thermoelectric Coolers: Progress, Challenges, and Opportunities," Small Methods, vol. 6, no. 2, p. 2101235, 2022/02/01 2022.

[20] F. Yang et al., "Research on Wafer-Level MEMS Packaging with Through-Glass Vias," Micromachines, vol. 10, no. 1, p. 15, 2019. [Online]. Available: https://www.mdpi.com/2072-666X/10/1/15.

[21] Q. Zhang, K. Deng, L. Wilkens, H. Reith, and K. Nielsch, "Micro-thermoelectric devices," Nature Electronics, vol. 5, no. 6, pp. 333-347, 2022/06/01 2022, doi: 10.1038/s41928-022-00776-0.

[22] A. Tanwar, S. Lal, R. Kaur, N. Padmanathan, E. Dalton, and K. M. Razeeb, "A fully automated measurement system for the characterization of micro thermoelectric devices near room temperature," Applied Thermal Engineering, vol. 224, p. 120111, 2023/04/01/ 2023, doi: https://doi.org/10.1016/j.applthermaleng.2023.120111.

[23] H. Liu, G. Li, X. Zhao, X. Ma, and C. Shen, "Investigation of the impact of the thermoelectric geometry on the cooling performance and thermal—mechanic characteristics in a thermoelectric cooler," Energy, vol. 267, p. 126471, 2023/03/15/ 2023, doi: https://doi.org/10.1016/j.energy.2022.126471.

[24] R. A. Kishore, A. Nozariasbmarz, B. Poudel, M. Sanghadasa, and S. Priya, "Ultra-high performance wearable thermoelectric coolers with less materials," Nature Communications, vol. 10, no. 1, p. 1765, 2019/04/16 2019, doi: 10.1038/s41467-019-09707-8.

[25] S. Lal, D. Gautam, and K. M. Razeeb, "Optimization of annealing conditions to enhance thermoelectric performance of electrodeposited p-type BiSbTe thin films," APL Materials, vol. 7, no. 3, p. 031102, 2019.

[26] S. Corbett et al., "Electrodeposited Thin-Film Micro-Thermoelectric Coolers with Extreme Heat Flux Handling and Microsecond Time Response," ACS Applied Materials & Interfaces, vol. 13, no. 1, pp. 1773-1782, 2021/01/13 2021, doi: 10.1021/acsami.0c16614.

[27] A. Tanwar, S. Lal, and K. M. Razeeb, "Structural Design Optimization of Micro-Thermoelectric Generator for Wearable Biomedical Devices," Energies, vol. 14, no. 8, p. 2339, 2021. [Online]. Available: https://www.mdpi.com/1996-1073/14/8/2339.

[28] A. B. Shorey and R. Lu, "Progress and application of through glass via (TGV) technology," in 2016 Pan Pacific Microelectronics Symposium (Pan Pacific), 25-28 Jan. 2016 2016, pp. 1-6, doi: 10.1109/PanPacific.2016.7428424.

[29] V. Sundaram et al., "First demonstration of a surface mountable, ultra-thin glass BGA package for smart mobile logic devices," in 2014 IEEE 64th Electronic Components and Technology Conference (ECTC), 27-30 May 2014 2014, pp. 365-370, doi: 10.1109/ECTC.2014.6897313.

[30] B. C. Chou et al., "Modeling, design, and fabrication of ultra-high bandwidth 3D Glass Photonics (3DGP) in glass interposers," in 2013 IEEE 63rd Electronic Components and Technology Conference, 28-31 May 2013 2013, pp. 286-291, doi: 10.1109/ECTC.2013.6575585.

[31] J. Zhang, H. Zhao, B. Feng, X. Song, X. Zhang, and R. Zhang, "Numerical simulations and optimized design on the performance and thermal stress of a thermoelectric cooler," International Journal of Refrigeration, vol. 146, pp. 314-326, 2023/02/01/ 2023, doi: https://doi.org/10.1016/j.ijrefrig.2022.11.010.

[32] W.-H. Chen et al., "A comprehensive review of thermoelectric generation optimization by statistical approach: Taguchi method, analysis of variance (ANOVA), and response surface methodology (RSM)," Renewable and Sustainable Energy Reviews, vol. 169, p. 112917, 2022/11/01/ 2022, doi: https://doi.org/10.1016/j.rser.2022.112917.

[33] T. Iwai et al., "Glass Multilayer Package Substrate using Conductive Paste Via Connection," in 2018 IEEE CPMT Symposium Japan (ICSJ), 19-21 Nov. 2018 2018, pp. 105-108, doi: 10.1109/ICSJ.2018.8602741.

[34] J. Yu, Q. Zhu, L. Kong, H. Wang, and H. Zhu, "Modeling of an Integrated Thermoelectric Generation–Cooling System for Thermoelectric Cooler Waste Heat Recovery," Energies, vol. 13, no. 18, doi: 10.3390/en13184691.

Chapter 6: Copper Clip as Heat Spreaders for Glass Interposers

6.1 Introduction

The co-packaging of electronic (EIC) and photonic chips (PIC) on glass interposers presents a unique thermal management challenge. In order to maintain optimal functionality of the optical elements on the PIC, thermal crosstalk between EIC and PIC needs to be lowered. This is aided by the low thermal conductivity of the glass interposer. On the other hand, the heat dissipated by the EICs must be managed to avoid reliability issues [1]. Hence, the benefit of thermal isolation provided by the glass interposers needs to be balanced against the heat dissipation requirements of the photonic packages.

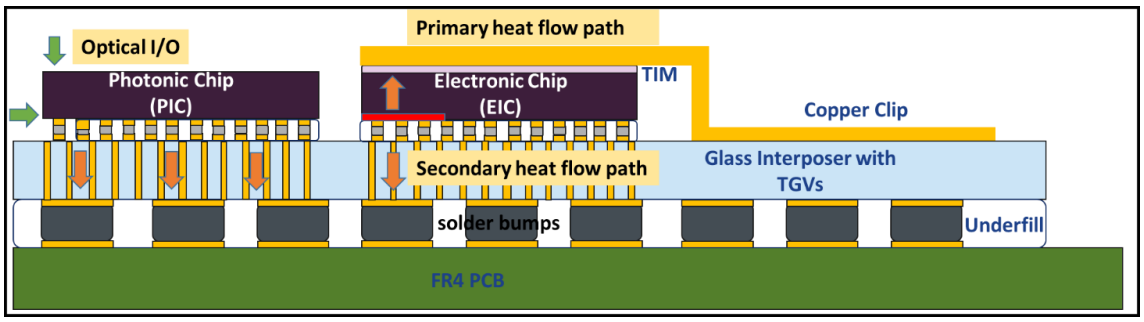


Figure 6.1: Schematic illustrating the heat dissipation pathways for the heat sources on the active region of the electronic chip (EIC). The heat dissipation towards the glass interposer forms a secondary heat flow path due to the solder microbumps and underfill introducing thermal resistance to heat conduction. The heat dissipation towards the topside of the chip and subsequently to the copper clip through the thermal interface material (TIM) forms the primary heat flow path due to its lower thermal resistance.

Previously, the authors have demonstrated using TGVs [2] and SimTEC [3] as a thermal pathway through the glass interposer to dissipate and regulate the heat generated by the electronic chips. This heat flows from the chip's active region towards the glass interposer and PCB is a secondary heat flow path (**Figure 6.1**) [4]. The back end of line (BEOL) wires and the passivation layers which are fabricated on top of the heat-generating regions (transistor-silicon interface) of the electronic chips act as a thermal impediment to the heat conduction (from heat-generating regions of the chip towards the PCB) [5]. The solder bumps and underfill applied between the

chip-interposer interface and the interposer-PCB interface further add to this thermal impediment. Hence, the majority of the heat generated by the active regions of the electronic chips is conducted to the topside of the chip forming the primary heat flow path (**Figure 6.1**). In addition to this, there are certain cases where it is not possible to integrate TGVs under the electronic chips. For example, when there are RF elements on the electronic chip, which can cause electromagnetic interference or reflections between the elements of the electronic chip and TGVs in the glass interposer. In such cases, heat removal from the topside of the electronic chip becomes an essential option.

The heat generated by the electronic chip which spreads to the topside of the chip can hence be removed through the integration of a heat spreader on the electronic chip. The authors have termed this heat spreader as a "copper clip". There is no heat sink or fan integrated on top of the electronic chips to avoid mechanical stress in the solder bump [7] and vibrations [8] in the package. This absence of a heat sink/fan integrated on top of the electronic chips makes the secondary heat flow path significant for investigation in previous chapters. Copper clips also exhibit design and assembly trade-offs between their thermal and thermomechanical behavior, as shown in [9]. Secondly, the heat sink/fan cannot be integrated on top of the photonic chip due to the sensitive optical facets to enable fiber connection (**Figure 6.1**), which again highlights the importance of the secondary heat flow path for the PICs.

Thus, the primary heat flow path is investigated in this chapter through the integration of copper clip on top of the electronic chips to spread the heat generated from the topside of the chip. In Section 6.3, the concept of segregated copper clip and single copper clip is compared through simulation. The Finite Element Method (FEM) simulation model of segregated copper clips involves the use of separate copper clips attached to each of the electronic chips whereas the single copper clip involves a larger surface area of the copper clip covering the top of all electronic chips. There is a trade-off between the two methods from a packaging process development perspective. The segregated copper clips allow the package designer to include electronic chips with differing thickness whereas the integration of a single copper clip is facilitated by a single step pick and place process for copper clip integration in the package. Secondly, the single copper clip must be designed according to the placement of the electronic

chips on the interposer such that the single copper clip covers the entire surface of the electronic chips. However, the segregated copper clips allow flexibility for the different copper clips to be placed at the precise locations where the electronic chips are present on the interposer.

The thermal performance of the electronic chips co-packaged with photonic chips on the glass interposer in the case of segregated copper clips and single copper clip is detailed in Section 6.3. Secondly, the impact of change in parameters such as copper clip thickness, copper clip length, TIM thickness, electronic chip thickness and spacing between electronic chip and photonic chip on the maximum chip temperature is detailed in Section 6.3. Lastly, the importance of a continuous heat flow path through the integration of heat sink in the PCB is explained in Section 6.4. The concept of an extended copper clip, which makes contact with the heat sink is introduced in Section 6.5 through an experiment. The experiment uses reference thermal chips (mentioned in Chapter 3) as the heat source; the cooling of which is studied through the introduction of a copper clip and an extended copper clip.

6.2 Copper Clip for Heat Dissipation

The effectiveness of the heat dissipation through the copper clip is analyzed through the finite element method simulations. The Comsol® multiphysics model includes a silicon PIC co-packaged with silicon electronic chips (EIC1, EIC2 and EIC3) on a glass interposer with no TGVs under the electronic chips. The gap between the three electronic chips is 1mm. There are TGVs under the PIC, where the hourglass shaped TGVs have 50µm diameter and 100µm pitch. The effective in-plane and out-of-plane thermal conductivity of these TGVs are 1.5087 W/m.K and 37.87 W/m.K respectively. The chips are assembled on the glass interposer and the glass interposer is then assembled on the PCB with solder bumps. The sizes and effective thermal conductivity of the elements in the FEM model are shown in **Table 6.1** and **Table 6.2**.

Table 6.1: Geometrical parameters (length, width and height) of the different components in the FEM simulation

Component	Length (mm)	Width (mm)	Height (mm)
PCB	50	50	0.50
Bumps	25	25	0.27
Interposer	25	25	0.46
Microbumps	5	5	0.033
EIC	5	5	0.50
PIC	17	6	0.50
TIM	5	5	0.10
Copper Clip on top of chip	5mm for segregated copper clips 5+5+5+1+1=17mm for single copper clip	5.10	0.50
Copper clip on side of chip	5mm for segregated copper clips 5+5+5+1+1=17mm for single copper clip	0.50	1.033
Copper Clip on top of interposer	5mm for segregated copper clips 5+5+5+1+1=17mm for single copper clip	4	0.50
Copper Clip on side of interposer	5mm for segregated copper clips 5+5+5+1+1=17mm for single copper clip	0.50	1.23
Heat sink in PCB	5mm for segregated copper clips 5+5+5+1+1=17mm for single copper clip	4	0.50

Table 6.2: Effective in-plane and out-of-plane thermal conductivities of different components in the FEM simulation

Component	Effective in-plane thermal conductivity (k_x) (W/m.K)	Effective in-plane thermal conductivity (k_y) (W/m.K)	Effective out-of-plane thermal conductivity (k_z) (W/m.K)
PCB	0.3	0.3	0.3
Bumps	1.8	1.8	4
Interposer	1.2	1.2	1.2
Microbumps	2.8	2.8	4.4
EIC	130	130	130
PIC	130	130	130
Clip	380	380	380
TIM	20	20	20
TGVs under PIC	1.51	1.51	37.87

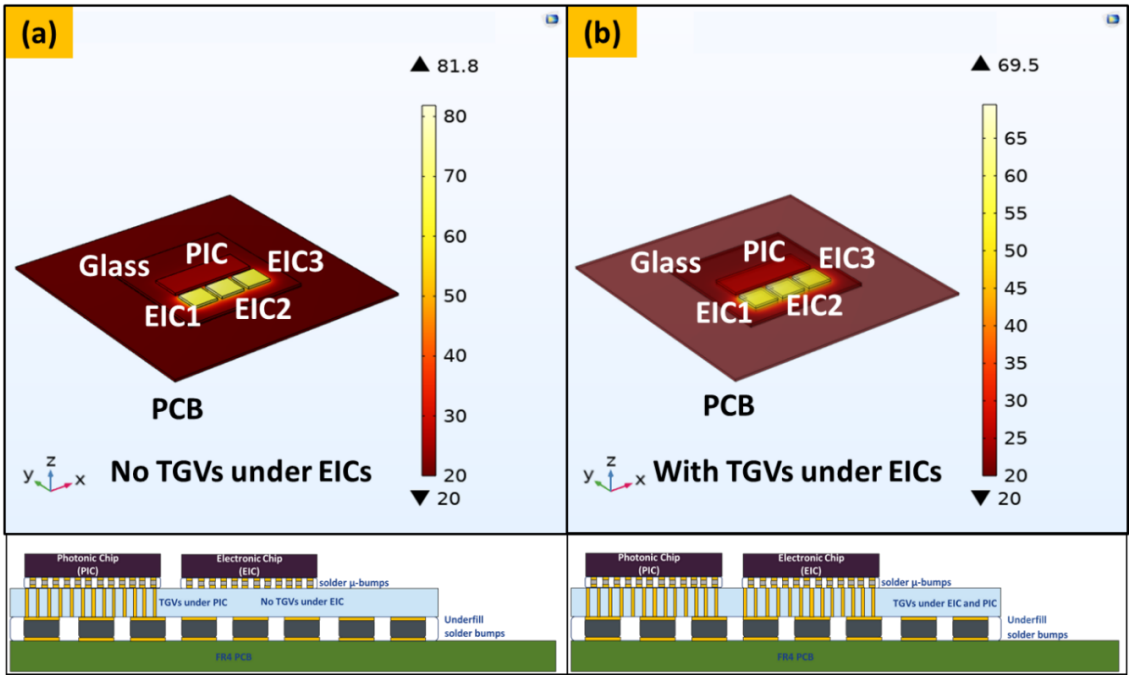


Figure 6.2: Simulation results of the FEM simulation showing the maximum temperature of the co-packaged EICs and PIC with (a) no TGVs under the EICs for heat dissipation and (b) TGVs under the EICs for heat dissipation. The presence of TGVs under the EICs lowers the maximum temperature of the EICs.

Table 6.3: Maximum temperature of the EICs (EIC1, EIC2 and EIC3) and PIC derived from the FEM simulation with no TGVs under the EICs and with TGVs under the EICs

Component	No TGVs under EIC Maximum Temperature (˚C)	TGVs under EIC Maximum Temperature (˚C)
EIC1	79.25	67.31
EIC2	81.82	69.47
EIC3	79.15	67.05
PIC	25.45	25.76

Figure 6.2 shows the impact of the placement of TGVs in the area under the EICs on the maximum temperature of the EICs. The placement of TGVs under the EIC significantly lowers the temperature of the EICs as the TGVs provide a local heat dissipation pathway through the copper vias. There is a minimal increase in the maximum PIC temperature with the introduction of TGVs under the EICs due to a small increase in thermal crosstalk. However, when comparing **Figure 6.2** and **Figure 6.4**, the decrease in the maximum EIC temperature with the introduction of TGVs and copper clip is 15% and 26% respectively. Thus, the heat dissipation from the EIC is more effective in the case of copper clip on top of the EIC as compared to the TGVs under the EIC. This underpins the importance of investigating this primary heat flow path (copper clip) in addition to the secondary heat flow (TGVs). The maximum PIC temperature increases by 1.2% and decreases by 7% with the introduction of TGVs and copper clip respectively. The decrease in the PIC temperature with the introduction of the copper clip is because of heat spreading from the top of the EIC and lowering the thermal crosstalk between the EIC and PIC.

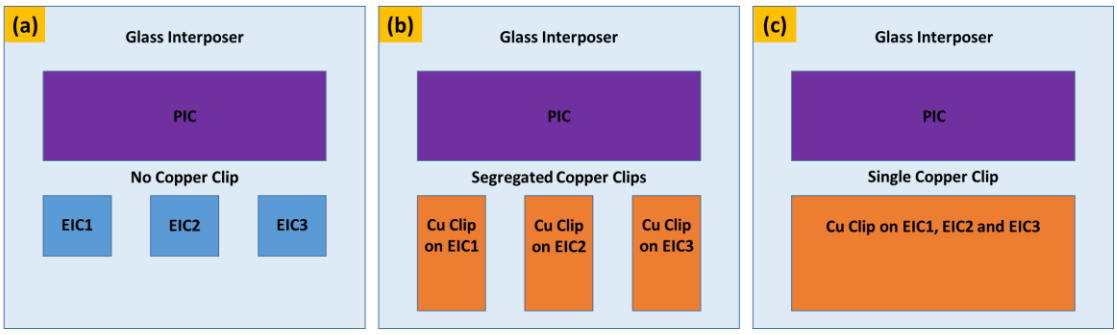


Figure 6.3: Top view schematic showing co-packaged electronic chips (EIC1, EIC2 and EIC3) and photonic chip (PIC) when there is (a) no copper clip in the assembly, (b) segregated copper clips which denotes separate copper clip on each EIC and (c) single copper clip which covers all the three EICs.

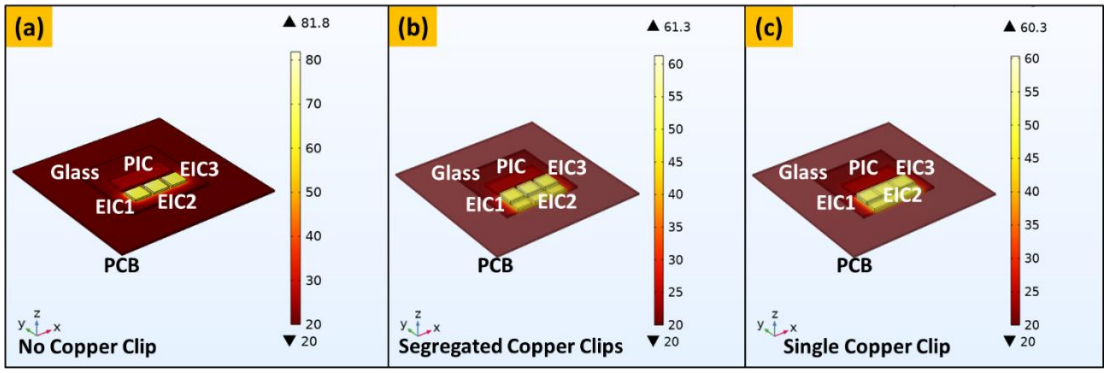


Figure 6.4: Simulation results of the FEM simulation showing the maximum temperature of the co-packaged EICs and PIC with (a) no copper clip, (b) segregated copper clips and (c) single copper clip. The segregated copper clips allow for individual copper clips to be attached to the different EICs and the single copper clip allows for a single copper clip which is larger in size to be attached to the EICs.

Table 6.4: Maximum temperature of the EICs (EIC1, EIC2 and EIC3) and PIC derived from the FEM simulation with no copper clip, segregated copper clips and single copper clip attached on top of the EICs. Note that in these cases, there are no TGVs in the glass interposer under the EICs.

Component	No Copper Clip Maximum Temperature (˚C)	Segregated Copper Clips Maximum Temperature (˚C)	Single Copper Clip Maximum Temperature (˚C)
EIC1	79.25	59.29	60.32
EIC2	81.82	61.30	59.21
EIC3	79.15	59.27	58.41
PIC	25.45	23.71	23.64

There are two types of copper clips which are analyzed to remove heat from the electronic chip's topside. The first type is segregated copper clips, which are separate copper clips for each EIC and the second type involves a single copper clip attached over all three EICs (EIC1, EIC2 and EIC3). A thermal interface material (TIM) is used to connect the chips' topside to the copper clip; the cross-section is shown in **Figure 6.5**. The active surface (or heat-generating surface) on the chip is in close proximity to the microbumps as the chip is flip-chip attached to the glass interposer. The hotspots are located at the corners of EIC1, EIC2, EIC3 and are powered with heat fluxes of 1 W/mm^2 each.

As seen in **Figure 6.4**, the copper clip redistributes the heat across the copper surface, which brings down the temperature of the EIC and the PIC. The single copper clip acts marginally better than the segregated copper clips due to the additional copper clip surface area for thermal spreading.

6.3 Parametric study of components

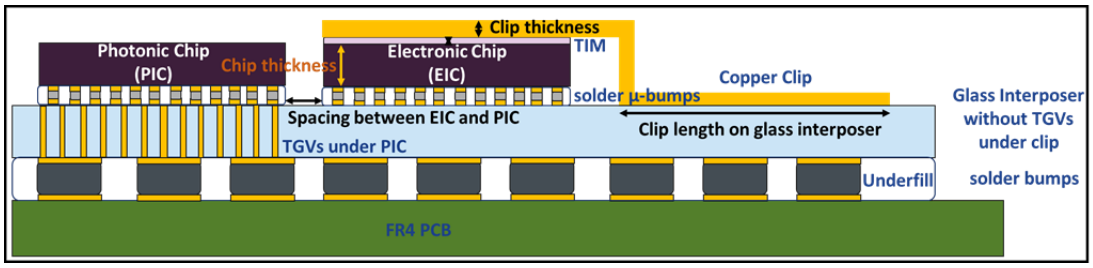


Figure 6.5: Side view schematic of the co-packaged EIC and PIC with copper clip attached on top of the flip-chip bonded EIC. The schematic shows the various components (such as EIC chip thickness, spacing between EIC and PIC, TIM thickness, copper clip thickness and length of the copper clip on the glass interposer) in the primary heat flow path which are parametrically studied in section 6.3.

6.3.1 Impact of Electronic Chip Thickness

The effect of electronic chip thickness variation on the maximum EIC and PIC temperature is studied across three cases, namely when there is no copper, segregated copper clips and single copper clip attached to the topside of the EICs. When the thickness of electronic chips (EIC1, EIC2, and EIC3) increases from 100 μm to 500 μm, the maximum temperature of the electronic chip decreases by approximately 32% in the absence of a copper clip. This decrease is attributed to the increased volume of the silicon chip (as shown in **Figure 6.6(a)**). The elevated temperature of thinner electronic chips results from the existence of only the secondary heat conduction path through the glass and PCB, both of which exhibit low thermal conductivities.

Compared to the chip without a copper clip, attaching a copper clip on top of the EICs (both in the case of segregated copper clips and a single copper clip) results in approximately a 24% decrease in the maximum temperature of the EIC and a 6.5% decrease in the maximum temperature of the PIC (in cases where the chip thickness is 500 μm). The copper clip provides an additional heat conduction and spreading path from the topside of the electronic chips, leading to reduced thermal crosstalk with the PIC as well (as shown in **Figure 6.6(b)**). The decrease in maximum chip temperature

of the PIC is lower than that of the EIC due to the low lateral thermal crosstalk between EIC and PIC, attributed to the low thermal conductivity of the glass interposer.

The presence of a copper clip mitigates the variation in maximum temperature as the electronic chip thickness (ranging from 100 µm to 500 µm) increases for both EIC (Electronic Integrated Circuit) and PIC (Photonic Integrated Circuit). Specifically, the variation decreases from 32% and 4.6% to 2.37% and 0.21% for EIC and PIC, respectively.

When comparing the use of a single copper clip to segregated copper clips, there are some interesting observations:

- The maximum temperature of EICs and PIC is marginally reduced (by a maximum of 1°C) with a single copper clip due to its larger surface area (as seen in **Figure 6.6 (b)** and **(c)**).
- However, EIC 2 experiences the highest temperature when using segregated copper clips (or no copper clip), while EIC 1 exhibits the highest temperature with a single copper clip. This behavior is attributed to the hotspot position at the corners of EICs and thermal crosstalk through the glass interposer between EIC1, EIC2, and EIC3.
- In the case of segregated copper clips (and no copper clip), thermal crosstalk increases the temperature of the middle chip (EIC2).
- Interestingly, the maximum temperatures of EIC1 and EIC3 are similar when using no copper clip or segregated copper clips.
- However, with a single copper clip, the additional heat flow path provided by the clip helps dissipate heat from the electronic chips. The hotspot located at the corner of EIC1 lacks sufficient heat spreading, leading to its elevated temperature.

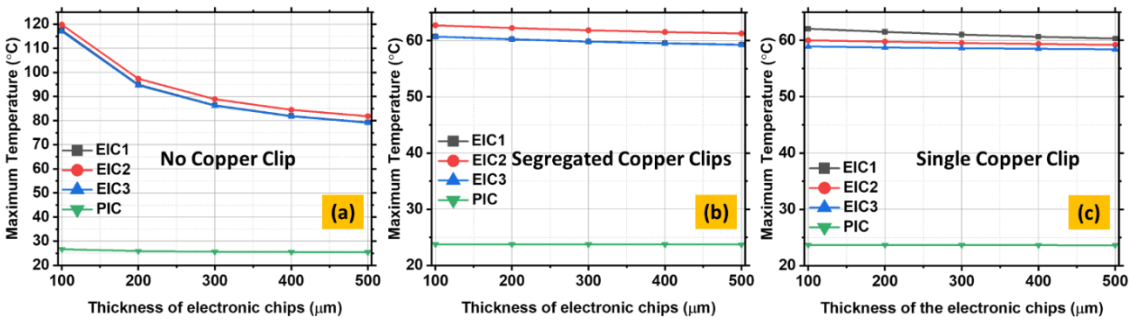


Figure 6.6: Maximum temperature of the EICs (EIC1, EIC2, EIC3) and PIC with varying thickness of the electronic chips in case of (a) no copper clip, (b) segregated copper clips and (c) single copper clip. The increase in EIC thickness reduces the EIC and PIC temperature because of the increased chip volume for thermal spreading.

6.3.2 Impact of Spacing between EIC and PIC

The effect of increasing the spacing between the Electronic Integrated Circuits (EICs) and Photonic Integrated Circuit (PIC) from 100 μm to 1000 μm on their maximum temperatures is analyzed across three scenarios: no copper clip, segregated copper clips, and a single copper clip. The observed trend is as follows:

- As the distance between EIC and PIC increases, the EIC temperature rises, while the PIC temperature decreases.
    - This behavior can be attributed to the diminishing thermal crosstalk between the thermally active EICs and the thermally passive PIC.

When considering the impact of spacing between Electronic Integrated Circuits (EICs) and Photonic Integrated Circuit (PIC), we observe the following changes in maximum chip temperatures:

- No Copper Clip:
    - EIC temperature increase: Approximately 7°C
    - PIC temperature decrease: Approximately 7.5°C
- Segregated Copper Clips:
    - EIC temperature increase: Approximately 3°C
    - PIC temperature decrease: Approximately 5.4°C
- Single Copper Clip:
    - EIC temperature increase: Approximately 2.8°C
    - PIC temperature decrease: Approximately 5.4°C

Notably, the presence of a copper clip significantly reduces the variation in EIC temperature. The copper clip facilitates better heat spreading (as shown in **Figure 6.7(b)**). Additionally, introducing the copper clip lowers the thermal crosstalk between electronic and photonic chips, resulting in improved PIC temperature stability.

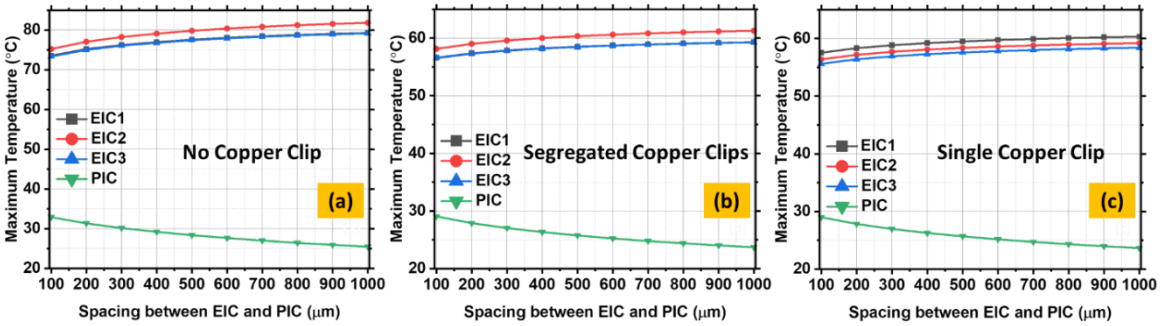


Figure 6.7: Maximum temperature of the EICs (EIC1, EIC2, EIC3) and PIC with varying spacing between electronic and photonic chips in case of (a) no copper clip, (b) segregated copper clips and (c) single copper clip. The increase in spacing between the EIC and PIC leads to an increase in the EIC temperature and a decrease in the PIC temperature due to lowered thermal crosstalk.

6.3.3 Impact of TIM Thickness

The thermal interface material (TIM) serves as the contact point between the topside of electronic chips and the copper clip. When the TIM thickness increases from 25 μm to 100 μm, it results in higher thermal resistance between the electronic chips and the copper clip. Consequently, we observe a small increase (approximately 1°C) in the maximum temperature of the electronic chips.

Interestingly, when comparing the use of a single copper clip to segregated copper clips:

- The maximum temperature of the Electronic Integrated Circuit (EIC) decreases with a single copper clip (**Figure 6.8(b)**) compared to segregated copper clips (**Figure 6.8 (a)**. This improvement is due to the additional clip area, which facilitates better heat spreading and lowers the EIC temperature.
- However, the change in Photonic Integrated Circuit (PIC) temperature with increasing TIM thickness is minimal (approximately 0.02°C).

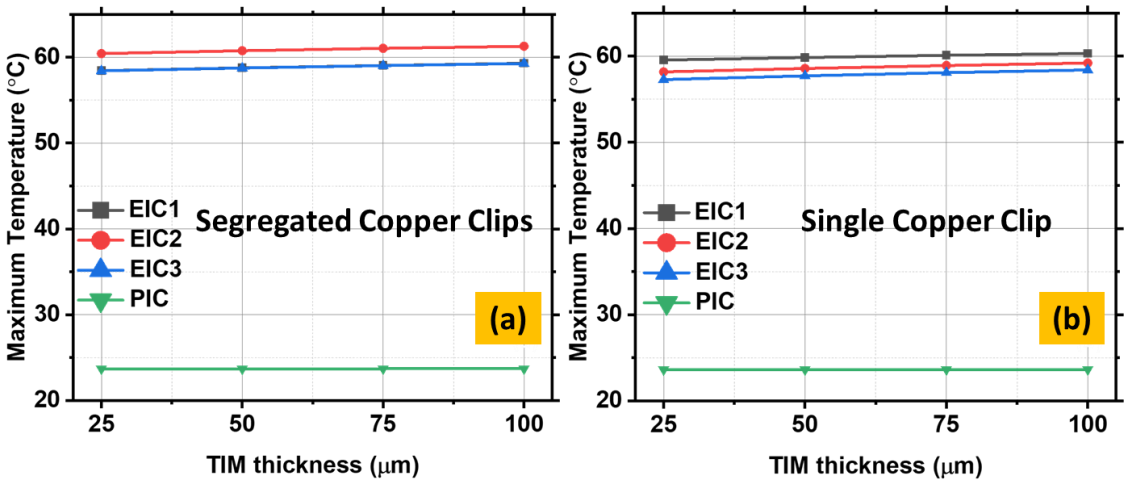


Figure 6.8: Maximum temperature of the EICs (EIC1, EIC2, EIC3) and PIC with varying TIM thickness in case of (a) segregated copper clips and (b) single copper clip. The increase in TIM thickness leads to an increase in the EIC temperature and minimal change in the PIC temperature respectively. It is explained due to the thermal resistance offered by the TIM and low lateral thermal conduction between EIC and PIC on glass interposer respectively.

6.3.4 Impact of Copper Clip Thickness

As the thickness of the copper clip increases, it facilitates better heat spreading from the chip to the outer surface of the copper clip, promoting natural convective cooling. This additional thickness contributes to both the cooling volume and the surface area in contact with the surrounding air.

Here the specific observations for different copper clip thicknesses:

- Segregated Copper Clips (**Figure 6.9 (a)**):
    - The maximum temperature of the Electronic Integrated Circuit (EIC) decreases by approximately 12.5% when the copper clip thickness increases from 50 µm to 800 µm.
    - The maximum temperature of the Photonic Integrated Circuit (PIC) decreases by approximately 2.5% for the same thickness range.
- Single Copper Clip (**Figure 6.9 (b)**):
    - In the case of a single copper clip, the maximum EIC temperature decreases by approximately 14% when the copper clip thickness increases from 50 µm to 800 µm.
    - Similarly, the maximum PIC temperature decreases by approximately 2.7% within the same thickness range.

Interestingly, the smaller decrease in maximum PIC temperature is primarily due to the low thermal crosstalk between electronic and photonic chips on the glass interposer. As the single copper clip's thickness increases, it effectively spreads heat across all three electronic chips (EIC1, EIC2, and EIC3), leading to their temperatures converging toward the same value.

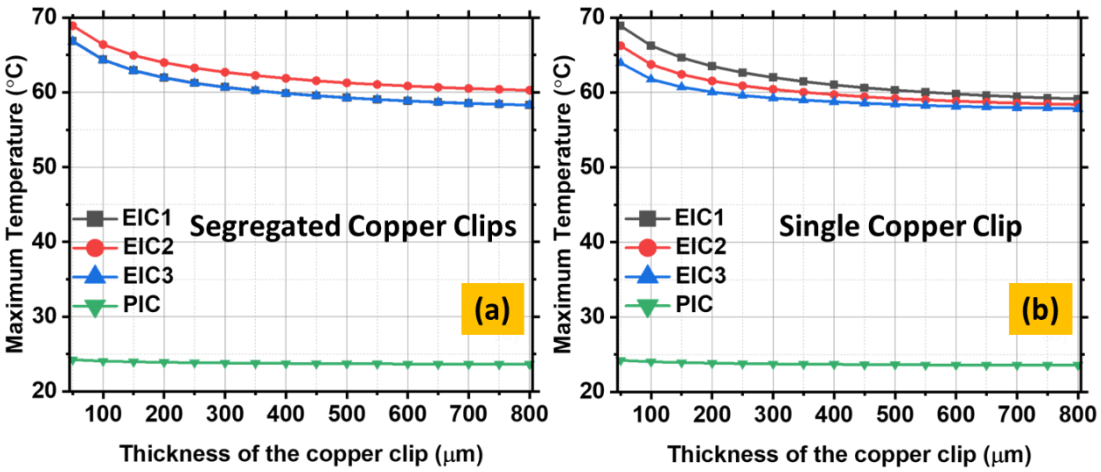


Figure 6.9: Maximum temperature of the EICs (EIC1, EIC2, EIC3) and PIC with varying copper clip thickness in case of (a) segregated copper clips and (b) single copper clip. The increase in copper clip thickness leads to a decrease in the maximum temperature of EIC and PIC due to improved conduction and heat spreading with increased clip thickness.

6.3.5 Impact of Copper Clip Length

In this section, we examine the impact of varying the length of the copper clip on the glass interposer on the maximum temperature of the Electronic Integrated Circuits (EICs) and Photonic Integrated Circuit (PIC).

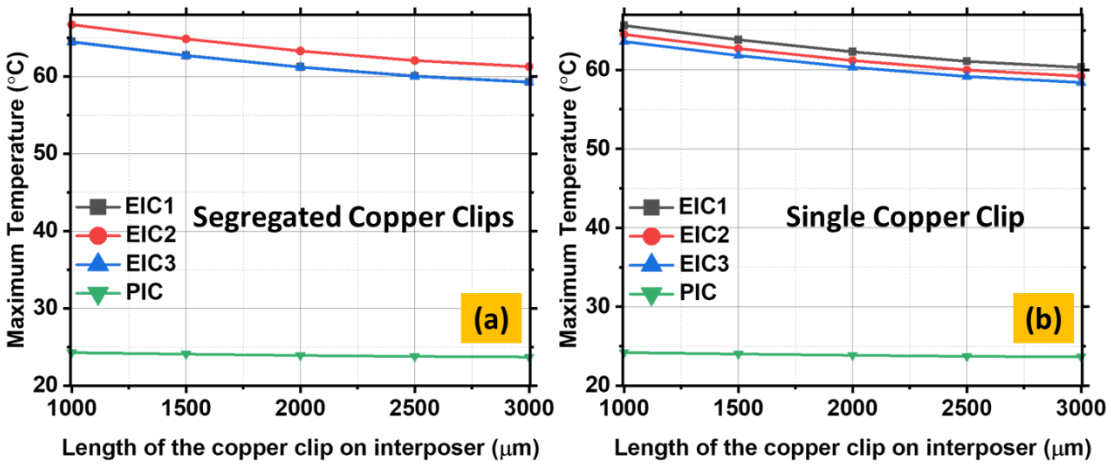


Figure 6.10: Maximum temperature of the EICs (EIC1, EIC2, EIC3) and PIC with varying copper clip length in case of (a) segregated copper clips and (b) single copper clip. The increase in copper clip length on the glass interposer leads to a decrease in the maximum temperature of EIC and PIC as it allows larger area for heat spreading.

- Segregated Copper Clips (**Figure 6.10 (a)**):
  - The maximum EIC temperature decreases by approximately 8.1% when the length of the copper clip increases from 1 mm to 3 mm.
  - The maximum PIC temperature experiences a marginal decrease of about 2.34% within the same length range.
- Single Copper Clip (**Figure 6.10 (b)**):
  - With a single copper clip, the maximum EIC temperature decreases by approximately 8.09% for the same length variation.
  - Similarly, the maximum PIC temperature decreases by approximately 2.31%.

The cooling performance of the copper clips remains consistent whether using segregated or single copper clips. Notably, the single copper clip provides an additional decrease of approximately 1°C in maximum temperature due to its larger copper surface area. As observed previously, EIC2 still exhibits the highest temperature in the case of segregated copper clips due to thermal crosstalk from EIC1 and EIC3. Conversely, EIC1 shows the highest temperature with a single copper clip, attributed to the hotspot position at the corner of the chip.

6.4 Requirement of a heat sink

6.4.1 TGVs under Copper Clip

In this study, we introduce TGVs under the copper clip in **Figure 6.11**. The temperature analysis is as follows:

- EICs: These experience a significant reduction in maximum temperature (approximately 4°C) when TGVs are introduced.
- PIC: The maximum PIC temperature decreases marginally by 1°C due to effective heat spreading from the copper clip and TGVs.

Notably, transitioning from segregated copper clips to a single copper clip leads to a minimal increase (0.5°C) in PIC temperature (**Table 6.5**). This increase is attributed to thermal crosstalk resulting from the incorporation of additional TGVs under the single copper clip.

The accommodation of TGVs under the copper clip can locally enhance the thermal pathway for heat conduction through the glass interposer.

To further improve this thermal pathway, the different components attached to the electronic chip for the topside heat removal are optimized. These components are the TIM, TGVs, solder bumps between the glass interposer and PCB. Note that the TGVs mentioned here refer to the TGVs under the copper clip in the glass interposer and the bumps mentioned here are specifically the solder bumps contacting the TGVs under the copper clip and PCB. The TGVs under the PIC remain the same as those in Section 6.2. The TIM thickness and the copper clip thickness are kept constant at 100µm and 500µm respectively. The area of the copper clip also remains the same as specified in **Table 6.1**. The effective out-of-plane thermal conductivity of the TIM, TGVs, and bumps between the glass interposer and PCB varied from 1.2 W/m.K to 400 W/m.K for the segregated copper clips (**Figure 6.12**) and single copper clip (**Figure 6.13**). The area of TGVs and solder bumps with changing effective out-of-plane thermal conductivity is kept the same as that of the copper clip on the top of the glass interposer surface for simplification. Similarly, the area of the TIM with changing effective out-of-plane thermal conductivity is kept the same as that of the chip.

Figure 6.12 and **Figure 6.13** show that the change in out-of-plane effective thermal conductivity of the TIM exerts the maximum impact on the thermal performance of

the EICs. However, the impact of variation in the effective out-of-plane thermal conductivity of the bumps between the glass interposer and PCB is the least on EICs. The maximum impact of the TIM is explained due to the close contact between the topside of the electronic chip and the copper clip. The minimum impact of the bumps is explained due to the lower effective volume of the bumps as compared to TGVs. As seen through **Figure 6.14**, when the interposer height (and TGV height) decreases from 460µm to 110µm, the impact of change in effective thermal conductivity of bumps overpowers that of the TGVs. This is because the effective volume of the bumps is higher as compared to the effective volume of the TGVs when the interposer height is reduced to 110µm. Similarly, the change in effective out-of-plane thermal conductivity of the TGVs overpowers that of TIM and bumps in terms of its effect on the change in the maximum temperature of the PIC; when the interposer height is increased from 110µm to 460µm (**Figure 6.15**).

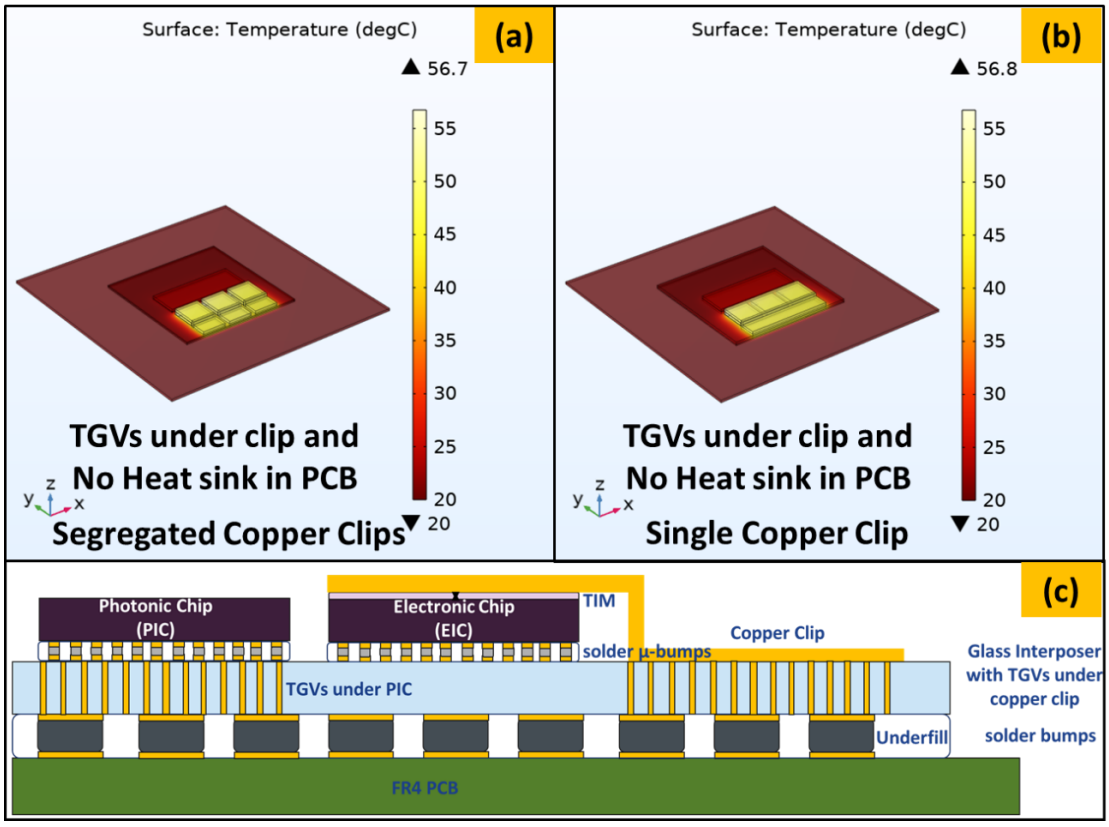


Figure 6.11: Simulation results of the FEM simulation showing the maximum temperature of the co-packaged EICs and PIC with (a) segregated copper clips and (b) single copper clip with TGVs in glass interposer under the clip length on the interposer as seen through the schematic (c).

Table 6.5: Maximum temperature of the EICs (EIC1, EIC2 and EIC3) and PIC derived from the FEM simulation with segregated copper clips and single copper clip attached on top of the EICs with TGVs in the glass interposer under the clip length on the interposer

Component	Segregated Copper Clips Maximum Temperature (˚C)	Single Copper Clip Maximum Temperature (˚C)
EIC1	55.05	56.75
EIC2	56.72	55.49
EIC3	55.04	54.60
PIC	22.82	23.32

This is because the TGVs under the copper clip allow for heat conduction through the glass interposer and hence influence thermal crosstalk with the PIC. As the interposer height is decreased from 460µm to 110µm, the impact of change in effective out-of-plane thermal conductivity of the bumps overtakes that of the TIM and TGVs. The increased effective volume of the bumps as compared to the TGVs and TIM is an explanation for this phenomenon. Hence, the effective volume through which heat conduction takes place plays an essential role in determining the component that makes the maximum impact on heat dissipation through glass interposer-based packages.

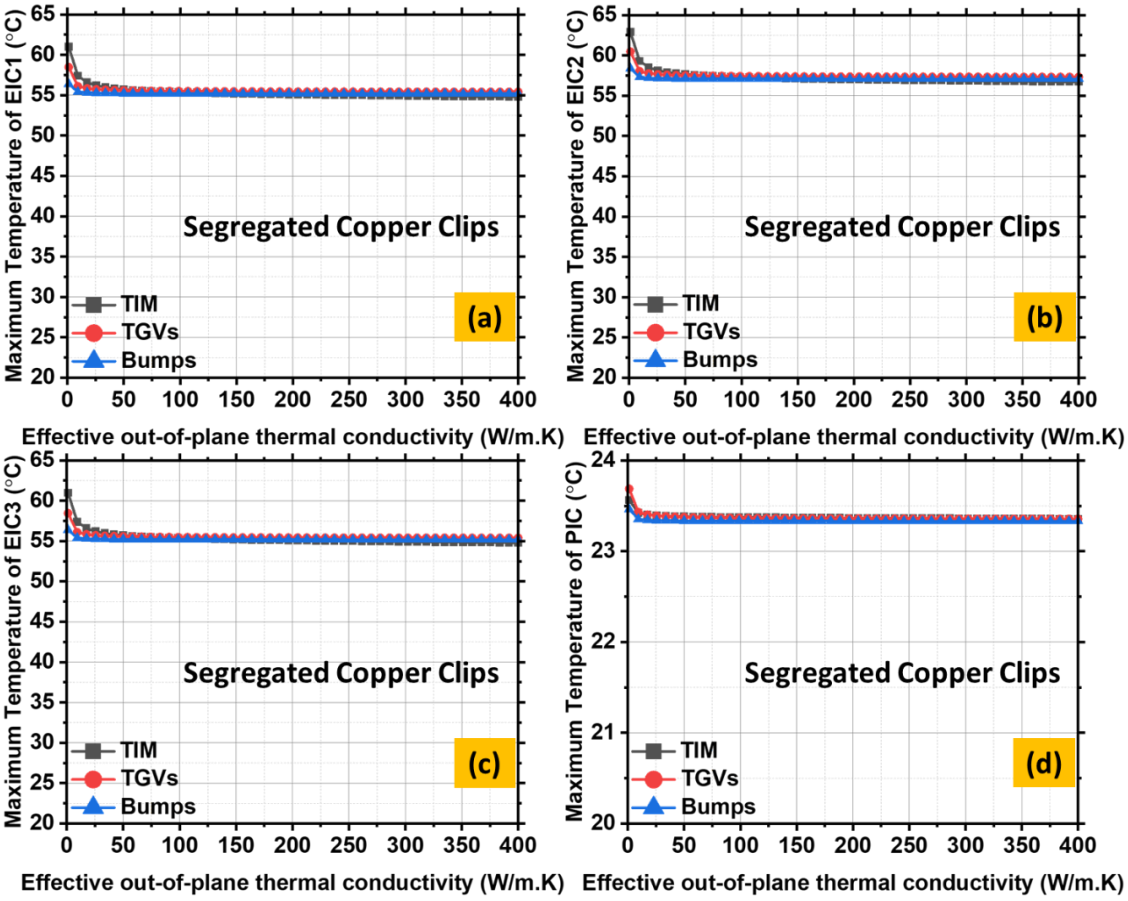


Figure 6.12: Variation in the maximum temperature of (a) EIC1, (b) EIC2, (c) EIC3 and (d) PIC with change in effective out-of-plane thermal conductivity (1.2 W/m.K-400 W/m.K) of the TIM, TGVs under the copper clip and bumps between the TGVs in glass interposer and PCB. This figure represents the case with segregated copper clips and the impact of change in thermal conductivity is studied through the magnitude of change in temperature of the chips.

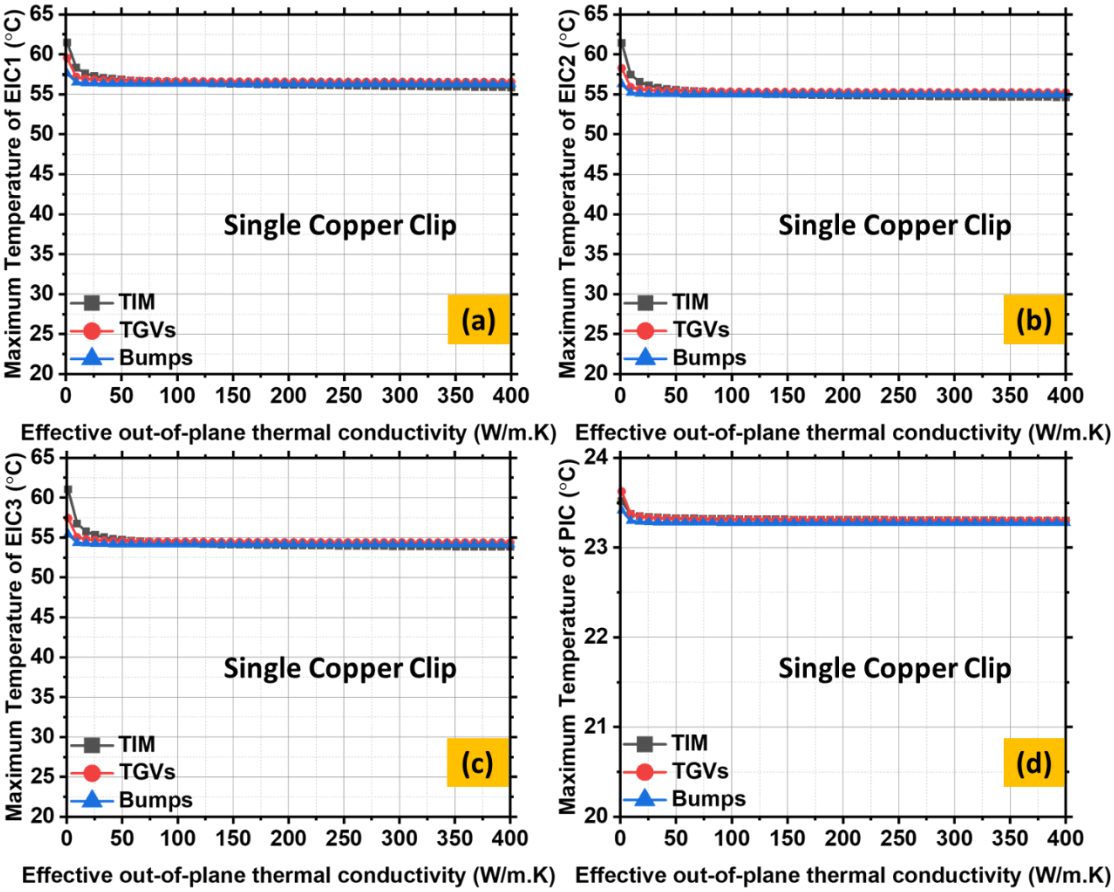


Figure 6.13: Variation in the maximum temperature of (a) EIC1, (b) EIC2, (c) EIC3 and (d) PIC with change in effective out-of-plane thermal conductivity (1.2 W/m.K-400 W/m.K) of the TIM, TGVs under the copper clip and bumps between the TGVs in glass interposer and PCB. This figure represents the case with single copper clip and the impact of change in thermal conductivity is studied through the magnitude of change in temperature of the chips.

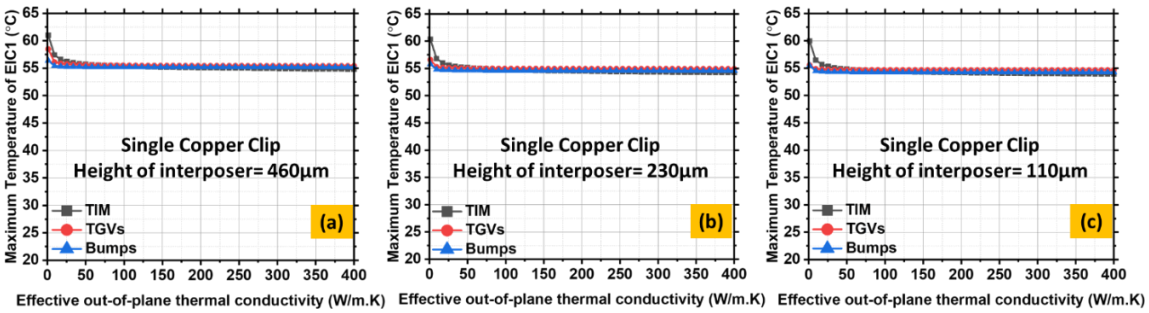


Figure 6.14: Variation in the maximum temperature of EIC1 with change in effective out-of-plane thermal conductivity (1.2W/m.K - 400 W/m.K) of TIM, TGVs under the copper clip and bumps between the TGVs in glass interposer and PCB, when the interposer (and TGV) height is (a) 460µm, (b) 230µm and (c) 110µm. Note that TIM remains the dominant impact factor across (a), (b) and (c) but the impact of TGVs is overshadowed by the bumps as the interposer height is decreased. Additionally, the EIC temperature decreases with the decrease in interposer height due to lowering thermal resistance.

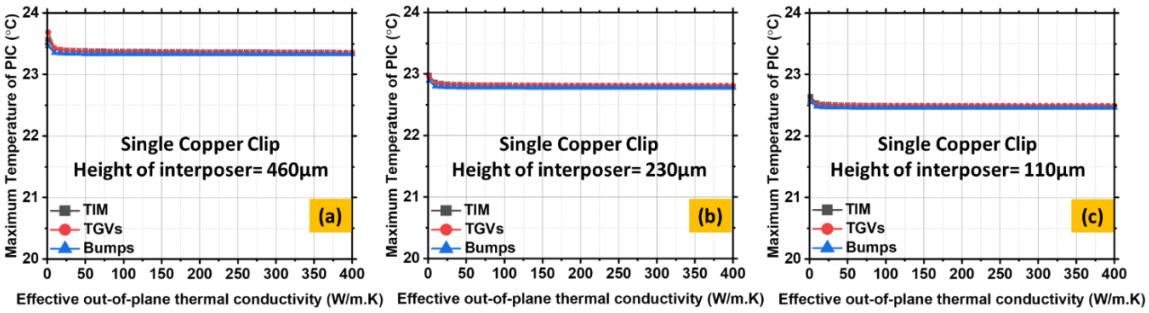


Figure 6.15: Variation in the maximum temperature of PIC with change in effective out-of-plane thermal conductivity (1.2 W/m.K - 400 W/m.K) of TIM, TGVs under the copper clip and bumps between the TGVs in glass interposer and PCB, when the interposer (and TGV) height is (a) 460µm, (b) 230µm and (c) 110µm. Note that the impact of TGVs is overshadowed by the bumps as the interposer height is decreased. Additionally, the PIC temperature decreases with the decrease in interposer height due to lowering thermal resistance (with presence of TGVs under PIC for heat conduction).

6.4.2 Heat Sink integrated in PCB

Considering the effective volume as a dominating factor for heat dissipation in glass packages, PCB in the package is the component with the highest effective volume and the lowest thermal conductivity (0.3 W/m.K). The thermal conduction through the PCB needs to be locally improved (under copper clip region) to improve the thermal pathway consisting of different components attached to the electronic chip for topside heat removal (TIM, TGVs, bumps and PCB). This is done through the addition of a heat sink in the PCB (**Figure 6.16**).

Note that the TGVs mentioned here refer to the TGVs under the copper clip in the glass interposer and the bumps here specifically refer to the solder bumps contacting the TGVs under the copper clip and heat sink in the PCB. The impact of the addition of a heat sink in the PCB is studied through a simulation model where the effective out-of-plane thermal conductivity of the TIM, TGVs, bumps and heat sink in PCB is varied from 1.2 W/m.K to 400 W/m.K for the segregated copper clips (**Figure 6.17**) and single copper clip (**Figure 6.18**). The TGVs under the PIC remain the same as that in Section 6.2. The area of TGVs, solder bumps and heat sink in PCB is kept the same as that of the copper clip on the top of the glass interposer surface for simplification. The TIM thickness and the copper clip thickness are kept constant at 100µm and 500µm respectively. The area of the copper clip also remains the same as specified in **Table 6.1**.

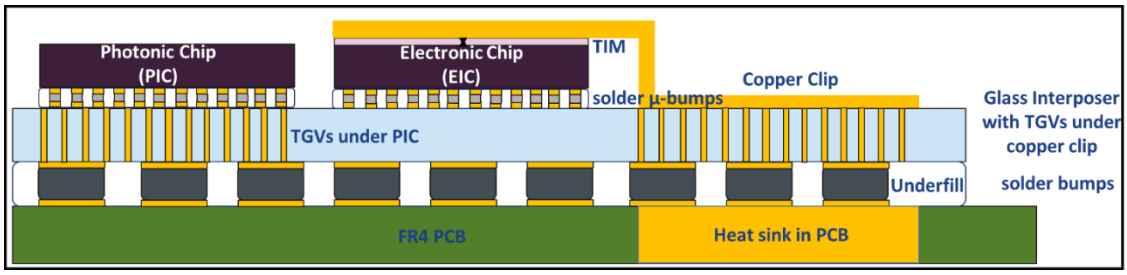


Figure 6.16: Side view schematic of the co-packaged EIC and PIC with a copper clip attached on top of the flip-chip bonded EIC and TGVs are present under the copper clip. In addition to this, there is a heat sink integrated into the PCB region under the copper clip for effective heat dissipation.

The variation in maximum temperature of EIC1, EIC2, EIC3 and PIC with the change in the effective out-of-plane thermal conductivity of TIM, TGVs, bumps and heat sink in PCB is simulated for both segregated copper clips and single copper clip in **Figure 6.17** and **Figure 6.18** respectively. From both these figures, the maximum surface temperature of the EICs and PIC is slightly lowered (by a maximum of 2-3ºC) in the case of a single copper clip as compared to the case of segregated copper clips because of the presence of a larger surface area for heat dissipation.

From **Figure 6.17** and **Figure 6.18**, it is also clear that the order of impact of varying effective-out-of-plane thermal conductivity of the different components (TIM, TGVs under copper clip, bumps between glass interposer and heat sink in PCB, heat sink in PCB) on the temperature of EIC follows the order of: Heat Sink>TIM>TGVs>Bumps.

This trend can be explained due to the high effective volume and high thermal conductivity offered by the heat sink in PCB for effective heat dissipation from the EICs. The TIM is in close thermal contact with the EICs; hence the thermal conductivity of the TIM should be increased. The TGVs and bumps provide a thermal pathway for the heat spread away from the EICs to be conducted to the heat sink in the PCB. Similarly, the PIC temperature's dependence on the varying effective-out-of-plane thermal conductivity of the different components follows the order of Heat Sink>TGVs>TIM>Bumps. The thermal conductivity of TGVs under the copper clip plays a larger role than the thermal conductivity of TIM (between the top of the EIC and copper clip) and bumps in affecting the temperature of the PIC. This is because the effective volume of TGVs (greater height) under the copper clip outweighs the effective volume of bumps and TIM involved in the thermal dissipation of heat generated by the electronic chips.

From the above discussion, the incorporation of a heat sink in PCB (for contacting the constant cold temperature/sink temperature of 20ºC on the backside of the PCB) hence becomes essential for improved heat dissipation in electronic chips (approximately 5ºC difference in maximum chip temperature) and photonic chip (approximately 1-1.5ºC difference in maximum chip temperature).

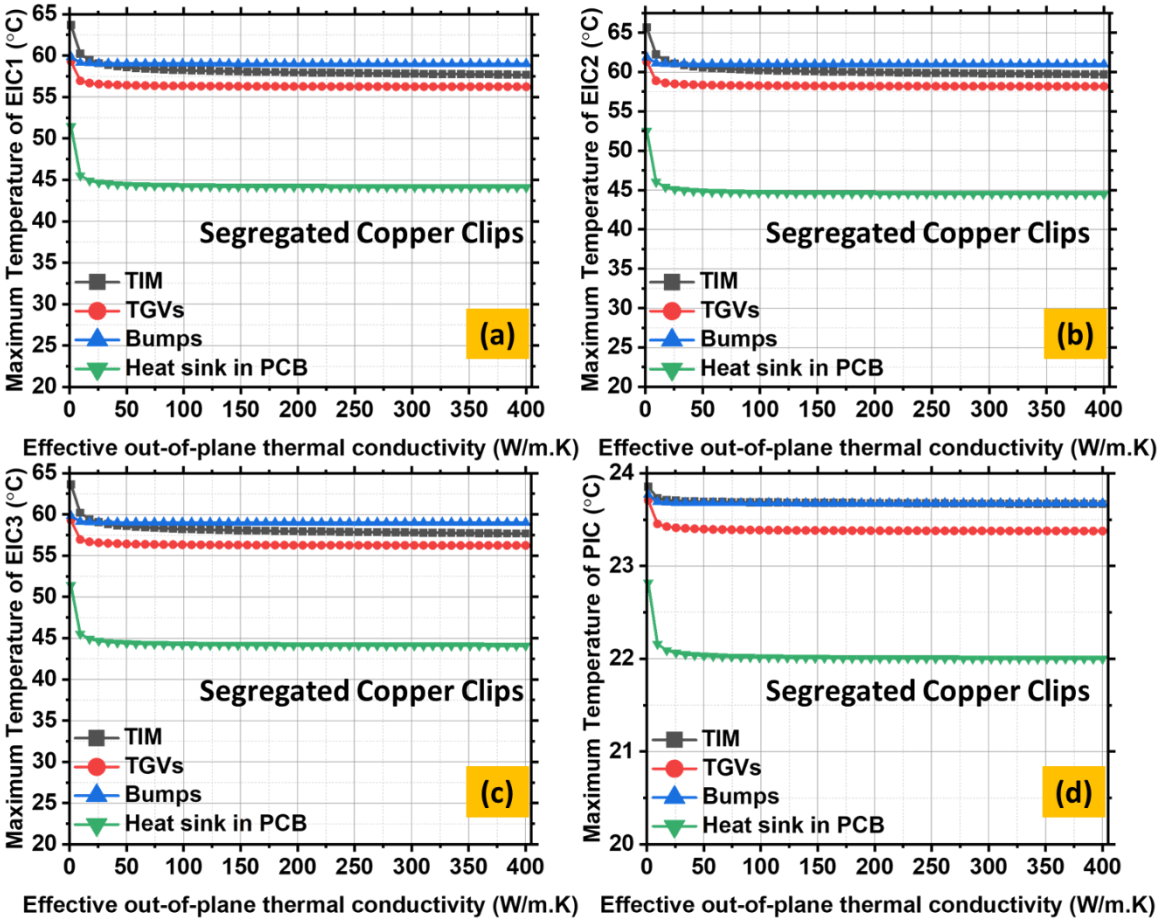


Figure 6.17: Variation in the maximum temperature of (a) EIC1, (b) EIC2, (c) EIC3 and (d) PIC with change in effective out-of-plane thermal conductivity (1.2W/m.K-400 W/m.K) of the TIM, TGVs under the copper clip, bumps between the TGVs in glass interposer-PCB and heat sink embedded in PCB. This figure represents the case with segregated copper clips and the impact of change in thermal conductivity is studied through the magnitude of change in temperature of the chips.

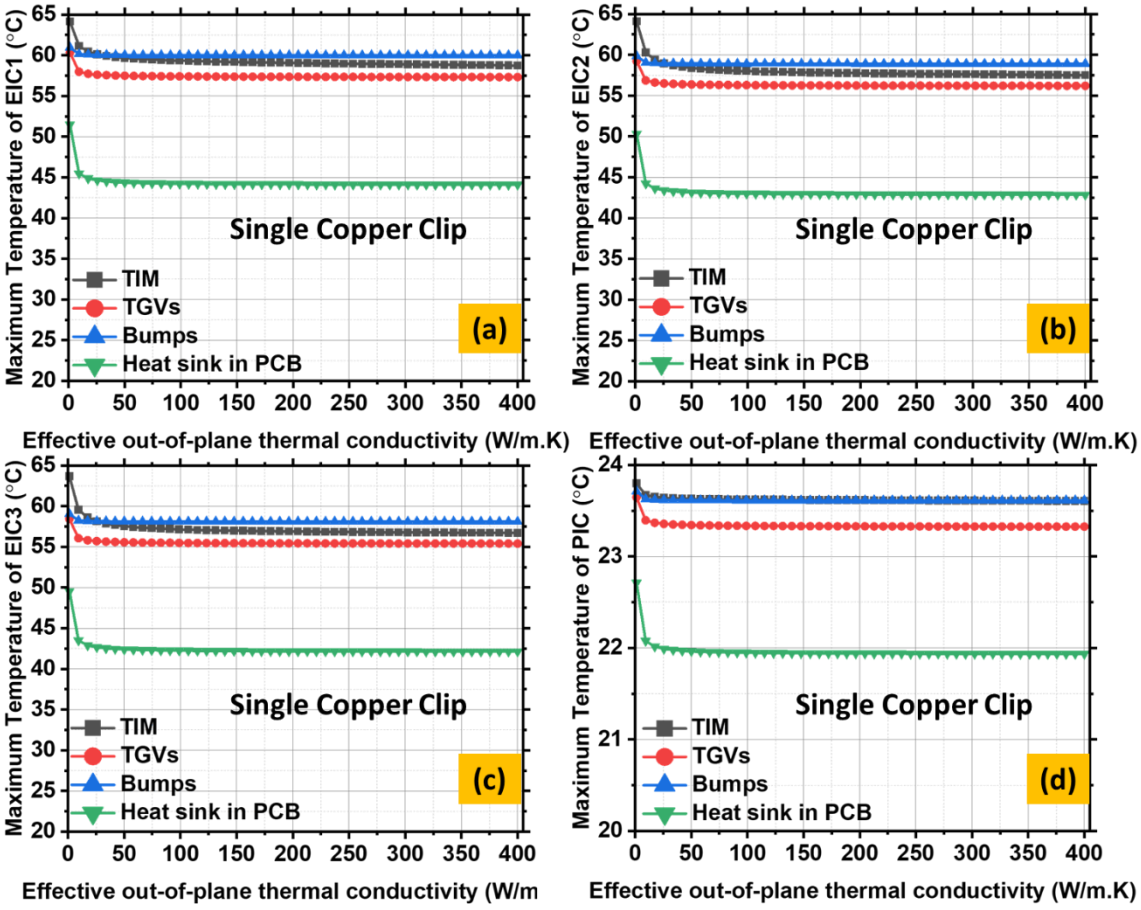


Figure 6.18: Variation in the maximum temperature of (a) EIC1, (b) EIC2, (c) EIC3 and (d) PIC with change in effective out-of-plane thermal conductivity (1.2W/m.K-400 W/m.K) of the TIM, TGVs under the copper clip, bumps between the TGVs in glass interposer-PCB and heat sink embedded in PCB. This figure represents the case with single copper clip and the impact of change in thermal conductivity is studied through the magnitude of change in temperature of the chips.

Based on the above discussion, further FEM simulations are conducted to see the impact of a copper heat sink integrated in the PCB in the case of segregated copper clips and a single copper clip, the thermal conductivities of the different materials used in the simulation are set as shown in **Table 6.6**.

Table 6.6: Effective in-plane and out-of-plane thermal conductivities of different components in the FEM simulation for segregated and single copper clip with heat sink integrated in the PCB in addition to the TGVs in the glass interposer under the copper clip area on the interposer.

Component	Effective in-plane thermal conductivity (k_x) (W/m.K)	Effective in-plane thermal conductivity (k_y) (W/m.K)	Effective out-of-plane thermal conductivity (k_z) (W/m.K)
PCB	0.3	0.3	0.3
Bumps	1.8	1.8	4
Interposer	1.2	1.2	1.2
Microbumps	2.8	2.8	4.4
EIC	130	130	130
PIC	130	130	130
Clip	380	380	380
TIM	57	57	57
TGVs under PIC	1.51	1.51	37.87
TGVs under copper clip	1.51	1.51	37.87
Heat sink in PCB	380	380	380

As seen in **Table 6.6**, the thermal conductivity of the TIM material is increased from 20 W/m.K (thermal grease) to 57 W/m.K (solder) as soldering the copper clip allows for a parallel clip attachment process and a higher thermal conduction between the top of the chip and copper clip interface. The thermal conductivity of the TGVs under the copper clip is kept the same as that under the PIC with the addition of a copper heat sink in the PCB. This direct thermal pathway leads to a significant decrease in the maximum temperatures of the electronic and photonic chips in the case of segregated copper clips and single copper clips as detailed in **Table 6.7**. As compared to **Figure 6.11**, the addition of a heat sink to the PCB has decreased the maximum temperature of the EICs by approximately 23ºC (**Figure 6.19**).

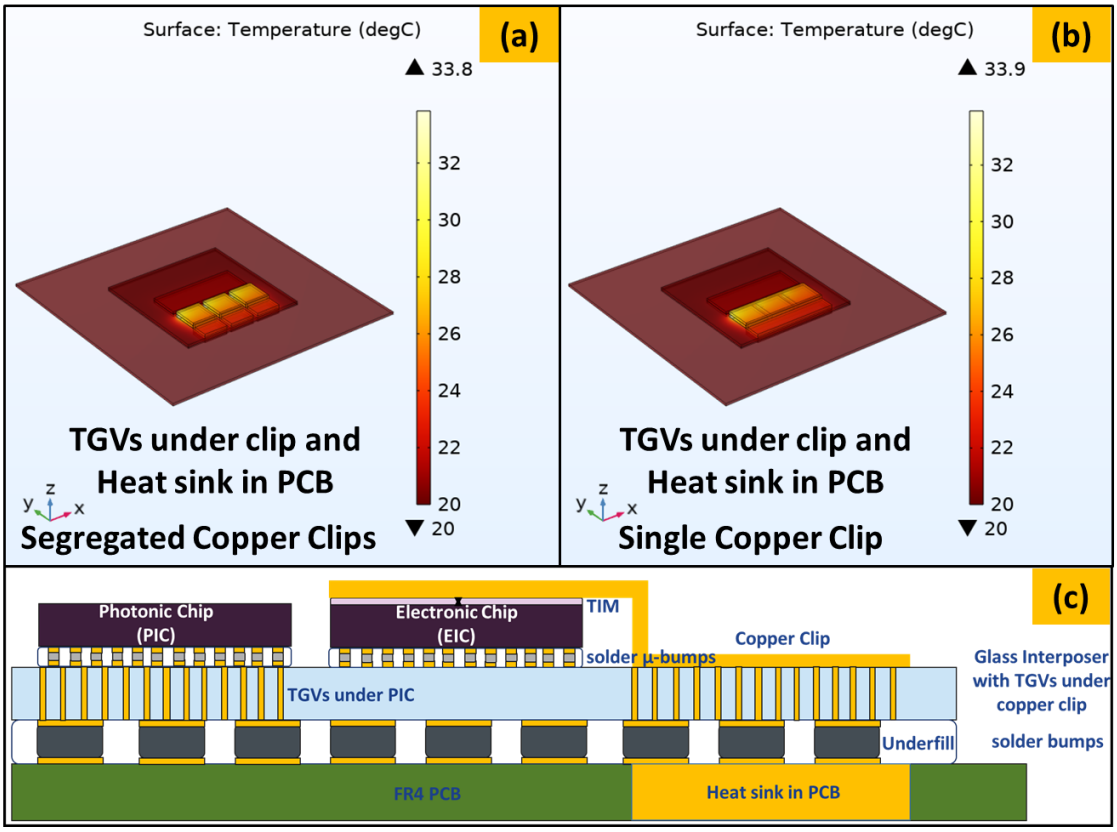


Figure 6.19: Simulation results of the FEM simulation showing the maximum temperature of the co-packaged EICs and PIC with (a) segregated copper clips and (b) single copper clip with heat sink embedded in the PCB as well as TGVs in glass interposer under the clip length on the interposer as seen through the schematic (c).

Table 6.7: Maximum temperature of the EICs (EIC1, EIC2 and EIC3) and PIC derived from the FEM simulation with segregated copper clips and single copper clip attached on top of the EICs with TGVs in the glass interposer under the clip length on the interposer and heat sink integrated in the PCB. The area of the heat sink in PCB is kept the same as the area of the copper clip on glass interposer

Component	Segregated Copper Clips Maximum Temperature (˚C)	Single Copper Clip Maximum Temperature (˚C)
EIC1	33.72	33.88
EIC2	33.80	32.44
EIC3	33.72	31.77
PIC	20.95	20.92

6.5 Extended Copper Clip

The integration of a heat sink into the PCB necessitates dedicated cavities within the PCB, specifically in a region beneath the glass interposer with TGVs. These cavities accommodate a metal sink or micro-thermoelectric cooler (micro-TEC). The purpose of this design is to establish an efficient thermal pathway, which includes the TIM, copper clip, TGVs, and the heat sink within the PCB. This pathway facilitates the dissipation of heat generated by electronic chips. However, achieving this in high-density interconnections poses challenges, as it restricts the available PCB area beneath the glass interposer. To address this, the proposed solution involves eliminating the TGVs from the thermal pathway and directly connecting the copper clip to the heat sink within the PCB. This modified approach, referred to as the "extended copper clip", allows the incorporation of the heat sink in a region farther away from the glass interposer. The structure of the extended copper clip is shown in **Figure 6.20**. The FEM simulations in **Figure 6.21(a)** and **Figure 6.21(b)** for extended segregated clips and single clip reveals its effective heat dissipation from the EICs in the package. The maximum temperature of the EICs and PIC are very similar for **Table 6.7** and **Table 6.8**. Notably, this approach directs the heat away from the electronic chips and can also be contacted directly with a cold plate (instead of a heat sink in the PCB) to couple the package and system-level cooling mechanisms.

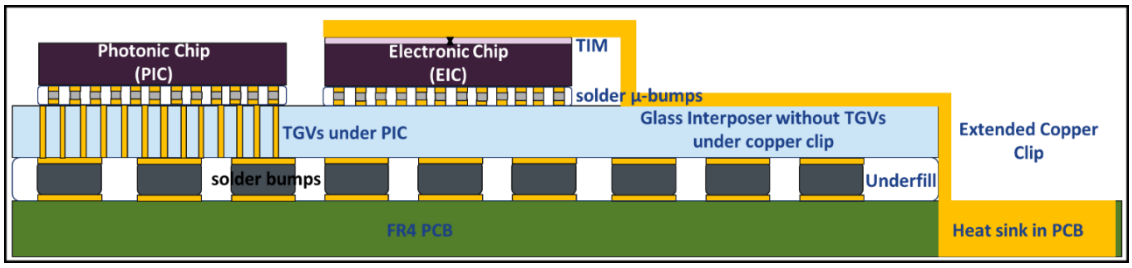


Figure 6.20: Side view schematic of the co-packaged EIC and PIC with copper clip attached on top of the flip-chip bonded EIC with no TGVs present under the copper clip. The length of the copper clip is extended towards the end of the interposer and is directly attached to the heat sink integrated in the PCB.

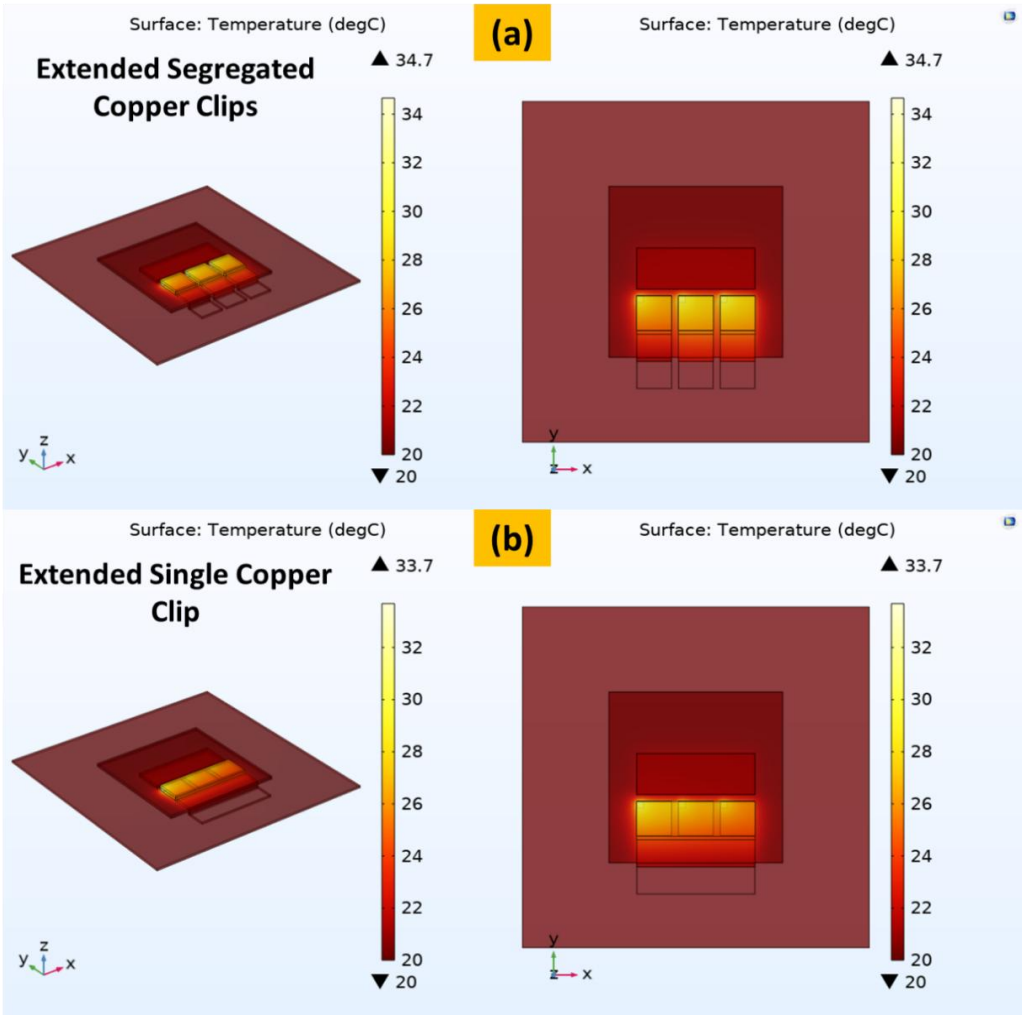


Figure 6.21: Simulation results of the FEM simulation showing the maximum temperature of the co-packaged EICs and PIC with (a) extended segregated copper clips and (b) extended single copper clip where the copper clip is extended to be directly attached to the heat sink in the PCB.

Table 6.8: Maximum temperature of the EICs (EIC1, EIC2 and EIC3) and PIC derived from the FEM simulation with extended segregated copper clips and extended single copper clip attached on top of the EICs. The length of the clip is extended over the surface of the glass interposer to be directly attached to the heat sink integrated in the PCB

Component	Segregated Copper Clips Maximum Temperature (˚C)	Single Copper Clip Maximum Temperature (˚C)
EIC1	33.54	33.65
EIC2	34.63	32.21
EIC3	34.56	31.54
PIC	20.99	20.90

In order to validate the concept of extended copper clip, an experiment is conducted with a reference thermal chip [6]. The reference thermal chip consists of heater loopbacks fabricated on silicon. The heater loopbacks act as hotspot sources on the chip [6]. The 525 µm thick silicon chip is bonded on a glass interposer using SnAgCu (SAC 305) solder bumps. This subassembly is then epoxy underfilled (EPOTEK 301-2) using capillary action, which is then cured at room temperature for 36 hours. Following the curing, this subassembly is then bonded on a copper plate using conductive silver epoxy (Chemtronics CW 2400). The copper plate acts as a heat sink in this case and is maintained at a constant temperature of 20ºC using a TEC. In order to supply power to the heater loopbacks on the flip-chip bonded reference thermal chip, the copper tracks on the glass interposer are fanned out and wire bonded to the PCB to enable DC connection. This assembly is shown in **Figure 6.22(a)** and is thermally characterized using an IR thermal microscope (FLIR X6540sc). Note that the glass interposer has no TGVs in this case.

The heat spreading in this assembly is also thermally characterized using copper clip and extended copper clip. The copper clip, as shown in **Figure 6.22(b)** is contacted on top of the flip-chip bonded reference thermal chip using a thermal grease (AiT COOL-GREASE ZXM). The copper clip spans uptil the surface of the glass interposer. The extended copper clip however, as shown in **Figure 6.22(c)** further spans onto the copper plate (or heat sink). The thickness of the copper clip and the thermal grease is approximately 440 µm and 100 µm respectively.

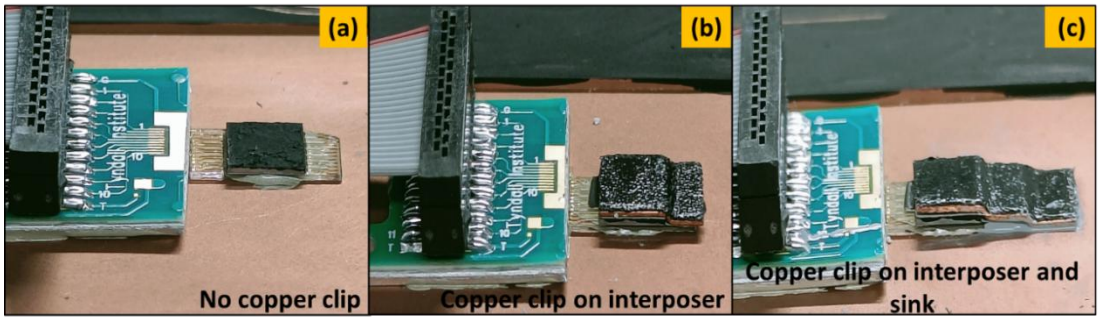


Figure 6.22: Characterization setup for infrared thermal measurement of (a) reference thermal chip on glass interposer, (b) reference thermal chip on glass interposer with copper clip attached on top of the flip-chip bonded chip (using thermal grease) and (c) reference thermal chip on glass interposer with an extended copper clip bonded on top of the chip (using thermal grease) and the extended copper clip is attached to the heat sink (copper plate maintained at 20ºC). Note that there are no TGVs in the glass interposer and the top surface of the chip, copper clip and extended copper clip are painted black to increase emissivity for infrared thermal measurement.

The thermal characterization of the three assemblies namely the assembly with no copper clip, with copper clip on the interposer and with copper clip on the interposer and extending onto the heat sink is shown in **Figure 6.23**. The schematic shows the infrared thermal image of the three assemblies and the maximum temperature profile along the heat-spreading region. In **Figure 6.23(a)**, a heater loopback is operated at increasing voltages which leads to an increase in the hotspot temperature. The position of the hotspot thus leads to a temperature peak in the area as detailed in the graph of **Figure 6.23(a)**. The introduction of a copper clip directs the heat concentrated at the hotspot region towards the glass interposer, as seen in **Figure 6.23(b)**. The graph in **Figure 6.23(b)** also demonstrates the uniformity in temperature across the copper clip. Lastly, the introduction of an extended copper clip, such that the copper clip contacts the glass interposer, and the copper plate (or heat sink) brings down the maximum temperature of the assembly significantly (as shown in **Figure 6.23(c)**). **Figure 6.24** shows the decrease in the junction temperature of the reference thermal chip, especially at higher powers with the introduction of a copper clip and extended copper clip. Note that the maximum measured temperature of the assembly is not very high in the previous case as the glass interposer subassembly is directly bonded to the copper plate.

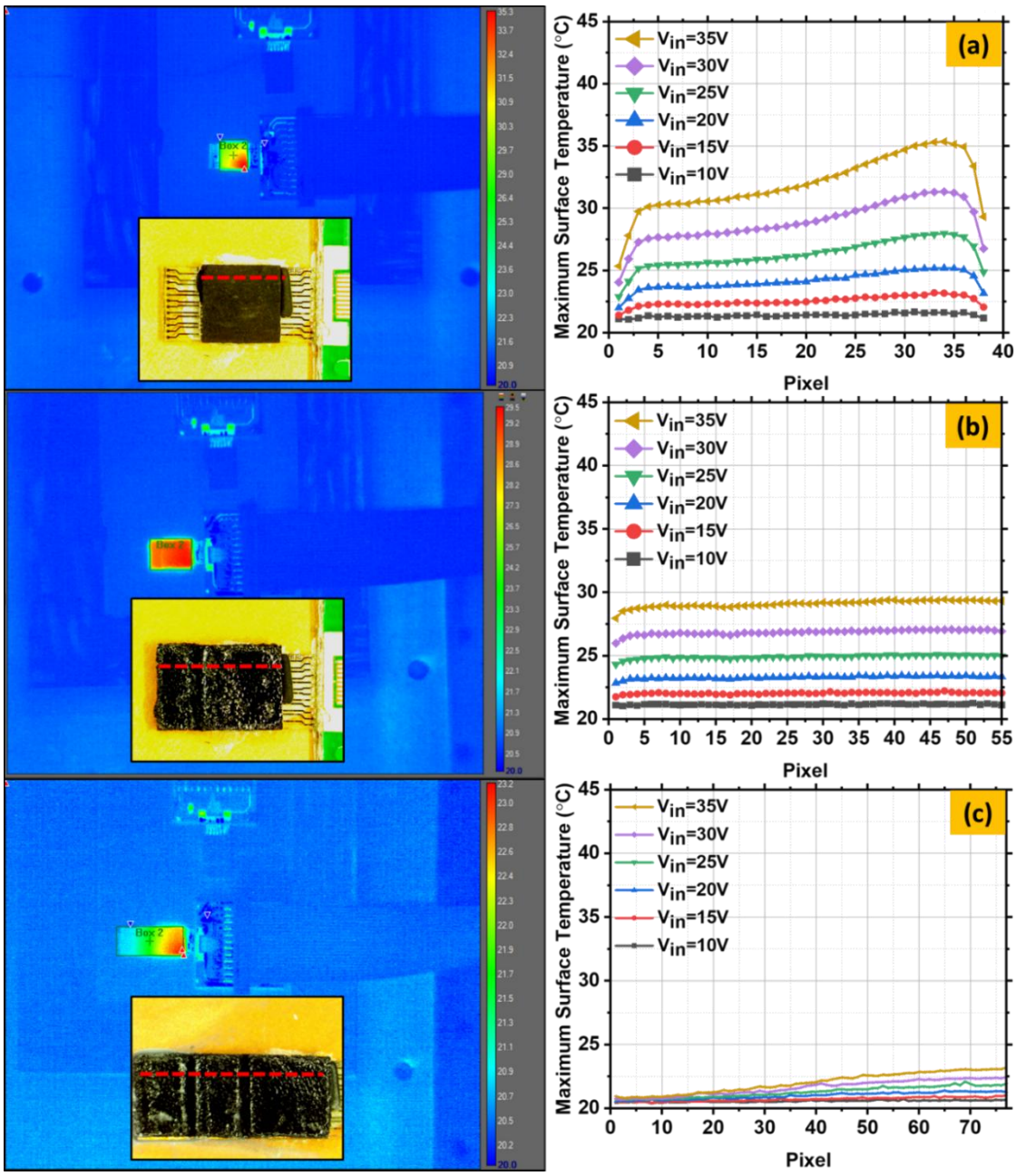


Figure 6.23: Infrared thermal images at maximum input power of a heater loopback in the reference thermal chip and maximum surface temperature profile along the horizontal direction (marked with a red dotted line) in case of (a) reference thermal chip flip-chip bonded on the glass interposer, (b) copper clip attached on top of the chip in the assembly (reference thermal chip flip-chip bonded on the glass interposer) and (c) extended copper clip attached on top of the chip in the assembly with the extended copper clip contacting the heat sink.

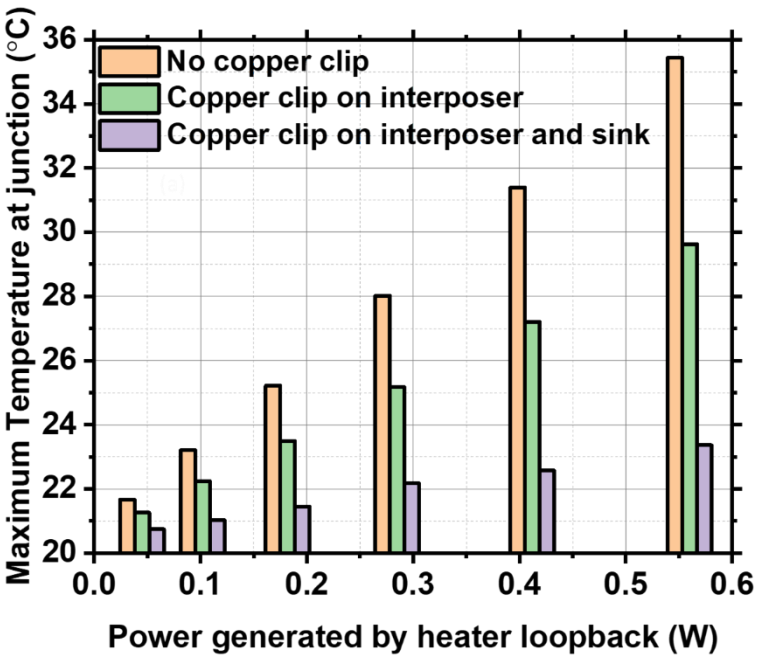


Figure 6.24: Comparison between the maximum junction temperature on the thermally active surface of the reference thermal chip when it is bonded to the glass interposer with no copper clip, copper clip only extending till the glass interposer and extended copper clip where its length is elongated to contact the heat sink surface. Note that only one heater loopback is operational in this case.

In addition to this, the active surface of the chip (the junction at the frontside of the chip bonded to the glass interposer) conducts the heat maximally towards the backside of the chip (lower thermal resistance), which is measured using the infrared thermal camera. In the case of the measurement with copper clip and extended clip attachment, the temperature of this active surface of the reference thermal chip will be only slightly higher than the measured temperature because of the thermal resistance offered by the thermal grease between the chip and copper clip, as seen in **Figure 6.24**.

The previous experiment is also repeated with the simultaneous operation of two heater loopbacks of the reference thermal chip. This simultaneous operation of two heater loopbacks leads to the rise in maximum hotspot temperature from 35.4ºC (**Figure 6.23 (a)**) to 50.2ºC (**Figure 6.25 (a)**). The introduction of a copper clip results in uniform heat spreading from the reference thermal chip (**Figure 6.25 (b)**). Additionally, when the length of the copper clip is extended to contact the heat sink, the maximum junction temperature of the chip goes down significantly by 24ºC as compared to the case with no copper clip (when power generated by heater loopback is 0.56 W). This is also illustrated in **Figure 6.26**. The requirement of a thermal contact

between the copper clip and heat sink is also illustrated in **Figure 6.21** and **Table 6.8** through simulation. The decrease in temperature with the incorporation of the copper clip connected to the heat sink (as compared to the case with no copper clip) in simulation is higher as compared to that in the measurement due to the larger surface area of the interposer and more than one chips and TGVs present in vicinity of the EIC. In the measurement, this decrease in temperature is clearly visible, though the decrease is lower due to the absence of PCB in measurement where glass interposer is directly contacted with the copper base heat sink.

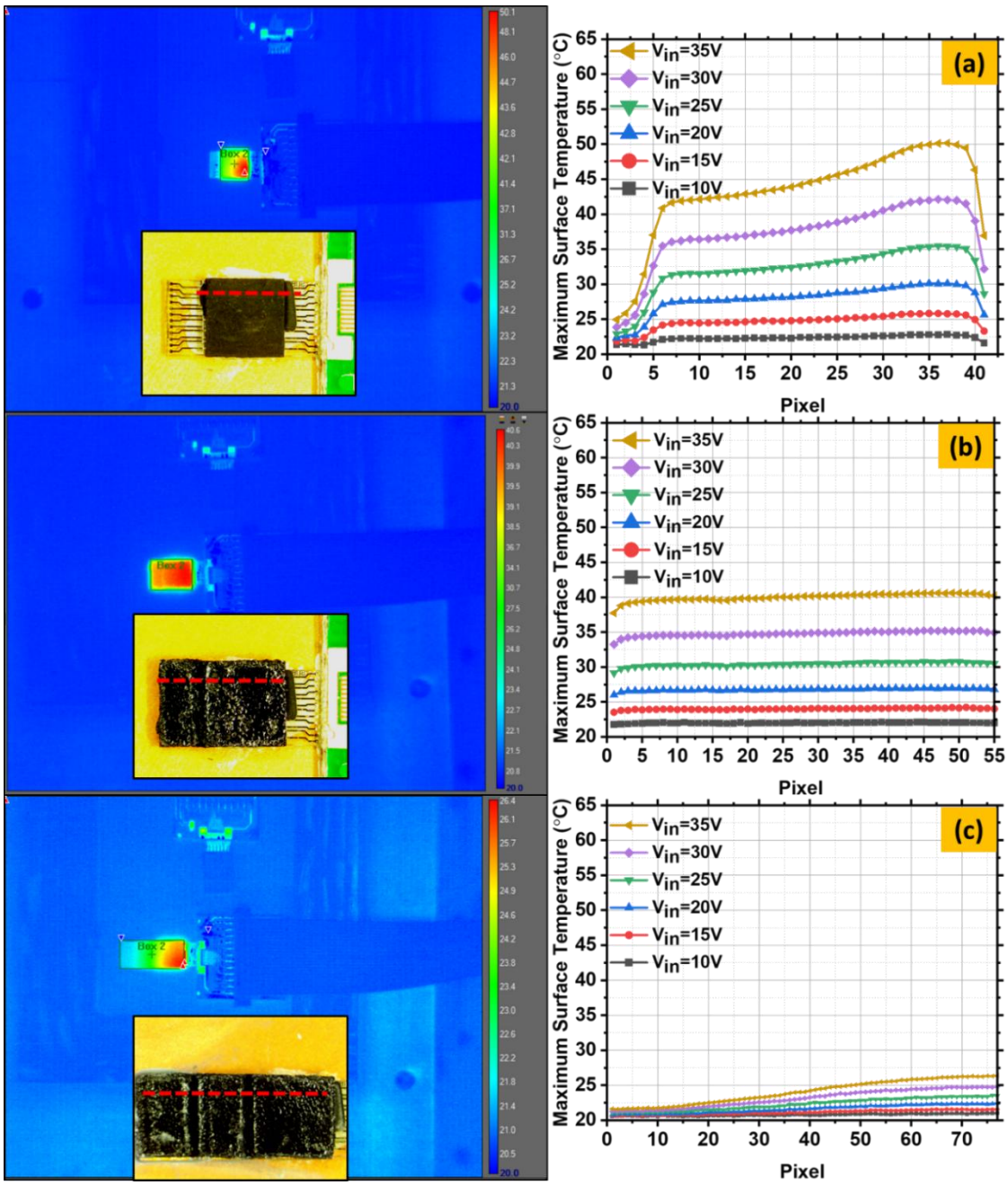


Figure 6.25: Infrared thermal images at maximum input power of heater loopbacks (two heater loopbacks are simultaneously operated) in the reference thermal chip and maximum surface temperature profile along the horizontal direction (marked with a red dotted line) in case of (a) reference thermal chip flip-chip bonded on the glass interposer, (b) copper clip attached on top of the chip in the assembly (reference thermal chip flip-chip bonded on the glass interposer) and (c) extended copper clip attached on top of the chip in the assembly with the extended copper clip contacting the heat sink.

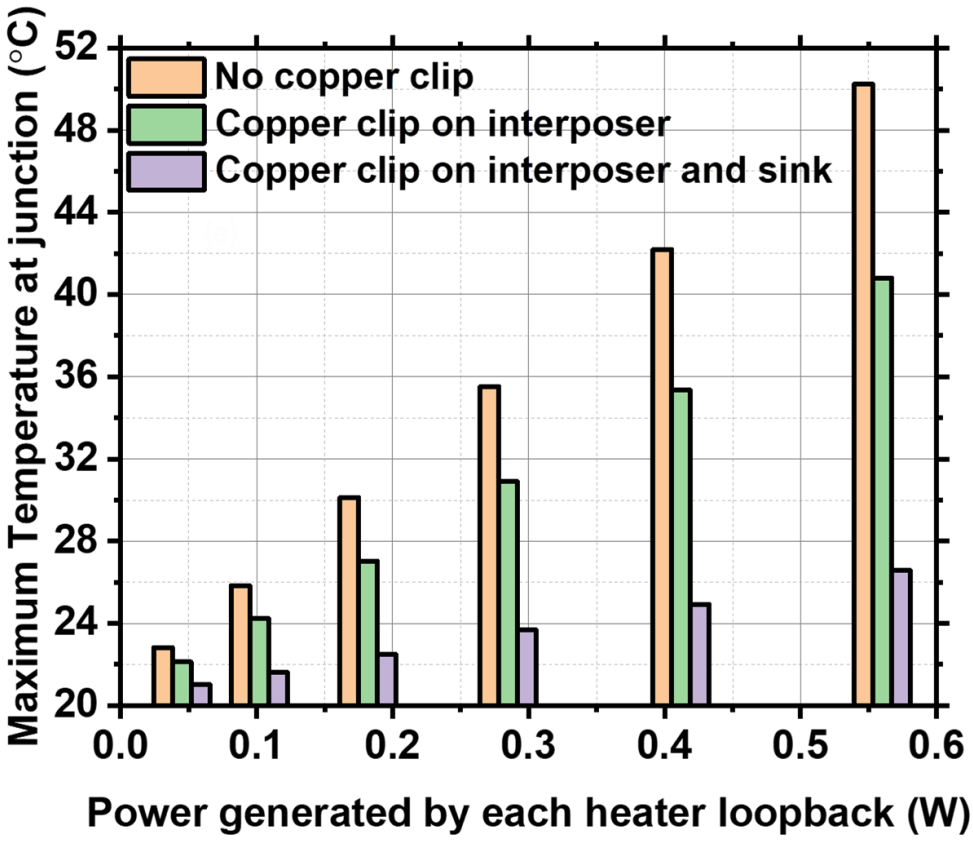


Figure 6.26: Comparison between the maximum junction temperature on the thermally active surface of the reference thermal chip when it is bonded to the glass interposer with no copper clip, copper clip only extending till the glass interposer and extended copper clip where it's length is elongated to contact the heat sink surface. Note that two heater loopbacks are simultaneously operational in this case.

6.6 Conclusion

Table 6.9: Maximum Temperatures of EIC1, EIC2, EIC3 and PIC in different configurations

Components		Maximum Temperature of the chip (ºC)								
		No Copper Clip	Copper Clip on glass interposer		Copper Clip on glass interposer with TGVs		Copper Clip on glass interposer with TGVs and heat sink in PCB		Extended Copper Clip with direct contact with heat sink	
			Segregated	Single	Segregated	Single	Segregated	Single	Segregated	Single
EIC	EIC1	79.25	59.29	60.32	55.05	56.75	33.72	33.88	33.54	33.65
	EIC2	81.82	61.30	59.21	56.72	55.45	33.80	32.44	34.63	32.21
	EIC3	79.15	59.27	58.41	55.04	54.60	33.72	31.77	34.56	31.54
PIC	PIC	25.45	23.71	23.64	22.82	23.32	20.95	20.92	20.99	20.90

The previously demonstrated work on thermal TGVs and SimTEC have been concentrated on the improvement of heat dissipation through the secondary heat flow path in 2.5D EIC-PIC co-packaged systems. The primary heat flow path which is essential for heat spreading is studied in detail through this chapter on a copper clip. The effect of change in electronic chip thickness, spacing between EIC and PIC, TIM thickness, copper clip thickness and length of the copper clip on the maximum temperature of EIC and PIC (with and without copper clip) is studied in detail. The single copper clip offers better heat dissipation and bonding process control as compared to the segregated copper clips but the segregated copper clips offer more design flexibility to the package designer.

Moreover, the impact of change in effective out-of-plane thermal conductivity of various elements in the primary heat flow path (such as TIM, TGVs under copper clip and bumps between glass interposer and PCB) on the temperature of EICs and PIC reveals that the effective volume for heat conduction is essential while choosing the component materials in the primary heat flow path. This also reiterates the requirement of the connection of the copper clip to the heat sink integrated PCB, either through the TGVS in glass interposer or direct contact with the heat sink. This is also experimentally proven by comparing the heat dissipation of reference thermal chip with no copper clip, copper clip on glass interposer (with no TGVs) and extended copper clip that makes direct contact with the heat sink.

This research enables further work for the integration of heat sinks in the PCB, either through microscale thermoelectric coolers (μ-TECs) or ultra-thin vapor chambers and micro-scale heat pipes integrated into the PCB. These package-level cooling mechanisms can also seamlessly integrate with the system-level cooling solutions.

6.7 References

[1] V. Lakshminarayanan and N. Sriraam, "The effect of temperature on the reliability of electronic components," *2014 IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT)*, Bangalore, India, 2014, pp. 1-6, doi: 10.1109/CONECCT.2014.6740182.

[2] P. Gupta et al., "Impact of Through Glass Vias Filling on the Performance of Passive Thermal Cooling in Photonic Packages," 2022 IEEE 9th Electronics System-Integration Technology Conference (ESTC), Sibiu, Romania, 2022, pp. 391-397, doi: 10.1109/ESTC55720.2022.9939531.

[3] Parnika Gupta, Amit Tanwar, Xiuyun He, Kamil Gradkowski, Kafil M. Razeeb, Padraic E. Morrissey, Peter O'Brien, "Substrate integrated micro-thermoelectric coolers in glass substrate for next-generation photonic packages," J. Optical Microsystems 4(1) 011006 (5 January 2024) https://doi.org/10.1117/1.JOM.4.1.011006.

[4] G. Bognár, G. Takács and P. G. Szabó, "A Novel Approach for Cooling Chiplets in Heterogeneously Integrated 2.5-D Packages Applying Microchannel Heatsink Embedded in the Interposer," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 13, no. 8, pp. 1155-1163, Aug. 2023, doi: 10.1109/TCPMT.2023.3298378.

[5] S. Snyder, J. Thompson, A. King, E. Walters, P. Tyler and M. R. Weatherspoon, "Thermally enhanced 3 dimensional integrated circuit (TE3DIC) packaging," 2014 IEEE 64th Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 2014, pp. 601-608, doi: 10.1109/ECTC.2014.6897347.

[6] P. Gupta et al., "Reference Thermal Chips for 2D and 3D Co-packaging Process Development," 2023 IEEE 73rd Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 2023, pp. 2160-2165, doi: 10.1109/ECTC51909.2023.00372.

[7] Mandal, R., Mui, Y. C., & Hengyun, Z. (2008, May). Effect of integrated heat spreader on thermal performance and bump joint reliability for flip chip packages. In 2008 11th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (pp. 786-792). IEEE.

[8] R. H. Lyon and A. E. Bergles, "Noise and Cooling in Electronics Packages," in IEEE Transactions on Components and Packaging Technologies, vol. 29, no. 3, pp. 535-542, Sept. 2006, doi: 10.1109/TCAPT.2006.880512.

[9] Wan, H., Iosifidis, N., Zhang, X., Rong, R., Antoniou, M., & Mawby, P. (2023, September). Thickness effect of copper clips on power module packaging design. In 2023 24th European Microelectronics and Packaging Conference & Exhibition (EMPC) (pp. 1-5). IEEE.

Chapter 7: Design guidelines for co-packaging electronic and photonic chips on glass interposers for next-generation photonic packages

7.1 Introduction

The co-packaging of electronic and photonic chips on a glass interposer demands efficient thermal management of the photonic chip and low-loss signal transmission between Electronic Integrated Circuits (EIC) and Photonic Integrated Circuits (PIC). Achieving this goal necessitates careful consideration of the placement and layout of Thermal Through Glass Vias (TGVs) and Electrical Through Glass Vias.

Ideally, thermal TGVs should be concentrated at the center of the chip or the areas where hotspots are being generated (EIC or PIC) to facilitate optimal thermal dissipation, while electrical TGVs should be distributed along the edges of the chips to ensure efficient signal transmission. We need to optimize the design and layout of both thermal and electrical TGVs to provide synergy between the chip designers and package designers with a comprehensive portfolio of design parameters.

Considering these requirements, the authors have compiled design guidelines aimed at guiding designers in the development of chips and glass interposers for co-packaging applications. These design rules serve as valuable guidelines to help designers make informed decisions regarding TGV placement, layout, and optimization, ultimately enhancing the performance and reliability of co-packaged electronic and photonic systems. The different parameters of electrical and thermal TGVs such as diameter, pitch, height and taper is studied and recommendations are made to maximize heat conduction and minimize insertion loss. The arrangement of TGVs, impact of hotspot location in EIC on PIC, spacing between EIC and PIC has also been studied to minimize thermal crosstalk with PIC and maximize heat conduction from EIC. These recommendations through the use of simulations and experiments will enable designers to choose the specifications (electrical and thermal) from glass interposer data sheets.

7.2 Arrangement of thermal TGVs

The impact of thermal TGVs arrangement on the heat dissipation of a chip placed on top of the thermal TGVs is studied in this case. We consider two thermal TGV arrangements, uniform pattern and honeycomb pattern, which are named Pattern 1 and Pattern 2 respectively, as shown in **Figure 7.1**. This figure shows the two arrangements for fully-filled copper vias. The analysis is also done for conformal-coated vias, where a given thickness of copper (t) covers only the sidewalls of the vias.

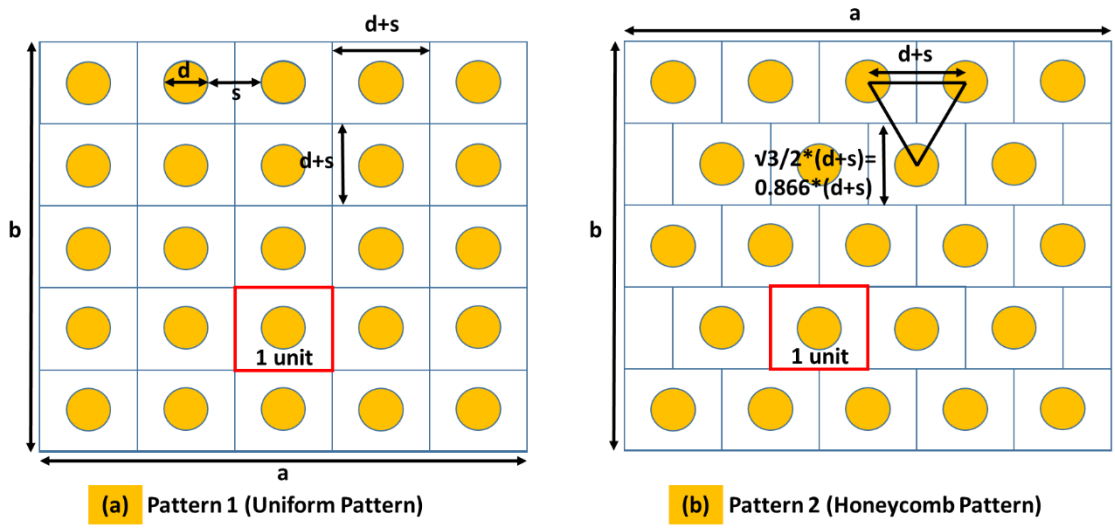


Figure 7.1: The arrangement of TGVs in (a) Pattern 1 or uniform pattern and (b) Pattern 2 or honeycomb pattern. Uniform pattern shows that the TGVs are arranged in a uniform pitch across all rows and columns whereas the honeycomb pattern shows that the TGVs are placed at half-pitch distances across alternating rows; where pitch signifies the distance between the center of two vias.

The normalized out-of-plane thermal resistance of a TGV for both Pattern 1 and Pattern 2 is derived for comparison using [1] as a reference. The following abbreviations are used in the derivation of the normalized out-of-plane thermal resistance of a TGV:

d - Diameter of TGV

s - spacing between TGVs

k_g -Thermal conductivity of glass

k_{Cu} - Thermal conductivity of Cu

k_{air} – Thermal conductivity of air

a - Length of space occupied by thermal TGVs on the interposer

b - Width of space occupied by thermal TGVs on the interposer

t - Thickness of copper in conformal-coated vias (along z direction)

T - Thickness of glass interposer and TGV (along z direction)

I - Number of columns of TGV array along length a

j- Number of rows of TGV array along width b

Pattern 1 (Fully Filled TGV)

In the case of Pattern 1 for fully filled TGVs, the thermal resistance of one unit is

$$\theta = \frac{T}{(k_{Cu} * \pi * \frac{d^2}{4}) + (k_g * [(d+s)^2 - \left(\pi * \frac{d^2}{4}\right)])}$$

Thus, the normalized thermal resistance for fully filled TGVs in Pattern 1 is

$$\theta_n = \frac{\theta}{\frac{T}{k_g * a * b}}$$

And the normalized thermal resistance for a fully-filled TGV in Pattern 1 is

$$\theta_{via} = \frac{\theta_n}{i * j}$$

Where, the number of fully filled TGVs in Pattern 1 are

$$i * j = \frac{(a * b)}{(d+s)^2}$$

Thus, the normalized thermal resistance for a fully-filled TGV is

$$\theta_{via} = \frac{k_g * (d+s)^2}{(k_{Cu} * \pi * \frac{d^2}{4}) + (k_g * [(d+s)^2 - \left(\pi * \frac{d^2}{4}\right)])} \quad (7.1)$$

Pattern 2 (Fully Filled TGV)

Similarly, the normalized thermal resistance for a fully filled TGV in Pattern 2 is

$$\theta_{via} = \frac{k_g * \frac{\sqrt{3}}{2} * (d+s)^2}{\left(k_{Cu} * \frac{d^2}{4}\right) + \left(k_g * \left[\frac{\sqrt{3}}{2} * (d+s)^2 - \left(\pi * \frac{d^2}{4}\right)\right]\right)} \quad (7.2)$$

Where, the number of fully filled TGVs in Pattern 2 are

$$i * j = \frac{(a * b)}{\frac{\sqrt{3}}{2} * (d+s)^2}$$

Pattern 1 (Conformal-Coated TGV)

In case of conformal-coated TGVs, the thermal resistance of a unit in Pattern 1 as shown in Figure 1 is calculated as

$$\frac{1}{\theta} = \frac{k_{air} * \pi * (\frac{d}{2} - t)^2}{T} + \frac{k_{Cu} * \pi t * (d - t)}{T} + \frac{k_g * [(d + s)^2 - (\pi * \frac{d^2}{4})]}{T}$$

$$\theta = \frac{T}{[k_{air} * \pi * \left(\frac{d}{2} - t\right)^2 + k_{Cu} * \pi t * (d - t) + k_g * (d + s)^2 - k_g * (\pi * \frac{d^2}{4})]}$$

The normalized thermal resistance for conformal-coated TGVs in Pattern 1

$$\theta_n = \frac{\theta}{\frac{T}{k_g * a * b}}$$

Consequently, the normalized thermal resistance for conformal-coated TGVs in Pattern 1 is

$$\theta_n = \frac{T}{[k_{air} * \pi * \left(\frac{d}{2} - t\right)^2 + k_{Cu} * \pi t * (d - t) + k_g * (d + s)^2 - k_g * (\pi * \frac{d^2}{4})]} * \frac{k_g * a * b}{T}$$

Number of conformal-coated TGVs in Pattern 1 are

$$i * j = \frac{(a * b)}{(d + s)^2}$$

The normalized thermal resistance for a conformal-coated TGV in Pattern 1 is

$$\theta_{via} = \frac{k_g * (d+s)^2}{\left[k_{air} * \pi * \left(\frac{d}{2} - t\right)^2 + k_{Cu} * \pi t * (d-t) + k_g * (d+s)^2 - k_g * \left(\pi * \frac{d^2}{4}\right)\right]} \quad (7.3)$$

Pattern 2 (Conformal-Coated TGV)

Similarly, the thermal resistance of a unit of conformal-coated TGVs in Pattern 2 is

$$\frac{1}{\theta} = \frac{k_{air} * \pi * (\frac{d}{2} - t)^2}{T} + \frac{k_{Cu} * \pi t * (d - t)}{T} + \frac{k_g * [\frac{\sqrt{3}}{2} * (d + s)^2 - (\pi * \frac{d^2}{4})]}{T}$$

Consequently, the normalized thermal resistance for conformal-coated TGVs in Pattern 2 is

$$\theta_n = \frac{T}{[k_{air} * \pi * \left(\frac{d}{2} - t\right)^2 + k_{Cu} * \pi t * (d - t) + k_g * \frac{\sqrt{3}}{2} * (d + s)^2 - k_g * (\pi * \frac{d^2}{4})]} * \frac{k_g * a * b}{T}$$

Where the number of conformal-coated TGVs in Pattern 2 are

$$i * j = \frac{(a * b)}{[\frac{\sqrt{3}}{2} * (d + s)^2]}$$

The normalized thermal resistance of a conformal-coated TGV in Pattern 2 is

$$\theta_{via} = \frac{\theta_n}{i*j} = \frac{k_g*\frac{\sqrt{3}}{2}*(d+s)^2}{\left[k_{air}*\pi*\left(\frac{d}{2}-t\right)^2+k_{Cu}*\pi t*(d-t)+k_g*\frac{\sqrt{3}}{2}*(d+s)^2-k_g*\left(\pi*\frac{d^2}{4}\right)\right]} \quad (7.4)$$

Using the equations 1 and 2 when the via diameter and spacing is varied between 50µm-200µm and 0-300µm respectively, the variation in the normalized out-of-plane thermal resistance of a fully filled TGV is shown in **Figure 7.2**.

Using the equations 3 and 4 when the via diameter, spacing and conformal-coated copper thickness in a TGV is varied between 50µm-200µm, 0-300µm and 5-50µm respectively, the variation in the normalized thermal resistance of a conformal-coated TGV is shown in **Figure 7.3**. **Figure 7.2** clearly shows that for both Pattern 1 and Pattern 2, the normalized thermal resistance increases for increased spacing between the vias. However, this increase in thermal resistance is substantially more for the case of 50µm diameter with increased spacing between TGVs, because of the smaller copper volume in glass. There is a one-third drop in the normalized thermal resistance, when the diameter increases from 50µm to 100µm (doubles) at a spacing of 300µm between TGVs, because of the increase in the volume of copper in glass.

Additionally, when we compare **Figure 7.2(a)** and **Figure 7.2(b)**, there is a decrease of 11.5% in normalized out-of-plane thermal resistance of Pattern 2 as compared to Pattern 1 for the worst case scenario (50µm via diameter and 300µm spacing between vias). In addition to this, the drop in the normalized thermal resistance in this worst-case scenario when the diameter increases from 50µm to 100µm is lower as compared to that in Pattern 1. However, the drop in the normalized out-of-plane thermal resistance in the ideal scenario (when the diameter is 200µm and the spacing between TGVs is 100µm) from Pattern 1 to Pattern 2 is very low (approximately 0.001).

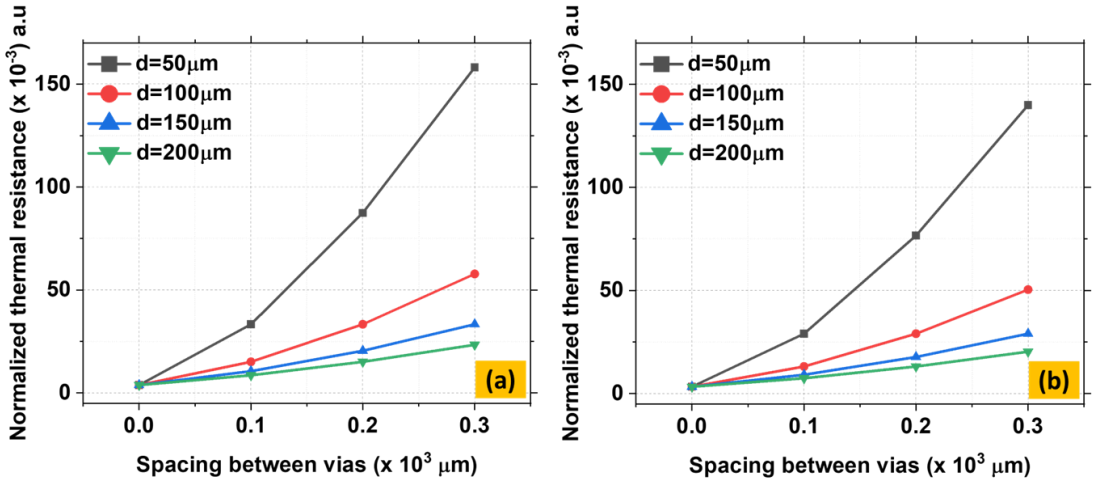


Figure 7.2: The change in normalized thermal resistance with change in TGV diameter for fully filled vias in (a) Pattern 1 and (b) Pattern 2. The decrease in the normalized thermal resistance in (b) as compared to (a) is high with the lowest diameter (50μm) and highest spacing (300μm).

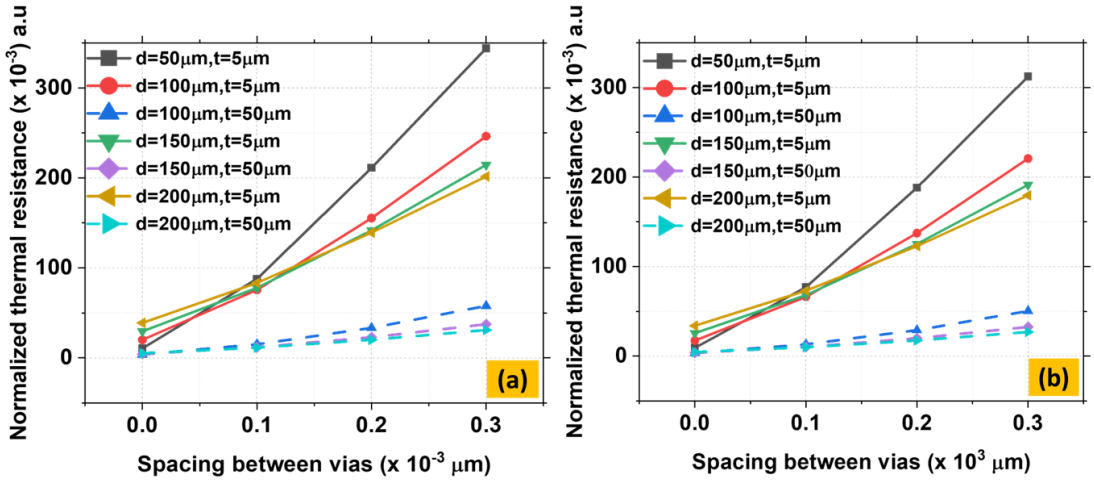


Figure 7.3: The change in normalized thermal resistance with change in TGV diameter and spacing for conformal coated vias with changing conformal coated copper thickness in (a) Pattern 1 and (b) Pattern 2. The decrease in normalized thermal resistance in the case of (b) honeycomb pattern as compared to (a) uniform pattern is more prominent in the case of the lowest diameter (50μm), highest spacing (300μm) and lowest thickness of the conformal coating of copper (5μm).

Similarly, in the case of conformal-coated TGVs, the lowering of the normalized thermal resistance from Pattern 1 to Pattern 2 is more evident in the cases where the conformal-coated copper in TGV has a thickness of 5μm as compared to the ones where the thickness of the conformal-coated TGV is 50μm. This is because of the increased volume impact of very low thermal conductivity of air (0.025 W/m.K) inside

the TGV cavity that heightens the out-of-plane thermal resistance. In the same vein, this lowering in normalized out-of-plane thermal resistance from Pattern 1 to Pattern 2 is very low (approx. 0.004 at 300 μm spacing between vias) when the conformal-coated copper thickness in TGV is higher (50μm); and especially lower at smaller spacing between TGVs. This is because of the increase in the volume of copper in glass and the decrease in the volume of air in glass.

Specifically, looking at the scenario when the thickness of conformal-coated copper is low (5μm) and the diameter of the TGV increases from 50μm to 200μm, the trend of change in normalized thermal resistance with different diameter reverses from spacing of 0μm to spacing of 300μm. This trend reversal is mainly attributed to the fact that when the spacing between TGVs is 0μm, the TGVs are essentially connected together, and the volume of air becomes very high when the diameter becomes higher. Conversely, when the spacing increases to 300μm, the volume of glass dominates that of air and hence the volume of glass and copper have a more significant impact on the normalized thermal resistance.

Previously, we saw a drop in the effective out-of-plane thermal resistance when the TGVs are arranged in a honeycomb pattern compared to the uniform pattern arrangement. In order to implement the effectiveness of honeycomb pattern (pattern 2) over uniform pattern (pattern 1) in the case of fully filled TGVs, we simulate thermal dissipation through the TGVs in both arrangements. In the simulation model, we also have the added effects of in-plane thermal conductivity, convection and radiation. The details of the simulation are shown in **Figure 7.4** and **Table 7.1**.

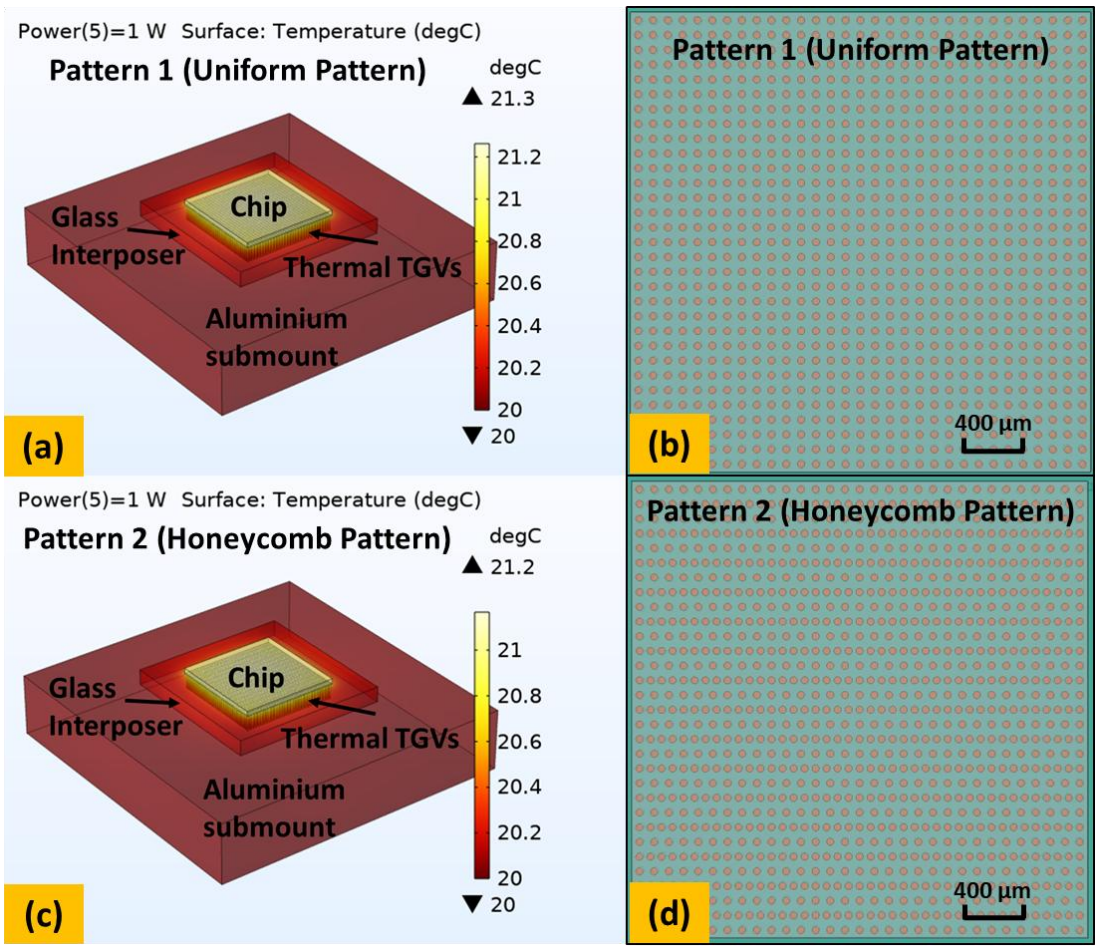


Figure 7.4: The simulation results of a 3.1mm×3.1mm chip bonded on the glass interposer with TGVs arranged in (a) Pattern 1 and (c) Pattern 2. The arrangement of TGVs in the simulation model is shown in (b) Pattern 1 and (d) Pattern 2.

Table 7.1: Parameters used in the simulation model for analyzing heat dissipation in Pattern 1 and Pattern 2.

Component in model	Length (mm)	Width (mm)	Thickness (mm)
Chip	3.1	3.1	0.167
Glass Interposer	5	5	0.5
Aluminium submount	10	10	2

The number of vias and the size of the chip is shown in **Table 7.2**. The diameter and pitch of the fully filled TGV is kept constant as 50µm and 100µm respectively. The increase in maximum temperature of the chip when the chip is uniformly powered at increasing powers of 0.1, 0.25, 0.5, 0.75 and 1W is shown. The number of TGVs under the chip increases from 961 to 1111 when the arrangement pattern changes from Pattern 1 to Pattern 2 for the chip size of 3.1×3.1 mm^2.

As the area of the chip becomes smaller, the number of vias under the chip decrease and the effectiveness of Pattern 2 over Pattern 1 becomes more prominent. The increase of this effectiveness of Pattern 2 over Pattern 1 on the maximum temperature of the chip is shown in **Figure 7.5**. This clearly shows that the decrease in the peak chip temperature is 3% when the 0.5×0.5 mm^2 chip is uniformly powered at 1W for the TGVs are arranged in a honeycomb pattern as compared to that arranged in a uniform pattern due to the increase in the number of vias and hence the increase in the volume of copper in glass (see Table 2). Note that the introduction of TGVs in Pattern 1 leads to an approximately 89% decrease in the chip's maximum temperature as compared to the case where there are no TGVs. However, the introduction of TGVs in Pattern 2 leads to an approximately 89.5% decrease in the chip's maximum temperature as compared to the case where there are no TGVs. Thus, the introduction of TGVs has a very significant impact on the maximum temperature of the chip bonded on the glass interposer with TGVs, but the arrangement of TGVs has a lesser impact on the thermal performance of the glass interposer.

Table 7.2: Table detailing the number of thermal TGVs used in the simulation model for Pattern 1 and Pattern 2 with varying chip sizes.

Size of Chip (Length×Width×Thickness mm^3)	**Number of thermal TGVs**	
	Pattern 1 (Uniform Pattern)	Pattern 2 (Honeycomb Pattern)
3.1×3.1×0.167	961	1111
1.5×1.5×0.167	225	260
0.5×0.5×0.167	25	29

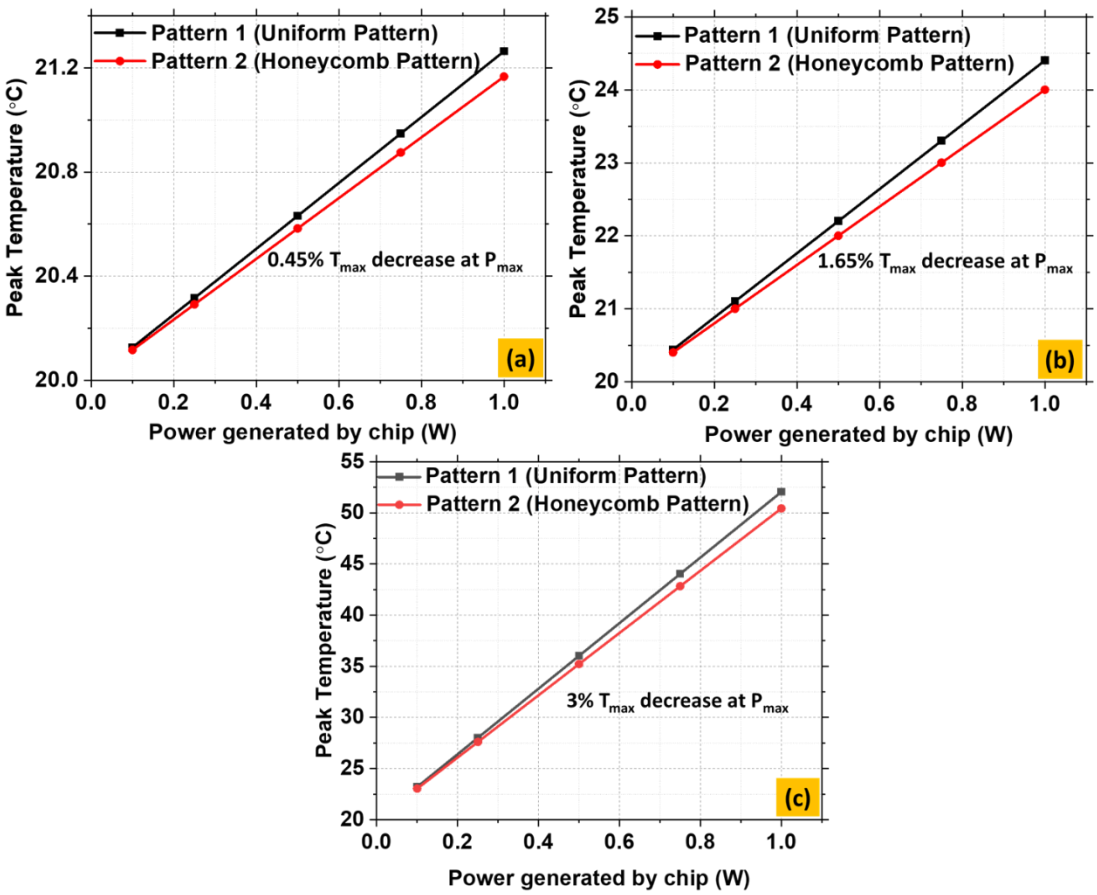


Figure 7.5: The increase in peak temperature of the chip with increasing power generated by the chip for Pattern 1 and Pattern 2 for different chip sizes such as (a) 3.1×3.1mm^2 (b) 1.5×1.5mm^2 and (c) 0.5×0.5mm^2.

Key Takeaways:

- The honeycomb pattern (Pattern 2) arrangement of fully filled TGVs leads to a larger decrease in the normalized out-of-plane thermal resistance through the glass interposer with TGVs as compared to the uniform pattern (Pattern 1), especially in the case when chip sizes are small and operating with high power, for example heat dissipation of a laser chip.
- The effectiveness of the honeycomb pattern arrangement of conformal copper coated TGVs can be exploited more in the case when the thickness (t) of the conformal-coated copper is lower.

7.3 Thermal TGV parameters and Requirement of Heat Sink

The electronic and photonic chips are packaged together on a glass substrate as shown in **Figure 7.6**. The dimensions of the chips, interposer and PCB are detailed in **Table 7.3**.

Table 7.3: Simulation Parameters for the electronic chip and photonic chip co-packaged on the glass interposer

	Length (mm)	**Width (mm)**	**Thickness (µm)**
Electronic Chip (EIC)	5	5	500
Photonic Chip (PIC)	5	5	500
Glass Interposer	25	25	460
PCB	50	50	500
Heat Sink	5	5	500

The in-plane and out-of-plane effective thermal conductivities for the different components in the simulation model are shown in **Table 7.4**.

7.3.1 Effective Thermal Conductivities used in simulation model

Table 7.4: The effective in-plane (k_{xy}) and out-of-plane (k_z) thermal conductivities for the different components used in the simulation model

Component in model	**k_{xy} (W/m.K)**	**k_z (W/m.K)**	**Reference**
Glass	1.2	1.2	[2]
Copper	400	400	[2]
PCB	0.3	0.3	[3]
Microbumps	2.8	4.4	[3]
Bumps	1.8	4	[3]

The main task of this simulation model is to analyze the effect of varying TGV diameter and pitches on the heat dissipated by the EIC and the thermal crosstalk between EIC and PIC, when the spacing between the EIC and PIC is increased from 100µm to 1000µm.

The different cases for the changing diameter and pitch of TGVs are listed in **Table 7.5**. The authors have included Case 1 and Case 22 as glass and copper under the chips instead of TGVs to act as a baseline for the simulation. In each of these cases, the effective thermal conductivities are included under both EIC and PIC. The TGV is assumed to have a hyperbolic structure where the middle diameter is assumed to be half of the TGV diameter (top and bottom diameter). The thickness of the TGVs is the same as that of the glass interposer. The effective thermal conductivities are isotropic in the cases of Glass, Copper and PCB. The maximum temperatures of the electronic chip and photonic chip when the electronic chip is uniformly powered to 1W is shown in **Figure 7.7**.

Table 7.5: The effective in-plane (k_{xy}) and out-of-plane (k_z) thermal conductivities for the different diameter and pitch of the thermal TGVs. The table also contains the cases 1 and 22 when there are no thermal TGVs present (glass in Case 1) and when the TGVs are replaced with an equivalent copper block in the glass interposer (Copper in Case 22).

Case Number	Diameter	Pitch	k_{xy} (W/m.K)	k_z (W/m.K)
1	Glass	Glass	1.2	1.20
2	50	150	1.33	17.61
3	50	175	1.29	13.31
4	50	200	1.27	10.51
5	50	225	1.26	8.58
6	60	150	1.39	24.71
7	60	175	1.34	18.54
8	60	200	1.30	14.52
9	60	225	1.28	11.76
10	70	150	1.47	33.08
11	70	175	1.39	24.69
12	70	200	1.34	19.24
13	70	225	1.31	15.49
14	80	150	1.56	42.72
15	80	175	1.46	31.76
16	80	200	1.39	24.65
17	80	225	1.35	19.78
18	90	150	1.68	53.63
19	90	175	1.53	39.76
20	90	200	1.45	30.77
21	90	225	1.39	24.61
22	Copper	Copper	400	400

7.3.2 EIC and PIC packaged on Glass Interposer and PCB

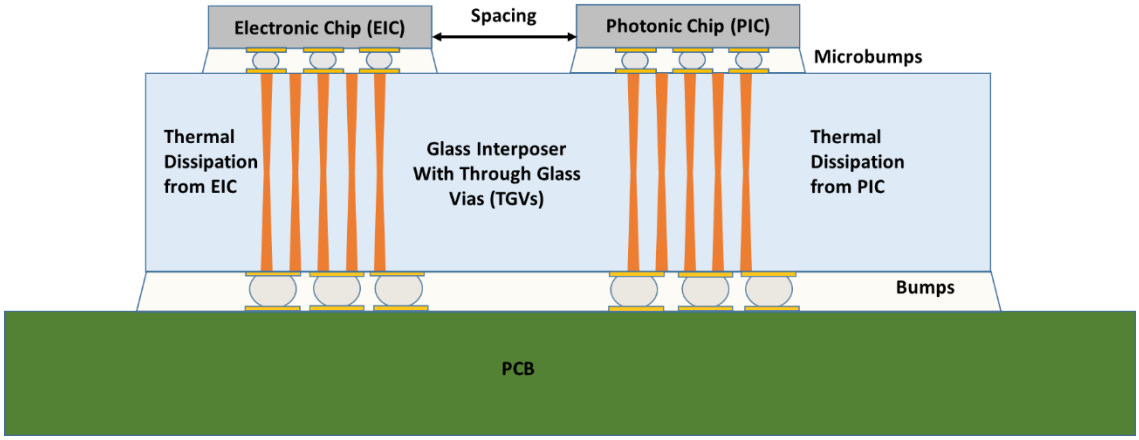


Figure 7.6: The electronic chip (EIC) and photonic chip (PIC) co-packaged on the glass interposer with TGVs under the chips. The spacing between the EIC and PIC varies which varies the volume of glass present between the chips. The TGVs connect the chips on top to the PCB board.

The maximum temperatures of the electronic chip when it is uniformly powered to 1W are tabulated in **Table B.1** (S1, Appendix B). The maximum temperatures of the photonic chip when the electronic chip is uniformly powered to 1W are tabulated in **Table B.2** (S1, Appendix B).

The scatter plot (**Figure 7.7**) derived from **Table B.1** and **Table B.2** (S1, Appendix B) shows the maximum temperature of the electronic and photonic chip with varying spacing between them when the electronic chip is powered to 1W. It is clear from the data that as the spacing is increased between EIC and PIC, the maximum temperature of the electronic chip increases and the temperature of the photonic chip decreases. The increase in EIC temperature due to increased spacing between EIC and PIC is the least in Case 1 (approximately 2ºC) and the highest in Case 22 (approximately 4.9ºC). Similarly, the decrease in PIC temperature with increased spacing between EIC and PIC is the least in Case 1 (approximately 4.9ºC) and the highest in Case 22 (approximately 6.9ºC). This is because the heat dissipation in glass (Case 1) is very low due to its low thermal conductivity and the increased spacing of the PIC from EIC does not have a significant impact because of low lateral heat conduction, which explains the lower temperature differences of EIC and PIC as the spacing is increased. However, in Case 22, the copper under the EIC and PIC allows significant lateral thermal crosstalk, resulting in a significant increase in temperature of EIC and a

significant drop in temperature of the PIC as the spacing is increased. Case 1 (Glass) and Case 22 (Copper) form the highest and lowest peak temperature points for EIC whereas they form the lowest and highest peak temperature points for the PIC at a given spacing. This is due to the combined effect of vertical and lateral heat conduction in the glass interposer.

When specifically looking at Cases 2-21, the trend of increasing EIC temperature and decreasing PIC temperature with increase in spacing between EIC and PIC remains the same. The maximum EIC temperature (49.554ºC) belongs to Case5 at 1000µm spacing and the minimum EIC temperature (45.022ºC) belongs to Case 18 at 100µm spacing. As already explained, the maximum EIC temperature with higher spacing and minimum EIC temperature with lower spacing occurs due to the effect of lateral thermal conduction. The maximum EIC temperature in Case 5 entails the TGVs with lowest diameter and highest pitch, thus lowering the heat dissipation from EIC. The minimum EIC temperature in Case 18 entails the highest TGV diameter and lowest pitch, thus increasing the thermal dissipation from the EIC.

Conversely, the maximum PIC temperature (29.5672ºC) belongs to Case 18 at 100µm spacing and the minimum PIC temperature (24.132ºC) belongs to Case 5 at 1000µm spacing, when taking Cases2-21 into account. The higher PIC temperature at lowest spacing and lower PIC temperature at highest spacing is owed to the thermal crosstalk between EIC and PIC. Secondly, the maximum PIC temperature in Case 18, which involves highest diameter and lowest pitch of TGVs increases the lateral heat conduction (highest k_{xy}). The minimum PIC temperature is visible in Case 5 due to the lowest diameter and highest TGV pitch thus lowering the lateral thermal conduction (lowest k_{xy}).

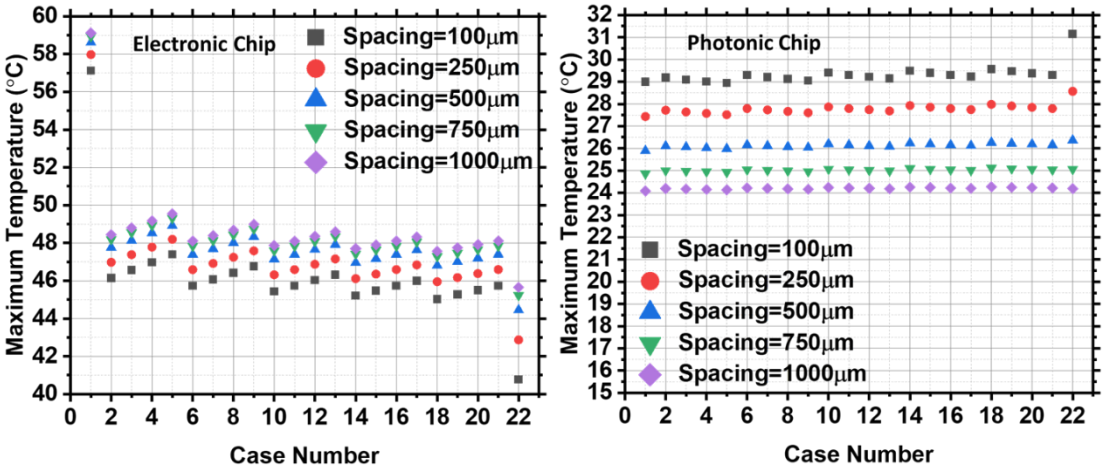


Figure 7.7: Scatter plot showing the maximum temperatures of the EIC and PIC when they are co-packaged on the glass interposer with TGVs. The volume under the EIC and PIC signifying the effective thermal conductivity of the TGVs is changed across glass (Case 1), TGVs with different diameter and pitches (Case 2-21) and copper in glass interposer (Case 22).

The next noticeable domain is in the case of EIC, the maximum temperature drops by more than 10 ºC when we go from Case 1 to Case 2-21. Thus, the introduction of TGVs has a significant impact on the thermal performance of the EIC on the glass interposer. However, the drop in the maximum EIC temperature as we go from Case 2-21 to Case 22 is approximately 6 ºC (100µm spacing) – 3 ºC (1000µm spacing). This drop is higher in the case of lower spacing (see the change in the grey dot from Case 21 to Case 22 for electronic chip in **Figure 7.7**) due to the additional impact of lateral thermal conduction path offered by the copper block under the PIC located at the minimum distance of 100µm. This largest drop in temperature is approximately 6 ºC as we move from TGVs to a copper block in glass substrate.

Thus, introduction of thermal TGVs under EIC in a glass interposer creates a substantial difference in the temperature of the electronic chip especially at lower spacing between EIC and PIC.

In the case of the PIC, the maximum temperature increases by the highest of approximately 0.6 ºC as we move from Case 1 to Case2-Case 21, thus the introduction of TGVs does not significantly impact the temperature of the PIC. This is because of the volume of glass between the TGVs under the EIC and PIC respectively preventing lateral thermal conduction. Additionally, the maximum PIC temperature increases by a maximum of 1.6 ºC as we move from Case 1-21 to Case 22. This change is visible at a spacing of 100µm (see the change in the grey dot from Case 21 to Case 22 for photonic chip in **Figure 7.7**) and this change becomes very low (approx. 0.01ºC) at a spacing of 1000µm. Thus, the move from TGVs to copper block under the PIC only shows a visible impact on the PIC temperature at the lowest spacing. This can be explained by the copper block (both under EIC and PIC) allowing for the highest thermal crosstalk between EIC and PIC at the lowest spacing between them.

Since we are concerned about minimizing the EIC and PIC temperature while they are co-packaged on the glass interposer, we should be using the highest manufacturable TGV diameter and lowest pitch under the EIC to enable effective heat dissipation. In addition to this, the lowest TGV diameter and highest pitch under the PIC at a lower spacing between EIC and PIC should be preferred to lower thermal crosstalk between electronic and photonic chip. Depending on the application requirements, the ideal design, can change to having no TGVs under the PIC and a high density of TGVs under the EIC; with longer spacing between EIC and PIC (beyond 0.5mm) to free up design space as the thermal impact of TGVs on PIC becomes negligible in that case.

7.3.3 EIC and PIC packaged on Glass Interposer with heat sink integrated into the PCB

The EIC and PIC temperature goes to the lowest of 45ºC and 24.1ºC respectively for the co-packaged structure on glass interposer with TGVs and no heat sink. In order to further lower the temperatures of the EIC and PIC, we have to include a copper heat sink in the PCB in the area under the bumps connecting the glass interposer to the PCB. The incorporation of this heat sink in the PCB lowers the EIC and PIC

temperature, which is shown in **Table B.3** (S1, Appendix B) and **Table B.4** (S1, Appendix B) respectively.

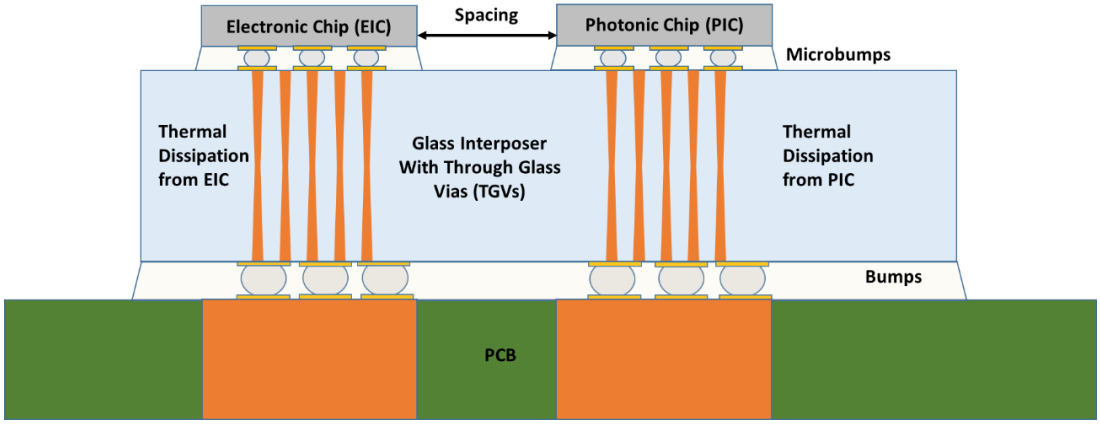


Figure 7.8: The electronic chip and photonic chip co-packaged on the glass interposer with TGVs and heat sink embedded in the PCB. The heat sink is a copper block embedded in the PCB to allow for the heat removal from the EIC and PIC and it connects to the backside of the PCB maintained at 20ºC.

The maximum temperatures of the electronic chip when it is uniformly powered to 1W are tabulated in **Table B.3** (S1, Appendix B).

The maximum temperatures of the photonic chip when the electronic chip is uniformly powered to 1W are tabulated in **Table B.4** (S1, Appendix B).

The scatter plot in **Figure 7.9** clearly shows the lowered EIC and PIC temperatures as compared to the previous section (**Figure 7.7** in Section 7.3.2) without including the heat sink. This heat sink thus reduces the variation in maximum temperature of both EIC and PIC with variations in the spacing between the chips. This is explained because of the dominant copper block integrated in PCB offering the primary thermal path for heat conduction and hence reducing the effect of changes in the spacing. The variation in maximum EIC temperature with increased spacing between EIC and PIC (100µm-1000µm) is very low (maximum of 0.3ºC in Case 1) as compared to the variation in maximum PIC temperature (maximum of 0.9ºC in Case 1). This is because the heat sink in the PCB provides a substantial path for heat flow to reduce the variation of EIC temperature with different spacing between EIC and PIC, whereas the PIC having no TGVs is still susceptible to minimal thermal crosstalk (see the scales in **Figure 7.9** for electronic and photonic chip). Compared to the case without heat sink, the trend of decrease in EIC temperature with the introduction of TGVs remains

the same as the volume of copper under the EIC is increased. The introduction of TGVs does bring about a difference of approximately 11ºC in the maximum EIC temperature moving from Case 1 to Cases 2-21; which proves the importance of integration of TGVs for effective heat dissipation of EIC. However, in the case of the PIC, the maximum temperature variation (0.9ºC) with spacing is highest in Case 1 in **Figure 7.9** below. This can be accounted due to the thermal crosstalk being a little more prevalent in Case 1, when no heat sinking is present to lower the PIC temperature, whereas in other cases (with TGVs and copper block), the heat sink allows for the lateral heat to be transferred to the heat sink very quickly.

Looking specifically at Cases 2-21, the maximum EIC temperature occurs in Case 5 (25.1ºC) at 1000µm spacing and the minimum EIC temperature occurs in Case 18 (23.37ºC) at 100µm spacing. The same explanation where the lowest TGV diameter and highest pitch (Case 5) when the PIC is placed far away from the EIC results in an increased EIC temperature. In addition to this, the highest TGV diameter and lowest pitch with PIC placed near to the EIC brings down the EIC temperature to the lowest.

However, in the case of the PIC, for Cases 2-21, **Table B.4** (S1, Appendix B) and **Figure 7.9** show the maximum temperature for Case 5 (20.26ºC) at a spacing of 100µm and the minimum temperature for Case 18 (20.035ºC) at a spacing of 1000µm. This is opposite to the previous section with no heatsink (Section 7.3.2) integrated in PCB. This trend is observed because the lowest diameter and highest TGV pitch (Case 5) allows less lateral heat conducted from the EIC to be transferred to the heat sink, making the PIC temperature go up. The largest diameter and smallest pitch of the TGV in case 18 allows more laterally transferred heat from the EIC to be effectively conducted to the heat sink in the PCB, allowing PIC temperature to go down.

The integration of heat sink in PCB makes a significant impact on the thermal performance of glass interposer as the difference in maximum temperature of EIC and PIC is halved in this case as compared to the case with no heat sink (Section 7.3.2) in PCB ($\Delta T_{EIC\text{-}PIC}$ lowers from 28.9ºC to 14.7ºC in Case 1). The design rule in this case changes in the case of PIC, such that in order to lower the temperature of co-packaged EIC and PIC with heat sink integrated in the PCB, we need to include TGVs with largest diameter and smallest pitch under the EIC and PIC, at any given spacing between the EIC and PIC.

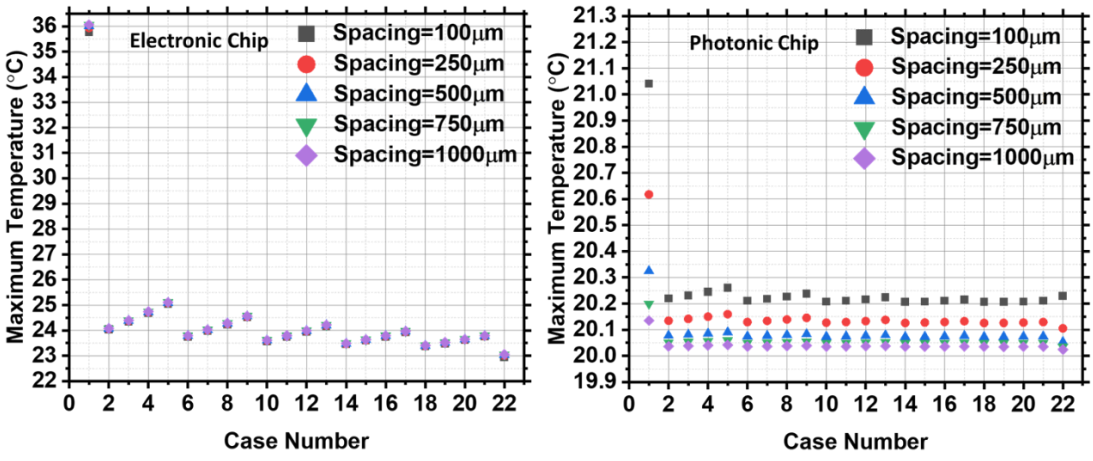


Figure 7.9: Scatter plot showing the maximum temperatures of the EIC and PIC when they are co-packaged on the glass interposer with TGVs and heat sink integrated in the PCB. The volume under the EIC and PIC signifying the effective thermal conductivity of the TGVs is changed across glass (Case 1), TGVs with different diameter and pitches (Case 2-21) and copper in glass interposer (Case 22). The heat sink embedded in the PCB reduces the temperature variation for different spacings across all cases when compared to **Figure 7.7**.

7.3.4 EIC and PIC packaged on Glass Interposer with heat sink attached directly under thermal TGVs

The difference between the maximum temperatures of EIC and PIC can be further lowered from 14.7ºC in the case of co-packaged electronic and photonic chip on glass interposer with no TGVs and heat sink integrated in PCB to 13ºC by increasing the thickness of the heat sink to 770µm (Case 1). This includes eliminating the C4 bumps and underfill interface between the glass interposer and PCB and bringing the thermal TGVs in direct contact with the heat sink or micro-thermoelectric cooler (micro-TEC) allowing a lower thermal resistance path to the heat sink/micro-TEC. The maximum EIC and PIC temperatures are displayed in **Table B.5** (S1, Appendix B) and **Table B.6** (S1, Appendix B) and scatter plot is shown in **Figure 7.11** respectively.

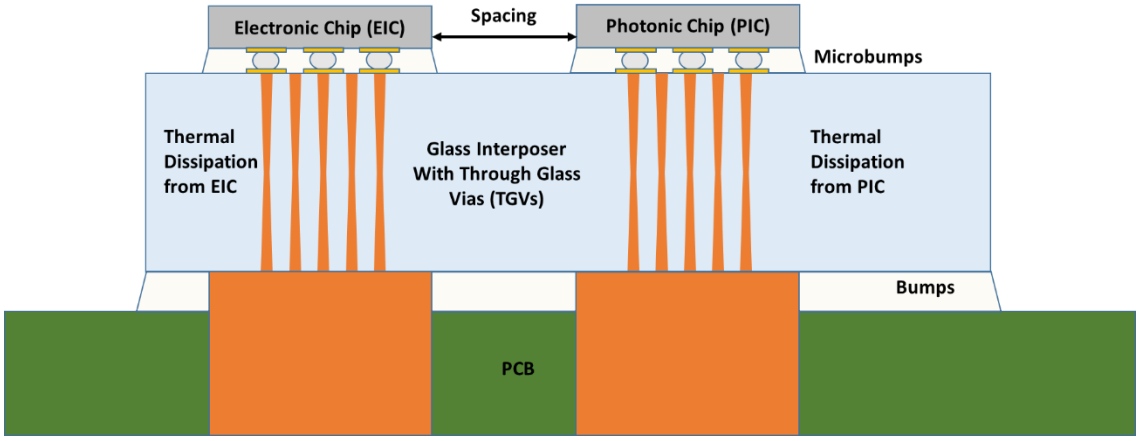


Figure 7.10: The electronic chip and photonic chip co-packaged on the glass interposer with TGVs and heat sink embedded in the PCB right under the thermal TGVs. The height of the copper block embedded in the PCB is increased to make contact with the thermal TGVs under EIC and PIC. This is done because the replacement of the bumps layer with copper reduces thermal resistance, and it is feasible to include it in the package architecture and packaging process flow.

The maximum temperatures of the electronic chip when it is uniformly powered to 1W are tabulated in **Table B.5** (S1, Appendix B).

The maximum temperatures of the photonic chip when the electronic chip is uniformly powered to 1W are tabulated in **Table B.6** (S1, Appendix B).

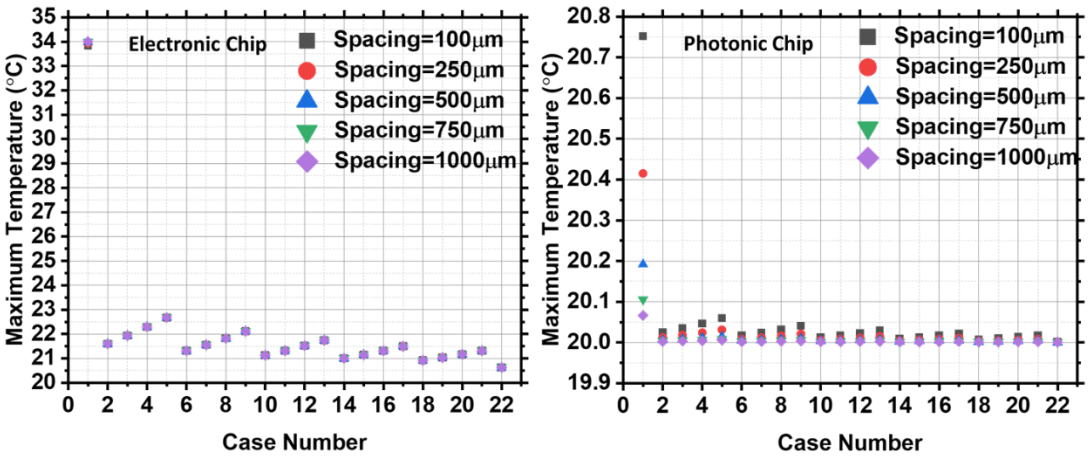


Figure 7.11: Scatter plot showing the maximum temperatures of the EIC and PIC when they are co-packaged on the glass interposer with TGVs and heat sink integrated in the PCB right under the thermal TGVs. The volume under the EIC and PIC signifying the effective thermal conductivity of the TGVs is changed across glass (Case 1), TGVs with different diameter and pitches (Case 2-21) and copper in glass interposer (Case 22). The heat sink embedded in the PCB under the thermal TGVs further reduces the temperature variation for different spacings across all cases for the PIC, as compared to **Figure 7.9**.

The scatter plot in **Figure 7.11** details the maximum temperatures of the EIC and PIC with varied spacing between EIC and PIC on the glass interposer with TGVs, when the heat sink/micro-TEC is in direct contact with thermal TGVs. This plot clearly shows that the largest variation of the maximum EIC temperature (0.18ºC) and maximum PIC temperature (0.68ºC) with varied spacing between EIC and PIC is lower than the previous scenario (**Figure 7.9** in section 7.3.3). The attachment of the heat sink/micro-TEC directly below the thermal TGVs thus reduces the temperature variation of EIC and PIC with respect to spacing between them. The variation of the maximum PIC temperature as we go forward from Case 1 to Case 22 is decreasing due to the higher volume of copper incorporated in glass which makes it easier for the laterally conducted heat to be dissipated through vias and heat sink/micro-TEC.

In the Cases 2-21, the maximum EIC temperature belongs to Case 5 (22.676ºC) at 1000µm spacing and the minimum EIC temperature belongs to Case 18 (20.915ºC) at

100µm spacing. The explanation is the same as that in Section 7.3.2 and 7.3.3, which essentially means that the highest TGV diameter and smallest TGV pitch under the EIC leads to the minimum temperature for the EIC.

Similarly, the maximum PIC temperature belongs to Case 5 (20.05ºC) at 100µm spacing and the minimum PIC temperature belongs to Case 18 (20.008ºC) at 1000µm spacing. The explanation remains the same as that in Section 7.3.3, which states that the highest TGV diameter and smallest TGV pitch under the PIC, brings down the PIC temperature as it becomes easier to dissipate the heat conducted laterally from the EIC. The design rule for this model remains the same as that in section 7.3.3.

7.3.5 EIC and PIC packaged on Glass Interposer with heat sink attached directly under the thermal TGVs (only for EIC)

This analysis is similar to section 7.3.4 but the 770µm heat sink is only placed below the thermal TGVs of the EIC and not the PIC. The difference between the maximum temperature of the EIC and PIC is further reduced from 13ºC to 12.2ºC as the thermal crosstalk between the EIC and PIC becomes slightly higher. The maximum temperatures of the EIC and PIC when the EIC is powered to 1W are shown in the **Table B.7** (S1, Appendix B) and **Table B.8** (S1, Appendix B) respectively.

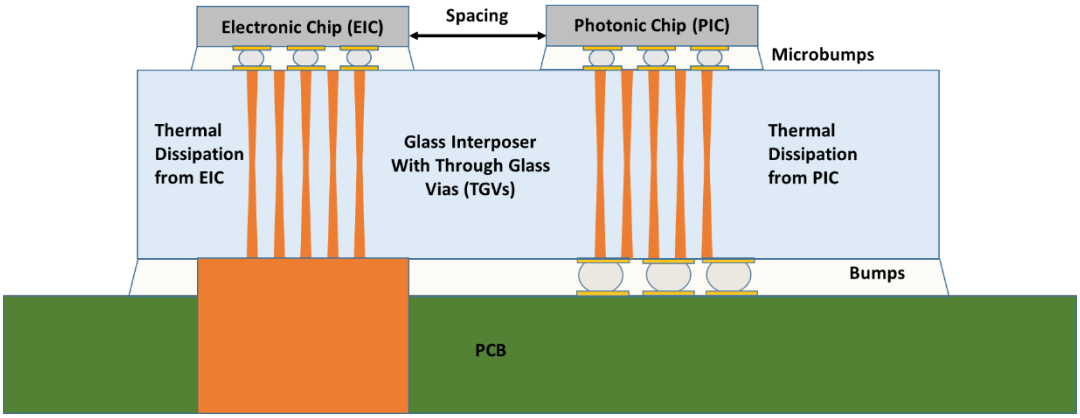


Figure 7.12: The electronic chip and photonic chip co-packaged on the glass interposer with TGVs and heat sink embedded in the PCB right under the thermal TGVs only for EIC. The height of the copper block embedded in the PCB is increased to make contact with the thermal TGVs only under the EIC. This is done to remove heat effectively from the EIC and allows for less lateral heat conduction to the thermally passive PIC.

The maximum temperatures of the electronic chip when it is uniformly powered to 1W are tabulated in **Table B.7** (S1, Appendix B).

The maximum temperatures of the photonic chip when the electronic chip is uniformly powered to 1W are tabulated in **Table B.8** (S1, Appendix B).

In the case of the EIC, the maximum temperature of the EIC considering cases 2-21, occurs in Case 5 owing to the smallest diameter, largest TGV pitch and maximum spacing between EIC and PIC. The minimum EIC temperature comes across in Case 18 due to the largest TGV diameter, smallest TGV pitch and minimum spacing.

In case of the PIC, the maximum and minimum PIC temperature between Cases 2-21 occurs in Case 5 at 100µm spacing and Case 18 at 1000µm spacing. The explanation remains the same as that of Section 7.3.2 and Section 7.3.3. However, when we compare the scatter plots in **Figure 7.11** and **Figure 7.13**, we notice the higher variation or spread of PIC temperatures with increased spacing between the EIC and PIC. This is because there is no copper block or sink underneath the thermal vias for PIC and hence the path for thermal conduction under the PIC encounters more thermal resistances.

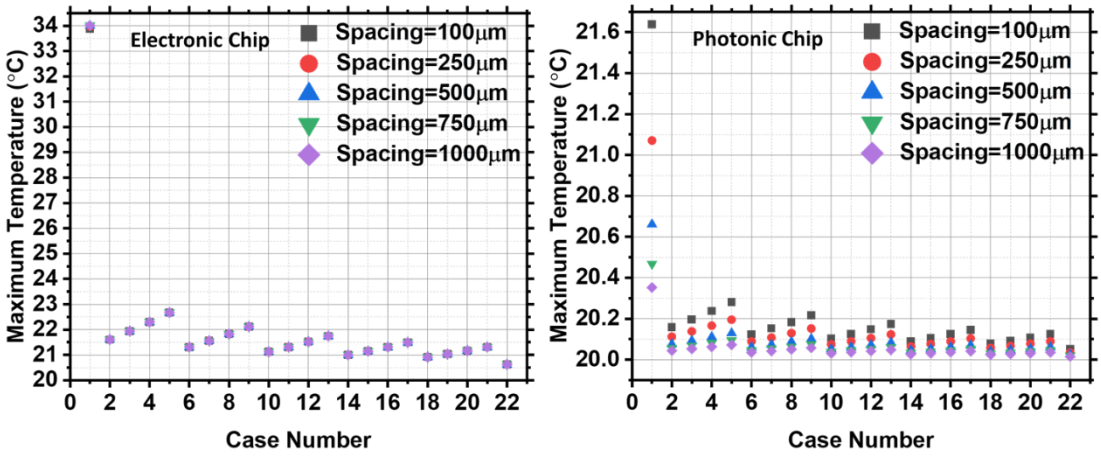


Figure 7.13: Scatter plot showing the maximum temperatures of the EIC and PIC when they are co-packaged on the glass interposer with TGVs and heat sink integrated in the PCB right under the thermal TGVs of the EIC only. The volume under the EIC and PIC signifying the effective thermal conductivity of the TGVs is changed across glass (Case 1), TGVs with different diameter and pitches (Case 2-21) and copper in glass interposer (Case 22). The heat sink embedded in the PCB under the thermal TGVs of the EIC reduces the temperature variation for different spacings across all cases for both the EIC and PIC, as compared to **Figure 7.7**.

Key Takeaways:

- In Section 7.3.2, with EIC and PIC co-packaged on glass interposer and PCB, the importance of incorporating TGVs under the EIC for effective heat dissipation from EIC is underlined. The use of largest TGV diameter and smallest TGV pitch under the EIC for effective heat dissipation and smallest TGV diameter and largest TGV pitch (if thermal TGVs are needed, otherwise authors recommend no thermal TGVs) under the PIC to lessen thermal crosstalk is recommended, when the spacing between EIC and PIC is less than 0.5mm. When the spacing is greater than 0.5mm, largest TGV diameter and smallest TGV pitch under the EIC and smallest TGV diameter and largest TGV pitch under the PIC is recommended.
- In Section 7.3.3, where the EIC and PIC are co-packaged on the glass interposer and PCB includes a copper heat sink integrated in the PCB; the authors recommend using the largest manufacturable diameter and smallest manufacturable pitch under the EIC and PIC for all spacings. The maximum EIC and PIC temperature decreases by approximately 40% and 27% respectively as compared to that in section 7.3.2 (without heat sink integrated in the PCB).
- In Section 7.3.4, the EIC and PIC are co-packaged on the glass interposer and PCB with the heat sink/micro-TEC directly contacting the thermal vias under the EIC and PIC. The incorporation of heat sink/micro-TEC directly under the thermal vias decreases the maximum EIC and PIC temperature by approximately 50% and 28% respectively. The use of the largest manufacturable TGV diameter and smallest TGV pitch under both the EIC and PIC is recommended.
- In Section 7.3.5, the EIC and PIC are co-packaged on the glass interposer and PCB with the heat sink/micro-TEC directly contacting the thermal vias only under the EIC. The incorporation of heat sink/micro-TEC directly under the thermal vias of the EIC keeps the maximum EIC temperature almost same as that in Section 7.3.4. However, the maximum PIC temperature slightly increases and the variation of the maximum PIC temperature with increased spacing also increases. The use of the largest manufacturable TGV diameter and smallest TGV pitch under both the EIC and PIC is recommended.

7.4 Hotspot Management

The aim for this section is to realize effective thermal design of the electronic chip (EIC) to facilitate thermal dissipation from the EIC and lessen the thermal crosstalk between the EIC and photonic chip (PIC). In Section 7.3, the EIC is uniformly powered to enunciate the impact of the TGV dimensional parameters on the thermal performance of glass interposers. In real designs, the chips have certain heat generating areas known as hotspots, which are replicated through the reference thermal chip [4] to emulate the thermal performance of the EIC. The reference RF chip and reference PIC are included in this experiment to study the thermal impact of hotspot location (heater loopbacks on reference thermal chip) on the reference RF chip and reference PIC. The reference RF chip and reference PIC is used to emulate the RF performance and optical performance of a PIC. In addition to this, there are thermal TGVs under the area of the EIC and PIC in Section 7.3, but in the real-life application there can be TGVs all around the glass interposer for stitching ground planes. The experiment in this section showcases the impact of TGVs spread out across the interposer on the thermal crosstalk between the reference chips.

The experiment involves the design of a 13mm × 7mm glass interposer to attach the reference chips on top of this glass interposer. The design of the glass interposer includes the under-bump metallization (UBM) pads which are a mirror image of the bond pads on the reference chips to bond the reference chips on the glass interposer. In addition to this, there is a large gold pad, which is effective for thermal spreading of temperature generated by the reference thermal chip. The glass interposer includes two polyimide layers on the top side of the glass interposer and one polyimide layer on the bottom side of the glass interposer. The UBM and gold pad are fabricated on top of the polyimide layers on glass interposer. The UBM is connected to RDL 2 on top of the second polyimide layer, which in turn is connected to RDL1 (on the surface of glass) through microvias. This RDL 1 on the glass surface is then connected to the backside RDL through TGVs. The TGVs have a pitch of 500µm and are spread out across the glass interposer, which adds on to the thermal crosstalk between the reference chips. The backside RDL is then connected to the BGA pads on top of the bottom polyimide layer through microvias. The design of the glass interposer for co-

packaging reference thermal chip, reference RF chip and reference PIC is shown in **Figure 7.14**.

The pads in all the reference chips are solder jetted with SAC 305 solder balls followed by sequential alignment of the reference chip pads with the corresponding UBM pads on the glass interposer using the Finetech flip-chip bonder. The reference chips are all reflowed at the same time and are bonded face down on the glass interposer. In the second step, this subassembly is then bonded on the Rogers PCB using BiSn solder balls. Finally, the soldered interfaces between the chip-glass interposer and glass interposer-PCB are epoxy underfilled. This assembly process is the same as that followed in the previous chapter. The uniformity of the epoxy underfill also impacts the thermal performance of the 2.5D package (see S2, Appendix B for more details).

There are 10 heater loopbacks (H1-H10) at the edges of the reference thermal chip, which are powered up sequentially to study their thermal impact on maximum temperature of the reference RF chip and reference PIC. The design and sizes of the reference chips, glass interposer and orientation of the chips and heater loopbacks is shown in **Figure 7.15**.

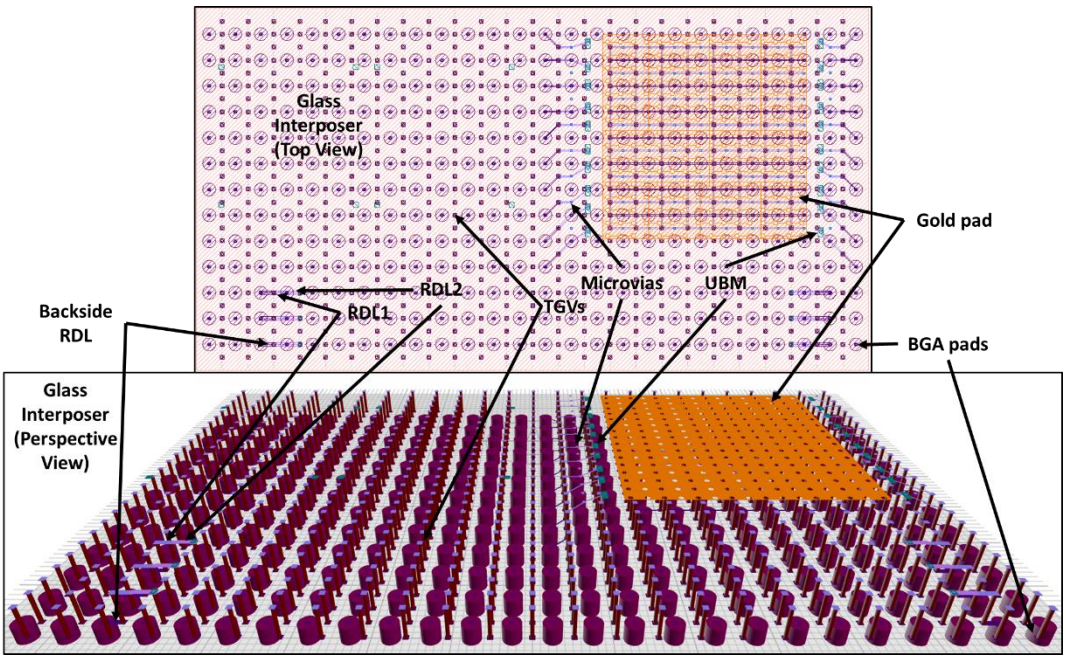


Figure 7.14: Design of the glass interposer with different components for co-packaging reference chips on the glass interposer. These components such as UBM, microvia, RDL2, RDL1, TGVs, Backside RDL and BGA facilitate the electrical and thermal connections from the top to the bottom of the glass interposer. The glass interposer also consists of two polyimide layers on the top and one polyimide layer on the bottom, this architecture is explained in detail earlier (refer Chapter 4).

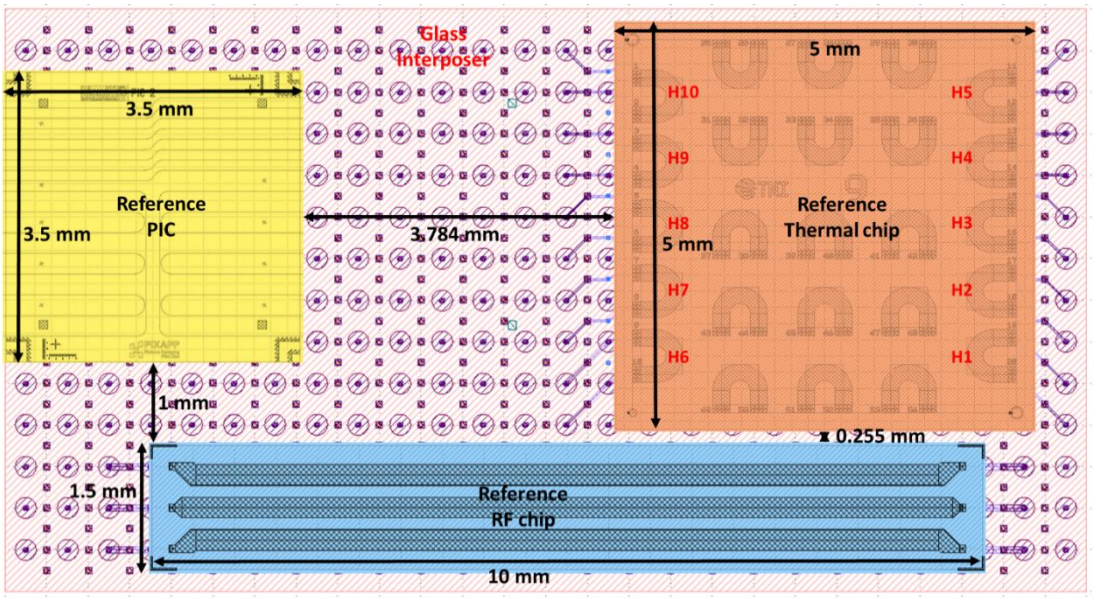


Figure 7.15: Design of the glass interposer with the positions of the reference PIC, reference thermal chip and reference RF chip bonded on the glass interposer, with reference PIC positioned at the edge of the interposer. The reference thermal chip is thermally active as it is powered through the heater loopbacks on the chip, marked as H1-H10 in the figure.

The reference chips bonded on the glass interposer using SAC305 solder for first level interconnection in **Figure 7.16**.

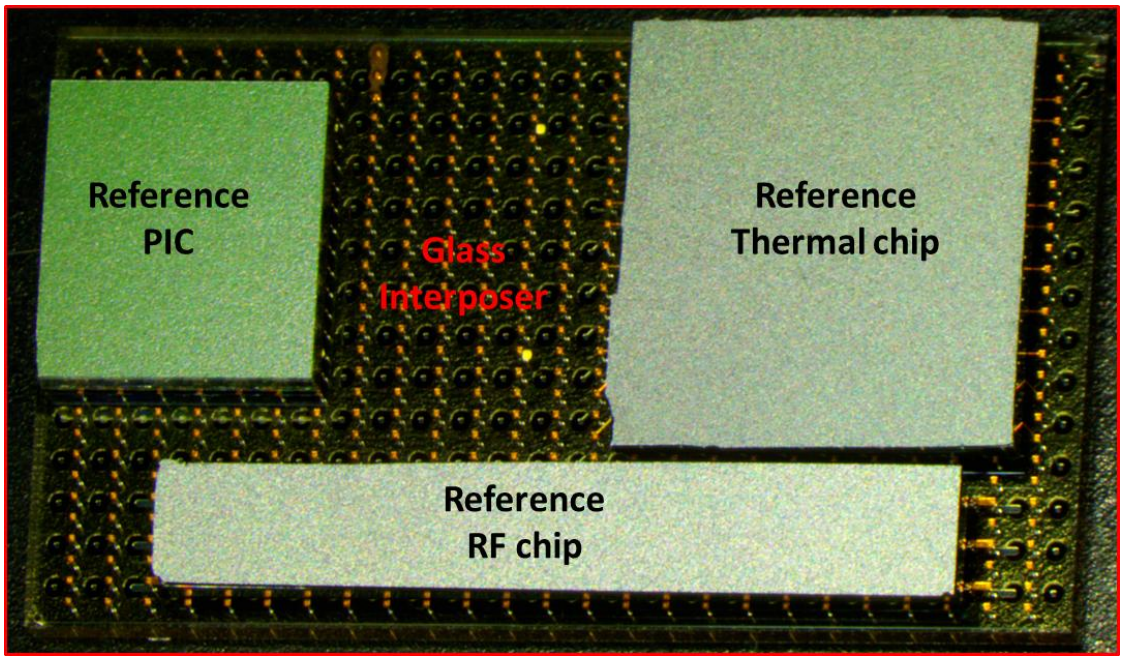


Figure 7.16: Subassembly consisting of the reference PIC, reference thermal chip and reference RF chip bonded on the glass interposer using simultaneous SAC solder reflow for all the chips, with reference PIC positioned at the edge of the interposer.

This subassembly in **Figure 7.16** with the glass interposer is then bonded on the PCB using BiSn solder to form the second level interconnection in **Figure 7.17**.

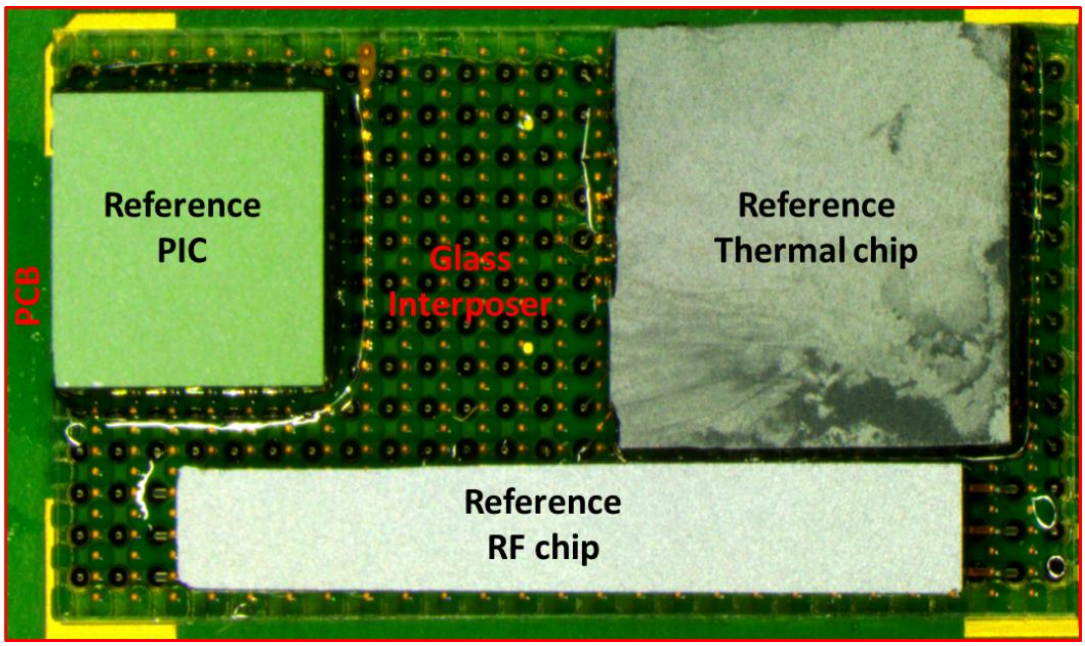


Figure 7.17: Assembly consisting of the reference PIC, reference thermal chip and reference RF chip bonded on the glass interposer, which is then bonded on the PCB using BiSn solder reflow to connect the subassembly to the PCB, with the reference PIC positioned at the edge of the interposer.

The assembled package for thermal characterization is shown in **Figure 7.18**. In the package, the DC connectors are used to give power/ground connections to the heater line loopbacks on the reference thermal chip. Secondly, the RF connectors are used for measuring the RF transmission in the glass interposer and reference RF chip. In this case, we are powering up the different heater line loopbacks in a sequential manner (which are emulating the hotspots on the chip) using the DC connectors and measuring the maximum surface temperature across the backside of all the reference chips at different input powers (81.33, 375.4 and 903.3 mW) of the heater line loopbacks.

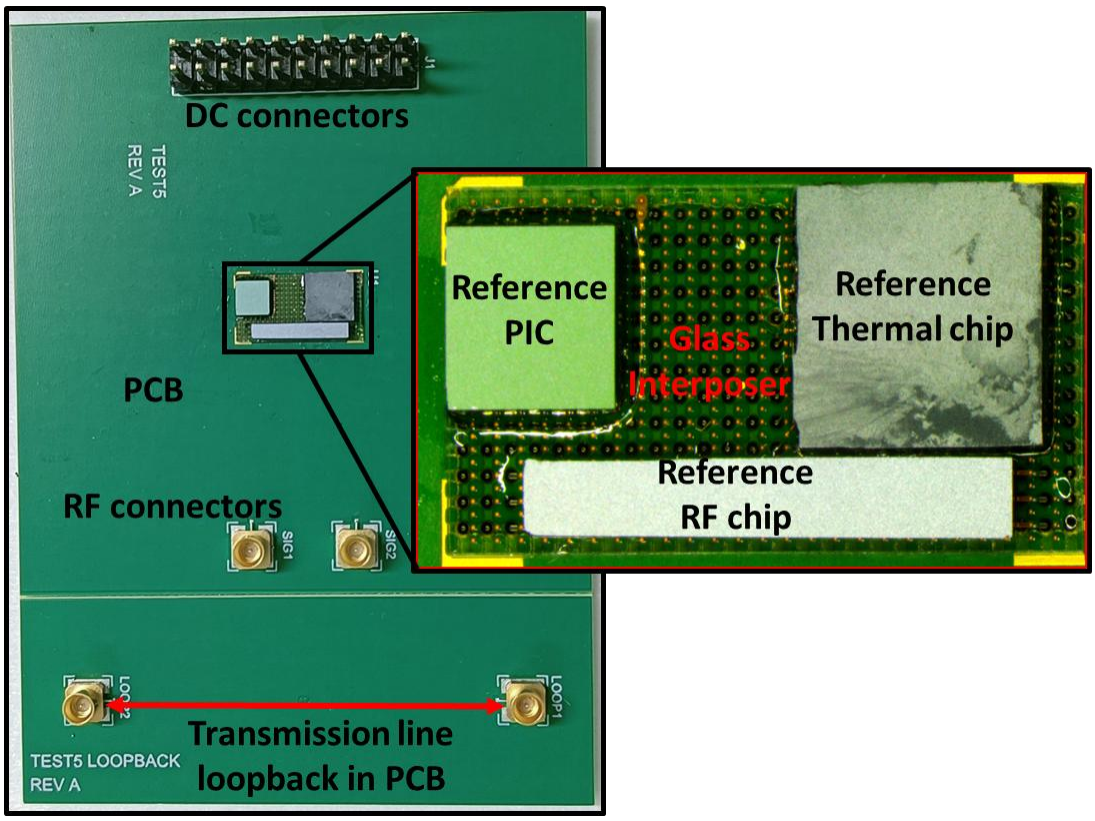


Figure 7.18: Final assembly of the co-packaged reference chips, with reference PIC positioned at the edge of the interposer. This assembly is used for thermal characterization to see the impact of the TGVs in glass interposer on thermal crosstalk between the reference chips.

The thermal measurements are conducted with the IR microscope FLIR X6540sc. The package is placed on a copper block with an integrated TEC where the temperature of the copper block surface is set at 20ºC using a TEC controller. This is then followed by powering up the heater line loopbacks on the reference thermal chip (H1 to H10) sequentially. The steady-state thermal measurement when H6 is powered up to 903.3mW is shown in **Figure 7.19**. The transient effect of powering up H6 heater loopback in the reference thermal chip on the reference PIC and reference RF chip is also shown in **Figure 7.20**.

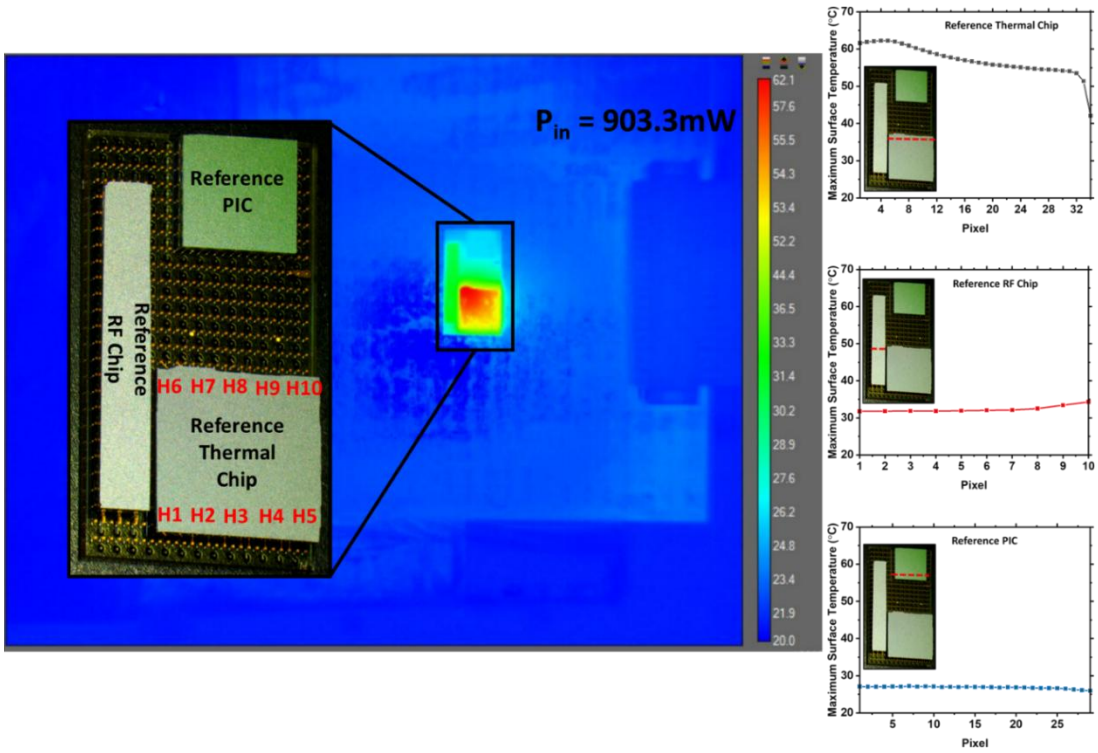


Figure 7.19: The steady-state IR thermal measurement of the co-packaged reference chips along the horizontal axis marked for reference thermal chip, reference RF chip and reference PIC; when the heater loopback H6 is powered to 903.3 mW, with reference PIC positioned at the edge of the interposer. The variation in temperature across the horizontal marked lines for the reference thermal chip, reference RF chip and reference PIC is dependent on the position of the operational heater loopback (on reference thermal chip).

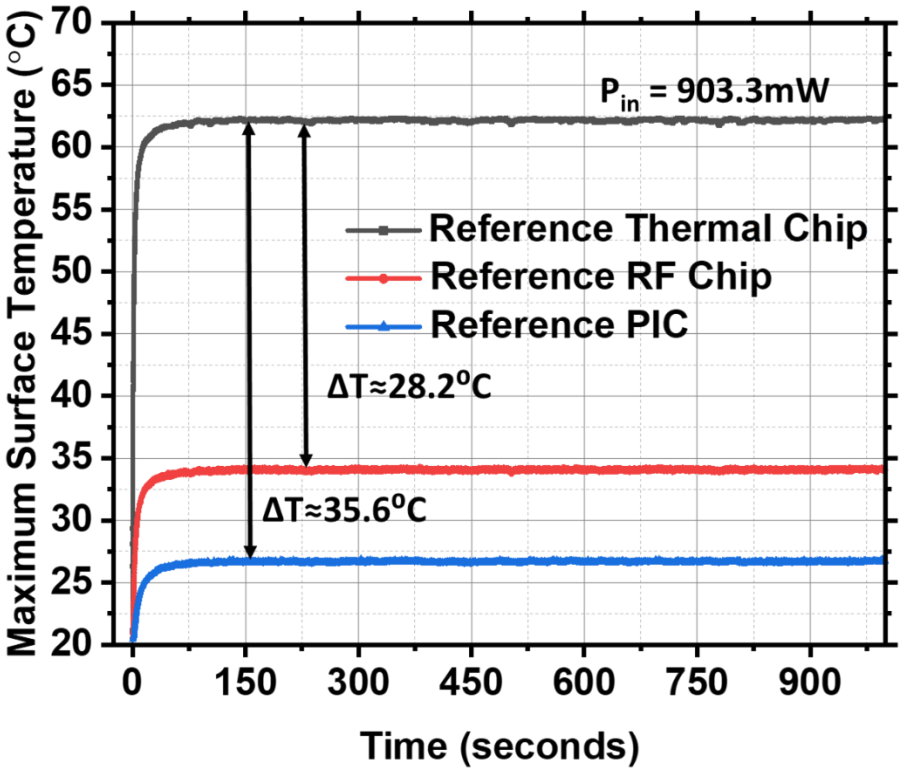


Figure 7.20: The transient IR thermal measurement of the co-packaged reference chips along the horizontal axis when the heater loopback H6 is powered to 903.3 mW, with reference PIC positioned at the edge of the interposer. The presence of TGVs in the glass interposer led to low thermal crosstalk with the difference in maximum temperatures of the reference chips ranging from approximately 28ºC to 36ºC.

Particularly for H6, we can clearly see the temperature difference between the reference thermal chip and reference RF chip of 28.2ºC. The temperature difference between the reference thermal chip and reference PIC of 35.6ºC. This temperature difference is influenced by the thermal crosstalk between the reference chips when there are 675 TGVs spread out across the glass interposer. The thermal crosstalk is low because the in-plane effective thermal conductivity of TGVs (1.211 W/m.K) is approximately 55% lower than the out-of-plane effective thermal conductivity of the TGVs (2.7129 W/m.K) in the glass interposer.

This thermal crosstalk is also seen when different heater loopbacks (H1-H10) are powered up at three different input powers of 81.33mW, 375.4mW and 903.3 mW. At these applied input powers, the maximum surface temperatures of the reference thermal chip, reference RF chip and reference PIC are shown in **Figure 7.21**.

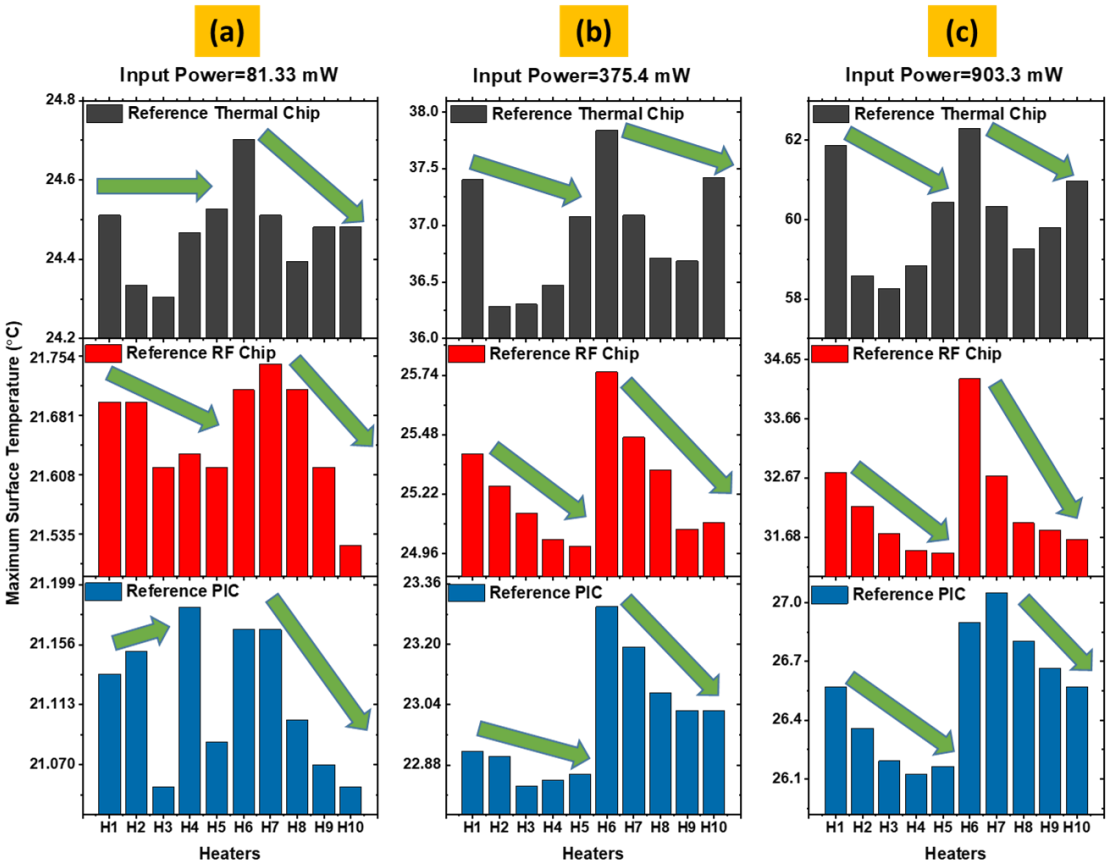


Figure 7.21: The dependence of the maximum surface temperatures of the reference PIC at the edge of the interposer and reference RF chip on the different heater loopbacks in the reference thermal chip (H1-H10) being operated at different powers generated by the heaters (a) 81.33mW, (b) 375.4mW and (c) 903.3mW. The thermal crosstalk between the reference thermal chip, reference RF chip and reference PIC is highlighted with the same temperature variation trend across all input powers.

As the input powers increase from **Figure 7.21(a)** to **Figure 7.21(c)**, the increase in maximum surface temperature is seen in all the reference chips. The reference thermal chip undergoes the highest increase in temperature with increasing input power (as it is the hotspot source), which is followed by the reference RF chip due to its proximity with the hotspot sources and the least increase in maximum surface temperature is visible in the reference PIC due to the higher spacing between the reference thermal chip and reference PIC.

The change in maximum surface temperature in the reference thermal chip when the heater loopbacks are powered up is also dependent on the location of the heater loopback. This is shown through the higher temperatures of H1, H5, H6 and H10 due to the presence of these heater loopbacks at the corners of the silicon chip [4]. This

phenomenon is also observed when there is a decrease in the maximum temperature of the reference RF chip and reference PIC as the hotspot source is changed from H1 to H5. This decrease is explained due to the increase in spacing between the hotspot source (on the reference thermal chip) and reference RF chip/PIC as we move from H1 to H5. Similarly, the maximum temperatures of the reference RF chip/PIC go through a second drop as we move from H6-H10 due to the proximity effect explained already. The maximum temperatures of reference RF chip and reference PIC are higher (when the heater loopbacks H6-H10 are operated) as compared to the maximum temperatures of reference RF chip and reference PIC when the heater loopbacks H1-H5 are operated due to the lower distance between hotspot source and thermally passive reference chips.

This effect of the location of the hotspot source clearly shows that the thermal design of the EIC (reference thermal chip mimics its thermal operation) is quite essential to enable the efficient optical operation of the photonic chip.

Key Takeaways:

- The hotspot sources on the EIC should be designed such that it minimizes the thermal crosstalk between EIC and PIC through the interposer, especially in cases with large number of vias between EIC and PIC in the interposer and no heatsink present in the PCB.

7.5 Electrical Design of TGVs

7.5.1 Diameter and Pitch of TGVs

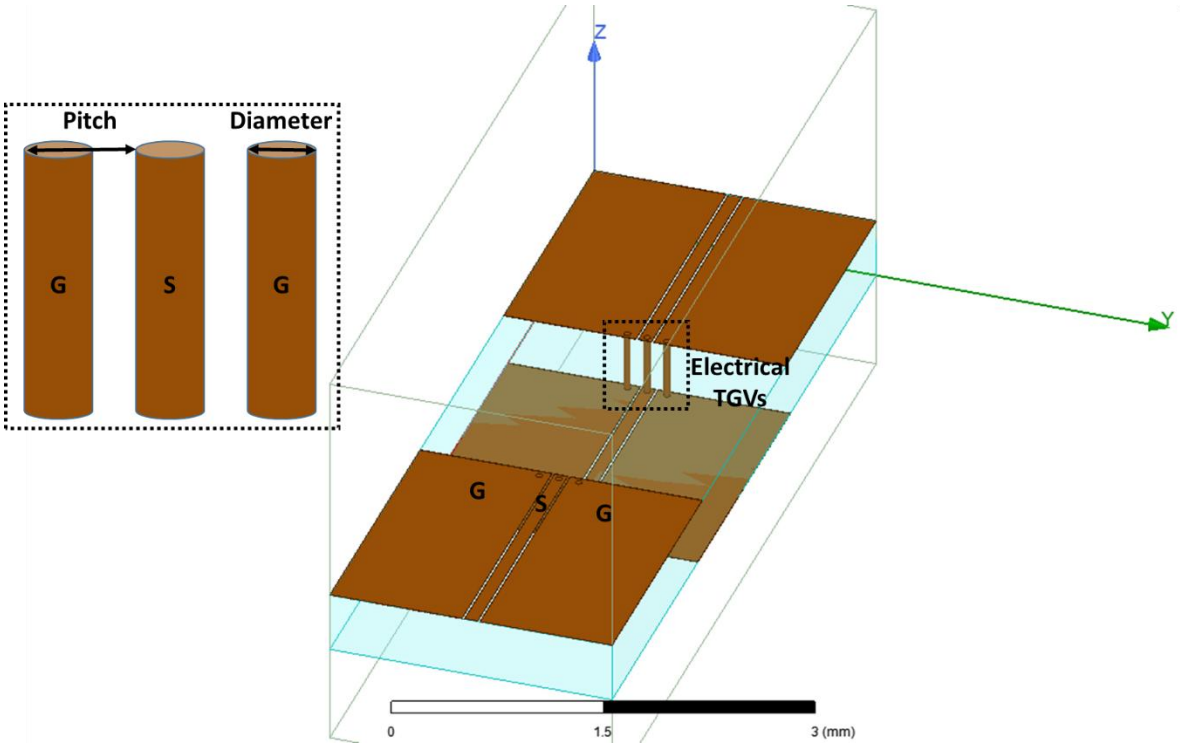


Figure 7.22: The simulation model of the CPW transmission line loopback with three cylindrical TGVs (Ground-Signal-Ground) connecting the ground and signal lines.

The electrical design of TGVs is studied through the vertical interconnection between GSG coplanar transmission lines on top-bottom-top of the glass interposer as a loopback structure. The coplanar transmission line has a signal line width of 100µm and the gap between the signal line and ground is 18µm, targeting the characteristic impedance of 50Ω. The TGVs are assumed to be cylindrical to reduce the parasitic losses due to the via taper in **Figure 7.22**.

The starting parameters for the signal and ground TGV diameter is 50µm and the starting parameter for the pitch between signal and ground TGV is 150µm. This diameter and pitch are varied from 50µm to 90µm and 150µm to 500µm respectively. The impact of this changing diameter and pitch on the insertion loss of the loopback is shown in **Figure 7.23**. Due to the low dielectric constant and high resistivity of glass, the conductance of glass does not have a significant impact on the characteristic impedance and loss of TGVs. The increase in the diameter of signal and ground TGVs at a given pitch leads to a decrease in inductance and resistance of the TGV [5].

This decrease in inductance and resistance is comparable and hence we see a small decrease in insertion loss (a maximum of 2.8dB at 40 GHz for the highest pitch of 500µm from **Figure 7.23(a)** to **Figure 7.23(e)**). This decrease in insertion loss becomes lower at smaller pitches.

On the other hand, as the pitch between the signal and ground TGVs increases, the inductance increases, and capacitance decreases logarithmically [5]. This logarithmic change leads to a larger impact of the increasing pitch on the increase in insertion loss. As seen in **Figure 7.23**, for a given diameter, the insertion loss increases as the pitch between the signal and ground TGV increases because of the decrease in mutual inductance between TGVs [6]. The interesting case appears when the TGV diameter increases to 80 and 90 µm when the insertion loss for smaller pitches tend to increase. This trend is also highlighted in the contour plot. This is due to the combined increase in mutual inductance and mutual capacitance of the TGVs.

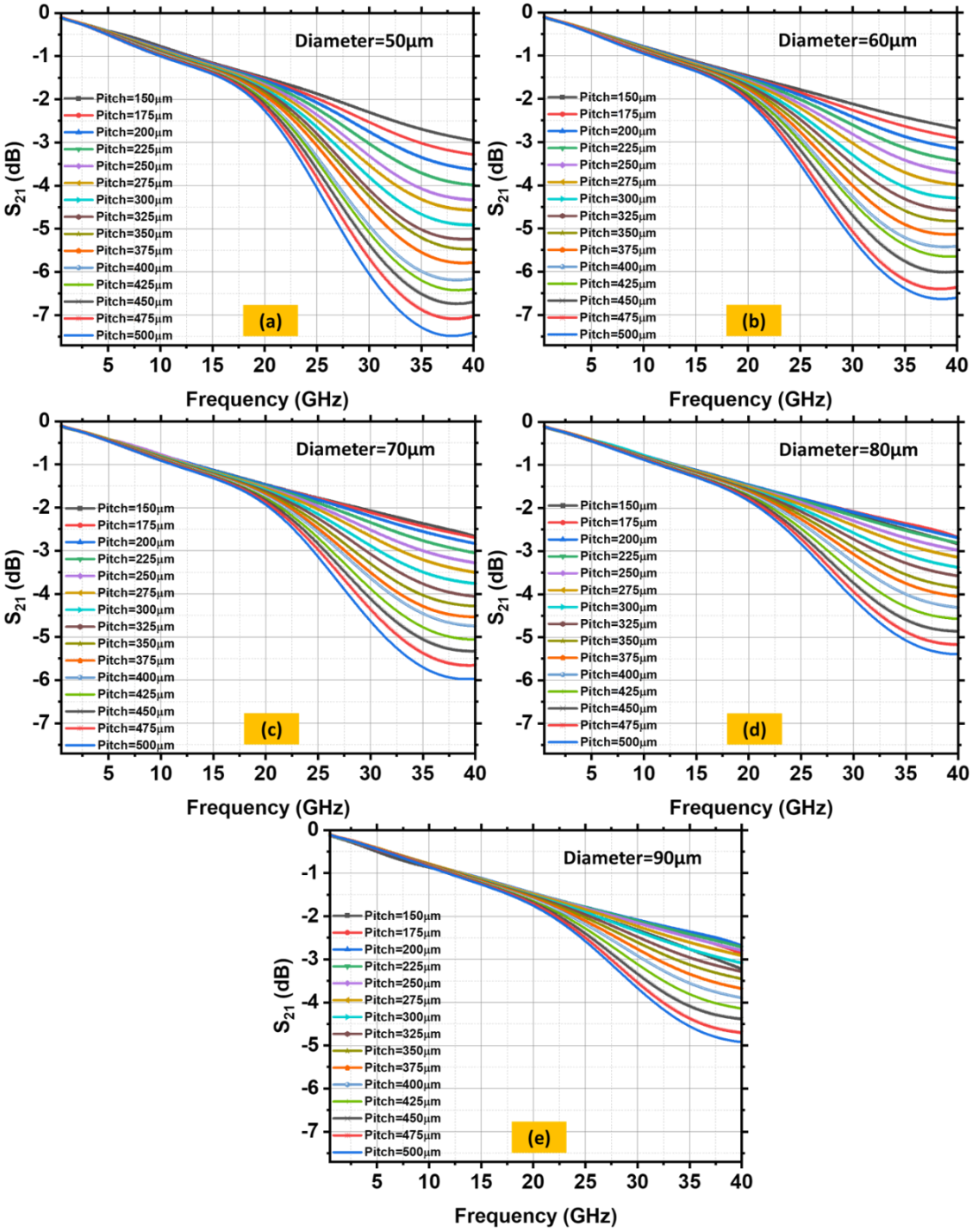


Figure 7.23: The variation of insertion loss of the CPW transmission line loopback with changing signal and ground TGV diameters (a) 50µm, (b) 60µm, (c) 70µm, (d) 80µm and (e) 90µm and changing pitch (150µm-500µm) for each of these TGV diameters. As the TGV diameter increased from (A) 50µ to € 90µm, the variation of the insertion loss at higher frequency starts getting lower and shows a trade-off when choosing the appropriate pitch for the maximum diameter.

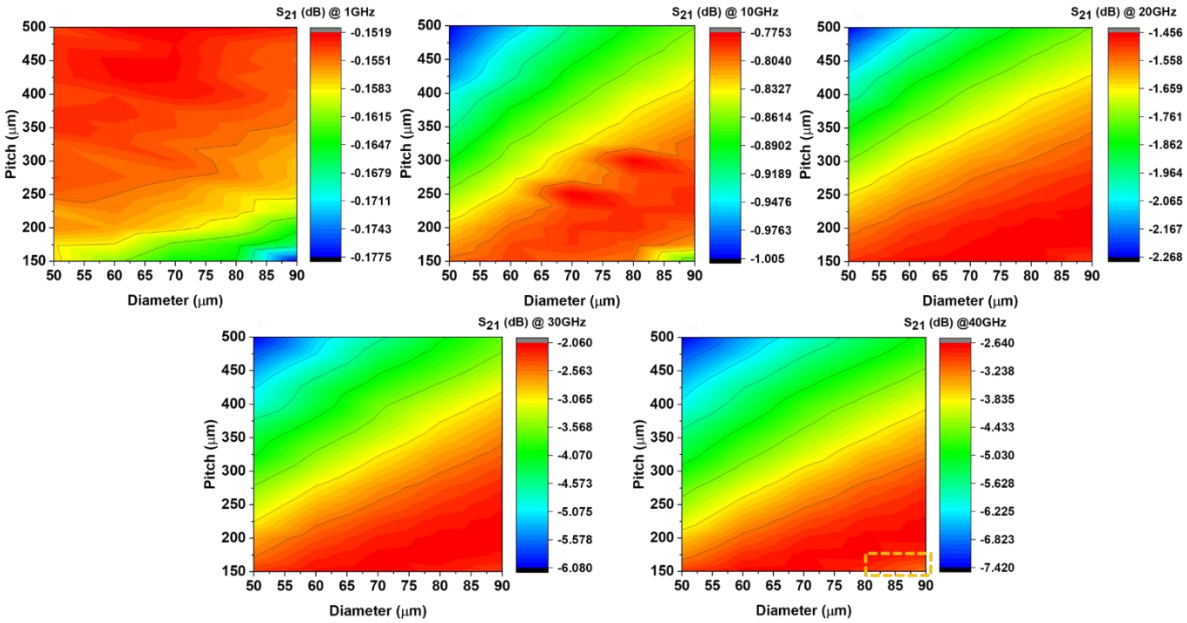


Figure 7.24: The contour plots showcasing the insertion loss of the CPW transmission line for varying TGV diameters and pitches at different frequencies like 1GHz, 10 GHz, 20 GHz, 30 GHz and 40 GHz. The challenge which arises with increased mutual capacitance and mutual inductance of the signal and ground TGVs is highlighted in the contour plot for insertion loss at 40 GHz.

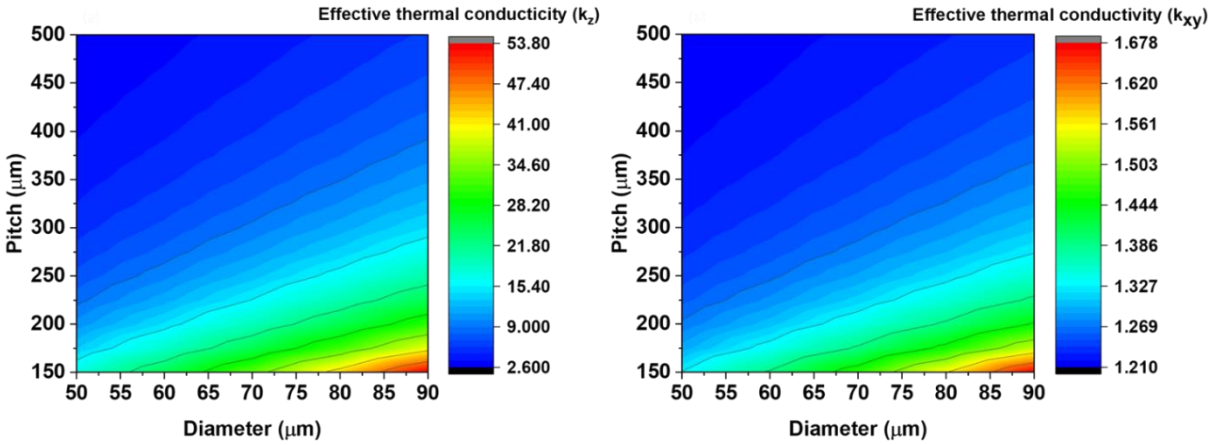


Figure 7.25: The contour plots showcasing the change in effective out-of--plane and in-plane thermal conductivities of the TGV with changing diameter and pitch of the TGVs.

The change in insertion loss with diameter of TGVs and pitch between TGVs is the lowest at 1 GHz and it progressively increases up to 40 GHz primarily due to conductor losses. As seen from the contour plots, increasing the diameter and lowering pitch of TGVs leads to lower losses in signal transmission. In addition to this, the effective in-plane and out-of-plane thermal conductivities of the TGV become higher at larger diameter and smaller pitch.

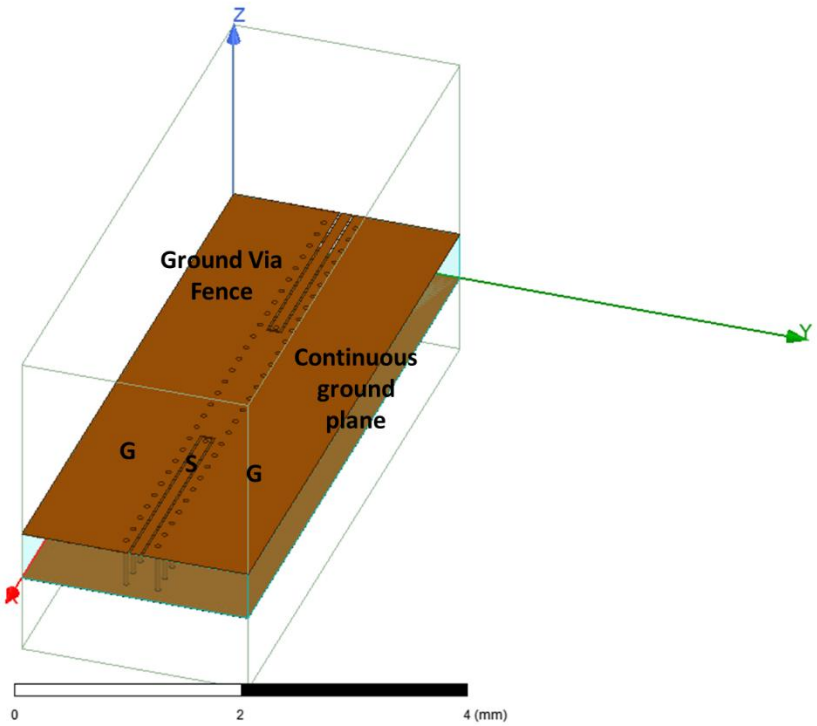


Figure 7.26: The simulation model of the CBCPW transmission line loopback with cylindrical TGVs connecting the ground and signal lines. The ground TGV fence along the loopback connects the continuous ground planes on top and bottom of the glass interposer.

In order to further lower the signal losses certain design changes such as incorporating a continuous ground plane or return path underneath the signal lines on both sides of the glass interposer and ground fencing vias with a ground via-ground via pitch of 200 µm are made. The pitch between the signal via and the ground vias is varied, as seen in **Figure 7.27**. We still see the effect of the range of S_{21} values (range of S_{21} with pitch variation from 150µm to 500µm) becoming lower with increasing diameter up to 80µm diameter but the increase in mutual inductance and mutual capacitance between signal and ground TGVs impose a trade-off between the ideal diameter and pitch for a given structure in **Figure 7.27**.

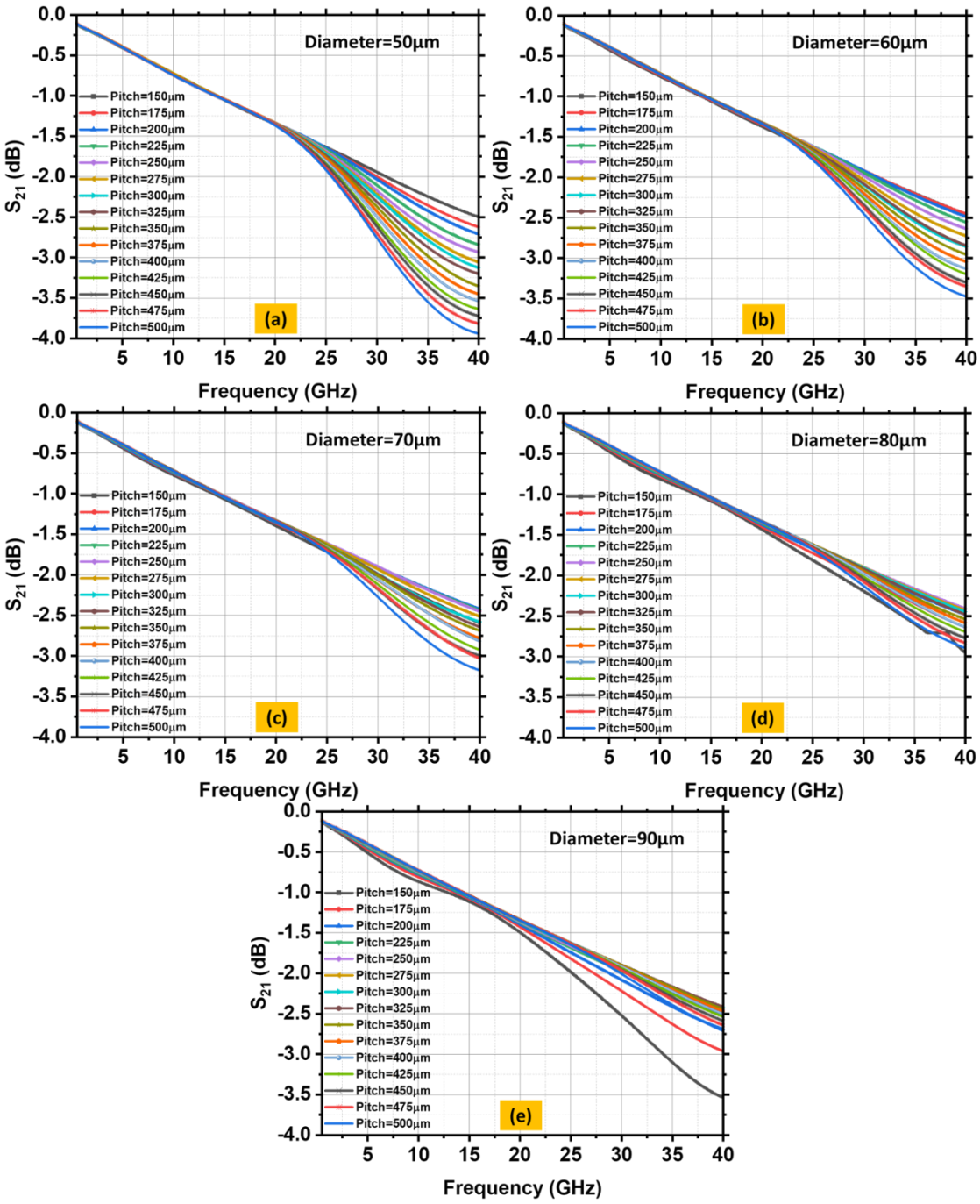


Figure 7.27: The variation of insertion loss of the CBCPW transmission line loopback with TGV ground fence with changing signal and ground TGV diameters (a) 50µm, (b) 60µm, (c) 70µm, (d) 80µm and (e) 90µm and changing pitch (150µm-500µm) for each of these TGV diameters showing a trade-off when choosing the appropriate pitch for the maximum diameter. The variation in the insertion loss at higher frequencies for increasing diameter from (a) 50µm to (e) 90µm with different pitches gets lower and the trade-off between maximum diameter and pitch exists to achieve low-loss transmission.

7.5.2 Height and Shape of TGVs

The height of the TGVs connecting the signal/ground lines on the top and bottom of the glass interposer is varied from 100µm to 500µm in **Figure 7.28(a)**, and the TGV diameter, signal-ground TGV pitch and ground-ground TGV pitch is kept constant at 50µm, 150µm and 200µm respectively. The increase in height of the TGVs lead to an increase in the inductance, resistance, conductance and capacitance [5]. This translates to an increase in TGV impedance with increase in resistance, inductance, and a decrease in TGV impedance with an increase in capacitance and conductance. In the case of glass interposers, the effect of inductance and resistance overpowers the increase in capacitance with an increase of height, thus leading to an increase in the insertion loss at high frequencies [7]. There is a visible increase of 0.5 dB insertion loss at 40 GHz frequency when the TGV/substrate height is increased from 100µm to 500µm. The vias are modelled as cylindrical structures in the simulation. Similarly, the heat dissipation is studied through a COMSOL® model, with a silicon chip bonded on the glass interposer with copper filled thermal vias placed underneath the chip. This model includes a PCB in **Figure 7.28(b)** and copper heat sink in **Figure 7.28(c)** bonded to the glass interposer. The effect of varying TGV/substrate height when the TGV diameter and pitch are kept constant at 50µm and 150µm is shown in **Figure 7.28(b)** and **Figure 7.28(c)**. The silicon chip is uniformly powered at 1W.

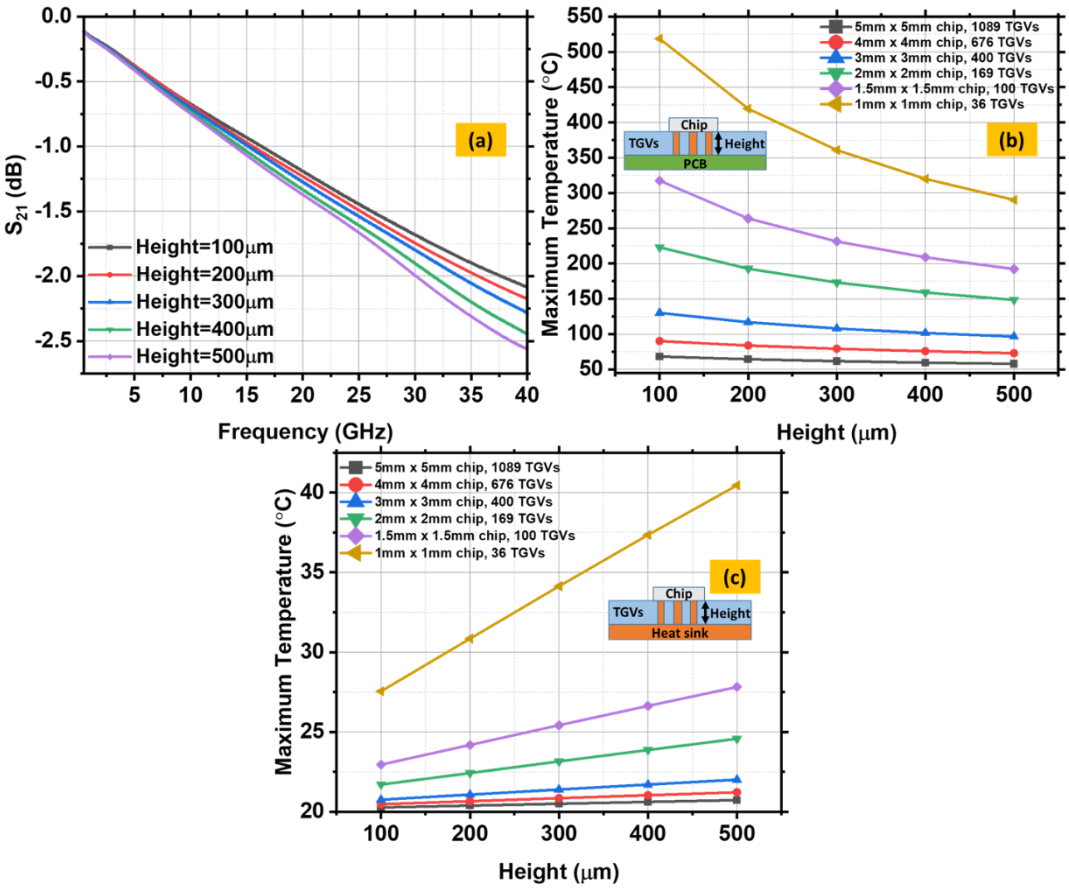


Figure 7.28: (a) Insertion loss of CBCPW transmission line loopback with ground fence when the TGV and glass substrate height is changed from 100μm to 500μm, (b) showing the change in maximum temperature of a chip bonded on the glass interposer (with PCB underneath) and (c) showing the change in maximum temperature of a chip bonded on the glass interposer (with copper heat sink underneath) when the chip size and the corresponding number of TGVs under the chip is changed. The TGVs are assumed to be cylindrical in these cases.

The increase in TGV height with PCB under the glass interposer leads to a decrease in the maximum chip temperature. This is due to the higher lateral thermal resistance with decreasing interposer height [8]. However, the increase in TGV height with copper heat sink under glass leads to an increase in thermal resistance which results in an increased maximum temperature of the chip. This maximum chip temperature increases by only 2.247% when the chip area is 25 mm^2 whereas it rises by approximately 46.85% when the chip area is decreased to 1 mm^2. Thus, a decrease in the glass substrate/TGV height leads to lower losses in signal transmission and better thermal performance with heat sink bonded under the glass interposer.

In addition to this, the shape of the TGV also impacts the signal transmission and thermal dissipation performance of the glass interposer. The hyperbolic shape of the TGV involves a taper, and the taper angle of the TGV is varied by varying the middle section diameter of the TGV. The middle diameter of the hyperbolic TGV is varied from 25µm to 50µm which equates to the taper angle changing from 86.89º to 90º. The upper diameter, lower diameter, pitch and height of the TGVs are kept constant at 50µm, 50µm, 150µm and 500µm respectively. We can clearly see in **Figure 7.29(a)**, an approximately 0.75dB improvement in the insertion loss as the shape of the TGV changes from hyperbolic to cylindrical for the loopback structure with no continuous ground plane and no ground fence TGVs. There is also an approximately 0.5 dB improvement in the insertion loss with lowered tapering of the TGVs in case of the structure with continuous ground plane and ground fence TGVs (**Figure 7.29(b)**). The thermal performance of the glass interposer also becomes worse when the TGVs are increasingly tapered when comparing **Figure 7.28(b)** and **Figure 7.29(b)**. The maximum temperature of the chip decreases by approximately 2.4% when the chip area is 25 mm^2 and the maximum chip temperature decreases by 25% when the chip area is 1 mm^2. This is due to the increased volume of glass as compared to copper that deteriorates the thermal performance, especially for the smaller chip areas (less than 1.5×1.5 mm^2 area).

Key Takeaways:

- High diameter and low pitch of TGVs can successfully lower insertion loss of a conductor backed coplanar GSG structure; however, a certain trade-off occurs where we need to tune the suitable pitch for the highest via diameter due to mutual inductive and capacitive parasitics.
- Reducing impedance discontinuity along the signal path where a continuous ground plane and ground fence vias, which can suppress higher order modes, are recommended.
- Lowering the glass interposer/TGV height and reducing the taper along the via sidewalls for the hyperbolic TGVs can improve signal transmission and heat dissipation through the glass interposer.

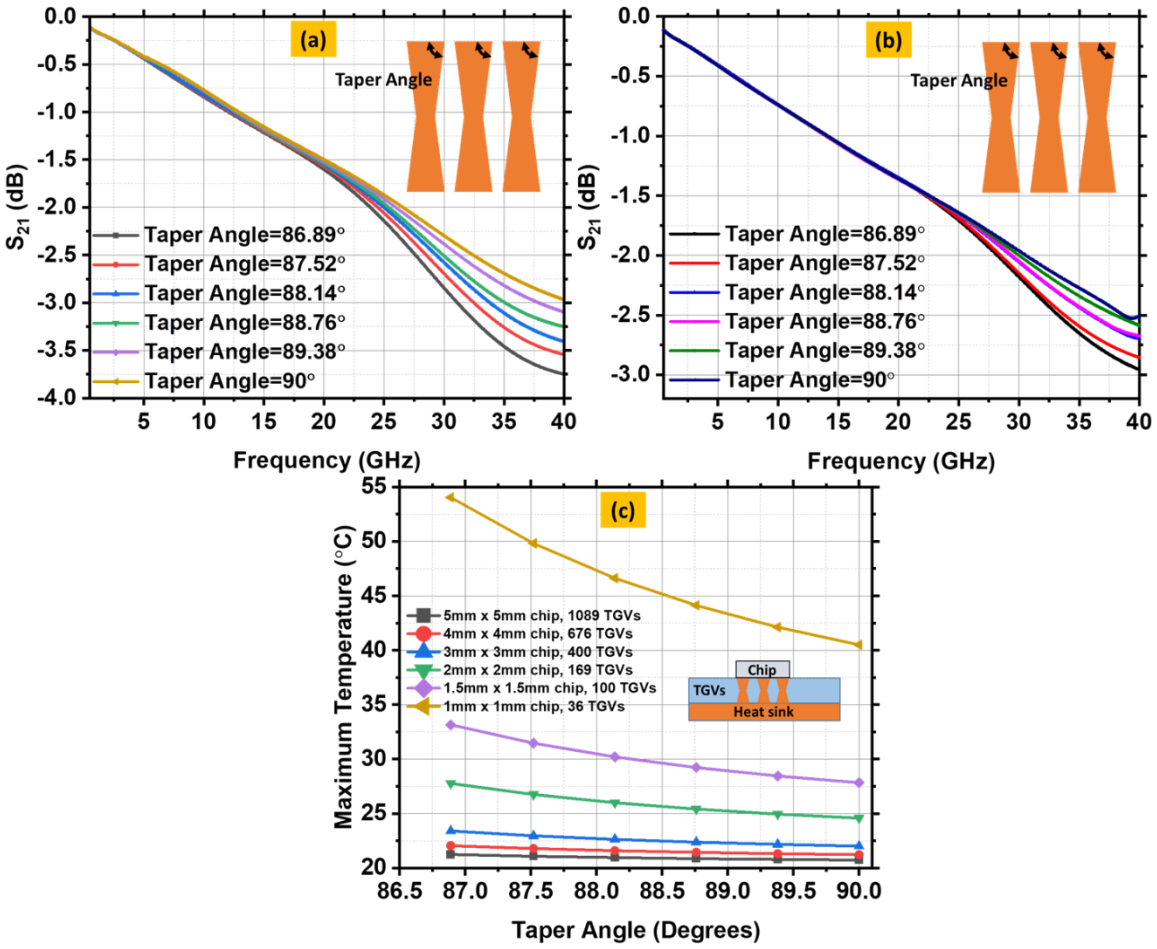


Figure 7.29: (a) Insertion loss of CPW transmission line loopback with no backside ground and no ground fence for increasing taper angle of the signal/ground TGVs, (b) Insertion loss of CBCPW transmission line loopback with backside ground and via ground fence for increasing via taper angles and (c) showing the change in maximum chip temperature when the chip size, number of TGVs under the chip are changing for different TGV taper angles.

7.6 Conclusion

The design guidelines recommended for the chips/glass interposer designers are analyzed and elaborated. These design guidelines are also summarized below.

	TGVs		PCB	
	Thermal	**Electrical**	**Thermal**	**Electrical**
Laser chip	Honeycomb pattern	DC connections	-	-
EIC	• High diameter, Low Pitch • Design the EIC hotspot producing areas such that it is at a larger distance from the temperature sensitive optical elements on the PIC • Lower TGV height/interposer thickness (with heat sink) and lower taper along the sidewalls of the TGV	• Trade-off between suitable pitch for high diameter • Lower TGV height/interposer thickness (with heat sink) and lower taper along the sidewalls of the TGV	• Add heat sink or micro-TEC in the PCB • Right selection of thermal interface materials and underfills	• Signal discontinuities such as solder connections and underfill materials should be chosen correctly • Appropriate design of PCB interconnects
PIC	• Low diameter, High Pitch (No heat sink in PCB) • High diameter, Low Pitch (With heat sink in PCB) • Design the thermally sensitive areas of the PIC away from the	• Trade-off between suitable pitch for high diameter • Lower TGV height/interposer thickness (with heat sink) and lower taper along	• Add heat sink, micro-TEC in the PCB • Prevent the underfill/thermal interface material to reach the	• PCB design to be controlled such that space is left for external optical connections (eg. Micro-lenses and fiber array)

	EIC's hotspot location ● Lower TGV height/interposer thickness (with heat sink) and lower taper along the sidewalls of the TGV	the sidewalls of the TGV	sensitive optical facets of the PIC	

The honeycomb pattern arrangement of thermal TGVs are recommended under the laser chip to allow effective heat dissipation. Secondly, the largest TGV diameter and smallest TGV pitch (according to the fabrication process) under the EIC as well as smallest TGV diameter and largest pitch under the PIC is recommended when there is no heat sink in the PCB. In cases where the heat sink is used (both in PCB and directly contacting the thermal vias), largest TGV diameter and smallest TGV pitch is recommended. This is done to allow for heat dissipation from the EIC and lower thermal crosstalk between the EIC and PIC. This requirement of the heat sink is actually the motivation for ongoing research to integrate vapor chambers and liquid cooling structures in the PCB for efficient heat dissipation, but it depends on the cooling requirements of the optical package in conjunction with its ability to integrate with the system-level cooling requirements for appropriate heat rejection. The interposer layout designers can choose the appropriate configuration (with or without heat sink), depending on the allowed temperature range for optimal chip operation.

Thirdly, the hotspot management when designing the electronic chip is essential especially when there are TGVs present in the spacing between the EIC and PIC in the glass interposer. This also impacts the spacing between the EIC and PIC in 2.5D glass based photonic packages to manage crosstalk.

Lastly, the trade-off between TGV diameter and pitch is highlighted in the coplanar configuration (especially when the TGV diameter is increased, the layout designer needs to find an appropriate pitch) to minimize the insertion loss. Additionally, the height of the TGVs/glass interposer and taper of the TGVs need to be lowered for low-

loss electrical transmission and lower thermal resistance (in the presence of a heat sink under the glass interposer).

7.7 References

[1] Y. Shen, H. Wang, F. Blaabjerg, H. Zhao and T. Long, "Thermal Modeling and Design Optimization of PCB Vias and Pads," in IEEE Transactions on Power Electronics, vol. 35, no. 1, pp. 882-900, Jan. 2020, doi: 10.1109/TPEL.2019.2915029.

[2] P. Gupta et al., "Impact of Through Glass Vias Filling on the Performance of Passive Thermal Cooling in Photonic Packages," 2022 IEEE 9th Electronics System-Integration Technology Conference (ESTC), Sibiu, Romania, 2022, pp. 391-397, doi: 10.1109/ESTC55720.2022.9939531.

[3] S. Cho, V. Sundaram, R. R. Tummala and Y. K. Joshi, "Impact of Copper Through-Package Vias on Thermal Performance of Glass Interposers," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 5, no. 8, pp. 1075-1084, Aug. 2015, doi: 10.1109/TCPMT.2015.2450731.

[4] P. Gupta et al., "Reference Thermal Chips for 2D and 3D Co-packaging Process Development," 2023 IEEE 73rd Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 2023, pp. 2160-2165, doi: 10.1109/ECTC51909.2023.00372.

[5] J. Kim et al., "Precise RLGC modeling and analysis of through glass via (TGV) for 2.5D/3D IC," 2015 IEEE 65th Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2015, pp. 254-259, doi: 10.1109/ECTC.2015.7159601.

[6] W. Li et al., "General Analytical Method for Investigating Parasitic Characteristics of Through Glass Vias (TGVs) in 3-D Integration," in IEEE Transactions on Electron Devices, vol. 70, no. 9, pp. 4554-4559, Sept. 2023, doi: 10.1109/TED.2023.3299461.

[7] J. Tong, Y. Sato, K. Panayappan, V. Sundaram, A. F. Peterson and R. R. Tummala, "Electrical Modeling and Analysis of Tapered Through-Package via in Glass Interposers," in IEEE Transactions on Components, Packaging and

Manufacturing Technology, vol. 6, no. 5, pp. 775-783, May 2016, doi: 10.1109/TCPMT.2016.2545160.

[8] L. Qian, Y. Xia, G. Shi, J. Wang, Y. Ye and S. Du, "Electrical–Thermal Characterization of Through Packaging Vias in Glass Interposer," in IEEE Transactions on Nanotechnology, vol. 16, no. 6, pp. 901-908, Nov. 2017, doi: 10.1109/TNANO.2017.2722686.

Chapter 8: Conclusions and Future Work

This thesis focuses on thermal management strategies for co-packaged electronic and photonic chips on a glass interposer. The primary advantage of using a glass interposer in electronic-photonic 2.5D packages is the low thermal crosstalk between the electronic and photonic chips. Our research emphasizes on improving heat dissipation from electronic chips while maintaining minimal lateral heat conduction between the electronic and photonic chips in glass interposer packages. Initially, heat dissipation through the glass interposer is examined using Through-Glass Vias (TGVs). To establish a reliable heat source for studying heat conduction through the glass interposer, reference thermal chips are introduced. These reference chips serve as hotspot sources to analyze heat dissipation in glass interposers. Various thermal management strategies for the glass interposer, such as thermal TGVs and copper clips, are investigated using these reference thermal chips as heat sources. Additionally, a novel strategy called Substrate integrated micro-TEC (SimTEC), which involves TGVs partially filled with thermoelectric materials, is explored through simulations. The electrical transmission through glass interposers to enable the co-packaging of electronic chips and photonic chips is also studied in this thesis. Finally, design rules are derived based on the analysis of heat dissipation as well as electrical losses incurred in the glass interposer.

8.1 Contributions and Highlights

Key contributions and highlights made through this thesis include:

Chapter 1:

Introduction to Photonic Packaging

Photonic Packaging is presented, highlighting the integration of electronic and photonic chips through co-packaging on glass interposers. The electrical and mechanical benefits of glass interposers are also discussed. This establishes the motivation and objectives of the thesis, which aims to evaluate glass interposers for 2.5D photonic packages.

Fabrication of Glass Interposer

The processes involved in fabricating TGVs, RDLs, and interconnects are thoroughly explained. Chapter 4 also provides an in-depth look at the design, assembly, and characterization of these glass interposers.

Chapter 2:

Effectiveness of Thermal TGVs for Heat Dissipation

The heat dissipation performance of Through-Glass Vias (TGVs) is evaluated using a laser chip as the heat source. Integrating TGVs lowers the laser chip's temperature as it improves the lateral and vertical heat dissipation as compared to glass without TGVs. Note that thermal TGVs work especially well when the heat sources have a smaller area. (or larger heat flux density).

TGV Filling Sensitivity

The discrepancy between simulated and measured temperature results for TGVs is due to partial copper filling, which decreases the effective out-of-plane thermal conductivity of the TGVs from 94.78 W/m·K to 18 W/m·K.

Chapter 3:

Reference Thermal Chips

Reference Thermal Chips are used as heat sources to study heat dissipation in the glass interposer. Heater loopbacks of varying lengths are characterized as hotspots with different $\Delta T/\Delta P$ values. The $\Delta T/\Delta P$ is also examined when the reference thermal chips are stacked with reference PICs in both 2D and 3D configurations.

Thermal and Optical Characterization of Joule Heating Effect

The 3D configuration shows a higher $\Delta T/\Delta P$ for the PIC compared to the 2D configuration due to joule heating and thermal crosstalk. Additionally, a red shift in the central wavelength is observed for the optical coupling between the grating coupler loopback and fiber in the 2D and 3D stacked configurations, respectively.

Chapter 4:

Impact of Thermal TGV Pitch Variation

The impact of variation in thermal TGV pitch on heat dissipation through TGVs is evaulated through thermal test vehicle. The design, assembly and characterization of the theral test vehicle is also elaborated. The study finds that changes in TGV pitch have a limited impact on the thermal performance of the glass interposer once the effective out-of-plane thermal conductivity of the TGVs reaches a certain level. Experimental results indicate that reducing the TGV pitch below 100 μm results in only a slight increase in heat conduction through the glass interposer.

Importance of Heat Sink in PCB

The insignificant change in heat dissipation through TGVs beyond a certain point is attributed to the PCB, which has a larger volume for heat conduction but lower thermal conductivity compared to glass. The study underscores the importance of integrating a heat sink or micro-TEC into the PCB.

Electrical Losses in Glass Interposer

Additionally, the electrical performance of the glass interposer is examined through GSG structures in the electrical test vehicle. The electrical test vehicle consists of glass interposer (with CBCPW transmission lines, TGVs, microvias and BGA pads) bonded on the PCB. The study highlights that the design of TGVs, microvias and BGA pads is crucial for achieving an approximate 11 dB reduction in insertion loss for the electrical test vehicle.

Chapter 5:

Substrate integrated micro-TEC (SimTEC)

A novel structure called SimTEC is proposed for thermal stabilization in electronic-photonic packages. This structure incorporates Through-Glass Vias (TGVs) that are partially filled with copper and thermoelectric materials. SimTEC vias are compared to free-standing micro-TEC pillars with varying via parameters, highlighting the thermal losses associated with the incorporation of glass in SimTEC.

Application of SimTEC

The maximum change in ΔT achieved by varying the via parameters in SimTEC is 6.63 K, which is six times greater than the change achieved by varying the parameters

of micro-TEC pillars. The ΔT achieved through SimTEC can be further enhanced by improving the properties of the thermoelectric materials.

Chapter 6:

Copper Clip as Primary Heat Flow Path

In addition to the heat conduction path through the glass interposer, the primary heat flow path through the top of the electronic chip is examined using a copper clip. The copper clip demonstrates superior cooling performance as a heat spreader compared to TGVs and SimTEC.

Importance of Continuous Heat Flow Path from Copper Clip

It can be used in conjunction with TGVs and a heat sink/micro-TEC in the PCB for effective heat removal. The concept of an extended copper clip, which makes direct contact with the heat sink or cold plate, has been experimentally validated, showing a temperature reduction of 24°C.

Chapter 7:

Design Rules for Thermal TGVs

The honeycomb pattern of TGVs is particularly recommended for effective heat dissipation in high flux density devices like laser chips. When a heat sink is not integrated into the PCB, it is advisable to use the largest TGV diameter and smallest TGV pitch under the electronic chip, and the smallest TGV diameter and largest TGV pitch under the photonic chip. Conversely, if a heat sink or micro-TEC is integrated into the PCB, the largest TGV diameter and smallest TGV pitch should be used under both the electronic and photonic chips. Additionally, while TGVs distributed across the interposer demonstrate low thermal crosstalk between reference chips, managing hotspots becomes crucial. This involves floorplanning the hotspot sources on the electronic chip to minimize thermal crosstalk with the photonic chip.

Design Rules for Electrical TGVs

The balance between enlarging TGV diameter and reducing TGV pitch in a GSG configuration is emphasized, with TGVs serving as transition points between the top and bottom CPW lines. To minimize insertion loss, a shorter TGV/interposer height and a lower taper along the TGV sidewalls are preferred.

This work has delved into different thermal management strategies that can be interfaced/integrated with glass interposers, resulting in certain design guidelines. However, these thermal management strategies need a package-system interface to establish effective thermal management. In addition to this, thermal deviations in data center systems can induce reliability challenges in glass based packages. These reliability challenges need to be addressed as well. These endeavours can be explored through future studies.

8.2 Future Work

Combination of Package-Level and System-Level Heat Sink Mechanisms

Figure 8.1 illustrates how the maximum temperatures of the electronic chip (EIC) and photonic chip (PIC) vary with changes in the effective out-of-plane thermal conductivity of TGVs, as the thickness of the glass interposer is adjusted from 100 µm to 500 µm. The point at which the thermal performance of TGVs plateaus is influenced by the thickness of the glass interposer.

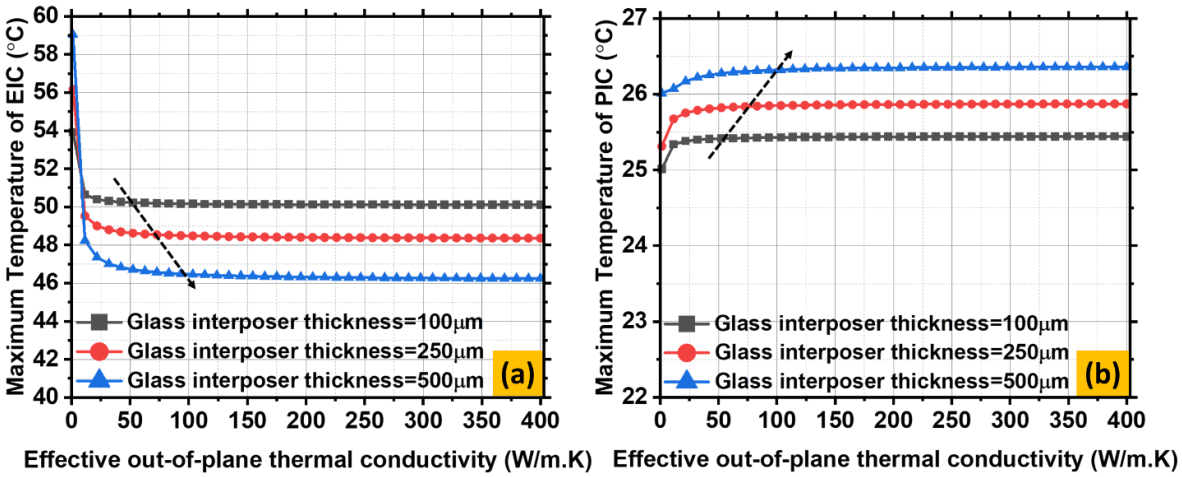


Figure 8.1: Maximum Temperature of (a) electronic chip and (b) photonic chip when the effective out-of-plane thermal conductivity of the TGV volume under the chips is varied from 1.2 W/m.K (glass) to 400 W/m.K (Copper). The variation in maximum temperature is simulated for different thickness of the TGVs/glass interposer 100, 250 and 500 µm. The simulation model is derived from Section 7.3 (Chapter 7).

The dependency on the thickness of the glass interposer can be mitigated by integrating a heat sinking or cooling mechanism within the PCB. Therefore, further research is needed on PCB cooling mechanisms that can be combined with system-level cooling solutions for photonic packages. This is crucial for integrating passive cooling solutions in glass interposer-based photonic packages (such as thermal TGVs

and copper clips) with active system-level cooling solutions. For active package-level cooling solutions like SimTEC, additional studies are necessary to optimize the thermoelectric material properties and fabrication processes to demonstrate SimTEC effectively. In PhotonicLEAP project, the learnings from this thesis will be utilized for design of glass interposer based photonic packages (EIC-PIC packages).
The heat sinking capabilities (both package-level and system-level) become essential to prevent heat accumulation in packages, which can lead to reliability concerns.

The design rules derived because of this thesis provide future directions towards exploration of synergy between package and system level cooling solutions for next-generation electro-optical transceivers in data centres.

Reliability Study of Glass Interposer Based 2.5D Photonic Packages

The reliability of glass interposer based photonic packages also need to be studied further. These studies become crucial owing to the reliability failures which can occur due to the CTE mismatch between glass and copper, as seen in **Figure 8.2**. The thermal cycling results show copper pumping out of glass due to its higher CTE. This can lead to reliability failures for RDL lines connected on top of the copper filled TGVs. For future work, a reliability study of TGVs is extremely important because it provides a necessary complement to thermal and electrical design considerations. The reliability of glass interposers can be significantly improved by selecting appropriate materials, optimizing thermal cycling conditions, and conducting thorough reliability testing. These studies provide valuable insights and guidelines for reducing the failure rate of glass interposers in advanced packaging technologies. Combining the reliability studies of glass interposer-based microelectronic packages with those of optical interfaces can provide a comprehensive case study.

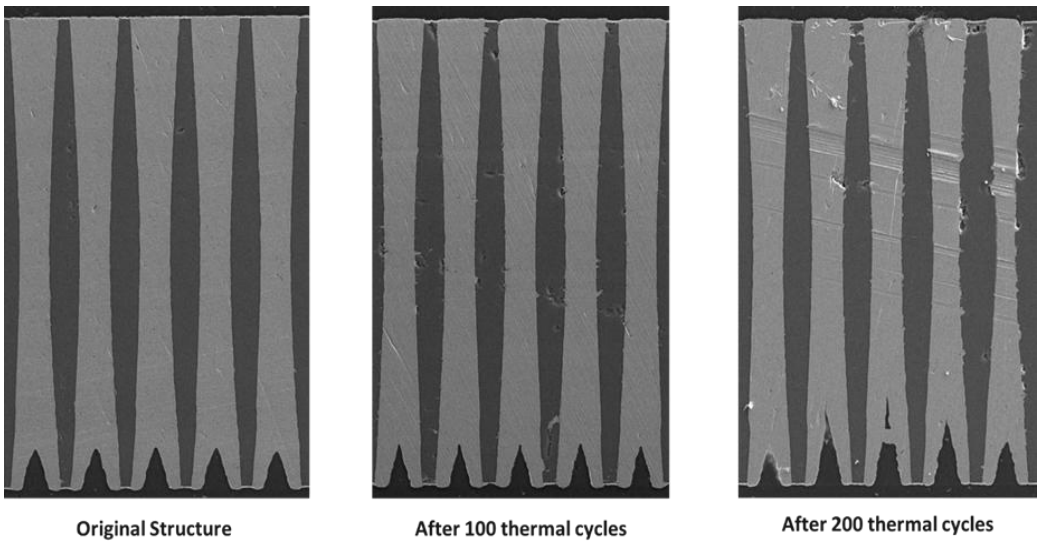


Figure 8.2: Thermal Cycling Test (TCT) was conducted on a set of samples with hyperbolic TGV structures in glass. The TCT was performed from -40˚C to 125˚C with a dwell time of 15 minutes for the maximum and minimum temperature. The rate of temperature change was fixed at 4˚C/minute. The results of the TCT samples before thermal cycling and samples after 100 and 200 thermal cycles.

Appendix A

S1: Glass Interposer Design for Thermal Characterization

The size of the different components in the glass interposer for thermal characterization is given in the **Table A.1** below:

Table A.1: Glass Interposer Design for Thermal Test

Component	Function	Diameter/ Pitch (µm)	Landing Pad/Trace size (µm×µm)
UBM	Serves as a barrier layer to prevent solder diffusion into the interposer	NA	200×200
Gold pad	Thermal spreading from chip to RDL2	NA	4200×5000
Microvia (2nd Polyimide layer)	Connect UBM to RDL2	40/300	70×90
RDL2	Connect UBM to RDL1	NA	25
Microvia (1st Polyimide layer)	Connect RDL2 to RDL1	35/200	45×45
RDL1	Connect RDL2 to TGV	NA	4500×5000
TGV	Connect RDL1 to BRDL	50/(100/200/300/400)	75×75
Backside RDL (BRDL)	Connect TGV to BGA	NA	4500×5000
Microvia (Backside Polyimide layer)	Connect BRDL to BGA pad	35/500	55×55
BGA pad	Connect glass interposer to PCB	250/500	NA

S2: Glass Interposer Design for Electrical Characterization

The size of the different components in the glass interposer for thermal characterization is given in the **Table A.2** below:

Table A.2: Glass Interposer Design for Electrical Test

Component	Function	Line/Space (µm)	Landing pad size (µm×µm)
RDL1	Signal line and ground	100/18 (Signal line width/gap)	NA
TGV	Connect signal/ ground from RDL1 to BRDL	50/(Signal-Ground 160/Ground-Ground 500)	75×75
Backside RDL (BRDL)	Connect TGV to BGA	100/18	NA
Microvia (Backside Polyimide layer)	Connect BRDL to BGA pad	35/500	55×55
BGA pad	Connect glass interposer to PCB	250/500	NA

S3: Assembly of thermal test vehicle

The reference thermal chip is initially bonded to the glass interposer employing SAC 305 solder. The reflow profile utilized for bonding the reference thermal chip onto the glass interposer via the Finetech flip-chip bonder is detailed in **Figure A.1**. This profile shows the temperature-time profile applied during the reflow process, ensuring proper bonding and reliability of the assembly.

After this initial reflow process, which bonds the reference thermal chip to the glass interposer using SAC 305 solder, the subassembly proceeds to a second reflow step. During this stage, the Bi-Sn solder is reflowed to bond the BGA pads of the subassembly onto the corresponding BGA pads of the PCB, as seen in **Figure A.2**.

Subsequently, the assembled structure is underfilled with epoxy material, followed by curing and characterization for thermal measurements. This process ensures proper bonding within the assembly, facilitating reliable performance and accurate thermal characterization.

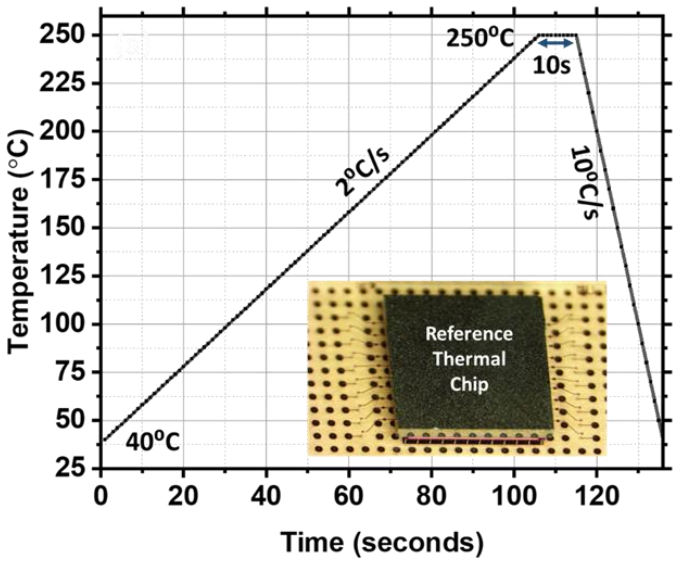


Figure A.1: Reflow profile for SAC305 solder bonding between reference thermal chip and glass interposer with the bonded subassembly shown in the inset.

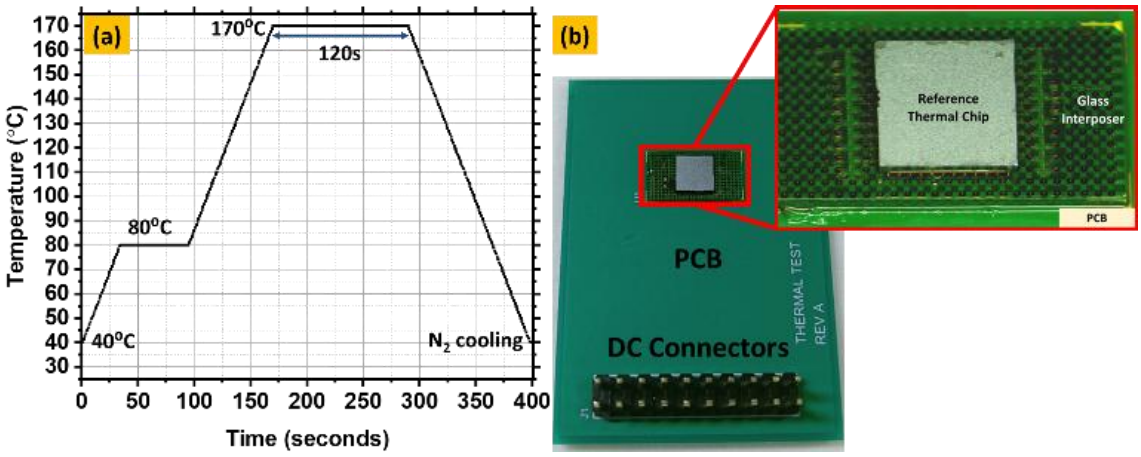


Figure A.2: (a) Reflow profile for BiSn solder bonding between the reference thermal chip subassembly and PCB with the (b) bonded assembly and magnified view of the bonded sample.

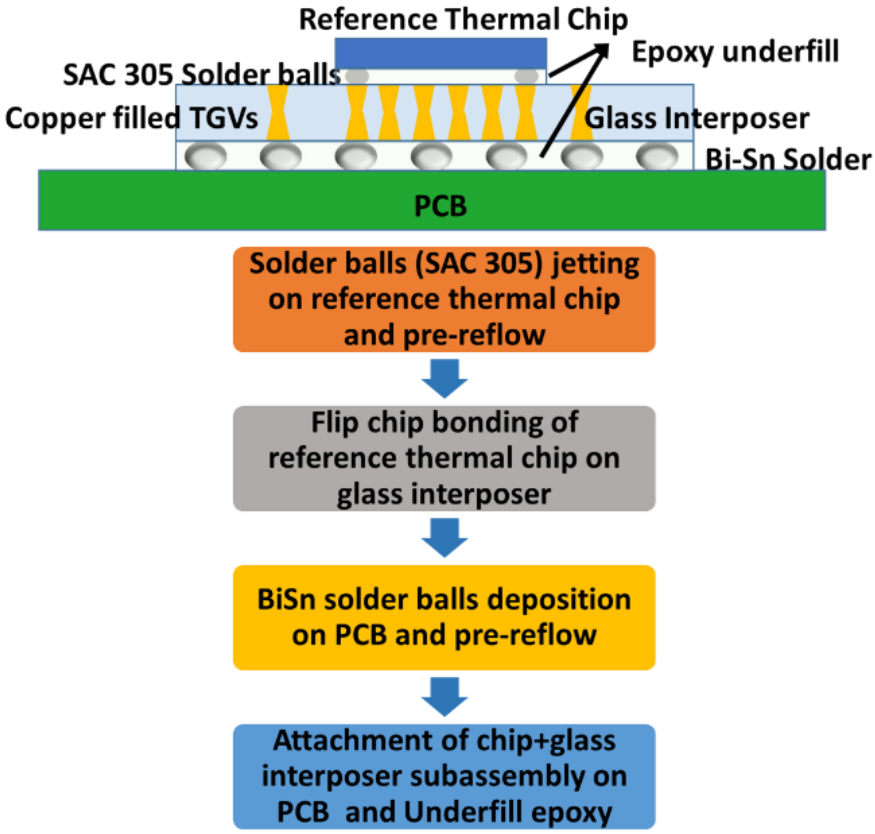


Figure A.3: Assembly process of the thermal test vehicle.

S4. Simulation Of Thermal Test Vehicle

The Finite Element Method (FEM) simulation consists of the conduction, convection and radiation boundary conditions in Comsol Multiphysics®. The convective heat transfer coefficient is set at 10 W/m^2K for natural convection and the emissivity of the chip surface is kept at 0.95 because the surface of the chip is coated with black paint in the measurement setup. The base of the PCB is kept at 20ºC in the simulation model as the PCB was in contact with the surface of the copper block (with integrated TECs) which was maintained at 20ºC in the measurement setup using a TEC source. The geometrical parameters for the glass interposer remain the same as detailed in **Table A.1**. The simulation model of the thermal test vehicle is built using the effective thermal conductivity approach. The effective thermal conductivities of the BGA, microvias connecting the backside RDL to the BGA bond pad, thermal TGVs at different pitches, microvias connecting RDL2 to RDL1 and microvias connecting gold thermal spreading pad to RDL2 are specified in **Table A.3**

Table A.3: Effective Thermal Conductivities Used in Simulation Model

Component	Effective-out-of-plane thermal conductivity (k_z) (W/m.K)	Effective-in-plane thermal conductivity (k_{xy}) (W/m.K)
PCB	0.70	0.70
BGA pad on PCB + solder + BGA pad on backside polyimide	7.46	1.5002
Polyimide	0.25	0.25
Microvia in backside polyimide layer	0.495	0.251
Backside RDL	400	400
TGV (100µm pitch)	37.87	1.50
TGV (200µm pitch)	10.509	1.27
TGV (300µm pitch)	5.38	1.23
TGV (400µm pitch)	3.56	1.21
RDL1	400	400
Microvia in 1st polyimide layer	4	0.27
RDL2	400	400
Microvia in 2nd polyimide layer	0.26	1.59
Gold	315	315
Glass	1.20	1.20
Underfill	1	1
UBM	400	400
SAC305 Solder	58	58
Silicon (Reference Chip)	130	130
Copper heat sink	400	400

These thermal conductivities are crucial parameters in the simulation model, influencing the overall thermal behaviour and heat dissipation characteristics of the system. Their accurate specification ensures the fidelity and reliability of the simulation results.

The components have isotropic thermal conductivity when the out-of-plane and in-plane effective thermal conductivities are listed same in the **Table A.3** above. The gold pad for heat spreading, backside RDL and RDL1 are included in the FEM model as 4.2×5 mm^2, 4.5×5 mm^2 and 4.5×5 mm^2 plates in the glass interposer. The surface temperature of the simulated assembly is shown in **Figure A.4**.

The incorporation of thermal TGVs in glass interposers yields significant advantages, as demonstrated by a notable decrease of 5.5 ºC in the maximum surface temperature observed when transitioning from glass interposers to those with 100µm pitch thermal TGVs (refer to **Figure A.4(a)** and **Figure A.4(b)**). This reduction in temperature becomes even more pronounced, reaching 24.5 ºC, with the integration of a copper heat sink in the PCB, in comparison to the glass interposer alone (as depicted in **Figure A.4(c)**).

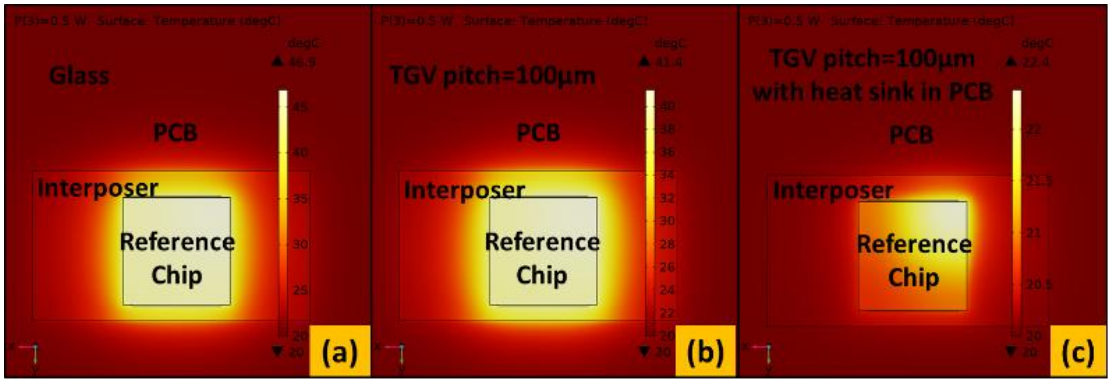


Figure A.4: Top view of reference thermal chip assembly showing heat spreading across the chip's top surface when the reference thermal chip is bonded on (a) glass interposer which is then bonded on PCB; (b) glass interposer with 100µm pitch thermal TGVs which is then bonded on PCB and (c) glass interposer with 100µm pitch thermal TGVs which is then bonded on PCB with heat sink embedded in it. The figure clearly shows the improved lateral thermal spreading by incorporating thermal TGVs and the improvement in the downward heat dissipation (through interposer and PCB) with incorporation of thermal TGVs and heat sink in PCB.

S5. Assembly of electrical test vehicle

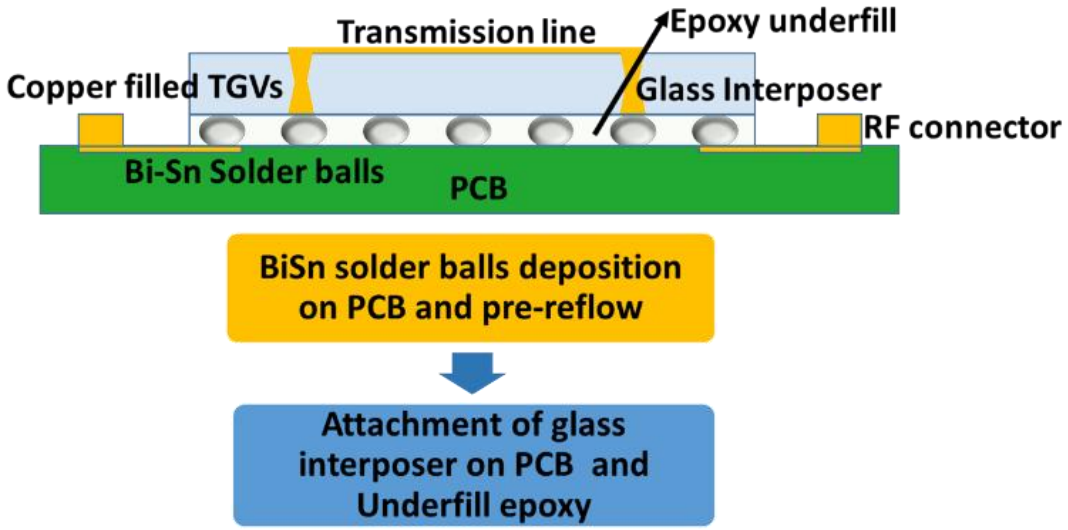


Figure A.5: Assembly process of the electrical test vehicle.

S6. Simulation Of Thermal Test Vehicle

The transmission line on glass results of the S-parameters show some common features of a transmission line where the insertion loss starts near zero dB and decays monotonically with frequency. This monotonic decay is directly related to the losses of the propagating medium. The losses during signal propagation could be due to various reasons, such as the dielectric loss, conductor loss (due to roughness), radiation loss, or cross-coupling with adjacent structure. Assuming no radiation losses and given that the width of the traces is large compared to conductor roughness, the losses are predominantly controlled by the dielectric losses (i.e. the dielectric constant and loss tangent of the material which the signal is propagating through). If we calculate the slope of the S21 plot where the decay is monotonic and normalize that to frequency and the length of the line, we could produce a figure representing the dielectric loss from the glass substrate. For instance, for the 3-mm line and up to 10 GHz, the dielectric loss would be around 0.0435 dB/GHz/cm which is very close to the values obtained with low-loss FR4 material.

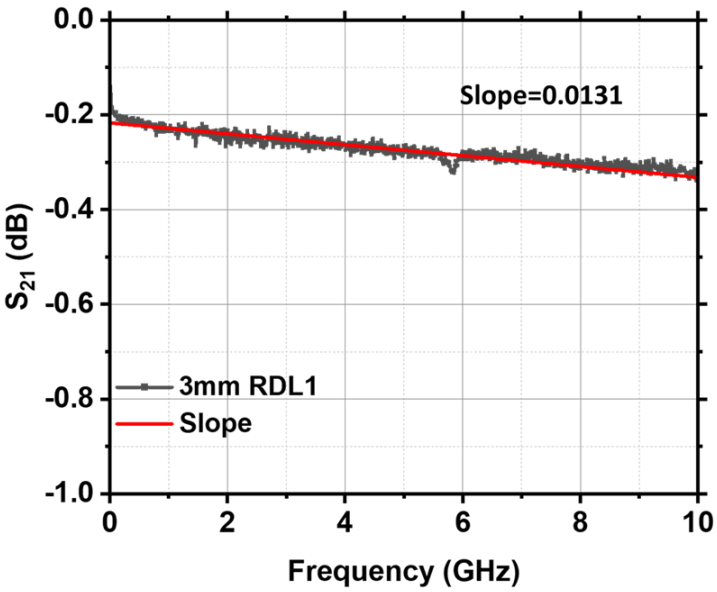


Figure A.6: Insertion loss of the CPW transmission line in glass (RDL1=3mm in length) displaying monotonic decay in the signal upto 10 GHz. The slope of this insertion loss is useful for computing the dielectric loss of the glass interposer, which is calculated as 0.0435 dB/GHz/cm.

In the electrical test vehicle, the uneven spread of the underfill between glass interposer and PCB is seen through the A-scan in the Scanning Acoustic Microscopy (SAM) image (**Figure A.7**). This is also seen by **Figure A.8(a)** where 57% of the ultrasonic signal is reflected when the probe is positioned at the points with uniform Underfill. However, in **Figure A.8(b)**, 100% of the signal is reflected back when the ultrasonic probe is placed at a position with no underfill.

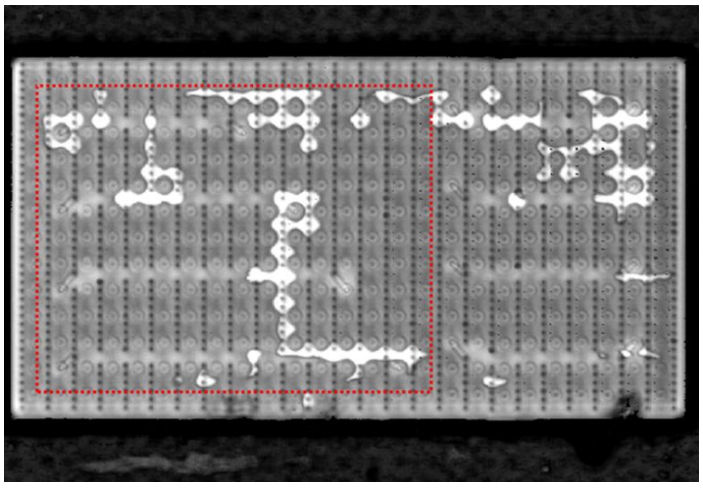


Figure A.7: SAM image displaying the uneven spread of the underfill between glass interposer and PCB, with the area under the signal transmission structures marked through a red dotted box.



Figure A.8: Image displaying reflections of the ultrasonic signal being (a) 57% in the region of evenly spread underfill and (b) 100% in the region with no underfill. This means that the underfill is unevenly spread and the process of underfill dispension through capillary mechanism needs optimization.

The simulated return loss of the packaged glass interposer test vehicle is compared against the de-embedded measurement results of the packaged glass interposer in **Figure A.9**. The simulation and measurement results exhibit the same trend. However, the measured return loss exhibits lower reflections than the simulated return loss, which can be accounted to the uneven spread of the underfill between the glass interposer and the PCB.

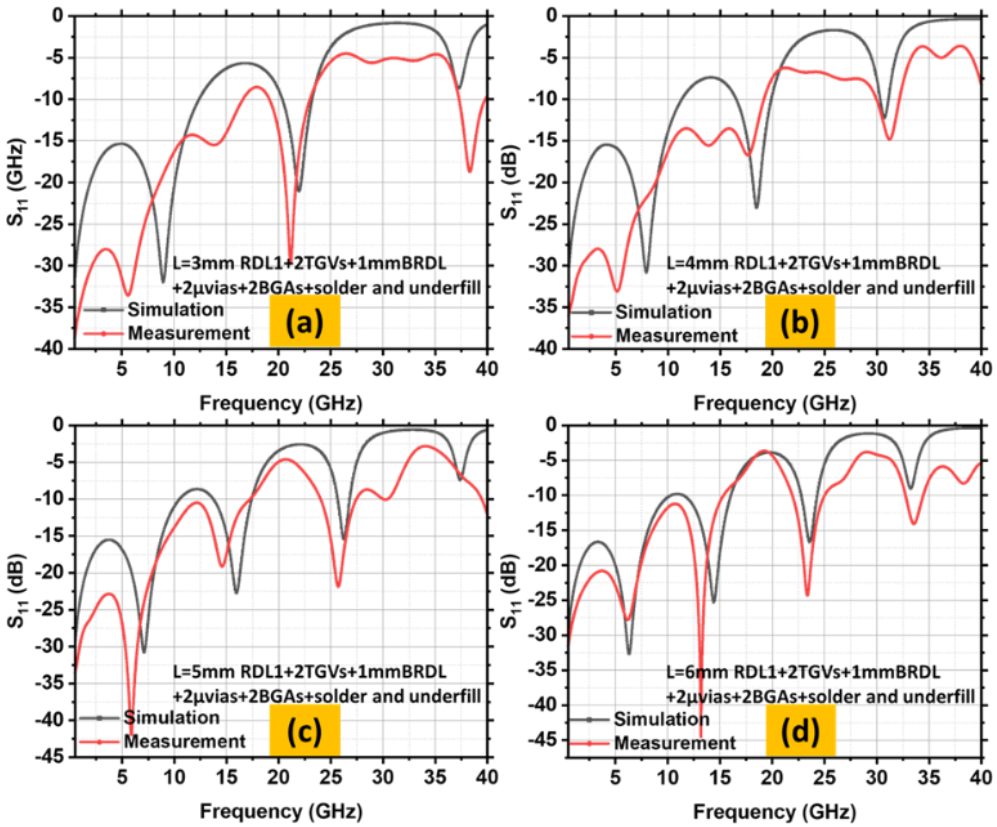


Figure A.9: Simulation and measurement of return loss results for the de-embedded electrical test vehicle. This includes the losses incurred in the glass interposer with solder and underfill beneath it. The measured return loss is lower as compared to the simulated return loss due to the presence of air pockets due to the uneven spread of the underfill between glass interposer and PCB.

Appendix B

S1. Study of Thermal TGV parameters in glass interposer

Table B.1: The maximum temperature of the EIC when the EIC and PIC are co-packaged together on the glass interposer with TGVs.

Case Number	Diameter (µm)	Pitch (µm)	Spacing between EIC and PIC (µm)				
			100	250	500	750	1000
			Max. Temp (ºC)	Max. Temp (ºC)	Max. Temp (ºC)	Max. Temp (ºC)	Max. Temp (ºC)
1	Glass	Glass	57.11823	57.97565	58.61436	58.9364	59.12212
2	50	150	46.1411	46.98011	47.75673	48.18771	48.44821
3	50	175	46.55678	47.37842	48.13398	48.55308	48.8067
4	50	200	46.9753	47.78394	48.52131	48.92978	49.17651
5	50	225	47.39358	48.19278	48.9142	49.31356	49.55422
6	60	150	45.72853	46.58924	47.39235	47.83776	48.1057
7	60	175	46.07261	46.91455	47.69554	48.12891	48.39063
8	60	200	46.41869	47.24543	48.00782	48.43063	48.68657
9	60	225	46.76767	47.5822	48.32841	48.74185	48.9918
10	70	150	45.43379	46.31666	47.14127	47.59751	47.87172
11	70	175	45.7292	46.58996	47.39306	47.83846	48.1064
12	70	200	46.02437	46.86857	47.65265	48.0876	48.35017
13	70	225	46.32116	47.15185	47.9193	48.34487	48.60244
14	80	150	45.20781	46.11153	46.95606	47.42149	47.701
15	80	175	45.47153	46.35144	47.1731	47.62787	47.90125
16	80	200	45.7302	46.59098	47.39408	47.83946	48.10739
17	80	225	45.98892	46.83488	47.62128	48.05742	48.32061
18	90	150	45.02273	45.94816	46.81016	47.28502	47.56856
19	90	175	45.26786	46.16606	47.00485	47.46795	47.74583
20	90	200	45.50119	46.37889	47.19828	47.65192	47.92466
21	90	225	45.73155	46.59235	47.39541	47.84076	48.10868
22	Copper	Copper	40.76833	42.86908	44.4508	45.22233	45.6592

Table B.2: The maximum temperature of the PIC when the EIC and PIC are co-packaged together on the glass interposer with TGVs.

Case Number	Diameter (µm)	Pitch (µm)	Spacing between EIC and PIC (µm)				
			100	250	500	750	1000
			Max. Temp (ºC)	Max. Temp (ºC)	Max. Temp (ºC)	Max. Temp (ºC)	Max. Temp (ºC)
1	Glass	Glass	28.99802	27.43146	25.89015	24.86241	24.08289
2	50	150	29.18562	27.71504	26.10352	25.00514	24.19269
3	50	175	29.08923	27.63808	26.05742	24.97639	24.17062
4	50	200	29.00726	27.57321	26.01574	24.95056	24.14998
5	50	225	28.93989	27.51798	25.98046	24.92776	24.13264
6	60	150	29.30093	27.79011	26.1569	25.03981	24.21854
7	60	175	29.20342	27.729	26.11174	25.01099	24.19779
8	60	200	29.11942	27.66201	26.07209	24.98562	24.1777
9	60	225	29.04562	27.60415	26.03516	24.96301	24.15941
10	70	150	29.40018	27.86267	26.19859	25.06779	24.23894
11	70	175	29.3009	27.79007	26.15684	25.03977	24.21851
12	70	200	29.21635	27.73822	26.11765	25.01467	24.20062
13	70	225	29.14195	27.67973	26.08287	24.99235	24.18286
14	80	150	29.48771	27.92403	26.23449	25.09394	24.25588
15	80	175	29.387	27.85331	26.19309	25.06432	24.23641
16	80	200	29.30081	27.78998	26.15675	25.03971	24.21846
17	80	225	29.2261	27.74421	26.12206	25.0174	24.20272
18	90	150	29.56723	27.97685	26.26518	25.11445	24.27037
19	90	175	29.46396	27.90611	26.2251	25.08547	24.25161
20	90	200	29.37689	27.84609	26.18882	25.06162	24.23444
21	90	225	29.30062	27.78984	26.15661	25.03963	24.21839
22	Copper	Copper	31.1485	28.56487	26.36747	25.06421	24.18436

Table B.3: The maximum temperature of the EIC when the EIC and PIC are co-packaged together on the glass interposer with TGVs and heat sink integrated in the PCB.

Case Number	Diameter (µm)	Pitch (µm)	Spacing between EIC and PIC (µm)				
			100	250	500	750	1000
			Max. Temp (ºC)	Max. Temp (ºC)	Max. Temp (ºC)	Max. Temp (ºC)	Max. Temp (ºC)
1	Glass	Glass	35.77559	35.93196	36.01513	36.04831	36.06509
2	50	150	24.03782	24.05828	24.07205	24.07779	24.08076
3	50	175	24.35196	24.37451	24.3894	24.39562	24.39882
4	50	200	24.6918	24.71689	24.7331	24.73987	24.74331
5	50	225	25.05179	25.07974	25.0975	25.10482	25.10858
6	60	150	23.75577	23.7746	23.78746	23.79283	23.79563
7	60	175	23.98894	24.0091	24.0227	24.02837	24.03131
8	60	200	24.24493	24.26674	24.28127	24.28729	24.29041
9	60	225	24.52052	24.54428	24.55984	24.56633	24.56965
10	70	150	23.57715	23.59519	23.60757	23.61276	23.61546
11	70	175	23.75649	23.77533	23.78819	23.79357	23.79637
12	70	200	23.95512	23.97508	23.98856	23.9942	23.99711
13	70	225	24.17111	24.19244	24.20668	24.21261	24.21568
14	80	150	23.45702	23.47475	23.48684	23.49196	23.4946
15	80	175	23.5992	23.61733	23.62976	23.63497	23.63768
16	80	200	23.75745	23.77631	23.78917	23.79455	23.79735
17	80	225	23.93066	23.95047	23.96388	23.96948	23.97238
18	90	150	23.37222	23.38991	23.40192	23.407	23.40962
19	90	175	23.48785	23.50567	23.51781	23.52296	23.52561
20	90	200	23.6169	23.63511	23.64759	23.65282	23.65554
21	90	225	23.75869	23.77755	23.79042	23.7958	23.7986
22	Copper	Copper	22.94449	23.0131	23.04113	23.05096	23.05573

Table B.4: The maximum temperature of the PIC when the EIC and PIC are co-packaged together on the glass interposer with TGVs and heat sink integrated in the PCB.

Case Number	Diameter (µm)	Pitch (µm)	Spacing between EIC and PIC (µm)				
			100	250	500	750	1000
			Max. Temp (ºC)	Max. Temp (ºC)	Max. Temp (ºC)	Max. Temp (ºC)	Max. Temp (ºC)
1	Glass	Glass	21.04094	20.61724	20.32509	20.19919	20.13489
2	50	150	20.21922	20.13471	20.07798	20.05172	20.03683
3	50	175	20.23063	20.14162	20.08149	20.05378	20.03819
4	50	200	20.24457	20.14991	20.0858	20.05629	20.03986
5	50	225	20.26066	20.15943	20.09059	20.05921	20.04179
6	60	150	20.21089	20.12948	20.07525	20.05017	20.03582
7	60	175	20.21764	20.13373	20.07747	20.05143	20.03664
8	60	200	20.22657	20.13917	20.08031	20.05305	20.03771
9	60	225	20.23738	20.14566	20.08358	20.055	20.039
10	70	150	20.20724	20.12696	20.07393	20.04942	20.03535
11	70	175	20.21093	20.1295	20.07526	20.05017	20.03582
12	70	200	20.21658	20.13307	20.07713	20.05123	20.03651
13	70	225	20.22388	20.13754	20.07946	20.05256	20.03738
14	80	150	20.20616	20.12589	20.07332	20.04909	20.03515
15	80	175	20.20762	20.12724	20.07407	20.0495	20.0354
16	80	200	20.21098	20.12953	20.07528	20.05018	20.03583
17	80	225	20.21584	20.13261	20.07689	20.05109	20.03642
18	90	150	20.2066	20.12569	20.07316	20.04901	20.03512
19	90	175	20.20632	20.12612	20.07344	20.04916	20.03519
20	90	200	20.20796	20.12748	20.0742	20.04957	20.03544
21	90	225	20.21104	20.12956	20.07529	20.05019	20.03583
22	Copper	Copper	20.22967	20.1054	20.05376	20.03456	20.02429

Table B.5: The maximum temperature of the EIC when the EIC and PIC are co-packaged together on the glass interposer with TGVs and heat sink integrated in the PCB right under the thermal TGVs, with no C4 bumps in between.

Case Number	Diameter (µm)	Pitch (µm)	Spacing between EIC and PIC (µm)				
			100	250	500	750	1000
			Max. Temp (ºC)	Max. Temp (ºC)	Max. Temp (ºC)	Max. Temp (ºC)	Max. Temp (ºC)
1	Glass	Glass	33.82271	33.93231	33.98193	33.99867	34.00857
2	50	150	21.60462	21.60574	21.60633	21.60652	21.60661
3	50	175	21.93416	21.93613	21.93711	21.93743	21.93758
4	50	200	22.29098	22.29409	22.29557	22.29605	22.29627
5	50	225	22.66897	22.67349	22.67562	22.67631	22.67663
6	60	150	21.30945	21.30995	21.31023	21.31032	21.31037
7	60	175	21.5534	21.5544	21.55494	21.55512	21.5552
8	60	200	21.82186	21.8235	21.82433	21.82461	21.82474
9	60	225	22.11114	22.11365	22.11486	22.11526	22.11544
10	70	150	21.12413	21.12433	21.1244	21.12443	21.12446
11	70	175	21.31022	21.31072	21.311	21.31109	21.31114
12	70	200	21.51798	21.51891	21.51941	21.51957	21.51965
13	70	225	21.74442	21.74587	21.7466	21.74686	21.74697
14	80	150	21.00108	21.00121	21.00122	21.00127	21.00129
15	80	175	21.1469	21.14713	21.14723	21.14724	21.14726
16	80	200	21.31125	21.31175	21.31203	21.31213	21.31217
17	80	225	21.49237	21.49325	21.49372	21.49388	21.49395
18	90	150	20.91501	20.9151	20.91509	20.91514	20.91516
19	90	175	21.0326	21.03274	21.03277	21.03281	21.03283
20	90	200	21.16524	21.1655	21.1656	21.1656	21.16562
21	90	225	21.31255	21.31305	21.31333	21.31343	21.31348
22	Copper	Copper	20.6219	20.62194	20.62196	20.62197	20.62197

Table B.6: The maximum temperature of the PIC when the EIC and PIC are co-packaged together on the glass interposer with TGVs and heat sink integrated in the PCB right under the thermal TGVs, with no C4 bumps in between.

Case Number	Diameter (µm)	Pitch (µm)	Spacing between EIC and PIC (µm)				
			100	250	500	750	1000
			Max. Temp (ºC)	Max. Temp (ºC)	Max. Temp (ºC)	Max. Temp (ºC)	Max. Temp (ºC)
1	Glass	Glass	20.75222	20.41482	20.19174	20.10534	20.06654
2	50	150	20.02485	20.01278	20.00605	20.00351	20.00234
3	50	175	20.03481	20.01798	20.00843	20.00484	20.0032
4	50	200	20.04651	20.02413	20.01125	20.00639	20.00419
5	50	225	20.05982	20.03116	20.01446	20.00816	20.00532
6	60	150	20.01674	20.00857	20.00412	20.00243	20.00165
7	60	175	20.02338	20.01201	20.0057	20.00332	20.00222
8	60	200	20.03133	20.01615	20.00759	20.00437	20.0029
9	60	225	20.0405	20.02097	20.0098	20.00559	20.00368
10	70	150	20.01212	20.00618	20.00302	20.00181	20.00124
11	70	175	20.01676	20.00858	20.00412	20.00244	20.00165
12	70	200	20.02238	20.01149	20.00546	20.00319	20.00213
13	70	225	20.02898	20.01493	20.00703	20.00406	20.0027
14	80	150	20.00928	20.00472	20.00234	20.00143	20.00099
15	80	175	20.01267	20.00646	20.00315	20.00189	20.00129
16	80	200	20.01679	20.00859	20.00413	20.00244	20.00165
17	80	225	20.02166	20.01112	20.00529	20.00309	20.00207
18	90	150	20.00744	20.00377	20.00189	20.00118	20.00083
19	90	175	20.00999	20.00508	20.00251	20.00153	20.00106
20	90	200	20.01311	20.00669	20.00325	20.00195	20.00133
21	90	225	20.01682	20.00861	20.00414	20.00245	20.00165
22	Copper	Copper	20.00166	20.00076	20.00041	20.00027	20.0002

Table B.7: The maximum temperature of the EIC when the EIC and PIC are co-packaged together on the glass interposer with TGVs and heat sink integrated in the PCB right under the thermal TGVs of the EIC only, with no C4 bumps in between.

Case Number	Diameter (µm)	Pitch (µm)	Spacing between EIC and PIC (µm)				
			100	250	500	750um	1000
			Max. Temp (ºC)	Max. Temp (ºC)	Max. Temp (ºC)	Max. Temp (ºC)	Max. Temp (ºC)
1	Glass	Glass	33.87387	33.96457	34.00228	34.01268	34.01689
2	50	150	21.60544	21.60619	21.60655	21.60665	21.60669
3	50	175	21.93547	21.93685	21.93747	21.93763	21.9377
4	50	200	22.29289	22.29513	22.29609	22.29634	22.29644
5	50	225	22.67161	22.67496	22.67635	22.67672	22.67687
6	60	150	21.30987	21.31017	21.31035	21.31039	21.31042
7	60	175	21.55415	21.55482	21.55515	21.55523	21.55527
8	60	200	21.82297	21.82413	21.82465	21.82479	21.82485
9	60	225	22.11273	22.11452	22.11529	22.1155	22.11558
10	70	150	21.12433	21.12441	21.12443	21.12446	21.12447
11	70	175	21.31064	21.31094	21.31112	21.31116	21.31119
12	70	200	21.51868	21.5193	21.51961	21.51968	21.51972
13	70	225	21.74542	21.74643	21.74689	21.74701	21.74707
14	80	150	21.0012	21.00125	21.0013	21.00131	21.0013
15	80	175	21.14712	21.14721	21.14724	21.14727	21.14728
16	80	200	21.31167	21.31197	21.31215	21.31219	21.31223
17	80	225	21.49304	21.49361	21.49391	21.49398	21.49402
18	90	150	20.9151	20.91512	20.91513	20.91517	20.91514
19	90	175	21.03273	21.03279	21.03284	21.03285	21.03284
20	90	200	21.16547	21.16555	21.16561	21.16564	21.16565
21	90	225	21.31297	21.31328	21.31346	21.3135	21.31353
22	Copper	Copper	20.62195	20.62196	20.62198	20.62196	20.62197

Table B.8: The maximum temperature of the PIC when the EIC and PIC are co-packaged together on the glass interposer with TGVs and heat sink integrated in the PCB right under the thermal TGVs of the EIC only, with no C4 bumps in between.

Case Number	Diameter (µm)	Pitch (µm)	Spacing between EIC and PIC (µm)				
			100	250	500	750	1000
			Max. Temp (ºC)	Max. Temp (ºC)	Max. Temp (ºC)	Max. Temp (ºC)	Max. Temp (ºC)
1	Glass	Glass	21.63853	21.07041	20.66169	20.46718	20.35211
2	50	150	20.1578	20.11204	20.07587	20.05596	20.0437
3	50	175	20.19588	20.13788	20.09247	20.06802	20.05279
4	50	200	20.23728	20.16574	20.11032	20.08083	20.06249
5	50	225	20.28122	20.19505	20.12906	20.09423	20.07264
6	60	150	20.12379	20.08878	20.06086	20.04507	20.03543
7	60	175	20.15189	20.10801	20.07327	20.05408	20.04228
8	60	200	20.18288	20.12909	20.08682	20.06387	20.04971
9	60	225	20.21641	20.15172	20.10135	20.0744	20.05761
10	70	150	20.10245	20.07406	20.05132	20.03814	20.03014
11	70	175	20.12389	20.08885	20.0609	20.0451	20.03545
12	70	200	20.14781	20.10523	20.07148	20.05278	20.04129
13	70	225	20.17393	20.12302	20.08292	20.06106	20.04758
14	80	150	20.08834	20.06419	20.04492	20.03345	20.02655
15	80	175	20.10508	20.07588	20.05249	20.039	20.03079
16	80	200	20.12402	20.08894	20.06095	20.04514	20.03548
17	80	225	20.14487	20.10322	20.07018	20.05184	20.04058
18	90	150	20.07857	20.05734	20.04022	20.03023	20.02412
19	90	175	20.09196	20.06671	20.04655	20.03463	20.02748
20	90	200	20.10719	20.07735	20.05344	20.03969	20.03132
21	90	225	20.12419	20.08904	20.06102	20.04519	20.03552
22	Copper	Copper	20.05154	20.03471	20.02407	20.0185	20.01438

S2. The curious case of underfill thickness uniformity

The hotspot management in the EIC design is also studied through the 2.5D package similar to **Figure 7.17**, with a change in the position of the reference PIC. A new package is designed where the position of the reference PIC is changed from the edge of the interposer to near the center of the interposer. **Figure B.1** details the geometrical details of the reference chips as well as distances between the reference chips in this new package.

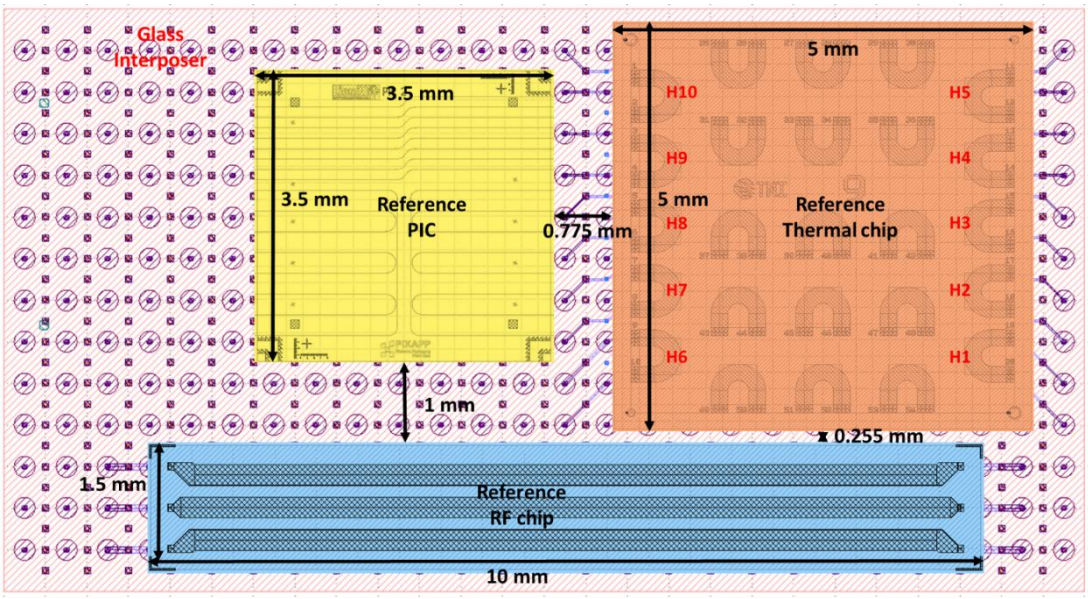


Figure B.1: Design of the glass interposer with the reference PIC, reference thermal chip and reference RF chip bonded on the glass interposer, with reference PIC positioned near the center of the interposer.

Figure B.2 shows the reference chips bonded on the glass interposer using the SAC305 solder and this subassembly is then bonded on the PCB using BiSn solder, which is shown in **Figure B.3**.

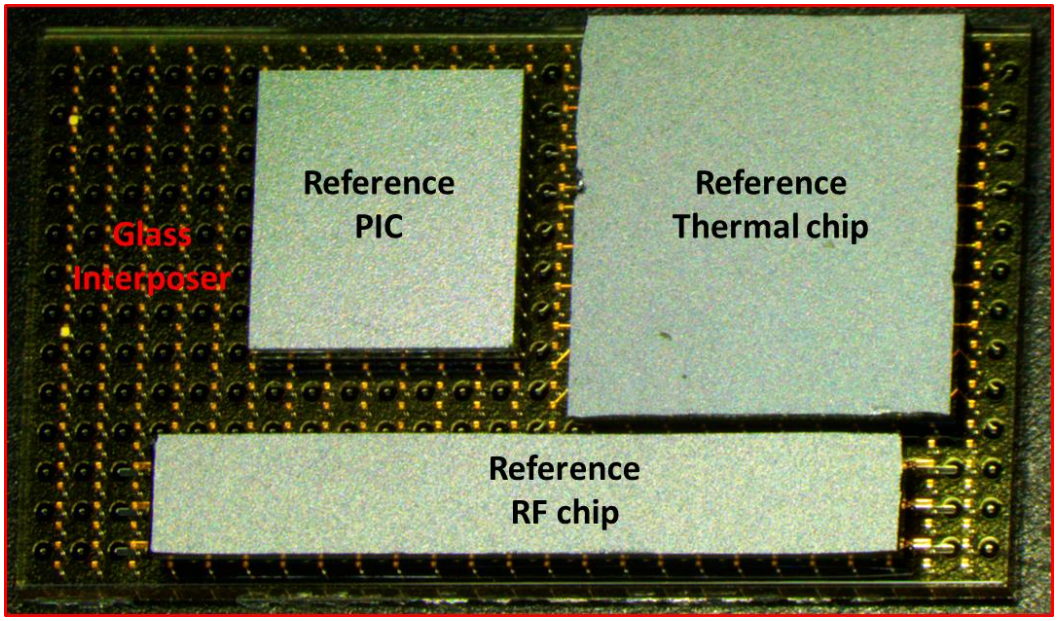


Figure B.2: Subassembly consisting of the reference PIC, reference thermal chip and reference RF chip bonded on the glass interposer using simultaneous SAC solder reflow for all the chips, with reference PIC positioned near the center of the interposer.

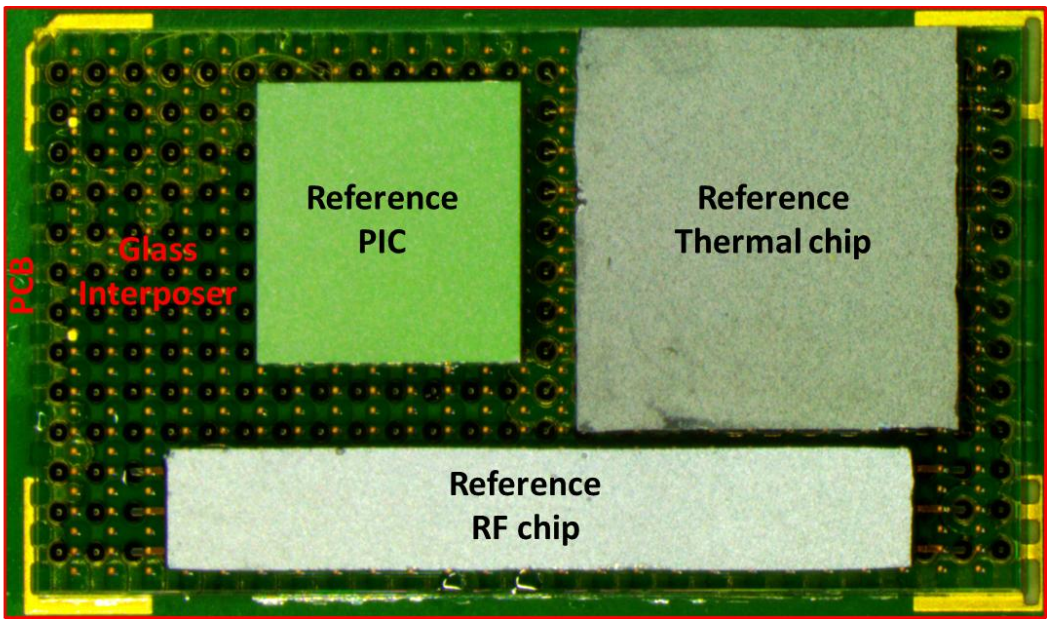


Figure B.3: Assembly consisting of the reference PIC, reference thermal chip and reference RF chip bonded on the glass interposer, which is then bonded on the PCB using BiSn solder reflow to connect the subassembly to the PCB, with reference PIC positioned near the center of the interposer .

The final assembly for thermal characterization is shown in **Figure B.4** below. The IR thermal measurement of the package when the heater loopback H6 is powered, is shown in **Figure B.5**.

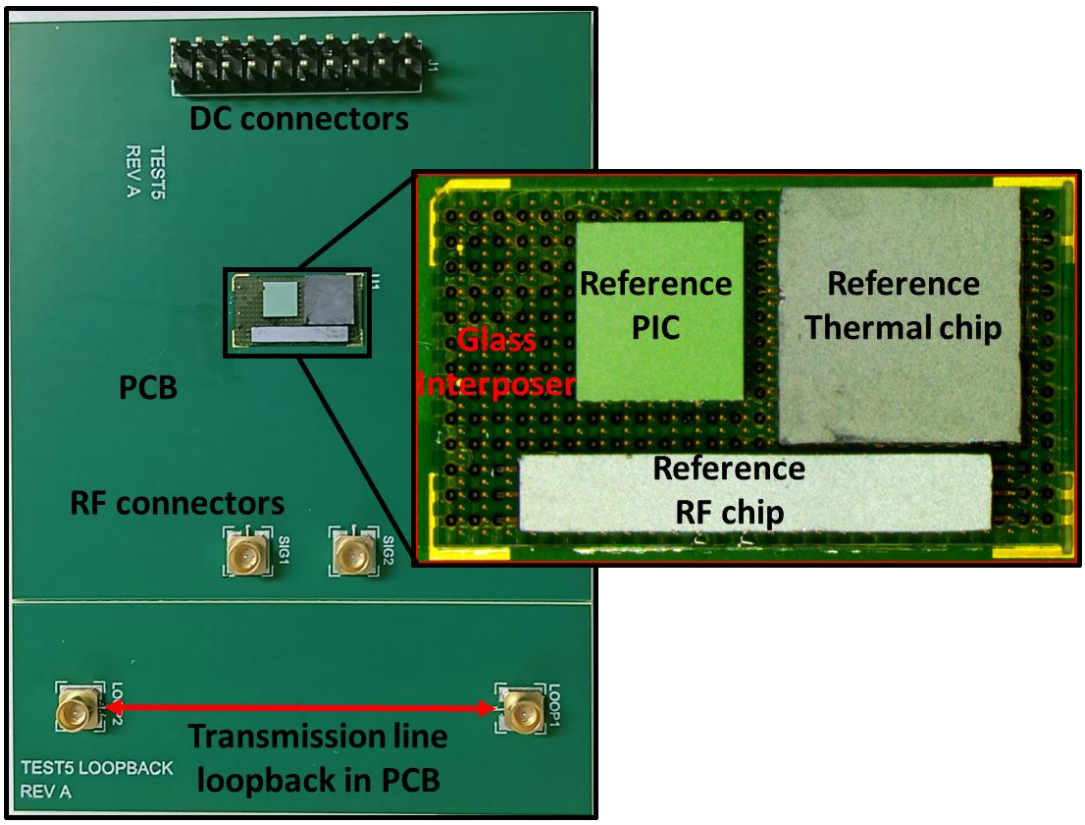


Figure B.4: Final assembly of the co-packaged reference chips, with reference PIC positioned near the center of the interposer.

The comparison of **Figure B.5** with **Figure 7.19** reveals that the steady state temperature profile (insets in Figure 19 and **Figure B.5**) across the surface of the reference thermal chip a nd reference RF chip remains similar. However, the surface temperature profile for the reference PIC shows a change in the profile dependent on the location of the hotspot. In **Figure 7.19**, the temperature profile of the reference PIC shows a slight decrease across the surface. However, this decrease is less pronounced in the temperature profile of the reference PIC in **Figure B.5**.

In addition to this, **Figure B.6** shows the transient measurement of the maximum surface temperatures of the reference chips. The difference between **Figure 7.20** and **Figure B.6** clearly shows the elevated temperature (62.1ºC in Figure 20 to 70ºC in **Figure B.6**) in the case of the reference thermal chip. The temperature difference between the reference RF chip and reference PIC is lower in this case (2.5ºC in the case of **Figure B.6**) as compared to that in **Figure 7.20** (7.4ºC). However, the

difference in temperature between the reference thermal chip and reference RF chip as well as the temperature difference between the reference thermal chip and reference PIC is higher in **Figure B.6** as compared to that in **Figure 7.20**. This anomaly is also visible in **Figure B.7 (a)**, **(b)** and **(c)** where the dependence of change in temperature of the reference RF chip and reference PIC on the different positions of the heater loopback on the reference thermal chip is also inconsistent.

Figure B.7 clearly shows that the maximum temperature of the reference PIC is higher for H6-H10, because of the lowered distance between the reference thermal chip and reference PIC, resulting in higher thermal crosstalk. However, this maximum PIC temperature (**Figure B.7** at 0.5W) has increased only minimally (approximately 3ºC) as compared to the case (**Figure 7.21** at 0.5W) where there is more spacing between the reference PIC and reference thermal chip. Thus, the change in location of the PIC from edge of the interposer in **Figure 7.18** to near the centre of the interposer in **Figure B.4** is not changing the PIC temperature much and is also leading to higher temperature of the reference thermal chip. This phenomenon is investigated through scanning acoustic microscopy (SAM) of both the packages (in **Figure 7.18** and **Figure B.4**). This is done to determine the role of the epoxy underfill under the reference thermal chip on the increased temperature of the reference thermal chip and its effect on the temperature of the reference PIC.

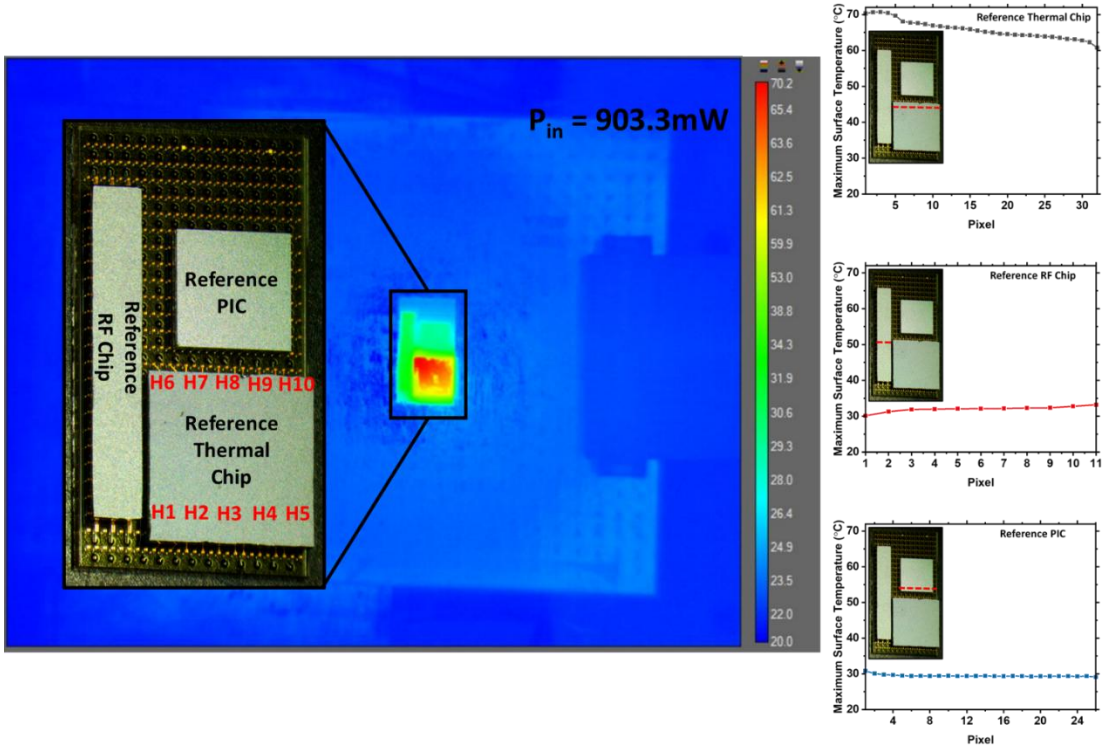


Figure B.5: The steady-state IR thermal measurement of the co-packaged reference chips along the horizontal axis when the heater loopback H6 is powered to 903.3 mW, with reference PIC positioned near the center of the interposer.

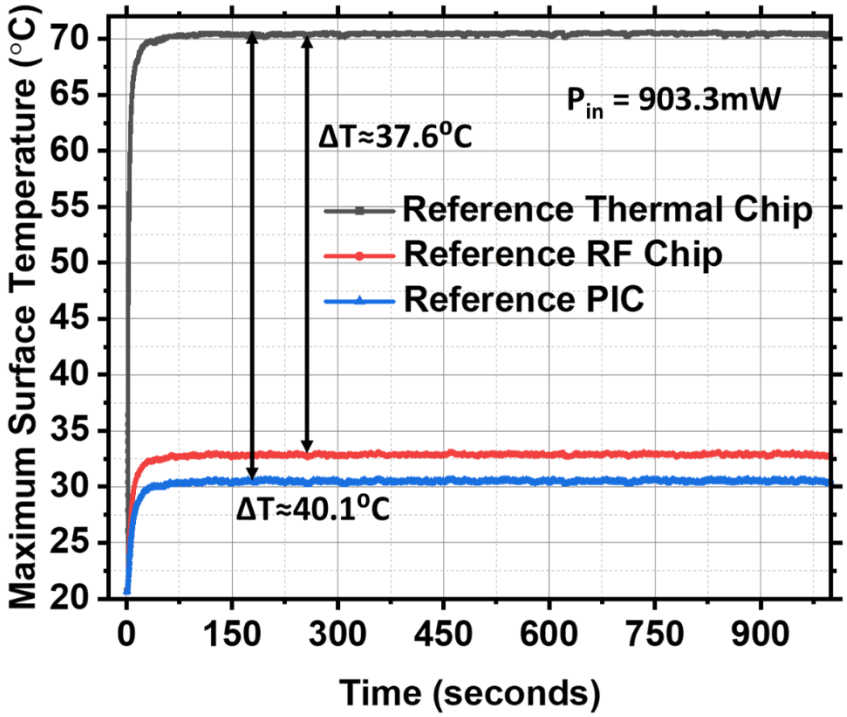


Figure B.6: The transient IR thermal measurement of the co-packaged reference chips along the horizontal axis when the heater loopback H6 is powered to 903.3 mW, with reference PIC positioned near the center of the interposer

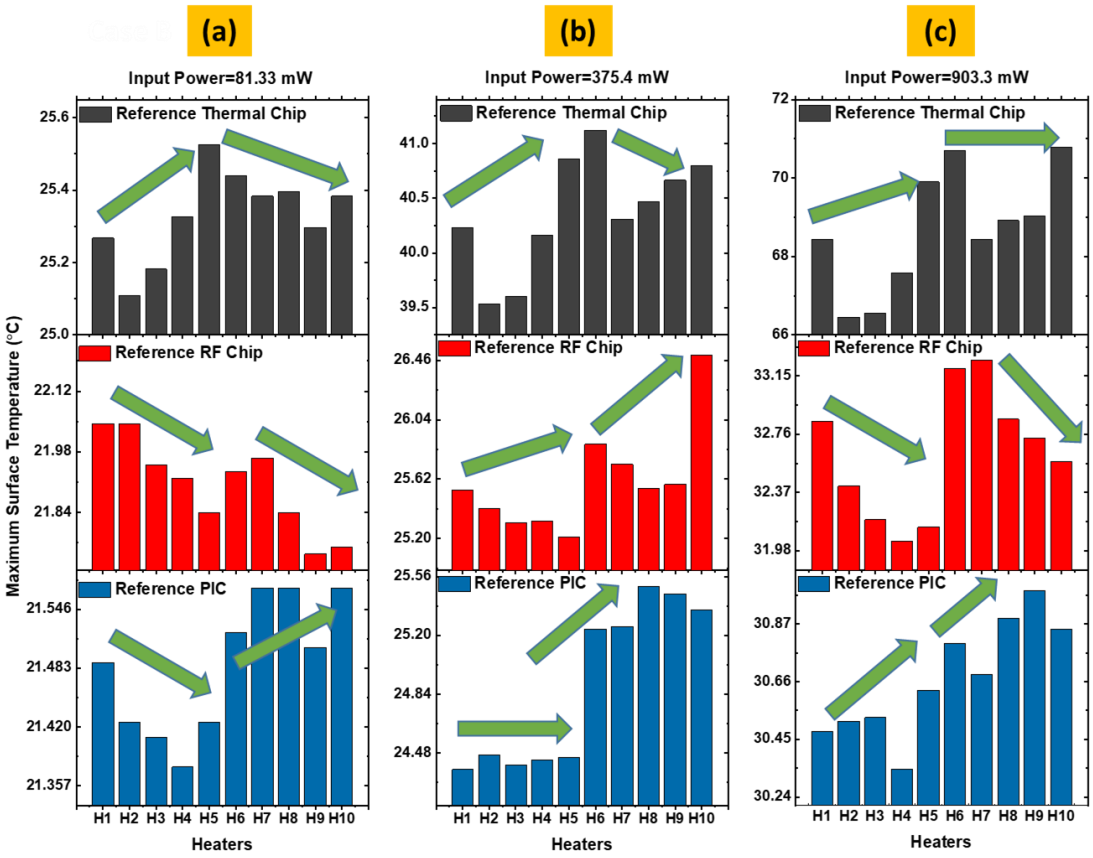


Figure B.7: The dependence of the maximum surface temperatures of the reference PIC near the center of the interposer and reference RF chip on the different heater loopbacks in the reference thermal chip (H1-H10) being operated at different powers generated by the heaters (a) 81.33mW, (b) 375.4mW and (c) 903.3mW.

The A-scan is carried out with Sonoscan D9600 CSAM for the packages in both **Figure 7.18** (PIC at edge) and **Figure B.4** (PIC near centre). The probe wavelength is 100 MHz with 0.50" spectral density. The package with PIC at edge (**Figure B.8**) shows a general even spread of the underfill under the reference thermal chip. Though, there are certain small areas with uneven spread of the underfill under the reference thermal chip, the scan displays only 66% of the signal reflected. This is also evident with the thermal crosstalk between the reference thermal chip and reference PIC is visible as temperatures for both chips follow the same trend (**Figure 7.21**).

However, in the case of the package with PIC near centre (**Figure B.9**), the spread of the underfill under the reference thermal chip is very uneven and 74% of the signal is reflected back (**Figure B.9**). The difference in the color intensity signifies the uneven spread of the epoxy underfill, which translates that the thickness of the underfill is uneven across the area of the reference thermal chip.

This in turn impacts the thermal contact between the reference thermal chip and the glass interposer, which is visible in the higher temperature of the reference thermal chip (especially heaters H6-H10) and the lower thermal crosstalk between reference thermal chip and reference PIC.

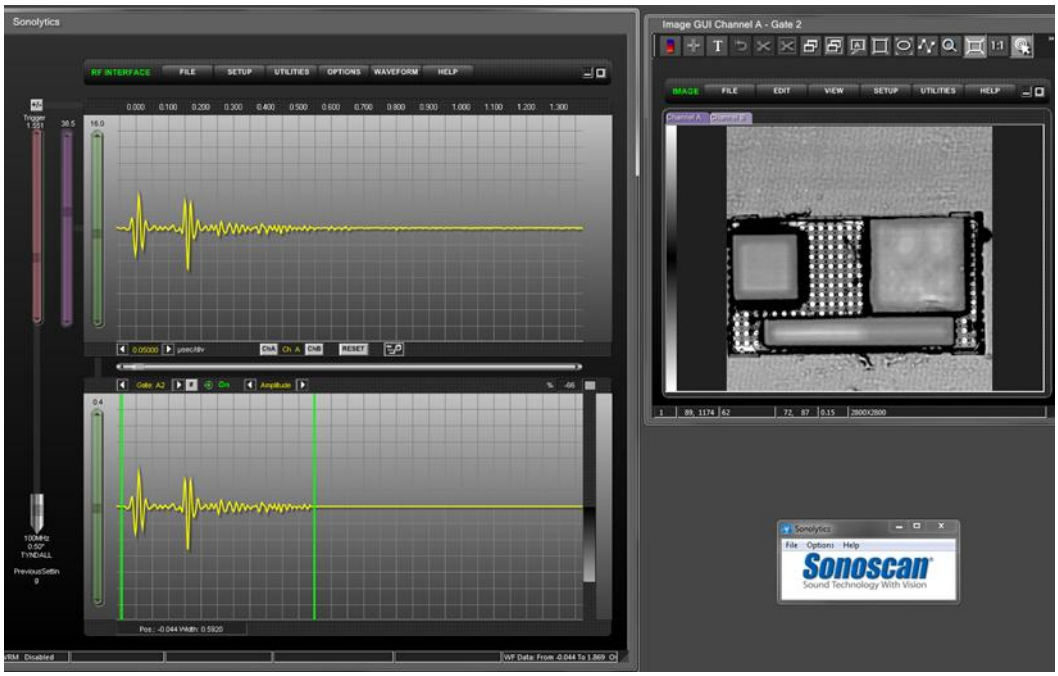


Figure B.8: SAM image of the package consisting of the reference chips bonded on the glass interposer and PCB with PIC positioned at the edge of the interposer.

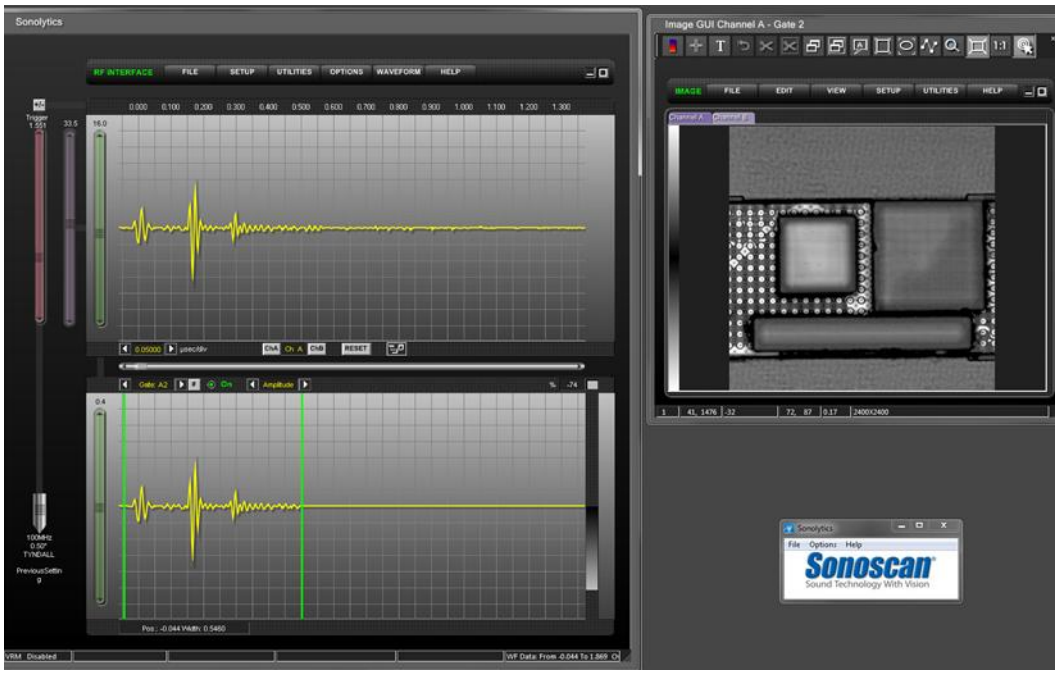


Figure B.9: SAM image of the package consisting of the reference chips bonded on the glass interposer and PCB with PIC positioned near the center of the interposer.