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Overview of advanced optical interconnect technologies, processes, and equipment in co-packaged optics

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Abstract: An overview of advanced optical interconnects is presented in the context of co-packaged optics, including high-density optical interconnects, 3D printed micro-optics, and novel glass interposer technologies, which are key to overcoming key photonics packaging challenges.

1. Introduction

As silicon photonics becomes more complex to meet the exponentially increasing power and bandwidth demands in computing and datacentres, overcoming the challenge of optical interconnectivity remains a primary packaging challenge. Co-packaging of electronic and photonic chips are required in most practical applications of photonics. This is now being driven by CPO for data centre applications, where high edge bandwidths and low energy consumption are key requirements [1]. Meeting the demand of future systems will require both high data rates per channel and a large increase in the number of channels, and research thus far has mainly focused on the former. Therefore, efforts must now be made to facilitate a massive expansion in channel count. In addition, a shift in assembly from package- to wafer-level must be made to improve the manufacturability of co-packaged optics. As such, novel glass interposer platforms and assembly processes are being developed [2,3]. Furthermore, developments in two-photon polymerization allow the fabrication of complex-shape 3D printed micro-optics such as beam-turning collimators [4], anti-reflective surface patterns [5] and diffractive beam splitters [6], which all offer innovative routes towards high-density low-loss optical packaging of fiber-to-PIC and chip-to-chip interconnects.

2. Multi-chip co-packaged optics (CPO) and high-density optical interconnects

In previous work, we developed a scalable process to integrate fiber arrays with multiple silicon PICs on an organic substrate for a co-packaged FPGA-based multi-chip module. A compact module that coupled 168 fibers to one side of an FPGA package was demonstrated, which is a key step towards co-packaged optics exceeding 10 Tbps [7]. While the need for high-density optical interconnects is well-established for multi-chip data processors and in novel computing technologies, such as neuromorphic computing PICs, the fabrication and packaging challenges are less widely reported. Current optical interconnects are limited to the perimeter of a chip ("shoreline") with fiber arrays typically at pitches of 127 or 250 µm. An alternative approach is moving to the chip surface using grating couplers or turning prisms and shifting connectivity from a 1D to 2D configuration (Fig 1b). In this presentation, we will discuss the technologies, implications, and limitations of increasing channel density for 1D and 2D fiber-to-chip interconnects and present an optical demonstrator package which showcases an increase in optical interconnect density on-chip by a factor of 5 over a standard pitch of 127 µm.

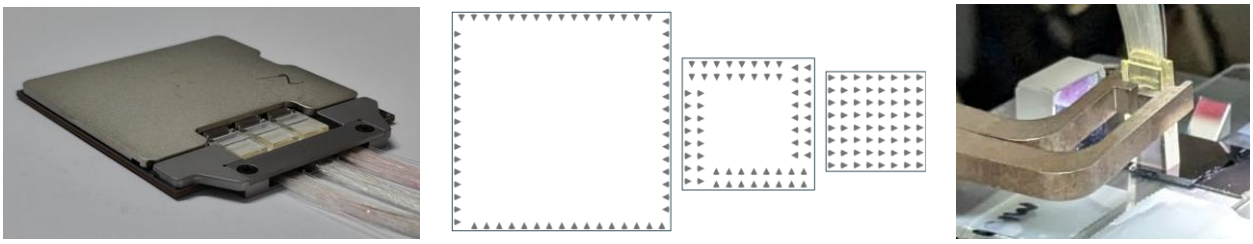


Figure 1: (a) Edge-coupled FPGA multi-chip package with three 56-channel FAs attached to one side (b) Illustrated on-chip area reduction for one-line, two-line, and 2D matrix optical coupler arrays. (c) A demonstrator package for a 96 channel ultra-fine pitch two-line fiber array.

3. Novel interposer technologies for wafer-level packaging

Glass interposers are a promising platform for co-packaged 2.5D integration of photonic and electronic devices at higher volumes. Compared to organic substrates, glass offers low dielectric loss, high dimensional stability, optical

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transparency, and a coefficient of thermal expansion closely matched to Si and InP. These properties make it ideal for integrating PICs, driver/TIA chiplets, and micro-optics with low-parasitic electrical routing and thermal management structures. Fine-pitch through-glass vias (TGVs) and multi-layer redistribution lines enable high-frequency electrical fan-out, and the transparent glass substrate allows micro-optical elements like lenses or gratings to be directly incorporated with wafer-level accurate alignment of optical elements. Etched cavities and transparent laser-welded caps create hermetic seals for sensitive components, enabling higher yields through wafer-scale assembly and testing. In this presentation, we will demonstrate scalable packaging and assembly methods through two key demonstrator CPO packages of next-generation optical communications and bio-sensing technologies based on wafer-level glass interposers, and how this interposer platform supports scaled assembly.

4. 3D printed micro-optics

Further improvements in CPO technology can be made by introducing pluggable fiber-to-PIC interconnects using beam-expanding micro-optics, a technology that has been well-reported in the literature with insertion losses as low as 0.7 dB [8]. By expanding and collimating a beam on the fiber array, which is then coupled into a refocusing lens on the PIC, the alignment tolerances of a system are significantly relaxed. However, small mode mismatches of the connecterised module, due to differences between the design and fabricated MFDs and wafer-to-wafer variation, are inevitable with fixed-design off-the-shelf micro-optics. In this presentation, we will explore how 3D printed micro-optics with beam-steering structures, collimating lenses, and anti-reflective coatings offer a route towards ultra-low loss, epoxy-free, passively aligned pluggable interfaces by better mode matching through bespoke design.

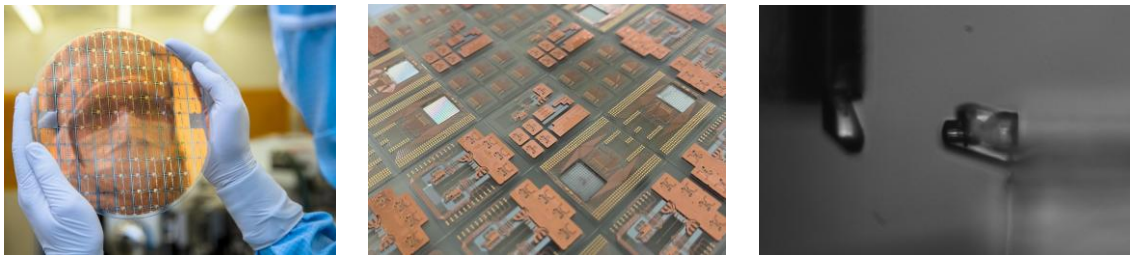


Figure 2: Novel glass interposer technologies for wafer-level scale up of PIC packaging developed in the PhotonicLEAP project: (a) full wafer (b) detailed view. (c) beam-steering fiber (left) to PIC (right) optical interconnect using 3D printed micro-optics

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