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High aspect ratio iridescent three-dimensional metal–insulator–metal capacitors using atomic layer deposition

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The authors report on the structural and electrical properties of $TiN/Al_2O_3/TiN$ metal–insulator–metal (MIM) capacitor structures in submicron three-dimensional (3D) trench geometries with an aspect ratio of ~30. A simplified process route was employed where the three layers for the MIM stack were deposited using atomic layer deposition (ALD) in a single run at a process temperature of 250 °C. The TiN top and bottom electrodes were deposited via plasma-enhanced ALD using a tetrakis(dimethylamino)titanium precursor. 3D trench devices yielded capacitance densities of 36 fF/μm^2 and quality factors >65 at low frequency (200 Hz), with low leakage current densities (<3 nA/cm^2 at 1 V). These devices also show strong optical iridescence which, when combined with the covert embedded capacitance, show potential for system in package (SiP) anticounterfeiting applications. © *2014 American Vacuum Society*.
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I. INTRODUCTION

Methods for on-chip fabrication of high surface area three-dimensional 3D electrodes and device architectures at mesoscopic length scales (10 nm–10 μm) are of significant interest for a range of applications, including energy storage, radio-frequency communications, memory devices, and anti-counterfeiting.[1–14] With the demand for continued electronic device miniaturization, integration of metal–insulator–metal (MIM) capacitor architectures with such high surface area electrodes is of great importance, particularly in boosting overall capacitance while reducing device footprint.[1–11] Moving from two-dimensional (2D) planar device structures to three-dimensional (3D) structures is obviously attractive in terms of the associated increase in capacitance density. However, significant fabrication challenges remain. A key challenge is conformally coating high-aspect ratio structures using conventional physical vapor deposition or chemical vapor deposition techniques at deep submicron critical dimensions.

Atomic layer deposition (ALD), which is based on alternating self-limiting surface reactions, whereby films are fabricated submonolayer at a time by repeating two subsequently executed half-cycle reactions, remains the only thin film technique, which can provide the necessary conformity and thickness control required for coating both metal and dielectric films in high aspect ratio structures. Additional benefits of all-ALD processing for MIM device architectures include the ability to form successive layers without breaking vacuum, thus minimizing the unwanted introduction of atmospheric impurities and contaminants.[3,7,8] However, while there has been a strong focus on achieving large capacitance densities with such architectures, there has been little in the way of assessing the performance of all-ALD 3D capacitors for such applications. For a comprehensive overview of device performance, the quality factor (Q-factor) or related equivalent series resistance (ESR) should be characterized alongside capacitance density, leakage current density, and breakdown voltage.[3–6,11] Here we present a detailed study of the structural and electrical properties of $TiN/Al_2O_3/TiN$ metal–insulator–metal capacitor structures in 3D trench geometries with high aspect ratio (~30) and narrow trench widths (<500 nm). We discuss the benefits and challenges associated with all-ALD processing of metal–insulator–metal device structures.

II. EXPERIMENT

Sets of both planar and trench capacitors were designed side by side on the same mask set, enabling both device types to be fabricated in the same process flow and characterized under identical conditions. The substrate was n-type Si(100), As surface doping, $\sim 5 \times 10^{19}$ cm^{-3}. For photolithographic patterning of the trench arrays, Fujifilm HiPR6512 photoresist was spun at 5000 rpm for 30 s followed by a 90 s soft-bake at 90 °C. The trench arrays (nominally 1 μm line/space) were defined using a SF_6/C_4F_8 plasma etch followed by resist removal. Prior to MIM processing, the silicon trench features and the unpatterned Si substrate were coated with ~610 nm of Al_2O_3 via thermal ALD (Cambridge Nanotech Fiji system) using trimethylaluminum and water precursors. This step was undertaken to increase the aspect ratio by a factor of ~3 to assess the conformity and electrical performance of thin MIM capacitor stacks (<150 nm) in high aspect ratio geometries. Next, a metal/insulator/metal stack of TiN (20 nm)/Al_2O_3 (10 nm)/TiN (100 nm) was deposited in succession in the same ALD chamber at a constant temperature of 250 °C. Plasma-enhanced ALD (300 W) at 300 mTorr was employed for the TiN layers using a tetrakis (dimethylamino) titanium precursor with 60 SCCM N_2 flow

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and 200 SCCM Ar carrier gas. Thermal ALD was used for the Al_2O_3 layer. The thickness of the top TiN layer (100 nm) was chosen in order to seal the top of the trenches and thus obviate the need for a planarization layer for subsequent lithographic patterning.

In order to lithographically pattern the MIM capacitors, the top TiN electrodes [marked *S* in Fig. 1(e)] were etched using a Cl_2 etch process, which is highly selective to the underlying Al_2O_3. A via to the bottom planar TiN electrode [marked *D* in Fig. 1(e)] was then opened using a nonselective BCl_3 etch process. Capacitance and quality factor versus voltage measurements (C–V, Q–V) were performed using an Agilent E4980A Precision LCR Meter. Current–voltage (I–V) measurements were performed using a HP4156A Semiconductor Parameter Analyzer. All measurements were performed in a vacuum probe station ($\sim 10^{-6}$ mbar, Lakeshore TTPX) at 25 °C. Scanning electron microscopy (SEM) imaging of mechanically cleaved cross sections was performed on a JEOL 7500F cold-cathode field-emission scanning electron microscope with an in-lens detector.

III. RESULTS AND DISCUSSION

Figures 1(a)–1(c) show cross-sectional X-SEM images for a typical metal–insulator–metal trench capacitor. The 610 nm layer of Al_2O_3 deposited by ALD on the lithographically patterned Si trenches significantly increases the aspect ratio from ~10 to ~30 while also reducing sidewall roughness through cumulative smoothing of the original trench features. Highly conformal step coverage of the 610 nm layer of Al_2O_3 is also evident at both the top and bottom of the trenches. However, analysis of measured SEM images using ImageJ reveals a significantly smaller average layer thickness for the TiN bottom electrodes at the bottom of each trench (15 ± 2 nm) versus the measured values at the top of the trench (20 ± 1 nm). While care need to be taken in the accuracy of thickness measurements using this approach (due to the resolution limit of ~1 nm for the SEM), this trend in thickness reduction has been reported and modeled for plasma-enhanced ALD in high aspect ratio structures and attributed to unwanted recombination of plasma radicals at trench sidewalls leading to recombination-limited growth toward the bottom of the trenches.[15,16] By contrast, image analysis reveals that the average thickness of the Al_2O_3 layer deposited using thermal ALD is only slightly smaller at the bottom of the trenches (9 ± 1 nm) compared to the top of the trenches (10 ± 1 nm).

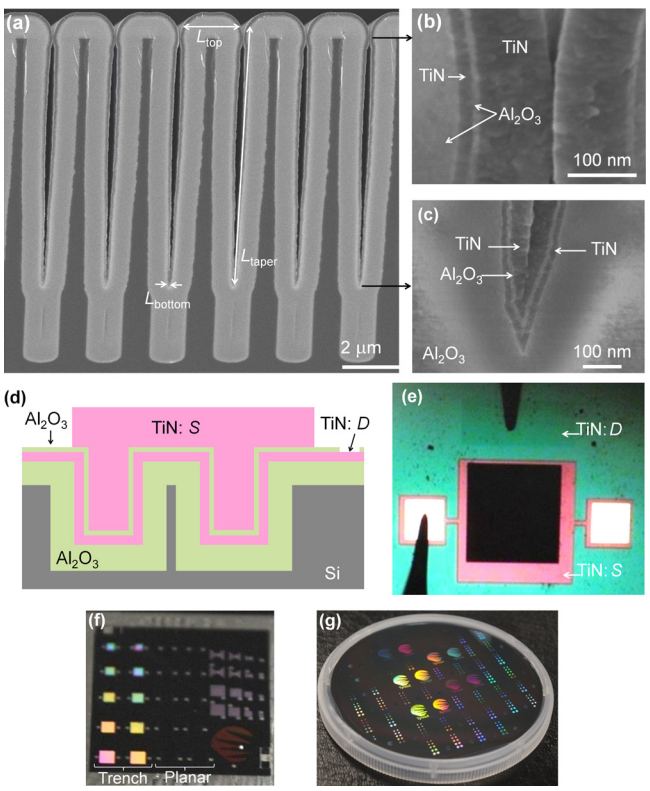


FIG. 1. (Color online) (a) Cross section X-SEM images of a trench array capacitor. Higher magnification images showing the TiN/Al_2O_3/TiN MIM stack: (b) top of trench; (c) bottom of trench. (d) Side-view schematic. (e) Top-view microscope image of a trench capacitor structure showing an etched rectangular via to the planar bottom TiN contact (*D*) and the patterned top TiN electrode (*S*) with top metal probe pads. (f) Photograph of a tilted device chip with arrays of trench and planar devices. (g) 4 in. silicon wafer patterned with arrays of 3D trench capacitors (bright squares) and logos (via capacitors).

Optical micrographs and photographs [Figs. 1(e)–1(g)] reveal that the ALD layers enable retention (and even enhancement) of the iridescence of the micropatterned Si features. The observed intense rainbow pattern, arising from the periodic array of vertical (square footprint) and horizontal (logo footprint) etched trenches show potential for anti-counterfeiting applications whereby an overt optical signature could be combined with a covert embedded electrical signature derived from conformal coatings of metal–insulator–metal layers via atomic layer deposition.[13,14] The iridescence signature could be achieved from either lithographically patterned or self-assembled photonic crystal templates, e.g., anodized aluminium oxide.[17] Roll-to-roll fabrication of anodic alumina honeycomb templates,[18] together with spatial ALD methods compatible with large area processing,[19,20] show great promise for development of these devices on flexible and low-cost substrates.

Figure 2 shows the frequency dependence of capacitance density for both trench and planar MIM capacitors. A

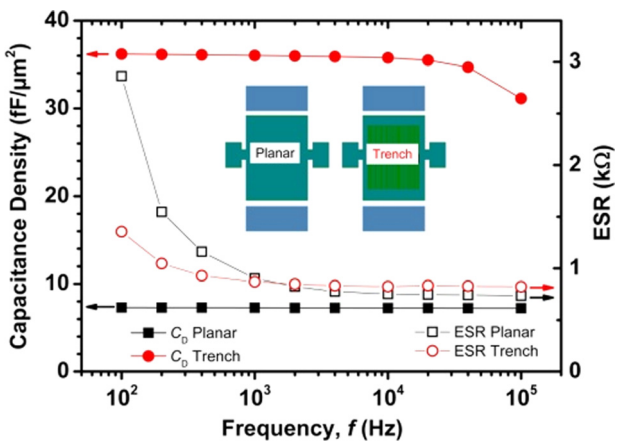


FIG. 2. (Color online) Dependence of zero-bias capacitance density (filled symbols) and ESR (open symbols) on frequency for trench and planar MIM capacitor with the same footprint area (0.33 mm^2).

significant high capacitance of 36.2 fF/μm^2 is measured at 200 Hz for the trench capacitor in comparison to 7.3 fF/μm^2 for its planar equivalent with the same surface footprint ($A_{pl} = 0.33$ mm^2). This increase in capacitance of ~5 shows potential for system in package (SiP) anticounterfeit applications when considered from the perspective of footprint reduction. The capacitance densities for both planar and trench devices remain almost constant from 200 Hz to 10 kHz. At frequencies between 10 and 100 kHz the capacitance density for the planar device remains relatively unchanged (0.2% drop); however, a roll-off in capacitance density is observed for the trench device (12% drop). The ESR data for both planar and trench devices is also shown in Fig. 2. The ESR data does not vary significantly from 10 to 100 kHz (<5% drop) with measured values at 100 kHz of 740 Ω for the planar device and 820 Ω for the trench device. The large ESR values are likely due to the sheet resistance of the TiN electrodes, $R_{\square} \approx 400$ Ω/□ for a 25 nm thick film on the same substrate and also the access track design for the top contact [see Fig. 1(e)]. Subsequent process development has led to sheet resistance values ~70 Ω/□ for 20 nm thick planar TiN films,[21] future devices shall employ this development where we expect to see an appreciable reduction in ESR.

The total impedance (Z) for the planar device follows the expected $\log(|Z|) \propto -\log(f)$ dependence for a simple RC circuit. However, the roll-off in capacitance for the trench device cannot be adequately described using a single RC relaxation time and suggests the presence of a parasitic element. A likely cause is the presence of recombination-limited ALD reaction by-products formed during deposition of the TiN electrodes in the high-aspect ratio trench structures.[15,16] These contaminants could then lead to a higher density of impurities and interface traps at the TiN surface prior to deposition of the Al_2O_3 insulating layer, analogous to CVD growth of TiN,[4] or ALD growth of TiN on planar surfaces with insufficient plasma duration.[22] Recent time-of-flight mass spectrometry data on planar films grown with similar process parameters showed significant carbon levels, which would be expected to increase for films grown in high aspect-ratio structures.[21] Thus, increased access resistance resulting from plasma radical recombination losses may set a limit on the aspect ratio for 3D devices with plasma enhanced ALD metal electrodes, therefore future work will focus on thermal titanium nitride ALD processing routes.

Figure 3 shows the measured capacitance values (at 200 Hz) for both planar and trench capacitors with increasing surface footprint area (A_{pl}). The capacitance values estimated from Eqs. (1) and (2), respectively, show good agreement with the measured values for the planar (C_{pl}) and trench devices (C_{tr})

$$C_{pl} = \varepsilon_0 k A_{pl}/d, \quad (1)$$

$$C_{tr} = \varepsilon_0 k[A_{per} + W_{tr} n_{tr}(L_{bottom} + L_{top} + 2L_{taper})]/d, \quad (2)$$

where ε_0 is the permittivity of free space (8.85×10^{-12} F/m); d is the thickness of the Al_2O_3 layer (measured by X-SEM as being ~10 nm); and k is the dielectric constant of Al_2O_3 (~8.3), extracted from the measured C_{pl} vs A_{pl} data taking

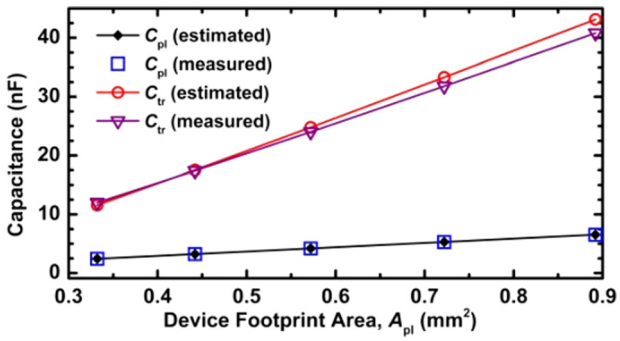


FIG. 3. (Color online) Measured vs estimated capacitance values for planar devices (C_{pl}) and trench devices (C_{tr}) vs increasing device footprint area.

$d = 10$ nm. For the trench capacitors, estimated values for capacitance were derived using Eq. (2), where A_{per} is the planar perimeter area (including the bond pads) surrounding each trench array [see Fig. 1(e)]; W_{tr} is the width of the trench region; n_{tr} is the number of trenches; L_{bottom}, L_{top}, and L_{taper} are the lengths along the bottom; the top and the tapered walls of the trench, respectively.

Figure 4(a) shows the quality factor (Q_{pl}) versus frequency (f) data for planar capacitors with increasing footprint area. There is a consistent reduction in quality factor at 200 Hz from $Q_{pl} \approx 210$ to $Q_{pl} \approx 100$ as the device footprint

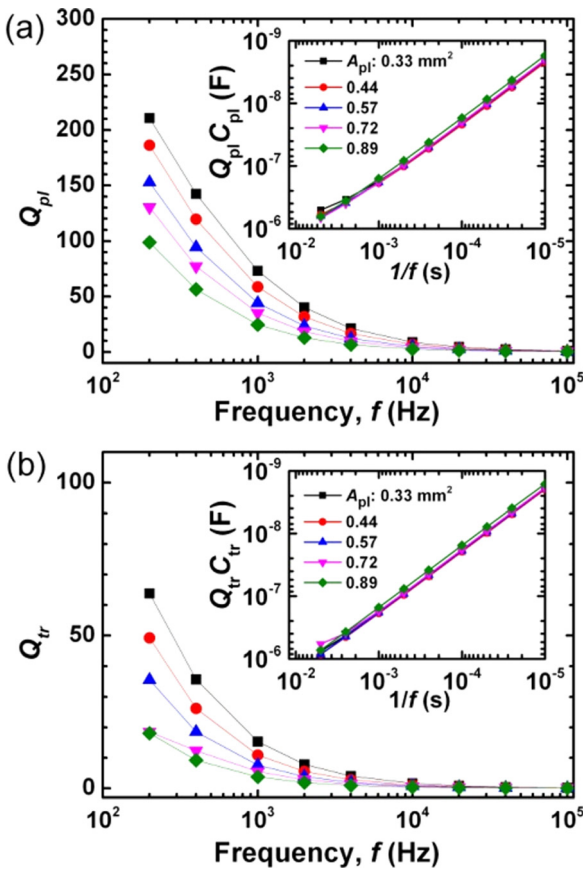


FIG. 4. (Color online) Measured quality factor as a function of frequency for (a) planar capacitors (Q_{pl}), (b) trench capacitors (Q_{tr}) of increasing footprint area (A_{pl}). Insets: $Q_{pl}C_{pl}$ and $Q_{tr}C_{tr}$ products, respectively, plotted vs inverse frequency.

increases from 0.33 to 0.89 mm^2. This trend is mirrored in Fig. 4(b) for trench capacitors with the exception that lower quality factors are observed ($Q_{tr} \leq 65$). The log–log plots of the capacitance-quality factor products ($Q_{pl}C_{pl}$ and $Q_{tr}C_{tr}$) shown in the insets demonstrate that the quality factors for both trench and capacitor devices scale inversely with both capacitance and frequency, as expected, $Q \propto (f\mathrm{RC})^{-1}$. This would suggest a suitable application for such high aspect ratio MIM devices may lie in the low frequency (<100 kHz) regime.

Figure 5 shows the leakage current density versus voltage data for both planar and trench capacitors (bottom electrode injection). The device footprint, A_{pl}, was used as the area for the planar device and the area of the trench device was estimated using Eq. (2). The planar capacitors exhibit a conventional leakage profile with a clear breakdown at ~6.8 V and low leakage current density at 1 V ($J_{pl} \approx 7 \times 10^{-10}$ A cm^{-2}), in agreement with reports for TiN/Al_2O_3/Si MOS capacitors deposited using single-reactor ALD.[23] In the high-bias range, 4.2 V < V < 6.8 V, the J_{pl}–V data are well described by a simple Fowler–Nordheim fit

$$\ln\left(J_{FN}/E^2\right) \propto -\phi_0^{3/2}E^{-1}, \tag{3}$$

for $E = V/d$, where ϕ_0 is the TiN/Al_2O_3 barrier offset energy.[4]

The trench devices show higher leakage current density at low bias, $J_{tr} \approx 3 \times 10^{-9}$ A cm^{-2} at 1 V. The J_{tr}-V data can only be fit with the simple Fowler–Nordheim model in Eq. (3) for a narrower voltage window (4.2 V < V < 5.7 V). The fits over this range suggest a reduction in work function for the trench device, $\phi_0{}^{tr} \approx 0.95\phi_0{}^{pl}$, consistent with trapping at the TiN/Al_2O_3 electrode interface,[4] as discussed for the trench capacitance data presented in Fig. 2. There are several step-changes in the high-bias leakage data for the trench device, in contrast to the single breakdown step in the planar device. The gradual breakdown profile for the trench device, together with the increased leakage ($J_{tr} > J_{pl}$) at low bias suggest contributions from multiple processes. The leakage could result from incorporation of carbon contaminants in the dielectric toward the bottom of the trenches due to radical recombination during TiN deposition, slight reductions in the dielectric thickness or local field enhancement due to asperities at the sidewalls and bottom of trench, or additionally due to series resistance effects. Further work will focus on assessing the relative magnitude of these effects and their implications for device performance. For example, because the power density in supercapacitors is inversely proportional to the equivalent series resistance, a trade-off is required between trench depth (aspect ratio), trench pitch and metal thickness.[12,24] For the proposed iridescent capacitor structures, where contactless reading via RF is desirable, capacitance density is not the dominant figure of merit. Lower aspect ratio structures may suffice to achieve suitable performance at frequencies up to several GHz, enabling contactless authentication at larger reader-label separations.

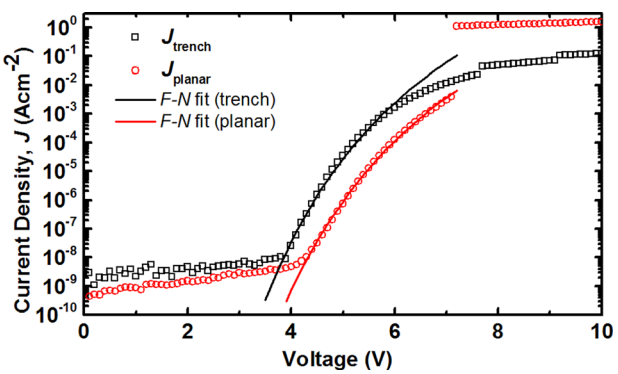


FIG. 5. (Color online) Current density vs voltage breakdown measurements for typical planar and trench capacitors having the same device footprint (0.57 mm^2), together with Fowler–Nordheim fits.

IV. SUMMARY AND CONCLUSIONS

All-ALD TiN/Al_2O_3/TiN MIM capacitors have been demonstrated for both planar and 3D configurations over frequency ranges from 200 Hz to 100 kHz. The large capacitance density and low leakage of these all-ALD 3D MIM devices shows promise for energy storage applications at low frequency and radio-freqency identification at intermediate frequency (125 kHz). Capacitance roll-off in 3D devices at frequencies above 10 kHz suggest that contaminants from recombination-limited plasma enhanced ALD in ultranarrow 3D structures may inhibit development of ultrahigh aspect ratio, all-plasma enhanced ALD TiN/Al_2O_3/TiN MIM capacitors for RF or memory applications at deep submicron critical dimensions. However, the lower thermal budget achieved using plasma enhanced ALD would be of benefit in back end of line processing for integrated lower aspect ratio (<20) 3D MIM devices. Challenges will include process optimization to reduce sheet resistance and also ensure thickness uniformity in high aspect ratio trenches for the metal electrodes, coupled with fabrication improvements for reducing sidewall roughness and asperities. Recently developed roll-to-roll templating methods together with spatial ALD offer exciting prospects for development of energy storage and anticounterfeiting devices on flexible and low-cost substrates.

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