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Simulation of junctionless Si nanowire transistors with 3 nm gate length

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Inspired by recent experimental realizations and theoretical simulations of thin silicon nanowire-based devices, we perform proof-of-concept simulations of junctionless gated Si nanowire transistors. Based on first-principles, our primary predictions are that Si-based transistors are physically possible without major changes in design philosophy at scales of ~1 nm wire diameter and ~3 nm gate length, and that the junctionless transistor avoids potentially serious difficulties affecting junctioned channels at these length scales. We also present investigations into atomic-level design factors such as dopant positioning and concentration. © *2010 American Institute of Physics*. [doi:10.1063/1.3478012]

As the semiconductor technology roadmap nears its end, more and more fundamental changes are becoming necessary to design transistor devices. Short-channel effects[1–3] degrade subthreshold slope, aggravate drain-induced barrier lowering, and limit overall performance. In response, designs using more gates and thinner channels to enhance gating control and alleviate these effects are becoming popular.[1–3] Other proposals[3,4] for ultrashort-channel transistors include tunneling field-effect transistors (FETs) and impact ionization FETs, but all of these require precise control of dopant positioning to arrive at a profile that includes junctions, for example, p-i-p, p-i-n, etc.

However, *junctionless* nanowire transistors were recently fabricated with a trigate electrode structure.[5] These nanowire transistors have a thickness of a few nanometers and channel length of 1 μm. This design, essentially a "gated resistor" that turns off by pinch-off when gate voltage is applied, avoids the difficulty and high thermal budget of fabricating ultrashallow junctions [as in standard metal oxide semiconductor FETs (MOSFETs)] at nanometer length scales.[5,6] Moreover, previous semiclassical simulations indicate it has better short-channel characteristics than comparable trigate MOSFETs.[6]

In this letter, we continue our previous efforts[7,8] to understand transport in Si nanowires by simulating an atomic-scale device with a gating field and calculating its I-V_{ds} characteristics. Calculations of the response of doped junctionless silicon nanowire (SiNW) transistors to source-drain bias, V_{ds}, and gate voltage, V_g, are presented. By employing a first-principles approach for the electronic structure at small bias, our simulations provide a proof-of-concept, applying to devices both thinner and shorter than those currently achievable in the laboratory[5] or by effective-mass calculation.[6] At such small scales, standard two-junction transistor designs are difficult to fabricate, and (because of dopant de-localization, as we will discuss) may not be physically possible. Most importantly, we find the junctionless transistor device concept works at scales as small as wire diameter of ~1 nm and gate length of ~3 nm.

A typical structure of our simulated junctionless SiNW transistors is shown in Fig. 1. As the name implies, these devices are uniformly doped throughout the wire from a macroscopic perspective. As shown, the SiNWs have a gate-all-around (GAA) architecture. In the actual devices realized experimentally,[5] field effects from the work function of the gate cause the device to turn off at $V_g=0$ V. But in principle, a junctionless device is a "gated resistor" that is *on* at $V_g=0$ V, as is the case in our simulations.

We used the [110]-oriented hydrogenated Si nanowire structures from previous work[7] (Fig. 1). The wire diameter is $2R_{NW}=1.15$ nm. We found the electronic structure and Hamiltonian for all valence electrons in the doped SiNW device self-consistently in a full quantum-mechanical treatment using the density functional tight-binding[9] code, DFTB$^+$. DFTB$^+$ performs self-consistent electronic structure calculations in a tight-binding framework using parameters calculated from first-principles density functional theory (DFT).[9] This enabled us to simulate ~800 atoms in our supercells.

We simulated the gating field from a GAA structure by using point charges (the positions and charges of these are held fixed within the electronic-structure calculation) to represent the gate. We assembled the point charges in rings of radius $R_g=1.6$ nm around the nanowire structure, typically containing 100 point charges per ring and spaced about 1 Å apart along the wire axis. We used a gate length $L_g=3.1$ nm. This approach yields a discrete approximation to the charge distribution of a gate with the required geometric characteristics. The values of the point charges were fixed by the desired gate voltage, V_g. To relate V_g to the gate charges, we modeled the oxide surrounding the nanowires by a continuum with hafnium oxide dielectric constant, $\epsilon_{HfO_2}=25$.

To model doped nanowires, we inserted substitutional dopant atoms into the SiNW lattice. We used Ga for a p-type dopant, and As for n-type. Because of the relatively small supercells amenable to first-principles calculations, we used

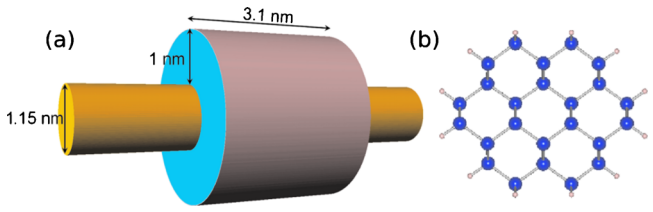


FIG. 1. (Color online) (a) Geometry of junctionless GAA SiNW devices simulated. (b) Cross section of Si nanowire structures simulated.

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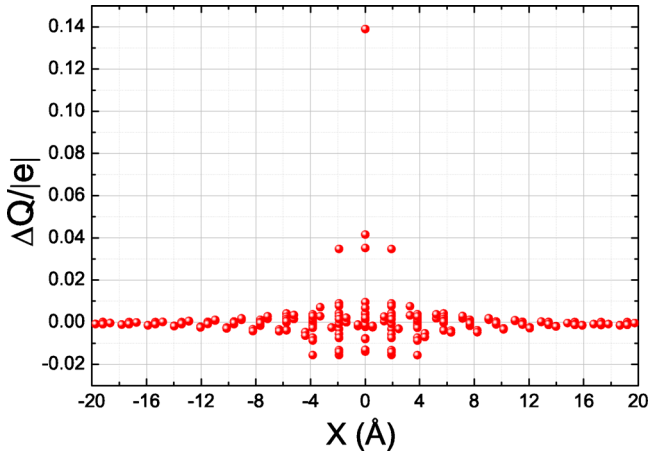


FIG. 2. (Color online) Mulliken charge differences (in units of $|e|$) for n-doped vs intrinsic Si nanowires as a function of position x along the wire axis. Shown here is a donor at the origin.

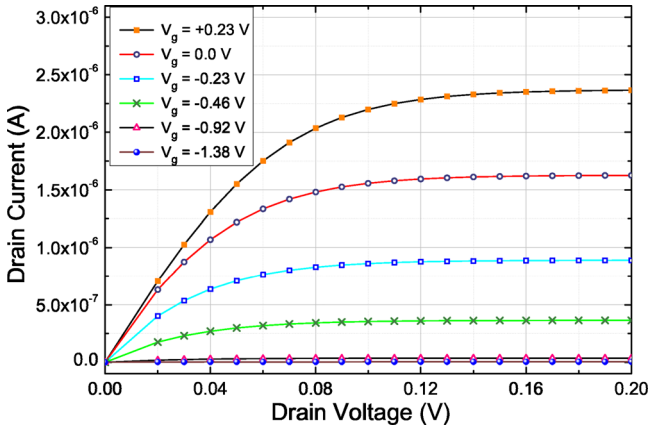


FIG. 3. (Color online) Room temperature I-V_{ds} characteristic for SiNW junctionless transistor doped n-type by As atoms with dimensions shown in Fig. 1.

very high doping concentrations N in the leads, typically $N=8\times10^{20}$ cm^{-3}, about ten times higher than in previous semiclassical simulations.[6] Nevertheless, this still gives just seven dopant atoms to be distributed within the ~800 atom supercell.

We used the electronic temperature $T_e=300$ K. However, due to the high N, we found the dopant band displays a large curvature. Moreover, the Fermi levels and band structures in the leads were consistent with many free carriers,

$$|E_F - E_d| \approx 350 \text{ meV}, \tag{1}$$

with E_d the edge of the dopant band. Taken together, these facts mean a high density of free carriers *independently* of whether the temperature is high enough for dopants to ionize. This can be explained by modeling a dopant atom as a hydrogenlike system with effective electron mass m^* and dielectric constant ϵ from Si.[10] Then the typical localization radius of the dopant electron or hole is

$$R_{\text{loc}} = \frac{m}{m^*}\epsilon\, a_0, \tag{2}$$

with a_0 the Bohr radius. Using $m^*/m=0.15$ for [110] SiNWs from our calculations[8] and the bulk value $\epsilon_{\text{Si}}=11.7$, we find $R_{\text{loc}}=4$ nm, even at 0 K. This is to compare to a dopant spacing of ~1 nm along the wire.

To understand this behavior better, we studied the Mulliken populations for our doped and undoped SiNWs. Mulliken population analysis[11] is a postprocessing step for localized-basis calculations yielding a charge associated with each atom. Figure 2 shows the Mulliken charge differences, $\Delta Q_i^M \equiv Q_i^M - Q_i^{M,0}$, where i is an atom index, Q_i^M is the Mulliken charge on atom i in the n-doped wire, and $Q_i^{M,0}$ is the Mulliken charge in the intrinsic wire. As shown in the figure, the donated electron de-localizes around the dopant atom with an exponential localization distance $R_{\text{loc}}=1.5$ nm (for the wave function), in rough agreement with Eq. (2). Further, Q_i^M differs from $Q_i^{M,0}$ throughout our supercell, confirming that at high N and in a thin nanowire, dopants do not have to ionize to contribute to the channel's "on" conductivity. Since $L_g \sim R_{\text{loc}}$, we predict that carriers are present in the channel region even when there are no dopant atoms there. This behavior, quite generally, makes standard *junctioned* nanowire transistors with small gate lengths difficult to achieve. By contrast, de-localization should make the junctionless design more robust against dopant fluctuations, a major design concern at these scales.

The calculations of Rurali *et al.*[12] show that dopant levels are very deep in thin SiNWs, making *isolated* dopants unlikely to ionize. However, for high N, this does not contradict our findings of Eq. (1) and the surrounding discussion. Furthermore, for n-doped [110] SiNWs of diameter $2R_{\text{NW}}=1$ nm, they found that a donated electron de-localizes significantly along the wire axis, consistent with our results. But for thicker wires, they found R_{loc} increasing from $R_{\text{loc}}=2$ Å for $2R_{\text{NW}}=1.5$ nm to $R_{\text{loc}}=2$ nm in bulk. For slightly thicker wires than the ones we model, localization could thus pose a challenge.

For our transport calculations at fixed V_g, first we solved the DFT Kohn–Sham equations under the influence of the applied external gating potential (as described above). This yields the correct ground state charge distribution within the channel in a self-consistent manner. Then, we computed the linear response conductance by the Landauer formula. We used our in-house transport code, TIMES (Ref. 7) to solve for the transmission function $T(E)$ from Green's functions for the DFT Hamiltonians. This nonself-consistent approach is valid as a linear response to V_{ds} but captures some non-Ohmic behavior because we integrate $T(E)$ rather than assume[13] that $dT/dE \ll 1/eV_{ds}$.

Because the device we model is heavily doped, screening of the leads from the gate takes place over a short length scale. Moreover, we include 1.9-nm-long contact regions on each side between the gated region and the leads as part of our atomic-scale simulation, so the leads are suitably screened from the channel.

Figures 3 and 4 show the calculated I-V_{ds} characteristics for n- and p-type junctionless devices, respectively. Clearly, these devices are on for $V_g=0$ V, and they turn off based on a pinch-off principle when V_g causes a sufficiently large barrier in the gating region. Short-channel effects are a serious issue at these length scales, as tunneling across the V_g barrier could undermine the device's effectiveness. To mitigate short-channel effects, a rule of thumb for GAA geometry requires gate length[1,2]

$$L_g > 2R_{\text{NW}},$$

a condition satisfied here by only a small margin.

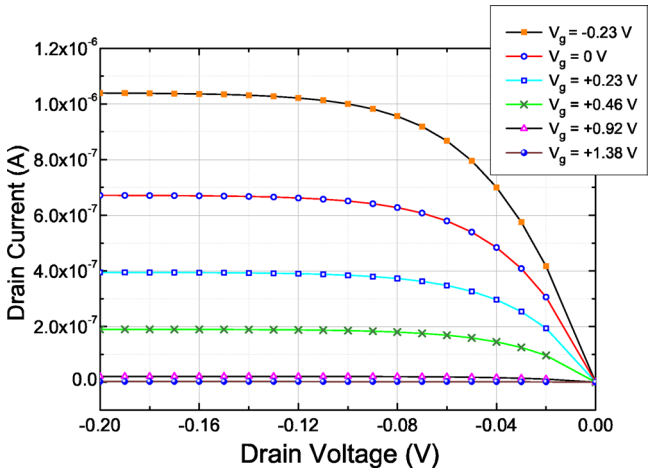


FIG. 4. (Color online) Room temperature I-V_{ds} characteristic for SiNW junctionless transistor doped p-type by Ga atoms.

However, GAA geometries are well-known to have superior gate control.[14,2] Our results confirm this remains true in the junctionless design even for gate lengths ~3 nm, enabling the devices to turn off. This is our most important finding.[15]

Nevertheless, our approximations limit our quantitative description of short-channel effects. For example, our prediction of the turnoff gate voltage V_{off} is an upper bound because of the lack of self-consistency in our non-equilibrium Green's function (NEGF) calculations and the limited supercell. Still, our calculations indicate a good subthreshold slope, and much better than for other nanoscale device designs.[1,2]

We found various effects of dopant positioning of relevance to prospective device design. First, as already mentioned, carrier delocalization blurs the junction boundary over a length scale R_{loc} comparable to the length L_g of the channel itself. This makes the junctionless transistor more robust against dopant fluctuations, while making a junctioned channel difficult to achieve.

We also found that the positioning of the dopant in the wire cross section makes a difference in the band structure of the device. A periodic array of dopants near the SiNW surface is found to create a dopant band that narrows the SiNW band gap, which is ordinarily about twice the band gap of bulk Si.[7] This narrowing leads to a steeper I-V_{ds} characteristic.

We have performed transport simulations on junctionless GAA SiNW devices of radius $R_{\text{NW}}=0.6$ nm and gate length $L_g=3.1$ nm. We predict that the junctionless transistor continues to work well at this scale, turning off with source-drain leakage $I_{\text{off}}<10^{-6}I_{\text{on}}$, and has good electrostatic control and a good subthreshold characteristic. By contrast, standard junctioned MOSFET designs are very difficult to fabricate at this scale. And, more importantly, the distribution of charge carriers around the dopant blurs the boundaries of a junction over a distance comparable to the channel length, so junctions at these scales would likely fail to keep carriers out of the channel.

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[15] We validated this by using $V_g=0$ V but introducing a uniform energy shift to the NEGF Hamiltonian in the gated region. This neglects capacitance and screening in the oxide and SiNW but enables us to quantify the tunneling current through the channel.