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In situ H_2S passivation of $In_{0.53}Ga_{0.47}As$ / InP metal-oxide-semiconductor capacitors with atomic-layer deposited HfO_2 gate dielectric

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In situ H_2S passivation of $In_{0.53}Ga_{0.47}As/InP$ metal-oxide-semiconductor capacitors with atomic-layer deposited HfO_2 gate dielectric

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We have studied an *in situ* passivation of $In_{0.53}Ga_{0.47}As$, based on H_2S exposure (50–350 °C) following metal organic vapor phase epitaxy growth, prior to atomic layer deposition of HfO_2 using $Hf[N(CH_3)_2]_4$ and H_2O precursors. X-ray photoelectron spectroscopy revealed the suppression of As oxide formation in air exposed InGaAs surfaces for all H_2S exposure temperatures. Transmission electron microscopy analysis demonstrates a reduction of the interface oxide between the $In_{0.53}Ga_{0.47}As$ epitaxial layer and the amorphous HfO_2 resulting from the *in situ* H_2S passivation. The capacitance-voltage and current-voltage behavior of $Pd/HfO_2/In_{0.53}Ga_{0.47}As/InP$ structures demonstrates that the electrical characteristics of samples exposed to 50 °C H_2S at the end of the metal-organic vapor-phase epitaxy $In_{0.53}Ga_{0.47}As$ growth are comparable to those obtained using an *ex situ* aqueous $(NH_4)_2S$ passivation. © *2008 American Institute of Physics*.
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In order to continue complementary metal oxide semiconductor (CMOS) development beyond the 22 nm node, alternative channel materials in combination with high dielectric constant (k) gate layers are currently under investigation. One of these approaches is to use high-mobility III-V materials such as InGaAs and GaAs as channel layers.[1–6] High mobility substrates offer the potential for increased transconductance at reduced voltages, increasing performance at supply voltages $\leqslant 1$ V. However, a significant factor which has inhibited the use of such materials is the lack of stable, high quality gate insulators on III-V channels. A gate oxide is required with high dielectric constant and sufficiently low density of interface states to avoid Fermi level pinning at the interface with the III-V substrate. As atomic layer deposition (ALD) of high-k dielectrics on Si is becoming a reality in manufactured devices, recent research is investigating this approach for use in III-V based devices.[7,8] A number of groups have also investigated surface passivation of the $In_xGa_{1-x}As$ substrate prior to oxide deposition.[9–11] *In situ* gaseous passivation is preferable to *ex situ* aqueous techniques which are more likely to introduce contaminants such as C, Na, and heavy metals, as well as increasing InGaAs surface roughness. In addition, both ALD and MOVPE are more attractive techniques than MBE for use in manufacturing technology. In this letter, we evaluate an *in situ* passivation performed at the end of the MOVPE growth of high indium content lattice matched $In_{0.53}Ga_{0.47}As$ grown on InP substrates. The technique is based on the exposure of the $In_{0.53}Ga_{0.47}As$ surface to H_2S at the end of the growth process, prior to gate dielectric formation. The approach is particularly suited to MOVPE III-V growth as H_2S is used as a n-type dopant source for InGaAs. The gate oxide employed in this work is ALD grown HfO_2 using the metal organic precursor $Hf[N(CH_3)_2]_4$.[12]

$In_{0.53}Ga_{0.47}As$ lattice-matched epitaxial layers of thickness 2 μm and S doped to $4\times10^{17}/cm^3$, were grown in a MOVPE system immediately following growth of a 0.1 μm InP buffer layer (S doped, $2\times10^{18}/cm^3$) on n-type InP(100) wafers (S doped, $(1-3)\times10^{18}/cm^3$). *In situ* passivation of the InGaAs surface was performed in the MOVPE chamber immediately after growth by flowing H_2S over the samples at a flow-rate of 0.1 SCCM (SCCM denotes cubic centimeter per minute at STP), at three different temperatures (50, 200, or 350 °C), for 90 min in a H_2 carrier gas. Subsequently the wafers were moved to an *ex situ* ALD reactor involving ~90 s ambient exposure. HfO_2 layers (~3–~15 nm) were deposited at a temperature of 250 °C by alternating pulses of H_2O and the HfO_2 precursor $Hf[N(CH_3)_2]_4$, the initial pulse being that of the Hf precursor. MOS structures were completed by vacuum evaporation of ~100 nm of Pd using a deposition rate of 2.5 Å/s, and lift-off, to define capacitors of various areas. No Ohmic back contacts to the InP were formed. *Ex situ* aqueous sulfur (S) passivation was performed in ambient by dipping InGaAs/InP samples in $(NH_4)_2S$ diluted to 20% in de-ionized water at ~60 °C for 20 min. The $Pd/HfO_2/In_{0.53}Ga_{0.47}As/InP$ structures examined in this work experienced no annealing following either dielectric deposition or gate metal formation.

Passivated InGaAs surfaces were studied using x-ray photoelectron spectroscopy (XPS), following ~60 s ambient exposure before loading to the XPS system, to evaluate the effectiveness of the *in situ* passivation approach in suppressing native oxide regrowth. XPS spectra of a sample passivated using *ex situ* aqueous $(NH_4)_2S$ are also included for comparison. Figure 1(a) shows a comparison of the S 2s peak for all samples. XPS does detect S on the InGaAs surface for both the 350 °C *in situ* passivated sample and the *ex*

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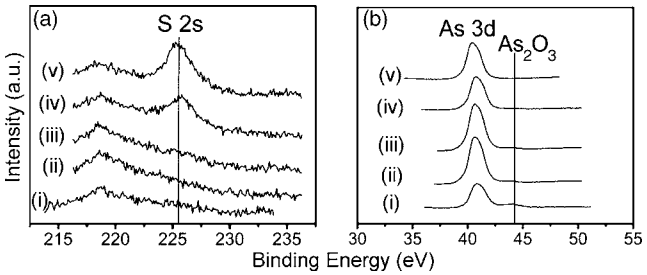

FIG. 1. XPS spectra of (a) the S 2*s* peak and (b) the As 3*d* peak for (i) unpassivated InGaAs, (ii) 50 °C, (iii) 200 °C, (iv) 350 °C *in situ* H_2S passivated InGaAs, and (v) *ex situ* aqueous $(NH_4)_2S$ passivated InGaAs.

situ aqueous S passivated sample, but in the case of the 50 and 200 °C *in situ* passivated samples no S is detected on the surface. XPS spectra of the As 3*d* core level for the unpassivated and passivated samples are shown in Fig. 1(b). This XPS peak is selected to examine the effect of the passivation on suppressing native oxide growth due to the large chemical shift between the As 3*d* peak and that of the arsenic oxide. In the case of the unpassivated sample, a peak is observed at ~45 eV and assigned to As_2O_3. In the case of all the *in situ* passivated samples this peak is not evident, indicating that this approach is effective in preventing As_2O_3 formation on the InGaAs surface. This is desirable as it has been reported that the unstable As_2O_3 can react to form elemental As which results in Fermi level pinning.[10,13] The absence of S on the surface of the 50 and 200 °C samples and the fact that As_2O_3 formation was inhibited on both, indicate that S may not be the primary passivating element in this process.

Figure 2(a) compares high frequency capacitance voltage (*CV*) curves for the unpassivated device and the various *in situ* passivation approaches for a nominal ALD HfO_2 thickness of 9 nm. The minimum capacitance (C_{min}), at $V_g = -2$ V, is approaching the expected theoretical value of 0.0019 F/m^2, calculated for these structures assuming inversion at the InGaAs/HfO_2 interface.[13] The device fabricated on the 50 °C *in situ* passivated surface (50 °C device) displays the highest maximum capacitance in accumulation (C_{max}) and also exhibits the sharpest transition from depletion to accumulation. The inset of Fig. 2(a) shows the current density-voltage (*JV*) characteristics for unpassivated and *in situ* passivated MOS structures. All structures exhibit low leakage current density ($<5\times10^{-7}$ A/cm^2 at $V_{fb}+1$ V), demonstrating that these ALD HfO_2 films on InGaAs are highly insulating. It is lowest in the case of the 50 °C device, $\sim5\times10^{-8}$ A/cm^2 at $V_{fb}+1$ V. Figure 2(b) shows multifrequency *CV* curves measured over the range of 1 kHz–1 MHz for the 50 °C device. The low frequency *CV* behavior observed in the 1 kHz curve has been reported previously in narrow bandgap materials.[14–16] The inset of Fig. 2(b) shows the *CV* hysteresis curve for the 50 °C device, which has the lowest measured hysteresis, ~380 mV around C_{fb}. These levels of frequency dispersion and hysteresis are to be expected as no postdeposition thermal anneal was performed on these MOS structures.[9] The fact that the 50 °C passivated device, which XPS showed to have no detectable S signal at the surface, displays the best electrical properties is further evidence that S is not the primary passivating element for the *in situ* process. It is possible to speculate that hydrogen may be passivating the InGaAs surface. One possibility is low temperature dissociative adsorption of H_2S to produce H–S and H species which may bond to As at the

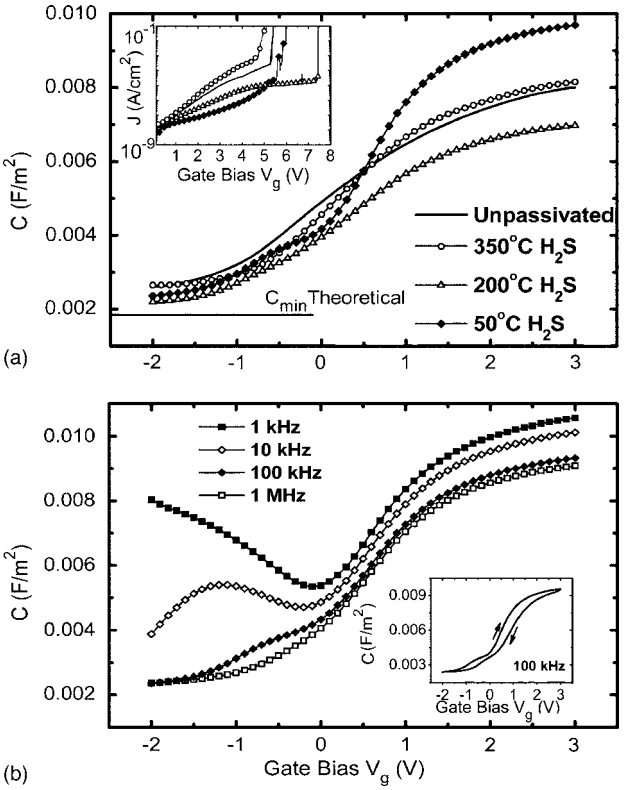

FIG. 2. (a) High frequency (100 kHz) capacitance-voltage characteristics and inset leakage current density as a function of gate bias (same legend), for unpassivated and *in situ* passivated Pd/9 nm(nominal) ALD HfO_2/InGaAs/InP MOS devices. (b) Multiple frequency *CV*, and inset hysteresis, curves for *in situ* 50 °C H_2S passivated InGaAs MOS device. No capacitance correction was made for inductive and resistive elements in the circuit. The average frequency dispersion of the flatband capacitance C_{fb}, is <3.5% per decade for all devices. The hysteresis measured around C_{fb} at 100 kHz was 460 mV for the unpassivated device, and 380, 585, and 410 mV for the 50, 200, and 350 °C *in situ* H_2S passivated devices, respectively.

epitaxial layer surface. This has been observed in previous studies of H_2S treatment of GaAs(001).[17] In addition, the fact that H species formed on the surface by H_2S dissociation will be in equilibrium with the H_2 MOVPE carrier gas may assist in allowing H passivation to occur by reducing hydrogen desorption from the surface. The possibility that hydrogen passivation occurs in this process is subject to further investigation.

Figure 3(a) shows a bright field transmission electron microscopy (TEM) micrograph for a 50 °C *in situ* H_2S passivated InGaAs device with a 9.4 nm HfO_2 layer and a 0.8 nm thick interfacial layer (IL) between the HfO_2 and InGaAs. This is less than half the thickness of the IL of 1.9 nm measured by TEM for the unpassivated device [Fig. 3(b)]. This indicates that this *in situ* passivation technique is effective in significantly inhibiting interfacial oxide growth. Considering that the maximum H_2S flow rate was limited to 0.1 SCCM in this MOVPE process, there is scope for refinement and potential improvement of this *in situ* passivation technique.

CV curves for a thickness series of 3, 9.4, and 16.8 nm thick ALD HfO_2 layers on 50 °C *in situ* passivated InGaAs are shown in Fig. 4(a). The inset plots the *JV* response for the three thicknesses. As expected, the leakage current density at $V_{fb}+1$ V is significantly higher for the 3 nm device, $\sim2\times10^{-6}$ A/cm^2, compared to $\sim3\times10^{-8}$ A/cm^2 and 2×10^{-8} A/cm^2 for the 9.4 and 16.8 nm devices, respectively.

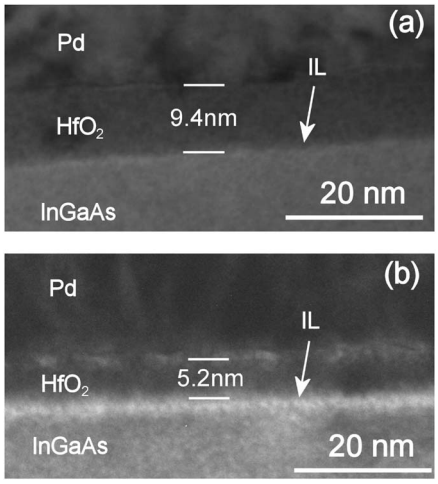

FIG. 3. Bright field TEM micrographs of Pd/9 nm(nominal) ALD HfO_2/InGaAs/InP MOS devices for (a) *in situ* 50 °C H_2S passivated InGaAs and (b) unpassivated InGaAs. The actual HfO_2 layer [and interfacial layer (IL)] thicknesses measured by TEM were 5.2 nm (1.9 nm IL) unpassivated device, 9.4 nm (0.8 nm IL) 50 °C device, 13.5 nm (0.9 nm IL) 200 °C device, 10.8 nm (0.9 nm IL) 350 °C device, and 11 nm (1.3 nm IL) $(NH_4)_2S$ passivated device.

For these HfO_2 layers, we estimate a HfO_2 k value of ~23. Figure 4(b) compares the electrical characteristics of a 9.4 nm thick ALD HfO_2 layer (0.8 nm IL) deposited on InGaAs passivated *in situ* by H_2S flow at 50 °C, and an 11 nm thick ALD HfO_2 layer (1.3 nm IL) on InGaAs passivated *ex situ* in aqueous $(NH_4)_2S$. Although a slight V_{fb} shift is apparent, a similar profile is observed in the *CV* curves of both devices. Both devices have a similar C_{max} in accumulation while the *in situ* passivated device appears to have slightly higher interface state density. The *JV* plot in the inset of Fig. 4(b) shows similar leakage current density at V_{fb} +1 V with a higher electric breakdown field for the *in situ*

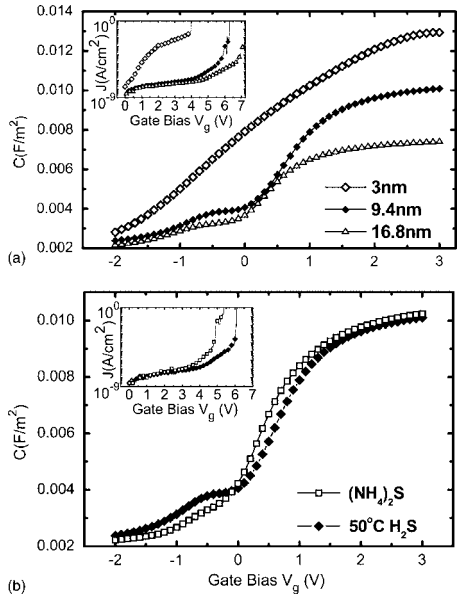

FIG. 4. (a) *CV* (100 kHz) curves and inset *JV* (same legend) for nominal 3, 9, and 15 nm thick ALD HfO_2 layers on 50 °C *in situ* passivated InGaAs. The actual HfO_2 (and IL) thicknesses from TEM were 3 nm (0.8 nm IL), 9.4 nm (0.8 nm IL), and 16.8 nm (0.9 nm IL). No significant degradation of the bulk and interface properties is observed after repeated *CV* measurement of the MOS structures. (b) *CV* (100 kHz) and inset *JV* (same legend) characteristics for *in situ* 50 °C H_2S passivated and *ex situ* aqueous $(NH_4)_2S$ passivated devices.

passivated device. This demonstrates that the *in situ* passivation approach employed in this work can achieve results comparable to those obtained using *ex situ* aqueous $(NH_4)_2S$ passivation.

In summary, we have studied an *in situ* passivation of $In_{0.53}Ga_{0.47}As$ performed using the H_2S dopant source (50–350 °C) at the end of MOVPE growth prior to deposition of ALD HfO_2. XPS analysis revealed the suppression of As oxide growth on *in situ* passivated InGaAs layers. The MOS device, which experienced a passivation temperature of 50 °C, displays the best electrical characteristics, with TEM indicating a significant reduction in interfacial oxide thickness compared to the unpassivated and $(NH_4)_2S$ passivated devices. The potential for developing this passivation approach for use in future CMOS applications is demonstrated by the fact that results comparable to those obtained using *ex situ* aqueous $(NH_4)_2S$ passivation can be achieved.

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