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Simulation of Multigate SOI Transistors with Silicon, Germanium and III-V Channels

Pedram Razavi

A thesis submitted in accordance with the requirements for the degree of

Doctor of Philosophy



NATIONAL UNIVERSITY OF IRELAND, CORK

School of Engineering

Department of Electrical and Electronic Engineering

August 2013

Supervisors: Prof. Jean-Pierre Colinge

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Declaration

This thesis is the candidate's own work and has not been submitted for another degree, either at the University College Cork or elsewhere.

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Abstract

In this work by employing numerical three-dimensional simulations we study the electrical performance and short channel behavior of several multi-gate transistors based on advanced SOI technology. These include FinFETs, triple-gate and gate-all-around nanowire FETs with different channel material, namely Si, Ge, and III-V compound semiconductors, all most promising candidates for future nanoscale CMOS technologies. Also, a new type of transistor called "junctionless nanowire transistor" is presented and extensive simulations are carried out to study its electrical characteristics and compare with the conventional inversion- and accumulation-mode transistors. We study the influence of device properties such as different channel material and orientation, dimensions, and doping concentration as well as quantum effects on the performance of multi-gate SOI transistors. For the modeled n-channel nanowire devices we found that at very small cross sections the nanowires with silicon channel are more immune to short channel effects. Interestingly, the mobility of the channel material is not as significant in determining the device performance in ultrashort channels as other material properties such as the dielectric constant and the effective mass. Better electrostatic control is achieved in materials with smaller dielectric constant and smaller source-to-drain tunneling currents are observed in channels with higher transport effective mass. This explains our results on Si-based devices.

In addition to using the commercial TCAD software (Silvaco and Synopsys TCAD), we have developed a three-dimensional Schrödinger-Poisson solver based on the non-equilibrium Green's functions formalism and in the framework of effective mass approximation. This allows studying the influence of quantum effects on electrical performance of ultra-scaled devices. We have implemented different mode-space methodologies in our 3D quantum-mechanical simulator and moreover introduced a new method to deal with discontinuities in the device structures which is much faster than the coupled-mode-space approach.

List of publications

Journal papers

(I) Based on results presented in this thesis:

[1] "Performance comparison of III-V junctionless nanowire transistors and inversion-mode devices," **P. Razavi**, G. Fagas, *Applied Physics Letters*, vol. 103, p. 063506, 2013.

[2] "Influence of channel material properties on performance of nanowire transistors," **P. Razavi**, G. Fagas, I. Ferain, R. Yu, S. Das, and J.-P. Colinge, *Journal of Applied Physics*, vol. 111, pp. 124509-124509-8, 2012.

[3] "A Simulation Comparison between Junctionless and Inversion-Mode MuGFETs," J.-P. Colinge, A. Kranti, R. Yan, I. Ferain, N. D. Akhavan, **P. Razavi**, C.-W. Lee, , R. Yu, and C. Colinge, *ECS Trans.,* vol. 35, issue 5, pp, 63-72, 2011.

[4] "Improvement of carrier ballisticity in junctionless nanowire transistors," N. D. Akhavan, I. Ferain, **P. Razavi**, R. Yu, and J.-P. Colinge, *Applied Physics Letters*, vol. 98, p. 103510, 2011.

[5] "Junctionless Nanowire Transistor (JNT): Properties and design guidelines," J.-P. Colinge, A. Kranti, R. Yan, C. Lee, I. Ferain, R. Yu, N. D. Akhavan, **P. Razavi**, *Solid-State Electronics*, vol. 65-66, pp. 33-37, 2011.

[6] "Performance estimation of junctionless multigate transistors," C.-W. Lee, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, **P. Razavi**, and J.-P. Colinge, *Solid-State Electronics*, vol. 54, pp. 97-103, 2010.

[7] "LDD and Back-Gate Engineering for Fully Depleted Planar SOI Transistors with Thin Buried Oxide," R. Yan, R. Duane, **P. Razavi**, A. Afzalian, I. Ferain, C.-W. Lee, N. D. Akhavan, B.-Y. Nguyen, K.K. Bourdelle, and and J.-P. Colinge, *Electron Devices, IEEE Transactions on*, vol. 57, pp. 1319-1326, 2010.

[8] "Nanowire transistors without junctions," J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, **P. Razavi**, B. O'Neill, A. Blake, and M. White, *Nature nanotechnology*, vol. 5, pp. 225-229, 2010.

[9] "A new F (ast)-CMS NEGF algorithm for efficient 3D simulations of switching characteristics enhancement in constricted tunnel barrier silicon nanowire

MuGFETs," A. Afzalian, N. D. Akhavan, C.-W. Lee, R. Yan, I. Ferain, **P. Razavi**, and J.-P. Colinge, *Journal of computational electronics*, vol. 8, pp. 287-306, 2009.

(II) Other contributions of the author

[10] "Impact ionization induced dynamic floating body effect in junctionless transistors," R. Yu, A. N. Nazarov, V. S. Lysenko, S. Das, I. Ferain, **P. Razavi**, M. Shayesteh, A. Kranti, R. Duffy, J-P. Colinge, Solid-State Electronics, (Article in press) 2013.

[11] "Device Design and Estimated Performance for p-Type Junctionless Transistors on Bulk Germanium Substrates," R. Yu, S. Das, I. Ferain, **P. Razavi**, M. Shayesteh, A. Kranti, R. Duffy, and J-P. Colinge, Electron Devices, IEEE Transactions on, vol. 59, pp. 2308-2313, 2012.

[12] "Mobility enhancement effect in heavily doped junctionless nanowire silicon-on-insulator metal-oxide-semiconductor field-effect transistors," T. Rudenko, A. Nazarov, I. Ferain, S. Das, R. Yu, S. Barraud, **P. Razavi**, Applied Physics Letters, vol. 101, p. 213502, 2012.

[13] "Emission and absorption of optical phonons in Multigate Silicon Nanowire MOSFETs," N. Dehdashti Akhavan, I. Ferain, R. Yu, **P. Razavi**, and J.-P. Colinge, Journal of Computational Electronics, vol. 11, pp. 249-265, 2012.

[14] "Influence of discrete dopant on quantum transport in silicon nanowire transistors," N. D. Akhavan, I. Ferain, R. Yu, **P. Razavi**, and J.-P. Colinge, *Solid-State Electronics*, vol. 70, pp. 92–100, 2012.

[15] "Bipolar effects in unipolar junctionless transistors,"M. S. Parihar, D. Ghosh, G. A. Armstrong, R. Yu, **P. Razavi**, and A. Kranti, Applied Physics Letters, vol. 101, pp. 093507-093507-3, 2012.

[16] "Characterization of a junctionless diode," R. Yu, I. Ferain, N. D. Akhavan, **P. Razavi**, R. Duffy, and J.-P. Colinge, Applied Physics Letters, vol. 99, p. 013502, 2011.

[17] "Investigation of high-performance sub-50 nm junctionless nanowire transistors," R. Yan, A. Kranti, I. Ferain, C.-W. Lee, R. Yu, N. Dehdashti, **P. Razavi**, and J.-P. Colinge, Microelectronics Reliability, vol. 51, pp. 1166-1171, 2011.

[18] "Comparative Study of Random Telegraph Noise in Junctionless and Inversion-Mode MuGFETs," A. Nazarov, C.-W. Lee, A. Kranti, I. Ferain, R. Yan, N. D. Akhavan, P. Razavi, R. Yu, J.-P. Colinge, *ECS Trans.,* vol. 35, issue 5, pp.73-78, 2011.

[19] "Analog Operation Temperature Dependence of nMOS Junctionless Transistors Focusing on Harmonic Distortion," R. T. Doria, M. A. Pavanello, R. D. Trevisoli, M. de Souza, C.-W. Lee, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, R. Yu, A. Kranti, and J.-P. Colinge, Journal of Integrated Circuits and Systems, vol. 6, pp. 114-121, 2011.

[20] "Junctionless Multiple-Gate Transistors for Analog Applications," R. T. Doria, M. A. Pavanello, R. D. Trevisoli, M. de Souza, C.-W. Lee, I. Ferain, N. D. Akhavan, R. Yan, **P. Razavi**, R. Yu, A. Kranti, and J.-P. Colinge, Electron Devices, IEEE Transactions on, vol. 58, No. 8, pp. 2515-2519, 2011.

[21] "Field-effect mobility extraction in nanowire field-effect transistors by combination of transfer characteristics and random telegraph noise measurements,"A. Nazarov, I. Ferain, N. D. Akhavan, **P. Razavi**, R. Yu, and J. Colinge, Applied Physics Letters, vol. 99, p. 073502, 2011.

[22] "Random telegraph-signal noise in junctionless transistors,"A. Nazarov, I. Ferain, N. D. Akhavan, **P. Razavi**, R. Yu, and J.-P. Colinge, Applied Physics Letters, vol. 98, p. 092111, 2011.

[23] "Nanowire to Single-Electron Transistor Transition in Trigate SOI MOSFETs," N. D. Akhavan, A. Afzalian, C.-W. Lee, R. Yan, I. Ferain, **P. Razavi**, R. Yu. G. Fagas, J-P. Colinge, Electron Devices, IEEE Transactions on, vol. 58, pp. 26-32, 2011.

[24] "Junctionless Nanowire Transistor: Complementary Metal-Oxide-Semiconductor Without Junctions," J.-P. Colinge, I. Ferain, A. Kranti, C.-W. Lee, N. D. Akhavan, **P. Razavi**, R. Yan, and R. Yu, Science of Advanced Materials, vol. 3, pp. 477-482, 2011.

[25] "Junctionless Transistors: Physics and Properties," J.-P. Colinge, C. Lee, N. Dehdashti Akhavan, R. Yan, I. Ferain, **P. Razavi**, A.Kranti, and R.Yu, Semiconductor-On-Insulator Materials for Nanoelectronics Applications, pp. 187-200, 2011.

[26] "Influence of Elastic and Inelastic Electron–Phonon Interaction on Quantum Transport in Multigate Silicon Nanowire MOSFETs,"N. D. Akhavan, A. Afzalian,

A. Kranti, I. Ferain, C.-W. Lee, R. Yan, **P. Razavi**, Ran Yu, and J.-P. Colinge, *Electron Devices, IEEE Transactions on*, vol. 58, pp. 1029-1037, 2011.

[27] "The Roles of the Electric Field and the Density of Carriers in the Improved Output Conductance of Junctionless Nanowire Transistors," R. T. Doria, M. A. Pavanello, R. D. Trevisoli, M. De Souza, C.-W. Lee, I. Ferain, N. D. Akhavan, R. Yan, **P. Razavi**, R. Yu, A. Kranti, J.-P. Colinge, ECS Trans., vol. 35, issue 5, pp, 283-288, 2011.

[28] "Junctionless 6T SRAM cell," A. Kranti, C.-W. Lee, I. Ferain, R. Yan, N. Akhavan, **P. Razavi**, R. Yu, G.A. Armstrong, and J-P. Colinge, Electronics letters, vol. 46, pp. 1491-1493, 2010.

[29] "Low subthreshold slope in junctionless multigate transistors," C.-W. Lee, A. N. Nazarov, I. Ferain, N. D. Akhavan, R. Yan, **P. Razavi**, R. Yu, R. T. Doria, J-P. Colinge, Applied Physics Letters, vol. 96, p. 102106, 2010.

[30] "High-temperature performance of silicon junctionless MOSFETs," C.-W. Lee, A. Borne, I. Ferain, A. Afzalian, R. Yan, N. Dehdashti Akhavan, **P. Razavi**, and J.-P. Colinge, Electron Devices, IEEE Transactions on, vol. 57, pp. 620-625, 2010.

[31] "Analog Operation and Harmonic Distortion Temperature Dependence of nMOS Junctionless Transistors," R. T. Doria, M. A. Pavanello, C.-W. Lee, I. Ferain, N. Dehdashti-Akhavan, R. Yan, **P. Razavi**, R. Yu, A. Kranti and J.-P. Colinge, ECS Trans., vol. 31, issue 1, pp, 13-20, 2010.

[32] "Reduced electric field in junctionless transistors," J.-P. Colinge, C.-W. Lee, I. Ferain, N. D. Akhavan, R. Yan, **P. Razavi**, R. Yu, A. N. Nazarov, and R. T. Doria, Applied Physics Letters, vol. 96, p. 073510, 2010.

[33] "Effect of intravalley acoustic phonon scattering on quantum transport in multigate silicon nanowire metal-oxide-semiconductor field-effect transistors," N. D. Akhavan, A. Afzalian, C.-W. Lee, R. Yan, I. Ferain, **P. Razavi**, R. Yu, G. Fagas, and J-P. Colinge, Journal of Applied Physics, vol. 108, pp. 034510-034510-8, 2010.

[34] "Simulation of quantum current oscillations in trigate SOI MOSFETs," N. D. Akhavan, A. Afzalian, C.-W. Lee, R. Yan, I. Ferain, **P. Razavi**, G. Fagas, and J-P. Colinge, Electron Devices, IEEE Transactions on, vol. 57, pp. 1102-1109, 2010.

[35] "NBTI and hot-carrier effects in accumulation-mode Pi-gate pMOSFETs," C.-W. Lee, I. Ferain, A. Afzalian, R. Yan, N. Dehdashti, **P. Razavi**, J-P. Colinge, and J. T. Park, Microelectronics Reliability, vol. 49, pp. 1044-1047, 2009.

Conference papers

(I) Based on results presented in this thesis:

[1] "Electron transport in germanium junctionless nanowire transistors," **P. Razavi**, G. Fagas, I. Ferain, R. Yu, and S. Das, *in Solid-State Device Research Conference (ESSDERC), 2012 Proceedings of the European*, 2012, pp. 326-329. [Oral presentation]

[2] "Intrinsic gate delay and energy-delay product in junctionless nanowire transistors," **P. Razavi**, I. Ferain, S. Das, R. Yu, N. D. Akhavan, and J.-P. Colinge, *in Ultimate Integration on Silicon (ULIS), 2012 13th International Conference on*, 2012, pp. 125-128. [Poster presentation]

[3] "Performance investigation of short-channel junctionless multigate transistors," **P. Razavi**, G. Fagas, I. Ferain, N. D. Akhavan, R. Yu, and J.-P. Colinge, *in Ultimate Integration on Silicon (ULIS), 2011 12th International Conference on*, 2011, pp. 1-4. [Poster presentation]

[4] "Investigation of Short-Channel Effects in Junctionless Nanowire Transistors," **P. Razavi**, N. Dehdashti-Akhavan, R. Yu, G. Fagas, I. Ferain, and J.-P. Colinge, *International Conference on Solid State Devices and Materials (SSDM2011)*, Nagoya, Japan, 2011. [Poster presentation]

[5] "Comparison of the switching speed in junctionless and accumulation-mode gate-all-around nanowire transistors," **P. Razavi**, R. Yan, I. Ferain, N. Dehdashti Akhavan, R. Yu, and J.-P. Colinge, *Proceedings of EUROSOI 2011*, *VII Workshop of the Thematic Network on Silicon On Insulator Technology, Devices and Circuits*, 2011. [Oral presentation]

[6] "Comparison of Breakdown Voltage in Bulk and SOI FinFETs," **P. Razavi**, R.Duane, R. Yan, I. Ferain, N. Dehdashti Akhavan, R. Yu, C.-W. Lee, and J.-P. Colinge, *in Proceedings of EUROSOI Conference*, 2010. [Oral presentation]

[7] "Short-channel junctionless nanowire transistors," C. Lee, I. Ferain, A. Kranti, N. D. Akhavan, **P. Razavi**, R. Yan, R. Yu, B. O'Neill, A. Blake, M. White, A.M. Kelleher, B. McCarthy, S. Gheorghe, R. Murphy, and J.-P. Colinge, *International Conference on Solid State Devices and Materials (SSDM 2010)*, pp. 1044-1045, 2010.

[8] "Back-gate mirror doping for fully depleted planar SOI transistors with thin buried oxide," R. Yan, R. Duane, **P. Razavi**, A. Afzalian, I. Ferain, C.-W. Lee, N.

Dehdashti, B.-Y. Nguten, K. K. Bourdelle, and J.-P. Colinge, *in VLSI Technology Systems and Applications (VLSI-TSA), 2010 International Symposium on*, 2010, pp. 76-77.

[9] "A new F (ast)-CMS Algorithm for Efficient Three-Dimensional NEGF Simulations of Arbitrarily Shaped Silicon Nanowire MUGFETs," A. Afzalian, C.-W. Lee, N. D. Akhavan, R. Yan, I. Ferain, **P. Razavi**, and J.-P. Colinge, *in Simulation of Semiconductor Processes and Devices, 2009. SISPAD'09. International Conference on*, 2009, pp. 1-4.

[10] "LDD depletion effects in thin-BOX FDSOI devices with a ground plane," R. Yan, R. Duane, **P. Razavi**, A. Afzalian, I. Ferain, C. Lee, N. Dehdashti-Akhavan, K. Bourdelle, B. Nguyen, and J.-P. Colinge, *in SOI Conference, 2009 IEEE International*, 2009, pp. 1-2.

[11] "SOI gated resistor: CMOS without junctions," J.-P. Colinge, C. Lee, A. Afzalian, N. Dehdashti, R. Yan, I. Ferain, **P. Razavi**, B. O'Neill, A. Blake, and M. White, *in SOI Conference, 2009 IEEE International*, 2009, pp. 1-2.

(II) Other contributions of the author:

[12] "Sensitivity analysis of steep subthreshold slope (S-slope) in Junctionless nanotransistors," M. S. Parihar, D. Ghosh, G. A. Armstrong, R. Yu, **P. Razavi**, S. Das, I. Ferain, and A. Kranti, *in Nanotechnology (IEEE-NANO), 2012 12th IEEE Conference on*, 2012, pp. 1-4.

[13] "Top-down process of Germanium nanowires using EBL exposure of Hydrogen Silsesquioxane resist," R. Yu, S. Das, R. Hobbs, Y. Georgiev, I. Ferain, **P. Razavi**, N. D. Akhavan, C. A. Colinge, and J.-P. Colinge, *in Ultimate Integration on Silicon (ULIS), 2012 13th International Conference on, 2012*, pp. 145-148.

[14] "Extraction of channel mobility in nanowire MOSFETs using Id (Vg) characteristics and random telegraph noise amplitude," A. Nazarov, C. Lee, A. Kranti, I. Ferain, R. Yan, N. D. Akhavan, **P. Razavi**, R. Yu, and J.-P. Colinge, *in Ultimate Integration on Silicon (ULIS), 2011 12th International Conference on*, 2011, pp. 1-3.

[15] "Influence of single-atom impurity scattering on quantum transport in silicon nanowire transistors," N. Dehdashti Akhavan, I. Ferain, R. Yan, **P. Razavi**, R. Yu,

and J.-P. Colinge, *in Proceedings of EUROSOI Conference*, *VII Workshop of the Thematic Network on Silicon On Insulator Technology, Devices and Circuits*, 2011.

[16] "Random dopant variation in junctionless nanowire transistors,"N. D. Akhavan, I. Ferain, **P. Razavi**, R. Yu, and J.-P. Colinge, *in SOI Conference (SOI), 2011 IEEE International*, 2011, pp. 1-2.

[17] "Junctionless nanowire transistor (JNT): Properties and design guidelines," A. Kranti, R. Yan, C.-W. Lee, I. Ferain, R. Yu, N. D. Akhavan, **P. Razavi**, and J. Colinge*, in Solid-State Device Research Conference (ESSDERC), 2010 Proceedings of the European*, 2010, pp. 357-360.

[18] "Analog operation of junctionless transistors at cryogenic temperatures," R. Doria, M. Pavanello, R. Trevisoli, M. de Souza, C. Lee, I. Ferain, N. Dehdashti Akhavan, R. Yan, **P. Razavi**, R. Yu, A. Kranti, and J.-P. Colinge *in SOI Conference (SOI), 2010 IEEE International*, 2010, pp. 1-2.

[19] "Dissipative transport in Multigate silicon nanowire transistors," N. Dehdashti, A. Kranti, I. Ferain, C.-W. Lee, R. Yan, **P. Razavi**, R. Yu, and J.-P. Colinge*, in Simulation of Semiconductor Processes and Devices (SISPAD), 2010 International Conference on*, 2010, pp. 97-100.

[20] "Emission and absorption of optical phonons in multigate silicon nanowire MOSFETs," N. Dehdashti, A. Kranti, I. Ferain, C. W. Lee, R. Yan, **P. Razavi**, R. Yu, and J.-P. Colinge, *in Computational Electronics (IWCE), 2010 14th International Workshop on*, 2010, pp. 1-4.

[21] "Electric Field in Junctionless MuGFETs," J.-P. Colinge, C.-W. Lee, I. Ferain, N. Dehdashti Akhavan, R. Yan, **P. Razavi**, R. Yu, A.N. Nazarov, and R. T. Doria, *in Proceedings of EUROSOI Conference*, 2010.

[22] "Nanowire zero-capacitor DRAM transistors with and without junctions," C.-W. Lee, R. Yan, I. Ferain, A. Kranti, N. Akhvan, **P. Razavi**, R. Yu, and J.-P. Colinge, *in Nanotechnology (IEEE-NANO), 2010 10th IEEE Conference on*, 2010, pp. 242-245.

[23] "Emission and absorption of optical phonons in multigate silicon nanowire MOSFETs," N. Dehdashti, A. Kranti, I. Ferain, C. Lee, R. Yan, **P. Razavi**, R. Yu, and J.-P. Colinge, *in Computational Electronics (IWCE), 2010 14th International Workshop on*, 2010, pp. 1-4.

[24] "Junctionless Multiple Gate Transistors Performance for Analog Applications," R.T. Doria, M.A. Pavanello, C.-W. Lee, I. Ferain, N. Dehdashti

Akhavan, R. Yan, **P. Razavi**, R. Yu, and J.-P.Colinge, *in Proceedings of EUROSOI Conference*, 2010.

[25] "3D Simulation of RTS Amplitude in Accumulation-Mode and Inversion-Mode Trigate SOI MOSFETs,"R. Yan, A. Cullen, A. Afzalian, I. Ferain, C.-W. Lee, N. Dehdashti Akhavan, **P. Razavi**, and J.-P. Colinge, *in Proceedings of EUROSOI Conference*, 2010.

[26] "Substrate bias effects in MuGFETs," C.-W. Lee, A. Borne, I. Ferain, A. Afzalian, R. Yan, N. Dehdashti Akhavan, **P. Razavi**, and J.-P. Colinge, *in Proceedings of EUROSOI Conference*, 2010.

[27] "Effect of intravalley acoustic phonon scattering on mobility in silicon nanowire transistor," N. Dehdashti Akhavan, A. Afzalian, C.-W. Lee, R. Yan, I. Ferain, **P. Razavi**, and J.-P. Colinge, *in Proceedings of EUROSOI Conference*, 2010.

[28] "Hot carrier (HC) and bias-temperature-instability (BTI) degradation of MuGFETs on silicon oxide and silicon nitride buried layers," C.-W. Lee, I. Ferain, A. Afzalian, K.-Y. Byun, R. Yan, N. Dehdashti, **P. Razavi**, W. Xiong, J.-P. Colinge, and C. Colinge, *in Solid State Device Research Conference, 2009. ESSDERC'09. Proceedings of the European*, 2009, pp. 261-264.

[29] "Variable-barrier tunneling SOI transistor (VBT),"A. Afzalian, N. Dehdashti, I. Ferain, C. Lee, R. Yan, **P. Razavi**, and J.-P. Colinge, *in SOI Conference, 2009 IEEE International*, 2009, pp. 1-2.

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Chapter 1 : Introduction

1.1. Scaling of CMOS technology

Electronics products and their related services hold considerable a share of today's world economy. Since the concept of an integrated circuit (IC) was introduced by J. Kilby in 1958, the number of electronic components on a microchip has increased exponentially with time while the performance of transistors on a microchip has also been improved. In 1965 Gordon Moore predicted that the number of transistors on a chip would be doubled every 18 month, which has been valid for the past four decades. However, conventional MOSFET structures are reaching scaling limits and short-channel effects (SCEs) have become a huge problem for end-of-the-roadmap technologies. In an ideal MOSFET the channel potential is controlled by the gate electrode only, however, in devices with a very short channel length the drain potential can significantly influence the channel potential and degrade the control of the gate on the channel potential. This causes the short-channel effects that degrade the device performance. This degradation includes the drain-induced barrier lowering (*DIBL*), increased off-state leakage current (I_{off}) and subthreshold swing (*SS*), and the threshold voltage roll-off. These short-channel effects can jeopardize CMOS scaling. Decreasing the gate oxide thickness and the source/drain junction depth while decreasing the gate length, has been used to minimize these short-channel effects in conventional bulk MOSFETs. However, scaling of the SiO_2 gate oxide reached a physical limitation at around ~2nm due to the increased gate leakage current caused by the tunneling through the oxide. For this reason higher permittivity materials were proposed to be used as gate dielectrics. These allow further reduction of the equivalent oxide thickness (*EOT*) while using a physically thicker oxide. This helps to prevent the gate tunneling and allows for further scaling of MOSFETs. Nevertheless, shrinking MOSFETs to the sub-10nm regime can lead to a huge direct tunneling between source and drain which degrades the subthreshold swing, increases the leakage current and limits further scaling due to a huge increase of power dissipation. These are some of the serious challenges for the scaling of nanotransistors.

1.2. Advanced CMOS technology

Silicon-on-Insulator (SOI) technology is able to solve some of the physical limits of bulk CMOS [1-3]. In SOI technology, transistors are made in a thin silicon layer sitting on top of a silicon dioxide layer. SOI technology is being used in many major semiconductor companies such as IBM, AMD and ST Microelectronics. SOI technology can push CMOS scaling beyond the limits of classical silicon devices [4-6].

A schematic view of the bulk and SOI multi-gate FET, as well as, the cross-section of different multi-gate FET (MuGFET) structures and their effective number of gates are shown in Figure 1.1 [7-12].

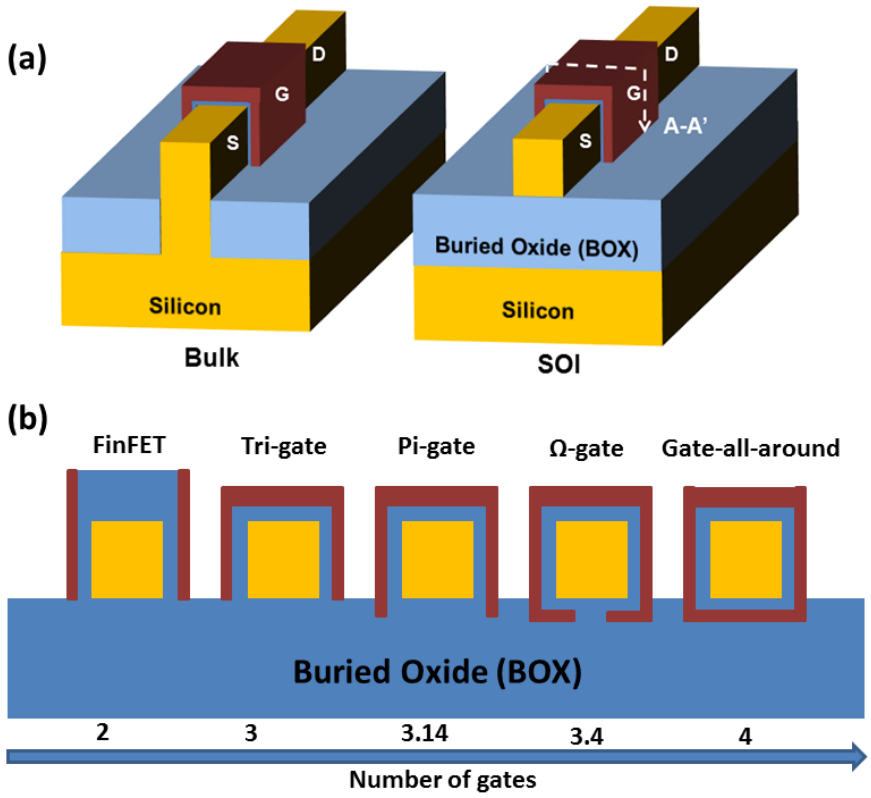


Figure 1.1 – Schematic of (a) bulk and SOI multi-gate FETS, as well as, (b) cross-section of different multi-gate FETS and their corresponding effective number of gates.

The small silicon thickness of an SOI MOSFET can effectively suppress the leakage current compared to the conventional bulk MOSFET. This is done by eliminating the part of the channel region that cannot be effectively controlled by the gate. However, this may not be practical for very short devices as the channel thickness of a planar single gate SOI MOSFET needs to be ultra-thin ($T_{si}/4<L_{gate}$) to suppress SCEs. But increasing the number of gates can increase the gate control

ability and relax the body thickness. In multiple-gate devices, the gate electrode is wrapped around a silicon wire to increase the gate control ability of the channel carriers. According to the International Technology Roadmap for Semiconductor (ITRS) the multiple-gate SOI MOSFETs can be scaled to sub-10nm dimensions and are promising candidates for future nanoelectronic devices (Figure 1.2 [13]).

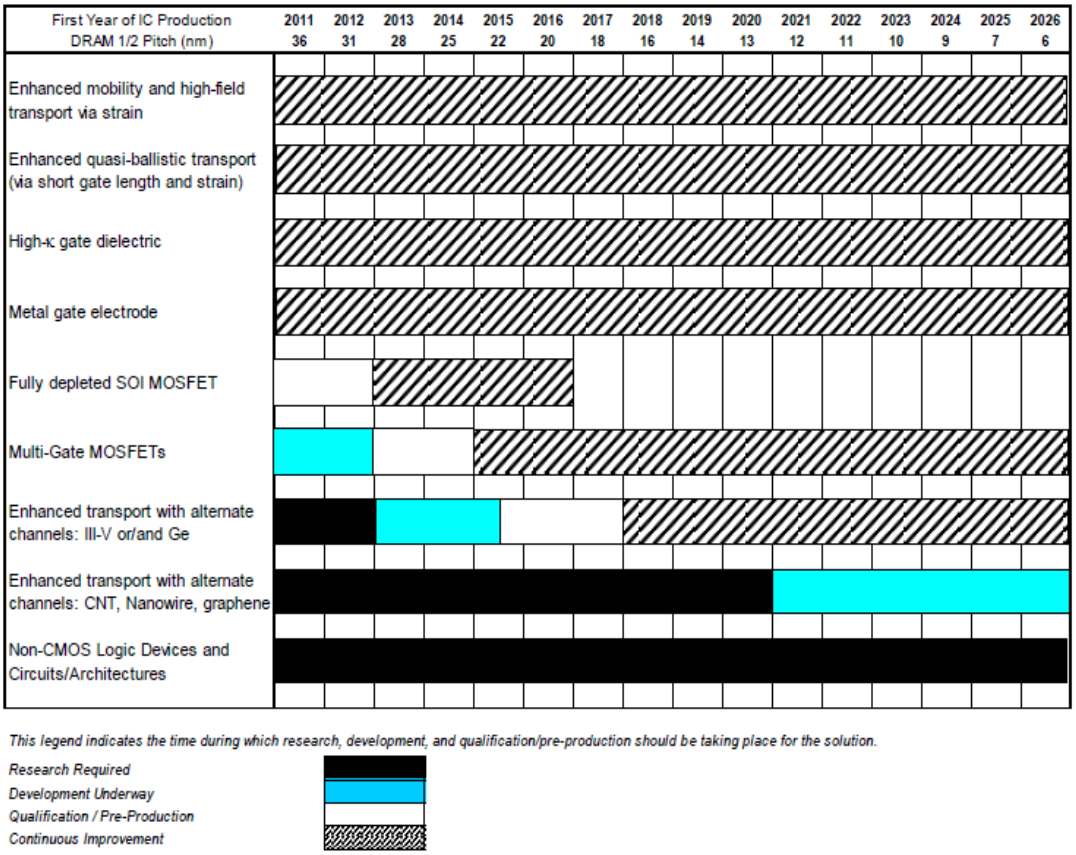


Figure 1.2 - Evaluation of potential solutions for logic CMOS [Source: ITRS Edition 2011].

1.3. New type of MOSFET

Conventional Metal Oxide Semiconductor (MOS) transistors are made of two PN junctions (the source-channel junction and the drain-channel junction). For example, the n-channel MOSFET has an N-P-N structure while the p-channel device has a P-N-P structure. To make faster and smaller devices for the electronic industry, scaling transistors down to the nano-scale regime is necessary. This scaling raises significant manufacturing challenges for semiconductor companies. Forming source/drain junctions in classical MOSFETs with very short channel length is very challenging because of the diffusion of source and drain dopant atoms in to the channel area of

these transistors, as shown in Figure 1.3. The diffusion of source and drain dopant atoms into the channel region becomes a bottleneck to the fabrication of transistors with very short channels, and as a result very low thermal budget processing techniques need to be used [14]. However, even with minimizing the diffusion of source/drain dopants to the channel region using of very costly techniques, the statistical variation of the impurity concentration caused by ion implantation or other doping techniques can cause variation of device parameters which is a problem.

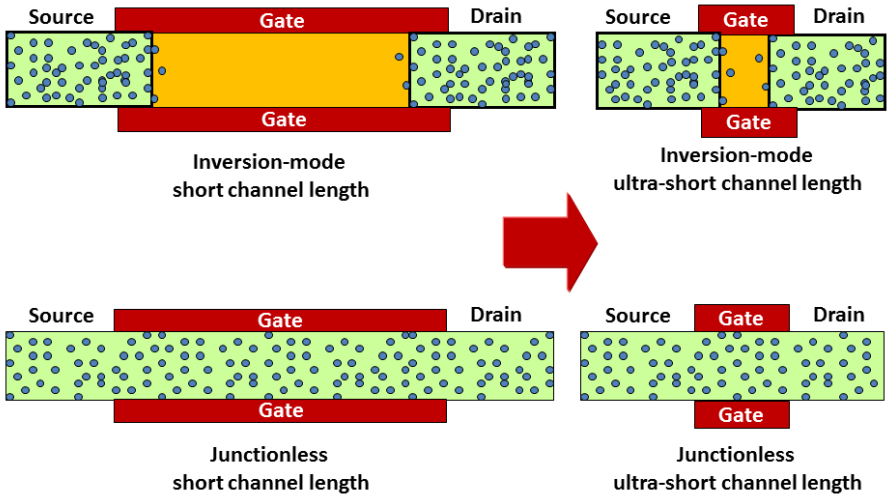


Figure 1.3 - Source and drain doping of inversion-mode and junctionless transistor with short channel and ultra-short channel.

Julius Edgar Lilienfeld introduced the first transistor in 1925 [15]. His field-effect device was very similar to the modern metal-oxide–semiconductor devices. It consisted of a thin semiconductor film deposited on a thin insulator layer, which on itself was deposited a metal electrode. The metal electrode acted as the gate of the device. It worked pretty similar to the modern MOSFET. The current flew in the resistor between two contact electrodes. The Lilienfeld device was a simple resistor that used a gate voltage to deplete the semiconductor film from carriers and modulate its conductivity. His transistor, unlike all other types of transistors, did not have any junction. A transistor is a solid-state active device that controls current flow, and the word “transistor” derives from “trans-resistor”. The Lilienfeld transistor was, technically, a gated resistor; its gate controlled the carrier density and the current flow. It is the simplest and first patented transistor structure, but it was never successfully fabricated.

As explained earlier, MuGFETs have an excellent gate-to-channel coupling and allow full depletion of the channel region even if it is heavily doped. The junctionless devices studied in this thesis do not need the formation of extremely abrupt source and drain junctions. The doping type and concentration in the channel region is equal to that in the source and drain regions, or at least to that in the source and drain extensions. This decreases the complexity and cost of the fabrication processes.

1.4. Semiconductor device modeling

As we discussed earlier rapid shrinking of semiconductor devices has increased the cost and complexity of the fabrication processes. Due to this fact, the optimization of these devices by trial and error methods is not economical. Computers are much cheaper resources and can be used for device modeling. Device modeling allows evaluation of device performance before their manufacturing as well as better understanding of device behavior using the simulation results of phenomena that cannot be readily measured. Using simulation software, carrier transport in semiconductor devices can be modeled at different levels of sophistication. A pure semi-classical treatment is appropriate for devices with large dimensions while for ultra-small devices, quantum treatment needs to be employed. For example, for devices with very small dimensions where the active channel is smaller than 25 nm, the semi-classical approach may lose its validity. The semi-classical models (such as drift-diffusion, energy balance, hydrodynamic, etc.) which are most widely used in TCAD software to model carrier transport are derived from the solution of the Boltzmann Transport Equation (BTE). However, the BTE is not valid for devices with dimensions below the De Broglie wavelength. Some of the well-known methods which have been proposed to model carrier transport in semiconductor devices using the Schrödinger equation are Wigner transformations, Density Matrix approach and non-equilibrium Green's function technique [16-23]. These approaches are technically equivalent. However, their detailed methodology regarding the inclusion of the various quantum effects is different. The non-equilibrium Green's function (NEGF) formalism has been well established in the past decades and has a great numerical stability. It has been used extensively to model quantum transport in single and multiple-gate MOSFETs. Using NEGF, different

types of scattering can be included in the carrier transport of the semiconductor devices. Therefore, we choose this method as base of our 3D numerical simulation tool. Figure 1.4 shows the diagram of some of the widely used semi-classical and quantum models [24-26].

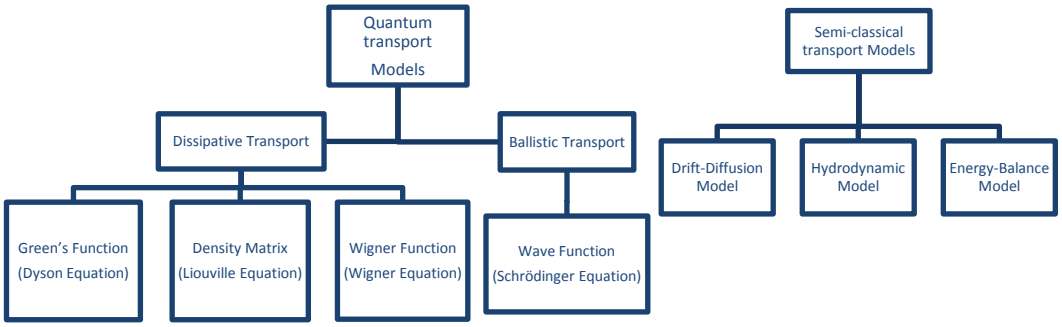


Figure 1.4 – Diagram of some of the widely used semi-classical and quantum transport models.

1.5. Thesis organization

In this thesis we study the performance of different types of nano-scale multiple-gate nanowire devices. To simulate devices with large dimensions, we use commercial TCAD software (Silvaco-TCAD and Synopsys-TCAD). We have also developed a three-dimensional quantum mechanical simulator based on the NEGF formalism and the effective mass approximation using MATLAB and COMSOL Multiphysics softwares to study the performance of different semiconductor (such as Silicon, Germanium and III-V materials) nanowire transistors in either the ballistic regime or in the presence of electron-phonon scattering. Chapter 2 introduces the quantum mechanical models which have been used in this thesis for the simulation of semiconductor devices with advanced device structures. Chapter 3 describes the principles and methods we have used to develop our 3D quantum-mechanical simulator which are based on non-equilibrium Green's functions. Chapter 4 presents the various electron-phonon scattering mechanisms in the framework of the NEGF formalism. In chapters 5-7, we present our simulation results on the investigation of the electrical performance in different Si, Ge, and III-V nanowire transistors. The influence of channel material on the performance of Si, Ge, III-V nanowire MOSFETs is studied and a comparison of the junctionless nanowire transistor versus

inversion-mode and accumulation nanowire transistors is presented. Finally, in chapter 8 conclusions are drawn and directions for the future research are suggested.

References

[1] H. S. P. Wong, "Beyond the conventional transistor," *Solid-State Electronics,* vol. 49, pp. 755-762, May 2005.

[2] S. Cristoloveanu, "Silicon on insulator technologies and devices: from present to future," *Solid-State Electronics,* vol. 45, pp. 1403-1411, 2001.

[3] S. Cristoloveanu, "Future trends in SOI technologies," *Journal of the Korean Physical Society,* vol. 39, pp. S52-S55, Dec 2001.

[4] R. H. Yan, A. Ourmazd, and K. F. Lee, "Scaling the Si MOSFET: from bulk to SOI to bulk," *Electron Devices, IEEE Transactions on,* vol. 39, pp. 1704-1710, 1992.

[5] S. R. N. Yun, W. S. Park, B. H. Lee, and J. T. Park, "Hot electron induced punchthrough voltage of p-channel SOI MOSFET's at room and elevated temperatures," *Microelectronics Reliability,* vol. 43, pp. 1477-1482, Sep-Nov 2003.

[6] C. P. Auth and J. D. Plummer, "Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFET's," *Electron Device Letters, IEEE,* vol. 18, pp. 74-76, 1997.

[7] B. S. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros*, et al.*, "High performance fully-depleted tri-gate CMOS transistors," *Electron Device Letters, IEEE,* vol. 24, pp. 263-265, 2003.

[8] P. Jong-Tae and J.-P. Colinge, "Multiple-gate SOI MOSFETs: device design guidelines," *Electron Devices, IEEE Transactions on,* vol. 49, pp. 2222-2229, 2002.

[9] P. Jong-Tae, J.-P. Colinge, and C. H. Diaz, "Pi-Gate SOI MOSFET," *Electron Device Letters, IEEE,* vol. 22, pp. 405-406, 2001.

[10] J. T. Park, C. A. Colinge, and J.-P. Colinge, "Comparison of gate structures for short-channel SOI MOSFETs," in *SOI Conference, 2001 IEEE International*, 2001, pp. 115-116.

[11] Y. Fu-Liang, C. Hao-Yu, C. Fang-Cheng, H. Cheng-Chuan, C. Chang-Yun, C. Hsien-Kuang*, et al.*, "25 nm CMOS Omega FETs," in *Electron Devices Meeting, 2002. IEDM '02. Digest. International*, 2002, pp. 255-258.

[12] J.-P. Colinge, M. H. Gao, A. Romano-Rodriguez, H. Maes, and C. Claeys, "Silicon-on-insulator `gate-all-around device'," in *Electron Devices Meeting, 1990. IEDM '90. Technical Digest., International*, 1990, pp. 595-598.

[13] http://public.itrs.net/.

[14] S. H. Jain, P. B. Griffin, J. D. Plummer, S. McCoy, J. Gelpey, T. Selinger*, et al.*, "Low resistance, low-leakage ultrashallow p+ junction formation using millisecond flash anneals," *Electron Devices, IEEE Transactions on,* vol. 52, pp. 1610-1615, 2005.

[15] J. E. Lilienfeld, "Method and apparatus for controlling electric current," US patent, 1,745,175 Patent, 1925.

[16] S. Barraud, "Phase-coherent quantum transport in silicon nanowires based on Wigner transport equation: Comparison with the nonequilibrium-Green-function formalism," *Journal of Applied Physics,* vol. 106, 2009.

[17] D. K. Blanks, G. Klimeck, R. Lake, D. Jovanovic, R. C. Bowen, C. Fernando*, et al.*, "NEMO: general release of a new comprehensive quantum device

simulator," in *Compound Semiconductors, 1997 IEEE International Symposium on*, 1998, pp. 639-642.
[18] G. Klimeck, R. Lake, M. J. Maclennan, and S. Datta, "QUEST user's manual," Technical Report TR-EE 93-17, Purdue University1993.
[19] D. K. Ferry and H. L. Grubin, *Modeling of quantum transport in semiconductor devices*. Arizona State University, Tempe, AZ, 1994.
[20] P. Bordone, M. Pascoli, R. Brunetti, A. Bertoni, C. Jacoboni, and A. Abramo, "Quantum transport of electrons in open nanostructures with the Wigner-function formalism," *Physical Review B,* vol. 59, pp. 3060-3069, Jan 15 1999.
[21] M. V. Fischetti, "Master-equation approach to the study of electronic transport in small semiconductor devices," *Physical Review B,* vol. 59, pp. 4901-4917, Feb 15 1999.
[22] R. Lake and S. Datta, "Nonequilibrium Green's-function method applied to double-barrier resonant-tunneling diodes," *Physical Review B,* vol. 45, p. 6670, 1992.
[23] A. Svizhenko, M. P. Anantram, T. R. Govindan, B. Biegel, and R. Venugopal, "Two-dimensional quantum mechanical modeling of nanotransistors," *Journal of Applied Physics,* vol. 91, pp. 2343-2354, 2002.
[24] A. Gehring and S. Selberherr, "Evolution of current transport models for engineering applications," in *Computational Electronics, 2004. IWCE-10 2004. Abstracts. 10th International Workshop on*, 2004, pp. 20-21.
[25] S. Jin, "Modeling of Quantum Transport in Nano-Scale MOSFET Devices," PhD, Seoul National University, Seoul, 2006.
[26] M. Pourfath, "Numerical Study of Quantum Transport in Carbon Nanotube-Based Trabsistors," PhD, Institute for Microelectronics, Vienna University of Technology, Vienna, 2007.

Chapter 2 : Semi-classical and quantum transport in n-channel MOSFETS

2.1. Introduction

Rapid shrinking of semiconductor feature sizes into the nanoscale regime, leads to complicated device behavior due to the occurrence of new physical phenomena at short dimensions and requires deeper understanding of actual operation of ultra-scaled devices [1]. Moreover, the fabrication process becomes more complicated and time-consuming for devices at the nanoscale regime [2]. Due to this fact, optimizing these devices by pure trial-and-error methods is not economical and has to be done by other means. Technology computer-aided design (TCAD) offers both device and process simulation which can be used to model semiconductor device operation and fabrication, respectively. Using device simulation one can simulate the charge carrier transport and its related electrical behavior of semiconductor devices while using process simulation one can simulate physical processes such as material growth, oxidation, ion implantation, dopant diffusion, etching and metal deposition in device fabrication.

The important goal of using device simulation tools is to capture the necessary physics needed to evaluate accurate device operation and at the same time minimize the computational time and cost. Semiconductor device simulation can be done by solving self-consistently the transport equations that govern charge flow and the equations of the fields that drive charge flow. These equations are coupled, hence simultaneous solution is required [2]. From the solution of Maxwell's equations, the fields arising from external sources, as well as charge and current densities can be obtained. In the absence of a changing magnetic field, only the electric fields arising from the solution of the Poisson's equation are required. At larger scales (devices down to 0.5um) the electrical characteristics of semiconductor devices can be estimated solving the drift-diffusion (DD) equations numerically. Scharfetter and Gummel proposed a very robust discretization of the DD equations for numerical simulation of carrier transport in semiconductor devices which is still used [3].

However, shrinking of semiconductor devices to the submicron regime required the refinement and extension of transport models to capture the physical phenomena that occur in small-dimensions. The supply voltages cannot be scaled accordingly due to loss of circuit performance. As a result, the electric field inside these devices has increased, generating hot-carrier and non-local effects. These effects can dominate device performance of small-scale devices. To overcome the limitations of the DD model, many extensions have been proposed. These extensions consider an additional balance equation for the average carrier energy and add a driving term to the current expression. This additional term is proportional to the gradient of the carrier temperature [4]. Many of these models exist and hydrodynamic and energy-balance models are two of the most famous ones. However, these models do not have the capability to accurately simulate ultra-small devices. For these devices, the quantum simulation of carrier transport becomes necessary since the charge-carrier DeBroglie wavelength is comparable to scaled device features. Some of these quantum models are as follows. The quantum hydrodynamic model keeps all classical hydrodynamic features but adds some quantum corrections. The quantum-kinetic equation (Wigner-Boltzmann) is accurate up to a single particle description. The Green's functions include correlations in both space and time domain and can accommodate many-body effects. Finally, one could attempt the direct solution of the Schrödinger equation which can be performed only for small number of particles. Indeed, the simulation of ultra-scaled devices suffers from several computational challenges such as the necessity to solve both the carrier transport and Poisson's equations for the full 3D domain. Very efficient algorithms, multi-processor platforms, and the appropriate level of approximation are essential to capture the necessary transport physics for the description of future technologies.

2.2. Semi-classical transport

2.2.1 Drift-Diffusion simulations

The Boltzmann transport equation has been widely used to describe the transport properties of materials semi-classically [5]. However, combining the direct solution of the Boltzmann equation with field solvers for device simulation is computationally expensive. Therefore, another model based on the solution of the

so-called drift-diffusion equations is dominant for traditional semiconductor simulations. The drift-diffusion equations are local in terms of the driving forces. The DD model is based on the following set of equations [2]:

Current equations:

$$J_n = qn\mu_n E + qD_n \nabla n \quad 2.1$$

$$J_p = qn\mu_p E - qD_p \nabla p \quad 2.2$$

D_n and D_p are the diffusion constants.

Continuity equations (which are the conservation laws for the carriers):

$$\frac{dn}{dt} = \frac{1}{q}\nabla . J_n + U_n \quad 2.3$$

$$\frac{dp}{dt} = -\frac{1}{q}\nabla . J_p + U_p \quad 2.4$$

U_n and U_p are the net generation-recombination rates.

Poisson's equation:

$$\nabla \varepsilon . \nabla V = -q(p - n + N_D - N_A) \quad 2.5$$

where p, n are the electron and hole concentration and N_D, N_A are the donor and acceptor impurity concentrations. For the drift-diffusion equations, it is not possible to obtain a solution in one step and a non-linear iteration method is necessary. The two widely used methods are Gummel's iteration [6] and Newton's method [7].

2.2.2 Hydrodynamic simulations

In deeply-scaled semiconductor MOSFETs velocity overshoot can occur which makes the drift-diffusion model invalid. In the HD model the information about average carrier energies is in the form of carrier temperatures. The electron gas is assumed to be in thermal equilibrium with the lattice temperature in the DD model. However, the presence of a strong electric field drives electrons to gain energy and

increase the temperature of the electron gas (T_n) [2]. The pressure of the electron gas is proportional to nK_bT_n and the driving force becomes a pressure gradient instead of only the density gradient. As a result, a temperature gradient is added as an additional driving force. We can rewrite the current equation as follows:

$$J_n = qn\mu_n E + qD_n \nabla n + qnD_T \nabla T_n \qquad 2.6$$

where D_T is the thermal diffusivity and T_n represents the electronic temperature.

2.2.3 Energy-Balance simulations

The energy balance model is another approach with higher order solutions to the general Boltzmann transport equation. It is suitable for simulations of deeply-scaled semiconductor MOSFETs and provides a more accurate description of device physics, especially effects such as velocity overshoot and non-local impact ionization which cannot be captured by the classical DD model. Energy balance models consider coupling of the current density to the carrier temperature, or energy. The current density equations from the DD model are modified to include this additional physical relationship [8].

2.3. Quantum transport

2.3.1 Introduction

Ultra-scaled semiconductor devices have approached the quantum transport regime. To model the quantum transport phenomena one can use the non-equilibrium Green's function (NEGF) formalism. NEGF is a very powerful and useful technique which was introduced at the beginning of the 1960's [9-12]. Using NEGF one can study the time evolution of a many-particle quantum system. NEGF formalism and its mathematical derivation has been discussed extensively and can be easily found in the literature [13-15]; therefore here we do not present the many-body discussion of the NEGF formalism.

The NEGF formalism has become a very popular approach in the development of quantum-mechanical simulators for CMOS nanoscale devices [16-23]. Even within the effective-mass approximation, it allows for the treatment of sophisticated

bandstructure models derived from the atomic level [14, 24-27]. The NEGF formalism has been widely used to simulate quantum ballistic transport (i.e., disregarding energy relaxation processes of charge carriers) in semiconductor devices [28-33] but different types of scattering processes can be treated with various degrees of approximation through the NEGF formalism [23, 25, 30, 34-36].

Also, different numerical methods can be used to simulate 3D quantum transport in the conduction band of semiconductor MOSFETs within the effective mass approximation. Real-space and mode-space approaches are two different methods which can be used [37, 38]. Both real-space and mode-space approaches are able to model electron transport in arbitrary device structures with different shapes. These approaches discretize the Hamiltonian in spatial coordinates. The real-space approach is very general and accurate but it requires huge computational time and resources which is a drawback of this method [28, 38]. On the other hand, the mode-space approach is capable of handling most of the problems of interest as the real-space approach but with reasonable computational efficiency [37, 39, 40].

The mode-space approach is a well-established technique. A transformation from real-space to mode-space as well as the reverse transformation, applied to the solution of the NEGF quantum transport problem, can be found in the literature [39, 41]. In the mode-space approach, it is well known that as long as the wavefunction does not vary along the transport direction, the coupling between modes can be neglected and it does not affect the simulation results [37, 42]. This is very useful to efficiently model semiconductor nanowire transistors which have uniform profile in the transport direction [37, 39]. But strong mode coupling is expected for non-uniform devices or whenever the shape of the transverse modes varies along the channel direction. For example, the presence of any geometrical constrictions, surface roughness or considering discrete impurity atoms, all require to include coupling effects between modes [39, 42-46]. In this section we discuss different mode-space approaches which we have implemented in our 3D quantum-mechanical simulator.

2.3.2 Real-Space vs. Mode-Space Approach

In the real-space approach the 3D Schrödinger equation with open boundary conditions, is solved by direct discretization of the kinetic energy operator in the spatial coordinates involving $\partial^2/\partial x^2$, $\partial^2/\partial y^2$, $\partial^2/\partial z^2$ where x, y, z are spatial directions in the Cartesian system. This can be done using any available numerical methods, namely finite difference method (FDM) or finite element method (FEM).

In Eq. 2.7 H_{3D} is the 3D device Hamiltonian, E is energy and $\Psi(x,y,z)$ is the 3D wavefunction. In the RS approach after direct discretization of the 3D Hamiltonian in the geometrical domain of the device structure, the NEGF formalism is applied to obtain physical quantities. Real-space approach can be used to capture any physical phenomena in arbitrarily-oriented device structure with different shapes. However, to use this method, one needs to explicitly treat the whole spatial domain of the device and as a result to store and manipulate very large matrices. This drawback makes RS approach hard to use for extensive device simulation.

$$H_{3D}\Psi(x,y,z) = E\Psi(x,y,z) \qquad 2.7$$

The mode-space approach is based on subband decomposition and can be used instead of real-space approach to solve the 3D Schrödinger equation for semiconductor nanowire transistors in which strong quantum confinement exists [37, 42, 47]. Using the MS approach the quantum confinement and transport can be separated to solve the Schrödinger equation in a computationally efficient manner. As a result of this procedure [14], the 3D Schrödinger equation is decomposed into: (I) a 2D Schrödinger equation which is solved with closed boundary condition in different cross-sections of the nanowire to obtain the wave functions and the electron subbands along the device, and (II) a 1D transport equation which is solved using NEGF formalism along the source-drain axis to obtain the electron charge density. The flowchart of the mode-space approach is shown in Figure 2.1.

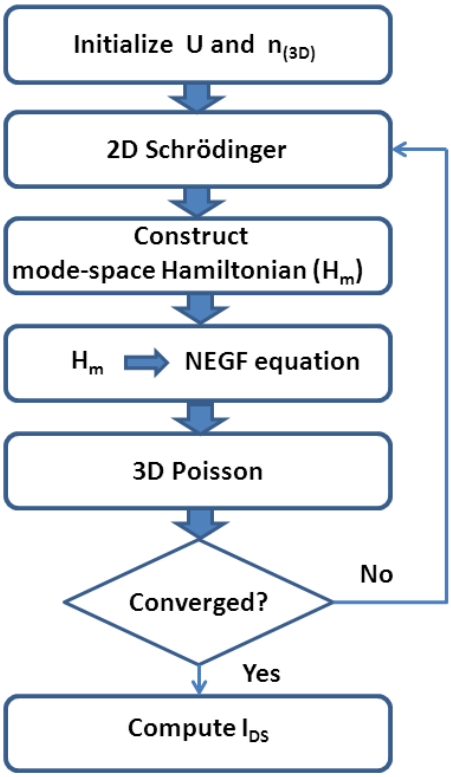


Figure 2.1 - The flow chart of mode-space approach implemented in our simulator.

Different strategies with the same principal idea to implement the mode-space technique have been proposed and can be found in the literature [18, 33, 37, 39, 41, 42, 47, 48]. Depending on the device structure and the physics of the problem, one can use any of the 4 different methods. We have implemented these methods into our 3D simulator. These are coupled mode-space, uncoupled mode-space, fast uncoupled mode-space, and fast coupled mode-space approaches which are explained below.

2.3.2.1 Coupled mode-space (CMS) approach

The 3D full stationary Schrödinger equation is given by Eq. 2.7. Assuming a diagonal effective-mass tensor and ellipsoidal parabolic energy band (for the case that the effective-mass tensor in not diagonal, please refer to chapter 6), the 3D Hamiltonian can be written as follows [37]:

$$H_{3D} = -\frac{\hbar^2}{2}\left(\frac{1}{m_x(y,z)}\frac{\partial^2}{\partial x^2} + \frac{\partial}{\partial y}\left[\frac{1}{m_y(y,z)}\frac{\partial}{\partial y}\right] + \frac{\partial}{\partial z}\left[\frac{1}{m_z(y,z)}\frac{\partial}{\partial z}\right]\right) + U(x,y,z) \qquad 2.8$$

where m_x, m_y, *and* m_z are electron effective-masses in the device coordinate system, and $U(x, y, z)$ is the potential energy. One needs to note that the effective mass varies in the transversal directions (in our case *y*-*z* plane). This is due to the transition between the Si body and the SiO_2 oxide layer. The penetration of the electron wave function into the oxide layer is also considered as it is necessary for the validation of the effective-mass approximation for Si nanowire transistors [49]. One should note that for the devices with cross-section diameter smaller than 5 nm, the *E*-*k* dispersion relationship is no longer parabolic and using the bulk values of the effective mass may result in inaccurate results. So to obtain accurate results, the deviation of the effective mass from the bulk values has to be taken into account. Now the 3D electron wavefunction can be written as follows [37, 42]:

$$\psi(x,y,z) = \sum_n \varphi^n(x)\xi^n(y,z;x) \tag{2.9}$$

where $\xi^n(y,z;x=x_0)$ is the n^{th} eigenfunction of the following 2D Schrödinger equation (Eq. 2.10) at the slice $x=x_0$ of the semiconductor nanowire device:

$$\left[-\frac{\hbar^2}{2}\left(\frac{\partial}{\partial y}\left[\frac{1}{m_y(y,z)}\frac{\partial}{\partial y}\right]+\frac{\partial}{\partial z}\left[\frac{1}{m_z(y,z)}\frac{\partial}{\partial z}\right]\right)+(U(y,z;x_0) - E^n_{sub}(x_0)\right]\xi^n(y,z;x_0)=0 \tag{2.10}$$

In Eq. 2.10 $E^n_{sub}(x_0)$ is the n^{th} subband energy level at $x=x_0$ and $\xi^n(y,z;x)$ satisfies the following equation for any of the *x* values:

$$\oint_{y,z} \xi^m(y,z;x)\xi^n(y,z;x)dydz = \delta_{m,n} \tag{2.11}$$

where $\delta_{m,n}$ is the Kronecker delta function. All the eigenfunctions are normalized as follows at each position in the *x*-direction:

$$\xi^n(y,z;x) = \frac{\xi^n(y,z;x)}{\sqrt{\oint_{y,z} \xi^n(y,z;x)dydz}} \qquad 2.12$$

Inserting (Eq. 2.8) and (Eq. 2.9) into Eq. (2.7) and using the (Eq. 2.10), one can obtain:

$$-\frac{\hbar^2}{2m_x^*(y,z)}\frac{\partial^2}{\partial x^2}\left(\sum_n \varphi^n(x)\xi^n(y,z;x)\right) + \sum_n \varphi^n(x)E_{sub}^n(x)\xi^n(y,z;x) = E\sum_n \varphi^n(x)\xi^n(y,z;x) \qquad 2.13$$

After multiplying by $\xi^m(y,z;x)$ on both sides of the equation and performing an integral in the *y*-*z* plane, we obtain the basic coupled equation of the CMS approach as follows:

$$-\frac{\hbar^2}{2}\left(\sum_{n=1}^{\infty} a_{mn}(x)\right)\frac{\partial^2\varphi^m(x)}{\partial x^2} - \frac{\hbar^2}{2}\sum_n c_{mn}(x)\varphi^n(x) - \hbar^2\sum_n b_{mn}(x)\frac{\partial\varphi^n(x)}{\partial x} + E_{sub}^m(x)\varphi^m(x) = E\varphi^m(x) \qquad 2.14$$

where the coefficients are as follows:

$$\begin{aligned} a_{m,n} &= \oint_{y,z} \frac{1}{m_x^*(y,z;x)}\xi^m(y,z;x)\xi^n(y,z;x)\,dydz \\ b_{m,n} &= \oint_{y,z} \frac{1}{m_x^*(y,z;x)}\xi^m(y,z;x)\frac{\partial}{\partial x}\xi^n(y,z;x)\,dydz \\ c_{m,n} &= \oint_{y,z} \frac{1}{m_x^*(y,z;x)}\xi^m(y,z;x)\frac{\partial^2}{\partial x^2}\xi^n(y,z;x)\,dydz \end{aligned} \qquad 2.15$$

One can neglect a_{mn} if $m \neq n$ as in our simulation the electron wave function is mainly located in the semiconductor region and $a_{mm} >> a_{mn}$. As a result, Eq. 2.14 can be rewritten as follows [37]:

$$-\frac{\hbar^2}{2}\frac{\partial^2}{\partial x^2}\varphi^m(x) - \frac{\hbar^2}{2}\sum_n c_{mn}(x)\varphi^n(x) - \hbar^2\sum_n b_{mn}(x)\frac{\partial\varphi^n(x)}{\partial x} + E_{sub}^m(x)\varphi^m(x) = E\varphi^m(x) \qquad 2.16$$

One can easily find that considering all the modes in Eqs. 2.14 and 2.15, make the CMS formalism mathematically equivalent to the real-space approach. The advantage of this method to the real-space approach is that one can choose how many modes need to be considered. In ultra-scaled nanowire devices, due to the very strong quantum confinement, only few of the lowest subbands participate in transport and need to be considered in the simulations. This is a huge advantage of the mode-space approach and can reduce the computational cost and time significantly.

Now by considering the first M subbands (*i.e., m,n*=1,…,*M*), we can express Eq. 2.16 in a matrix format as follows:

$$H\begin{bmatrix}\varphi^1(x)\\ \varphi^2(x)\\ \cdots\\ \cdots\\ \varphi^M(x)\end{bmatrix}=E\begin{bmatrix}\varphi^1(x)\\ \varphi^2(x)\\ \cdots\\ \cdots\\ \varphi^M(x)\end{bmatrix} \qquad 2.17$$

$$H=\begin{bmatrix}h_{11} & h_{12} & h_{13} & \cdots & h_{1M}\\ h_{21} & h_{22} & h_{23} & \cdots & h_{2M}\\ \cdots & \cdots & \cdots & \cdots & \cdots\\ \cdots & \cdots & \cdots & \cdots & \cdots\\ h_{M1} & h_{M2} & h_{M3} & \cdots & h_{MM}\end{bmatrix} \qquad 2.18$$

Where,

$$h_{mn}=\delta_{mn}\left[-\frac{\hbar^2}{2}a_{mn}(x)\frac{\partial^2}{\partial x^2}+E^m_{sub}(x)\right]-\frac{\hbar^2}{2}c_{mn}(x)-\frac{\hbar^2}{2}b_{mn}(x)\frac{\partial}{\partial x}\left(m,n=1,2,\cdots,M\right) \qquad 2.19$$

It is clear that by using the mode-space approach, the size of the device Hamiltonian has been reduced significantly from ($N_{yz}N_x$)×($N_{yz}N_x$) in real-space approach, where N_{yz} is around 1,000 for the device structures we consider in this work and N_x is the number of points in the transport (*x)* direction, to (MN_x)×(MN_x), where the number of

required modes (M) is usually around 5 for device structures we simulate in this work.

After building the mode-space Hamiltonian, the quantum transport equations need to be solved to calculate the I-V characteristics, the electron carrier density, or other required physical quantities. We use the NEGF formalism for this purpose. The stationary quantum transport equations are defined as [25, 50, 51]:

$$G^r(E) = [EI - H - \sum_S - \sum_1 - \sum_2]^{-1} \quad 2.20$$

$$G^<(E) = G^r(\sum_S^< - \sum_1^< - \sum_2^<)G^a \quad 2.21$$

G^r and G^a are the retarded and advanced Green's function, respectively, $G^<$ is the lesser Green's function, H is the 1D Hamiltonian in the mode-space presentation, and Σ_S accounts for the self-energy due to the (incoherent) scattering interactions in the device and $\Sigma_{1,2}$ are self-energies due to coupling between the source/drain reservoirs and the device region.

For the 1D NEGF equation that we have, the self-energies $\Sigma_{1,2}$ are defined as follows [51]:

$$\Sigma_1[p,q](E) = -t_{m,1}\exp(jk_{m,1}a) \quad \delta_{p,(m-1)Nx+1}\,\delta_{q,(m-1)Nx+1} \quad 2.22$$

$$\Sigma_2[p,q](E) = -t_{m,Nx}\exp(jk_{m,Nx}a) \quad \delta_{p,mNx}\,\delta_{q,mNx} \quad 2.23$$

where,

$$t_{m,1} = \left(\frac{\hbar^2}{2a^2}\right) a_{mm}(x)\Big|_{x=0} \quad 2.24$$

$$t_{m,Nx} = \left(\frac{\hbar^2}{2a^2}\right) a_{mm}(x)\Big|_{x=(Nx-1)a} \quad 2.25$$

and where,

$$E = E_{sub}^m(0) + 2t_{m,1}\left[1 - \cos\left(k_{m,1}a\right)\right] \quad 2.26$$

$$E = E_{sub}^{m}\left[(N_x - 1)a\right] + 2t_{m,Nx}\left[1 - \cos\left(k_{m,Nx}a\right)\right] \quad 2.27$$

As one can see from Eqs. 2.22 and 2.23, the self-energies Σ_1 and Σ_2 only modify the first and last diagonal elements of h_{mm} (m=1, 2,…, M), respectively. The lesser self-energies for the source/drain contacts are defined as follows:

$$\Sigma_1^{<}(E) = -2\Im\left[\Sigma_1(E)\right] f\left(E - \mu_S\right) = \Gamma_1 f\left(E - \mu_S\right) \quad 2.28$$

$$\Sigma_2^{<}(E) = -2\Im\left[\Sigma_2(E)\right] f\left(E - \mu_D\right) = \Gamma_2 f\left(E - \mu_D\right) \quad 2.29$$

where f is the Fermi-function distribution and μ_S and μ_D are the source and drain Fermi levels. Now we can obtain the electron carrier density and current as follows. The 1D electron density for each mode can be obtained using Eq. 2.30,

$$n_{1D}^{m}(x) = \frac{-i}{2\pi a}\int G_{mm}^{<}(x,x,E)dE \quad 2.30$$

The total 3D electron density at each spatial coordinate is calculated using Eq. 2.31,

$$n_{3D}(x,y,z) = \frac{-i}{2\pi a}\sum_{m}\int G_{mm}^{<}(x,x,E)\left|\xi^{m}(y,z;x)\right|^2 dE \quad 2.31$$

In Eqs. 2.30 and 2.31, "*a*" is the discretized mesh spacing in the transport (*x)* direction. We use the obtained 3D electron density as an input for our 3D Poisson solver till convergence is achieved by our self-consistent calculations. The total current can be calculated by integrating the following equation which shows the current density at each longitudinal node and for different energies:

$$J(x_i,E) = -\frac{q}{\hbar}\sum_{n,m}\left(h_{nm}(x_i,x_{i+1})G_{mn}^{<}(x_{i+1},x_i,E) - h_{mn}(x_{i+1},x_i)G_{nm}^{<}(x_i,x_{i+1},E)\right) \quad (n,m = 1,2,\cdots,M) \quad 2.32$$

For ballistic transport, using the Landauer-Büttiker formula, the total electron current can also be calculated as follows [51]:

$$I_{SD} = \frac{q}{\hbar}\int T(E)\left[f\left(E-\mu_S\right)-f\left(E-\mu_D\right)\right]dE \qquad 2.33$$

where the *T(E)* is the transmission coefficient at the energy *E* and defined as [52]:

$$T(E) = Tr[\Gamma_1(E)G^r(E)\Gamma_2(E)G^a(E)] \qquad 2.34$$

where *Tr* is the trace operator and $\Gamma_{1,2}$=j[$\sum_{1,2}$-$\sum^{\dagger}_{1,2}$].

2.3.2.2 Uncoupled mode-space (UMS) approach

The CMS approach which was discussed in the previous section considers coupling between modes. However in some circumstances we do not need to consider coupling between the modes. For devices which do not have a uniform body, coupling between modes cannot be neglected but for nanowire devices with small cross-section and uniform body, the confinement potential profile (in the transversal plane) has very slow changes along the channel direction and despite of the different eigenvalues, eigenfunctions are approximately the same along the channel. As a result one can assume [37]:

$$\xi^m(y,z;x) = \overline{\xi^m}(y,z) \qquad 2.35$$

And

$$\frac{\partial}{\partial x}\xi^m(y,z;x) = 0 \quad ,(m=1,2,...,M) \qquad 2.36$$

Substituting Eqs. 2.35 and 2.36 in Eq. 2.15 gives us the new coupling constants as follows:

$$a_{mm}(x) = \overline{a_{mm}} = \oint_{y,z} \frac{1}{m_x^*(y,z;x)} \left|\xi^m(y,z;x)\right|^2 dy\,dz \qquad 2.37$$

$$b_{mn}(x) = 0 \quad and \quad c_{mn}(x) = 0 \quad (m,n = 1,2,\cdots,M) \qquad 2.38$$

This infers h_{mn}=0 ($m \neq n$ and m,n=1,2,…,M) and we get the block-diagonal Hamiltonian matrix (Eq. 2.33) which means that all modes are uncoupled.

$$H = \begin{bmatrix} h_{11} & 0 & \cdots & \cdots & 0 \\ 0 & h_{22} & 0 & \ddots & \vdots \\ \vdots & 0 & \ddots & \ddots & \vdots \\ \vdots & \ddots & \ddots & \ddots & 0 \\ 0 & \cdots & \cdots & 0 & h_{MM} \end{bmatrix} \qquad 2.39$$

This gives us a block diagonal retarded Green's function (according to the Eq. 2.20). Finally we use an efficient recursive Green's function algorithm and compute all the Green's functions. However, the solution of N_x (which is the number of nodes in the x-direction) 2D Schrödinger equations is still needed to obtain the subband profile and this can be time-consuming. In the next section, we discuss the fast uncoupled mode-space approach. Using this method, we only need to solve just one 2D Schrödinger equation to obtain the subband profile.

2.3.2.3 Fast uncoupled mode-space (FUMS) approach

As we described in previous sections, both the CMS and UMS approaches need solution of N_x 2D Schrödinger equations in a self-consistent loop to obtain the electron subbands and eigenfunctions. This process is computationally intensive and requires multi-processor computation. The fast uncoupled mode space approach [37, 47] is a very fast and efficient method with very good accuracy and is useful for extensive device simulation. The FUMS approach only needs one 2D Schrödinger equation to be solved in a self-consistent loop and provides very good agreement with results obtained by the CMS and UMS approaches.

We use the assumption we made in the previous section, that is, the eigenfunctions $\xi^m(y,z;x)$ vary very slowly along the x direction, $\xi^m(y,z)=\overline{\xi^m}(y,z)$, and the new assumption that the average wavefunctions $\overline{\xi^m}(y,z)$ are the eigenfunctions of the following 2D Schrödinger equation at position $x=x_0$,

$$\left[-\frac{\hbar^2}{2}\frac{\partial}{\partial y}\left(\frac{1}{m_y^*(y,z)}\frac{\partial}{\partial y}\right)-\frac{\hbar^2}{2}\frac{\partial}{\partial z}\left(\frac{1}{m_z^*(y,z)}\frac{\partial}{\partial z}\right)+\overline{U}(y,z)\right]\overline{\xi^m}(y,z)=\overline{E_{sub}^m}\,\overline{\xi^m}(y,z) \quad 2.40$$

where the average conduction band-edge potential $U(y,z)$ is calculated as follows:

$$\overline{U}(y,z)=\frac{1}{L_x}\int_0^{Lx}U(y,z,x)dx \quad 2.41$$

where L_x is the total length of the simulated nanowire transistor (including the source/drain extensions). After computing the associated eigenvalues $\overline{E_{sub}^m}$ and eigenfunctions $\overline{\xi^m}$, using first-order stationery perturbation theory we can obtain the subband profile [37, 47]:

$$E_{sub}^m(x)=\overline{E_{sub}^m}+\oint_{y,z}U(y,z;x)\left|\overline{\xi^m}(y,z;x)\right|^2dydz-\oint_{y,z}\overline{U}(y,z;x)\left|\overline{\xi^m}(y,z;x)\right|^2dydz \quad 2.42$$

Figure 2.2 compares the computed I_{DS}-V_{GS} characteristics for the gate-all-around silicon nanowire transistors using FUMS (solid lines) and CMS (circles) approaches, respectively. One can see that FUMS is in excellent agreement with the more accurate CMS. It is clear that the FUMS approach is a very suitable approach for extensive device simulation of nanowire transistors with invariant device shape, as it is much faster than CMS approach.

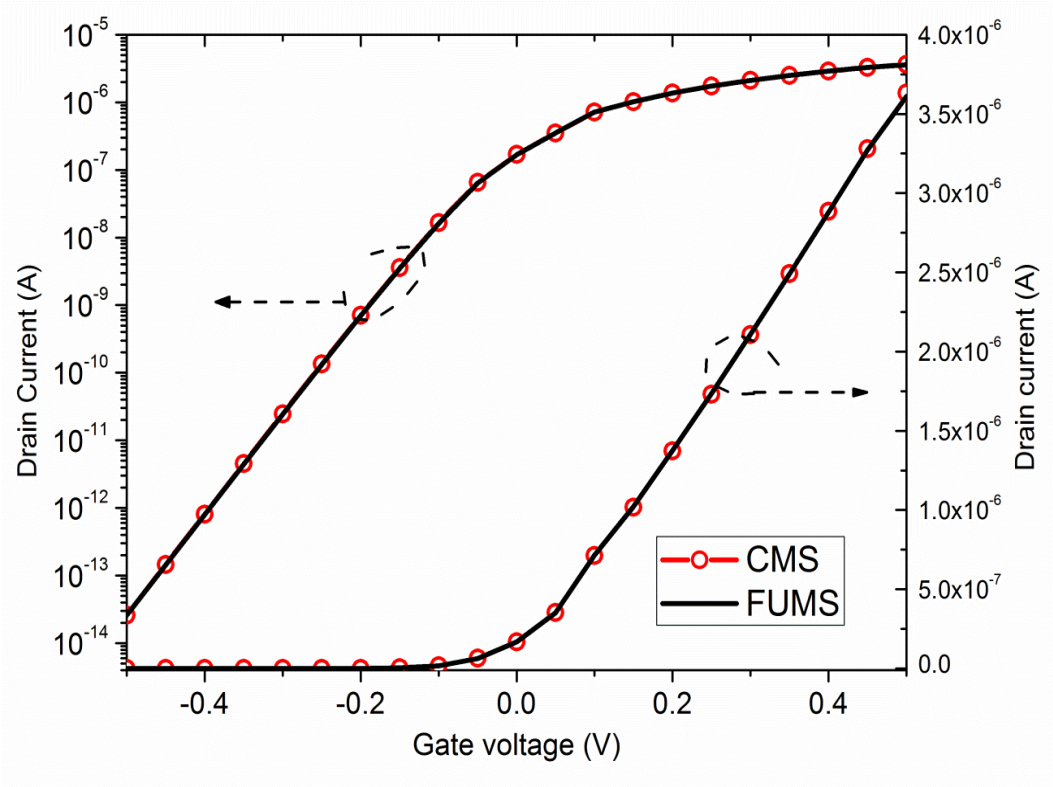


Figure 2.2 - The I_{DS}-V_{GS} curves for silicon nanowire transistors in logarithm (left) and linear (right) scales (the circle symbols (red) and solid lines (black) represent results obtained by CMS approach, and the FUMS approach, respectively).

2.3.2.4 Fast coupled mode-space (FCMS) approach

As we discussed earlier in this chapter, the CMS approach is useful to simulate device structures with different body shape and discontinuities across the body of the device and explained how it is much faster than real-space simulations but still is time-consuming and needs parallel-processing to be used as it imposes the computation of a full 2D Schrödinger problem for each *x*-mesh point. We also described for nanowires with small cross-section and a constant body shape, the FUMS approach can be used to extensively speed up the simulation time. But the problem is that FUMS cannot be used for devices with variable cross-sections or considering discreet dopant atoms, since the wavefunction varies rapidly around a discontinuity in a semiconductor nanowire device.

In this section we discuss a new approach that allows us simulating device structures with discontinuities across the semiconductor nanowire device (Figure 2.3) and is much faster than the CMS approach but its simulation results are still in very good agreement with CMS approach results [53]. This approach, which we

have called it fast coupled mode space (FCMS), combines the advantages of both CMS and FUMS methods and is explained below.

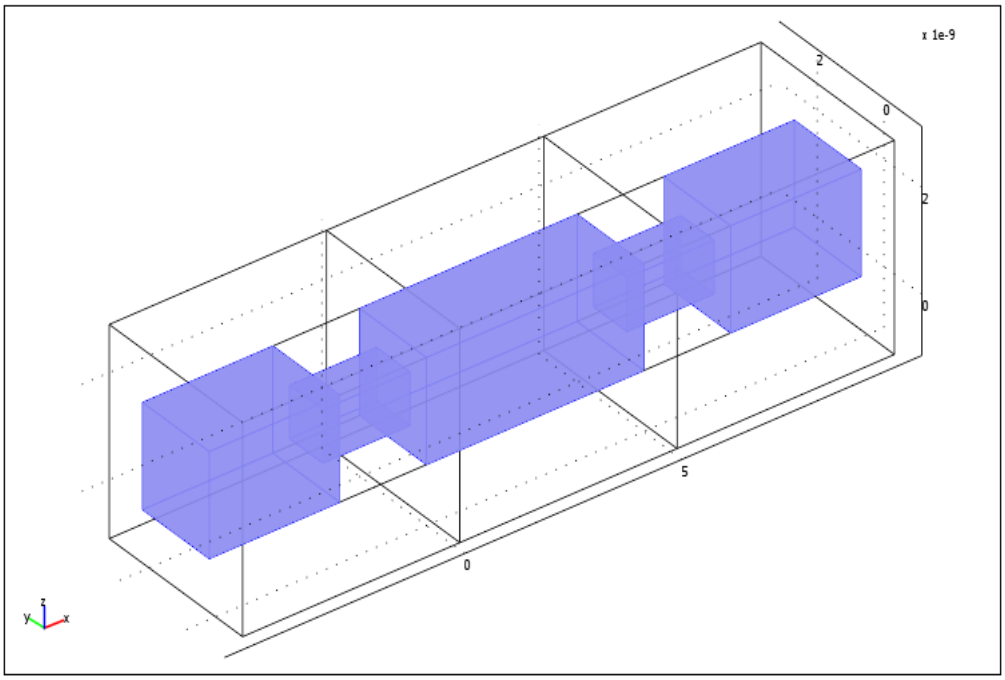


Figure 2.3 – Device with variant body shape.

The basic assumption of the FCMS method is that the variation of the wavefunction is localized around the discontinuities but is constant far from them. With this assumption, we can neglect the mode coupling at points far from the discontinuities. We then solve one 2D Schrödinger equation with an *x*-averaged potential in the cross-section and derive the energy subbands in each part identified as constant as in the FUMS algorithm but take the coupling into account in the Hamiltonian around the discontinuities, considering enough distance from the edges of discontinuties, and solve a 2D Schrödinger equation with the real potential in these cross-sections at each *x*-mesh points as in the CMS algorithm.

Figure 2.4 illustrates the evolution of the first lateral wavefunction in the middle of the silicon nanowire transistor with varying body structure (as in Figure 2.3) using the FCMS and CMS approaches. It can be seen that results obtained using the FCMS approach are in an excellent agreement with the results obtained from the CMS approach.

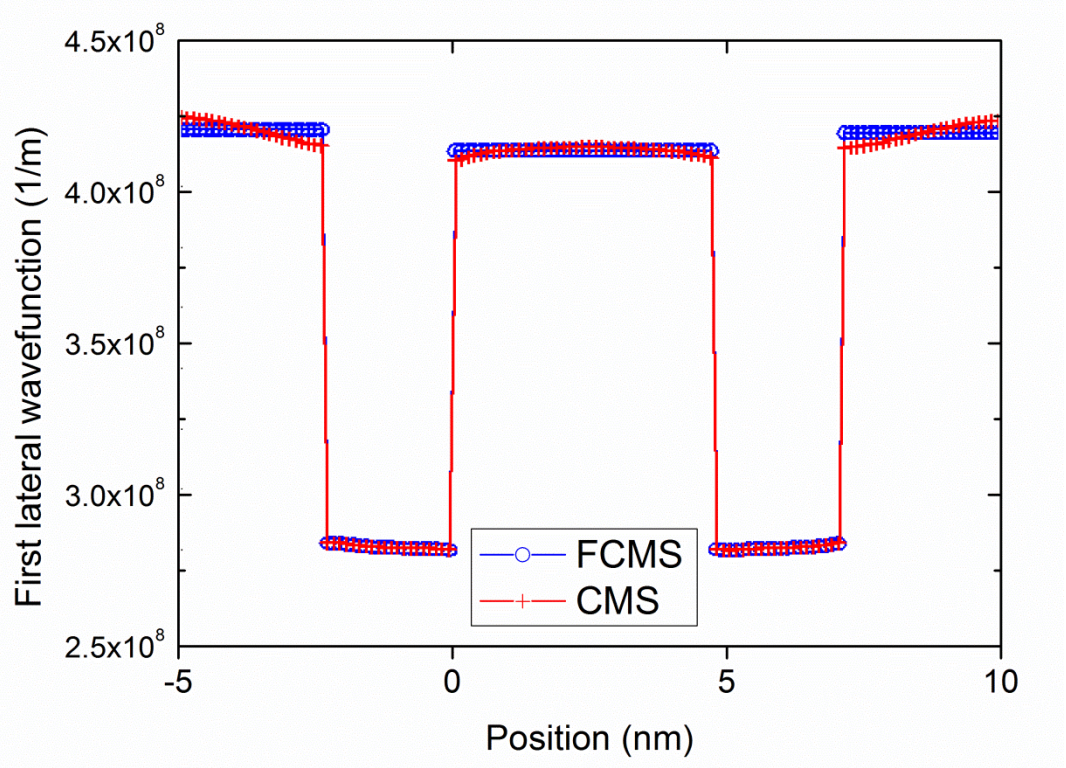


Figure 2.4 - Evolution of first lateral wavefunction in the middle of the silicon nanowire transistor with variant body structure obtained by FCMS (blue) and CMS (red) approaches.

The FCMS algorithm allows for the simulation of structures with variable cross-section, tunnel barriers or other types of discontinuities in a semiconductor nanowire device, as it would be the case for a real space algorithm. We can also use a more computational efficient iterative adaptive energy mesh. This iterative energy mesh method cannot be parallelized and therefore cannot be used in the RS simulations. Table 2.1 summarizes the different NEGF methods, their relative speed and performances for 3D simulations.

Table 2.1- Comparison of different 3D NEGF methods.

Method	Time on 1 processor (typical, relative unit)	Cross-section shape	Run on standard PC
FUMS	1	Constant only	yes
CMS	5-10	Any	Possible but long
FCMS	1.2	Any	yes
RS	1000	Any	No, parallel processing needed (typicaly>100 processors)

2.3.3 Self-consistent Simulations

Assuming parabolic energy bands and the effective-mass approximation, the 3D time-independent Schrödinger equation can be written as follows [25, 28, 33]:

$$\left(-\frac{\hbar^2}{2}\nabla.\frac{1}{m^*_{(x,y,z)}}\nabla + U(x,y,z)\right)\psi(x,y,z) = E\,\psi(x,y,z) \qquad 2.43$$

Where U is the conduction band potential energy profile and m^* is the position dependent effective-mass tensor. The electrostatic potential φ is also computed through the solution of the Poisson equation as follows:

$$\nabla^2\varphi(x,y,z) = -\frac{q}{\varepsilon_{si}}\left(p(x,y,z) - n(x,y,z) + N_D - N_A\right) \qquad 2.44$$

where p, n are the electron and hole concentration and N_D, N_A are the donor and acceptor impurity concentrations. Then through calculation of the conduction band profile ($U \leftrightarrow -q\varphi$, where q is the elementary charge), the electrostatic potential φ enters in the Schrödinger equation. On the other hand, as discussed before, the electron density depends on the square of the electron wavefunction ψ which is the solution of the Schrödinger equation. Therefore, we have implemented an iterative

self-consistent routine that needs to be applied to determine the charge density and electrostatic potential quantitatively [54].

Our self-consistent routine is composed of two main parts, the Poisson's equation solver and the quantum transport solver. We use the COMSOL Multiphysics™ software to solve the Poisson equation and calculate the electrostatic potential in the device for given electron and hole densities. The quantum transport solver gives the electron and hole densities and the electrical current for a given potential using the NEGF formalism.

The self-consistent loop starts by an initial guess for the electrical potential and feeds to the NEGF solver to calculate the electron and hole densities. Then the calculated densities are fed to Poisson's solver to find the new electrostatic potential in the device and check for convergence. If convergence is achieved, the electrical current will be calculated otherwise we go back and forth between the Poisson's and NEGF solvers until convergence is achieved. Figure 2.5 shows our iterative self-consistent procedure.

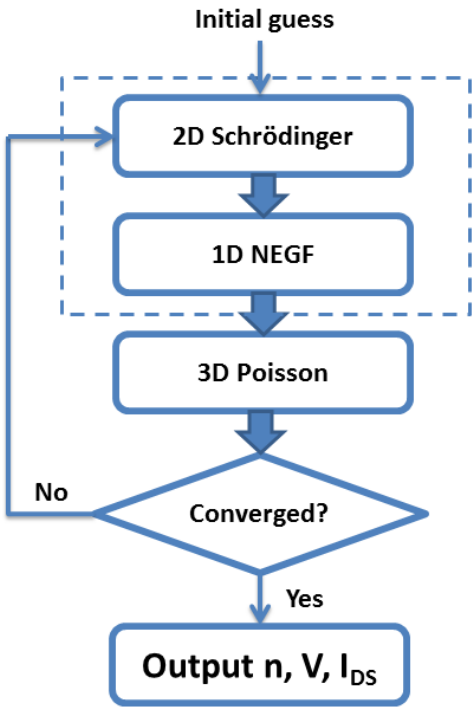


Figure 2.5- The schematic representation of self-consistent solution between charge density and electrostatic potential.

2.4. Conclusion

In this chapter, we discussed four different methods for implementation of a three-dimensional Schrödinger–Poisson solver with open boundary conditions in the framework of the effective mass approximation using the non-equilibrium Green's function formalism. These are useful for the purpose of quantum transport modeling in semiconductor nanowire transistors. We discussed the real-space and mode-space approaches which can be used to solve the 3D Schrödinger equation. We also introduced a fast coupled mode-space (FCMS) approach which has the advantages of both the CMS and FUMS approaches (the accuracy of CMS method and the speed of FUMS). We showed that FCMS is capable of producing the very same wavefunction as in the case of the CMS approach for devices with local discontinuities.

References

[1] S. M. G. David K. Ferry, Jonathan Bird, *Transport in Nanostructures*, 2nd ed., Cambridge University Press, August 2009.

[2] D. Vasileska, D. Mamaluy, H. R. Khan, K. Raleva, and S. M. Goodnick, "Semiconductor Device Modeling," *Journal of Computational and Theoretical Nanoscience,* vol. 5, pp. 999-1030, 2008.

[3] D. L. Scharfetter and H. K. Gummel, "Large-signal analysis of a silicon Read diode oscillator," *Electron Devices, IEEE Transactions on,* vol. 16, pp. 64-77, 1969.

[4] K. Blotekjaer, "Transport equations for electrons in two-valley semiconductors," *Electron Devices, IEEE Transactions on,* vol. 17, pp. 38-47, 1970.

[5] J. M. Ziman, *Electrons and Phonons: The Theory of Transport Phenomena in Solids*: Clarendon Press, 2001.

[6] H. K. Gummel, "A self-consistent iterative scheme for one-dimensional steady state transistor calculations," *Electron Devices, IEEE Transactions on,* vol. 11, pp. 455-465, 1964.

[7] *Multi-Variable Calculus and Linear Algebra*: John Wiley & Sons Canada, Limited, 1973.

[8] http://www.silvaco.com.

[9] S. Fujita, "Partial self-energy parts of Kadanoff-Baym," *Physica,* vol. 30, pp. 848-856, 1964.

[10] J. Schwinger, "Brownian motion of a quantum oscillator," *Journal of Mathematical Physics,* vol. 2, pp. 407-432, 1961 1961.

[11] L. P. Kadanoff and G. Baym., *Quantum Statistical Mechanics*. New York: W. A. Benjamin, Inc, 1962.

[12] L. V. Keldysh, "Diagram technique for nonequilibrium processes," *Soviet Physics Jetp-Ussr,* vol. 20, pp. 1018, 1965.

[13] M. Pourfath, "Numerical Study of Quantum Transport in Carbon Nanotube-Based Trabsistors," PhD, Institute for Microelectronics, Vienna University of Technology, Vienna, 2007.

[14] M. Luiser, "Quantum Transport Beyond the Effective Mass Approximation," PhD, Swiss Federal Institute of Ttechnology, Zurich, 2007.
[15] S. Jin, "Modeling of Quantum Transport in Nano-Scale MOSFET Devices," PhD, Seoul National University, Seoul, 2006.
[16] S. Steiger, R. G. Veprek, and B. Witzigmann, "Electroluminescence from a Quantum-Well LED using NEGF," in *Computational Electronics, 2009. IWCE '09. 13th International Workshop on*, 2009, pp. 1-4.
[17] G. Fiori and G. Iannaccone, "Simulation of graphene nanoribbon field-effect transistors," *Ieee Electron Device Letters,* vol. 28, pp. 760-762, Aug 2007.
[18] M. Shin, "Efficient simulation of silicon nanowire field effect transistors and their scaling behavior," *Journal of Applied Physics,* vol. 101, Jan 15 2007.
[19] M. Shin, "Three-dimensional quantum simulation of multigate nanowire field effect transistors," *Mathematics and Computers in Simulation,* vol. 79, pp. 1060-1070, Dec 15 2008.
[20] N. Neophytou, J. Guo, and M. S. Lundstrom, "Three-dimensional electrostatic effects of carbon nanotube transistors," *IEEE Transactions on Nanotechnology,* vol. 5, pp. 385-392, Jul 2006.
[21] G. Klimeck, R. Lake, R. C. Bowen, W. R. Frensley, and T. S. Moise, "Quantum device simulation with generalized tunneling formula," *Applied Physics Letters,* vol. 67, pp. 2539-2541, Oct 23 1995.
[22] R. C. Bowen, G. Klimeck, R. K. Lake, W. R. Frensley, and T. Moise, "Quantitative simulation of a resonant tunneling diode," *Journal of Applied Physics,* vol. 81, pp. 3207-3213, Apr 1 1997.
[23] S. Birner, T. Zibold, T. Andlauer, T. Kubis, M. Sabathil, A. Trellakis*, et al.*, "nextnano: General Purpose 3-D Simulations," *Electron Devices, IEEE Transactions on,* vol. 54, pp. 2137-2142, 2007.
[24] R. Lake, G. Klimeck, R. C. Bowen, and D. Jovanovic, "Single and multiband modeling of quantum electron transport through layered semiconductor devices," *Journal of Applied Physics,* vol. 81, pp. 7845-7869, Jun 1997.
[25] S. Datta, "Nanoscale device modeling: the Green's function method," *Superlattices and Microstructures,* vol. 28, pp. 253-278, 2000.
[26] A. Svizhenko, P. W. Leu, and K. Cho, "Effect of growth orientation and surface roughness on electron transport in silicon nanowires," *Physical Review B,* vol. 75, p. 125417, 2007.
[27] G. Klimeck, S. S. Ahmed, N. Kharche, M. Korkusinski, M. Usman, M. Prada*, et al.*, "Atomistic simulation of realistically sized nanodevices using NEMO 3-D - Part II: Applications," *IEEE Transactions on Electron Devices,* vol. 54, pp. 2090-2099, Sep 2007.
[28] A. Svizhenko, M. P. Anantram, T. R. Govindan, B. Biegel, and R. Venugopal, "Two-dimensional quantum mechanical modeling of nanotransistors," *Journal of Applied Physics,* vol. 91, pp. 2343-2354, 2002.
[29] D. Mamaluy, M. Sabathil, and P. Vogl, "Efficient method for the calculation of ballistic quantum transport," *Journal of Applied Physics,* vol. 93, pp. 4628-4633, Apr 2003.
[30] R. Zhibin, R. Venugopal, S. Goasguen, S. Datta, and M. S. Lundstrom, "nanoMOS 2.5: A two-dimensional simulator for quantum transport in double-gate MOSFETs," *Electron Devices, IEEE Transactions on,* vol. 50, pp. 1914-1925, 2003.
[31] M. Bescond, N. Cavassilas, K. Kalna, K. Nehari, L. Raymond, J. L. Autran*, et al.*, "Ballistic transport in Si, Ge, and GaAs nanowire MOSFETs," in *IEEE International Electron Devices Meeting*, Washington, DC, 2005, pp. 533-536.

[32] G. Fiori and G. Iannaccone, "Three-dimensional simulation of one-dimensional transport in silicon nanowire transistors," *Ieee Transactions on Nanotechnology,* vol. 6, pp. 524-529, Sep 2007.
[33] M. Luisier, A. Schenk, and W. Fichtner, "Quantum transport in two- and three-dimensional nanoscale transistors: Coupled mode effects in the nonequilibrium Green's function formalism," *Journal of Applied Physics,* vol. 100, 2006.
[34] G. D. Mahan, *Many-Particle Physics*. New York: Plenium, 1990.
[35] M. Luisier, A. Schenk, W. Fichtner, and G. Klimeck, "Atomistic simulation of nanowires in the sp(3)d(5)s(*) tight-binding formalism: From boundary conditions to strain calculations," *Physical Review B,* vol. 74, 2006.
[36] A. Wacker, "Semiconductor superlattices: a model system for nonlinear transport," *Physics Reports-Review Section of Physics Letters,* vol. 357, pp. 1-111, Jan 2002.
[37] J. Wang, E. Polizzi, and M. Lundstrom, "A three-dimensional quantum simulation of silicon nanowire transistors with the effective-mass approximation," *Journal of Applied Physics,* vol. 96, pp. 2192-2203, 2004.
[38] A. Martinez, M. Bescond, J. R. Barker, A. Svizhenko, M. P. Anantram, C. Millar*, et al.*, "A self-consistent full 3-D real-space NEGF simulator for studying nonperturbative effects in nano-MOSFETs," *Ieee Transactions on Electron Devices,* vol. 54, pp. 2213-2222, 2007.
[39] R. Venugopal, Z. Ren, S. Datta, M. S. Lundstrom, and D. Jovanovic, "Simulating quantum transport in nanoscale transistors: Real versus mode-space approaches," *Journal of Applied Physics,* vol. 92, pp. 3730-3739, Oct 2002.
[40] A. Martinez, A. R. Brown, A. Asenov, and N. Seoane, "A Comparison between a Fully-3D Real-Space Versus Coupled Mode-Space NEGF in the Study of Variability in Gate-All-Around Si Nanowire MOSFET," in *Simulation of Semiconductor Processes and Devices, 2009. SISPAD '09. International Conference on*, 2009, pp. 1-4.
[41] P. S. Damle, A. W. Ghosh, and S. Datta, "Nanoscale Device Modeling, Chapter in Molecular Nanoelectronics," M. Reed and T. L. Lee, Eds., ed: American Scientific Publishers, 2003.
[42] E. Polizzi and N. Ben Abdallah, "Subband decomposition approach for the simulation of quantum electron transport in nanostructures," *Journal of Computational Physics,* vol. 202, pp. 150-180, Jan 1 2005.
[43] S. Poli, M. G. Pala, T. Poiroux, S. Deleonibus, and G. Baccarani, "Size Dependence of Surface-Roughness-Limited Mobility in Silicon-Nanowire FETs," *Ieee Transactions on Electron Devices,* vol. 55, pp. 2968-2976, Nov 2008.
[44] R. Venugopal, S. Goasguen, S. Datta, and M. S. Lundstrom, "Quantum mechanical analysis of channel access geometry and series resistance in nanoscale transistors," *Journal of Applied Physics,* vol. 95, pp. 292-305, Jan 1 2004.
[45] J. Wang, E. Polizzi, A. Ghosh, S. Datta, and M. Lundstrom, "Theoretical investigation of surface roughness scattering in silicon nanowire transistors," *Applied Physics Letters,* vol. 87, Jul 25 2005.
[46] C. Buran, M. G. Pala, M. Bescond, M. Dubois, and M. Mouis, "Three-Dimensional Real-Space Simulation of Surface Roughness in Silicon Nanowire FETs," *IEEE Transactions on Electron Devices,* vol. 56, pp. 2186-2192, Oct 2009.
[47] E. Polizzi and N. Ben Abdallah, "Self-consistent three-dimensional models for quantum ballistic transport in open systems," *Physical Review B,* vol. 66, Dec 15 2002.

[48] M. Shin, "Quantum simulation of device characteristics of silicon nanowire FETs," *Ieee Transactions on Nanotechnology,* vol. 6, pp. 230-237, 2007.
[49] S. Horiguchi, "Validity of effective mass theory for energy levels in Si quantum wires," *Physica B: Condensed Matter,* vol. 227, pp. 336-338, 1996.
[50] S. Datta, *Electronic Conduction in Mesoscopic Systems*: Cambridge Univ. Press 1996.
[51] S. Datta, *Electronic Transport in Mesoscopic Systems*: Cambridge University Press, 1997.
[52] M. P. Anantram and A. Svizhenko, "Multidimensional Modeling of Nanotransistors," *Electron Devices, IEEE Transactions on,* vol. 54, pp. 2100-2115, 2007.
[53] A. Afzalian, N. D. Akhavan, C. W. Lee, Y. R., I. Ferain, P. Razavi*, et al.*, "A new F(ast)-CMS NEGF algorithm for efficient 3D simulations of switching characteristics enhancement in constricted tunnel barrier silicon nanowire MuGFETs," *Journal of Computational Electronics,* vol. 8, pp. 287-306, 2009.
[54] E. Polizzi and S. Datta, "Multidimensional nanoscale device modeling: the finite element method applied to the non-equilibrium Green's function formalism," in *Nanotechnology, 2003. IEEE-NANO 2003. Third IEEE Conference on*, 2003, pp. 40-43 vol.2.

Chapter 3 : Electron-Phonon interaction in polar and non-polar semiconductor devices

3.1. Introduction

It is expected that device dimensions reach the sub-10nm regime in the near future. For devices with gate length equal to 10 nm or below 10 nm, the channel and gate length become comparable to scattering lengths. In this case the interplay between the various mobility limiting mechanisms needs to be established. In long channel MOSFETs, the channel and gate lengths are much larger than the scattering lengths and electron-phonon interaction yields a significant contribution to decreasing the mobility. Since the physics of nanodevices can be affected by electron-phonon scattering interactions, these effects cannot be neglected in determining the correct drive current. In this section, we briefly describe the expressions for self-energies of the electron-phonon and polar optical interactions which are included in the NEGF formalism within a perturbative model within the self-consistent Born approximation [1-6].

Electron-phonon scattering contributions are included as in- and out-scattering functions in NEGF. Assuming thermal equilibrium and using the self-consistent Born approximation, the in- and out-scattering functions due to the electron-phonon interaction can be written as [6-8]:

$$\sum^{in,out}(x_1, x_2) = D^{n,p}(x_1, x_2)G^{n,p}(x_1, x_2) \qquad 3.1$$

where $x_1=(\mathbf{r}_1,t_1)$ and $x_2=(\mathbf{r}_2,t_2)$ contain spatial coordinate and time variables. Figure 3.1 represents the Feynman diagram for the first self-consistent Born approximation of phonon scattering interaction [6].

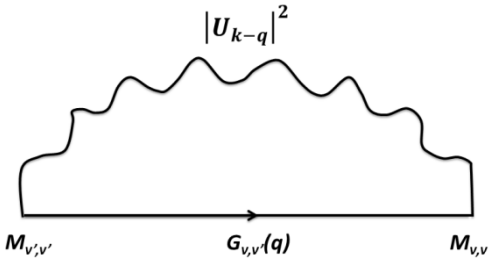


Figure 3.1 - Feynman diagram representation for the first self-consistent Born approximation of phonon scattering

The phonon propagator carries the average over the random variables of the phonon reservoir and can be written as follows [6]:

$$D^n(x_1, x_2) = \langle H_{ep}(x_1) H_{ep}(x_2) \rangle \qquad 3.2$$

$$D^p(x_1, x_2) = \langle H_{ep}(x_2) H_{ep}(x_1) \rangle \qquad 3.3$$

H_{ep} is the electron-phonon interaction Hamiltonian and is defined as follows:

$$H_{ep}(r,t) = \sum_q M_q a_q \left(b_q e^{-i\omega_q t + iqr} + b_q^\dagger e^{i\omega_q t - iqr} \right) \qquad 3.4$$

where b_q and $b_q^\dagger$ are the creation and annihilation operators for phonons in the mode q, and a_q is the half-amplitude of one phonon and is defined as:

$$a_q = \sqrt{\frac{\hbar}{2\rho V \omega_q}} \qquad 3.5$$

where V and ρ are the total volume and density of the device, respectively.
At the thermal equilibrium condition, the averages of the operator products in a reservoir satisfy the following expressions:

$$\langle b_q b_{q'}^\dagger \rangle = \delta_{qq'} N_q \,, \qquad \langle b_{q'} b_q^\dagger \rangle = \delta_{qq'} \left(N_q + 1 \right) \qquad 3.6$$

Where N_q is the phonon occupation number that follows the Bose-Einstein distribution and is given by:

$$N_q = \frac{1}{e^{\hbar\omega_q/k_BT} - 1} \tag{3.7}$$

where k_B and T are the Boltzmann constant and the lattice temperature, respectively. Note that all other averages of the operator products are zero. By substituting Eqs. 3.4-3.6 in Eq. 3.2 one gets:

$$D^n(r_1,t_1,r_2,t_2) = \sum_q |M_q|^2 a_q^2 \left[N_q e^{\left(i\omega_q(t_1-t_2)+iq(r_2-r_1)\right)} + (N_q+1)e^{\left(i\omega_q(t_2-t_1)+iq(r_1-r_2)\right)}\right] \tag{3.8}$$

A similar expression can be derived for D^p. By considering the stationary state and after applying the Fourier transform with respect to (t_1-t_2) the energy-dependent in- and out-scattering functions become as follows [6]:

$$\sum^{in}(r_1,r_2;E) = D(r_1,r_2;E)\,(N_q+1)G^n(r_1,r_2;E+\hbar\omega_q) + D^*(r_1,r_2;E)N_qG^n(r_1,r_2;E-\hbar\omega_q) \tag{3.9}$$

$$\sum^{out}(r_1,r_2;E) = D^*(r_1,r_2;E)\,(N_q+1)G^p(r_1,r_2;E-\hbar\omega_q) + D(r_1,r_2;E)N_qG^p(r_1,r_2;E+\hbar\omega_q) \tag{3.10}$$

The first and second terms in the expressions above indicate emission and absorption of a phonon, respectively. The electron-phonon scattering operator D is defined as follows:

$$D(r_1,r_2;E) = \sum_q |M_q|^2 a_q^2 e^{(iq(r_1-r_2))} \tag{3.11}$$

Three specific phonon-mediated scattering mechanisms which have been used in this work are briefly discussed in the following sections.

3.2. Self-energy for intravalley acoustic phonon scattering

In quasi-elastic scattering processes, we can neglect the energy of a phonon when comparing with the characteristic energy differences. This is approximately the case for acoustic phonons, hence we assume acoustic phonon scattering as an elastic process.

For intravalley acoustic phonon scattering, the phonon energy $\hbar\omega_q$ is usually much smaller than the thermal energy k_BT, therefore, the phonon number can be approximated as:

$$N(\hbar\omega_q) \approx N(\hbar\omega_q) + 1 \approx \frac{k_B T}{\hbar\omega_q} \gg 1 \qquad 3.12$$

As a result, the expression of absorption processes becomes the complex conjugate of the expression for the emission processes. For elastic acoustic phonon scattering, we take $|M_q| \approx qD_{ac}$ and $\omega_q = u_l q$ where u_l is the sound velocity. Knowing that the summation of the exponent over the first Brillouin zone, where the coordinates belong to the Bravais lattice gives the Kronecker delta function of the grid coordinates [9] one can conclude [6]:

$$\sum^{in}(r_1, r_2; k, E) = \sum_{q_l, q_t} (qD_{ac})^2 \frac{\hbar}{2\rho V \omega_q} \frac{k_B T}{\hbar\omega_q} e^{(iq(r_1 - r_2))} G^n(r_1, r_2; k, E) + c.c. \qquad 3.13$$

In the above an isotropic deformation potential model has been applied with the coupling constant D_{ac}. Although the deformation potential interaction between electrons and acoustic phonons is anisotropic it has been reported that nonparabolicity cancels the effect of the anisotropy [10]. Therefore, we can assume a standard scalar deformation potential for the intravalley phonon scattering [11] which vanishes the matrix element for the transverse acoustic modes. The isotropic model also applies in 110-oriented Si nanowire channels with very small diameter (below 5 nm) [12]. Finally, lumping the emission and absorption processes into one term gives [6]:

$$\sum^{in}(r_1, r_1; k, E) = K_{ac} G^n(r_1, r_1; k, E) \qquad 3.14$$

where acoustic phonon coupling constant is:

$$K_{ac} = \frac{D_{ac}^2 k_B T}{\rho u_l^2 a} \qquad 3.15$$

One can see that the in-scattering function is diagonal, thereby allowing us to use a very efficient algorithm such as the recursive Green's function algorithm to make simulations faster. The parameters for the acoustic phonon scattering rate in silicon and germanium are summarized in Table 3.1 [11, 13].

Table 3.1 - The acoustic phonon scattering rate (X and L reperesnts the related values for X and L valleys)

Material	D_{acX}	D_{acL}	P	u_l
Silicon	9.5 eV	-	2.33×10^{-3} kg/cm^3	9.0×10^5 cm/sec
Germanium	9 eV	11 eV	5.32×10^{-3} kg/cm^3	5.4×10^5 cm/sec

3.3. Self-energy for intervalley optical phonon scattering

Electron transition between states of two different equivalent valleys can be triggered by both acoustical and optical phonons. For equivalent X-X intervalley scattering, the scattering process is subdivided into the so-called f-type and g-type processes, while for equivalent L-L intervalley scattering there is no separation into f- and g-type processes. If electrons are scattered between valleys oriented along the same axis the process is called f-type, otherwise it is called g-type. Assuming isotropic scattering with phonons of constant energy where $|M_q| \approx D_{op}$ and $\omega_q = \omega_0$, which can be a valid assumption for optical phonons in non-polar crystals, the electron-phonon scattering operator becomes [6]:

$$D(r_1, r_2; E) = \frac{\hbar {D_{op}}^2}{2\rho\omega_0 V} \sum_{q_l} e^{(iq(r_1 - r_2))} \qquad 3.16$$

As stated before the summation here gives a Kronecker delta of the grid coordinates [9]. As a result, the in-scattering function becomes:

$$\sum^{in}(r_1, r_1; k, E) = k_{op}(N_q + 1)\sum_{q_t} G^n(r_1, r_1; k + q_t, E + \hbar\omega_q) + k_{op}N_q \sum_{q_t} G^n(r_1, r_1; k - q_t, E - \hbar\omega_q) \quad 3.17$$

where the optical phonon coupling constant (k_{op}) is written as follows:

$$k_{op} = \frac{\hbar {D_{op}}^2}{2\rho\omega_0 a} \quad 3.18$$

where D_{op} denotes the optical deformation potential and ω_0 is the energy of the phonon involves in the scattering process. Again as before, the in-scattering function can be treated as diagonal and the recursive Green's function algorithm is used to make the speed up the simulations. The coupling constants and phonon energies for silicon and germanium are shown in Tables 3.2 and 3.3 for X-X and L-L intervalley scattering, respectively [11, 13, 14].

Table 3.2 - The coupling constants and phonon energies for the X-X intervalley scattering rate

		Silicon		Germanium	
Mode	Selection rule	D_{op} ($\times 10^8$ eV/cm)	$\hbar\omega_{vv}$ (eV)	D_{vv} ($\times 10^8$ eV/cm)	$\hbar\omega_{vv}$ (eV)
TA	g	0.5	0.012	0.49	0.006
LA	g	0.8	0.019	0.79	0.009
LO	g	11	0.062	9.5	0.037
TA	f	0.3	0.019	0.28	0.010
LA	f	2.0	0.047	1.94	0.028
LO	f	2.0	0.059	1.69	0.033

Table 3.3 - The coupling constant and phonon energy for the L-L intervalley scattering rate

	Silicon	Germanium
D_{op} ($\times 10^8$ eV/cm)	5.26	3.0
$\hbar\omega_{vv}$ (eV)	0.024	0.028

3.4. Self-energy for polar optical phonon scattering

Polar optical phonon scattering only takes place in polar III-V semiconductors such as GaAs, InAs and InP which are considered for channel materials. The M_q coupling constant is defined as follows [6]:

$$M_q^2 = \rho q^2 \omega_0^2 \left(\frac{1}{k_\infty} - \frac{1}{k_0}\right) \frac{q^2}{(q^2 + q_0^2)^2} \tag{3.19}$$

where k_∞ is the high frequency dielectric constant and q_0 is the inverse screening length. Inserting this in to Eq. 3.9, one can get:

$$\sum^{in}(r_1, r_2; k_t, E) = \frac{q^2\hbar\omega_0(N_q+1)}{2V}\left(\frac{1}{k_\infty} - \frac{1}{k_0}\right)\sum \frac{q^2}{(q^2+q_0^2)^2} e^{(iq(r_1-r_2))} G^n(r_1, r_2; k_t + q_t, E + \hbar\omega_0) + absorption \tag{3.20}$$

Then by calculating the dimensionless integral over momenta, the final form of the in-scattering function will be as follows [6]:

$$\sum^{in}(r_1, r_2; E) = \frac{q^2\hbar\omega_0}{2a(2\pi)^3}\left(\frac{1}{k_\infty} - \frac{1}{k_0}\right) J(|r_1 - r_2|, q_0)\left(\left(N_q + 1\right)G^n(r_1, r_2; E + \hbar\omega_0) + N_q G^n(r_1, r_2; E - \hbar\omega_0)\right) \tag{3.21}$$

The polar optical phonon coupling constant can be defined as follows:

$$k_{pop} = \frac{q^2\hbar\omega_0}{2a(2\pi)^3}\left(\frac{1}{k_\infty} - \frac{1}{k_0}\right) J(|r_1 - r_2|, q_0) \tag{3.22}$$

where the dimensionless integral over momenta is defined as [6]:

$$J(r, q_0) = a \int_0^{q_m} \frac{4\pi q^4}{(q^2 + q_0^2)^2} sinc(qr) dq \qquad 3.23$$

Here q_m is the maximum momentum. As this integral is complicated, the best way for its calculation is using numerical methods. Figure 3.2 shows the relative value of the integral for infinite screening length (q_0=0). It shows that the off-diagonal terms can be neglected within a reasonable approximation.

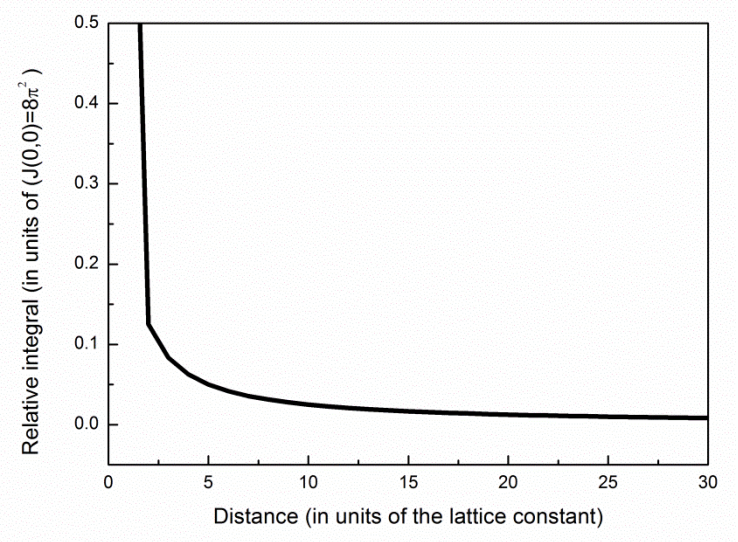


Figure 3.2 - Relative values of the integral J (r,q) for infinite screening length (q0=0).

3.5. Self-energy representation of phonon scattering in mode-space

In this section we discuss how to transform the self-energies from the real-space to the mode-space representation, since confined carriers in transverse directions separate the electronic states into the subbands (modes). The effect of the confined transversal modes can be considered by the summation of all possible transitions between subbands using corresponding form-factors. For a nanowire, the form factor (F) is defined as [15]:

$$F_{\nu',n}^{\nu,m}(x) = \oint \left|\xi^{\nu',n}(y,z;x)\right|^2 |\xi^{\nu,m}(y,z;x)|^2 \, dydz \qquad 3.24$$

and the general form of in/out scattering functions via the coupling constant, can be written as follows:

$$\sum^{in}(x;m;E) = k_{scat}(N_q+1)\sum_{n=1}^{M} F_{\nu',n}^{\nu,m}(x)G^n(x;n;E+\hbar\omega_q) + k_{scat}N_q\sum_{n=1}^{M} F_{\nu',n}^{\nu,m}(x)G^n(x;n;E-\hbar\omega_q) \quad 3.25$$

$$\sum^{out}(x;m;E) = k_{scat}(N_q+1)\sum_{n=1}^{M} F_{\nu',n}^{\nu,m}(x)G^p(x;n;E-\hbar\omega_q) + k_{scat}N_q\sum_{n=1}^{M} F_{\nu',n}^{\nu,m}(x)G^p(x;n;E+\hbar\omega_q) \quad 3.26$$

3.6. Conclusion

In this chapter we briefly explained how to derive the self-energy functions of the three different electron-phonon interactions, namely intervalley acoustic phonon and polar optical phonon, and intervalley optical phonon scattering, within the self-consistent Born approximation. We also showed how to transform these functions from the real-space representation to the mode-space representation. These self-energies are readily introduced into the NEGF formalism to take into account charge-carrier scattering by phonons.

References

[1] G. Klimeck, R. Lake, S. Datta, and G. W. Bryant, "Elastic and inelastic scattering in quantum dots in the Coulomb-blockade regime," *Physical Review B,* vol. 50, p. 5484, 1994.

[2] R. Lake and S. Datta, "Nonequilibrium Green's-function method applied to double-barrier resonant-tunneling diodes," *Physical Review B,* vol. 45, p. 6670, 1992.

[3] M. J. McLennan, Y. Lee, and S. Datta, "Voltage drop in mesoscopic systems: A numerical study using a quantum kinetic equation," *Physical Review B,* vol. 43, pp. 13846-13884, 06/15/ 1991.

[4] G. Klimeck, R. Lake, R. C. Bowen, W. R. Frensley, and D. Blanks, "Nano electronic modelling (NEMO)," in *Device Research Conference, 1995. Digest. 1995 53rd Annual*, 1995, pp. 52-53.

[5] S. Datta, "A simple kintetic-equation for steady-state quantum transport," *Journal of Physics-Condensed Matter,* vol. 2, pp. 8023-8052, Oct 1990.
[6] D. Nikonov, H. Pal, P. Gargini and G. Bourianoff, "Scattering in NEGF: Made simple," 2009. https://nanohub.org/resources/7772
[7] H. Haug and A.-P. Jauho, "Quantum Kinetics in Transport and Optics of Semiconductors," vol. 123, ed: Springer series in solid-state sciences, 1996.
[8] R. Lake, G. Klimeck, R. C. Bowen, and D. Jovanovic, "Single and multiband modeling of quantum electron transport through layered semiconductor devices," *Journal of Applied Physics,* vol. 81, pp. 7845-7869, Jun 1997.
[9] N. W. Ashcroft and N. D. Mermin, *Solid State Physics*: Brooks Cole, 1976.
[10] M. V. Fischetti and S. E. Laux, "Monte Carlo study of electron transport in silicon inversion layers," *Physical Review B,* vol. 48, pp. 2244-2274, 07/15/ 1993.
[11] C. Jacoboni and L. Reggiani, "The Monte Carlo method for the solution of charge transport in semiconductors with applications to covalent materials," *Reviews of Modern Physics,* vol. 55, pp. 645-705, 1983.
[12] F. Murphy-Armando, G. Fagas, and J. C. Greer, "Deformation Potentials and Electron−Phonon Coupling in Silicon Nanowires," *Nano Letters,* vol. 10, pp. 869-873, 2010/03/10 2010.
[13] M. Lundstrom, *Fundamentals of Carrier Transport*, 2 ed., Cambridge University Press, 2000.
[14] M. V. Fischetti, "Monte Carlo simulation of transport in technologically significant semiconductors of the diamond and zinc-blende structures. I. Homogeneous transport," *Electron Devices, IEEE Transactions on,* vol. 38, pp. 634-649, 1991.
[15] S. Jin, Y. J. Park, and H. S. Min, "A three-dimensional simulation of quantum transport in silicon nanowire transistor in the presence of electron-phonon interactions," *Journal of Applied Physics,* vol. 99, pp. 123719-10, 2006.

Chapter 4 : Comparison of breakdown voltage in bulk and SOI FinFETs

4.1. Introduction

As discussed in the introductory chapter of this thesis, the semiconductor industry faces new challenges due to continuous shrinking of device dimensions. Double-gate MOSFETs show better control of short-channel effects than single-gate MOSFETs and are a promising candidate for future CMOS applications. For example, the 16 nm or 14 nm FinFET, which is a self-aligned double-gate MOSFET [1], is already in the production plans of chip manufacturers such as TSMC, Samsung, IBM, and Global Foundries. FinFET devices can be fabricated on both silicon-on-insulator (SOI) and bulk wafers. Each of these devices presents some advantages and some drawbacks. SOI devices have better control of short channel effects but may suffer from floating body effect and self-heating issues. Wafer cost and defect density may be lower if bulk devices are used [2].

The breakdown phenomenon limits the highest applicable voltage to the device, and therefore affects the speed and power handling capability of MOSFET devices [3]. Therefore, breakdown voltage is a very important parameter in MOSFET design. Moreover, understanding the breakdown phenomenon in multiple-gate MOSFETs (MuGFETs) is very important for several reasons. For example, impact ionization and bipolar effects are bases of programming in a device such as the ZRAM memory cell. These effects must be used without triggering drain breakdown [4]. In this section, we simulate and compare the drain breakdown voltage of SOI and bulk FinFETs [5]. We also investigate the influence of different channel doping values, gate lengths, and fin widths on the breakdown voltage of SOI and bulk FinFETs.

Our aim is to identify the differences in the breakdown voltage of SOI and bulk MOSFETs and determine the effect of the various geometrical parameters and doping concentration for each type of device. We also compare with experimental data to validate our simulation results. After introducing the device structures and parameters of our simulations in the next section, we present the discussion of our results and their validation in section 4.3. The chapter concludes with a brief summary.

4.2. Device structure and simulation parameters

The 3D schematic and cross-sectional view along the gate of the simulated devices is shown in Figure 4.1. We have used the Silvaco Atlas 3D device simulator [6] to simulate and compare the breakdown voltage of n-channel SOI and bulk FinFETs. The simulated structures have a uniform doping concentration in the source and drain regions ($N_{S/d}=1\times10^{20}$ cm^{-3}) and in the channel regions. Different channel doping values, gate lengths, and fin widths have been considered. In all simulations the gate workfunction is set to 4.65 eV and the breakdown voltages of all devices are extracted at V_{GS}=0.1V by applying a voltage ramp to the drain and the substrate is grounded. In order to account for non-local effects we have used the energy balance model in our simulations. Compared with the drift diffusion models, the energy balance model provides a more accurate description of physical device effects such as the effect of velocity overshoot and non-local impact ionization which is important in breakdown simulations.

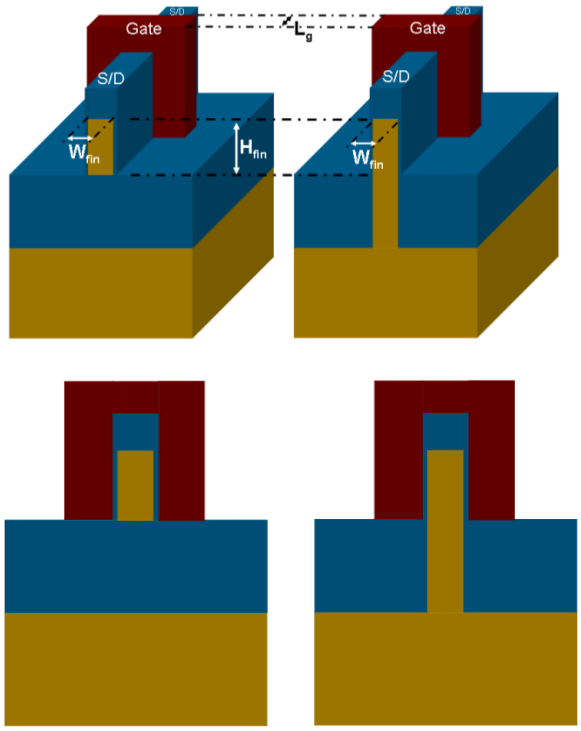


Figure 4.1- (a) 3D schematics and (b) Cross-sectional view along the gate of bulk and SOI FinFET structures

4.3. Simulation results and discussion

In order to compare the drain breakdown voltage, we have to use a definition of drain breakdown voltage that can be used with devices with different channel lengths, fin widths, and doping concentrations. To this end, the derivative method is applied [4]. Since it is hard to determine the breakdown voltage accurately from the output characteristics, we have extracted the breakdown voltage by plotting $d(\log(I_{DS})/dV_{DS}$ as a function of drain voltage. Such a plot yields well-defined peaks that correspond to the drain breakdown voltage. These peaks can be seen in Figure 4.2. This method has been found to be reliable and reproducible for extracting drain breakdown voltages [4].

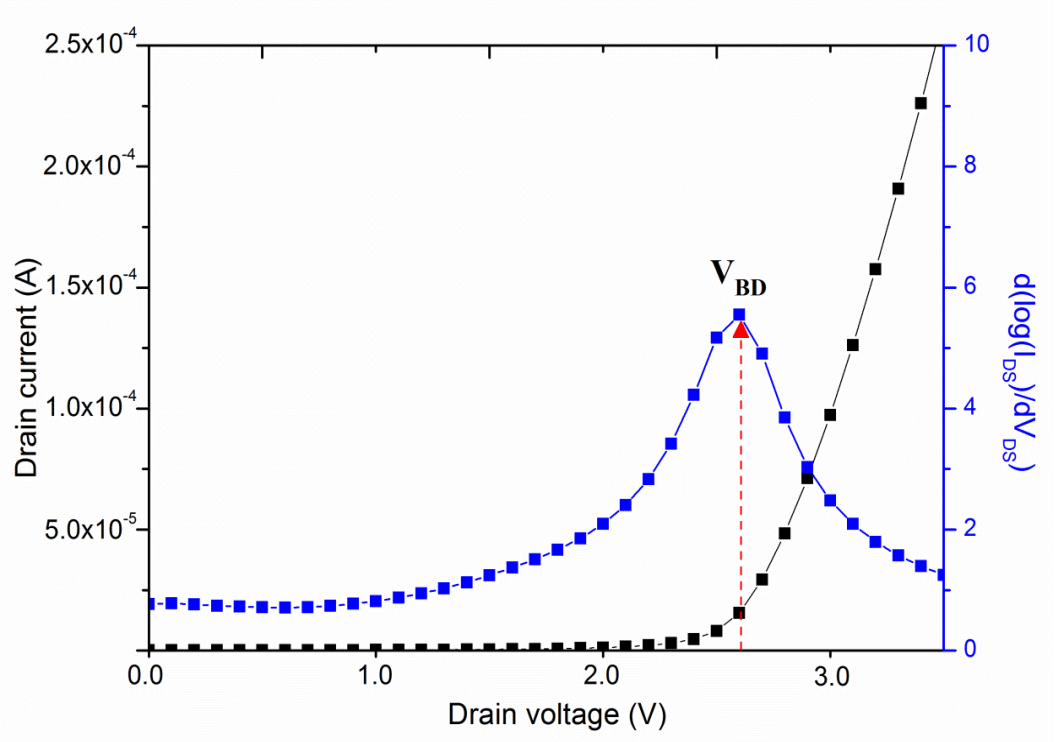


Figure 4.2 - Extraction of breakdown voltage by the derivative method (V_{gs} = 0.1 V).

Figure 4.3 shows the breakdown voltage of the bulk and SOI FinFETs for different gate lengths. It can be seen in this figure that the breakdown voltage of both structures decreases when decreasing the gate length due to the increased impact ionization and decreased potential barrier in the channel of the devices (Figures 4.4 and 4.5). Figure 4.3 also shows that the breakdown voltage of the SOI FinFET is lower than that of the bulk FinFET. The floating-body effect of the SOI device and the parasitic n-p-n bipolar transistor which is present in the SOI device causes the

breakdown voltage of the SOI device to be lower than in the bulk device [2]. Figure 4.6 illustrates the presence of the floating-body. The impact ionization which occurs near the drain junction produces electron–hole pairs and the generated holes drift toward the source side. This hole drift provide the base current of the parasitic n-p-n bipolar transistor.

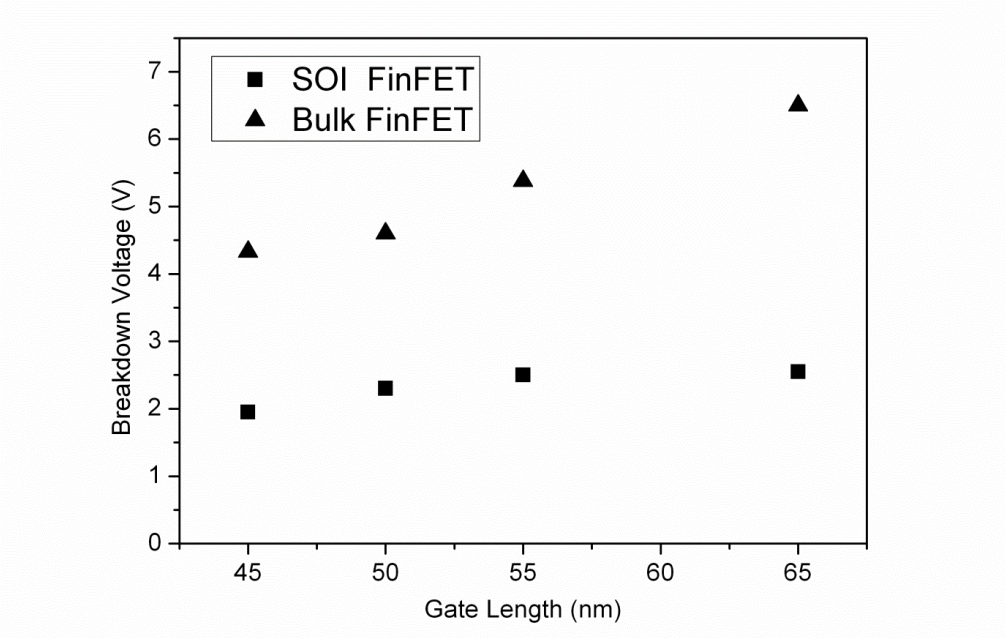


Figure 4.3 - Breakdown voltage comparison of bulk and SOI FinFETs for different gate lengths (W_{fin}=11 nm, H_{fin}=60 nm)

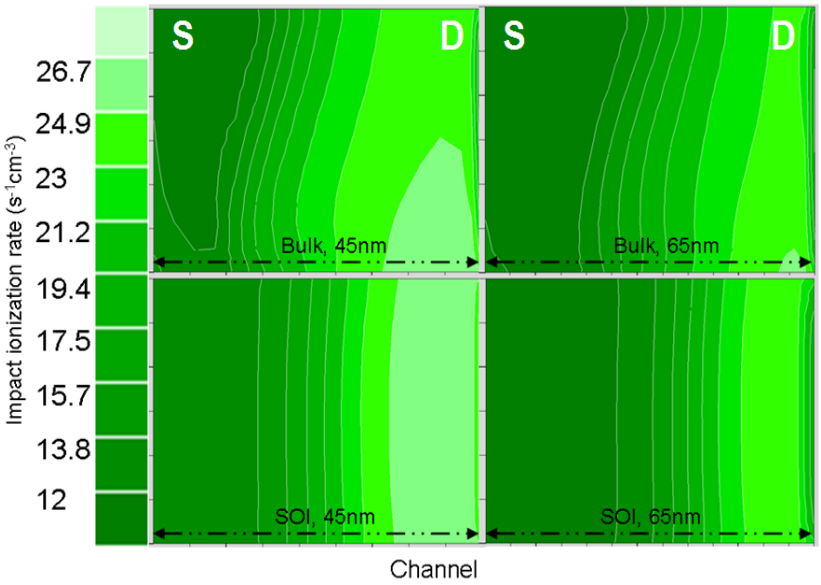


Figure 4.4 - Impact ionization rate of bulk and SOI FinFETs for different gate lengths (Vertical cut along source and drain, V_{ds}=1.5 V).

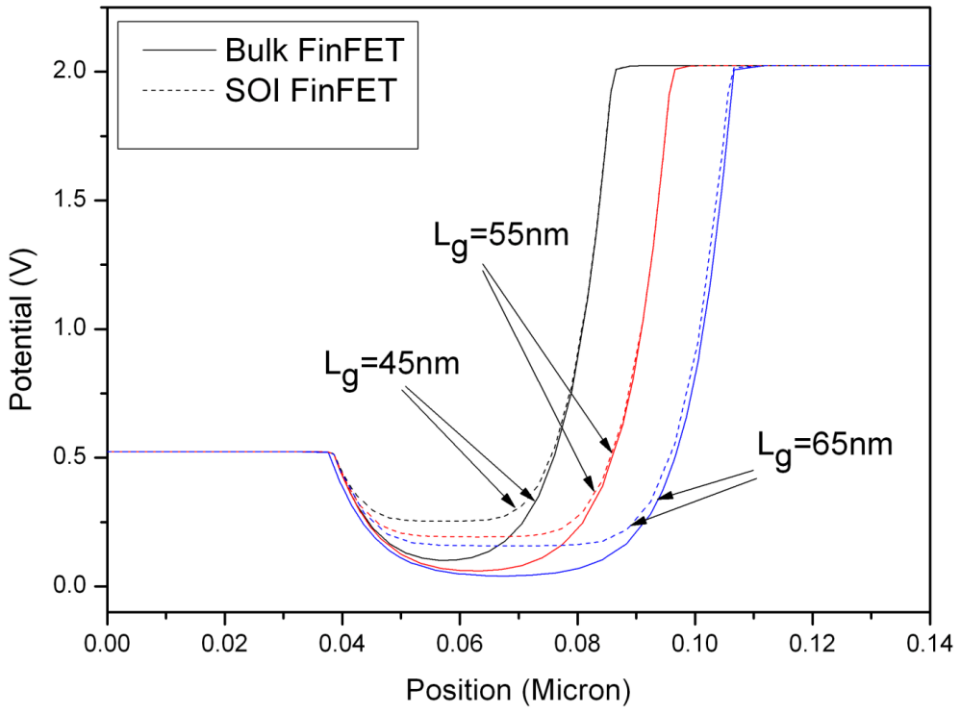


Figure 4.5 - Potential barrier of bulk and SOI FinFETs for different gate lengths (vertical cut along source and drain, V_{ds}=1.5V).

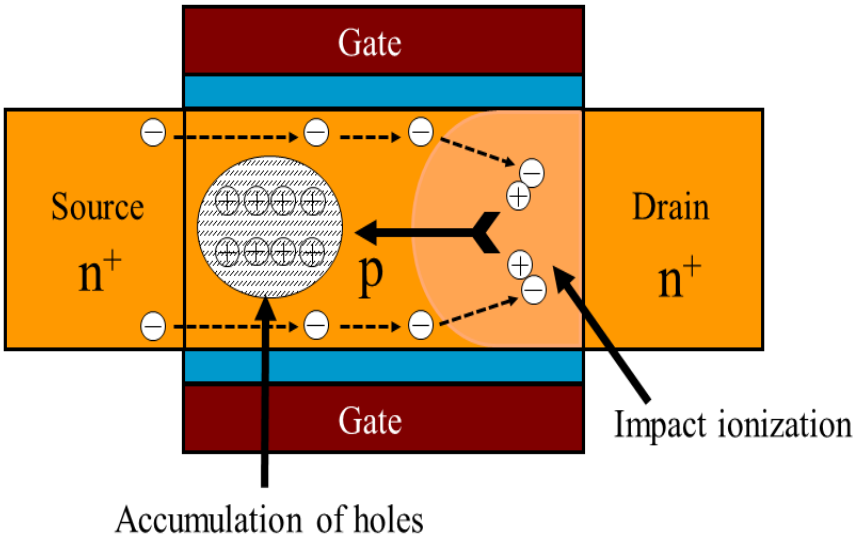


Figure 4.6 - Cross-sectional schematics of floating-body effect in SOI MOSFETs.

Figures 4.7 and 4.8, respectively, show the breakdown voltage of the bulk and SOI FinFETs for different fin widths and different channel doping values. As it can be seen in these figures, the breakdown voltage in both types of devices decreases when increasing the fin width or when decreasing the channel doping concentration. The reason for the reduction of breakdown voltage in both structures while lowering the channel doping concentration is the increase of the impact ionization rate and

decrease of the source to drain potential barrier as a result of lowering the channel doping concentration (as seen in Figure 4.9).

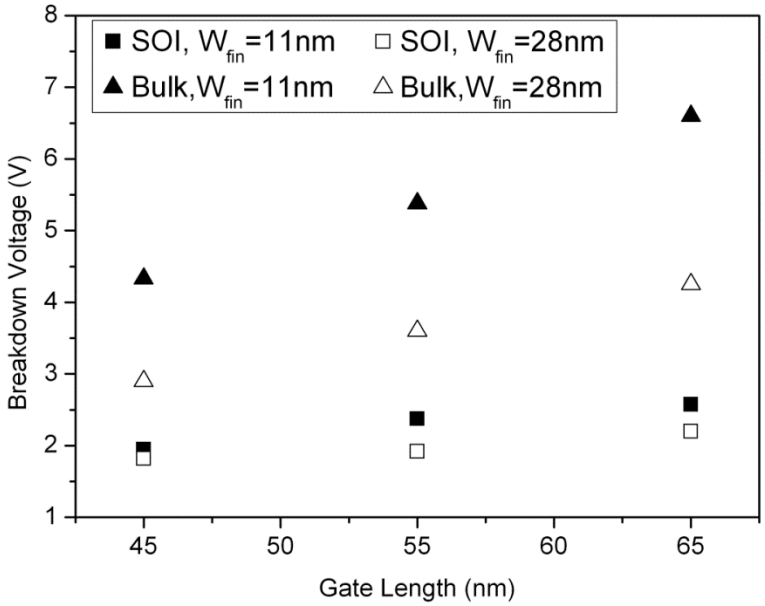


Figure 4.7 - Breakdown voltage of bulk and SOI FinFETs for different fin widths in different gate lengths (N_{ch}=2×10^{18} cm^{-3}).

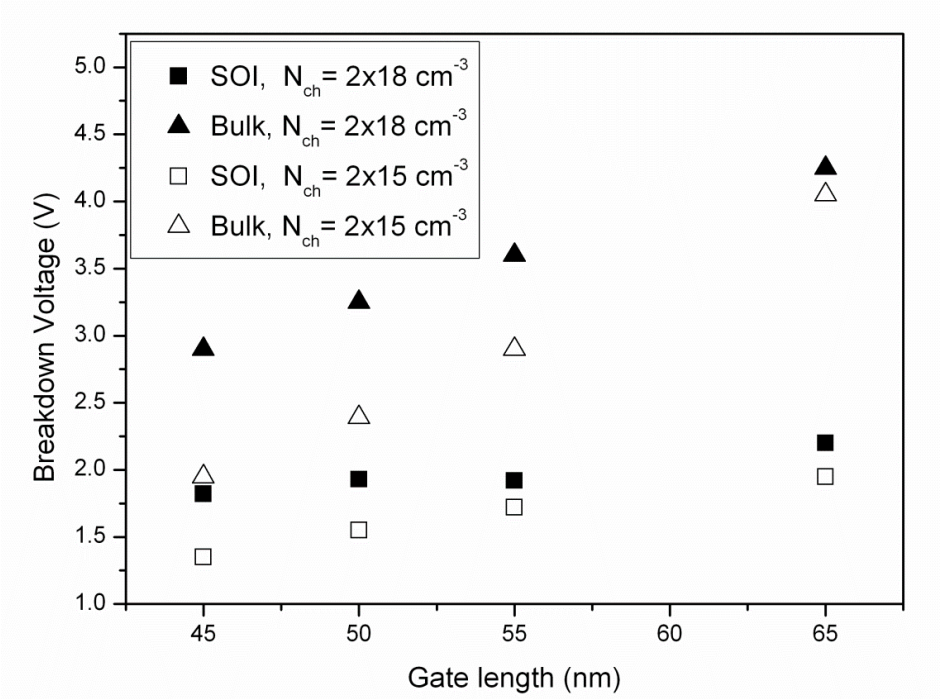


Figure 4.8 - Breakdown voltage of bulk and SOI FinFETs for different channel doping in different gate lengths (W_{fin}=28 nm)

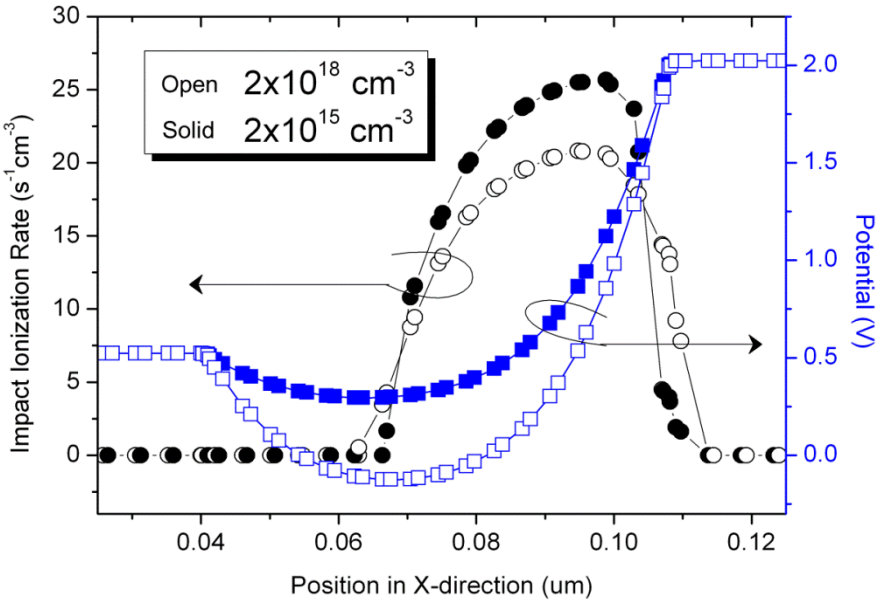


Figure 4.9 - Impact ionization and potential barrier in the middle of the channel of the SOI device for different channel doping (Vertical cut along source and drain, W_{fin}=28 nm, Lg= 65 nm).

All results obtained above are extracted after calibration of the simulator parameters using measurement results to get more accurate results. Measurement data have been provided by silicon research group at Tyndall National Institute. Figure 4.10 shows the good agreement of simulation and measured results for SOI FinFETs with different gate lengths.

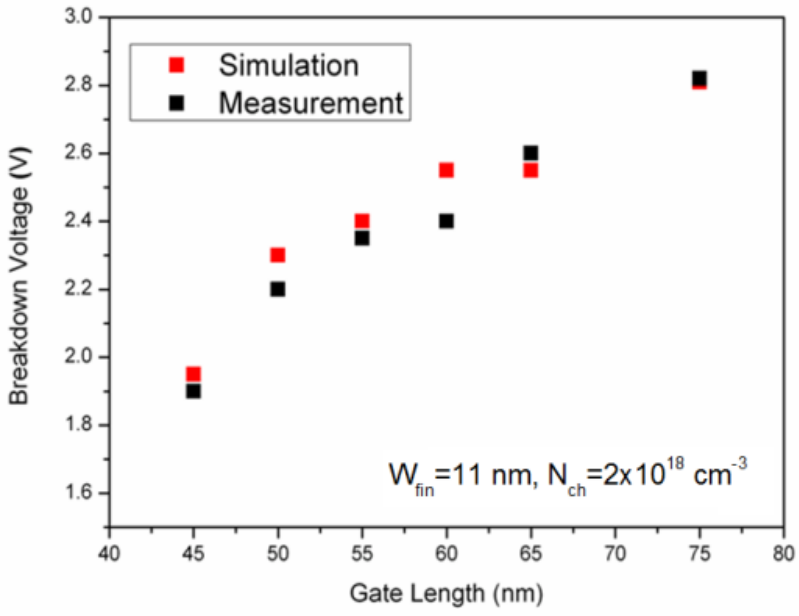


Figure 4.10 - Comparison of simulation and measured results for the SOI FinFET devices with different gate lengths.

4.4. Conclusion

The breakdown voltage of SOI FinFETs is lower than the breakdown voltage of bulk FinFETs because of the floating body effect and the parasitic bipolar structure with floating base that can amplify the impact ionization effect in the SOI device. The breakdown voltage of both bulk and SOI FinFETs decreases when decreasing the gate length, increasing the fin width, or decreasing the channel doping concentration.

References

[1] D. Hisamoto, L. Wen-Chin, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo*, et al.*, "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," *Electron Devices, IEEE Transactions on,* vol. 47, pp. 2320-2325, 2000.

[2] J.-P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*, 2nd ed., Springer, 1997.

[3] T. Toyabe, K. Yamaguchi, S. Asai, and M. S. Mock, "A numerical model of avalanche breakdown in MOSFET's," *Electron Devices, IEEE Transactions on,* vol. 25, pp. 825-832, 1978.

[4] C. W. Lee, A. Afzalian, R. Yan, N. D. Akhavan, X. Weize, and J.-P. Colinge, "Drain Breakdown Voltage in MuGFETs: Influence of Physical Parameters," *Electron Devices, IEEE Transactions on,* vol. 55, pp. 3503-3506, 2008.

[5] P. Razavi, R. Yan, I. Ferain, N. D. Akhavan, R. Yu, C.-W. Lee, and J.-P. Colinge, "Comparison of Breakdown Voltage in Bulk and SOI FinFETs," in *EUROSOI 2010, Sixth Workshop of the Thematic Network on Silicon on Insulator technology, devices and circuits*, Grenoble, France, 2010.

[6] http://www.silvaco.com.

Chapter 5 : Performance investigation of short-channel junctionless nanowire transistors versus inversion- and accumulation-mode Nanowire Transistors

5.1. Introduction

Conventional MOSFETs consist of two PN junctions called the source junction and the drain junction and these two regions are separated by a region with opposite doping type. For example for n-type MOSFET, the source and drain region have the n-type doping concentration while the channel has nominal p-type doping concentration. The distance which separates source and drain junctions determine the physical gate length of the device.

As stated in previous chapter, MOSFETs are shrinking rapidly, and will reach sub-10 nm regime in the next few years. Significant challenges such as the formation of source and drain junctions in short-channel devices has increased the complexity and cost of fabrication process. To minimize diffusion, flash annealing techniques are currently being used to heat semiconductors for a very short period of time. But even with the minimized diffusion, ion implantation and other doping techniques do not let manufactures to have perfectly abrupt junctions with infinite concentration gradients [1]. Therefore, using of different device structures has attracted attention of manufacture companies for very short channel devices to overcome the above-mentioned issues.

Using the Silicon-On-Insulator (SOI) technology, accumulation-mode (AM) devices, in which the channel region has the same doping type as the source and drain regions, can be an alternative choice for inversion-mode devices. AM MOSFETs are majority carrier devices, and use the ability of the gates to accumulate or deplete a channel region and turn the device ON or OFF, respectively [2]. An n-channel accumulation-mode device has N^+-N-N^+ dopant profile and a p-channel AM device has P^+-P-P^+ dopings in the source, channel and drain region, respectively. The AM devices with relatively thick silicon films (thicker than 30 nm) exhibit worse short-channel characteristics compared with the inversion-mode MOSFETs. This is

due to the fact that in AM devices the channel is formed deeper in the film, and as a result is further away from the gate electrodes. However, in thinner devices, this issue disappears [3]. Specifically in Multiple-Gate MOSFETs (MuGFETs) with a small enough cross section, it has been shown that there is no significant difference in short-channel effects between accumulation-mode and inversion-mode devices [4].

The other device architecture that is based on advanced SOI technology and is considered in this chapter is junctionless nanowire transistors (JNTs). These devices are heavily doped gated resistors with full MOSFET functionality and are made of thin N+ or P+ semiconductor nanowires. JNTs do not need the formation of extremely abrupt source and drain junctions, and as a result, fabrication process of these devices is much simpler than that of conventional CMOS devices [5]. The physics of the junctionless devices is different from that of the conventional inversion-mode (IM) devices [6]. JNTs are basically accumulation-mode transistors with high channel doping concentration and are essentially junction-free. The channel dimensions of nanowire in a junctionless device must be small enough to let the full depletion of carriers in the channel region when the device is in the off-state.

In this chapter we present our results on the performance of short-channel junctionless, inversion-mode and accumulation-mode nanowire transistors using classical and quantum simulations. Specifically, we start in the next section with a comparison of the gate-delay and emergy-delay product between JNTs and IM devices. In section 5.3 we discuss the switching speed in junctionless and accumulation-mode gate-all-around nanowire transistors. An evaluation of scaled JNTs against IM and AM devices is presented in sections 5.4 and 5.5 respectively, by comparing performance parameters in short-channel devices. These include the subthreshold swing, drain-induced-barrier-lowering, on-off current ratio, are presented. The chapter concludes with remarks on our findings.

5.2. Intrinsic gate delay and energy-delay product: JNTs vs IM devices

In this section, two key device metrics, namely, the intrinsic gate delay and energy-delay product, are studied for junctionless nanowire transistors with various

doping concentration [7]. These are compared with those of conventional triple-gate inversion-mode MOSFETs for short gate lengths of 22 nm and 15 nm. The effect of additional doping concentrations in source/drain contact regions of JNTs is also investigated.

5.2.1 Device structures and parameters

The energy-delay product is defined by $CV/I \times CV^2$ and the intrinsic gate-delay is defined by $\tau=CV/I$, where C is the gate capacitance, V is the supplied voltage of operation (V_{dd}), I is the on-state current and CV^2 is the switching energy (power-delay product). The intrinsic gate delay is important as it represents the frequency limit of the transistor operation. The energy-delay product is also a significant parameter as it represents the energy efficiency of the device. Figure 5.1 (a) and (b) show a bird's eye view of junctionless and IM triple-gate nanowire MOSFETs indicating the gate electrode length (L_{gate}), the width (W_{Si}) and the height (H_{Si}) of the silicon nanowire, gate overlap (L_{ov}) with the source and drain contact regions, as well as the doping profile in the longitudinal cross-sections of both junctionless and IM devices.

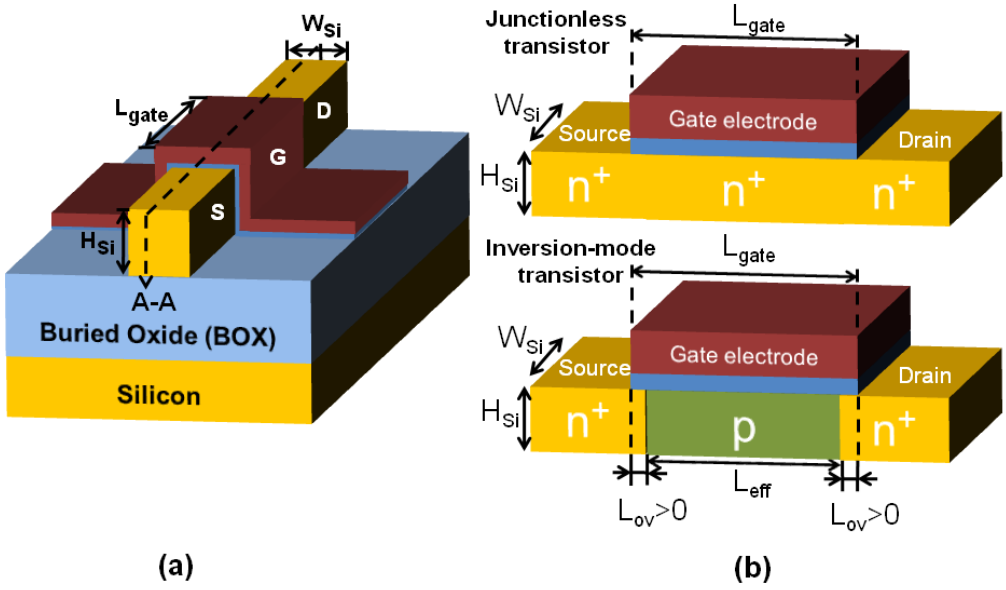


Figure 5.1 - (a) Bird's eye view of a junctionless and IM triple-gate nanowire MOSFETs (b) doping profile in the longitudinal cross-sections of JNTs and IM devices.

The Sentaurus three-dimensional device simulation tool [8] was used to design devices and simulate their electrical characteristics. The simulations were carried out for different gate lengths from 22 nm down to 15 nm. These correspond to technology nodes of current interest. For JNTs different doping concentrations and for IM devices different gate overlaps with source and drain contact regions are considered: from 0 nm (ideal device) up to 2 nm. Uniform doping concentration throughout the channel of the devices and source and drain regions has been used for both junctionless and IM devices. The doping concentration in JNTs is varied from 5×10^{18} cm^{-3} to 2×10^{19} cm^{-3}. JNTs are also simulated with extra doping concentration (10^{20} cm^{-3}) in the source and drain contact regions, away from an optimized distance from the gate edges. Source and drain junctions are assumed to be abrupt for the IM devices. Source/drain regions and channel doping concentrations in IM devices are 1×10^{20} cm^{-3} and 5×10^{17} cm^{-3}, respectively. An effective oxide thickness (EOT) of 1 nm is considered for all devices. By tuning the metal gate work function, all devices are designed to have the same threshold voltage of 0.5 V. The drift-diffusion simulations are carried out using Fermi-Dirac carrier statistics and quantization effects are included using the density gradient model. Mobility models include the effects of doping concentration and electric fields. Auger and Shockley-Read-Hall (SRH) recombination models are also included in the simulations to account for leakage currents. The supply voltages (V_{dd}) of 0.9 V and 0.78 V are considered for devices with gate length of 22 nm and 15 nm, respectively.

5.2.2 Results and discussion

Figures 5.2 and 5.3 illustrate the intrinsic gate delay and energy-delay product of JNTs for different doping concentration values, respectively. As it can be seen in these figures, by increasing the doping concentration from 5×10^{18} cm^{-3} to 2×10^{19} cm^{-3}, the intrinsic gate delay and the energy-delay product decrease. It is also shown that using additional doping concentrations in the source and drain contact regions, considering an optimized distance from the gate edges, decrease the intrinsic gate delay and energy-delay product.

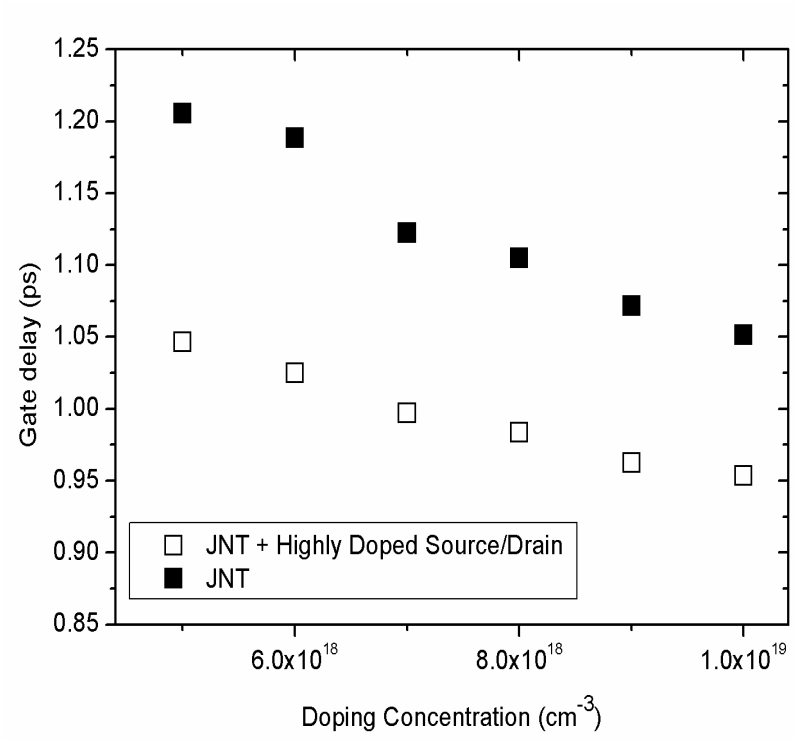


Figure 5.2 - Intrinsic gate delay of junctionless nanowire transistors for different doping concentration values (L_{gate}=15 nm).

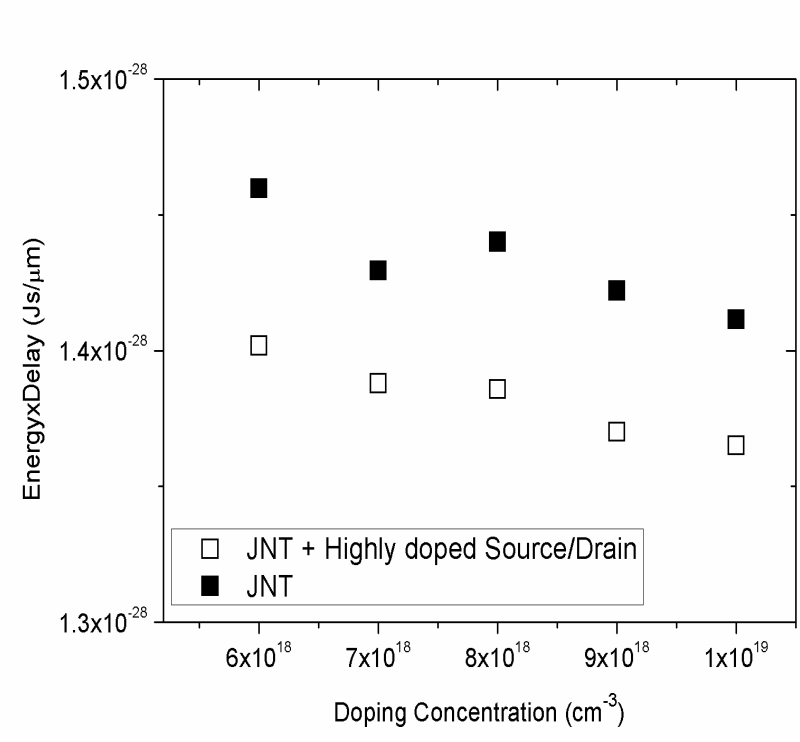


Figure 5.3 - Energy-delay product of junctionless nanowire transistors for different doping concentration values (L_{gate}=15 nm).

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Figure 5.4 shows the comparison of intrinsic gate delay in JNTs and IM devices. Varying doping concentrations and cross sections for JNTs and different cross sections and gate overlap with source and drain contact regions for IM devices have been considered for devices with gate lengths 15 nm and 22 nm. As it can be seen in this figure, intrinsic gate delay is less in IM devices compared with the simulated JNTs. This is because of the higher on-state current in IM devices as it can be seen in Figures 5.5 and 5.6.

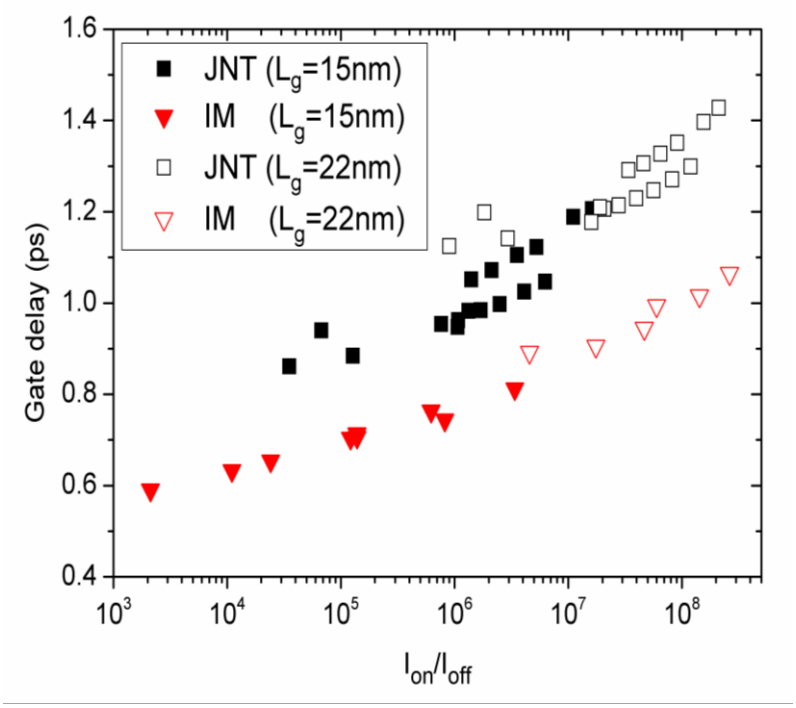


Figure 5.4 - Comparison of intrinsic gate delay in JNTs and IM devices for gate lengths 15 nm and 22 nm.

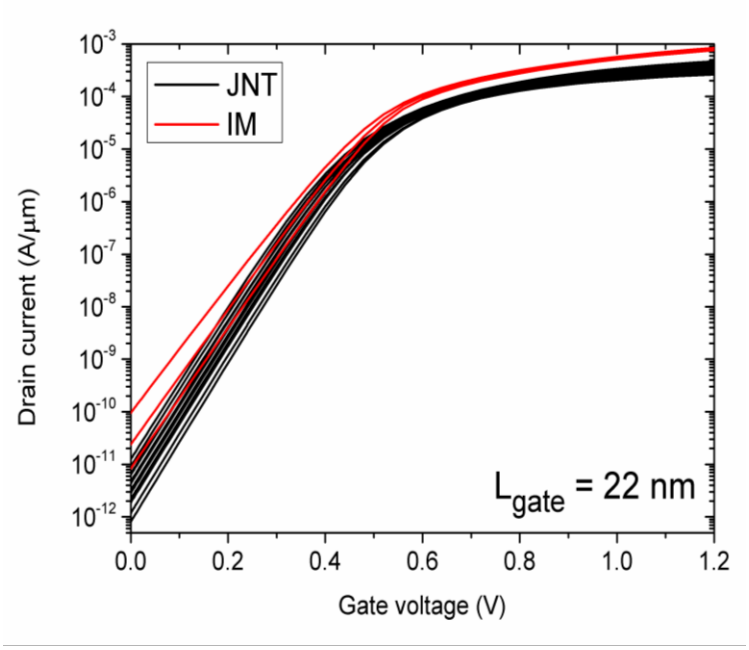


Figure 5.5 - Comparison of drain current versus gate voltage in JNTs and IM devices (L_{gate}=22 nm).

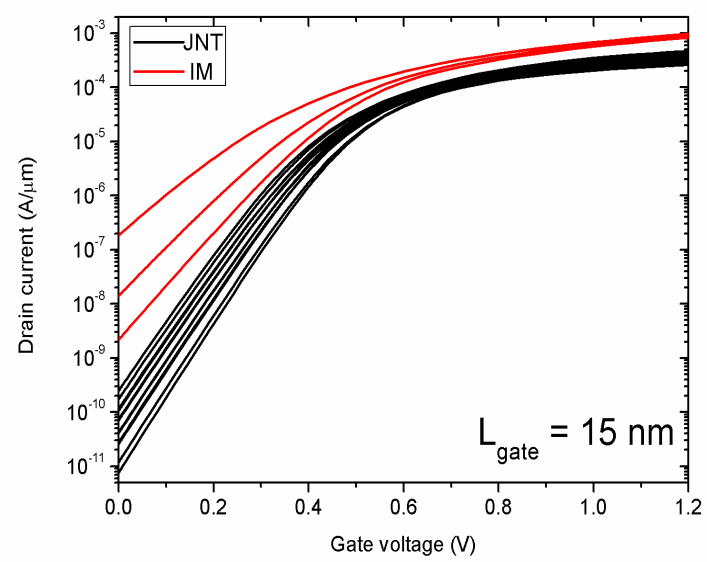


Figure 5.6 - Comparison of drain current versus gate voltage in JNTs and IM devices (L_{gate}=15 nm).

Comparison of the switching energy in JNTs and IM devices can be seen in Figure 5.7. As it has been illustrated in this figure, the switching energy in JNTs is less than IM devices which is due to smaller gate capacitances in JNTs compared with that of IM devices. As a result, although the intrinsic gate delay of JNTs is more than in IM devices, the energy-delay product of JNTs and IM devices is almost identical due to the lower switching energy of JNTs. This is demonstrated in Figure 5.8.

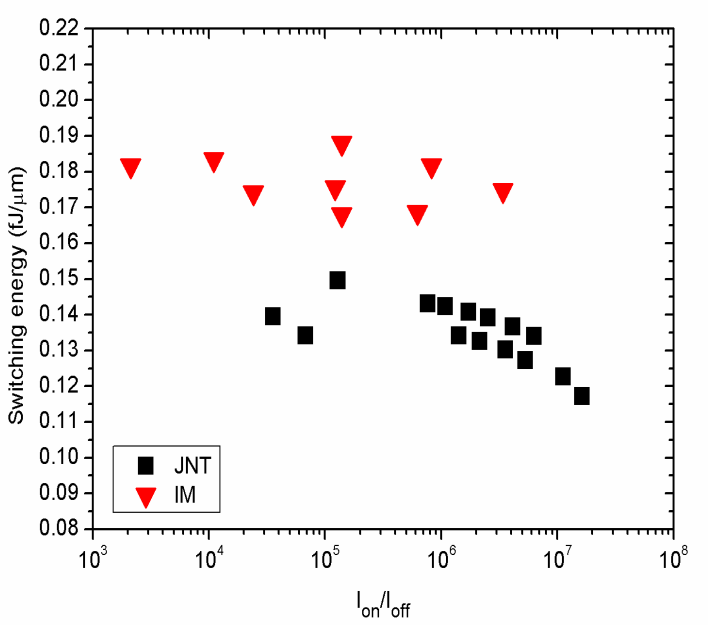


Figure 5.7 - Comparison of switching energy in JNTs and IM devices (L_{gate}=15 nm).

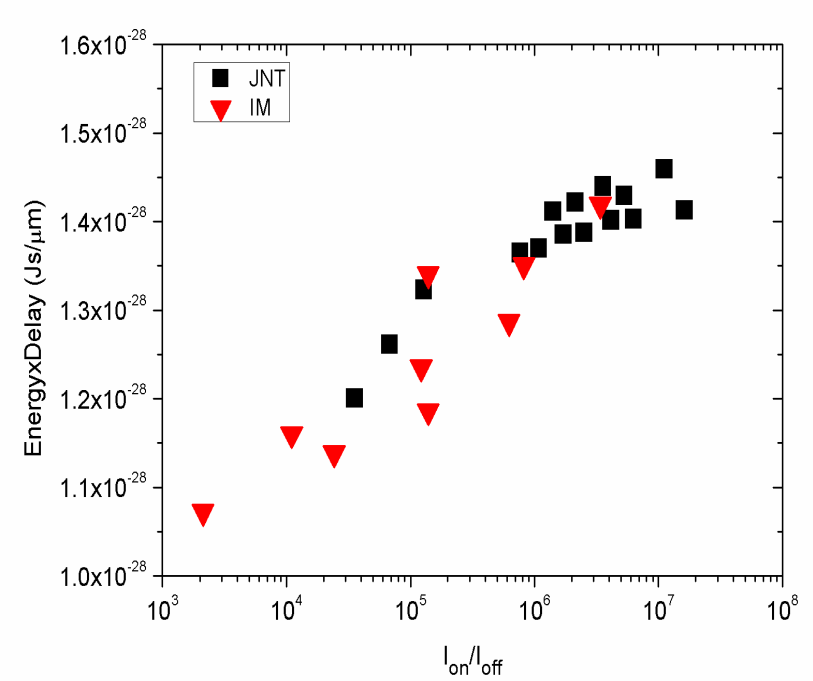


Figure 5.8 - Comparison of energy-delay product in JNTs and IM devices (L_{gate}=15 nm).

5.3. Switching speed in junctionless and accumulation-mode gate-all-around nanowire transistors

In this section, we investigate and compare the switching speed of junctionless and accumulation-mode (AM) gate-all-around (GAA) nanowire transistors using both 3D quantum and classical simulations [9].

5.3.1 Device structures and parameters

The 3D schematic and longitudinal cross-section view of the simulated devices are shown in Figures 5.9 and 5.10, respectively. We have used our 3D simulator based on the non-equilibrium Green's function (NEGF) formalism for the quantum results and the Atlas 3D device simulator [10] for our classical calculations. Simulations have been carried out for low (3×10^{19} cm^{-3}) and high (7×10^{19} cm^{-3}) doping concentrations for the junctionless devices. The AM devices have also low (3×10^{19} cm^{-3}) and high (7×10^{19} cm^{-3}) doping concentrations in the source/drain extensions and 1×10^{16} cm^{-3} in the channel. In all simulation results, the drain bias is 0.4 (V) and the gate length is 15 nm.

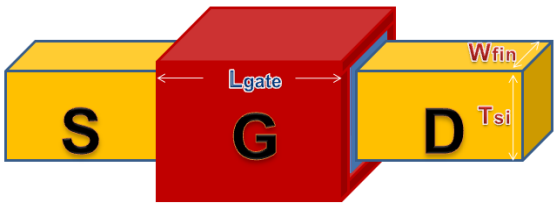


Figure 5.9 - 3D schematic of AM and junctionless GAA nanowire transistors.

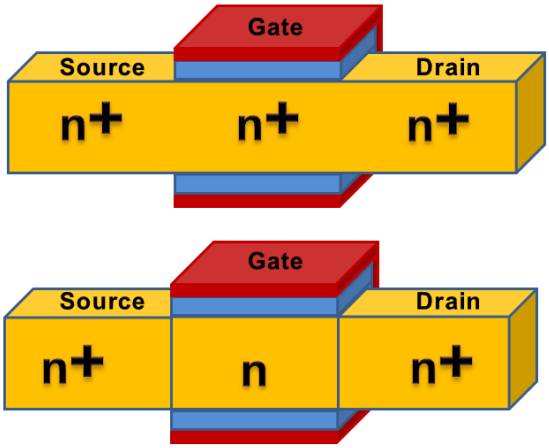


Figure 5.10 - Longitudinal cross-section view of junctionless GAA nanowire transistor (top) and AM GAA nanowire transistor (bottom) used in this work.

5.3.2 Results and discussion

To compare the switching speed of junctionless and AM gate-all-around nanowire transistors we use the switching time calculated using $\tau=Q/I$T, where Q is the charge in the gate when applying $V_g=V_{th}+0.2$ (V) and I is the drain current at $V_g=V_{th}+0.2$ (V). Tables 5.1 and 5.2 show the switching time of GAA nanowire transistors for different cross sections and doping concentration values, simulated using classical and quantum simulators, respectively. The quantum mechanical treatment results in increased threshold voltage of the device. As a result, the on-current calculated classically is higher than the on-current which is calculated by the quantum simulation. As it can be seen in Tables 5.1 and 5.2, usually the classical simulations predict less switching time compared to quantum simulations.

Table 5.1 - Switching time (ps) calculated by classical simulator at $V_{gs}=V_{th}+0.2$ (V).

Cross section (nm^2)	AM Low doped S/D	JNT Low doped	AM High doped S/D	JNT High doped
5×5	0.3	0.48	0.3	0.53
6×6	0.3	0.49	0.3	0.55
7×7	0.3	0.51	0.3	0.56

Table 5.2 - Switching time (ps) calculated by quantum simulator at *Vgs=Vth*+0.2 (V).

Cross section (nm^2)	AM Low doped S/D	JNT Low doped	AM High doped S/D	JNT High doped
5×5	0.41	0.41	0.61	0.61
6×6	0.48	0.51	0.75	0.9
7×7	0.58	0.63	0.93	1.08

From Table 5.1, it can be seen that the AM device has a lower switching time than the junctionless device for different cross sections and doping concentration values. Quite different results are obtained when quantum simulations are used (Table 5.2). From Table 5.2 it can be seen that for larger cross-sections the AM device has a lower switching time than JNTs but by decreasing the cross section of the devices

both junctionless and AM devices tend to have very similar switching times. The reason can be explained in Figures 5.11 and 5.12. Figure 5.11 shows the electron density of junctionless and AM devices calculated by quantum simulations. As it can be seen in this figure the current flow is in the middle of the junctionless device for both cross-sections. In AM devices the current flow is more at surface of the device when the cross section is large, while the current flows preferentially in the middle of the device when the cross section is decreased, due to quantum effects. Figure 5.12 shows the electron density in the junctionless and AM devices, calculated using classical simulations. As it can be seen in this figure, the current flow for the 7×7 nm^2 AM transistor is mostly at the surface of the device but unlike the quantum simulation, the current density is still mostly at the surface when the cross section is reduced. This shows that classical simulations are no longer valid for GAA devices with 5×5 nm^2 cross section dimensions.

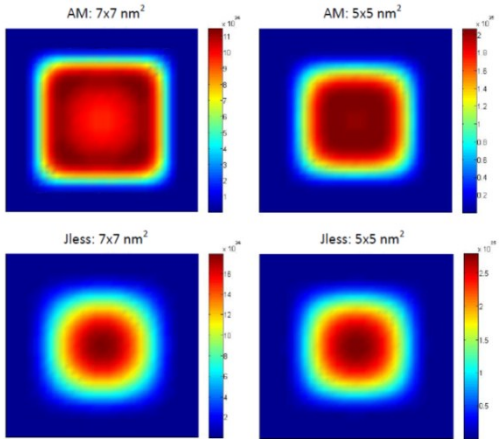


Figure 5.11 - Electron density at the middle of junctionless and AM devices for different cross-section dimensions (quantum simulations).

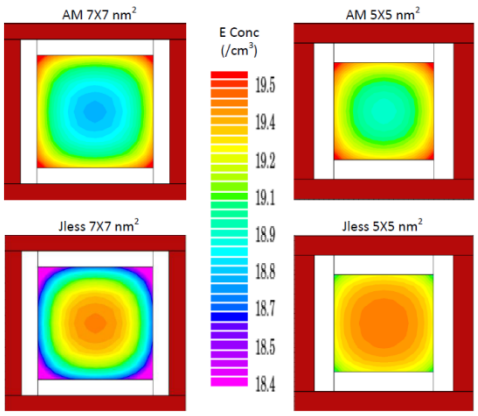


Figure 5.12 - Electron density at the middle of junctionless and AM devices for different cross-section dimensions (classical simulations).

5.4. Short-channel effects: JNTs vs IM devices

In this section, the subthreshold swing (SS), drain-induced barrier lowering (DIBL) and on/off current ratio of short channel JNTs are compared with those of conventional triple-gate IM MOSFETs [11].

5.4.1 Device structures and parameters

The 3D geometry of a triple-gate MOSFET and the doping profile of JNTs and IM devices are as indicated in Figure 5.1. The doping concentration in JNTs is 2×10^{19} cm^{-3}. In some JNTs, extra doping (10^{20} cm^{-3}) is used in the source and drain regions, but not within a distance L_{ov} from the gate edges. Abrupt source/drain junctions are used for the IM devices. The source/drain and channel doping concentrations in the IM devices are 1×10^{20} cm^{-3} and 5×10^{17} cm^{-3}, respectively.

All devices are designed to have the same threshold voltage of 0.5V, which is achieved by tuning the metal gate work function. The simulations are carried out using two carriers, the drift–diffusion model, doping concentration dependent and electric field dependent carrier mobility models. The Shockley-Read-Hall (SRH) recombination model is also included in the simulations to account for leakage currents.

5.4.2 Results and discussion

Figure 5.13 shows the I_{off}-I_{on} plots of JNTs and IM devices for L_{gate}=25nm and L_{gate}=10 nm. Additional doping (concentration N_D=10^{20} cm^{-3}) in the source/drain regions of the JNTs increases their current drive, due to lower source/drain resistances.

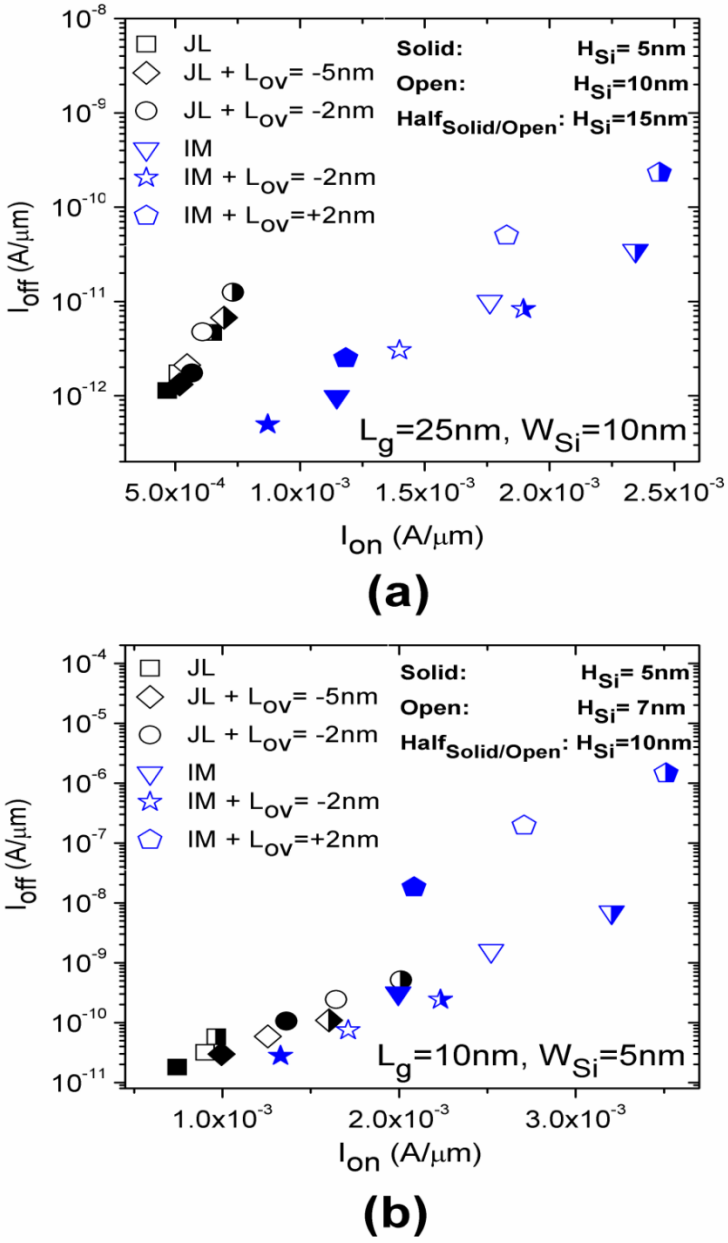


Figure 5.13 - I_{off}-I_{on} plots of JNTs and IM devices for (a) L_{gate}=25 nm and (b) L_{gate}=10 nm. The nanowire pitch is equal to $2\times W_{Si}$, such that the current in A/μm is equal to the current in a single nanowire times $1000/(2\times W_{Si})$. I_{on} is extracted at $V_{gs}=V_{ds}$ =1V while I_{off} is extracted at V_{gs}=0 V and V_{ds} =1 V. (L_{ov} is the gate overlap with the source and drain contact regions as shown in Figure 5.1)

For a 25 nm gate length and at the same off-current, IM devices have larger on-current than JNTs but when the gate length is decreased to 10 nm, the on/off current ratio becomes larger in the JNTs than in the IM MOSFETs. This conclusion holds for ideal IM devices (L_{ov}=0 nm) and for IM devices with gate overlap. IM devices with gate-underlap have a similar on/off current ratio to that of the JNTs. A gate overlap with source/drain regions in IM devices leads to a degraded on/off current

ratio, especially at very short gate lengths, as the effective gate length is shorter than the physical gate length. This confirms the importance of the JNT design as it does not suffer from dopant diffusion from source/drain regions into the channel region.

Figure 5.14 shows the DIBL of JNTs and IM devices for L_{gate}=25nm and L_{gate}=10nm. Any increase in the nanowire width or height, results in a degradation of the DIBL, due to a degradation of gate control over the channel charges. Furthermore, increasing the nanowire width for a fixed nanowire height yields a substantially larger degradation of DIBL than increasing the nanowire height for a fixed nanowire width, and this degradation is smaller in JNTs than in IM devices (Figure 5.14(b)). Moreover, JNTs have better DIBL at L_{gate}=10 nm than any IM device (with or without overlap). At L_{gate}=25 nm, JNTs have better DIBL than the ideal IM devices (L_{ov}=0 nm) and the IM devices with gate overlap (L_{ov}=2 nm). The reason for better DIBL in JNTs is that there is no space-charge region induced by source/drain junctions in the channel region, contrary to conventional IM devices. The IM devices with gate overlap have larger DIBL than all other devices as their effective gate length is smaller than the nominal gate length, and this results in much larger DIBL at L_{gate}=10 nm.

Figure 5.15 illustrates the SS of JNTs and IM devices for L_{gate}=25nm and L_{gate}=10nm. It is observed that JNTs have better SS at L_{gate}=10 nm than the conventional IM devices. Furthermore, as it was the case for the DIBL, increasing the nanowire height or nanowire width, degrades the SS in both type of devices. However, increasing the nanowire width at fixed nanowire height causes substantially more degradation of SS than increasing the nanowire height at fixed nanowire width in triple-gate nanowire devices.

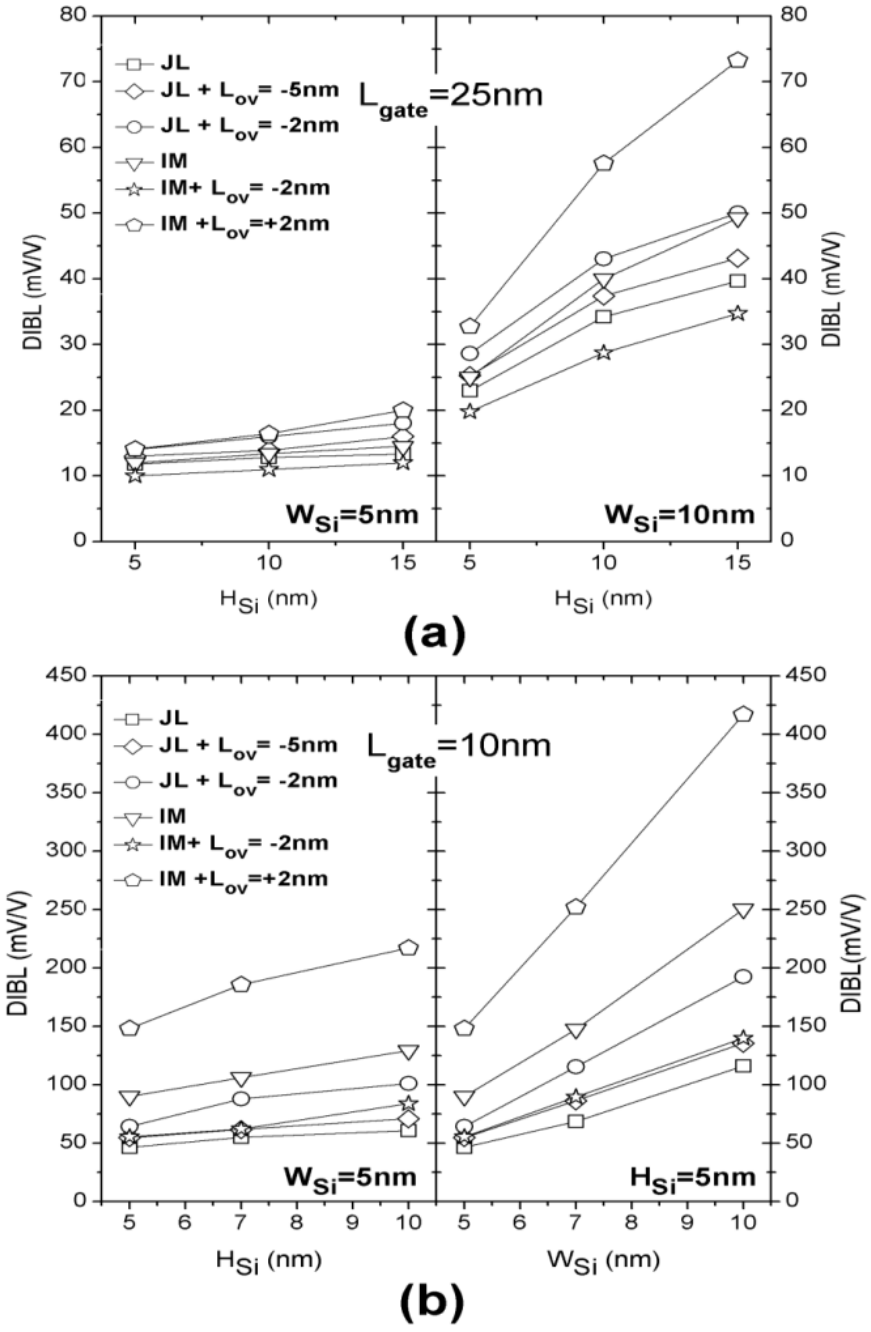


Figure 5.14 - DIBL in JNTs and IM devices for (a) L_{gate}=25 nm (b) L_{gate}=10 nm. DIBL is measured by the lateral shift of the transfer curves in the subthreshold regime between V_{ds}=50 mV and V_{ds}=1V divided by the drain voltage difference of the two curves (0.95V).

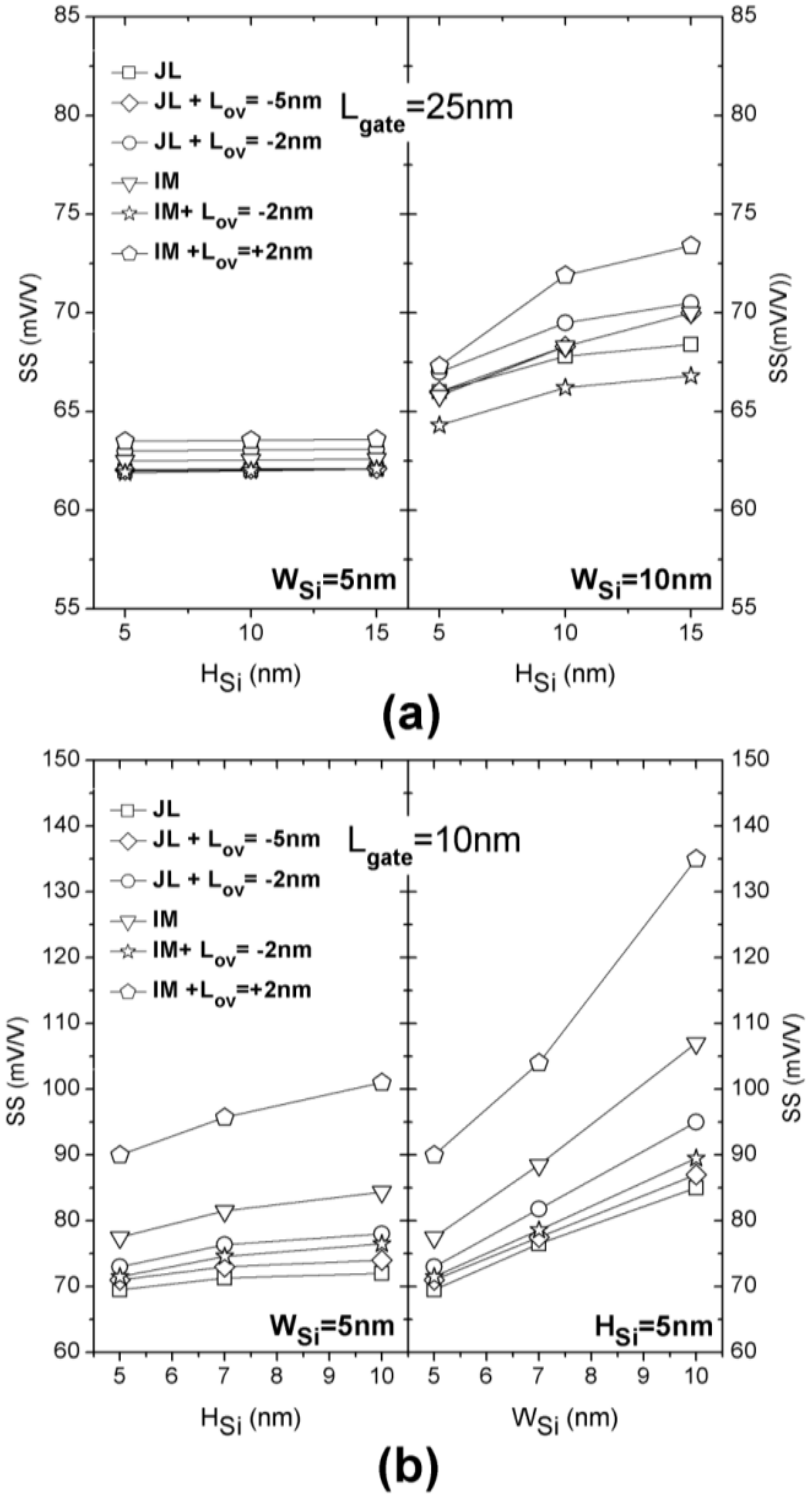


Figure 5.15 - Subthreshold swing of junctionless and IM devices for (a) L_{gate}=25 nm (b) L_{gate}=10 nm.

5.5. Short-channel effects: JNTs vs AM devices

In this section we investigate further the performance of short-channel devices based on junctionless GAA nanowires by simulating the I_{ds}-V_{gs} characteristics and extracting the subthreshold swing and DIBL. These are compared with the characteristics of AM GAA nanowire transistors. We also investigate the effect of channel orientation on I_{ds}-V_{gs} characteristics of junctionless GAA nanowire transistors by simulating and comparing the I_{ds}-V_{gs} characteristics of important nanowire orientations for different cross-section dimensions [12].

5.5.1 Device structures and parameters

Figures 5.9 and 5.10 show the 3D schematic and longitudinal cross-section view of devices, which we have used in our simulations. The source/drain and channel regions of the junctionless GAA nanowire transistors have n-type doping concentration of 1×10^{20} cm^{-3} and for AM GAA nanowire transistors, the source/drain regions have n-type doping concentration of 1×10^{20} cm^{-3} and the channel region has n-type doping concentration of 1×10^{16} cm^{-3} with no gate underlap/overlap. The simulations have been carried out for devices with different cross-section dimensions ranging from 3×3 nm^2 to 5×5 nm^2. As the device dimensions are very small and the channel of the AM device is low doped, the results obtained for the AM device in this section are very similar to the results obtained for inversion-mode (IM) device. To investigate the influence of channel orientation on the characteristics of junctionless GAA nanowire transistors we have simulated two important wire orientations, namely, <100> and <110> channels fabricated on wafer with (010) orientation. The gate length is 10 nm in all simulated devices. Simulations have been carried out using our three-dimensional quantum simulator which is based on the non-equilibrium Green's function (NEGF) formalism and the effective mass approximation. The DIBL is defined as the shift between the two I_{ds}-V_{gs} curves in linear regions at constant drain current of $I_d=10^{-10}$ (A) when increasing the drain voltage from 50 mV to 0.4V, divided by difference of these drain voltages (in mV/V).

5.5.2 Results and discussion

Figure 5.16 shows the I_{ds}-V_{gs} characteristics of junctionless and accumulation-mode GAA devices for different cross-section dimensions. From this figure, it can be

observed that the on-current of AM GAA transistors in devices with larger cross-section dimensions is higher than junctionless GAA transistors but in devices with smaller cross-section dimensions the current characteristics of both junctionless and AM GAA devices become very similar. Table 5.3 shows the comparison of subthreshold swing and DIBL values in junctionless and AM GAA nanowire transistors for different cross-section dimensions. As it can be seen in this table, the subthreshold swing is very similar in both devices for simulated cross-section dimensions and the DIBL is slightly better for junctionless GAA devices compared to AM GAA devices. Also it can be seen that in both cases the devices with larger cross-section dimensions have larger subthreshold swing and DIBL compared to the smaller ones and this is due to short-channel effects in these devices. Since the gate length for all simulated devices is 10 nm the impact of field penetration from drain side in to the channel of the device with 5×5 nm^2 cross-sections have more influence on gate controllability over the channel potential compared to devices with 3×3 nm^2 cross-sections.

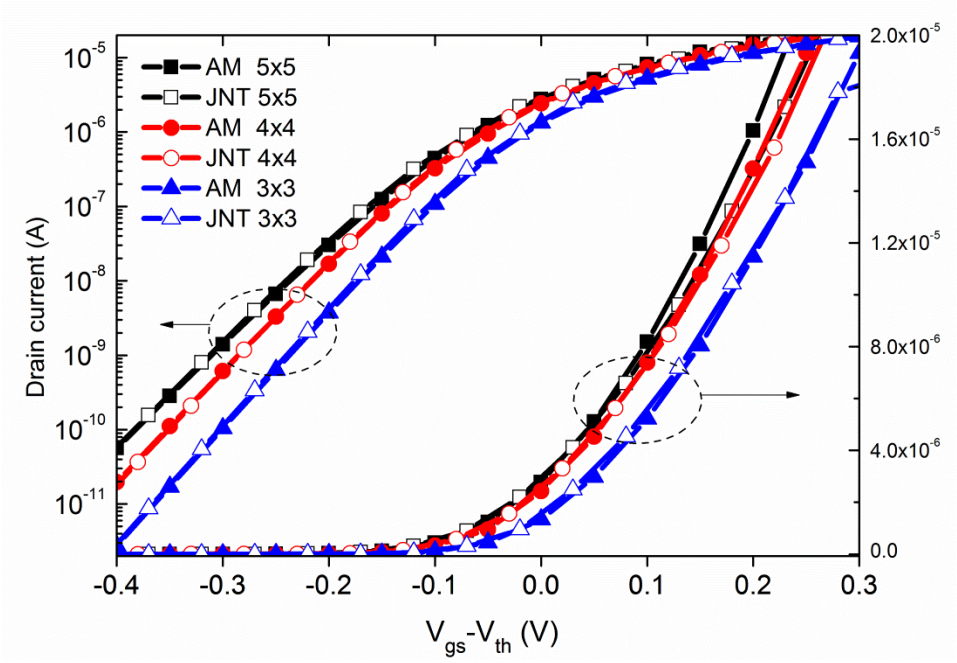


Figure 5.16 - Comparison of I_{ds}-V_{gs} characteristics in junctionless and accumulation-mode GAA nanowire transistors for different cross-section dimensions (V_{ds}=0.4V).

Table 5.3 - Comparison of subthreshold swing and DIBL in junctionless and AM GAA nanowire transistors for different cross-sections. (L_{gate} = 10 nm)

		3×3 nm^2	4×4 nm^2	5×5 nm^2
AM	DIBL (mV/V)	35	57	85
	SS (mV/dec)	64	68	72
JNT	DIBL (mV/V)	32	52.5	81
	SS (mV/dec)	63	67	71

It can also be seen in Figure 5.17 that the channel potential barrier in subthreshold region, in the devices with smaller cross-section dimensions decreases faster than in the larger ones, and as a result the subthreshold swing will be better in these devices compared with devices with larger cross-section dimensions.

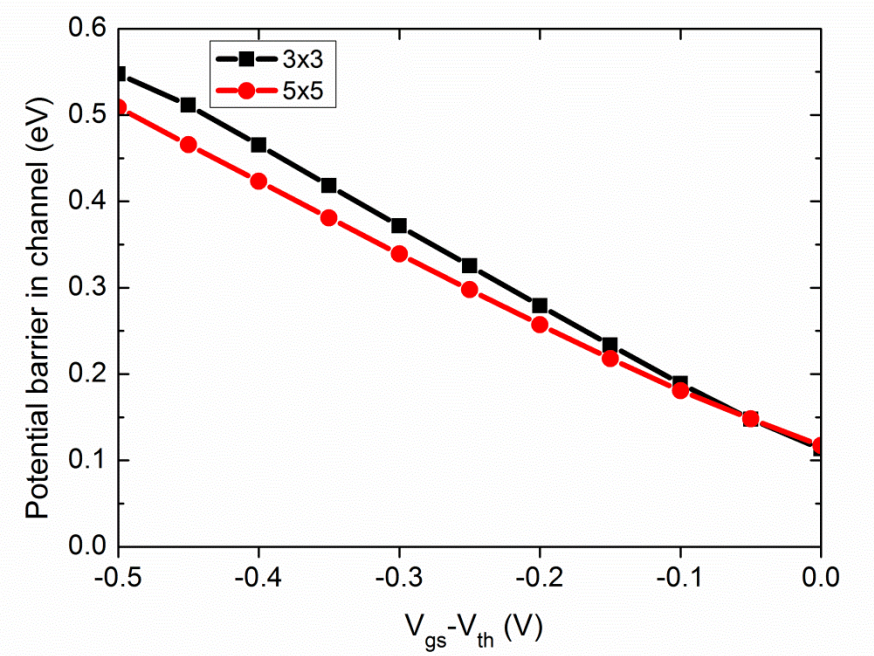


Figure 5.17 - Potential barrier in the channel of the junctionless GAA nanowire transistor for different cross-section dimensions in the subthreshold region.

To investigate the effect of channel orientation on I_{ds}-V_{gs} characteristics of junctionless GAA nanowire transistors, we have simulated and compared the I_{ds}-V_{gs} characteristics for two important wire orientations, namely, the <100> and <110> crystallographic directions. Table 5.4 shows the effective-masses and subband degeneracies which have been used in our simulations for <100> and <110> oriented wires on (010) wafer. Figure 5.18 shows the I_{ds}-V_{gs} characteristics of junctionless

GAA nanowire transistors for different cross-section dimensions ranging from 3×3 nm^2 to 5×5 nm^2. As it can be seen in this figure the <100>-oriented wire has more on-current compared to the <110> channel.

Table 5.4 - Effective masses and subband degeneracies of Δ valleys for two important semiconductor nanowire orientations. (Wafer orientation is (010), m_0 is free electron mass)

Wire orientation		*Degeneracy*	m_x/m_0	m_y/m_0	m_z/m_0
<100>	Δ_1	2	0.98	0.19	0.19
	Δ_2	2	0.19	0.98	0.19
	Δ_3	2	0.19	0.19	0.98
<110>	Δ_1	2	0.19	0.98	0.19
	Δ_2	2	0.585	0.3183	0.19
	Δ_3	2	0.585	0.19	0. 3183

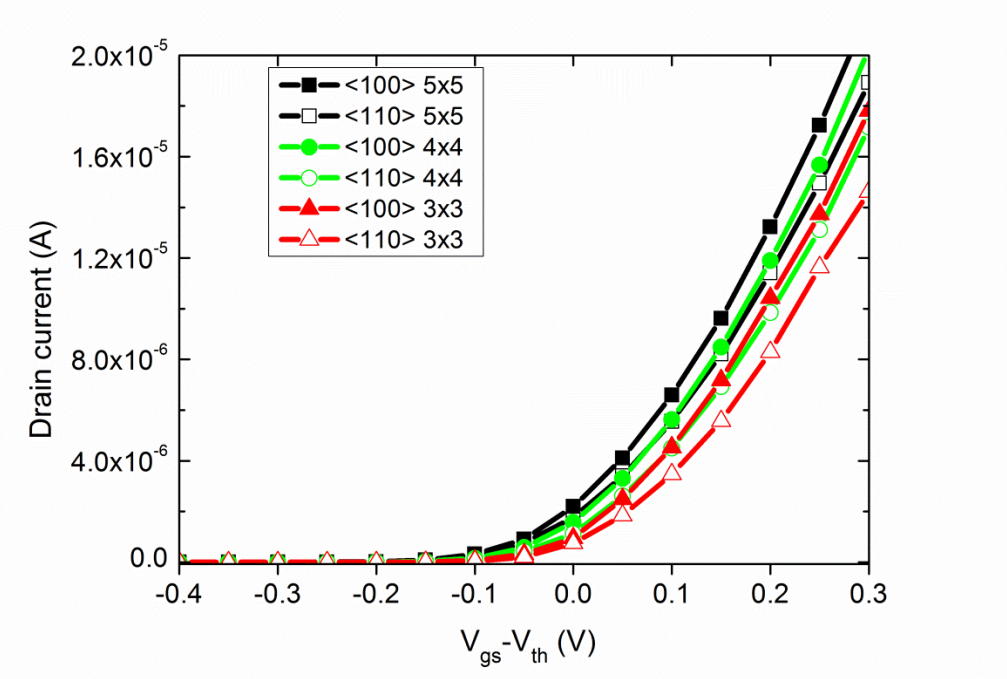


Figure 5.18 - I-V characteristics of junctionless GAA nanowire transistors for <100> and <110>channels (wafer orientation is (010), V_{ds} =0.4V).

Figures 5.19 and 5.20 show the contribution of each of the Δ valleys to the total current in <100> and <110>-oriented wires, respectively, for junctionless GAA nanowire transistors with 5×5 nm^2 cross-section dimensions. As it can be seen in these figures, the Δ2 and Δ3 valleys in the <100> wire-orientation and Δ1 valley in the <110> channel have the most contributions to the total currents of the devices.

This can be due to the values of confinement and transport effective masses and the arrangement of the subbands which can be seen in Figures 5.21 to 5.24. As it can be seen in these figures the distance between subbands is less in these valleys compared to the other valleys and more subbands contribute to the value of the total current.

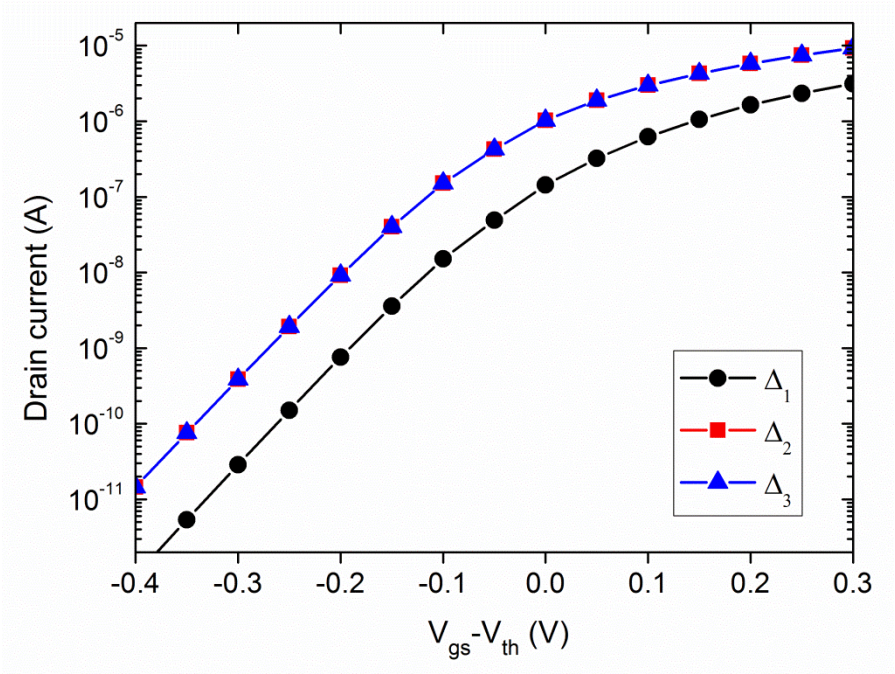


Figure 5.19 - Contribution of different Δ valleys in total current of junctionless GAA nanowire transistor with cross-section of 5×5 nm^2 and <100>-oriented wire (V_{ds}=0.4V, wafer orientation is (010)).

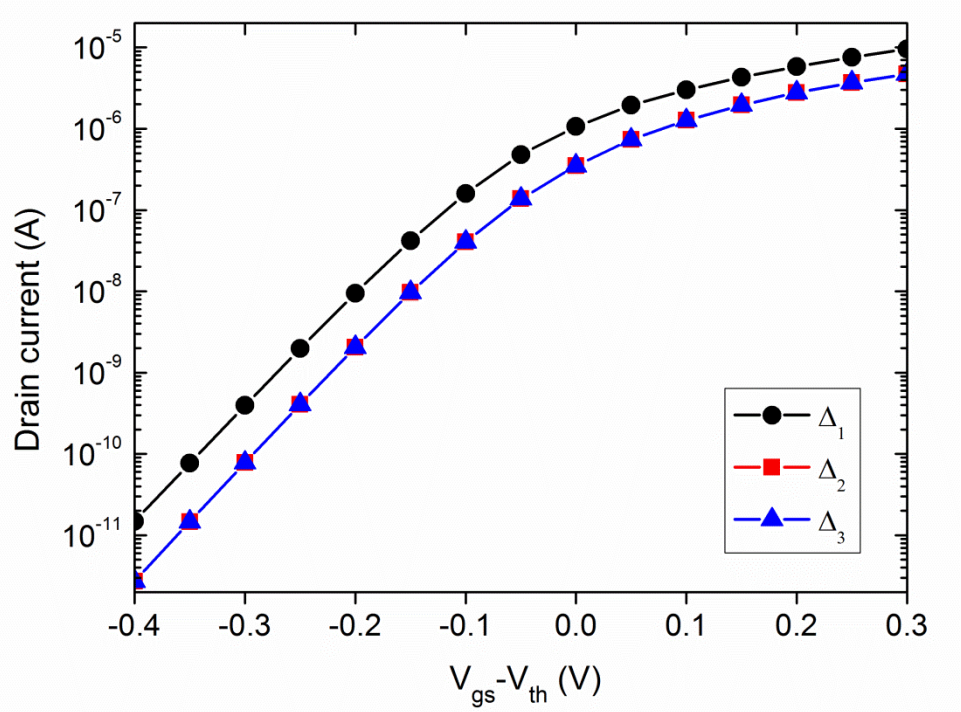


Figure 5.20 - Contribution of different Δ valleys in total current of junctionless GAA nanowire transistor with cross-section of 5×5 nm^2 and <110>-oriented wire (V_{ds}=0.4V, wafer orientation is (010)).

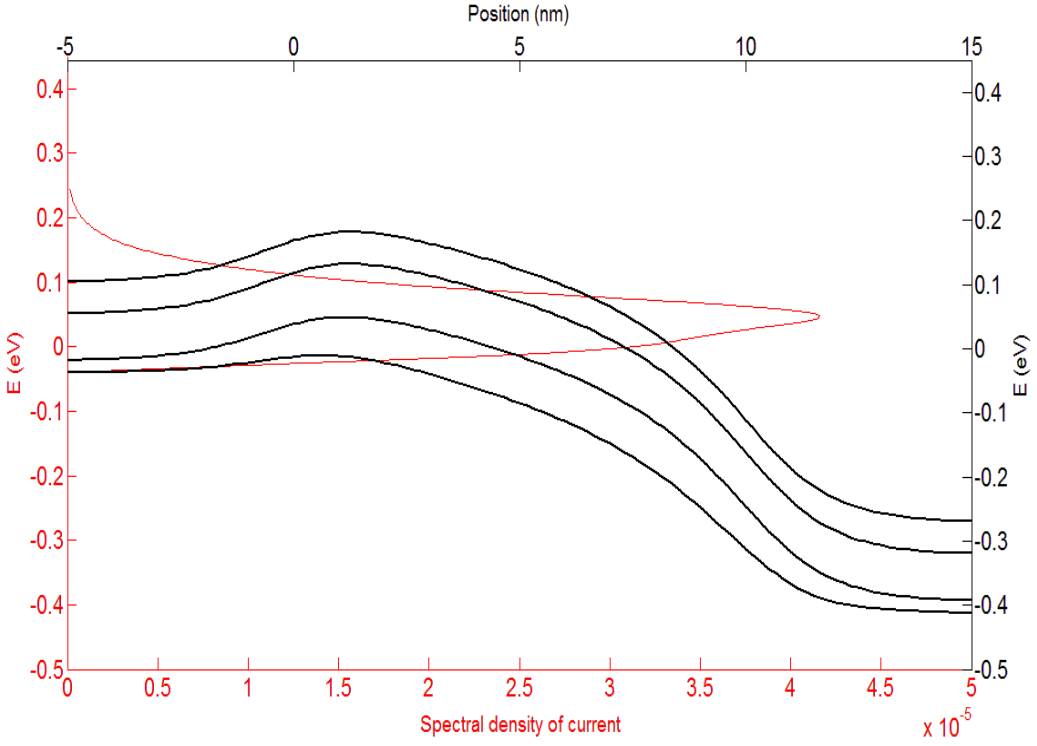


Figure 5.21 - Four lowest conduction subbands (black) and spectral density of current (red) at V_{gs}-V_{th} =0.3V for Δ_2 and Δ_3 valleys of <100> oriented junctionless nanowire transistor. Wafer orientation is (010), V_{ds}=0.4V, cross-section is 5×5 nm^2).

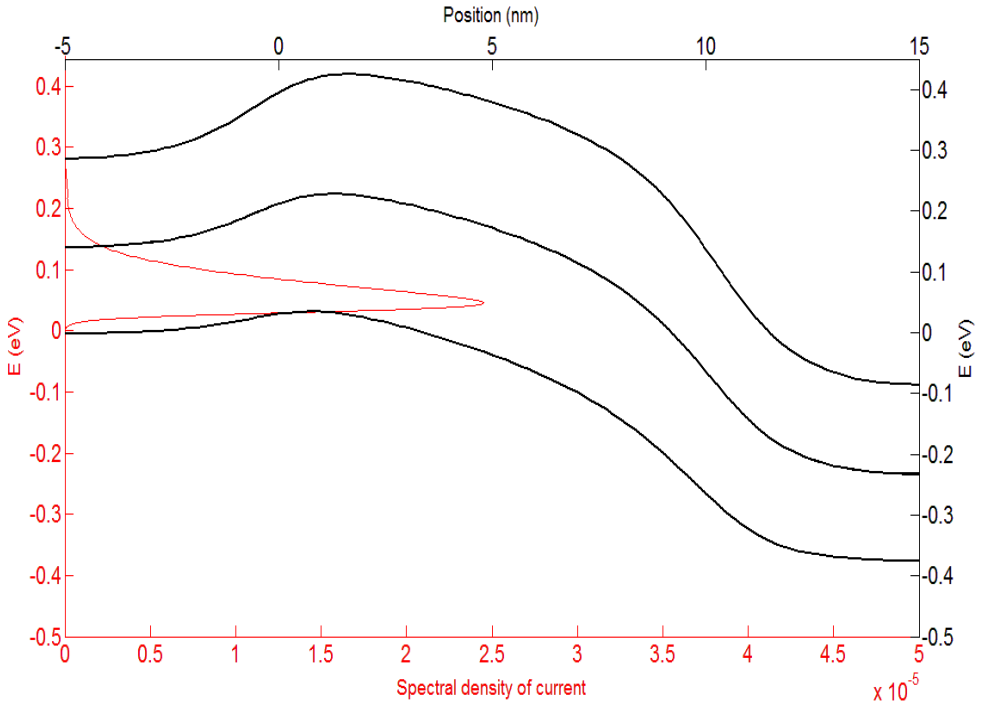


Figure 5.22 - Four lowest conduction (black) and spectral density of current (red) at V_{gs}-V_{th} =0.3V for Δ_1 valley of <100> oriented junctionless nanowire transistor. Wafer orientation is (010), V_{ds}=0.4V, cross-section is 5×5 nm^2.

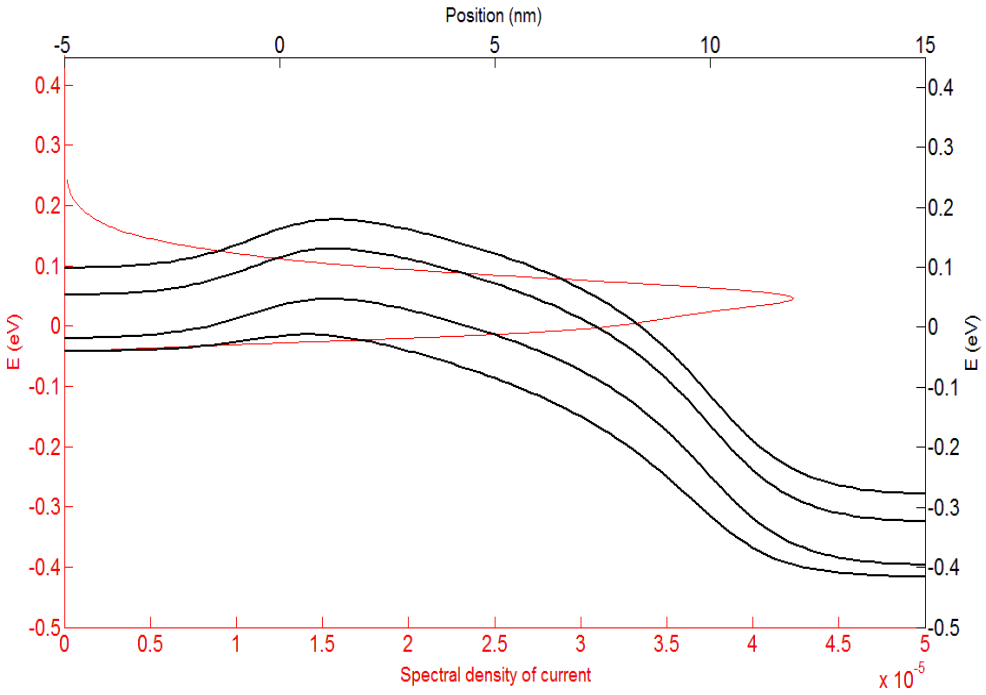


Figure 5.23 - Four lowest conduction (black) and spectral density of current (red) at V_{gs}-V_{th} =0.3V for Δ_1 valley of <110> oriented junctionless nanowire transistor. Wafer orientation is (010), V_{ds}=0.4V, cross-section is 5×5 nm^2.

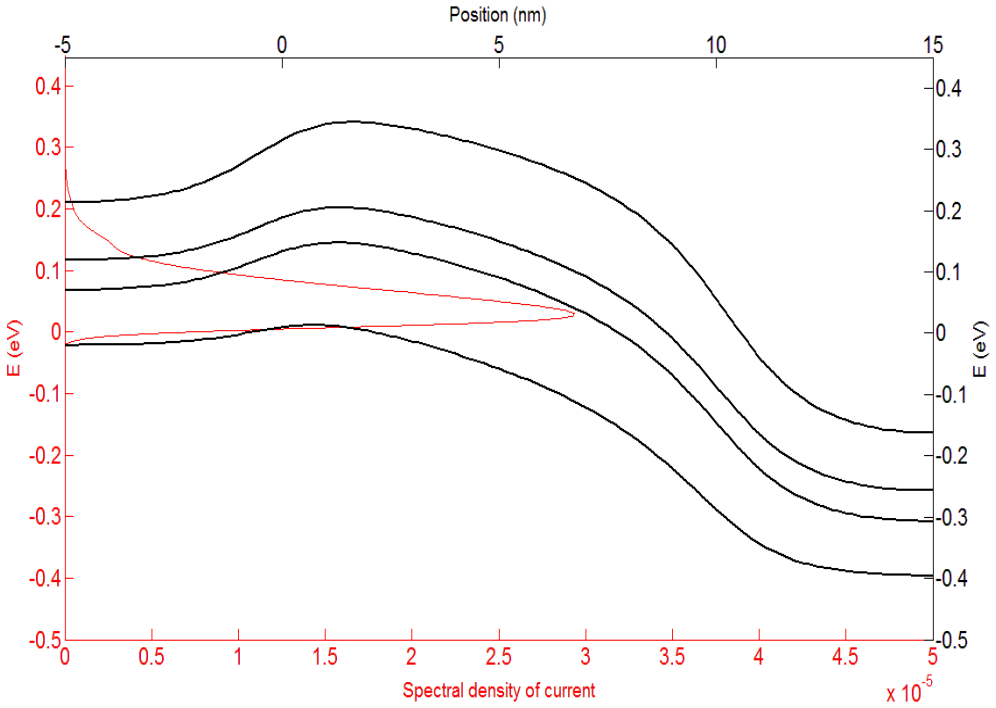


Figure 5.24 - Four lowest conduction subbands (black) and spectral density of current (red) at V_{gs}-V_{th} =0.3V for Δ_2 and Δ_3 valleys of <110> oriented junctionless nanowire transistor Wafer orientation is (010), V_{ds}=0.4V, cross-section is 5×5 nm^2.

5.6. Conclusion

Our simulation results show that the Intrinsic gate delay in JNTs with gate length of 22 nm down to 15 nm with doping concentration from 5×10^{18} cm^{-3} up to 2×10^{19} cm^{-3} is higher than those of IM devices with the same gate lengths due to smaller on-state current of JNTs compared to IM devices. On the other hand, switching energy is lower in JNTs compared to IM devices due to the lower gate capacitances in JNTs. And as a result, energy-delay product of JNTs and IM devices is almost identical for simulated devices. We also show that using additional doping concentration in the source and drain contact regions of JNTs, considering an optimized distance from gate edges, leads to further decrease of the intrinsic gate delay and energy-delay product. These results confirm the findings of Cho *et al.* regarding high-frequency performance of junctionless transistors [13].

Furthermore, we have simulated and compared the switching time of junctionless and AM gate-all-around nanowire transistors using quantum and classical simulators. We found that classical simulations are not valid for small dimension devices and may lead to wrong results in calculating of the switching speed in small dimension devices. We find that in larger devices, switching time of AM devices is

lower than in junctionless devices but both devices have a similar switching time when they have small dimensions.

JNTs exhibit better short-channel effect control and a larger on/off current ratio than IM triple-gate devices for a gate length equal to 10 nm. Increasing the height of the silicon nanowire at fixed nanowire width as well as using additional doping concentration in the source/drain regions of JNTs, considering an optimized gate-underlap, increases the drive current with limited loss of control on short channel effects in JNTs.

Finally, by simulating and comparing I_{ds}-V_{gs} characteristics, subthreshold swing and DIBL of short-channel junctionless and accumulation-mode (AM) gate-all-around (GAA) nanowire transistors, we found that in devices with larger cross-section dimensions, the AM device has more on-current but the current characteristics become very similar in devices with smaller cross-section dimensions. In the simulated devices, subthreshold swing is very similar in both junctionless and AM GAA devices while the DIBL is slightly better for junctionless devices. We also investigate the influence of wire orientation on I_{ds}-V_{gs} characteristics of junctionless nanowire transistors by simulating the I_{ds}-V_{gs} characteristics of <100> and <110> oriented wires on (010) wafer. We found that for the simulated devices, due to the values of confinement and transport effective-masses and arrangement of subbands , the on-current is more in <100>-oriented junctionless GAA nanowire transistors compared with <110>-oriented juncitonless GAA nanowire transistors.

References

[1] C. F. Nieh, K. C. Ku, C. H. Chen, H. Chang, L. T. Wang, L. P. Huang*, et al.*, "Millisecond Anneal and Short-Channel Effect Control in Si CMOS Transistor Performance," *Electron Device Letters, IEEE,* vol. 27, pp. 969-971, 2006.

[2] P. Garg, J. Wu, and S. J. Fonash, "Accumulation-Mode MOSFET (AMOSFETs) Fabricated on Silicon Nanowires and Polysilicon Thin Films," *ECS Transactions,* vol. 28, pp. 43-49, October 8, 2010 2010.

[3] M. Masahara, K. Endo, Y. X. Liu, T. Matsukawa, S. O'Uchi, K. Ishii*, et al.*, "Demonstration and analysis of accumulation-mode double-gate metal-oxide-semiconductor field-effect transistor," *Japanese Journal of Applied Physics Part 1-*

Regular Papers Brief Communications & Review Papers, vol. 45, pp. 3079-3083, Apr 2006.

[4] E. Rauly, B. Iniguez, D. Flandre, and C. Raynaud, "Investigation of single and double gate SOI MOSFETs in Accumulation Mode for enhanced performances and reduced technological drawbacks," in *Solid-State Device Research Conference, 2000. Proceeding of the 30th European*, 2000, pp. 540-543.

[5] J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain*, et al.*, "Nanowire transistors without junctions," *Nat Nano,* vol. 5, pp. 225-229, 2010.

[6] J.-P. Colinge, A. Kranti, R. Yan, C. Lee, I. Ferain, R. Yu*, et al.*, "Junctionless Nanowire Transistor (JNT): Properties and design guidelines," *Solid-State Electronics,* 2011.

[7] P. Razavi, I. Ferain, S. Das, Y. Ran, N. D. Akhavan, and J. Colinge, "Intrinsic gate delay and energy-delay product in junctionless nanowire transistors," in *Ultimate Integration on Silicon (ULIS), 2012 13th International Conference on*, 2012, pp. 125-128.

[8] "Device User Guide," C-2009.06 ed. Mountain View, CA: Synopsys, 2009.

[9] P. Razavi, R. Yan, I. Ferain, N. Dehdashti Akhavan, R. Yu, and J.-P. Colinge, "Switching speed in junctionless and accumulation-mode gate-all-around nanowire transistors," in *EUROSOI 2011; VII Workshop of the Thematic Network on Silicon On Insulator Technology; Devices and Circuits*, 2011, pp. 43-44.

[10] http://www.silvaco.com.

[11] P. Razavi, N. D. Akhavan., R. Yu, G. Fagas, I. Ferain, and J.-P. Colinge, "Investigation of Short-Channel Effects in Junctionless Nanowire Transistors," in *Solid State Devices and Materials (SSDM), the 2011 International Conference on*, 2011, pp. 106-107.

[12] P. Razavi, G. Fagas, I. Ferain, N. Dehdashti Akhavan, R. Yu, and J. P. Colinge, "Performance investigation of short-channel junctionless multigate transistors," in *Ultimate Integration on Silicon (ULIS), 2011 12th International Conference on*, 2011, pp. 1-4.

[13] C. Seongjae, K. Kyung Rok, P. Byung-Gook, and K. In Man, "RF Performance and Small-Signal Parameter Extraction of Junctionless Silicon Nanowire MOSFETs," *Electron Devices, IEEE Transactions on,* vol. 58, pp. 1388-1396, 2011.

Chapter 6 : Influence of Germanium Channel Properties on Performance of Nanowire Transistors

6.1. Introduction

According to the international technology roadmap of semiconductors (ITRS) metal-oxide-semiconductor field-effect transistors (MOSFETs) are shrinking rapidly and will reach sub-10 nm regime within the next few years [1]. Scaling device dimensions gives rise to short-channel effects (SCEs) which is caused by a less electrostatic control of the channel by the gate. The classical SCEs are an increase of the subthreshold swing (SS), a lowering of the threshold voltage (V_{th}) when gate length is reduced, and the drain-induced barrier lowering (DIBL) effect, which manifests itself as a lowering of the threshold voltage when the drain voltage (V_d) is increased. All these effects degrade device performance. Reducing short-channel effects is important for being able to scale transistors to decananometer dimensions. To this end, various device structures and materials have been proposed.

Multiple-gate structures, thin-body silicon-on-insulator (SOI) devices and high-κ gate dielectrics are being used to enhance gate control over the channel [2, 3]. From a design perspective, devices that resemble nanowires with a very small cross-section are very promising due to their excellent characteristics and a potential for high-density integration. On the materials side, channels made of germanium, carbon nanotubes and compound semiconductors are being investigated because of high carrier mobilities. Their science and technology have also attracted considerable attention as they have shown to yield enhanced drive current and improvement of electrical performances in nanotransistors [4-6].

The formation of ultra-sharp source and drain junctions is another challenge of modern devices in addition to the issue of controlling short-channel effects. For example, at very short channel length, extremely high doping concentration gradients are needed to form the p-n junctions. This results in increasing the cost and the complexity of the fabrication process. As stated in the previous chapters, the fabrication process of JNTs is much simpler than in conventional CMOS devices and they can provide full CMOS compatibility. The main key in the fabrication of JNTs

is that the channel region has to be narrow and thin enough to allow for full depletion of carriers to turn off the device [7].

The conduction mechanism in JNTs is based on the propagation of most carriers through the bulk of the channel rather than in surface channel [8] and atomic-scale simulations have confirmed the scalability of JNTs down to sub-5 nm dimensions [9]. Several publications on the characterization of JNTs and comparison of these devices with conventional CMOS devices can be found in the literature [10-18]. Germanium IM devices have been previously investigated [19, 20]. In this chapter we report the performance comparison of germanium and silicon JNTs using quantum mechanical study [21].

In chapter 4, we explored the effects of design by looking at multiple-gate device architecture and SOI technology. Here, using three-dimensional ballistic quantum mechanical simulations we comprehensively investigate the effect of different channel materials and orientation, namely, <100>- or <110>-oriented Ge and Si wires on a (010)-wafer, on the short channel characteristics of n-channel JNTs and compare them with the characteristics of conventional IM nanowire-based FETs. This analysis can explain the physical origin of the superior short channel behavior of JNTs compared with IM devices and identify the materials properties that affect device performance.

In the next section the device structures and parameters which have been used in the simulations are discussed. Section 6.3 introduces the simulation methodology followed by the presentation of the results in Section 6.4. We conclude with few summary remarks.

6.2. Device structures and parameters

Here we consider n-type Si and Ge nanowires with different channel orientations of <100> and <110> which are made on (010)-oriented wafers. Figures 6.1 (a) and (b) show a schematic view of gate-all-around (GAA) junctionless and inversion-mode nanowire transistors with a square cross-section as well as the doping profile in the longitudinal direction for these devices. The cross-sections are assumed to be square and have dimensions of $W_{Semicon} = T_{Semicon}$ where $T_{Semicon}$ ranges from 6 nm down to 4 nm. Gate lengths range from 12 nm to 8 nm and uniform doping concentrations throughout the channel and source/drain regions of the devices have

been used. We assume the abrupt source and drain junctions in IM and doping concentrations in the source/drain regions and channel are 1×10^{20} cm^{-3} and 1×10^{15} cm^{-3}, respectively. The doping concentration in source, drain and channel of JNTs is 1×10^{19} cm^{-3}. The effective oxide thickness (EOT) is equal to 1 nm for all devices. The supply voltage (V_{dd}) is equal to 0.65 V and by tuning the gate workfunction, all transistors are designed to have the same off-current of 10 pA/µm which is suitable for low standby power technologies [1].

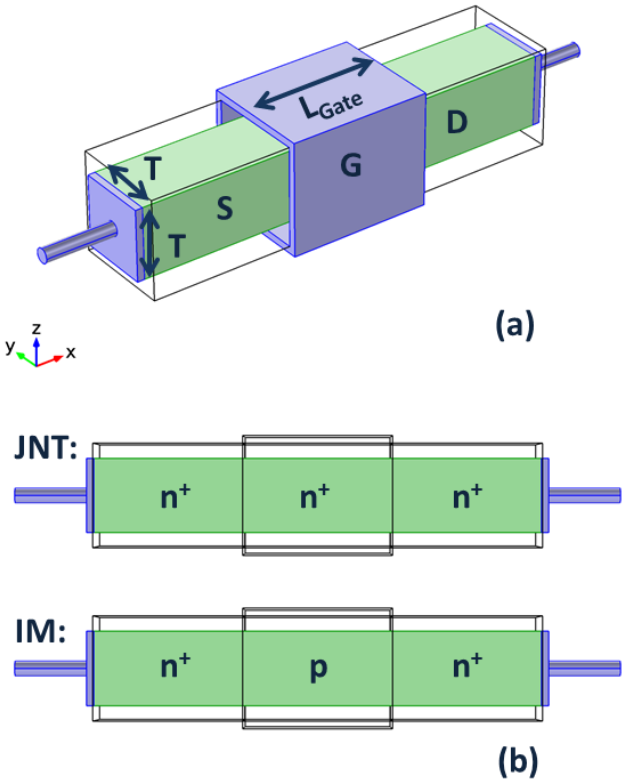


Figure 6.6.1 - (a) Bird eye's view of a gate-all-around nanowire transistor and (b) doping profile in the longitudinal direction in junctionless and inversion-mode devices.

The band alignments of the various direct and indirect gaps of Si and Ge at room temperature are shown in Figure 6.2. In bulk semiconductor devices, valleys which are lower in energy have the largest contribution to transport. As it can be seen in this figure, in bulk silicon the X-valleys are energetically much lower than the other valleys and, as a result, most of the electrons in the conduction band populate the X-valleys; other valleys can be ignored in the transport simulations. In small dimension nanowires, however, quantum confinement becomes important and effective masses perpendicular to the wire axis play an important role in determining the valleys that

form the energetically lowest subbands. Table 6.1 shows the general expressions for effective masses used in the simulations for Si and Ge nanowires with different crystal orientations. The transverse and longitudinal effective masses used for the X- and L- valleys in Si and Ge are shown in Table 6.2. The Γ-valley in Ge is non-degenerate and has an isotropic effective mass ($0.038\times m_0$ where m_0 is the free electron mass). Using this band structures and effective masses, we investigate the effect of wire materials and orientations on the subthreshold swing, DIBL, I_{on}/I_{off} ratio and source-to-drain tunneling in JNTs and compared them with IM devices.

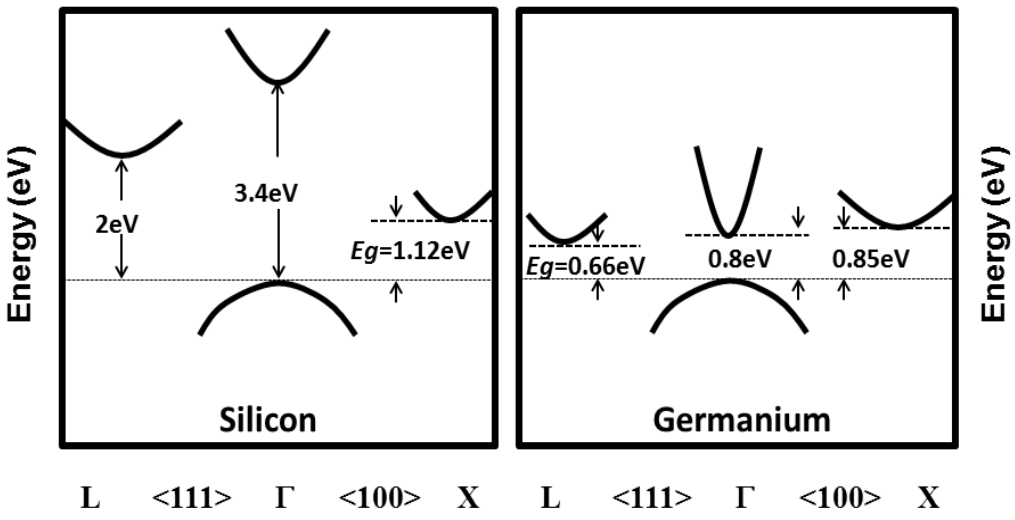


Figure 6.6.2 - The values of direct and indirect gaps of Si and Ge devices (at Temp=300K) used in our simulations.

The band-to-band tunneling (BTBT) has not been considered in our simulations. Note that due to the quantization effect the band gap in our devices becomes even larger than bulk devices as the channel thickness gets smaller and the BTBT rate decreases [22]. Using larger supply voltages could increase the leakage current and degrade the off-state performance of the devices [23]. A brief introduction of the simulation method that takes into account the effective masses for arbitrarily oriented wires is discussed in the next section.

Table 6.1 – General expressions of effective masses and subband degeneracy for <100>- and <110>- oriented semiconductor nanowires on the (010)-oriented wafer.

Wire orientation	Valley	m_{yy}	m_{zz}	m_{yz}	m_x	*Degeneracy*
<100>	X	m_t	m_t	*inf*	m_l	2
		m_l	m_t	*inf*	m_t	2
		m_t	m_l	*inf*	m_t	2
	L	$\frac{3m_l m_t}{m_t + 2m_l}$	$\frac{3m_l m_t}{m_t + 2m_l}$	$\frac{3m_l m_t}{m_t - m_l}$	$\frac{2m_t + m_l}{3}$	2
		$\frac{3m_l m_t}{m_t + 2m_l}$	$\frac{3m_l m_t}{m_t + 2m_l}$	$\frac{3m_l m_t}{m_l - m_t}$	$\frac{2m_t + m_l}{3}$	2
<110>	X	m_l	m_t	*inf*	m_t	2
		$\frac{2m_l m_t}{m_t + m_l}$	m_t	*inf*	$\frac{m_t + m_l}{2}$	2
		m_t	$\frac{2m_l m_t}{m_t + m_l}$	*inf*	$\frac{m_t + m_l}{2}$	2
	L	$\frac{3m_l m_t}{m_t + 2m_l}$	$\frac{3m_l m_t}{2m_t + m_l}$	$\frac{3m_l m_t}{\sqrt{2}(m_t - m_{l)}}$	m_t	1
		$\frac{3m_l m_t}{m_t + 2m_l}$	$\frac{3m_l m_t}{2m_t + m_l}$	$\frac{3m_l m_t}{\sqrt{2}(m_l - m_{t)}}$	m_t	1
		$\frac{3m_l m_t}{m_t + 2m_l}$	m_t	*inf*	$\frac{m_t + 2m_l}{3}$	2

Table 6.2 – Values of transverse and longitudinal effective masses for the X- and L-valleys in bulk Si and Ge which have been used in our simulations.

	valley	m_l/m_0	m_t/m_0
Si	X	0.98	0.19
	L	1.7	0.12
Ge	X	0.95	0.2
	L	1.64	0.082

6.3. Simulation methodology

We have used our fully self-consistent 3D quantum mechanical simulator that uses the effective-mass approximation. Calculation of band structures in Si and Ge nanowires using tight-binding simulations have shown that for devices with a cross-section larger than 4nm, the change in curvature of electronic bands along transport directions is negligible and as a result the parabolic approximation is valid and accurate [20, 24]. The simulation procedure was discussed extensively in chapter 2. Here, we repeat the main steps to complete a generalization that allows the correct treatment of the kinetic energy in arbitrarily oriented nanowires using the effective mass tensor.

The quantum transport is calculated using the Non-Equilibrium Green's Functions (NEGF) formalism [25] expressed in the mode space (MS) approach [26]. The 3D Poisson equation and 3D Schrödinger equation with open boundary conditions are solved self-consistently. COMSOL Multiphysics [27] is used to solve the Poisson equation and obtain the electrostatic potential in the device. Using MS approach the quantum confinement and transport can be separated to solve the Schrödinger equation in a computationally efficient manner. As a result of this procedure, the 3D Schrödinger equation is decomposed into: (I) a 2D Schrödinger equation which is solved with closed boundary condition in different cross-sections of the nanowire to obtain the wave functions and the electron subbands along the device, and (II) a 1D transport equation which is solved using NEGF formalism along source-drain axis to obtain the electron charge density.

The 3D full stationary Schrödinger equation is given by:

$$H_{3D}\Psi(x,y,z) = E\Psi(x,y,z) \qquad 6.1$$

where H_{3D} is the 3D device Hamiltonian, E is energy and $\Psi(x,y,z)$ is the 3D wavefunction. In arbitrarily oriented wires the inverse effective-mass tensor have non-diagonal terms which are due to misalignment of the iso-energy surfaces of the conduction bands with the device coordinate system. Assuming an ellipsoidal parabolic energy band, H_{3D} is defined as:

$$H_{3D} = -\frac{\hbar^2}{2}\left(\frac{1}{m_{xx}}\frac{\partial^2}{\partial x^2} + \frac{1}{m_{yy}}\frac{\partial^2}{\partial y^2} + \frac{1}{m_{zz}}\frac{\partial^2}{\partial z^2} + \frac{2}{m_{xy}}\frac{\partial^2}{\partial x \partial y} + \frac{2}{m_{yz}}\frac{\partial^2}{\partial y \partial z} + \frac{2}{m_{xz}}\frac{\partial^2}{\partial x \partial z}\right) + V(x,y,z) \quad 6.2$$

where $1/m_{ij}$ is the reciprocal effective mass tensor (EMT) in the device coordinate system, and $V(x,y,z)$ is the potential energy. Solving this equation is a computational challenge. By decoupling the associated energies along the confinement and transport directions, one can avoid having to solve the full 3D equation. We use the method extensively described in [28] to do this. By assuming constant confinement along the transport (x) direction, the 3D wavefunction can be written as follows:

$$\Psi(x,y,z) = \phi(y,z)e^{ik_x x} \quad 6.3$$

Where ϕ and k_x are the wavefunction in the cross-section and the wavevector in the transport direction, respectively. By writing the transverse part of the wavefunction as follows:

$$\phi(y,z) = \varphi(y,z)e^{ik_x(\alpha y + \beta z)} \quad 6.4$$

and choosing parameters α and β in such a way to cancel the first order derivatives with respect to y and z in the 3D Schrödinger equation, we obtain the following equation:

$$-\frac{\hbar^2}{2}\left(\frac{1}{m_{yy}}\frac{\partial^2\varphi}{\partial y^2} + \frac{1}{m_{zz}}\frac{\partial^2\varphi}{\partial z^2} + \frac{2}{m_{yz}}\frac{\partial^2\varphi}{\partial y \partial z}\right) + \left(\frac{\hbar^2 k_x^2}{2m_x} + V(y,z) - E\right)\varphi = 0 \quad 6.5$$

where m_x is effective mass in transport direction, $1/m_{ij}$ is the reciprocal EMT in the device coordinate system, E is the charge-carrier energy and V is the confinement potential energy. In this equation the associated energies in the confined cross-

section and in the channel direction *(x)* are decoupled, which allows one to use the NEGF formalism [25] expressed within the MS approach [26]. The 2D Schrödinger equation to be solved for the confined cross-section at each point along the transport direction *(x)* to yield the electron subbands energy levels and modes reads:

$$H_{2\mathrm{D}}\Psi^{\mathrm{n}}(y,z;x_i) = E_{sub}^{n}\Psi^{\mathrm{n}}(y,z;x_i) \qquad 6.6$$

where

$$H_{2D} = -\frac{\hbar^2}{2}\left(\frac{1}{m_{yy}}\frac{\partial^2}{\partial y^2} + \frac{1}{m_{zz}}\frac{\partial^2}{\partial z^2} + \frac{2}{m_{yz}}\frac{\partial^2}{\partial y \partial z}\right) + V(y,z) \qquad 6.7$$

where E_{sub}^{n} is the subband energy level and $\Psi^{\mathrm{n}}(y,z;x_i)$ is the corresponding transversal wave function at each slice $x=x_i$. The non-diagonal term *in* the effective mass tensor ($1/m_{yz}$) couples the transverse directions. The Figure 6.3 shows the influence of this non-diagonal term.

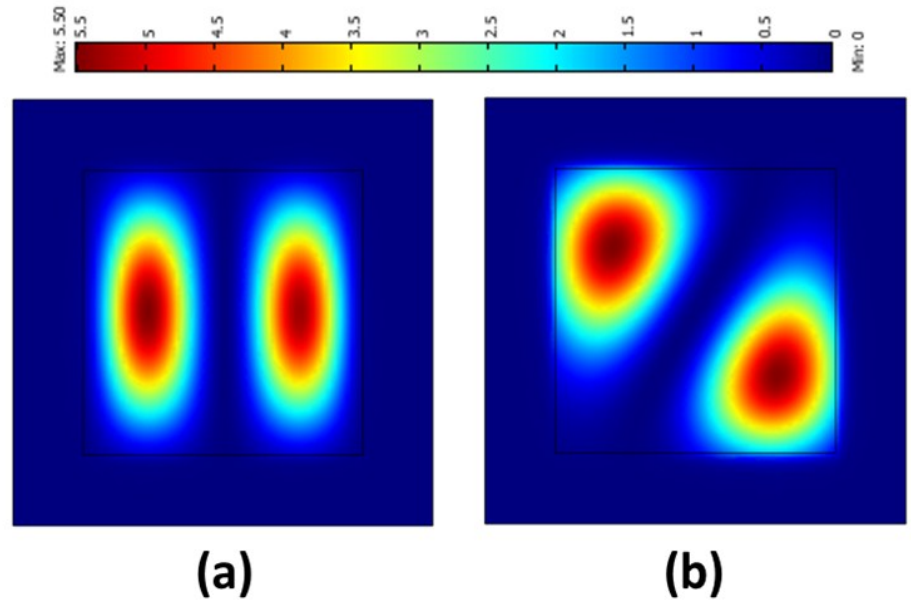


Figure 6.3 - Square modulus of the 2nd wavefunctions of the (a) X-valley and (b) L-valley of a Ge nanowire.

Finally, using the mode-space device Hamiltonian and assuming ballistic transport, the retarded Green's function (G) of the active device is calculated using:

$$G = [EI - H - \Sigma_1 - \Sigma_2]^{-1} \qquad 6.8$$

where I is the identity matrix. The self-energy functions Σ_1 and Σ_2 account for the open boundary conditions [29]. Using the NEGF formalism and knowing the retarded Green's function then the electron density and current can be obtained [25, 26]. Since just the first few subbands are essentially occupied by electron carriers and needed to be taken into account in the simulations, computation time is significantly reduced.

To benchmark the different devices we use the subthreshold swing and DIBL as performance indicators. The subthreshold swing measures the rate of current increase with gate voltage below threshold and is expressed in millivolts of gate voltage per decade of drain current. It is defined as:

$$SS = \frac{dV_G}{d(log_{10} I_D)} \qquad 6.9$$

which for a MOSFET yields

$$SS = n\frac{k_B T}{q}\ln(10) \quad (\mathrm{mV/dec}) \qquad 6.10$$

Here k_B is the Boltzmann constant, T is the temperature in Kelvin, q is the absolute value of the electron charge and n is the body factor. The body factor presents the efficiency of the gate control over the channel potential and in the best case is equal to 1, which at room temperature (T=300K) gives a value of SS=59.6 mV/decade.

Typically, the effective channel length decreases with the creation of depletion regions in the channel region because of the source/drain junctions and it results in the degradation of the gate control over the channel region. The channel potential is

no longer controlled just by the gate electrode but also depends on the distance between source and drain regions and the voltage applied to the drain. DIBL is defined as:

$$DIBL = (V_{th}|_{V_{DS}=0.05V} - V_{th}|_{V_{DS}=0.65V})/(0.65 - 0.05) \quad 6.11$$

6.4. Results and discussion

In this section we present the simulation results on the effect of channel dimension, orientation and material and on the performance of JNTs and IM devices [21].

6.4.1 Device characteristics

Figure 6.4 shows the impact of cross-section dimension on the subthreshold swing and DIBL of Si and Ge JNTs and IM devices. For a fixed gate length the SS improves towards the ideal value of 59.6 mV/decade as the cross-section decreases for both types of devices. DIBL also decreases with increasing confinement. This is largely expected as the electrostatic control of channel charges by the gate improves with smaller cross-sections. Figure 6.5 exemplifies the anticipated behavior; a drop in the source-channel potential barrier with drain voltage is much larger in devices with larger cross-sections. In devices with T_{Ge}=6nm, for instance, the subthreshold swings of <100>- and <110>- oriented wires in JNTs are 12% and 20% better than those of IM transistors, respectively. The respective DIBL is 70% and 75% lower. This is due to the presence of space-charge regions in the channel region of IM devices associated with the source and drain PN junctions and also the increase of the drain space-charge region with drain voltage which results in degradation of gate control over the channel charges in IM devices compared to JNTs. This and the varying sensitivity in orientation for the JNTs and IM devices will be explained in more detail below.

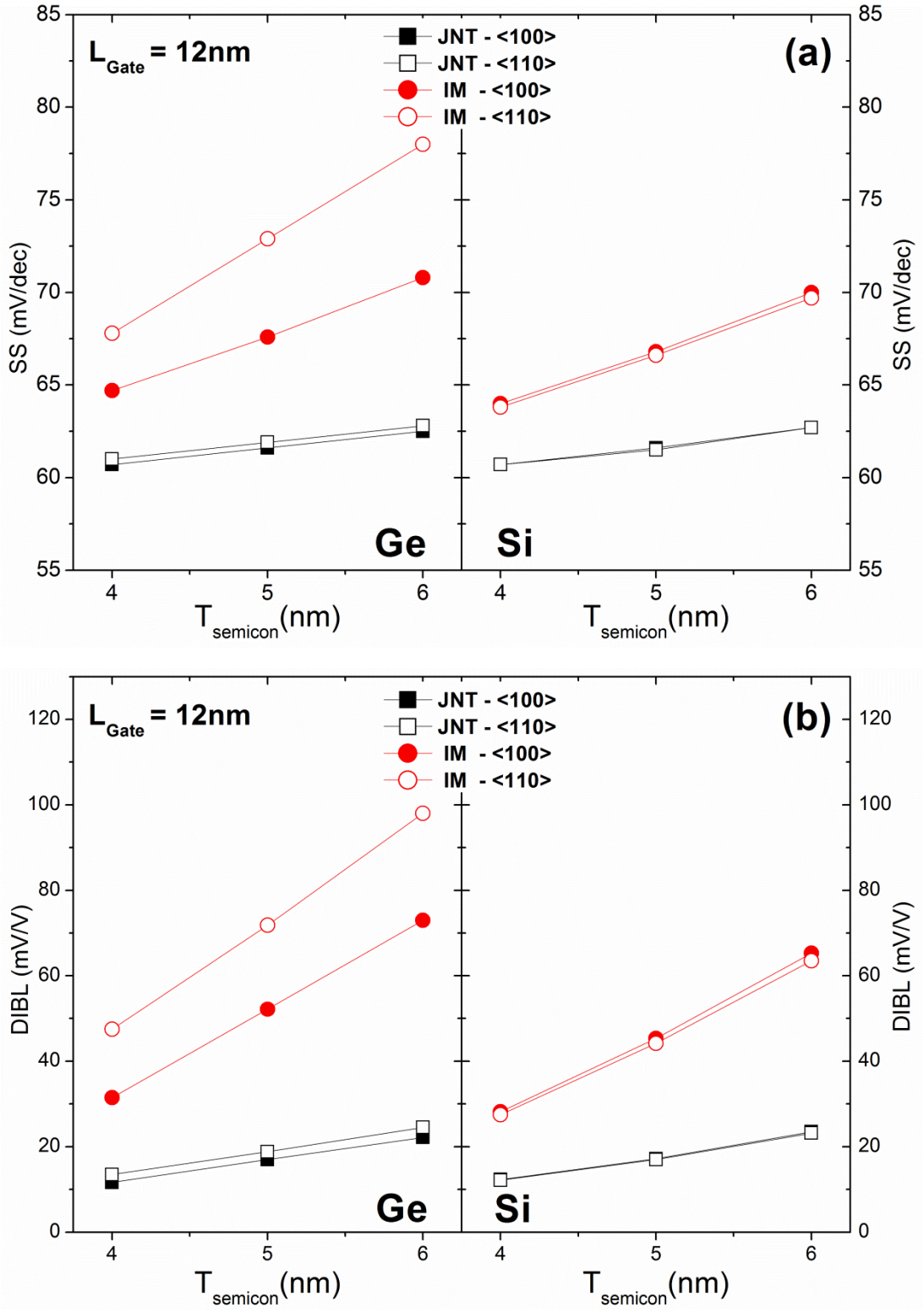


Figure 6.4 - (a) Subthreshold swing and (b) DIBL in junctionless nanowire transistors and inversion-mode devices for germanium and silicon nanowire channels.

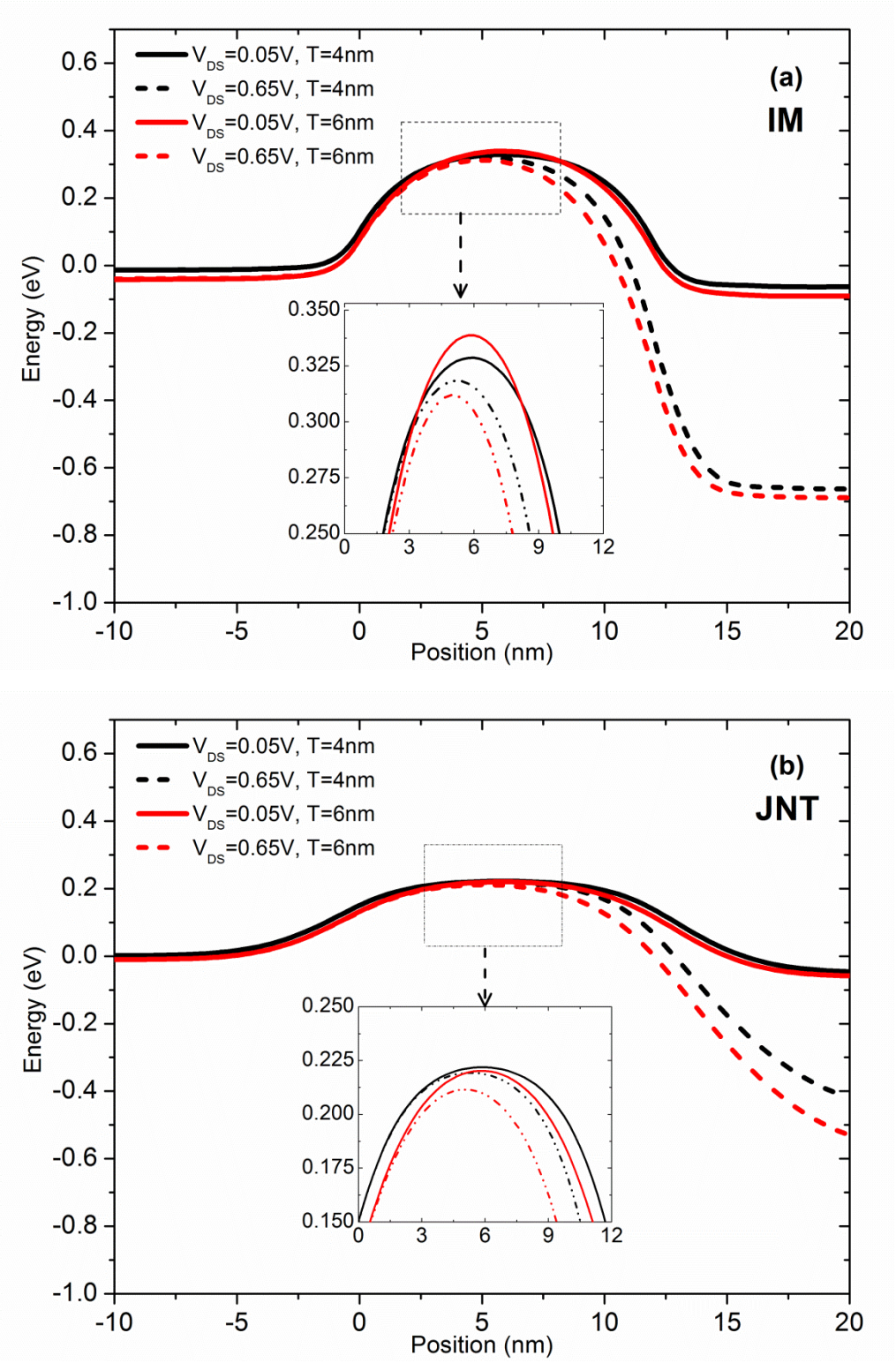


Figure 6.5 - Source-channel potential barrier of <100>-oriented silicon nanowires in (a) inversion-mode devices and (b) junctionless nanowire transistors. (L_{gate}=12 nm).

Figure 6.6 gives a general comparison of drive current characteristics of JNTs and IM nanowire transistors for different wire materials and channel orientations for a gate length of 10 nm. JNTs exhibits a better I_{on}/I_{off} ratio in every case, for a supply

voltage of V_{DD}=0.65V. It can also be seen that <110>-oriented IM germanium nanowires cannot be properly turned on at V_{gs}=V_{dd}=0.65V and have a poor I_{on}/I_{off} ratio due to a large subthreshold swing. The degradation of the device characteristics in this case results from the effective mass tensor of the Ge channel which determines the subband properties. There are three L-derived valleys for wires fabricated along the <110> direction (see Table 1). Those with higher effective masses along the confinement direction have the largest contribution to the total current since they are positioned lower in energy. On the other hand, their lower transport effective mass increases the source-to-drain tunneling, thereby, increasing the off-current. The details of the tunneling current contribution to the total current are discussed in the next section.

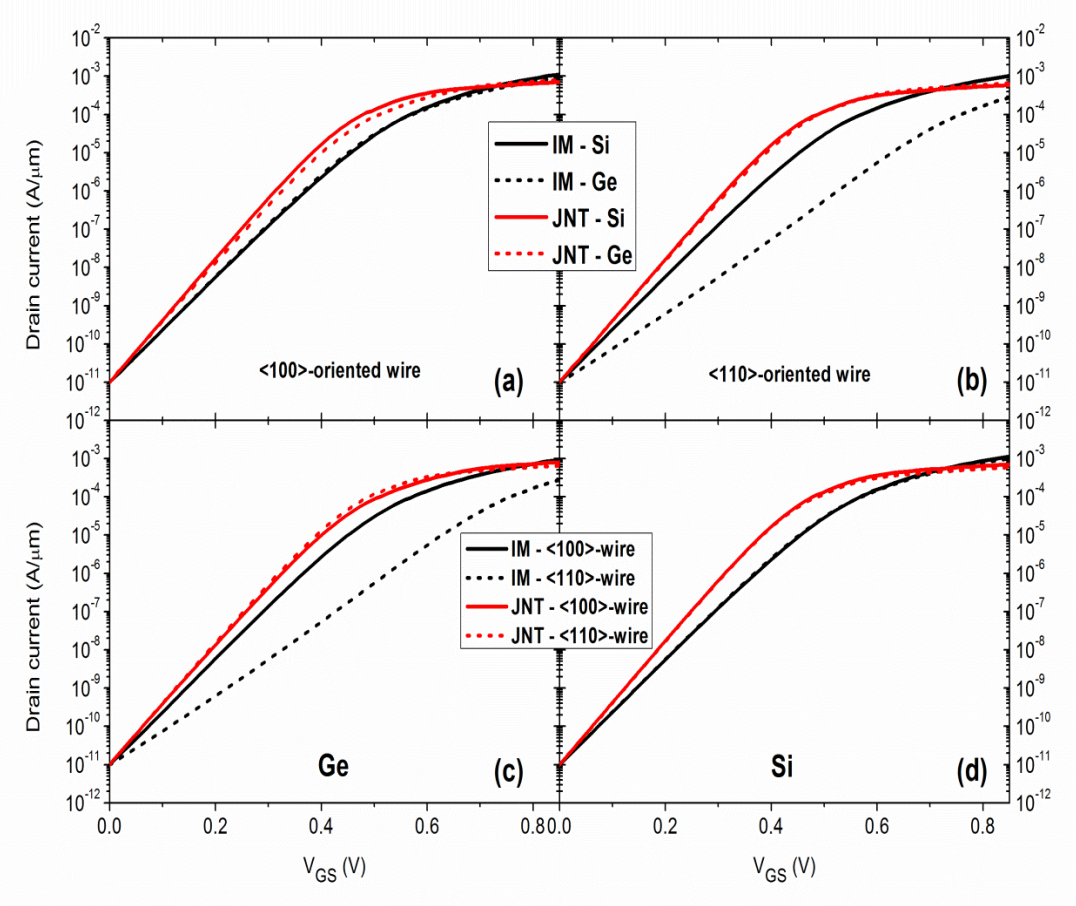


Figure 6.6 - Comparison of transfer characteristics for (a) <100>-wire orientation, (b) <110>-wire orientation and different channel material (c and d) in junctionless nanowire transistors and inversion-mode devices. (L_{gate}=10 nm, $T_{semicon}$=5 nm, V_{DS}=0.65V).

For completeness, Figure 6.7 shows how SS and DIBL depend on varying the cross-section in short channel devices, that is, keeping the ratio of gate length to thickness equal to two. As expected, short channel effects result in a larger increase in the DIBL and subthreshold-swing degradation in IM nanowire transistors compared with JNTs. Also, whilst Ge JNTs characteristics are comparable to the Si JNTs devices the use of <110>-oriented Ge as channel material in IM devices clearly yields the worse performance. An interplay between the larger effective gate length and the lower transport effective mass of the <100> Si channel compared to the Ge counterpart yields very similar short-channel behavior for both JNTs and IM devices made of these materials. Overall, Figure 6.7 shows that n-type Ge devices may at best be expected to perform equally well with their silicon counterparts.

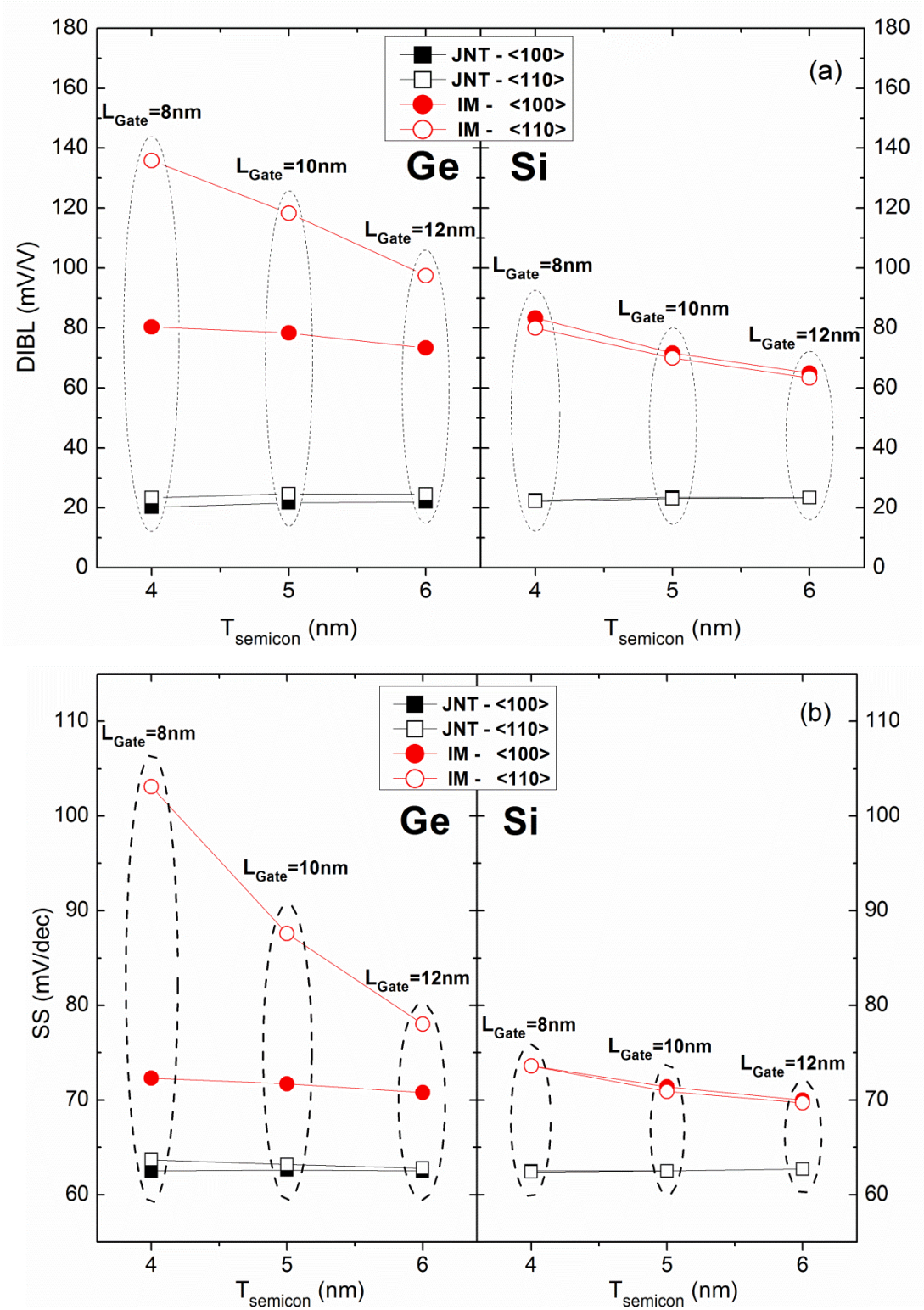


Figure 6.7 - Effect of channel material, wire orientation, and cross-section dimension on (a) DIBL and (b) subthreshold swing in junctionless nanowire transistors and inversion-mode devices.

6.4.2 Device physics

One reason for the worse short channel effect control in Ge nanowires than in Si devices can be explained by the concept of natural length (λ). The natural length is a

parameter which represents the extension of the electric field lines from the source and the drain into the channel region [30-32]. In gate-all-around devices with square cross-section is defined by the following expression:

$$\lambda = \sqrt{\frac{\varepsilon_{semicon}}{4\varepsilon_{ox}} T_{ox} T_{semicon}} \qquad 6.12$$

where ε_{ox} is the permittivity of the gate oxide, $\varepsilon_{semicon}$ is the permittivity of the wire material (Si or Ge), T_{ox} is the gate oxide thickness and $T_{semicon}$ is the nanowire thickness. The ratio of effective gate length to the natural length should be large enough for devices to be free of SCEs. According to this expression, short-channel effects can be minimized by: (i) decreasing the gate oxide thickness, (ii) decreasing the nanowire thickness, (iii) increasing the dielectric constant of the gate oxide material, and/or (iv) decreasing the dielectric constant of the wire material . Since $\varepsilon_{Si} < \varepsilon_{Ge}$ the natural length of Si nanowires is smaller than that of Ge nanowires ($\lambda_{Si} = 0.86\lambda_{Ge}$) and, as a result, Ge nanowires are more affected by short channel effects for the same gate length and device parameters.

The variation of the effective masses and specially their effect in the tunneling current is another reason for the difference in SCE control between Si and Ge devices. Figure 6.8 shows the contribution of source-to-drain tunneling current to the total current in the off state and in the on-state. As it can be seen in this figure, for both Si and Ge nanowires, source-to-drain tunneling in the subthreshold regime is much lower in JNTs than in IM devices. In the on-state, the source-to-drain tunneling is almost equal to zero in both Si and Ge JNTs, but not in IM devices. Moreover, the tunneling current is much larger in <110>-oriented than in <100>-oriented Ge nanowires. This is due to the small effective mass of the L-valleys ($0.082\times m_0$ along the transport direction), which carry the largest contribution to the total current. Within the <100>-oriented Ge nanowires the transport effective mass is much larger ($0.601\times m_0$), yielding a lower tunneling current. The smaller tunneling current in JNT compared to the IM nanowire device in the subthreshold regime can be explained by the larger effective gate length of JNTs in the off-state.

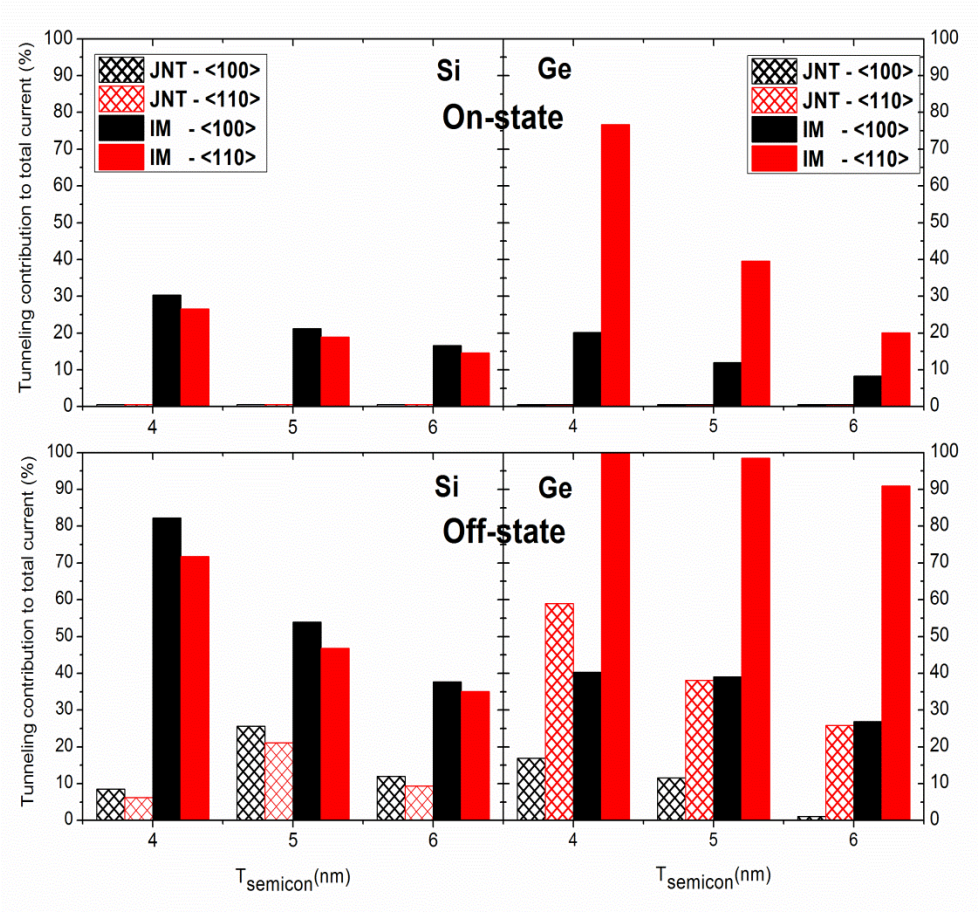


Figure 6.8 - The source-to-drain tunneling current contribution to the total current in the off- and the on-state regime for Si and Ge nanowires.

Figure 6.9 shows the first subband profile of Ge and Si JNTs and IM devices in both the off-state and the on-state. As it can be seen in this figure, for JNT in on-state there is no source/channel junction potential barrier, which virtually reduces the tunneling current to almost zero. As it is illustrated in Figure 6.9 the top of the potential barrier in the channel region is lower in the JNT than in the IM device in the off state. In addition, the potential barrier extends from the sides of the physical gate electrode into the source and drain regions, which produces an effective channel length longer than the physical gate length when the device is turned off. As a result, even in the off state regime, JNTs have smaller tunneling current than IM nanowire transistors.

JNTs have a larger effective gate length than the physical gate length ($L_{effective} > L_{physical}$) in the off-state and a smaller effective gate length than the physical gate length ($L_{effective} \leq L_{physical}$) in the on-state. This behavior justifies the highly improved short channel characteristics of JNTs [33, 34]. A plot of charge carrier concentrations

in the off- and on-states in a JNT illustrates the variation of effective gate length in Figure 6.10.

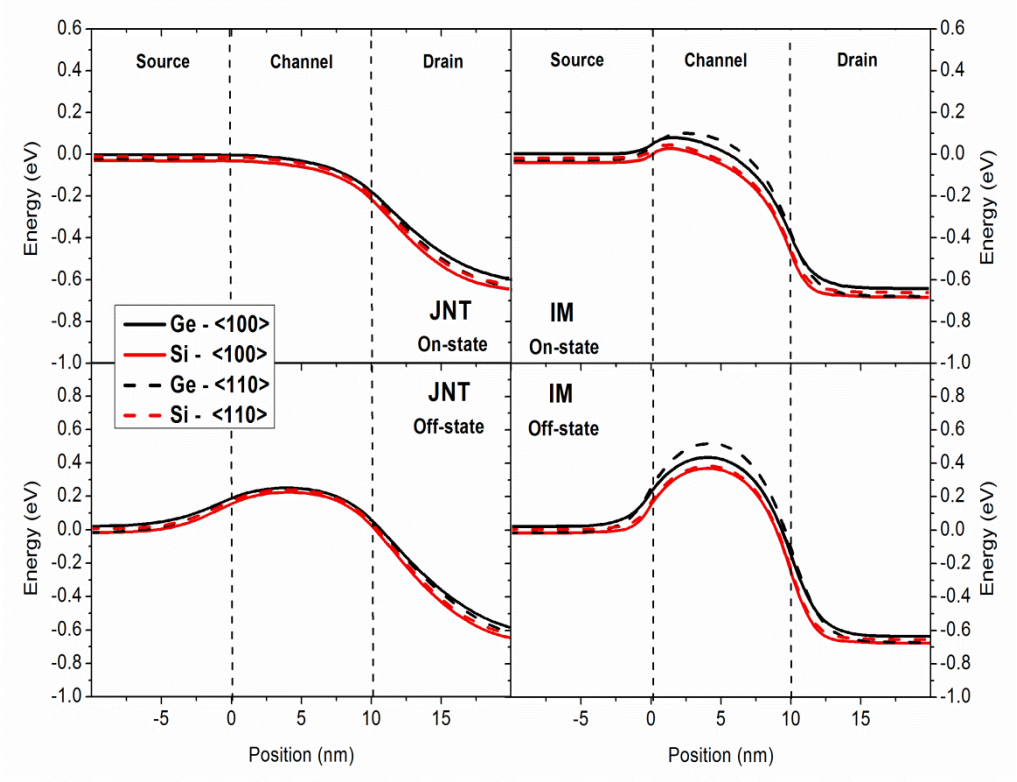


Figure 6.9 - The first subband profile of junctionless nanowire transistors and inversion-mode devices in both off-state and on-state regime for silicon and germanium nanowire transistors and different wire orientations. (L_{gate}=10 nm, $T_{semicond}$=5 nm).

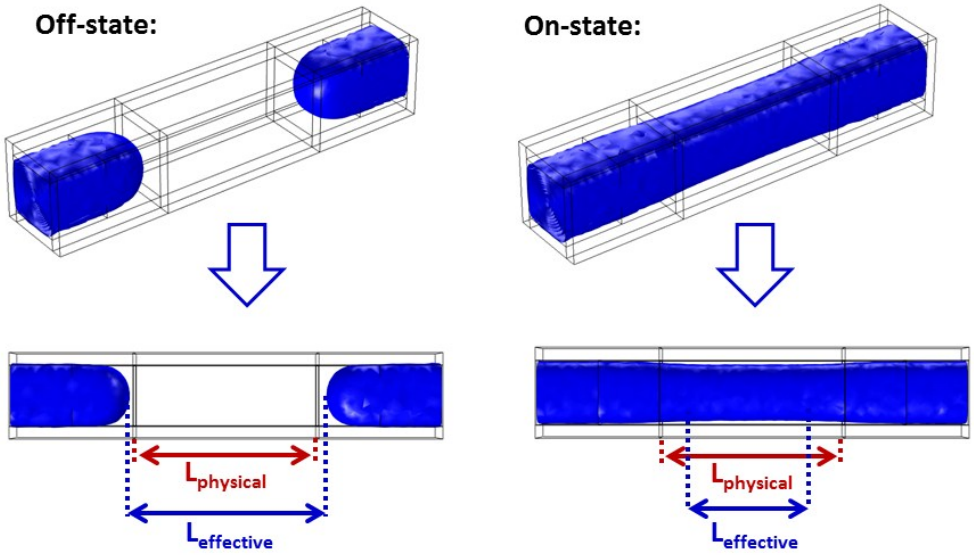


Figure 6.10 - Effective gate length variation from the off-state to the on-state in a junctionless nanowire transistor using the plot of charge carrier concentration. (The depleted region is transparent and the dark areas are neutral).

6.5. Conclusion

In this chapter the transfer characteristics, subthreshold swing, drain-induced barrier lowering, source-to-drain tunneling, and I_{on}/I_{off} ratio of junctionless nanowire transistors and inversion-mode devices were investigated using 3D quantum mechanical simulations. Impact of different wire orientation, material (namely, germanium and silicon), and device dimensions were studied. We conclude that <100>- and <110>-oriented junctionless nanowires with Si and Ge channels are more immune to short channel effects compared with the conventional IM devices. These JNTs provide smaller subthreshold swing, less DIBL, lower source-to-drain tunneling, and a larger I_{on}/I_{off} ratio.

We also showed that <110>-oriented Ge IM devices have much poorer short-channel characteristics than their Si counterparts. In contrast, the material and orientation of the channel does not have considerable effect on the device performance of JNTs which is because of the larger effective gate length that suppresses source-to-drain tunneling. As a result of this, regardless of the differences in the natural length and effective masses, n-type Ge and Si JNTs perform equally well.

References

[1] http://public.itrs.net/.

[2] J.-P. Colinge, "Multi-gate SOI MOSFETs," *Microelectronic Engineering,* vol. 84, pp. 2071-2076.

[3] N. Singh, A. Agarwal, L. K. Bera, T. Y. Liow, R. Yang, S. C. Rustagi*, et al.*, "High-performance fully depleted silicon nanowire (diameter ≤ 5 nm) gate-all-around CMOS devices," *Electron Device Letters, IEEE,* vol. 27, pp. 383-386, 2006.

[4] K. Saraswat, C. O. Chui, T. Krishnamohan, D. Kim, A. Nayfeh, and A. Pethe, "High performance germanium MOSFETs," *Materials Science and Engineering: B,* vol. 135, pp. 242-249, 2006.

[5] K. C. Saraswat, C. O. Chui, T. Krishnamohan, A. Nayfeh, and P. McIntyre, "Ge based high performance nanoscale MOSFETs," *Microelectronic Engineering,* vol. 80, pp. 15-21, 2005.

[6] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High-κ metal-gate stack and its MOSFET characteristics," *Electron Device Letters, IEEE,* vol. 25, pp. 408-410, 2004.

[7] J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain*, et al.*, "Nanowire transistors without junctions," *Nat Nano,* vol. 5, pp. 225-229, 2010.

[8] A. Kranti, R. Yan, C. W. Lee, I. Ferain, R. Yu, N. D. Akhavan*, et al.*, "Junctionless nanowire transistor (JNT): Properties and design guidelines," in *Solid-State Device Research Conference (ESSDERC), 2010 Proceedings of the European*, 2010, pp. 357-360.

[9] L. Ansari, B. Feldman, G. Fagas, J.-P. Colinge, and J. C. Greer, "Simulation of junctionless Si nanowire transistors with 3 nm gate length," *Applied Physics Letters,* vol. 97, pp. 062105-3, 2010.

[10] C.-W. Lee, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi*, et al.*, "Performance estimation of junctionless multigate transistors," *Solid-State Electronics,* vol. 54, pp. 97-103, 2010.

[11] J.-P. Raskin, J.-P. Colinge, I. Ferain, A. Kranti, C.-W. Lee, N. D. Akhavan*, et al.*, "Mobility improvement in nanowire junctionless transistors by uniaxial strain," *Applied Physics Letters,* vol. 97, pp. 042114-3, 2010.

[12] J.-T. Park, J. Y. Kim, C.-W. Lee, and J.-P. Colinge, "Low-temperature conductance oscillations in junctionless nanowire transistors," *Applied Physics Letters,* vol. 97, pp. 172101-2, 2010.

[13] D. Jang, J. W. Lee, C.-W. Lee, J.-P. Colinge, L. Montes, J. I. Lee*, et al.*, "Low-frequency noise in junctionless multigate transistors," *Applied Physics Letters,* vol. 98, pp. 133502-3, 2011.

[14] J.-P. Colinge, C.-W. Lee, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi*, et al.*, "Reduced electric field in junctionless transistors," *Applied Physics Letters,* vol. 96, pp. 073510-3, 2010.

[15] C.-W. Lee, A. Borne, I. Ferain, A. Afzalian, R. Yan, N. Dehdashti Akhavan*, et al.*, "High-Temperature Performance of Silicon Junctionless MOSFETs," *Electron Devices, IEEE Transactions on,* vol. 57, pp. 620-625, 2010.

[16] R. T. Doria, M. A. Pavanello, R. D. Trevisoli, M. de Souza, L. Chi-Woo, I. Ferain*, et al.*, "Junctionless Multiple-Gate Transistors for Analog Applications," *Electron Devices, IEEE Transactions on,* vol. 58, pp. 2511-2519, 2011.

[17] C. Seongjae, K. Kyung Rok, P. Byung-Gook, and K. In Man, "RF Performance and Small-Signal Parameter Extraction of Junctionless Silicon Nanowire MOSFETs," *Electron Devices, IEEE Transactions on,* vol. 58, pp. 1388-1396, 2011.

[18] P. Razavi, N. D. Akhavan., R. Yu, G. Fagas, I. Ferain, and J.-P. Colinge, "Investigation of Short-Channel Effects in Junctionless Nanowire Transistors," in *Solid State Devices and Materials (SSDM), the 2011 International Conference on*, 2011, pp. 106-107.

[19] M. Bescond, N. Cavassilas, K. Kalna, K. Nehari, L. Raymond, J. L. Autran, *et al.*, "Ballistic transport in Si, Ge, and GaAs nanowire MOSFETs," in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, 2005, pp. 526-529.

[20] J. Wang, A. Rahman, G. Klimeck, and M. Lundstrom, "Bandstructure and orientation effects in ballistic Si and Ge nanowire FETs," in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, 2005, pp. 4 pp.-533.

[21] P. Razavi, G. Fagas, I. Ferain, R. Yu, S. Das, and J.-P. Colinge, "Influence of channel material properties on performance of nanowire transistors," *Journal of Applied Physics,* vol. 111, pp. 124509-124509-8, 2012.

[22] D. Kim, T. Krishnamohan, Y. Nishi, and K. C. Saraswat, "Band to Band Tunneling limited Off state Current in Ultra-thin Body Double Gate FETs with High Mobility Materials : III-V, Ge and strained Si/Ge," in *Simulation of Semiconductor Processes and Devices, 2006 International Conference on*, 2006, pp. 389-392.

[23] S. Gundapaneni, M. Bajaj, R. K. Pandey, K. V. R. M. Murali, S. Ganguly, and A. Kottantharayil, "Effect of Band-to-Band Tunneling on Junctionless Transistors," *Electron Devices, IEEE Transactions on,* vol. 59, pp. 1023-1029, 2012.

[24] K. Nehari, N. Cavassilas, J. L. Autran, M. Bescond, D. Munteanu, and M. Lannoo, "Influence of band structure on electron ballistic transport in silicon nanowire MOSFET's: An atomistic study," *Solid-State Electronics,* vol. 50, pp. 716-721, 2006.

[25] S. Datta, "Nanoscale device modeling: the Green's function method," *Superlattices and Microstructures,* vol. 28, pp. 253-278, 2000.

[26] J. Wang, E. Polizzi, and M. Lundstrom, "A three-dimensional quantum simulation of silicon nanowire transistors with the effective-mass approximation," *Journal of Applied Physics,* vol. 96, pp. 2192-2203, 2004.

[27] http://comsol.com.

[28] M. Bescond, N. Cavassilas, and M. Lannoo, "Effective-mass approach for n-type semiconductor nanowire MOSFETs arbitrarily oriented," *Nanotechnology,* vol. 18, p. 255201, 2007.

[29] S. Datta, *Quantum Transport: Atom to Transistor*, Cambridge University Press, 2005.

[30] R. H. Yan, A. Ourmazd, and K. F. Lee, "Scaling the Si MOSFET: from bulk to SOI to bulk," *Electron Devices, IEEE Transactions on,* vol. 39, pp. 1704-1710, 1992.

[31] C.-W. Lee, S.-R.-N. Yun, C.-G. Yu, J.-T. Park, and J.-P. Colinge, "Device design guidelines for nano-scale MuGFETs," *Solid-State Electronics,* vol. 51, pp. 505-510, 2007.

[32] J.-P. Colinge, "Multiple-gate SOI MOSFETs," *Solid-State Electronics,* vol. 48, pp. 897-905, 2004.

[33] J.-P. Colinge, A. Kranti, R. Yan, I. Ferain, N. D. Akhavan, P. Razavi*, et al.*, "A Simulation Comparison between Junctionless and Inversion-Mode MuGFETs," *ECS Transactions,* vol. 35, pp. 63-72, 2011.

[34] P. Chan-Hoon, K. Myung-Dong, K. Ki-Hyun, S. Chang-Woo, B. Chang Ki, J. Yoon-Ha*, et al.*, "Comparative study of fabricated junctionless and inversion-mode nanowire FETs," in *Device Research Conference (DRC), 2011 69th Annual*, 2011, pp. 179-180.

Chapter 7 : Performance Investigation of III-V Nanowire Transistors

7.1. Introduction

As discussed in the previous chapters of this thesis, rapid scaling of MOSFETs down to decananometers leads to detrimental short channel effects and degrade the reliability of nanotransistors. Several device structures, such as MuGFETs and thin-body silicon-on-insulator (SOI) transistors, as well as the introduction of high-k gate dielectrics and channels made of high mobility materials have been proposed to improve the device performance and decrease short channel effects in nanotransistors [1-4]. In chapter 6, we extensively discussed the case of germanium used as a channel material for both junctionless nanowire transistors and inversion mode devices and explained the device physics underlying the behavior of basic performance parameters. Here, we study another class of channel materials, namely, III-V compound semiconductor nanowires such as GaAs, GaSb, and InP, which are also attractive candidates for next generation MOSFETs. They offer unique possibilities to control their fundamental properties during growth (through dimension, doping, and composition) as well as high electron mobility [5, 6]. However, in devices scaled below 10 nm the classic transfer characteristics are not necessarily determined by physical parameters such as the mobility and expectations from classical device concepts need to be tested.

In this chapter, we investigate the use of III-V semiconductors in state-of-the-art nanotransistor architectures and compare their electrical performance with Si channels [7]. The short channel characteristics of III-V junctionless and IM nanowire transistors are studied using 3D quantum mechanical simulations in the ballistic regime. The ballistic approximation is justified after explicit simulation of the acoustic and optical (polar optical in III-V channels) electron-phonon scattering. This analysis lets us explain the physical origin of the short channel behavior of III-V nanowires and determine the effect of their materials properties on device performance. After introducing the device structures and parameters of our simulations in the next section, we present the discussion of our results in section 7.3. The chapter concludes with a brief summary.

7.2. Device structure and simulation parameters

We consider different III-V materials namely GaAs, InP, and GaSb as channel materials of gate-all-around nanowire transistors with channel orientations of <100>. The devices are patterned on (010)-oriented wafers. Figures 7.1 (a) and (b) show a schematic view of gate-all-around (GAA) nanowire transistor with a square cross-section as well as the doping profile in the longitudinal direction for junctionless and inversion-mode devices. These do not differ from the devices investigated in chapter 5 and 6 but their diagrams are included here for completeness. Gate lengths are considered to be 10 nm. Uniform doping concentrations throughout the channel and source/drain regions of the devices have been used. In IM transistors the source and drain junctions to the undoped channel are assumed to be abrupt and doping concentrations in the source/drain regions are 1×10^{20} cm^{-3}. The doping concentration in JNTs is 1×10^{20} cm^{-3} throughout the device. The effective oxide thickness (EOT) is equal to 1 nm for all devices. The supply voltage (V_{dd}) is equal to 0.65 V and the same off-current of 100 nA/μm which is suitable for high performance logic technologies [3] is set for all transistors by tuning the gate workfunction. Band-to-band tunneling (BTBT) has not been considered in the simulations. In fact, because of the strong quantization effect, the band gap in the simulated nanowires becomes even larger than bulk devices as the channel thickness becomes smaller and BTBT rate is considerably decreased [8].

The material properties used in the simulations are listed in Tables 7.1 and 7.2 [9, 10] for the III-V materials and Si, respectively. In ultra-scaled devices, maintaining a good sub-threshold characteristic is very important. We use the subthreshold swing (SS) and drain-induced barrier lowering (DIBL) as performance indicators in our simulations. SS shows the rate of current increase with gate voltage below threshold and presents the efficiency of the gate control over the channel potential. It is expressed in mV/decade. Decrease of threshold voltage while increasing the drain voltage is expressed by DIBL. As explained in chapter 5, the reason of this reduction is that the channel potential is no longer controlled only by the gate. In the next section we present simulation results of the subthreshold swing, DIBL, I_{on}/I_{off} ratio in JNTs and compare them with those of conventional IM devices.

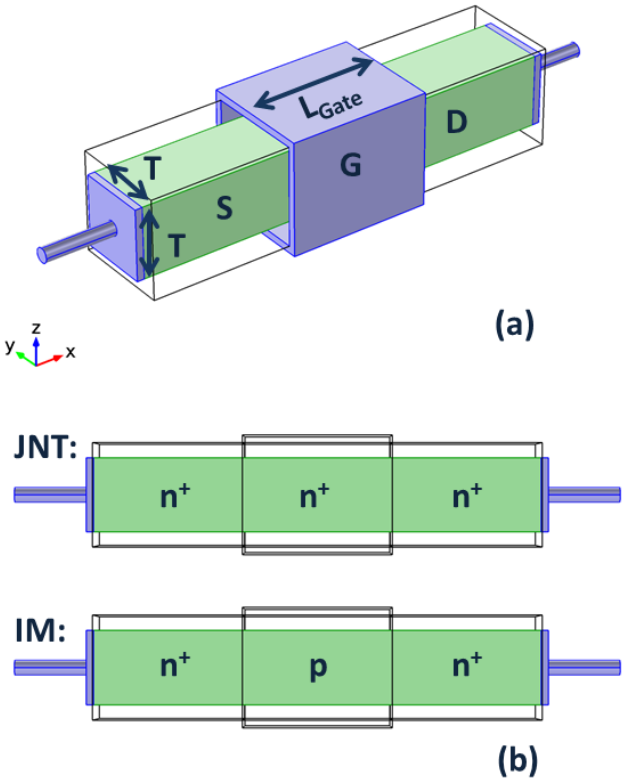


Figure 7.1 - (a) Bird eye's view of a gate-all-around nanowire MOSFET and (b) doping profile in the longitudinal direction in junctionless nanowire transistors and inversion-mode devices.

Table 7.1 – *Material properties for III-V compound semiconductors. (E_g^Γ is the bandgap, ΔE_L and ΔE_X are the L- and X- valley band-offsets from the Γ-valley, and m_t, m_l, and m_Γ are transverse, longitudinal and isotropic Γ-valley effective masses, respectively; and m_0 is the free electron mass).*

	Dielectric constant	E_g^Γ ***(eV)***	ΔE_L ***(eV)***	ΔE_X ***(eV)***	m_Γ/m_0	$m_t/m_0, m_l/m_0$ ***(L)***	$m_t/m_0, m_l/m_0$ ***(X)***
InP	*12.4*	*1.353*	*0.59*	*0.85*	*0.08*	*0.13, 1.64*	*0.34, 1.26*
GaAs	*12.9*	*1.422*	*0.29*	*0.48*	*0.067*	*0.075, 1.9*	*0.27, 1.98*
GaSb	*15*	*0.727*	*0.063*	*0.329*	*0.039*	*0.1, 1.3*	*0.22, 1.51*

Table 7.2 - Material properties for Si. *(E_g^X is the bandgap, ΔE_L is the L-valley band-offset from the X-valley, and m_t, m_l, and m_Γ are transverse, longitudinal and isotropic Γ-valley effective masses, respectively; and m_0 is the free electron mass).*

	Dielectric constant	E_g^X **(eV)**	ΔE_L **(eV)**	m_t/m_0, m_l/m_0 **(X)**	m_t/m_0, m_l/m_0 **(L)**
Si	11.7	1.12	0.88	0.19, 0.98	0.12, 1.7

7.3. Simulation results and discussion

In Figure 7.2 we compare I_{ds}-V_{gs} of Si and GaAs nanowire for gate length 22nm and 10 nm in the presence of phonon scattering. We consider acoustic and optical phonon scattering interactions in Si, and acoustic and polar optical scattering mechanisms in GaAs. One can see that for L_{gate}=10 nm the electron-phonon coupling does not affect the I_{ds}-V_{gs} significantly. Since in our simulations the considered gate length is 10nm, we use the ballistic transport simulations for the rest of this chapter.

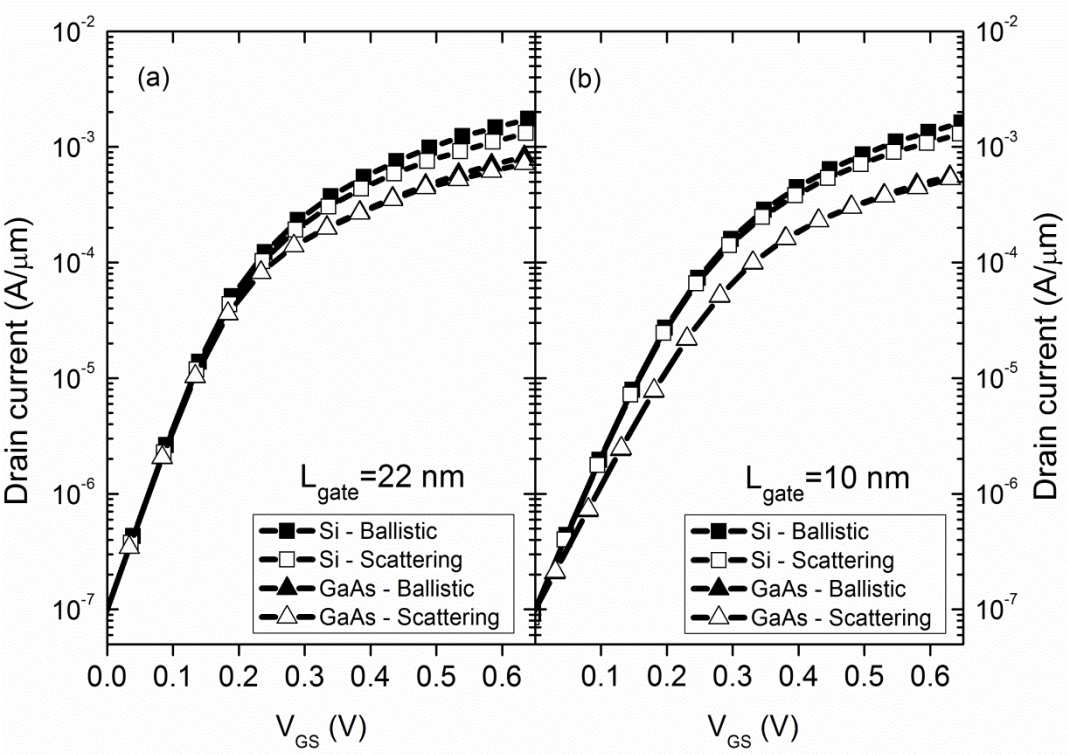


Figure 7.2 – Transfer characteristics of Si and GaAs channels with gate length (a) 22 nm and (b) 10 nm. A comparison between ballistic transport and transport including electron-phonon scattering is shown.

Figure 7.3 and 7.4 show the subthreshold swing and DIBL of different inversion-mode and junctionless III-V nanowires compared with the silicon nanowire device.

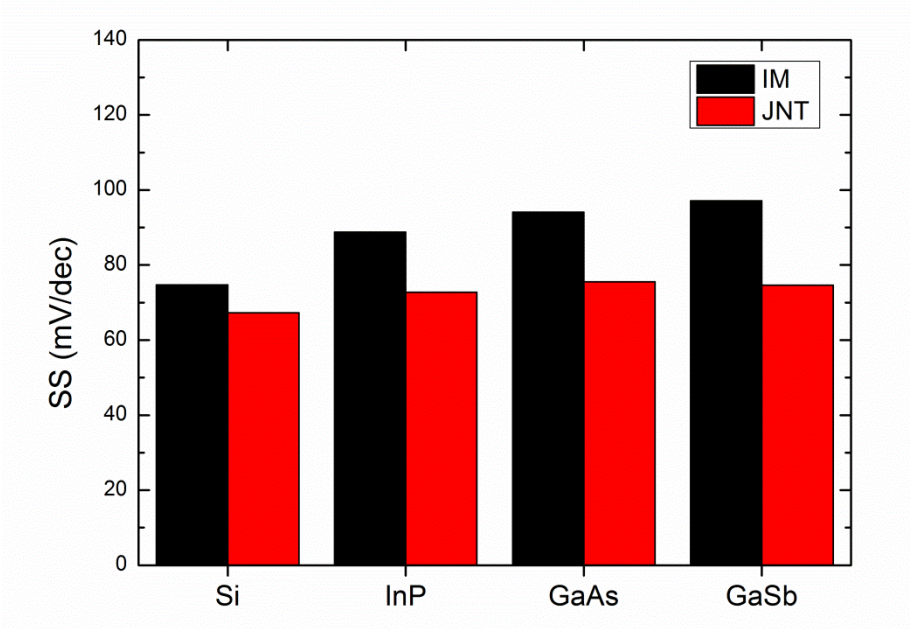


Figure 7.3 –Subthreshold swing in IM and junctionless nanowire transistors made of Si and III-V compound semiconductors.

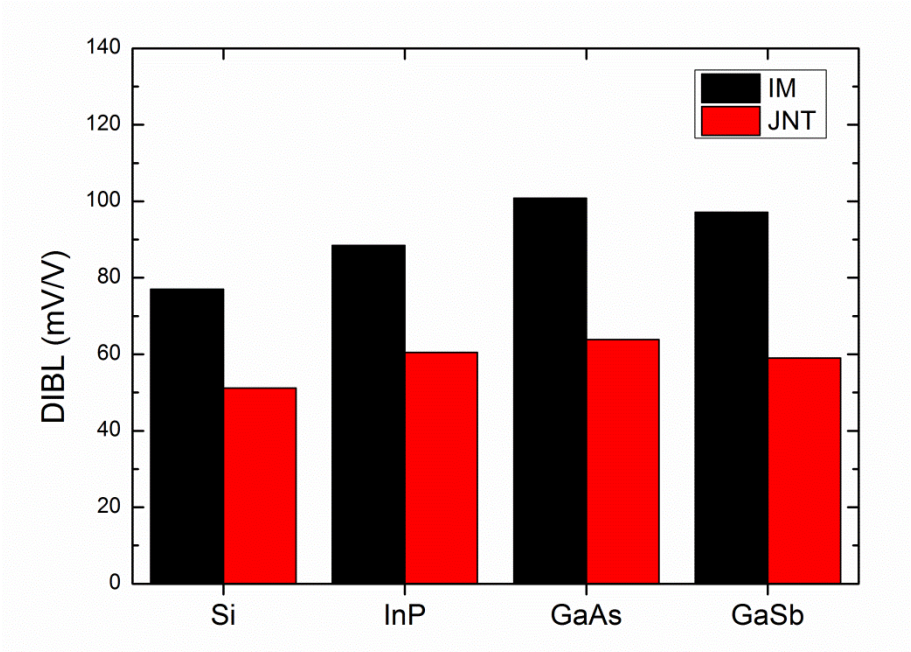


Figure 7.4 – Comparison of DIBL in IM and junctionless nanowire transistors made of Si and III-V compound semiconductors (*DIBL* is defined as $(\boldsymbol{V_{th}|_{V_{DS}=0.05V} - V_{th}|_{V_{DS}=0.65V}})/(\mathbf{0.65 - 0.05})$).

As it can be seen in these figures, a Si nanowire device is more immune to short channel effects. This is attributed to the larger transport effective mass and smaller dielectric constant of silicon which leads to smaller natural length [7]. As discussed in chapter 6, the ratio of gate length to the natural length should be large enough for devices to be free of SCEs. Figure 7.5 shows the natural length for Si and other III-V compound materials.

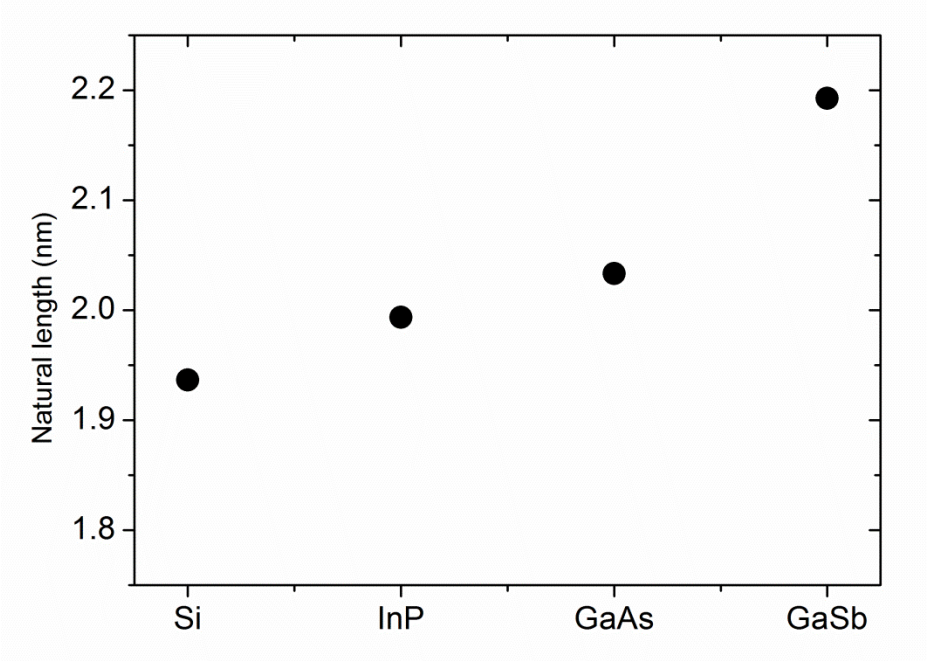


Figure 7.5 –Natural length for Si and different III-V compound semiconductors.

InP nanowire has the smallest subthreshold swing in comparison with the other III-V nanowire devices simulated here which is due to its larger effective mass along the current direction. The larger transport effective mass suppresses the source-to-drain tunneling current. On the other hand, GaSb has the largest subthreshold swing due to its smallest transport effective mass. Nonetheless, GaSb nanowire has higher on-current in comparison with the other simulated III-V nanowires which is due to the contribution of its L-valleys to the carrier transport at higher gate voltages (Figure 7.6). Figures 7.6 and 7.7 show respectively the drive current and on-to-off current ratio of different III-V JNTs and IM devices compared to nanowire transistors with silicon channels of the same geometrical parameters. It is found that at this scale channels made of silicon nanowires have better drive current and on-to-off current ratio compared to III-V nanowires. This is attributed to the better subthreshold swing of the silicon devices and also due to the fact that III-V materials have a low density of states (DOS) in the Γ-valley which results in the reduction of

the drive current [11]. The off current of the III-V nanowire channels is affected widely by source-to-drain tunneling compared with the silicon nanowire device which is due to their smaller transport effective mass; hence, they have larger subthreshold swing than Si JNTs and IM devices.

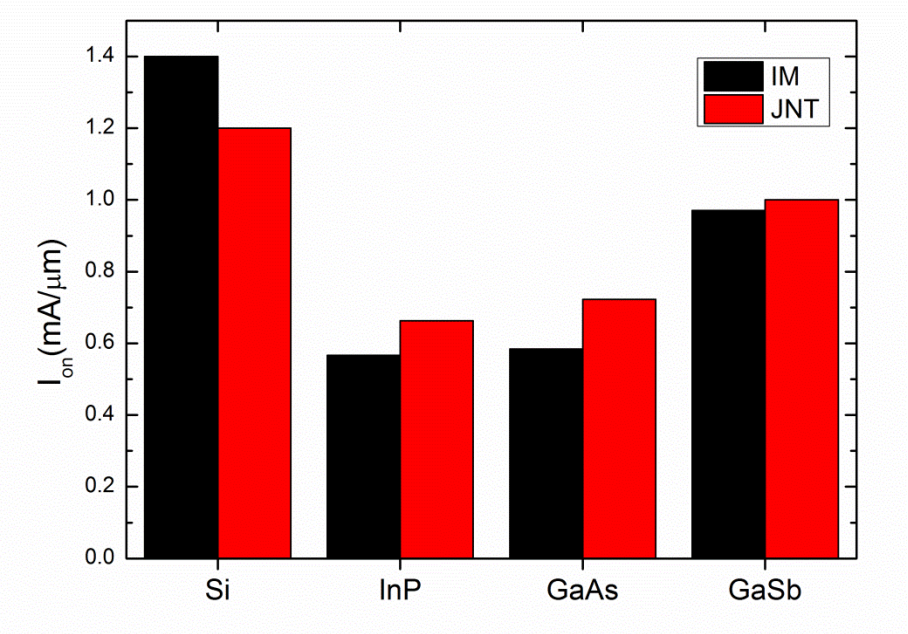


Figure 7.6 - On current of different III-V nanowires compared to silicon nanowire with the same physical parameters (I_{on} extracted at V_{GS}=0.65V).

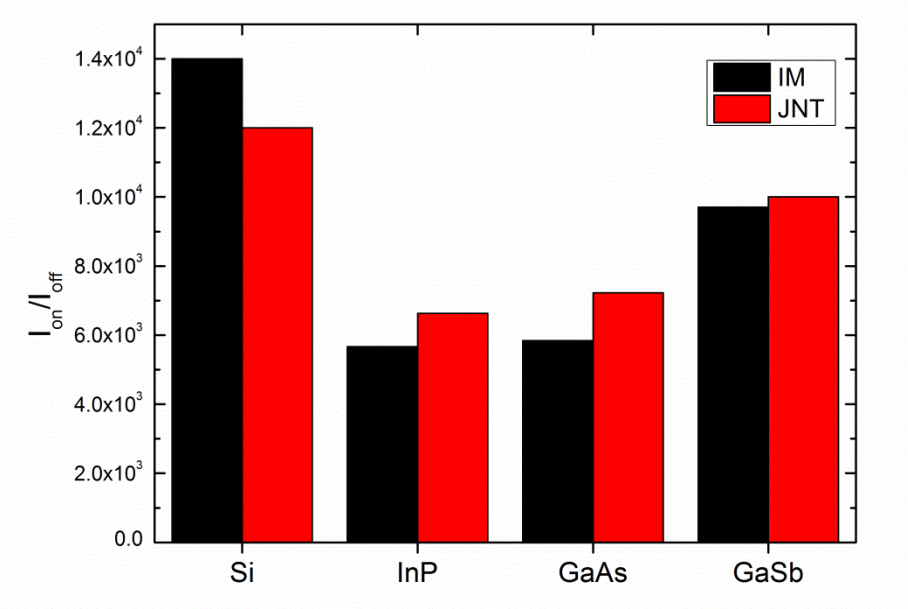


Figure 7.7 - On-to-off current ratio of different III-V nanowires compared to silicon nanowire with the same physical parameters.

Finally, upon comparison of the performance parameters of JNTs with IM devices, one concludes that JNTs are more immune to SCEs. This is because of the larger effective gate length in this device architecture compared with that of IM nanotransistors, as shown in chapter 6.

7.4. Conclusion

In this chapter the short channel behavior of III-V JNTs and IM nanowire devices was studied and compared with those of transistors made of Si nanowire channels. We considered the subthreshold swing, drain-induced barrier lowering, and I_{on}/I_{off} ratio as performance indicators in our simulations. Our study confirms that JNTs are more immune to short channel effects than conventional IM devices and present smaller subthreshold swing and DIBL. This is traced back to the larger effective gate length that suppresses source-to-drain tunneling. Discussing the materials dependence, we also showed that InP has the smallest subthreshold swing among the other simulated III-V nanowire devices simulated here (GaAs, GaSb). This is due to the larger transport effective mass of InP. Finally, we showed that at ultrascaled regime, silicon nanowire channels can have better drive current and on-to-off current ratio compared to III-V nanowire devices. This electrical performance is explained by suppression of source-to-drain tunneling due to the higher effective mass and materials parameters that determine the natural length (shortest for Si). Higher on-current is also observed for the Si device as the mobility concept does not apply at this length scale and the drive current is largely determined by the density of states in the confined channel. These considerations are important to take into account when designing transistors at the nanoscale.

References

[1] J.-P. Colinge, "Multi-gate SOI MOSFETs," *Microelectronic Engineering,* vol. 84, pp. 2071-2076, 2007.
[2] N. Singh, A. Agarwal, L. K. Bera, T. Y. Liow, R. Yang, S. C. Rustagi*, et al.*, "High-performance fully depleted silicon nanowire (diameter ≤ 5 nm) gate-all-around CMOS devices," *Electron Device Letters, IEEE,* vol. 27, pp. 383-386, 2006.
[3] http://public.itrs.net/.
[4] J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain*, et al.*, "Nanowire transistors without junctions," *Nat Nano,* vol. 5, pp. 225-229, 2010.

[5] M. A. Khayer and K. L. Roger, "Modeling and Performance Analysis of III-V Nanowire Field-Effect Transistors," ed, 2010.
[6] K. Tomioka, M. Yoshimura, and T. Fukui, "A III-V nanowire channel on silicon for high-performance vertical transistors," *Nature,* vol. 488, pp. 189-192, 2012.
[7] P. Razavi and G. Fagas, "Electrical performance of III-V gate-all-around nanowire transistors," *Applied Physics Letters,* vol. 103, pp. 063506-3, 2013.
[8] D. Kim, T. Krishnamohan, Y. Nishi, and K. C. Saraswat, "Band to Band Tunneling limited Off state Current in Ultra-thin Body Double Gate FETs with High Mobility Materials : III-V, Ge and strained Si/Ge," in *Simulation of Semiconductor Processes and Devices, 2006 International Conference on*, 2006, pp. 389-392.
[9] M. Lundstrom, *Fundamentals of Carrier Transport*, 2nd ed., Cambridge University Press, 2000.
[10] I. Vurgaftman, J. R. Meyer, and L. R. Ram-Mohan, "Band parameters for III--V compound semiconductors and their alloys," *Journal of Applied Physics,* vol. 89, pp. 5815-5875, 06/01/ 2001.
[11] A. Pethe, T. Krishnamohan, K. Donghyun, O. Saeroonter, H. S. P. Wong, Y. Nishi*, et al.*, "Investigation of the performance limits of III-V double-gate n-MOSFETs," in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, 2005, pp. 605-608.

Chapter 8 : General Conclusions and Future Perspectives

Since multi-gate MOSFETs are a major candidate for next-generation CMOS devices, in this thesis we studied the performance of several multigate structures such as FinFET, Triple-gate, and gate-all-around MOSFETs in both semi-classical and quantum regimes and considered different device properties such as channel materials and orientation, dimensions, and doping concentrations. The performance of different types of MOSFETs such as junctionless, inversion-mode and accumulation-mode MOSFETs was also compared. To this aim, in addition to using commercial TCAD software such as SILVACO TCAD and Synopsys TCAD, we developed a self-consistent three-dimensional quantum-mechanical simulator based on the non-equilibrium Green's function formalism and in the framework of effective mass approximation. Our 3D simulator is able to consider different semiconductors (namely Si, Ge, and several III-V compound semiconductors) as channel material as well as considering both ballistic and dissipative transport regimes. Different scattering mechanisms can be treated by our simulator, e.g., acoustic and optical phonon scattering for non-polar semiconductors and polar optical scattering for polar semiconductors. Four different methods have been implemented in the simulator to solve the Schrödinger–Poisson equations self-consistently in order to study the device physics and quantum properties of nanowire transistors at the end of the road map. We also proposed a new method called Fast-coupled-mode-space (FCMS) which is technically a mixture of both fast-uncoupled-mode-space (FUMS) and coupled-mode-space (CMS). This method benefits from the speed of FUMS and the accuracy of CMS approaches at the same time. FCMS method can be used to simulate quantum transport of devices with any shape and any kind of discontinuities and can be run on a standard PC. Unlike the real-space approach, FCMS is very useful for extensive simulations and results obtained with this approach are in good agreement with the real-space approach.

From the physical point of view, the device performance and short channel effects such as DIBL, subthreshold swing, off-leakage current of several multigate

structures as well as drain breakdown voltage of bulk and SOI FinFETs were studied.

We also carried out an extensive study on the performance of the newly proposed type of field-effect-transistors called junctionless nanowire transistor (JNT). The electrical characteristics of JNTs were compared to accumulation-mode (AM) and inversion-mode (IM) devices. For all the studied device structures and materials, we demonstrated that JNT is more immune to SCEs compared to IM device due to its larger effective gate length. Moreover, for the modeled n-channel nanowire devices we found that at very small cross sections the nanowires with silicon channel are more immune to SCEs. Interestingly, the mobility of the channel material is not as significant in determining the device performance in ultra-short channels as other material properties such as the dielectric constant and the effective mass. For a device with fixed gate length, the electrostatic control over the channel carriers improves with shorter natural length which scales as the square root of the dielectric constant. Also, the source-to-drain tunneling current which affects short-channel characteristics is higher for channel materials with smaller transport effective mass. From the comparison of important device metrics such as the intrinsic gate delay and energy-delay product, we found that JNTs with gate length of 22 nm down to 15 nm have larger intrinsic gate delay than those of IM devices with the same gate lengths due to smaller on-state current. But, on the other hand, switching energy is lower in JNTs compared to IM devices due to the lower gate capacitances in JNTs. As a result, energy-delay product of JNTs and IM devices is almost identical for simulated devices.

Although we tried our best to explain the short channel behavior of modern device structures with different channel materials using numerical simulation, there is definitely a lot of work left for further studies of physical phenomena as well as numerical models used in this work. For example, a lot of work can to be done on the physical modeling of different III-V nanowires such as InGaAs nanowire transistor and also junctionless transistors made in silicon, germanium, III-V compound semiconductor or any other materials. As the fabrication process of junctionless transistors is much simpler than the conventional transistors with junctions even at ultra-scaled regime, these devices are an attractive candidate for future technological nodes. Moreover, there is still plenty of work in extending and optimizing the numerical techniques which have been used in this work as well as

adding capabilities to model carrier transport in the valence band of p-type nanowire FETs and capturing the strain effects.