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Semiconductor Nanowire Fabrication by Bottom-Up and Top-Down Paradigms

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ABSTRACT: Semiconductor nanowires have been the subject of intensive research investment over the past few decades. Their physical properties afford them applications in a vast network of active microelectronic research fields, including logic device scaling in very large scale integrated circuits, sensor devices and energy harvesting. A range of routes to semiconductor nanowire production have opened up due to advances in nanowire fabrication techniques over the last number of decades. These nanowire fabrication routes can usually be categorized into one of two paradigms, bottom-up or top-down. Microelectronic systems typically rely on integrated device platforms, where each device and component thereof can be individually addressed. This requirement for precise addressability places significant demands on the mode of fabrication, specifically with regard to device definition, placement and density, which have typically been strengths of top-down fabrication processes. However, in recent years advances in bottom-up fabrication processes have opened up the possibility of a synergy between bottom-up and top-down processes to achieve the benefits of both. This review article highlights the important considerations required for the continued advancement of semiconductor nanowire fabrication with a focus on the application of semiconductor nanowire fabrication for next-generation field-effect transistor devices.

1. Semiconductor Nanowires

Semiconductor nanowires are pseudo 1-D structures where the magnitude of the semiconducting material is confined to a length of less than 100 nm in two dimensions. Semiconductor nanowires have a vast range of potential applications[1], including electronic (logic devices, diodes)[2], photonic (laser, photodetector)[3–5], biological (sensors, drug delivery)[6], energy (batteries, solar cells, thermoelectric generators)[7,8], and magnetic (spintronic, memory)[9–11] devices. Semiconductor nanowires can be fabricated by a range of methods which can be categorised into one of two paradigms, bottom-up or top-down. Bottom-up processes can be defined as those where structures are assembled from their sub-components in an additive fashion. Top-down fabrication strategies use sculpting or etching to carve structures from a larger piece of material in a subtractive fashion. The challenge of continuous microelectronic device scaling to meet industry targets, *e.g.* 'Moore's Law'[12], and the diversification of the microelectronics industry into new materials for specialized applications ('More than Moore')[12], has motivated research in semiconductor nanowires for the past number of decades. The massive competition for a share of the global 304 billion USD semiconductor market[13], has driven the expansion of the semiconductor nanowire research area, resulting in the evolution of, new fabrication techniques, innovative processes, new materials and creative advancements in semiconductor nanowire device design.

Nanowire materials offer a number of benefits over conventional planar materials for FET applications. Firstly, nanowires offer the option of creating gate-all-around (GAA) architectures, which allow for more efficient control over charge carriers in the channel of FET devices, thus reducing short channel effects caused by drain induced barrier lowering (DIBL).[14–16] The use of multi-gate architectures such as the GAA architecture, facilitates the formation of shorter channel devices, and thus allows for increased device density to be achieved on a given chip. Additionally, fabrication of nanowires of a wide range of materials has been demonstrated which may not be readily produced in wafer form.[1,17–22]

This review aims to summarize and compartmentalize the various approaches taken by both the bottom-up and top-down paradigms in this field, whilst identifying potential spaces in which both top-down and bottom-up approaches may be used in tandem. Primarily, this review will focus on Si and promising high charge carrier mobility materials for logic device applications, although, as mentioned previously the nanowire fabrication routes highlighted herein are also relevant to a whole host of potential device applications.

Firstly, the major fabrication routes to produce semiconductor nanowires in both paradigms will be discussed, whilst identifying recent advances and highlighting the benefits and drawbacks of these routes. The synergistic use of both top-down and bottom-up approaches to produce structures unattainable by either route alone will also be considered. Next, the most promising materials for high mobility logic device fabrication

will be considered. The current issues with processing these materials within each fabrication paradigm will also be addressed.

2. Bottom-Up Semiconductor Nanowire Fabrication

2.1. Semiconductor Nanowire Growth Methods

Numerous routes exist to the bottom-up fabrication of semiconductor nanowires. The vapor-liquid-solid (VLS) mechanism and analogues thereof, is the most commonly used route to semiconductor nanowire production.[1,23,24] The VLS mechanism relies on a vapor phase precursor of the nanowire material which impinges on a liquid phase seed particle, from which unidirectional nanowire growth proceeds. The choice of an appropriate seed material has the benefit of allowing control over the diameter of the nanowires produced, whilst the seed material can also significantly affect the crystalline quality of the nanowire.[25,26] At this point, the importance of selection of an appropriate precursor material should be highlighted. Within a given precursor, MR_x, where 'M' represents the semiconductor element, or elemental component of a compound semiconductor, and 'R', represents a ligand. The M-R bond should be sufficiently labile under nanowire synthesis conditions to directly liberate reactive M species for nanowire growth, or to disproportionate forming reactive M species indirectly.[27,28] Furthermore, the R group liberated upon precursor decomposition should ideally exist as a gas phase species to prevent contamination of the nanowire product with liquid or solid phase by-product. Consequently, metal hydrides are often used as precursor compounds for nanowire growth, as H_2 gas is an especially clean by-product which has the benefit of inhibiting undesirable oxide formation for non-oxide semiconductor nanowire growth. Metal hydride precursors are commonly used in the growth of nanowires by chemical vapor deposition (CVD), given that metal hydrides such as SiH_4 and GeH_4 generally exist as gas phase compounds[29]. Metal-organic precursors, such as diphenylsilane and diphenylgermane, often used in solution phase and supercritical fluid phase nanowire synthesis can produce carbonaceous by-products which may be difficult to completely separate from the nanowire product.[30,31] Semiconductor nanowire synthesis conditions often encourage the formation of reactive radical species which can initiate polymerisation reactions resulting in unwanted contaminating by-products,[32] and as such, precursor design should always be considered when designing an experiment for semiconductor nanowire synthesis. Analogues of the VLS mechanism include supercritical fluid-liquid-solid (SFLS)[24], supercritical fluid-solid-solid (SFSS),[33,34] solution-liquid-solid (SLS)[35], vapor-solid-solid (VSS)[36,37] and oxide assisted growth (OAG)[38] mechanisms. Common to all of these analogues is the existence of a collector or seed particle which acts as a sink for the nanowire material, and from which unidirectional growth proceeds.[39] Conventionally, the seed particle is a metal with which the nanowire material or component thereof forms an alloy. However, autocatalytic or self-seeded semiconductor growth has also been demonstrated.[40–46] Self-seeded VLS-type nanowire growth is most commonly observed for compound materials such as InP, GaN and SnO_2 whereby the metallic component of the material, In, Ga and Sn for InP, GaN and SnO_2 respectively, forms seed particles for nanowire growth of the compound material.[45–47] However, there have also been reports of self-seeded nanowire growth for elemental materials where a VLS-type mechanism has been invoked.[48] The most commonly used metal catalyst for VLS-type nanowire growth is Au, prepared either as colloidal Au nanoparticles or as an evaporated or sputtered thin film. However, Au is inherently incompatible with semiconductor device manufacturing. Au has a high diffusivity in Si and also acts as a deep level acceptor and thus has detrimental effects on device performance.[49–51] Furthermore, Au is a highly inert material which makes cleaning of instrumentation contaminated with Au extremely difficult. For example, traditional Au etchants include aqua regia (concentrated nitric acid and hydrochloric acid solution), KI/I_2 solution and alkali cyanide solutions, all of which would corrode stainless steel equipment and in the case of alkali solutions result in detrimental effects on semiconductor device performance, such as shifting of threshold voltage (V_t).[52,53] Consequently, there has been significant research into alternative, complementary metal-oxide-semiconductor (CMOS) production compatible, metal seeds for catalyzed VLS semiconductor nanowire growth.[54–56] Acceptable metals should have ionization energies far from the mid band-gap region of the semiconductor material. Si nanowire growth has been demonstrated using a number of Si CMOS compatible metals including Bi[35] and Al.[57] Great care must be applied even when using CMOS compatible metals for nanowire growth, as these metals can still act as active dopants in the nanowire material. Al, for example can readily migrate through Si via interstitial sites in the Si lattice, thus acting as an n-type dopant in Si.[58,59] Furthermore, Si migration through the Al metal is also possible and may dramatically affect the electrical performance of the nanowire material.[60] A seed metal, such as Al may also be beneficial for preparation of an Ohmic contact to the nanowire tip, thus facilitating nanowire FET device formation.

One benefit of bottom-up nanowire growth over top-down processing is that nanowires grown by bottom-up methods may be doped in-situ during crystal growth by incorporating dopant precursors in the nanowire synthesis procedure. Consequently, bottom-up grown nanowires may not require destructive techniques such as ion implanting to generate additional charge carriers. Ion implanting can destroy atomic ordering in the implanted region of the semiconductor crystal and requires subsequent thermal annealing steps to restore crystal ordering.[61]

In addition to VLS-type nanowire growth mechanisms there exists a range of other routes to produce bottom-up grown nanowires. These routes, which do not invoke the VLS growth mechanism include, oriented attachment,[62,63] metal organic vapor phase epitaxy (MOVPE),[64,65] molecular beam epitaxy (MBE),[66] soft templating,[22,67,68] dislocation driven unidirectional growth[42] and crystal habit modification.[69–71]

2.2. Nanowire Alignment Techniques

Bottom-up grown semiconductor nanowires fabricated by the methods outlined above are typically produced as entangled meshes of nanowires and as a result lack the periodic ordering and placement required for large-scale semiconductor device processing. Figure 1 displays an SEM image of an entangled mesh of SiO_2-coated Ge nanowires.

Recently there have been a number of techniques developed to align semiconductor nanowires produced as entangled meshes.[72] Examples include alignment of polar nanowires within strong electric fields,[73,74] dielectrophoresis,[75,76] microfluidic alignment,[77] lubricant-assisted contact printing,[78–80] and evaporation-induced alignment.[81–83] Electric field-based alignment techniques, including dielectrophoresis, have been shown to allow precise control over nanowire position with respect to metallic contact pads, however, these techniques have not yet demonstrated the high density of aligned nanowires required for high volume manufacturing (HVM), which is currently approaching a device half-pitch of 20 nm.[12] Figure 2 displays images of nanowires aligned by dielectrophoresis at a pitch of ~ 20 µm.

Microfluidic alignment, contact printing and evaporation induced alignment techniques have all demonstrated the capability to create parallel nanowire arrays, in some cases with high areal density. Fan *et al*., for example, have demonstrated aligned nanowires at a density of ~10 nanowires/µm.[78] However, these techniques lack the prerequisite precision of control over nanowire placement, required for individual nanowire addressability within very large scale integrated circuit (VLSI) technology. Nevertheless, such techniques have been used not only to demonstrate successful individual device operation, but, also to demonstrate integrated devices in a fully functioning nano-processor.[79]

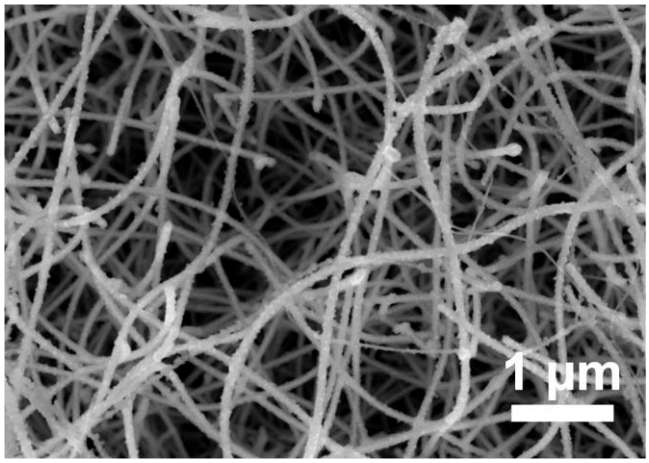


Figure 1. An SEM image of an entangled mesh of SiO_2-coated Ge nanowires grown from colloidal Au nanoparticles by the SFLS method.

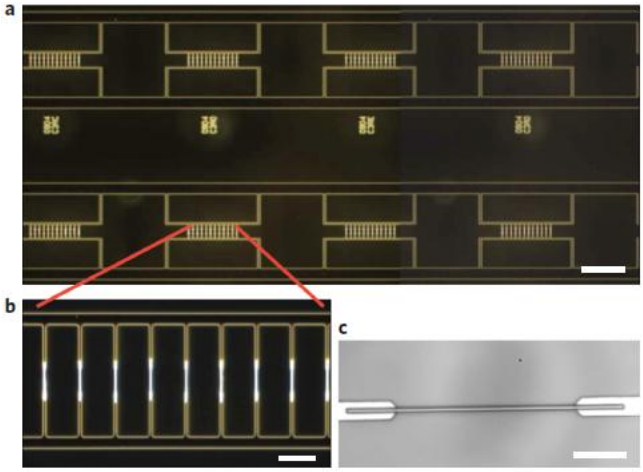


Figure 2. Optical dark-field and DUV images of nanowires assembled onto electrodes by dielectrophoresis: (a) dark-field image of defect-free nanowire assembly arranged on electrode arrays (scale bar = 200 µm), (b) high magnification dark-field image of nanowires aligned on 2 µm wide electrodes (scale bar = 20 µm) and (c) DUV image of a single nanowire aligned on electrodes separated by 12 µm (scale bar = 4 µm).[76]

A change of direction may be required for bottom-up approaches to achieve the requisite nanowire density, placement control and alignment required for VLSI manufacturing. High density vertical semiconductor nanowire films have been produced using a range of bottom-up techniques. These techniques include, epitaxial nanowire growth,[25,57,65,84–89] and hard-templated nanowire growth.[90,91] Figure 3 shows an SEM image of vertically aligned epitaxially grown nanowires, where the diameter was controlled by an anodized aluminium oxide (AAO) template.

The epitaxial route to semiconductor nanowire synthesis has the advantage of controlling nanowire crystal orientation

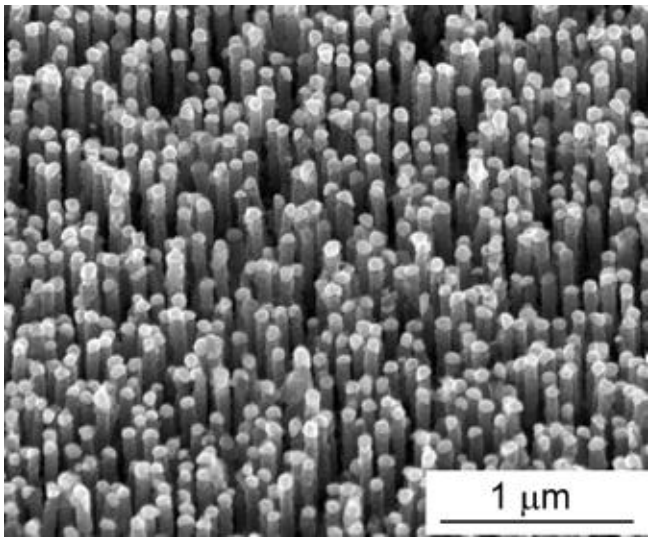


Figure 3. SEM image of epitaxial vertical Si nanowire arrays grown within an AAO hard template (template removed in image). Nanowire crystal orientation is controlled epitaxially by the substrate, whilst diameter and placement of the nanowires is controlled by the template.[90]

through the selection of an appropriate substrate crystal orientation. Wang *et al.* for example, have demonstrated the epitaxial growth of vertically aligned <111> oriented Si nanowires on a <111> Si substrate by CVD using an Al catalyst. Nanowires can also be produced epitaxially when there is a large lattice mismatch between the nanowire material and the substrate material. Tomioka *et al.* reported the growth of <111> oriented InAs nanowires on a Si <111> substrate, despite an 11.6 % lattice mismatch between the two crystals, by using a 'selective area' MOVPE technique whereby lattice mismatch strain was dissipated by limiting the interfacial area between the two crystals.[65] A patterned amorphous SiO_2 thin film, prepared by electron beam lithography and etching, acted as a mask for growth of the nanowires by vapor phase epitaxy. Shimizu *et al.* have shown that the combined use of epitaxial nanowire growth and an ordered template such as AAO to control the position of these nanowires, allows a route to ordered arrays of vertically aligned, coaxial, Si nanowires suitable for use in vertical nanowire device fabrication (figure 3).[90] Ordering of pores in AAO spontaneously occurs during AAO formation as a mechanism to reduce internal strain in the AAO film.[92] The formation of AAO with hexagonally close packed (HCP) pores can be considered a bottom-up process, as the pores self-assemble into a HCP arrangement from an initial disordered state, pore by pore.[92]

2.3. Vertical Nanowire Field Effect Transistors

There have been several reports of field effect transistor (FET) devices produced using vertically aligned, bottom-up grown semiconductor nanowires.[93–100] Figure 4 shows electron microscopy images of vertical Si nanowires used to create vertical nanowire FET devices. The reported devices showed reasonable performance characteristics with observed I_{ON}/I_{OFF} ratios > 10^5 and a sub-threshold slope of 120 mV/decade, although their performance was still significantly poorer than current state-of-the-art, top-down, strained Si devices.[14,101] The vertical nanowire devices demonstrated significantly lower on/off ratios and shallower sub-threshold slopes than their top-down counterparts. The reasons for their inferior performance can be attributed to a number of issues including, contact resistance at the source and drain interfaces, non-uniform dopant distribution within the nanowire channel, charge trapping at the gate dielectric interface, or charge carrier recombination due to Au incorporation within Au-seeded Si nanowires. Some of these issues may be rectified, for example, the choice of an appropriate seed metal for nanowire growth is important. Not only should the seed metal allow production of the desired nanowire structure, the metal should also have an appropriate work function to form an ohmic contact to the semiconductor nanowire.[102,103] Au tends to form Schottky contacts to n-Si resulting in high contact resistance to the semiconductor nanowire channel.[104] The choice of metal also depends strongly on the majority charge carrier and carrier concentration in the nanowire device, for example p-type devices require metals with increased work function values compared to n-type devices, and higher semiconductor charge carrier concentrations result in reduced depletion layer widths at the metal-semiconductor junction which facilitates carrier tunnelling and thus reduced contact resistance.[104] Alternatively, the option exists to use a seed metal which has an inappropriate work function to produce the nanowires and subsequently strip this metal away by chemical etching, followed by the deposition of a suitable electrical contact metal. However, this approach introduces additional device processing steps and complete removal of the seed metal after chemical etching is unlikely, especially when alloys may have formed with the semiconductor during nanowire growth. The issue of dopant distribution is critical to device performance. A homogeneous, activated dopant distribution is desired within semiconductor devices in order to assure a stable threshold voltage (V_t).[105] Perea *et al.* have mapped the dopant distribution within an individual VLS grown Ge nanowire, and have shown the dopant distribution to be non-uniform along the nanowire growth axis and radially across the nanowire.[106] Techniques such as single ion implantation have been shown to improve the homogeneity of dopant incorporation in the nanowire structure resulting in improved V_t stability from device to device.[105] A number of approaches have been taken to improve semiconductor nanowire surface passivation to remove surface state charge trapping sites, which can have capacitive effects at the nanowire surface and hinder device performance. These approaches include organic passivation of the nanowire surface,[107–110] deposition of dielectric materials such as SiO_2, and Al_2O_3 and nitridation or sulfidation of the nanowire surface.[111,112] Finally, issues arising due to metal dopants from the catalyst metal particle can be negated through the use of an appropriate metal for the semiconductor of choice. The metal should not have ionization energies at or near the centre of the band-gap of the semiconductor, *e.g.* Al or Bi for Si. Once the outstanding issues detailed above have been addressed, bottom-up grown vertical nanowire FETs may become a practical route toward continued device footprint scaling within VLSI technology.

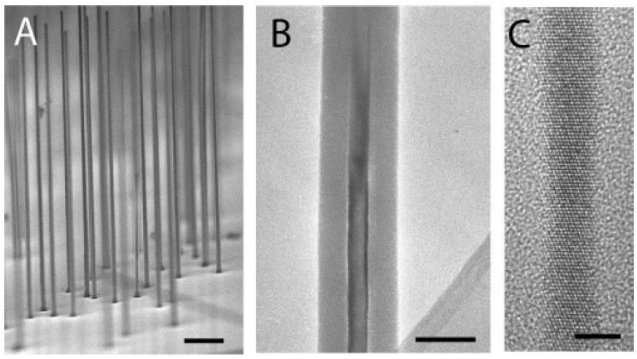


Figure 4. Vertically aligned, epitaxial, Au seeded, Si nanowires with thermally grown SiO_2 shells. Scale bars represent lengths of 1 µm, 75 nm and 4 nm in (a), (b) and (c) respectively.[99]

2.4. Bottom-Up Semiconductor Nanowire Outlook

There are a number of outstanding issues associated with the integration of bottom-up grown semiconductor nanowires into conventional integrated circuit (IC) design and processing. Conventional IC design is based on the active channel of the logic devices lying coplanar to the Si wafer substrate, and requires a very high degree of control over placement of the devices so that they may be individually addressed for successful IC operation. Traditionally, bottom-up grown semiconductor nanowires are grown as entangled meshes and consequently lack the prerequisite ordering, and control of place-

ment required for IC manufacturing.[24,40,113] Although there have been recent advances in extracting nanowires from such entangled meshes and aligning them on substrates, these approaches can produce neither the high density of nanowires desired, nor the large scale areal coverage required, for HVM.[74–77,79,81,114] As such, industrial applications of entangled meshes of semiconductor nanowires may be limited to the production of nanowire composites, which may have applications in areas such as batteries, flexible electrodes and thermoelectric generators.[115–117] However, there still remains significant value to be gained from the study of individual, novel, nanoscale structures, from a conceptual standpoint. Given the issues associated with the alignment of bottom-up grown semiconductor nanowires in the substrate coplanar orientation, it seems imperative that another route to IC fabrication be devised. Perhaps the most promising route toward integration of bottom-up grown semiconductor nanowires into an IC compatible arrangement is that of a vertically oriented active channel with respect to the substrate. Transferring to a vertical orientation would be a huge change for a very mature technology. However, recent developments in the industry with the adoption of tri-gate and finFET structures have shown that movement out of the plane of the Si substrate is possible and as such presents an opportunity for the development of 3-D device architectures.[118] Advances in CVD techniques for nanowire growth have allowed the production of epitaxial nanowires whereby the crystalline orientation of the nanowires with respect to a substrate is controlled at the epitaxial interface. Operational vertically integrated nanowire field effect transistors (VINFETs), produced using bottom-up grown semiconductor nanowires have been reported by several groups.[96,99,100,119] The VINFET concept remains a viable option for future semiconductor device processing as it potentially offers a route to high density stacks of GAA nanowire FET devices. The vertical orientation with respect to the substrate allows devices to be stacked on the substrate which ultimately increases the density of devices and thus computing power per chip area. A wrap around gate or GAA structure also offers superior electrostatic control of the channel compared to current devices in production, which may allow improved switching of the device. However, a great amount of work is still required to individually contact each device within such a high density, stacked architecture and consequently IC fabrication using VINFET devices is still in its infancy. Furthermore, the International Technology Roadmap for Semiconductors (ITRS) has targeted a line width roughness (LWR) value of 1.4 nm 3σ for device structures by 2015.[12] LWR values in the targeted range are not yet achievable in semiconductor nanowire fabrication by bottom-up means, where the narrowest nanowire diameter distributions typically possess 3σ values of approximately 3 nm.[120,121] Consequently, further work is required in the areas of alloy engineering and nanowire catalyst control to achieve the targeted control of nanowire diameter for device components in future VLSI manufacturing. Bottom-up grown nanowires are expected to possess fewer surface dangling bonds than their top-down analogues, which are fabricated by etching. A reduction in dangling bond density for bottom-up grown nanowires can be attributed to nanowire surface faceting during nanowire growth, which is driven by a reduction in the surface chemical potential and atomic diffusion during crystal growth.[122] Surface dangling bonds can trap charge carriers in the nanowire thus reducing carrier density, and also inhibit effective gating of nanowire FETs by introducing interface states at the semiconductor-dielectric interface.[56,123] Additional annealing steps are typically employed in top-down fabrication to reduce nanowire surface roughness and dangling bond density to improve electrical performance of top-down fabricated nanowires.[123–125]

3. Top-Down Semiconductor Nanowire Fabrication

3.1. Optical Lithography

Optical lithography has been the industry standard for semiconductor device definition and placement for decades. In that time there have been significant developments in optical lithography, both in terms of resist technology and optics.[126–129] There has been a general trend toward shorter wavelength radiation sources to achieve higher image resolution as given by the relationship in equation 1 derived from the Rayleigh criterion.[129]

$$CD = \frac{k\lambda}{NA} \quad (1)$$

CD represents the minimum critical dimension that can be imaged in a photoresist using a given process having a process latitude factor of *k*, an emission wavelength λ (nm), and a numerical aperture *NA*, where $NA = n\sin\theta$, where *n* represents the refractive index of the medium in which the final projection lens is operating and θ represents the half-angle of the maximum cone of light that exits the final lens of the system. In the 1970s, Hg G-line emission, at a wavelength of 436 nm, was the light-source of choice for optical lithography. Current VLSI manufacturing employs an ArF laser with an emission wavelength of 193 nm. In addition to reducing the wavelength of the radiation source, other measures have also been taken to improve image resolution. DUV scanners and steppers regularly incorporate a reduction lens as the final projection lens of the lithography system. Reduction lenses typically allow 4 × or 5 × reduction of features in the photomask.[128] The use of reduction lenses in scanners and steppers results in a consequent scaling of the image field, which translates as an increase in the number of exposure fields per wafer and thus a lower throughput of wafers. Consequently, 2 × reduction lenses are often used as a compromise between reduced feature size (*CD*) and wafer throughput. Although reduction lenses do not increase the resolution of the lithography process, they can be used to scale larger features in the photomask to a fraction of that size in the image projected on the photoresist. This scaling reduces some of the demands placed on mask manufacturing, as low density larger features are typically produced with fewer defects than high density, smaller features in mask

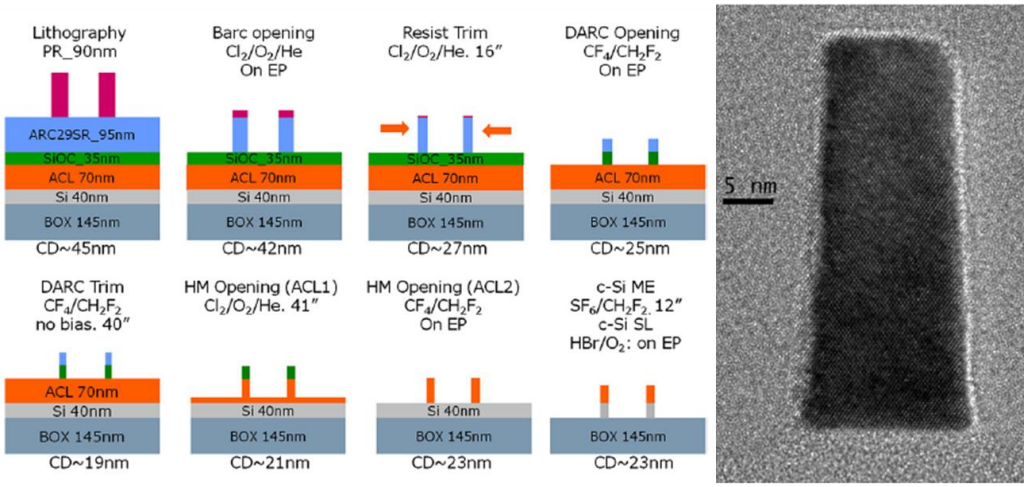


Figure 5. TEM image of a cross-section of a 10 nm × 40 nm Si nanowire produced from SOI using a 193 nm immersion lithography process incorporating resist trimming steps and overetching.[130]

fabrication. Interference lithography can be used to create arrays of features with *CD* values a fraction of the wavelength of the radiation source.[128,131–133] Interference lithography requires a number of coherent beams of radiation to be focused on a spot to create an interference pattern, where the period of the pattern is a fraction of the initial radiation wavelength. Typically interference lithography is only used to produce arrays of structures such as gratings. Immersion lithography is a technique whereby the final projection lens of the radiation source is immersed in a medium with a higher refractive index than air, *e.g.* water 1.436 at 193 nm. Increasing the refractive index of the medium in which the final lens operates, effectively increases the *NA* value of the system and as such reduces the minimum *CD* of features that can be imaged in the photoresist.[128] Media with higher refractive indices than water are also being investigated to further increase the process resolution.[128] The '*k*-factor' or process latitude factor given in equation 1, is a broad term which depends on a number of process dependant parameters. The '*k*-factor' accounts for photoresist effects, developer effects and reticle (photomask) effects, amongst others, and as such is a difficult term to predict for a new process. In essence, a high '*k*' value is representative of a lower resolution process, where process parameters limit the achievable resolution. Typical '*k*' values can be as low as 0.15, thus allowing features with dimensions a fraction of the wavelength of the incident light, to be imaged in the photoresist.[128,134] Techniques that can be used to reduce '*k*' values include the use of high resolution resists and resist trimming processes, as shown in figure 5.[129,134] However, even with such low '*k*' values, achieving the high feature densities desired for current semiconductor device production requires further process developments such as, optical proximity correction (OPC),[126,135] phase shift masks (PSM),[136] and double patterning (figure 6).[16,130] Ultimately continued device scaling and increased device density may require extreme ultra-violet (EUV) or x-ray lithography (XRL) due to the dramatically reduced wavelengths of these techniques, typically 13.5 nm for EUV and < 1 nm for XRL, compared to current UV lithography techniques. Whilst short wavelength techniques like EUV and XRL offer significant potential for nanolithography, they do have drawbacks. EUV lithography tools have to operate in vacuum due to strong EUV absorption by air. Consequently, EUV resists should not be volatile or swell or under vacuum.[137] Additionally, the requirement for loading and unloading wafers from vacuum chambers puts significant time demands on the process. Furthermore, shot noise, proximity effects and flare issues remain outstanding, all of which will hinder the ultimate resolution of the lithography process. XRL too has a number of issues which may prove to be prohibitive for HVM. XRL requires synchrotron radiation sources which may prove to be too large an investment for an unproven manufacturing process with considerable associated risk. However, XRL does not demonstrate the significant, detrimental, radiation-material interactions observed for EUV and as such it remains a pursued and viable option for further technological development.[129]

The significant technological advancements in the field of optical lithography outlined above demonstrate the suitability of these techniques to fabricate ordered arrays of semiconductor nanowires with excellent control over placement and feature-size. Lateral nanowires may be fabricated from layered substrates such as silicon-on-insulator (SOI), or epitaxial thin films, prepared by molecular beam epitaxy (MBE), or metal organic vapour phase epitaxy (MOVPE). Arrays of lateral nanowires can be prepared by fabricating gratings or line structures in the resist material and transferring the grating pattern to the substrate through the use of an appropriate etch process. Figure 5 displays a TEM image of a cross-section through a 10 nm wide Si nanowire fabricated from SOI using 193 nm immersion lithography.

Similarly, vertical nanowires may be prepared from bulk or layered substrates by using a resist mask consisting of dot or polygonal structures with maximum lateral dimensions below 100 nm and transfer of the mask pattern deep in to the substrate, again using an appropriate anisotropic etch process.[138]

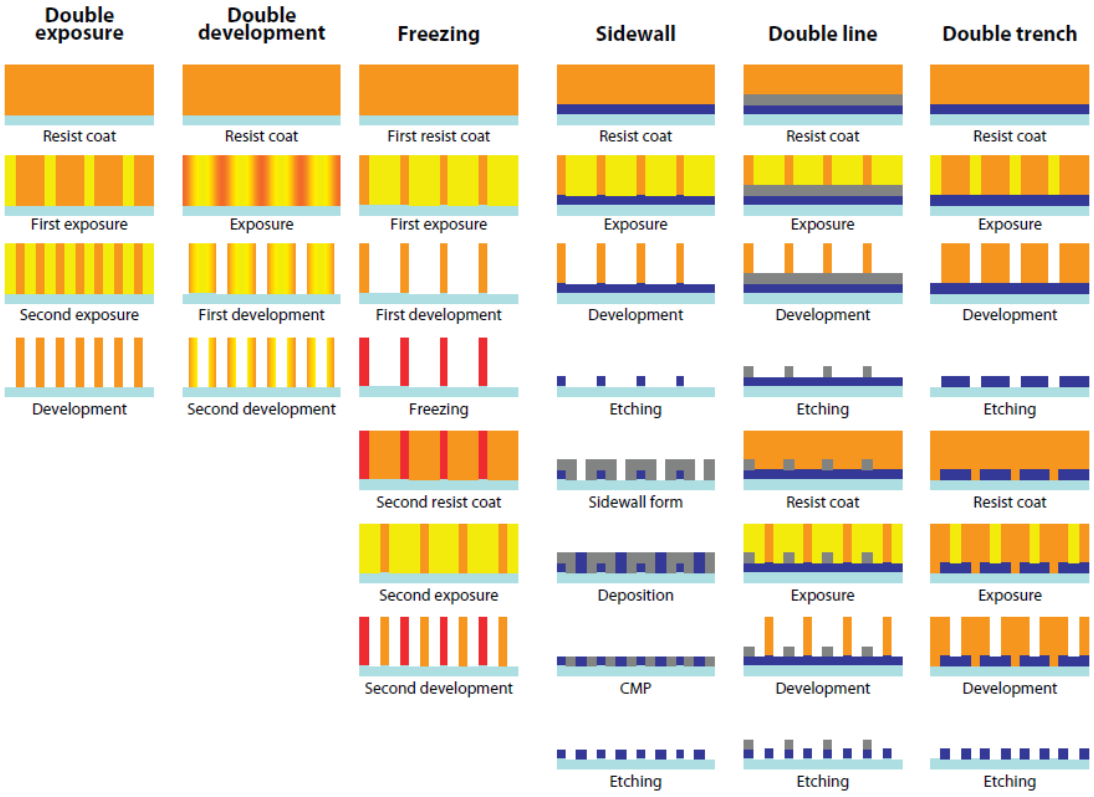


Figure 6. Schematic of a number of approaches for double-patterning lithography. CMP, refers to chemical mechanical planarisation.[128]

Inductively coupled plasma (ICP) and reactive ion etch (RIE) techniques are most commonly used for pattern transfer, although anisotropic wet etch and metal assisted etch (MAE) procedures have also been used.[138,139]

3.2. Next Generation Lithography: Electron Beam Lithography and Competing Techniques

A number of lithography processes are being considered to extend lithography scaling beyond current UV lithography capabilities, for semiconductor device manufacturing. These techniques include, electron beam lithography (EBL),[124,140,141] nanoimprint lithography (NIL),[142,143] XRL,[144,145] EUV lithography,[146,147] scanning probe lithography (SPL),[148] ion beam lithography (IBL),[149,150] and electron beam induced deposition (EBID) lithography.[151–153] EBL is at the heart of many of these techniques, including the optical lithography processes. EBL is generally used for the fabrication of high-resolution photomasks for DUV, EUV and XRL. NIL stamps are also produced using EBL direct-write processes. EBID lithography is essentially an EBL process that incorporates the use of a gas injection system which disperses a gaseous precursor that decomposes under the electron beam and directionally deposits on the substrate surface forming a mask. As such, current and future VLSI manufacturing is heavily dependent on the development of EBL processes and instrumentation. EBL has been shown to be capable of producing sub-10 nm features at sub-20 nm pitches.[154,155] Figure 7 displays examples of high-resolution EBL processes used to produce line-widths as small as 4.5 nm at pitches as low as 9 nm.

However, the primary concern with the implementation of EBL techniques in HVM is the low throughput of wafers due to the exposure times required for full wafer layouts. Exposure times depend on several factors which include the tone of the resist, the area of the wafer to be exposed, the electron beam current, electron energy, and the sensitivity of the resist (electron dose required to completely chemically alter the resist).[129,156] Resist technology may have a significant role to play in the reduction of EBL exposure times. Increasing the resist sensitivity will significantly reduce the required time for exposure; however, increased sensitivity should not compromise the ultimate resolution of the resist. Hydrogen silsesquioxane (HSQ), the smallest member of the polyhedral oligomeric silsesquioxane (POSS) family, is an example of one of the highest resolution negative-tone EBL resists. However, HSQ exposure doses are considered too high for use in HVM. Chemically amplified resists (CARs) have been developed with significantly increased sensitivity with respect to HSQ, but these resists offer lower ultimate resolution. The field of EBL resist research is an active one and recent demonstrations of EBL using analogues of HSQ with increased electron beam sensitivity are promising.[157]

Multi-beam EBL systems are under development which will increase wafer throughput either through beam-splitting techniques, or through the use of instruments with multiple electron sources, however, the technology is still not mature and as

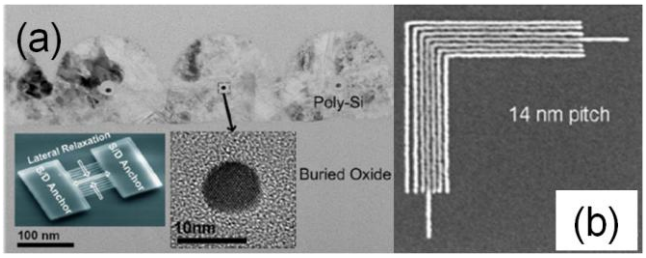


Figure 7. High resolution features produced by EBL: (a) 8 nm diameter strained n-Si nanowires produced using a hydrogen silsesquioxane (HSQ) EBL process for gate all-around FET devices and (b) nested lines at a pitch of 14 nm.[124,155]

such has yet to be implemented on a HVM scale.[158] Lee *et al*.[159] have reported a particularly innovative example of multi-beam EBL using a Si crystal as an electron beam mask (figure 8). A transmission electron microscope (TEM) was used to create arrays of electron beams where the shape and separation of the beams was governed by the crystal structure and crystal orientation of the mask with respect to the incident electron beam. Atomic resolution images of the Si crystal lattice were magnified and projected onto HSQ films creating arrays of nanostructures in the resist. This technique shows promise for increased throughput where periodic arrays of simple nanoscale structures are desired.

Arrays of dot structures produced by EBL can be used to fabricate vertical nanowire arrays through the use of a deep anisotropic etch.[160–162] The use of an etch resistant material to form the dot structures is paramount to facilitate deep etching to form high aspect ratio nanowires. Typically, Al_2O_3, Al, and SiN_x, have been used as etch masks for vertical Si nanowire fabrication. Figure 9 shows an SEM image of arrays of vertical Si nanowires produced using an EBL process.[162]

Commonly encountered issues for EBL processes include electron-substrate or electron-resist interactions and surface charging of insulating substrates. Electron-substrate and electron-resist effects can be grouped into three sub-classes, forward scattered electrons (scattering angle < 90°), backscattered electrons (scattering angle > 90°) and secondary electrons.[129] Forward scattered electron effects are most important within the resist as electrons which are forward scattered in the substrate have little contribution to resist exposure.

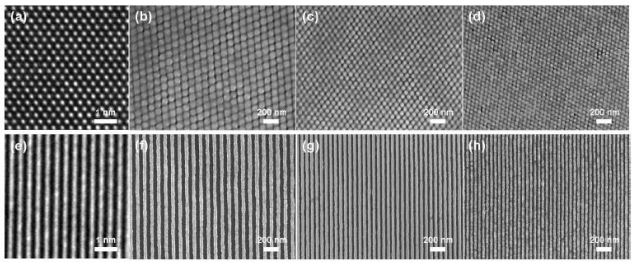


Figure 8. Arrays of HSQ nanostructures produced using projection of the atomic lattice of a Si crystal (a) and (e) in a TEM. SEM images (b-d) and (f-h) respectively show the critical dimension and pitch scaling of the structures with increasing TEM magnification, 160 × (b,f), 200 × (c,g) and 300 × (d,h).[159]

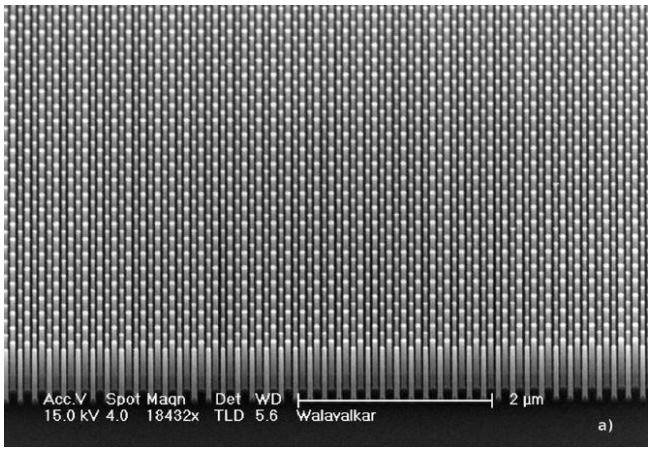


Figure 9. SEM image of an array of 50 nm diameter Si nanowires etched into a Si wafer. A sputtered Al_2O_3 hard mask, patterned by EBL was used as the Si etch mask.[162]

Forward scattering can be minimised by using a high accelerating voltage (higher energy electrons) or a thinner resist layer. Backscattered electron exposure effects are more prominent for high atomic weight (*Z*) materials and as such are more commonly a consequence of electron-substrate interactions. Secondary electrons are the primary electron-solid interaction, and as such they make the largest contribution to resist exposure. Importantly, although secondary electrons are responsible for most of the resist exposure, their path length in the resist is short, typically < 10 nm, and as such these electrons do not have a significant contribution to proximity effects. Proximity effects can largely be attributed to backscattered electrons which experience large angle scattering and can commonly travel large distances laterally in the substrate and resist (~1 µm for 10 keV incident beam energy). Proximity effects due to electron-solid interactions can be corrected through careful modelling of electron scattering, typically as a point spread function (PSF) and the use of appropriate electron dose contour maps based on these models.[158,163] Experimentally derived data can also be used to develop PSFs for use in proximity effect correction (PEC). PEC is particularly important for the exposure of high density features and large structures where electron scattering effects become prominent.

Charge accumulation at the surface of insulating substrates is another factor that can dramatically affect resolution and alignment in EBL. Surface charging results in an associated electric field at the substrate surface which acts to deflect the incident electron beam with detrimental effects on the EBL process. Surface charging effects can be avoided through a number of avenues. Deposition of a thin layer of conducting material (Au, Cr, Al or conducting polymers) atop the resist can remove surface charging effects, with the drawback of the introduction of an additional layer of material in the EBL process. Conducting polymers such as ESPACER (Showa-Denko), a member of the polythiophene family, are preferable to metals such as Au due to their superior process compatibility.[129] ESPACER is soluble in water and as such can be easily removed following electron beam exposure and prior to developing the resist, where as complete removal of Au and similar metals requires harsh etching conditions which may alter

the resist, and the substrate. Much work has been performed in the field of electron-solid interactions and as such modelling and correcting undesired electron-solid interactions is now possible.[163] However, until EBL sample throughput times are reduced to acceptable levels for HVM, EBL will remain confined to tasks such as quantum device demonstration, NIL stamp fabrication and high-resolution photomask fabrication. Development of multiple beam EBL systems will improve the throughput of EBL tools, however such systems are still unproven and require further investment to compete with their optical counterparts for a role in next generation VLSI manufacturing.[126,158,164,165]

Electron beam induced deposition (EBID) can be used as a lithographic tool to produce sub-10 nm features.[152,166] As stated previously, EBID essentially involves introducing a gaseous precursor species into the path of an electron beam in an EBL system. The precursor decomposes upon electron beam exposure and directionally deposits the solid decomposition product, typically a metal such as W, or Pt, on the substrate. EBID is a capable lithographic tool for the production of devices on a small scale.[151] However, EBID suffers from inherent drawbacks such as metal contamination of device structures and low throughput. Consequently, EBID is more suited to small-scale applications such as photomask defect repair.

Lithography using focused beams of ions such as He^+, Ga^+ and Ne^+ has been used to demonstrate structures with sub-10 nm critical dimensions.[149] Ions of He, Ga and Ne are significantly larger and heavier than electrons and as such travel shorter distances in resist materials than electrons. Consequently, ion beam lithography is a promising technique for generating a high-density of structures in a suitable resist material. Furthermore, Ne^+ ions have been shown to transfer energy to HSQ resist more efficiently than electrons, thus facilitating high-resolution pattern generation at low exposure doses. In fact, Ne^+ IBL has demonstrated exposure efficiencies ~1000× greater than electrons with equivalent landing energies.[150] Whilst Ga^+ focused ion beam (FIB) systems are widely available and used for a range of applications such as TEM sample preparation, optical lithography mask repair and cross-sectional analysis, He^+ and Ne^+ ion beam system are far less common. He^+ ion microscopy (HIM) has gained significant attention in recent years as it is not susceptible to surface charging effects commonly encountered in electron microscopy, and as such may be used to acquire surface sensitive images of insulating materials.[167] HIM may thus be particularly suited to lithography on insulating substrates. Although ion beam lithography techniques offer noticeable advantages over electron beam lithography in terms of reduced proximity effect, increased energy transfer efficiency to the resist material and reduced charging effects, significant concerns still remain with regard to ion beam stability over the timescales required for full wafer exposures.[167,168] Consequently, ion beam lithography is a very promising technique for next generation lithography, but requires significant investment for scalability of the technique for HVM and for techniques such as mask production where exposure times on the order of several hours will be required.

Many of the issues associated with the implementation of EUV, and XRL techniques in HVM have been discussed in the previous section. NIL is a mechanical lithography technique whereby a stamp or template created in a robust material, usually Ni or Si, for thermal NIL; PDMS for soft NIL; and quartz for step and flash NIL (S-FIL a trademark of Molecular Imprints Inc.), is pressed into a deformable resist on a substrate. The resist is then hardened so that when the template is removed the contours of the template are transferred to the resist. The patterned resist can then be used for subsequent pattern transfer procedures. NIL is a relatively inexpensive technique when compared to other nanolithography techniques and has demonstrated the production of very fine features at high areal densities.[142] Feature sizes as small as 6 nm have been demonstrated, with half-pitches below 20 nm also readily achievable.[169] Furthermore, NIL can be used to directly pattern interlayer dielectric (ILD) materials such as low-*k* silsesquioxanes (SSQs) thus reducing the number of process steps required in the dual-damascene process typically used to form metallic interconnects.[170,171] However, there are outstanding issues concerning overlay accuracy, defect density and throughput. Furthermore, NIL processes are mask specific and as such must be tuned to achieve the optimal resist volume for specific mask designs, which can limit the technique where large area patterns are required. Additionally, NIL may not be compatible with pattern transfer to porous low-*k* materials used as back-end-of-line (BEOL) insulators, which are inherently brittle and may be deformed by the pressure applied during NIL.[142]

Scanning probe lithography (SPL) encompasses a range of lithography techniques including, dip-pen nanolithography (DPN), local oxidation nanolithography (LON), atomic force microscope (AFM) lithography and scanning tunnelling microscope (STM) lithography. Common to these techniques is the use of a scanning nanoscale probe, typically an AFM tip, to pattern a resist or substrate directly.[172,173] In the case of DPN an AFM tip is used to transfer a material to the surface which can subsequently act as an etch mask or may act as an active device component itself. LON is used to locally oxidise a material thus forming a patterned surface oxide by applying a voltage bias between a conductive AFM tip and the substrate material in the presence of water vapour to induce localised oxidation of the substrate through electrochemical reaction with the water vapour.

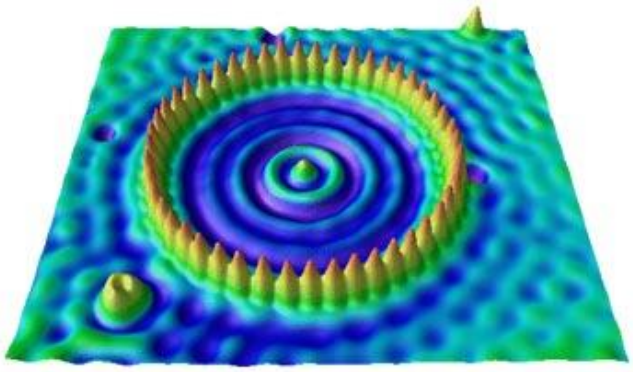


Figure 10. False colour STM image of a quantum corral structure created by the atomic manipulation of 48 Fe atoms on a Cu {111} surface. The Fe ring confines the surface electron wavefunction of the defect free Cu surface within.[174]

AFM lithography can operate in contact mode or non-contact mode. Contact mode AFM lithography in volves the mechan-

ical patterning of a substrate much like NIL. An AFM tip can be used to scratch or stamp a pattern into a resist material or into the substrate itself. Non-contact mode AFM can be used to pattern materials through local oxidation of the substrate surface as in the case of LON, through local heating of a resist material using a heated AFM tip, or through local electron exposure via a field emission AFM tip.[172,173] STM lithography has been used to produce nanostructures by a variety of means. Scappucci *et al*. have reported the use of STM to selectively dope regions on a H-terminated Ge (100) surface where H atoms have been removed by STM, thus creating doped nanowire structures.[148] STM can also be used for the individual manipulation of atoms on a surface to produced quantum structures, such as the quantum corral reported by Crommie *et al*. in 1993 (figure 10).[174] SPM lithography techniques are inherently slow even when multiple probes are used.[175] As such, low throughput will prevent such techniques from being used in HVM.[173]

3.3. Top-Down Semiconductor Nanowire Fabrication Outlook

Top-down semiconductor lithography processes have dominated the area of semiconductor device definition and placement for decades. However, as the density of devices on a chip continues to scale significant difficulties are encountered. Techniques such as EBL and XRL with significantly reduced wavelengths, may readily achieve the high densities of devices desired by the semiconductor industry, however, there are a number of difficulties associated with the integration of these short wavelength techniques in VLSI manufacturing. Consequently, it seems increasingly likely that current top-down processes may have to 'reach out' to a bottom-up technology to achieve the future goals of the semiconductor industry. Integration of bottom-up fabricated VLS nanowires in VLSI manufacturing may be a step too far in the short term as the VLSI industry is geared toward device fabrication in the plane of the Si wafer, and integration of vertically oriented and stacked FETs will require extensive design and process reconfiguration. Consequently, a bottom-up technique that facilitates continued scaling in the plane of the substrate may be a more likely first step toward the integration of a bottom-up technique in VLSI manufacturing. One such bottom-up technique is that of directed self-assembly of block copolymers.

4. Integration of Bottom-Up and Top-Down Processes for Nanowire Array Fabrication

4.1. Directed Self-Assembly

Directed self-assembly (DSA) is an advanced lithographic process based on the self-assembly of block copolymer (BCP) thin films. BCP self-assembly involves the bottom-up, microphase separation of chemically different blocks within the BCP. Typically, A-B diblock copolymers are used for DSA, where an A-B diblock copolymer consists of a linear chain of a monomer A, joined at one end by a covalent bond, to a linear chain of monomer B. When the two blocks, A and B, are sufficiently chemically distinct from one another, they can microphase separate so as to minimise the interaction of blocks A and B, whilst maximising the interaction between similar blocks. The chemical interaction of the two blocks in a BCP is often quantised by the Flory-Huggins interaction parameter (χ) for that BCP system which is related to the enthalpy of mixing for that polymer system.[176] Self-consistent mean field theory has been used to generate theoretical phase diagrams for diblock copolymer melts (figure 11).[177] Mean field phase diagrams are presented as a plot of χN against f, where N is the degree of polymerisation of the BCP and f is the volume fraction of a reference block in the BCP. χN is representative of the thermodynamic driving force for microphase separation within the diblock copolymer melt. χ represents the enthalpic component and is inversely related to temperature and directly related to polymer chain length, whilst N represents the entropic component, which depends on the chain length dependent number of conformations that can be adopted by the polymer.

Figure 12 shows schematic examples of phase morphologies within a microphase separated A-B diblock copolymer with increasing number fraction of block A (f_A).[176] Lamellar and hexagonally close packed cylinder phases of BCPs are typically used in DSA, where the phase of the BCP can be controlled through selection of appropriate polymer fractions in the BCP, and suitable polymer chain lengths. The microphase separation of BCPs can be guided both chemically and physically through the use of careful templating techniques, *i.e.* directed self-assembly. Physically guided microphase separation of a BCP is often termed graphoepitaxy. DSA of lamella forming BCPs by graphoepitaxy, is generally achieved by creating trenches in a substrate where the trench width is an integer multiple of the block length.[176,178]

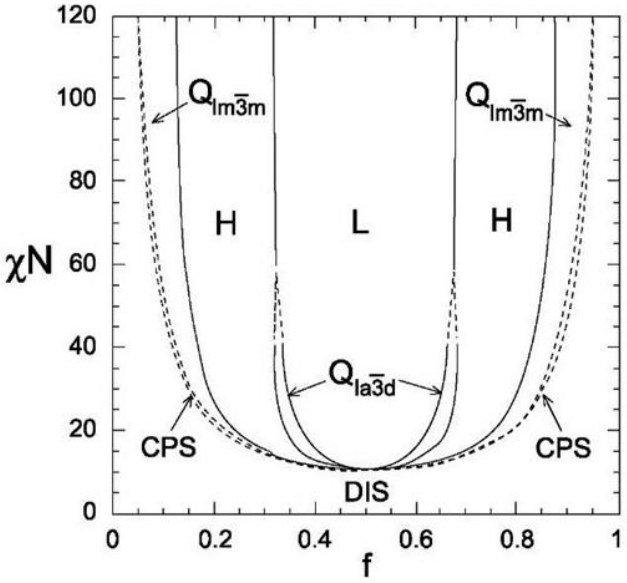


Figure 11. Phase diagram of a diblock copolymer as predicted by self-consistent mean field theory. Phases are labelled L (lamellar), H (hexagonally arranged cylinders), $Q_{Ia\bar{3}d}$ (bicontinuous $I_{a\bar{3}d}$ cubic), $Q_{Im\bar{3}m}$ (body centred cubic spheres), CPS (close packed spheres), and DIS (disordered).[177]

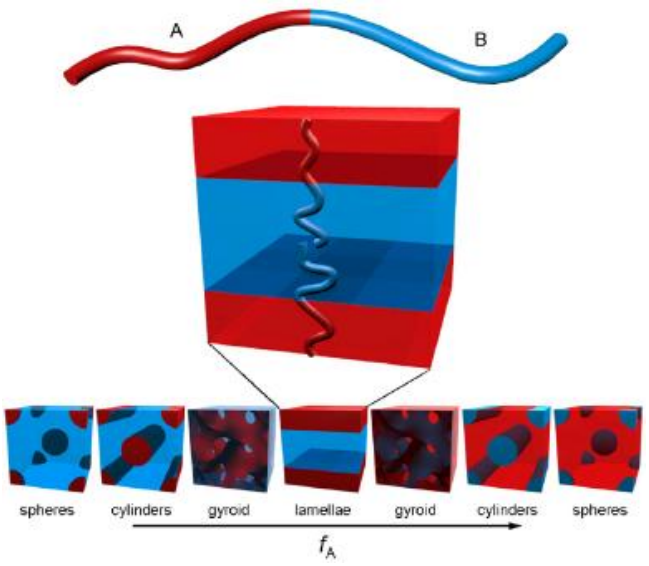


Figure 12. Schematic representation of the microphase morphologies of an A-B diblock copolymer with increasing number fraction of block A from left to right.[176]

Similarly, chemically guided microphase separation of a BCP is termed chemical epitaxy. DSA by chemical epitaxy is achieved using a substrate that has been chemically patterned to induce ordering during microphase separation of the BCP.[179,180] Consequently, DSA by both graphoepitaxy and chemical epitaxy is heavily dependent on conventional lithographic techniques such as those outlined in Section 3.

Ordered diblock copolymer films produced by DSA can be used as high-resolution etch masks for semiconductor nanowire fabrication. As such, DSA has gained significant interest in the field of nanolithography in recent years. DSA offers a number of advantages over conventional optical or direct-write lithography techniques. Firstly, DSA can achieve sub-lithographic resolution by pattern multiplication, thus increasing the density of features within low density patterns produced by conventional optical or mask-less lithography techniques.[181–184] Implementation of a pattern multiplication process in current lithographic methods for VLSI manufacturing would remove the necessity for complicated techniques such as double patterning and high density lithography.[179] DSA by chemical epitaxy has also been shown to exhibit self-healing properties, whereby defects in templates used to guide microphase separation are corrected in the extended pattern of the mask produced by DSA.[185,186] Additionally, DSA is a relatively inexpensive technique, depending on the process used to guide microphase separation. DSA has the potential to offer very high throughput if it were incorporated with current optical lithography processes, and can readily achieve sub-20 nm critical dimensions by controlling the molecular weight of the polymer blocks in the BCP. Furthermore, DSA has been shown to be capable of producing device specific geometries such as bends, T-junctions and jogs.[181,187] Parameters such as line-edge-roughness (LER) for DSA masks are determined by the quality of the microphase separation and associated guiding technique as well as the quality of the etch used to selectively remove one of the blocks of the BCP.

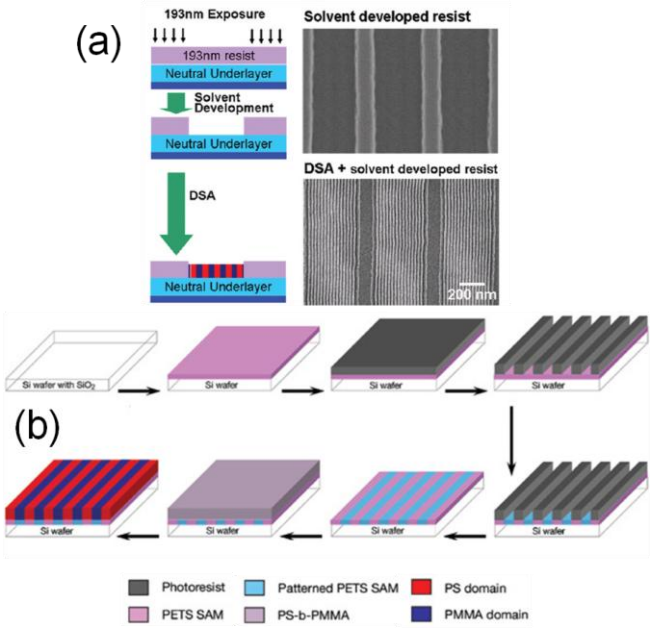


Figure 13. Typical process flows used to produce DSA of BCPs via (a) graphoepitaxy and (b) chemical epitaxy, respectively.[180,188]

LER values as low as 1.95 nm (3σ) have been reported for lines produced by DSA of a lamella forming BCP.[179]

However, there are a number of outstanding concerns associated with DSA as a lithographic technique. The primary concern with the process is high defect density, attributable to contamination, BCP purity, BCP molecular weight distribution, chemical uniformity of the substrate surface and defects within the DSA guiding template. Substrate surface uniformity is known to be a critical factor in achieving large areas of uniformly oriented microphases in BCP films. Consequently, there has been a large research investment in the study of self-assembled molecular monolayers and polymer brush layers to tailor the substrate surface energy, and BCP wetting, for BCP self-assembly.[179,189–192] Additionally, BCP layers are often prepared as thin monolayers of the microphases *e.g.* a single layer of substrate coplanar cylinders in the case of PS-*b*-PDMS, and often have poor etch resistance, *e.g.* PMMA, PS.

Whilst the defect density in DSA masks is improving with increased research investment, DSA processes still require further optimisation before they can be integrated into a HVM landscape. Figure 14 shows an example of relatively large area patterning achieved via the graphoepitaxy of PS-*b*-PDMS.[182] Chemical epitaxy DSA techniques can 'heal' defects present in the guiding template; however, chemical epitaxy has not yet demonstrated pattern multiplication to the extent of graphoepitaxy based techniques. Thus, it is likely that each approach, chemical epitaxy and graphoepitaxy, will find their own niche application within the semiconductor industry. Development of DSA masks with sufficient etch resistance will depend on the specific process requirements. PS-*b*-PDMS for example, is a promising material for DSA when a high etch resistance to Si etchants is required. PDMS has an inorganic Si-O backbone and as such offers superior etch resistance relative to organic polymers.

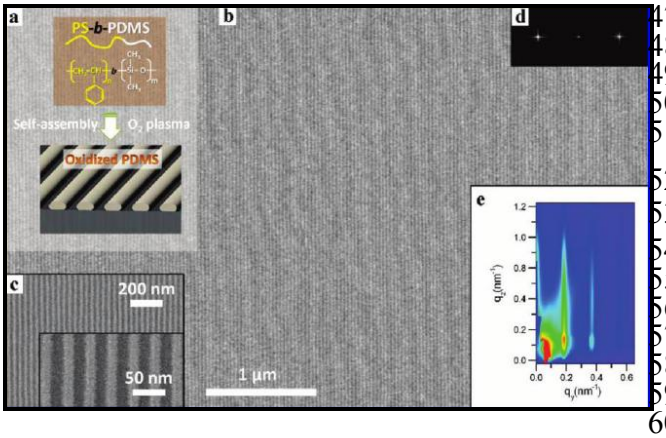


Figure 14. (a) A schematic of the structure of PS-*b*-PDMS and the structure formed by DSA. (b) SEM image showing large-scale alignment of PDMS lines produced by the graphoepitaxy of PS-*b*-PDMS within 10 μm wide, PDMS brush coated trenches etched in a Si wafer. (c) Higher magnification images of the aligned PDMS lines. (d) FFT of the image in (b) consistent with excellent long-range ordering. (e) Grazing incidence small angle x-ray scattering (GISAXS) pattern generated from a 1 cm^2 area of the PDMS line pattern.[182]

The outlook for DSA is promising. DSA has already demonstrated the requisite resolution capabilities for continued device scaling outlined within the International Technology Roadmap for Semiconductors (ITRS), defect density levels are dropping with continued research investment and issues regarding production of device specific geometries appear to be resolvable using chemical epitaxy approaches.[179] LER and CD control issues also need to be addressed to meet ITRS specifications.[179] Theoretical models predict LER to be related to $\chi^{0.5}$, in which case, BCP systems with high χ values such as PS-*b*-PDMS (χ ~ 0.26 at room temperature) are worthy of further investigation.[182]

Self-assembly of cylinder and sphere forming BCPs has also been used to produce ordered arrays of metal nanoparticles by both additive[193] and subtractive[194], processes. These metal nanoparticles may then be used to produce epitaxial growth of semiconductor nanowires by means of the relevant techniques outlined in Section 2. Furthermore, the metal nanoparticles may be used as etch masks to produced ordered arrays of vertical nanowires by a top-down approach. The use of BCP films to template catalysts for epitaxial nanowire growth and to template hard masks for top-down vertical nanowire array formation is an example of a synergistic process, employing both bottom-up and top-down methods. This synergistic process is to date, a poorly explored application of BCP lithography which warrants further investigation.

DSA is a promising blend of top-down and bottom-up techniques for advanced lithography applications. DSA allows a route to increased pattern resolution and feature density relative to conventional optical lithographic means, and whilst concerns still exist over LER, CD control and reproducibility, these concerns are gradually being improved by continued advances in the field. DSA depends on conventional lithography techniques such as optical lithography, interference lithography and EBL to form guiding templates to direct the self-assembly of BCPs and as such it will remain a complementary lithography technique. However, if and when the issues associated with DSA are resolved, this lithography technique may alleviate the growing demands on optical lithography and EUV for continued device scaling, thus extending the use of current optical lithography techniques in VLSI manufacturing.

4.2. Lithographic Catalyst Placement for Bottom-Up Nanowire Growth

EBL is a suitable tool for the preparation of ordered arrays of metal nanoparticles by subtractive or additive processes. Ordered arrays of metal nanoparticles can be readily prepared using a positive tone EBL process to generate a metal lift-off mask.[25,88,97,195] This process can be used to produce epitaxial nanowire growth via a VLS-type mechanism through careful control of the metal substrate interface, and choice of an appropriate substrate material, using nanowire growth methods such as those outlined in section 2. Coupling EBL and self-assembly of BCPs allows the production of defect free high-density arrays of dot structures.[196]

Similarly, phase shift lithography and interference lithography have been shown to be capable of producing very fine dot structures for the fabrication of metal nanoparticle arrays.[197,198] Metal nanoparticle arrays formed by these methods, too, could be used for the fabrication of nanowire arrays by bottom-up means.

4.3. Nanosphere Lithography

Nanosphere lithography (NSL) can be used to produce ordered arrays of vertical nanowires. NSL uses the bottom-up self assembly of spherical particles, such as polystyrene spheres, to create dot/anti-dot arrays on the surface of a substrate, which then may be used to transfer the pattern to the substrate creating structures such as vertically aligned nanowire arrays.[21,199–201] NSL can be used to produce arrays of vertical Si nanowires using a metal-assisted etching approach as shown in figure 15 below. Combined use of NSL and metal-assisted etching (MAE) provides a route to forming arrays of long (> 10 μm) Si nanowires which have applications in fields such as vertical ICs and solar cells (figure 15).[21] NSL can also be used to create an anti-dot array mask for the evaporation of arrays of metal nanoparticles for use as catalysts for epitaxial nanowire growth.[199]

4.4. Miscellaneous Synergistic Nanowire Fabrication Processes

A range of processes exist which use both bottom-up and top-down techniques in tandem to produce semiconductor nanowires. One example of such a technique is the supperlattice nanowire pattern transfer (SNAP) technique.[202] The SNAP technique is based on the formation of a stamp by selectively etching one of the layers in a superlattice material grown by a bottom-up epitaxy technique, such as MBE. Angular deposition of a metal on the etched superlattice then allows creation of a metal stamp which is pressed against the material of choice producing a metal grating which acts as an etch mask for the fabrication of nanowire arrays by pattern transfer.

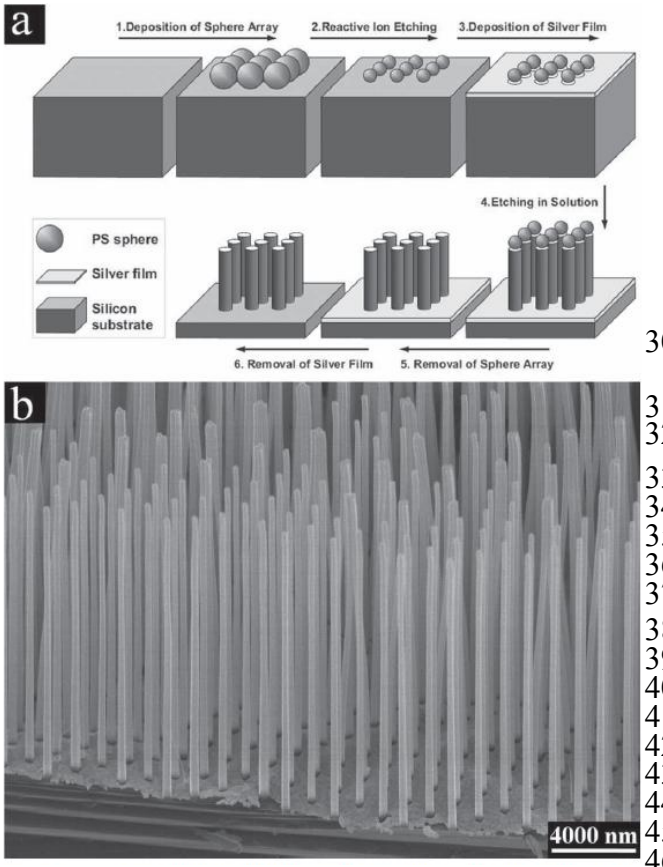


Figure 15. Schematic of NSL process for the fabrication of vertical Si nanowire arrays via MAE.[201,203]

Figure 16, shows a schematic of the SNAP process. The SNAP process has been used successfully to produce arrays of Si nanowires from SOI, as well as metal nanowires formed directly from the stamp. However, the technique is limited in terms of the geometries of the structures that can be produced, and the complexity of the process for large-scale nanowire fabrication. Furthermore, the SNAP technique is susceptible to many of the pitfalls associated with NIL outlined in Section 3.2. NIL can be used to created arrays of metal nanoparticles for bottom-up nanowire growth.[204] This process involves imprinting a bilayer positive-tone resist, developing the imprinted resist and evaporating a metal layer to produce arrays of metal nanoparticles by lift-off. The metal nanoparticles can subsequently be used as catalysts for nanowire array production by standard nanowire growth procedures.

AAO membranes with HCP pore arrangements are formed by a bottom-up process, as discussed in Section 2.2. When prepared as thin films, these ordered porous AAO membranes can be used as masks to produce patterned metal films on Si substrates for MAE of Si, producing ordered arrays of vertical Si nanowires.[205,206] MAE techniques usingpatterned metal layers are successful at producing dense, ordered arrays of vertical nanowires with high aspect ratios. However, as with all MAE techniques, the nanowires produced have rough sidewalls thus inhibiting their use in logic applications where surface scattering of charge carriers is a significant drawback.[201,207]

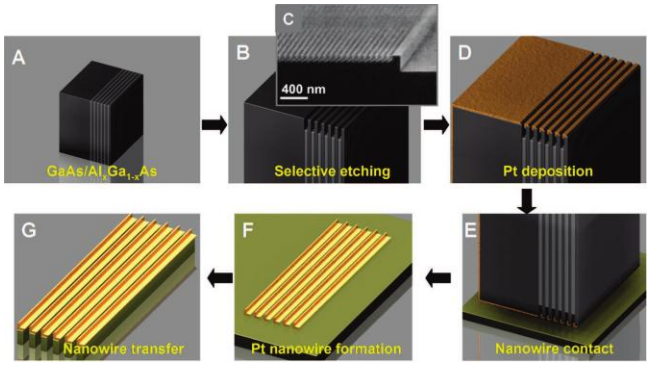


Figure 16. Schematic of the SNAP process for production of aligned nanowires.[202]

Nanowires produced by these methods are likely to find applications in solar cell, thermoelectric generator, sensor or battery anode applications where the increased surface area of nanowires with rough sidewalls may be beneficial to device performance.[208,209]

Ion track etched membranes are an example of another nanowire template material. These membranes are formed in a top-down process by ion etching of a polymer material, producing cylindrical or tapered pores. Infilling ion track etched membranes by methods such as electrodeposition can produce arrays of nanowires.[210] Whilst this method can be used to produce some interesting network structures (figure 17), it is unlikely to find use in VLSI manufacturing due to the complexity of the process and the difficulty producing single-crystalline materials within these membranes.

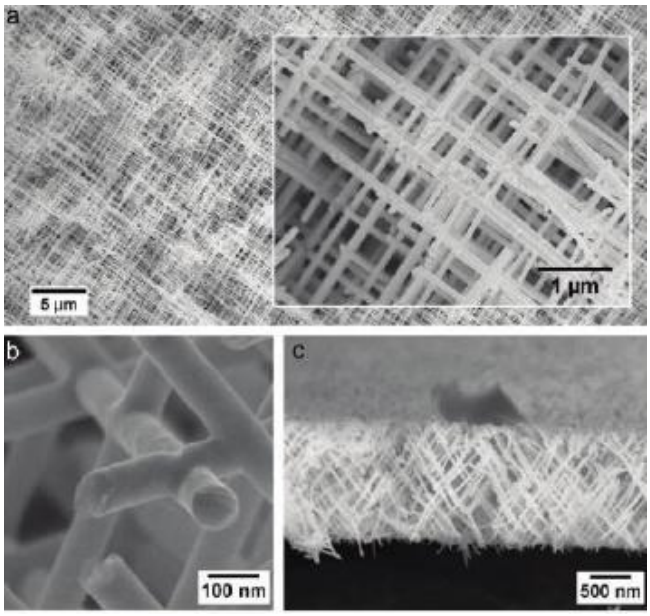


Figure 17. SEM images of polycrystalline Pt nanowire networks produced within ion track etched membranes: (a) low magnification SEM images of Pt nanowire networks, (b) high magnification SEM image of nanowire junctions and (c) cross-section of a nanowire network composed of 35 nm diameter nanowires.

5. Emerging Semiconductor Nanowire Materials

5.1. High Mobility Materials for Next Generation CMOS Devices

High charge carrier mobility materials have been subject to significant research investigation in the past few decades. These materials offer increased transconductance relative to Si, and as such, devices constructed from these materials may achieve similar drive current at lower power, or operate as high performance devices at equivalent power, to current Si devices.[211] Many materials are under consideration for integration in future CMOS devices due to their increased charge carrier mobility relative to Si.[12,211–213] Ge, for example, exhibits hole mobility over four times that of Si, and as such is a strong contender for use in future p-FET devices. Likewise, InSb, InAs and graphene demonstrate massively increased electron mobility relative to Si.[212,214] However, these high mobility materials are not without their drawbacks. Often, Ge and III-V materials possess complex native oxides with poor chemical or electrical properties for device fabrication.[112] GeO_2, a component of the complex native oxide on Ge crystals, is water soluble and as such must be removed or capped with a more suitable material to facilitate processing steps involved in device manufacturing. Additionally, GeO, another component of the native oxide on Ge, desorbs at temperatures above 400 °C, which may result in detrimental effects on overlying layers during annealing steps in device manufacturing.

Similar difficulties have been reported for III-V materials such as GaAs and $In_{1-x}Ga_xAs$, whose complex native oxides prevent the formation of a stable semiconductor-insulator interface. The result is a high density of interface states at the semiconductor-insulator interface in the gate stack.[111,215] Interface states often lie near the mid band-gap of the semiconductor and can lead to Fermi-level pinning at the semiconductor surface. Fermi-level pinning can result in a number of detrimental effects on device performance, including, rectifying characteristics in metal-semiconductor contacts, and depletion of free charge carriers in the device channel at the semiconductor-insulator interface.[104,216] Interface states result from unsaturated surface atoms, which act as charge acceptors and donors at the semiconductor surface. Consequently, reduction of the density of interface states is dependent on the formation of a stable and saturated semiconductor surface. There have been significant investigations into improvement of the electrical and chemical interfaces with these materials to facilitate their integration within next generation CMOS devices. The use of a capping Si layer of the order of a few monolayers thickness has been successful in reducing the density of interface states (D_{it}) in GaAs from 10^{13} cm^{-2} eV^{-1} to 10^{11} cm^{-2} eV^{-1}.[215] Similarly, deposition of SiO_2 directly on an untreated Ge surface results in a relatively high D_{it} of 10^{13} cm^{-2} eV^{-1}, whilst formation of a $Ge_{(100)}/GeO_xN_y/HfO_2/Pt$ gate stack produced a D_{it} of 3×10^{11} cm^{-2} eV^{-1}.[111,112] A further promising route toward improving the interface of inorganic semiconductor materials with gate-dielectric layers may be through the use of an appropriate organic dielectric material chemically tethered to the semiconductor. Extensive research has been pursued in the field of chemical functionalisation of Ge and III-V surfaces with high coverage of organic ligands.[217–219] High-*k* organic gate-dielectrics have been investigated primarily for use with organic FET devices, and have demonstrated competitive levels of performance when compared with current VLSI devices.[220] Consequently, the molecular tethering of high-*k* organic molecules directly to these surfaces may allow a route to high-*k* insulating layers with low D_{it}, thus improving device performance.

Graphene has demonstrated impressive electrical performance in reported device applications with charge carrier mobilities as high as 230000 $cm^2V^{-1}s^{-1}$.[221] However, there are a number of outstanding concerns with regard to the integration of graphene in VLSI manufacturing. Firstly, pristine graphene is a zero-gap semi-metal and as such exhibits poor switching behaviour in logic device applications. Significant efforts have been made to introduce a large and reproducible band-gap into graphene. These efforts have included quantum confinement of graphene within graphene nanoribbon (GNR) structures, doping, edge functionalisation and use of bilayer graphene.[221] Additionally, there are serious concerns regarding graphene processing for device fabrication. Production of large area, single layer graphene is a challenging task, and handling such a delicate material has associated difficulties. Metals and gate-oxides exhibit poor adhesion to graphene and graphene layers are extremely vulnerable to plasma induced damage.[222] Despite the many concerns regarding implementation of graphene in CMOS manufacturing, it maintains a massive research impetus and is firmly implanted on the ITRS for continued investigation.[12]

Similarly, carbon nanotube (CNT) structures have been investigated heavily for use as FET semiconductor channels and as metallic interconnect materials.[223] The primary difficulty with CNT material preparation for FET and interconnect applications is controlling the electronic band structure of the material, which is dependent on CNT growth direction, and diameter.[224] Furthermore, CNTs are subject to alignment and integration issues inherent to bottom-up nanowire and nanotube synthesis techniques as outlined in section 2.2.

The introduction of high-*k* dielectric materials in the gate stack of the active devices in VLSI manufacturing in recent years has paved the way for the introduction of high mobility, non-Si materials for FET applications. Materials such as Ge and III-Vs have long been held back by issues associated with their complex native oxides. However, the transition of the semiconductor industry from a SiO_2 gate dielectric to materials such as HfO_2, Al_2O_3 and ZrO_2,[59] has reignited interest in these high mobility materials. Consequently, there has been heavy research investment in the preparation of high-*k* materials on high mobility materials in recent years.[111,112]

6. Nanowire Fabrication Outlook

The continued scaling of semiconductor devices in the VLSI industry has created a landscape where the introduction of nanowire or nanoribbon devices into mass production seems increasingly likely. As the density of semiconductor devices in VLSI architectures increases there has been an associated shift of the semiconductor channel from a planar orientation, to the recently developed fin structure where the semiconductor channel is raised above the surface of the Si wafer. A natural progression from the finFET or tri-gate structure would appear to be a nanowire structure, be it lateral – parallel to the substrate – or vertical. The benefits of nanowires have been highlighted for a number of years now. Semiconductor nan-

owires allow production of GAA devices which offer superior control of the device channel and thus improved switching speed and on/off ratios. A nanowire structure can also be used to create quantum well, core-shell structures with improved electrical transport properties relative to standard structures. Nanowires may also incorporate strain, a prerequisite in current VLSI devices[16,225,226], through the incorporation of dopants or a lattice mismatched shell material.[227,228]

The exact fabrication route to future semiconductor nanowire-based integrated circuits is as yet, unclear; however, it is quite probable that the route will incorporate both top-down and bottom-up techniques in tandem to allow a scalable path to nanowire integrated circuit fabrication. Bottom-up nanowire growth processes allow routes to structures that may not be produced by top-down means, and also may allow production of exotic channel materials that may not be accessible in the bulk wafer form. Bottom-up grown semiconductor nanowires often exhibit faceted surfaces that may not be achieved by top-down fabrication. Control of the crystal surface facets formed during nanowire growth, may allow control over the density of interface states formed at nanowire surfaces, which is particularly important for Ge and III-V materials to develop improved device performance. Top-down processes such as optical and electron beam lithography consistently demonstrate their superiority in the nanometre control of device definition and placement. DSA of BCP films is an example of the synergistic cooperation of a bottom-up self-assembly process and traditional top-down lithography, allowing routes to aligned pattern multiplication, which is not feasible by either technique alone. As such, a conservative prediction would be that future nanowire-based electronics will be fabricated by a cooperative mix of both bottom-up and top-down processes.

Table 1, summarizes the achievable minimum feature sizes, and potential feature pitch, using a number of top-down and synergistic fabrication processes. All of the techniques listed in table 1 are suitable for the fabrication of nanowire arrays. However, the choice of a suitable technique for the fabrication of a particular nanowire system requires the consideration of all aspects of the fabrication technique, and not merely the ultimate resolution. AAO for example is usually used to prepare arrays of nanowires oriented vertically with respect to a substrate. Interference lithography is suited to the fabrication of linear arrays of nanowire structures and does not typically allow routes to arbitrary shapes and nanowire layouts such as those achievable via top-down optical lithography or direct-write charged particle lithography. Consequently, consideration of a number of fabrication techniques may be required when developing a nanowire fabrication process, and the benefits and drawbacks of each technique should be carefully weighed against one another so as to identify the technique best suited to the fabrication of the desired product.

Fabrication Technique	Minimum Feature Size	Linear Feature Pitch
Top-Down Optical Lithography	< 10 nm	< 40 nm[146]
Interference Lithography	< 15	< 25 nm[133,198]
Direct-Write Charged Particle Lithography	< 5 nm	< 10 nm[155]
NIL	< 10 nm	< 20 nm[142]
SPL	< 1 nm	< 2 nm[172]
DSA	< 5nm	< 20 nm[179,229]
AAO	< 20 nm	< 50 nm[230]
Bottom-Up EBL Synergy	< 30 nm[25]	< 500 nm
NSL	< 15 nm	~ 200 nm[231]

Table 1. Minimum feature sizes and potential minimum linear feature pitch achievable by a number of top-down and synergistic lithography techniques.

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Table of Contents Figure

Richard G. Hobbs, Nikolay Petkov and Justin D. Holmes Semiconductor Nanowire Fabrication by Bottom-Up and Top-Down Paradigms	This review article highlights the important considerations required for the continued advancement of semiconductor nanowire fabrication for next-generation field-effect transistor devices.	