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Semiconductor Nanowire Fabrication by Bottom-Up and Top-Down Paradigms

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ABSTRACT: Semiconductor nanowires have been the subject of intensive research investment over the past few decades. Their physical properties afford them applications in a vast network of active microelectronic research fields, including logic device scaling in very large scale integrated circuits, sensor devices and energy harvesting. A range of routes to semiconductor nanowire production have opened up due to advances in nanowire fabrication techniques over the last number of decades. These nanowire fabrication routes can usually be categorized into one of two paradigms, bottom-up or top-down. Microelectronic systems typically rely on integrated device platforms, where each device and component thereof can be individually addressed. This requirement for precise addressability places significant demands on the mode of fabrication processes. However, in recent years advances in bottom-up fabrication processes have opened up the possibility of a synergy between bottom-up and top-down processes to achieve the benefits of both. This review article highlights the important considerations required for the continued advancement of semiconductor nanowire fabrication with a focus on the application of semiconductor nanowire fabrication for next-generation field-effect transistor devices.

1 1. Semiconductor Nanowires

2 Semiconductor nanowires are pseudo 1-D structures where the 3 magnitude of the semiconducting material is confined to a 4 length of less than 100 nm in two dimensions. Semiconductor 5 nanowires have a vast range of potential applications¹, includ-6 ing electronic (logic devices, diodes)², photonic (laser, photo-7 detector)³⁻⁵, biological (sensors, drug delivery)⁶, energy (bat-8 teries, solar cells, thermoelectric generators)^{7,8}, and magnetic 9 (spintronic, memory)⁹⁻¹¹ devices. Semiconductor nanowires 10 can be fabricated by a range of methods which can be catego-11 rised into one of two paradigms, bottom-up or top-down. 12 Bottom-up processes can be defined as those where structures 13 are assembled from their sub-components in an additive fash-14 ion. Top-down fabrication strategies use sculpting or etching 15 to carve structures from a larger piece of material in a subtrac-16 tive fashion. The challenge of continuous microelectronic 17 device scaling to meet industry targets, e.g. 'Moore's Law' 18 and the diversification of the microelectronics industry into 19 new materials for specialized applications ('More than 20 Moore')¹², has motivated research in semiconductor nanowires 21 for the past number of decades. The massive competition for 22 a share of the global 304 billion USD semiconductor market¹³. 23 has driven the expansion of the semiconductor nanowire re-24 search area, resulting in the evolution of, new fabrication 25 techniques, innovative processes, new materials and creative 26 advancements in semiconductor nanowire device design.

27 Nanowire materials offer a number of benefits over conven-28 tional planar materials for FET applications. Firstly, nan-29 owires offer the option of creating gate-all-around (GAA) 30 architectures, which allow for more efficient control over 31 charge carriers in the channel of FET devices, thus reducing 32 short channel effects caused by drain induced barrier lowering 33 (DIBL).^{14–16} The use of multi-gate architectures such as the 34 GAA architecture, facilitates the formation of shorter channel 35 devices, and thus allows for increased device density to be 36 achieved on a given chip. Additionally, fabrication of nan-37 owires of a wide range of materials has been demonstrated 38 which may not be readily produced in wafer form.^{1,17–22}

39 This review aims to summarize and compartmentalize the 40 various approaches taken by both the bottom-up and top-down 41 paradigms in this field, whilst identifying potential spaces in 42 which both top-down and bottom-up approaches may be used 43 in tandem. Primarily, this review will focus on Si and promis-44 ing high charge carrier mobility materials for logic device 45 applications, although, as mentioned previously the nanowire 46 fabrication routes highlighted herein are also relevant to a 47 whole host of potential device applications.

48 Firstly, the major fabrication routes to produce semiconductor 49 nanowires in both paradigms will be discussed, whilst identi-50 fying recent advances and highlighting the benefits and draw-51 backs of these routes. The synergistic use of both top-down 52 and bottom-up approaches to produce structures unattainable 53 by either route alone will also be considered. Next, the most 54 promising materials for high mobility logic device fabrication 1 will be considered. The current issues with processing these 2 materials within each fabrication paradigm will also be ad-3 dressed.

4

5 2. Bottom-Up Semiconductor Nanowire Fabrication

2.1. Semiconductor Nanowire Growth Methods 6

7 Numerous routes exist to the bottom-up fabrication of semi-8 conductor nanowires. The vapor-liquid-solid (VLS) mecha-9 nism and analogues thereof, is the most commonly used route 10 to semiconductor nanowire production.^{1,23,24} The VLS mecha-11 nism relies on a vapor phase precursor of the nanowire materi-12 al which impinges on a liquid phase seed particle, from which 13 unidirectional nanowire growth proceeds. The choice of an 14 appropriate seed material has the benefit of allowing control 15 over the diameter of the nanowires produced, whilst the seed 16 material can also significantly affect the crystalline quality of 17 the nanowire.^{25,26} At this point, the importance of selection of 18 an appropriate precursor material should be highlighted. 19 Within a given precursor, MR_x , where 'M' represents the sem-20 iconductor element, or elemental component of a compound 21 semiconductor, and 'R', represents a ligand. The M-R bond 22 should be sufficiently labile under nanowire synthesis condi-23 tions to directly liberate reactive M species for nanowire 24 growth, or to disproportionate forming reactive M species 25 indirectly.^{27,28} Furthermore, the R group liberated upon pre-26 cursor decomposition should ideally exist as a gas phase spe-27 cies to prevent contamination of the nanowire product with 28 liquid or solid phase by-product. Consequently, metal hy-29 drides are often used as precursor compounds for nanowire 30 growth, as H_2 gas is an especially clean by-product which has 31 the benefit of inhibiting undesirable oxide formation for non-32 oxide semiconductor nanowire growth. Metal hydride precur-33 sors are commonly used in the growth of nanowires by chemi-34 cal vapor deposition (CVD), given that metal hydrides such as 35 SiH₄ and GeH₄ generally exist as gas phase compounds²⁹. 36 Metal-organic precursors, such as diphenylsilane and diphe-37 nylgermane, often used in solution phase and supercritical 38 fluid phase nanowire synthesis can produce carbonaceous by- 100 structive techniques such as ion implanting to generate addi-39 products which may be difficult to completely separate from 101 tional charge carriers. Ion implanting can destroy atomic or-40 the nanowire product.^{30,31} Semiconductor nanowire synthesis 102 dering in the implanted region of the semiconductor crystal 41 conditions often encourage the formation of reactive radical 103 and requires subsequent thermal annealing steps to restore 42 species which can initiate polymerisation reactions resulting in 104 crystal ordering.⁶ 43 unwanted contaminating by-products,³² and as such, precursor 44 design should always be considered when designing an exper- 105 In addition to VLS-type nanowire growth mechanisms there 45 iment for semiconductor nanowire synthesis. Analogues of 106 exists a range of other routes to produce bottom-up grown 46 the VLS mechanism include supercritical fluid-liquid-solid 107 nanowires. These routes, which do not invoke the VLS 47 (SFLS)²⁴, supercritical fluid-solid-solid (SFSS),^{33,34} solution- 108 growth mechanism include, oriented attachment,^{62,63} metal 48 liquid-solid (SLS)³⁵, vapor-solid-solid (VSS)^{36,37} and oxide 109 organic vapor phase epitaxy (MOVPE),^{64,65} molecular beam 49 assisted growth (OAG)³⁸ mechanisms. Common to all of the 110 epitaxy (MBE),⁶⁶ soft templating,^{22,67,68} dislocation driven uni-50 se analogues is the existence of a collector or seed particle 111 directional growth⁴² and crystal habit modification.⁶⁹⁻⁷¹ 51 which acts as a sink for the nanowire material, and from which 52 unidirectional growth proceeds.³⁹ Conventionally, the seed 112 **2.2. Nanowire Alignment Techniques** 53 particle is a metal with which the nanowire material or com- 113 Bottom-up grown semiconductor nanowires fabricated by the 54 ponent thereof forms an alloy. However, autocatalytic or self-55 seeded semiconductor growth has also been demonstrated. $^{40-46}$ 115 meshes of nanowires and as a result lack the periodic ordering 56 Self-seeded VLS-type nanowire growth is most commonly 116 and placement required for large-scale semiconductor device 57 observed for compound materials such as InP, GaN and $SnO_2 117$ processing. Figure 1 displays an SEM image of an entangled 58 whereby the metallic component of the material, In, Ga and Sn 118 mesh of SiO₂-coated Ge nanowires. 59 for InP, GaN and SnO₂ respectively, forms seed particles for 60 nanowire growth of the compound material.^{45–47} However,

61 there have also been reports of self-seeded nanowire growth 62 for elemental materials where a VLS-type mechanism has 63 been invoked.⁴⁸ The most commonly used metal catalyst for 64 VLS-type nanowire growth is Au, prepared either as colloidal 65 Au nanoparticles or as an evaporated or sputtered thin film. 66 However, Au is inherently incompatible with semiconductor 67 device manufacturing. Au has a high diffusivity in Si and also 68 acts as a deep level acceptor and thus has detrimental effects 69 on device performance.⁴⁹⁻⁵¹ Furthermore, Au is a highly inert 70 material which makes cleaning of instrumentation contaminat-71 ed with Au extremely difficult. For example, traditional Au 72 etchants include aqua regia (concentrated nitric acid and hy-73 drochloric acid solution), KI/I_2 solution and alkali cyanide 74 solutions, all of which would corrode stainless steel equipment 75 and in the case of alkali solutions result in detrimental effects 76 on semiconductor device performance, such as shifting of 77 threshold voltage (V_t) .^{52,53} Consequently, there has been sig-78 nificant research into alternative, complementary metal-oxide-79 semiconductor (CMOS) production compatible, metal seeds 80 for catalyzed VLS semiconductor nanowire growth.^{54–56} Ac-81 ceptable metals should have ionization energies far from the 82 mid band-gap region of the semiconductor material. Si nan-83 owire growth has been demonstrated using a number of Si 84 CMOS compatible metals including Bi³⁵ and Al.⁵⁷ Great care 85 must be applied even when using CMOS compatible metals 86 for nanowire growth, as these metals can still act as active 87 dopants in the nanowire material. Al. for example can readily 88 migrate through Si via interstitial sites in the Si lattice, thus 89 acting as an n-type dopant in Si.^{58,59} Furthermore, Si migration 90 through the Al metal is also possible and may dramatically 91 affect the electrical performance of the nanowire material.⁶⁰ A 92 seed metal, such as Al may also be beneficial for preparation 93 of an Ohmic contact to the nanowire tip, thus facilitating nan-94 owire FET device formation.

95 One benefit of bottom-up nanowire growth over top-down 96 processing is that nanowires grown by bottom-up methods 97 may be doped in-situ during crystal growth by incorporating 98 dopant precursors in the nanowire synthesis procedure. Con-99 sequently, bottom-up grown nanowires may not require de-

1 Recently there have been a number of techniques developed to 2 align semiconductor nanowires produced as entangled mesh-3 es.⁷² Examples include alignment of polar nanowires within 4 strong electric fields,^{73,74} dielectrophoresis,^{75,76} microfluidic 5 alignment,⁷⁷ lubricant-assisted contact printing,^{78–80} and evapo-6 ration-induced alignment.^{81–83} Electric field-based alignment 7 techniques, including dielectrophoresis, have been shown to 8 allow precise control over nanowire position with respect to 9 metallic contact pads, however, these techniques have not yet 10 demonstrated the high density of aligned nanowires required 11 for high volume manufacturing (HVM), which is currently 12 approaching a device half-pitch of 20 nm.¹² Figure 2 displays 13 images of nanowires aligned by dielectrophoresis at a pitch of 14 ~ 20 μm.

15 Microfluidic alignment, contact printing and evaporation in-16 duced alignment techniques have all demonstrated the capabil-17 ity to create parallel nanowire arrays, in some cases with high 18 areal density. Fan *et al.*, for example, have demonstrated 19 aligned nanowires at a density of ~10 nanowires/µm.⁷⁸ How-20 ever, these techniques lack the prerequisite precision of con-21 trol over nanowire placement, required for individual nan-22 owire addressability within very large scale integrated circuit 23 (VLSI) technology. Nevertheless, such techniques have been 24 used not only to demonstrate successful individual device 25 operation, but, also to demonstrate integrated devices in a fully 26 functioning nano-processor.⁷⁹

27



29 Figure 1. An SEM image of an entangled mesh of SiO_2 -coated Ge 30 nanowires grown from colloidal Au nanoparticles by the SFLS 31 method.



33 Figure 2. Optical dark-field and DUV images of nanowires as-34 sembled onto electrodes by dielectrophoresis: (a) dark-field image 35 of defect-free nanowire assembly arranged on electrode arrays 36 (scale bar = 200 μ m), (b) high magnification dark-field image of 37 nanowires aligned on 2 μ m wide electrodes (scale bar = 20 μ m) 38 and (c) DUV image of a single nanowire aligned on electrodes 39 separated by 12 μ m (scale bar = 4 μ m).⁷⁶

40 A change of direction may be required for bottom-up ap-41 proaches to achieve the requisite nanowire density, placement 42 control and alignment required for VLSI manufacturing. High 43 density vertical semiconductor nanowire films have been pro-44 duced using a range of bottom-up techniques. These tech-45 niques include, epitaxial nanowire growth,^{25,57,65,84–89} and hard-46 templated nanowire growth.^{90,91} Figure 3 shows an SEM im-47 age of vertically aligned epitaxially grown nanowires, where 48 the diameter was controlled by an anodized aluminium oxide 49 (AAO) template.

50 The epitaxial route to semiconductor nanowire synthesis has 51 the advantage of controlling nanowire crystal orientation



53 **Figure 3.** SEM image of epitaxial vertical Si nanowire arrays 54 grown within an AAO hard template (template removed in 55 image). Nanowire crystal orientation is controlled epitaxially 56 by the substrate, whilst diameter and placement of the nan-57 owires is controlled by the template.⁹⁰

1 through the selection of an appropriate substrate crystal orien-2 tation. Wang et al. for example, have demonstrated the epi-3 taxial growth of vertically aligned <111> oriented Si nan-4 owires on a <111> Si substrate by CVD using an Al catalyst. 5 Nanowires can also be produced epitaxially when there is a 6 large lattice mismatch between the nanowire material and the 7 substrate material. Tomioka et al. reported the growth of 8 <111> oriented InAs nanowires on a Si <111> substrate, de-9 spite an 11.6 % lattice mismatch between the two crystals, by 10 using a 'selective area' MOVPE technique whereby lattice 11 mismatch strain was dissipated by limiting the interfacial area 12 between the two crystals.⁶⁵ A patterned amorphous SiO₂ thin 13 film, prepared by electron beam lithography and etching, acted 14 as a mask for growth of the nanowires by vapor phase epitaxy. 15 Shimizu *et al.* have shown that the combined use of epitaxial 16 nanowire growth and an ordered template such as AAO to 17 control the position of these nanowires, allows a route to or-18 dered arrays of vertically aligned, coaxial, Si nanowires suita-19 ble for use in vertical nanowire device fabrication (figure 3).⁹⁰ 20 Ordering of pores in AAO spontaneously occurs during AAO 21 formation as a mechanism to reduce internal strain in the AAO 22 film.⁹² The formation of AAO with hexagonally close packed 23 (HCP) pores can be considered a bottom-up process, as the 24 pores self-assemble into a HCP arrangement from an initial 25 disordered state, pore by pore.⁹²

26 2.3. Vertical Nanowire Field Effect Transistors

27 There have been several reports of field effect transistor (FET) 28 devices produced using vertically aligned, bottom-up grown 29 semiconductor nanowires. $^{93-100}$ Figure 4 shows electron mi-30 croscopy images of vertical Si nanowires used to create verti-31 cal nanowire FET devices. The reported devices showed rea-32 sonable performance characteristics with observed I_{ON}/I_{OFF} 33 ratios > 10^5 and a sub-threshold slope of 120 mV/decade, alt-34 hough their performance was still significantly poorer than 35 current state-of-the-art, top-down, strained Si devices.^{14,101} 36 The vertical nanowire devices demonstrated significantly low-37 er on/off ratios and shallower sub-threshold slopes than their 38 top-down counterparts. The reasons for their inferior perfor-39 mance can be attributed to a number of issues including, con-40 tact resistance at the source and drain interfaces, non-uniform 41 dopant distribution within the nanowire channel, charge trap-42 ping at the





46 with thermally grown SiO_2 shells. Scale bars represent lengths of 47 1 µm, 75 nm and 4 nm in (a), (b) and (c) respectively.⁹⁹

48 gate dielectric interface, or charge carrier recombination due to 49 Au incorporation within Au-seeded Si nanowires. Some of 50 these issues may be rectified, for example, the choice of an 51 appropriate seed metal for nanowire growth is important. Not 52 only should the seed metal allow production of the desired 53 nanowire structure, the metal should also have an appropriate 54 work function to form an ohmic contact to the semiconductor 55 nanowire.^{102,103} Au tends to form Schottky contacts to n-Si 56 resulting in high contact resistance to the semiconductor nan-57 owire channel.¹⁰⁴ The choice of metal also depends strongly 58 on the majority charge carrier and carrier concentration in the 59 nanowire device, for example p-type devices require metals 60 with increased work function values compared to n-type de-61 vices, and higher semiconductor charge carrier concentrations 62 result in reduced depletion layer widths at the metal-63 semiconductor junction which facilitates carrier tunnelling and 64 thus reduced contact resistance.¹⁰⁴ Alternatively, the option 65 exists to use a seed metal which has an inappropriate work 66 function to produce the nanowires and subsequently strip this 67 metal away by chemical etching, followed by the deposition of 68 a suitable electrical contact metal. However, this approach 69 introduces additional device processing steps and complete 70 removal of the seed metal after chemical etching is unlikely, 71 especially when alloys may have formed with the semiconduc-72 tor during nanowire growth. The issue of dopant distribution 73 is critical to device performance. A homogeneous, activated 74 dopant distribution is desired within semiconductor devices in 75 order to assure a stable threshold voltage (V_t) .¹⁰⁵ Perea *et al.* 76 have mapped the dopant distribution within an individual VLS 77 grown Ge nanowire, and have shown the dopant distribution 78 to be non-uniform along the nanowire growth axis and radially 79 across the nanowire.¹⁰⁶ Techniques such as single ion implan-80 tation have been shown to improve the homogeneity of dopant 81 incorporation in the nanowire structure resulting in improved 82 V_t stability from device to device.¹⁰⁵ A number of approaches 83 have been taken to improve semiconductor nanowire surface 84 passivation to remove surface state charge trapping sites, 85 which can have capacitive effects at the nanowire surface and 86 hinder device performance. These approaches include organic 87 passivation of the nanowire surface,^{107–110} deposition of dielec-88 tric materials such as SiO_2 , and Al_2O_3 and nitridation or sulfi-89 dation of the nanowire surface.^{111,112} Finally, issues arising 90 due to metal dopants from the catalyst metal particle can be 91 negated through the use of an appropriate metal for the semi-92 conductor of choice. The metal should not have ionization 93 energies at or near the centre of the band-gap of the semicon-94 ductor, e.g. Al or Bi for Si. Once the outstanding issues de-95 tailed above have been addressed, bottom-up grown vertical 96 nanowire FETs may become a practical route toward contin-97 ued device footprint scaling within VLSI technology.

98 2.4. Bottom-Up Semiconductor Nanowire Outlook

99 There are a number of outstanding issues associated with the 100 integration of bottom-up grown semiconductor nanowires into 101 conventional integrated circuit (IC) design and processing. 102 Conventional IC design is based on the active channel of the 103 logic devices lying coplanar to the Si wafer substrate, and 104 requires a very high degree of control over placement of the 105 devices so that they may be individually addressed for suc-45 Figure 4. Vertically aligned, epitaxial, Au seeded, Si nanowires 106 cessful IC operation. Traditionally, bottom-up grown semi-107 conductor nanowires are grown as entangled meshes and con-108 sequently lack the prerequisite ordering, and control of place-

1 ment required for IC manufacturing.^{24,40,113} Although there 2 have been recent advances in extracting nanowires from such 3 entangled meshes and aligning them on substrates, these ap-4 proaches can produce neither the high density of nanowires 5 desired, nor the large scale areal coverage required, for 6 HVM.^{74–77,79,81,114} As such, industrial applications of entangled 7 meshes of semiconductor nanowires may be limited to the 8 production of nanowire composites, which may have applica-9 tions in areas such as batteries, flexible electrodes and thermo-10 electric generators.^{115–117} However, there still remains signifi-11 cant value to be gained from the study of individual, novel, 12 nanoscale structures, from a conceptual standpoint. Given the 13 issues associated with the alignment of bottom-up grown sem-14 iconductor nanowires in the substrate coplanar orientation, it 15 seems imperative that another route to IC fabrication be de-16 vised. Perhaps the most promising route toward integration of 17 bottom-up grown semiconductor nanowires into an IC com-18 patible arrangement is that of a vertically oriented active chan-19 nel with respect to the substrate. Transferring to a vertical 20 orientation would be a huge change for a very mature technol-21 ogy. However, recent developments in the industry with the 22 adoption of tri-gate and finFET structures have shown that 23 movement out of the plane of the Si substrate is possible and 24 as such presents an opportunity for the development of 3-D 25 device architectures.¹¹⁸ Advances in CVD techniques for nan-26 owire growth have allowed the production of epitaxial nan-27 owires whereby the crystalline orientation of the nanowires 28 with respect to a substrate is controlled at the epitaxial inter-29 face. Operational vertically integrated nanowire field effect 30 transistors (VINFETs), produced using bottom-up grown sem-31 iconductor nanowires have been reported by several 32 groups.^{96,99,100,119} The VINFET concept remains a viable op-33 tion for future semiconductor device processing as it potential-34 ly offers a route to high density stacks of GAA nanowire FET 35 devices. The vertical orientation with respect to the substrate 36 allows devices to be stacked on the substrate which ultimately 37 increases the density of devices and thus computing power per 38 chip area. A wrap around gate or GAA structure also offers 39 superior electrostatic control of the channel compared to cur-40 rent devices in production, which may allow improved switch-41 ing of the device. However, a great amount of work is still 42 required to individually contact each device within such a high 43 density, stacked architecture and consequently IC fabrication 44 using VINFET devices is still in its infancy. Furthermore, the 45 International Technology Roadmap for Semiconductors 46 (ITRS) has targeted a line width roughness (LWR) value of 47 1.4 nm 3σ for device structures by 2015.¹² LWR values in the 48 targeted range are not yet achievable in semiconductor nan-49 owire fabrication by bottom-up means, where the narrowest 100 lenses are often used as a compromise between reduced fea-50 nanowire diameter distributions typically possess 3σ values of 101 ture size (CD) and wafer throughput. Although reduction 51 approximately 3 nm.^{120,121} Consequently, further work is re-102 lenses do not increase the resolution of the lithography pro-52 quired in the areas of alloy engineering and nanowire catalyst 103 cess, they can be used to scale larger features in the photomask 53 control to achieve the targeted control of nanowire diameter 104 to a fraction of that size in the image projected on the photore-54 for device components in future VLSI manufacturing. Bot- 105 sist. This scaling reduces some of the demands placed on 55 tom-up grown nanowires are expected to possess fewer sur-106 mask manufacturing, as low density larger features are typical-56 face dangling bonds than their top-down analogues, which are 107 ly produced with fewer defects than high density, smaller fea-57 fabricated by etching. A reduction in dangling bond density 108 tures in mask 58 for bottom-up grown nanowires can be attributed to nanowire 109

59 surface faceting during nanowire growth, which is driven by a 60 reduction in the surface chemical potential and atomic diffu-61 sion during crystal growth.¹²² Surface dangling bonds can trap 62 charge carriers in the nanowire thus reducing carrier density, 63 and also inhibit effective gating of nanowire FETs by intro-64 ducing interface states at the semiconductor-dielectric inter-65 face. ^{56,123} Additional annealing steps are typically employed in 66 top-down fabrication to reduce nanowire surface roughness 67 and dangling bond density to improve electrical performance 68 of top-down fabricated nanowires.^{123–125}

69 3. Top-Down Semiconductor Nanowire Fabrication

70 3.1. Optical Lithography

79

71 Optical lithography has been the industry standard for semi-72 conductor device definition and placement for decades. In 73 that time there have been significant developments in optical 74 lithography, both in terms of resist technology and optics.^{126–} 75¹²⁹ There has been a general trend toward shorter wavelength 76 radiation sources to achieve higher image resolution as given 77 by the relationship in equation 1 derived from the Rayleigh 78 criterion.¹²⁹

$$CD = \frac{k\lambda}{NA} \tag{1}$$

80 CD represents the minimum critical dimension that can be 81 imaged in a photoresist using a given process having a process 82 latitude factor of k, an emission wavelength λ (nm), and a nu-83 merical aperture NA, where $NA = n\sin\theta$, where n represents the 84 refractive index of the medium in which the final projection 85 lens is operating and θ represents the half-angle of the maxi-86 mum cone of light that exits the final lens of the system. In 87 the 1970s, Hg G-line emission, at a wavelength of 436 nm, 88 was the light-source of choice for optical lithography. Current 89 VLSI manufacturing employs an ArF laser with an emission 90 wavelength of 193 nm. In addition to reducing the wavelength 91 of the radiation source, other measures have also been taken to 92 improve image resolution. DUV scanners and steppers regu-93 larly incorporate a reduction lens as the final projection lens of 94 the lithography system. Reduction lenses typically allow $4 \times$ 95 or 5 \times reduction of features in the photomask.¹²⁸ The use of 96 reduction lenses in scanners and steppers results in a conse-97 quent scaling of the image field, which translates as an in-98 crease in the number of exposure fields per wafer and thus a 99 lower throughput of wafers. Consequently, 2 \times reduction



Figure 5. TEM image of a cross-section of a 10 nm \times 40 nm Si nanowire produced from SOI using a 193 nm immersion lithography process incorporating resist trimming steps and overetching.¹³⁰

1 fabrication. Interference lithography can be used to create 39 2 3 arrays of features with CD values a fraction of the wavelength 40 of the radiation source.^{128,131–133} Interference lithography re-41 4 quires a number of coherent beams of radiation to be focused 42 5 on a spot to create an interference pattern, where the period of 436 the pattern is a fraction of the initial radiation wavelength. 44 7 Typically interference lithography is only used to produce 45 8 arrays of structures such as gratings. Immersion lithography is 46 9 a technique whereby the final projection lens of the radiation 47 10 source is immersed in a medium with a higher refractive index 4811 than air, e.g. water 1.436 at 193 nm. Increasing the refractive 49 12 index of the medium in which the final lens operates, effec- 5013 tively increases the NA value of the system and as such reduc- 51 14 es the minimum *CD* of features that can be imaged in the pho-52toresist.128 15 Media with higher refractive indices than water 53 16 are also being investigated to further increase the process reso-54 lution.¹²⁸ The 'k-factor' or process latitude factor given in 55 17 18 equation 1, is a broad term which depends on a number of 5619 process dependant parameters. The 'k-factor' accounts for 57 20photoresist effects, developer effects and reticle (photomask) 58 21 effects, amongst others, and as such is a difficult term to pre- 59 22 dict for a new process. In essence, a high 'k' value is repre-6023 sentative of a lower resolution process, where process parame-61 24 ters limit the achievable resolution. Typical 'k' values can be 6225 as low as 0.15, thus allowing features with dimensions a frac- 63 26 tion of the wavelength of the incident light, to be imaged in 64the photoresist.^{128,134} Techniques that can be used to reduce 6527 28 'k' values include the use of high resolution resists and resist $\overline{66}$ trimming processes, as shown in figure $5^{129,134}$ However, 6729 30 even with such low 'k' values, achieving the high feature den- $\overline{68}$ 31 32 sities desired for current semiconductor device production 69sities desired for current semiconductor device production 69 requires further process developments such as, optical proxim- 70 ity correction (OPC),^{126,135} phase shift masks (PSM),¹³⁶ and 71 double patterning (figure 6).^{16,130} Ultimately continued device 72 scaling and increased device density may require extreme ul- 73 tra-violet (EUV) or x-ray lithography (XRL) due to the dra- 74 matically reduced wavelengths of these techniques, typically 75 13.5 nm for EUV and < 1 nm for XRL, compared to current 33 34 35 36 37 38

UV lithography techniques. Whilst short wavelength techniques like EUV and XRL offer significant potential for nanolithography, they do have drawbacks. EUV lithography tools have to operate in vacuum due to strong EUV absorption by air. Consequently, EUV resists should not be volatile or swell or under vacuum.¹³⁷ Additionally, the requirement for loading and unloading wafers from vacuum chambers puts significant time demands on the process. Furthermore, shot noise, proximity effects and flare issues remain outstanding, all of which will hinder the ultimate resolution of the lithography process. XRL too has a number of issues which may prove to be prohibitive for HVM. XRL requires synchrotron radiation sources which may prove to be too large an investment for an unproven manufacturing process with considerable associated risk. However, XRL does not demonstrate the significant, detrimental, radiation-material interactions observed for EUV and as such it remains a pursued and viable option for further technological development.¹²⁹

The significant technological advancements in the field of optical lithography outlined above demonstrate the suitability of these techniques to fabricate ordered arrays of semiconductor nanowires with excellent control over placement and feature-size. Lateral nanowires may be fabricated from layered substrates such as silicon-on-insulator (SOI), or epitaxial thin films, prepared by molecular beam epitaxy (MBE), or metal organic vapour phase epitaxy (MOVPE). Arrays of lateral nanowires can be prepared by fabricating gratings or line structures in the resist material and transferring the grating pattern to the substrate through the use of an appropriate etch process. Figure 5 displays a TEM image of a cross-section through a 10 nm wide Si nanowire fabricated from SOI using 193 nm immersion lithography.

Similarly, vertical nanowires may be prepared from bulk or layered substrates by using a resist mask consisting of dot or polygonal structures with maximum lateral dimensions below 100 nm and transfer of the mask pattern deep in to the substrate, again using an appropriate anisotropic etch process.¹³⁸



Figure 6. Schematic of a number of approaches for double-patterning lithography. CMP, refers to chemical mechanical planarisation.¹²⁸

Inductively coupled plasma (ICP) and reactive ion etch (RIE) 29 2 3 techniques are most commonly used for pattern transfer, alt-30 hough anisotropic wet etch and metal assisted etch (MAE) 31 procedures have also been used.^{138,139} 4 32

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33 5 3.2. Next Generation Lithography: Electron Beam Li- 346 thography and Competing Techniques 35

7 A number of lithography processes are being considered to 36 8 extend lithography scaling beyond current UV lithography 37 capabilities, for semiconductor device manufacturing. These 38 techniques include, electron beam lithography (EBL),^{124,140,141} 39 nanoimprint lithography (NIL),^{142,143} XRL,^{144,145} EUV lithog- 40 9 10 11 raphy,^{146,147} scanning probe lithography (SPL),¹⁴⁸ ion beam 41 lithography (IBL),^{149,150} and electron beam induced deposition 42 (EBID) lithography.^{151–153} EBL is at the heart of many of these 43 12 13 14 15 techniques, including the optical lithography processes. EBL 44 is generally used for the fabrication of high-resolution photo- 45 16 masks for DUV, EUV and XRL. NIL stamps are also pro-46 17 duced using EBL direct-write processes. EBID lithography is 47 18 19 essentially an EBL process that incorporates the use of a gas 48injection system which disperses a gaseous precursor that de-49 20 21 composes under the electron beam and directionally deposits 50 22 on the substrate surface forming a mask. As such, current and 51 23 future VLSI manufacturing is heavily dependent on the devel- 52 24 opment of EBL processes and instrumentation. EBL has been 53 $\overline{25}$ shown to be capable of producing sub-10 nm features at sub- 54 20 nm pitches.^{154,155} Figure 7 displays examples of high-55 26 27 resolution EBL processes used to produce line-widths as small 28 as 4.5 nm at pitches as low as 9 nm.

However, the primary concern with the implementation of EBL techniques in HVM is the low throughput of wafers due to the exposure times required for full wafer layouts. Exposure times depend on several factors which include the tone of the resist, the area of the wafer to be exposed, the electron beam current, electron energy, and the sensitivity of the resist (electron dose required to completely chemically alter the resist).^{129,156} Resist technology may have a significant role to play in the reduction of EBL exposure times. Increasing the resist sensitivity will significantly reduce the required time for exposure; however, increased sensitivity should not compromise the ultimate resolution of the resist. Hydrogen silsesquioxane (HSQ), the smallest member of the polyhedral oligomeric silsesquioxane (POSS) family, is an example of one of the highest resolution negative-tone EBL resists. However, HSQ exposure doses are considered too high for use in HVM. Chemically amplified resists (CARs) have been developed with significantly increased sensitivity with respect to HSQ, but these resists offer lower ultimate resolution. The field of EBL resist research is an active one and recent demonstrations of EBL using analogues of HSQ with increased electron beam sensitivity are promising.157

Multi-beam EBL systems are under development which will increase wafer throughput either through beam-splitting techniques, or through the use of instruments with multiple electron sources, however, the technology is still not mature and as



Figure 7. High resolution features produced by EBL: (a) 8 nm diameter strained n-Si nanowires produced using a hydrogen silsesquioxane (HSQ) EBL process for gate all-around FET devices and (b) nested lines at a pitch of 14 nm.^{124,155}
such has yet to be implemented on a HVM scale.¹⁵⁸ Lee et ⁴¹

al.¹⁵⁹ have reported a particularly innovative example of multibeam EBL using a Si crystal as an electron beam mask (figure 42
8). A transmission electron microscope (TEM) was used to 43
create arrays of electron beams where the shape and separation 44
of the beams was governed by the crystal structure and crystal 45
orientation of the mask with respect to the incident electron
beam. Atomic resolution images of the Si crystal lattice were 46
magnified and projected onto HSQ films creating arrays of 47
nanostructures in the resist. This technique shows promise for 48
increased throughput where periodic arrays of simple na-49
noscale structures are desired.

Arrays of dot structures produced by EBL can be used to fabricate vertical nanowire arrays through the use of a deep anisotropic etch.¹⁶⁰⁻¹⁶² The use of an etch resistant material to form 54 the dot structures is paramount to facilitate deep etching to form high aspect ratio nanowires. Typically, Al₂O₃, Al, and 56 SiN_x, have been used as etch masks for vertical Si nanowire 57 fabrication. Figure 9 shows an SEM image of arrays of vertisea Si nanowires produced using an EBL process.¹⁶²

26 Commonly encountered issues for EBL processes include 27 electron-substrate or electron-resist interactions and surface 28 charging of insulating substrates. Electron-substrate and elec- 29 tron-resist effects can be grouped into three sub-classes, for- 30 ward scattered electrons (scattering angle > 90°), back- 31 scattered electrons (scattering angle > 90°) and secondary 29 electrons.¹²⁹ Forward scattered electron effects are most im- 30 portant within the resist as electrons which are forward scat- 41 tered in the substrate have little contribution to resist exposure.



Figure 8. Arrays of HSQ nanostructures produced using projec- 80 tion of the atomic lattice of a Si crystal (a) and (e) in a TEM. 81 SEM images (b-d) and (f-h) respectively show the critical dimension and pitch scaling of the structures with increasing TEM magnification, $160 \times (b,f)$, $200 \times (c,g)$ and $300 \times (d,h)$.¹⁵⁹ 84



Figure 9. SEM image of an array of 50 nm diameter Si nanowires etched into a Si wafer. A sputtered Al_2O_3 hard mask, patterned by EBL was used as the Si etch mask.¹⁶²

Forward scattering can be minimised by using a high accelerating voltage (higher energy electrons) or a thinner resist layer. Backscattered electron exposure effects are more prominent for high atomic weight (Z) materials and as such are more commonly a consequence of electron-substrate interactions. Secondary electrons are the primary electron-solid interaction, and as such they make the largest contribution to resist exposure. Importantly, although secondary electrons are responsible for most of the resist exposure, their path length in the resist is short, typically < 10 nm, and as such these electrons do not have a significant contribution to proximity effects. Proximity effects can largely be attributed to backscattered electrons which experience large angle scattering and can commonly travel large distances laterally in the substrate and resist (~1 µm for 10 keV incident beam energy). Proximity effects due to electron-solid interactions can be corrected through careful modelling of electron scattering, typically as a point spread function (PSF) and the use of appropriate electron dose contour maps based on these models.^{158,163} Experimentally derived data can also be used to develop PSFs for use in proximity effect correction (PEC). PEC is particularly important for the exposure of high density features and large structures where electron scattering effects become prominent.

Charge accumulation at the surface of insulating substrates is another factor that can dramatically affect resolution and alignment in EBL. Surface charging results in an associated electric field at the substrate surface which acts to deflect the incident electron beam with detrimental effects on the EBL process. Surface charging effects can be avoided through a number of avenues. Deposition of a thin layer of conducting material (Au, Cr, Al or conducting polymers) atop the resist can remove surface charging effects, with the drawback of the introduction of an additional layer of material in the EBL process. Conducting polymers such as ESPACER (Showa-Denko), a member of the polythiophene family, are preferable to metals such as Au due to their superior process compatibility.¹²⁹ ESPACER is soluble in water and as such can be easily removed following electron beam exposure and prior to developing the resist, where as complete removal of Au and similar metals requires harsh etching conditions which may alter

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the resist, and the substrate. Much work has been performed 622 3 in the field of electron-solid interactions and as such model-63 ling and correcting undesired electron-solid interactions is 64 now possible.¹⁶³ However, until EBL sample throughput 65 4 5 times are reduced to acceptable levels for HVM. EBL will 66 6 remain confined to tasks such as quantum device demonstra-67 7 tion, NIL stamp fabrication and high-resolution photomask 688 fabrication. Development of multiple beam EBL systems will 69 9 improve the throughput of EBL tools, however such systems 70 10 are still unproven and require further investment to compete 71 with their optical counterparts for a role in next generation 72 VLSI manufacturing.^{126,158,164,165} 73 11 12 Electron beam induced deposition (EBID) can be used as a 74 lithographic tool to produce sub-10 nm features.^{152,166} As stat-75 13 14 ed previously, EBID essentially involves introducing a gase- 76 15 ous previously, EBID essentially involves introducing a gase-70 ous precursor species into the path of an electron beam in an 77 EBL system. The precursor decomposes upon electron beam 78 exposure and directionally deposits the solid decomposition 79 product, typically a metal such as W, or Pt, on the substrate. 80 EBID is a capable lithographic tool for the production of de-vices on a small scale ¹⁵¹ However EBID suffers for a start 82 16 17 18 19 20 vices on a small scale.¹⁵¹ However, EBID suffers from inher- $\frac{82}{32}$ 21 22 ent drawbacks such as metal contamination of device struc- 83 tures and low throughput. Consequently, EBID is more suited $\frac{84}{2}$ 23 85 24 to small-scale applications such as photomask defect repair. Lithography using focused beams of ions such as He⁺, Ga⁺ and $\frac{86}{27}$ 25 Lithography using focused beams of ions such as He⁺, Ga⁺ and ⁸⁰ Ne⁺ has been used to demonstrate structures with sub-10 nm ⁸⁷ critical dimensions.¹⁴⁹ Ions of He, Ga and Ne are significantly ⁸⁸ larger and heavier than electrons and as such travel shorter ⁸⁹ distances in resist materials than electrons. Consequently, ion ⁹⁰ beam lithography is a promising technique for generating a ⁹¹ high-density of structures in a suitable resist material. Fur-thermore, Ne⁺ ions have been shown to transfer energy to HSQ ⁹³ resist more efficiently than electrons, thus facilitating high-⁹⁴ 26 27 $\overline{28}$ 29 30 31 32 resist more efficiently than electrons, thus facilitating high-94resolution pattern generation at low exposure doses. In fact, 95Ne⁺ IBL has demonstrated exposure efficiencies ~1000×96 33 34 35 greater than electrons with equivalent landing energies. $^{150}97$ 36 Whilst Ga^+ focused ion beam (FIB) systems are widely availa-98 bla and used for a range of amplications such as TEM sample 99 37 ble and used for a range of applications such as TEM sample 99 preparation, optical lithography mask repair and crossion 38 39 sectional analysis, He^+ and Ne^+ ion beam system are far less 01 40 41 common. He⁺ ion microscopy (HIM) has gained significant 42 attention in recent years as it is not susceptible to surface 43 charging effects commonly encountered in electron microsco-44 py, and as such may be used to acquire surface sensitive images of insulating materials.¹⁶⁷ HIM may thus be particularly 45 46 suited to lithography on insulating substrates. Although ion 47 beam lithography techniques offer noticeable advantages over 48 electron beam lithography in terms of reduced proximity ef-49 fect, increased energy transfer efficiency to the resist material 50 and reduced charging effects, significant concerns still remain 51 with regard to ion beam stability over the timescales required for full wafer exposures.^{167,168} Consequently, ion beam lithog-52 raphy is a very promising technique for next generation lithog10253 54 raphy, but requires significant investment for scalability of the 55 technique for HVM and for techniques such as mask produc-56 tion where exposure times on the order of several hours will 10357 104 be required. Many of the issues associated with the implementation of 105 EUV, and XRL techniques in HVM have been discussed in the province costing. 58 59 60 the previous section. NIL is a mechanical lithography tech107

61 nique whereby a stamp or template created in a robust materi108

al, usually Ni or Si, for thermal NIL; PDMS for soft NIL; and quartz for step and flash NIL (S-FIL a trademark of Molecular Imprints Inc.), is pressed into a deformable resist on a substrate. The resist is then hardened so that when the template is removed the contours of the template are transferred to the resist. The patterned resist can then be used for subsequent pattern transfer procedures. NIL is a relatively inexpensive technique when compared to other nanolithography techniques and has demonstrated the production of very fine features at high areal densities.¹⁴² Feature sizes as small as 6 nm have been demonstrated, with half-pitches below 20 nm also readily achievable.¹⁶⁹ Furthermore, NIL can be used to directly pattern interlayer dielectric (ILD) materials such as low-k silsesquioxanes (SSQs) thus reducing the number of process steps required in the dual-damascene process typically used to form metallic interconnects.^{170,171} However, there are outstanding issues concerning overlay accuracy, defect density and throughput. Furthermore, NIL processes are mask specific and as such must be tuned to achieve the optimal resist volume for specific mask designs, which can limit the technique where large area patterns are required. Additionally, NIL may not be compatible with pattern transfer to porous low-k materials used as back-end-of-line (BEOL) insulators, which are inherently brittle and may be deformed by the pressure applied during NIL.142

Scanning probe lithography (SPL) encompasses a range of lithography techniques including, dip-pen nanolithography (DPN), local oxidation nanolithography (LON), atomic force microscope (AFM) lithography and scanning tunnelling microscope (STM) lithography. Common to these techniques is the use of a scanning nanoscale probe, typically an AFM tip, to pattern a resist or substrate directly.^{172,173} In the case of DPN an AFM tip is used to transfer a material to the surface which can subsequently act as an etch mask or may act as an active device component itself. LON is used to locally oxidise a material thus forming a patterned surface oxide by applying a voltage bias between a conductive AFM tip and the substrate material in the presence of water vapour to induce localised oxidation of the substrate through electrochemical reaction with the water vapour.



Figure 10. False colour STM image of a quantum corral structure created by the atomic manipulation of 48 Fe atoms on a Cu $\{111\}$ surface. The Fe ring confines the surface electron wavefunction of the defect free Cu surface within.¹⁷⁴

AFM lithography can operate in contact mode or non-contact mode. Contact mode AFM lithography in volves the mechan-

ical patterning of a substrate much like NIL. An AFM tip can 60L 2 3 be used to scratch or stamp a pattern into a resist material or 61 into the substrate itself. Non-contact mode AFM can be used 62 4 to pattern materials through local oxidation of the substrate 63 5 surface as in the case of LON, through local heating of a resist 64 6 material using a heated AFM tip, or through local electron 65 exposure via a field emission AFM tip, 172,173 STM lithography 66 7 8 has been used to produce nanostructures by a variety of 67 9 means. Scappucci et al. have reported the use of STM to se-68 10 lectively dope regions on a H-terminated Ge (100) surface 69 11 where H atoms have been removed by STM, thus creating 70 doped nanowire structures.¹⁴⁸ STM can also be used for the 71 12 13 individual manipulation of atoms on a surface to produced 72 14 quantum structures, such as the quantum corral reported by 73 Crommie *et al.* in 1993 (figure 10).¹⁷⁴ SPM lithography tech-7415 niques are inherently slow even when multiple probes are 75 16 used.¹⁷⁵ As such, low throughput will prevent such techniques 76 17 18 from being used in HVM.¹⁷

193.3. Top-Down Semiconductor Nanowire Fabrication7820Outlook80

21 22 Top-down semiconductor lithography processes have domi-81 nated the area of semiconductor device definition and place-82 23 ment for decades. However, as the density of devices on a 83 24 25 chip continues to scale significant difficulties are encountered. 84 Techniques such as EBL and XRL with significantly reduced 85 26 27 28 29 wavelengths, may readily achieve the high densities of devices 86 desired by the semiconductor industry, however, there are a number of difficulties associated with the integration of these short wavelength techniques in VLSI manufacturing. Conse-30 quently, it seems increasingly likely that current top-down 31 processes may have to 'reach out' to a bottom-up technology 32 to achieve the future goals of the semiconductor industry. 33 Integration of bottom-up fabricated VLS nanowires in VLSI 34 manufacturing may be a step too far in the short term as the 35 VLSI industry is geared toward device fabrication in the plane 36 of the Si wafer, and integration of vertically oriented and 37 stacked FETs will require extensive design and process recon-38 figuration. Consequently, a bottom-up technique that facili-39 tates continued scaling in the plane of the substrate may be a 40 more likely first step toward the integration of a bottom-up 41 technique in VLSI manufacturing. One such bottom-up tech-42 nique is that of directed self-assembly of block copolymers.

43 4. Integration of Bottom-Up and Top-Down Processes44 for Nanowire Array Fabrication

45 **4.1. Directed Self-Assembly**

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46 Directed self-assembly (DSA) is an advanced lithographic process based on the self-assembly of block copolymer (BCP) 88 47 thin films. BCP self-assembly involves the bottom-up, mi- $\frac{89}{90}$ 48 crophase separation of chemically different blocks within the 90 49 BCP. Typically, A-B diblock copolymers are used for DSA, $\frac{91}{92}$ 50 51 where an A-B diblock copolymer consists of a linear chain of 52 a monomer A, joined at one end by a covalent bond, to a line-53 ar chain of monomer B. When the two blocks, A and B, are 54 sufficiently chemically distinct from one another, they can 55 microphase separate so as to minimise the interaction of 56 blocks A and B, whilst maximising the interaction between 57 similar blocks. The chemical interaction of the two blocks in 58 a BCP is often quantised by the Flory-Huggins interaction 59 parameter (χ) for that BCP system which is related to the en-

thalpy of mixing for that polymer system.¹⁷⁶ Self-consistent mean field theory has been used to generate theoretical phase diagrams for diblock copolymer melts (figure 11).¹⁷⁷ Mean field phase diagrams are presented as a plot of χN against *f*, where *N* is the degree of polymerisation of the BCP and *f* is the volume fraction of a reference block in the BCP. χN is representative of the thermodynamic driving force for microphase separation within the diblock copolymer melt. χ represents the enthalpic component and is inversely related to temperature and directly related to polymer chain length, whilst N represents the entropic component, which depends on the chain length dependent number of conformations that can be adopted by the polymer.

Figure 12 shows schematic examples of phase morphologies within a microphase separated A-B diblock copolymer with increasing number fraction of block A (f_A) .¹⁷⁶ Lamellar and hexagonally close packed cylinder phases of BCPs are typically used in DSA, where the phase of the BCP can be controlled through selection of appropriate polymer fractions in the BCP, and suitable polymer chain lengths. The microphase separation of BCPs can be guided both chemically and physically through the use of careful templating techniques, *i.e.* directed self-assembly. Physically guided microphase separation of a BCP is often termed graphoepitaxy. DSA of lamella forming BCPs by graphoepitaxy, is generally achieved by creating trenches in a substrate where the trench width is an integer multiple of the block length.



Figure 11. Phase diagram of a diblock copolymer as predicted by self-consistent mean field theory. Phases are labelled L (lamellar), H (hexagonally arranged cylinders), Q_{la3d} (bicontinuous I_{a3d} cubic), Q_{lm3m} (body centred cubic spheres), CPS (close packed spheres), and DIS (disordered).¹⁷⁷





Figure 12. Schematic representation of the microphase morphol-41 ogies of an A-B diblock copolymer with increasing number fraction of block A from left to right.¹⁷⁶ 42

Similarly, chemically guided microphase separation of a BCP 435 6 is termed chemical epitaxy. DSA by chemical epitaxy is 44 7 achieved using a substrate that has been chemically patterned 45 to induce ordering during microphase separation of the 468 BCP.^{179,180} 9 Consequently, DSA by both graphoepitaxy and 47 10 chemical epitaxy is heavily dependent on conventional litho-48 11 graphic techniques such as those outlined in Section 3. 49

12 Ordered diblock copolymer films produced by DSA can be 50 13 used as high-resolution etch masks for semiconductor nan-51 14 owire fabrication. As such, DSA has gained significant inter- 52 est in the field of nanolithography in recent years. DSA offers 5315 16 a number of advantages over conventional optical or direct- 54 17 write lithography techniques. Firstly, DSA can achieve sub- 55 18 lithographic resolution by pattern multiplication, thus increas- 56 19 ing the density of features within low density patterns pro- 57 duced by conventional optical or mask-less lithography tech- 58 20 niques.^{181–184} Implementation of a pattern multiplication pro-59 21 22 cess in current lithographic methods for VLSI manufacturing 60 would remove the necessity for complicated techniques such 61 as double patterning and high density lithography.¹⁷⁹ DSA by 62 chemical epitaxy has also been shown to exhibit self-healing 63 properties, whereby defects in templates used to guide mi-64 crophase separation are corrected in the extended pattern of 65 the mask produced by DSA.^{185,186} Additionally, DSA is a rela-tively inexpensive technique, depending on the process used to 66 23 24 25 26 27 28 29 tively inexpensive technique, depending on the process used to 67 30 guide microphase separation. DSA has the potential to offer 67 very high throughput if it were incorporated with current opti-68 cal lithography processes, and can readily achieve sub-20 nm 70 critical dimensions by controlling the molecular weight of the 71 polymer blocks in the BCP. Furthermore, DSA has been 72 shown to be capable of producing device specific geometries 73 such as bends, T-junctions and jogs.^{181,187} Parameters such as 74 line-edge-roughness (LER) for DSA masks are determined by 74 guide microphase separation. DSA has the potential to offer 31 32 33 34 35 36 line-edge-roughness (LER) for DSA masks are determined by 75 37 the quality of the microphase separation and associated guid- $\frac{75}{76}$ 38 ing technique as well as the quality of the etch used to selec- $\frac{70}{77}$ 39 40 tively remove one of the blocks of the BCP.

Figure 13. Typical process flows used to produce DSA of BCPs via (a) graphoepitaxy and (b) chemical epitaxy, respectively.^{180,188}

LER values as low as 1.95 nm (3σ) have been reported for lines produced by DSA of a lamella forming BCP.¹

However, there are a number of outstanding concerns associated with DSA as a lithographic technique. The primary concern with the process is high defect density, attributable to contamination, BCP purity, BCP molecular weight distribution, chemical uniformity of the substrate surface and defects within the DSA guiding template. Substrate surface uniformity is known to be a critical factor in achieving large areas of uniformly oriented microphases in BCP films. Consequently, there has been a large research investment in the study of selfassembled molecular monolayers and polymer brush layers to tailor the substrate surface energy, and BCP wetting, for BCP self-assembly.^{179,189–192} Additionally, BCP layers are often prepared as thin monolayers of the microphases e.g. a single layer of substrate coplanar cylinders in the case of PS-b-PDMS, and often have poor etch resistance, e.g. PMMA, PS.

Whilst the defect density in DSA masks is improving with increased research investment, DSA processes still require further optimisation before they can be integrated into a HVM landscape. Figure 14 shows an example of relatively large area patterning achieved via the graphoepitaxy of PS-b-PDMS.¹⁸² Chemical epitaxy DSA techniques can 'heal' defects present in the guiding template; however, chemical epitaxy has not yet demonstrated pattern multiplication to the extent of graphoepitaxy based techniques. Thus, it is likely that each approach, chemical epitaxy and graphoepitaxy, will find their own niche application within the semiconductor industry. Development of DSA masks with sufficient etch resistance will depend on the specific process requirements. PS-b-PDMS for example, is a promising material for DSA when a high etch resistance to Si etchants is required. PDMS has an inorganic Si-O backbone and as such offers superior etch resistance relative to organic polymers.

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Figure 14. (a) A schematic of the structure of PS-*b*-PDMS and 62 the structure formed by DSA. (b) SEM image showing large- 63 scale alignment of PDMS lines produced by the graphoepitaxy of 64 PS-*b*-PDMS within 10 μ m wide, PDMS brush coated trenches etched in a Si wafer. (c) Higher magnification images of the 65 aligned PDMS lines. (d) FFT of the image in (b) consistent with 66 excellent long-range ordering. (e) Grazing incidence small angle 67 x-ray scattering (GISAXS) pattern generated from a 1 cm² area of 68 the PDMS line pattern.¹⁸²

The outlook for DSA is promising. DSA has already demonstrated the requisite resolution capabilities for continued de- 71 vice scaling outlined within the International Technology 72 Roadmap for Semiconductors (ITRS), defect density levels are 73 dropping with continued research investment and issues re- 74 garding production of device specific geometries appear to be 75 resolvable using chemical epitaxy approaches.¹⁷⁹ LER and CD 76 control issues also need to be addressed to meet ITRS specifi- 77 cations.¹⁷⁹ Theoretical models predict LER to be related to χ 78 0^{0.5}, in which case, BCP systems with high χ values such as PS- 79 *b*-PDMS ($\chi \sim 0.26$ at room temperature) are worthy of further 80 investigation.¹⁸²

Self-assembly of cylinder and sphere forming BCPs has also 82 been used to produce ordered arrays of metal nanoparticles by 83 both additive¹⁹³ and subtractive¹⁹⁴, processes. These metal 84 nanoparticles may then be used to produce epitaxial growth of 85 semiconductor nanowires by means of the relevant techniques 86 outlined in Section 2. Furthermore, the metal nanoparticles may be used as etch masks to produced ordered arrays of vertical nanowires by a top-down approach. The use of BCP 88 films to template catalysts for epitaxial nanowire growth and 89 to template hard masks for top-down vertical nanowire array 90 formation is an example of a synergistic process, employing 91 both bottom-up and top-down methods. This synergistic process is to date, a poorly explored application of BCP lithography which warrants further investigation. 94 DSA is a promising blend of top-down and bottom-up tech-95

niques for advanced lithography applications. DSA allows a 96 route to increased pattern resolution and feature density rela-97 39 tive to conventional optical lithographic means, and whilst 98 40 concerns still exist over LER, CD control and reproducibility, 99 41 42 these concerns are gradually being improved by continued advances in the field. DSA depends on conventional lithogra-43 44 phy techniques such as optical lithography, interference lithog-45 raphy and EBL to form guiding templates to direct the self-46 assembly of BCPs and as such it will remain a complementary

lithography technique. However, if and when the issues associated with DSA are resolved, this lithography technique may alleviate the growing demands on optical lithography and EUV for continued device scaling, thus extending the use of current optical lithography techniques in VLSI manufacturing.

4.2. Lithographic Catalyst Placement for Bottom-Up Nanowire Growth

EBL is a suitable tool for the preparation of ordered arrays of metal nanoparticles by subtractive or additive processes. Ordered arrays of metal nanoparticles can be readily prepared using a positive tone EBL process to generate a metal lift-off mask.^{25,88,97,195} This process can be used to produce epitaxial nanowire growth via a VLS-type mechanism through careful control of the metal substrate interface, and choice of an appropriate substrate material, using nanowire growth methods such as those outlined in section 2. Coupling EBL and self-assembly of BCPs allows the production of defect free high-density arrays of dot structures.¹⁹⁶

Similarly, phase shift lithography and interference lithography have been shown to be capable of producing very fine dot structures for the fabrication of metal nanoparticle arrays.^{197,198} Metal nanoparticle arrays formed by these methods, too, could be used for the fabrication of nanowire arrays by bottom-up means.

4.3. Nanosphere Lithography

Nanosphere lithography (NSL) can be used to produce ordered arrays of vertical nanowires. NSL uses the bottom-up self assembly of spherical particles, such as polystyrene spheres, to create dot/anti-dot arrays on the surface of a substrate, which then may be used to transfer the pattern to the substrate creating structures such as vertically aligned nanowire arrays.^{21,199–201} NSL can be used to produce arrays of vertical Si nanowires using a metal-assisted etching approach as shown in figure 15 below. Combined use of NSL and metal-assisted etching (MAE) provides a route to forming arrays of long (> 10 μ m) Si nanowires which have applications in fields such as vertical ICs and solar cells (figure 15).²¹ NSL can also be used to create an anti-dot array mask for the evaporation of arrays of metal nanoparticles for use as catalysts for epitaxial nanowire growth.¹⁹⁹

4.4. Miscellaneous Synergistic Nanowire Fabrication Processes

A range of processes exist which use both bottom-up and topdown techniques in tandem to produce semiconductor nanowires. One example of such a technique is the supperlattice nanowire pattern transfer (SNAP) technique.²⁰² The SNAP technique is based on the formation of a stamp by selectively etching one of the layers in a superlattice material grown by a bottom-up epitaxy technique, such as MBE. Angular deposition of a metal on the etched superlattice then allows creation of a metal stamp which is pressed against the material of choice producing a metal grating which acts as an etch mask for the fabrication of nanowire arrays by pattern transfer.



Figure 15. Schematic of NSL process for the fabrication of verti cal Si nanowire arrays via MAE.^{201,203}

4 Figure 16, shows a schematic of the SNAP process. The 5 SNAP process has been used successfully to produce arrays of 6 Si nanowires from SOI, as well as metal nanowires formed 7 directly from the stamp. However, the technique is limited in 8 terms of the geometries of the structures that can be produced, 9 and the complexity of the process for large-scale nanowire 10 fabrication. Furthermore, the SNAP technique is susceptible 11 to many of the pitfalls associated with NIL outlined in Section 12 3.2. NIL can be used to created arrays of metal nanoparticles for bottom-up nanowire growth.²⁰⁴ This process involves im-13 14 printing a bilayer positive-tone resist, developing the imprint-15 ed resist and evaporating a metal layer to produce arrays of 16 metal nanoparticles by lift-off. The metal nanoparticles can 17 subsequently be used as catalysts for nanowire array produc-18 tion by standard nanowire growth procedures.

19 AAO membranes with HCP pore arrangements are formed by 20 a bottom-up process, as discussed in Section 2.2. When pre-21 pared as thin films, these ordered porous AAO membranes can 22 be used as masks to produce patterned metal films on Si sub- 48 $\overline{23}$ strates for MAE of Si, producing ordered arrays of vertical Si 24 25 nanowires.^{205,206} MAE techniques usingpatterned metal layers are successful at producing dense, ordered arrays of vertical 50nanowires with high aspect ratios. However, as with all MAE $\frac{51}{52}$ 26 techniques, the nanowires produced have rough sidewalls thus 52 $\overline{27}$ inhibiting their use in logic applications where surface scatter-ing of charge carriers is a significant drawback.^{201,207} 28 29 54



Figure 16. Schematic of the SNAP process for production of aligned nanowires.²⁰²

Nanowires produced by these methods are likely to find applications in solar cell, thermoelectric generator, sensor or battery anode applications where the increased surface area of nanowires with rough sidewalls may be beneficial to device performance.^{208,209}

Ion track etched membranes are an example of another nanowire template material. These membranes are formed in a top-down process by ion etching of a polymer material, producing cylindrical or tapered pores. Infilling ion track etched membranes by methods such as electrodeposition can produce arrays of nanowires.²¹⁰ Whilst this method can be used to produce some interesting network structures (figure 17), it is unlikely to find use in VLSI manufacturing due to the complexity of the process and the difficulty producing singlecrystalline materials within these membranes.



Figure 17. SEM images of polycrystalline Pt nanowire networks produced within ion track etched membranes: (a) low magnification SEM images of Pt nanowire networks, (b) high magnification SEM image of nanowire junctions and (c) cross-section of a nanowire network composed of 35 nm diameter nanowires.

1 5. Emerging Semiconductor Nanowire Materials

5.1. High Mobility Materials for Next Generation 63 CMOS Devices 64

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65 4 High charge carrier mobility materials have been subject to significant research investigation in the past few decades. 66 5 These materials offer increased transconductance relative to 67 6 Si, and as such, devices constructed from these materials may $\frac{68}{62}$ 7 achieve similar drive current at lower power, or operate as $\frac{69}{2}$ 8 9 high performance devices at equivalent power, to current Si $\frac{70}{20}$ 10 devices.²¹¹ Many materials are under consideration for inte- $\frac{71}{2}$ gration in future CMOS devices due to their increased charge 72 carrier mobility relative to Si.^{12,211–213} Ge, for example, exhib-7311 12 its hole mobility over four times that of Si, and as such is a $\frac{74}{2}$ 13 strong contender for use in future p-FET devices. Likewise, 75 14 InSb, InAs and graphene demonstrate massively increased 76 15 electron mobility relative to Si.^{212,214} However, these high 77 16 mobility materials are not without their drawbacks. Often, Ge $\frac{78}{28}$ 17 and III-V materials possess complex native oxides with poor $\frac{79}{22}$ 18 chemical or electrical properties for device fabrication.¹¹² 80 19 GeO_2 , a component of the complex native oxide on Ge crys-8120 tals, is water soluble and as such must be removed or capped $\frac{82}{32}$ 21 with a more suitable material to facilitate processing steps 83 involved in device manufacturing. Additionally, GeO, another 84 22 23 component of the native oxide on Ge, desorbs at temperatures 8524 above 400 °C, which may result in detrimental effects on over- 86 25 26 lying layers during annealing steps in device manufacturing. 87 Similar difficulties have been reported for III-V materials such 88 27 as GaAs and $In_{1-x}Ga_xAs$, whose complex native oxides prevent $\frac{89}{32}$ 28 the formation of a stable semiconductor-insulator interface. 90 The result is a high density of interface states at the semicon- 91 ductor-insulator interface in the gate stack.^{111,215} Interface 92 states often lie meet the semicon- 92 29 30 31 states often lie near the mid band-gap of the semiconductor 93 and can lead to Fermi-level pinning at the semiconductor sur-94 32 33 face. Fermi-level pinning can result in a number of detri-95 34 35 mental effects on device performance, including, rectifying 96 36 characteristics in metal-semiconductor contacts, and depletion 97 of free charge carriers in the device channel at the semicon-98 ductor-insulator interface.^{104,216} Interface states result from 99 37 38 39 unsaturated surface atoms, which act as charge acceptors and 0040donors at the semiconductor surface. Consequently, reduction 01 41 of the density of interface states is dependent on the formation 10242 of a stable and saturated semiconductor surface. There have 0343 been significant investigations into improvement of the elec 104 44 trical and chemical interfaces with these materials to facilitate 0545 their integration within next generation CMOS devices. The 06use of a capping Si layer of the order of a few monolayers 07 46 47 thickness has been successful in reducing the density of inter-48 face states (D_{ii}) in GaAs from $10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ to $10^{11} \text{ cm}^{-2} \text{ eV}^{1}08$ 49 $^{1.215}$ Similarly, deposition of SiO₂ directly on an untreated Ge Ω O surface results in a relatively high D_{it} of 10^{13} cm⁻² eV⁻¹, whilst 10 50 formation of a Ge₍₁₀₀₎/GeO_N/HfO₂/Pt gate stack produced 411 D_{ii} of 3×10^{11} cm⁻² eV⁻¹.^{111,112} A further promising route to 11251 52 53 ward improving the interface of inorganic semiconductor mail 13 54 terials with gate-dielectric layers may be through the use of an 14 appropriate organic dielectric material chemically tethered tq 15 55 the semiconductor. Extensive research has been pursued in 1656

the field of chemical functionalisation of Ge and III-V surfact 17se with high coverage of organic ligands.^{217–219} High-*k* organiq 18

59 gate-dielectrics have been investigated primarily for use with 19

60 organic FET devices, and have demonstrated competitive lev_{120}

els of performance when compared with current VLSI devices.²²⁰ Consequently, the molecular tethering of high-*k* organic molecules directly to these surfaces may allow a route to high*k* insulating layers with low D_{it} , thus improving device performance.

Graphene has demonstrated impressive electrical performance in reported device applications with charge carrier mobilities as high as 230000 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$.²²¹ However, there are a number of outstanding concerns with regard to the integration of graphene in VLSI manufacturing. Firstly, pristine graphene is a zero-gap semi-metal and as such exhibits poor switching behaviour in logic device applications. Significant efforts have been made to introduce a large and reproducible band-gap into graphene. These efforts have included quantum confinement of graphene within graphene nanoribbon (GNR) structures, doping, edge functionalisation and use of bilayer graphene.²²¹ Additionally, there are serious concerns regarding graphene processing for device fabrication. Production of large area, single layer graphene is a challenging task, and handling such a delicate material has associated difficulties. Metals and gate-oxides exhibit poor adhesion to graphene and graphene layers are extremely vulnerable to plasma induced damage.² Despite the many concerns regarding implementation of graphene in CMOS manufacturing, it maintains a massive research impetus and is firmly implanted on the ITRS for continued investigation.¹²

Similarly, carbon nanotube (CNT) structures have been investigated heavily for use as FET semiconductor channels and as metallic interconnect materials.²²³ The primary difficulty with CNT material preparation for FET and interconnect applications is controlling the electronic band structure of the material, which is dependent on CNT growth direction, and diameter.²²⁴ Furthermore, CNTs are subject to alignment and integration issues inherent to bottom-up nanowire and nanotube synthesis techniques as outlined in section 2.2.

The introduction of high-*k* dielectric materials in the gate stack of the active devices in VLSI manufacturing in recent years has paved the way for the introduction of high mobility, non-Si materials for FET applications. Materials such as Ge and III-Vs have long been held back by issues associated with their complex native oxides. However, the transition of the semiconductor industry from a SiO₂ gate dielectric to materials such as HfO₂, Al₂O₃ and ZrO₂,⁵⁹ has reignited interest in these high mobility materials. Consequently, there has been heavy research investment in the preparation of high-*k* materials on high mobility materials in recent years.^{111,112}

6. Nanowire Fabrication Outlook

The continued scaling of semiconductor devices in the VLSI industry has created a landscape where the introduction of nanowire or nanoribbon devices into mass production seems increasingly likely. As the density of semiconductor devices in VLSI architectures increases there has been an associated shift of the semiconductor channel from a planar orientation, to the recently developed fin structure where the semiconduc-tor channel is raised above the surface of the Si wafer. A natural progression from the finFET or tri-gate structure would appear to be a nanowire structure, be it lateral – parallel to the substrate – or vertical. The benefits of nanowires have been highlighted for a number of years now. Semiconductor nan-

owires allow production of GAA devices which offer superior 60
 control of the device channel and thus improved switching
 speed and on/off ratios. A nanowire structure can also be used
 to create quantum well, core-shell structures with improved
 electrical transport properties relative to standard structures.
 Nanowires may also incorporate strain, a prerequisite in cur rent VLSI devices^{16,225,226}, through the incorporation of do pants or a lattice mismatched shell material.^{227,228}

9 The exact fabrication route to future semiconductor nanowire-10 based integrated circuits is as yet, unclear; however, it is quite 11 probable that the route will incorporate both top-down and 12 bottom-up techniques in tandem to allow a scalable path to 13 nanowire integrated circuit fabrication. Bottom-up nanowire 14 growth processes allow routes to structures that may not be 15 produced by top-down means, and also may allow production 16 of exotic channel materials that may not be accessible in the 17 bulk wafer form. Bottom-up grown semiconductor nanowires 18 often exhibit faceted surfaces that may not be achieved by top-19 down fabrication. Control of the crystal surface facets formed 20 during nanowire growth, may allow control over the density of 21 22 interface states formed at nanowire surfaces, which is particularly important for Ge and III-V materials to develop improved 61 $\overline{23}$ device performance. Top-down processes such as optical and 62 24 electron beam lithography consistently demonstrate their supe-63 25 riority in the nanometre control of device definition and placement. DSA of BCP films is an example of the synergis- 64 26 27 tic cooperation of a bottom-up self-assembly process and tra-65 ditional top-down lithography, allowing routes to aligned pat- 66 28 29 tern multiplication, which is not feasible by either technique 30 alone. As such, a conservative prediction would be that future 31 nanowire-based electronics will be fabricated by a cooperative 6732 mix of both bottom-up and top-down processes. 33 Table 1, summarizes the achievable minimum feature sizes, 69 34 and potential feature pitch, using a number of top-down and 35 synergistic fabrication processes. All of the techniques listed 70in table 1 are suitable for the fabrication of nanowire arrays. 71 36 37 However, the choice of a suitable technique for the fabrication, of a particular nanowire system requires the consideration of $\frac{72}{73}$ 38 39 all aspects of the fabrication technique, and not merely the 40 ultimate resolution. AAO for example is usually used to pre-74 pare arrays of nanowires oriented vertically with respect to a 75 41 42 substrate. Interference lithography is suited to the fabrication 43 of linear arrays of nanowire structures and does not typically 26 of linear arrays of nanowire success $\frac{1}{78}$ allow routes to arbitrary shapes and nanowire layouts such as $\frac{1}{78}$ 44 45 those achievable via top-down optical lithography or directwrite charged particle lithography. Consequently, considera-79 46 47 tion of a number of fabrication techniques may be required 48 when developing a nanowire fabrication process, and the ben-80 49 efits and drawbacks of each technique should be carefully 81 50 weighed against one another so as to identify the technique 51 best suited to the fabrication of the desired product. 83 52 53 84 54 85 86 55 56 57 58

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Fabrication Technique	Minimum Feature Size	Linear Feature Pitch
Top-Down Optical Lithography	< 10 nm	< 40 nm ¹⁴⁶
Interference Li- thography	< 15	$< 25 \text{ nm}^{133,198}$
Direct-Write Charged Particle Lithography	< 5 nm	< 10 nm ¹⁵⁵
NIL	< 10 nm	$< 20 \text{ nm}^{142}$
SPL	< 1 nm	$< 2 \text{ nm}^{172}$
DSA	< 5nm	$< 20 \text{ nm}^{179,229}$
AAO	< 20 nm	$< 50 \text{ nm}^{230}$
Bottom-Up EBL Synergy	< 30 nm ²⁵	< 500 nm
NSL	< 15 nm	$\sim 200 \text{ nm}^{231}$

Table 1. Minimum feature sizes and potential minimum linear feature pitch achievable by a number of top-down and synergistic lithography techniques.

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Table of Contents Figure

Richard G. Hobbs,	This review article highlights	
Nikolay Petkov and	the important considerations	
Justin D. Holmes	required for the continued ad- vancement of semiconductor	
Semiconductor Nanowire Fabrication by Bottom-Up and Top-Down Paradigms	nanowire fabrication for next- generation field-effect transis- tor devices.	