Electrochemical Materials for Integrated Magnetics

A thesis submitted for the degree of Doctor of Philosophy (Ph.D.) in Engineering Science by

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Research supported by Science Foundation Ireland under the ADEPT Project No. 15/IA/3180 "Advanced Integrated Power Magnetics Technology - From Atoms to Systems" for which Prof. Cian O'Mathuna is the Principal Investigator.

The required precision demands that the model be a mathematical one, for otherwise one cannot be sure that these questions have well-defined answers.

– Roger Penrose, *The Road to Reality* (2004)

To my amazing parents, loving wife and everyone who has supported me along the way.

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Declaration

This is to certify that the work I am submitting is my own and has not been submitted for another degree, either at University College Cork or elsewhere. All external references and sources are clearly acknowledged and identified within the contents. I have read and understood the regulations of University College Cork concerning plagiarism.

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Daniel Smallwood

Acknowledgements

I wish to express my sincere gratitude to my supervisors, Dr. James Rohan and Dr. Paul McCloskey, for welcoming me into their research groups at Tyndall National Institute. Their scientific guidance, mentorship and vast knowledge of electrochemistry, physics and integrated magnetics greatly assisted in the momentum of this work. I wish to say a special thank you to the PI of our research project, Prof. Cian O'Mathuna, for his support, encouragement and inspirational leadership. I'd also like to express my gratitude to Prof. John Hayes for the engaging and insightful lessons in power electronics.

Thank you to all my friends and colleagues in both the Electrochemical Materials and Energy and the Integrated Magnetics groups. I especially wish to thank Declan Casey for his valued comradery and for assisting with many of the technical challenges of fabrication. Thank you to the amazing ADEPT project team: Darragh Cronin, Liang Ye, Daniel Lordan, Guannan Wei, Youssef Kandeel, Maeve Duffy and Chandra Shetty. I've really enjoyed being part of such a brilliant and motivated group of individuals.

There are so many people at Tyndall who have assisted me along the way. In particular, I wish to thank: Finbarr Waldron, Ann Foley, Richard Murphy, Joe O'Brien, Alan Hydes, Alan Blake, Lorraine Nagle, Paul Tassie, Krimo Khalfi, Dermot Houston, Vince Lodge, John Cashman, Ricky Anthony, Michael Schmidt and Tomás Clancy. Thank you to my thesis committee for their valuable advice and many discussions that shaped the path of my PhD. Thank you to Fatima Gunning, Willie Lawton and Ian Povey for their guidance and support throughout my postgraduate journey. Thank you to James O'Callaghan and Dara Fitzpatrick for giving me the opportunity to develop and share my passion and enthusiasm for teaching at the graduate and postgraduate level. Thank you to Alida Zauers for organizing so many great STEM outreach events, which I've enjoyed taking part in. Thank you to Prof. Eoin O'Reilly for reviewing and providing insightful commentary on our manuscript. Thanks to Julie Donnelly, John Slabbekoorn, Paul Roseingrave and Andy Miller for assisting with the imec ASCENT project. Thank you to Science Foundation Ireland for funding this research.

To my fellow colleagues, collaborators, PhD students and postdocs at Tyndall and UCC, thank you for the many engaging discussions, your friendship and for making this journey so enjoyable. A special thanks to Pranay Podder, Ansar Masood, Zoran Pavlović, Louise McGrath, Fiona Barry, Hasan Baghbaderani, Hugh Smiddy, Seamus O'Driscoll, Declan Jordan, Ruaidhrí Murphy, Zahra Ghaferi, Ehren Dixon, Mary Kent, Eilís Mulcahy, Sinead O'Sullivan, Orla Slattery and Jim Greer.

I'm deeply grateful to my family, friends and in-laws for all the fun times in between long hours of research, which included discovering the wild beauty of Ireland and fossil hunting on England's Jurassic coast. I especially wish to thank my mom and dad, Kristin and Chuck, for their endless love, support and advice. Finally, I am eternally grateful to my amazing and loving wife, Catherine. Thank you for always encouraging me to follow my dreams.

List of Acronyms

24/7	24 hours per day, 7 days per week
AC	Alternating Current
AI	Artificial Intelligence
ALD	Atomic Layer Deposition
AR	Aspect Ratio
ASIC	Application Specific Integrated Circuit
BIC	Bottom Interconnect
BTA	1,2,3-Benzotriazole
CAD	Computer Aided Design
CAGR	Compound Annual Growth Rate
CCM	Continuous Conduction Mode
CED	Critical Exposure Dose
CMOS	Complementary Metal-Oxide-Semiconductor
CMP	Chemical Mechanical Polishing
CPU	Central Processing Unit
CTE	Coefficient of Thermal Expansion
CVD	Chemical Vapor Deposition
DC	Direct Current
DG	Deformed Geometry
DI	Deionized
DM	Digital Matrix
DMSO	Dimethyl Sulfoxide
DRAM	Dynamic Random Access Memory
DRIE	Deep Reactive Ion Etching
D:SS	Diameter to Step Size Ratio
DUV	Deep Ultraviolet
e.g.	Exempli Gratia
EBR	Edge Bead Removal
ED	Exposure Dose
EDX	Energy Dispersive X-Ray

EHT	Electron High Tension
EM	Electromagnetic
EMF	Electromotive Force
EMI	Electromagnetic Interference
ESW	EBR Stream Width
FAR	Floor Area Ratio
FC	Flip-Chip
FEM	Finite Element Method
FEPA	Federation of European Producers of Abrasives
FIB	Focused Ion Beam
GPU	Graphics Processing Unit
GSGSG	Ground Source Ground Source Ground
HAR	High Aspect Ratio
HBM	High Bandwidth Memory
HDD	Hard Disk Drive
HF	High Frequency
HTC	Heat Transfer Coefficient
I/O	Input/Output
IC	Integrated Circuit
ID	Identifier
IoT	Internet of Things
IRDS	International Roadmap for Devices and Systems
ISO	International Standards Organization
ITRS	International Technology Roadmap for Semiconductors
IVR	Integrated Voltage Regulator
JGB	Janus Green B
KMC	kinetic Monte Carlo
l/s	Line to Space
LCR	Inductance, Capacitance and Resistance
LF	Laminar Flow
LIGA	Lithography Electroplating and Molding
LP	Long Pass

MEMS	Microelectromechanical Systems
MM	More Moore or Moving Mesh
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPS	3-Mercapto-1-Propanesulfonic Acid
MtM	More than Moore
N/A	Not Applicable
NA	Numerical Aperture
NEMS	Nanoelectromechanical Systems
OB	Open Boundary
PC	Personal Computer
PEB	Post Exposure Bake
PECVD	Plasma Enhanced Chemical Vapor Deposition
PEG	Polyethylene Glycol
PGMEA	Propylene Glycol Monomethyl Ether Acetate
PMIC	Power Management Integrated Circuit
PMMA	Poly(Methyl Methacrylate)
PoL	Point-of-Load
PoS	Point-of-Source
PPG	Polypropylene Glycol
PPR	Periodic Pulse Reverse
PR	Photoresist
psi	Pounds Per Square Inch
PVD	Physical Vapor Deposition
PwrSiP	Power Supply in Package
PwrSoC	Power Supply on Chip
R&D	Research and Development
RDL	Redistribution Layer
RF	Radio Frequency
rpm	Rotations Per Minute
RT	Room Temperature
SEM	Scanning Electron Microscope
SFI	Science Foundation Ireland

SiP	System in Package
SMPS	Switch-Mode Power Supply
SoC	System on Chip
SOP	Standard Operating Procedure
SPS	Bis-(3-Sulfopropyl) Disulfide
SQUID	Superconducting Quantum Interference Device
SSD	Solid State Drive
STP	Standard Temperature & Pressure
TCD	Tertiary Current Distribution
TDS	Technical Data Sheet
TIC	Top Interconnect
TMAOH	Tetramethylammoniumhydroxide
TPV	Through Polymer Via
TSV	Through Substrate/Silicon Via
UV	Ultraviolet
VIA	Vertical Interconnect Access
WD	Working Distance
WLVP	Wafer Level Vacuum Packaging

List of Symbols

$-$	Null field
$	Dollars
%	Percent
$\Delta I_{L(p-p)}$	Inductor ripple current magnitude
A_1	Transmitted attenuating path length
A_2	Internally reflected attenuating path length
C_0	Oxidized species concentration
C_F	Fixed costs
C_R	Reduced species concentration
C_V	Variable costs
ED_{spec}	Specified aerial exposure dose
E_a	Activation energy
E_{eq}	Equilibrium voltage
I_{λ_i}	Aerial relative intensity fraction of the ith species
I_0	Bulb irradiance
I_D	Diode current
I_{HV}	High voltage current
$I_{L(max)}$	Maximum inductor current
$I_{L(min)}$	Minimum inductor current
I_{LV}	Low voltage current
I_Q	Transistor current
I_{max}	Maximum current
I_{sat}	Saturation current
K_p	Preston coefficient
$R_{p_{i1,2}}$	P-polarized reflection coefficient at interfaces 1 and 2
$R_{s_{i1,2}}$	S-polarized reflection coefficient at interfaces 1 and 2
R_{AC}	Alternating current resistance

R_{DC}	Direct current resistance
R_{i1}	Reflection coefficient at interface 1
R_{i2}	Reflection coefficient at interface 2
T_S	Switching period
U_0	Unattenuated light amplitude
V_{HV}	High voltage value
V_{LV}	Low voltage value
Z'	Impedance real part
Z''	Impedance imaginary part
e^-	Electron
f_S, ω	Switching frequency
g_1	Non-attenuating path length
g_2	Refraction-adjusted non-attenuating path length
i_0	Exchange current density
i_{loc}	Local current density
i_p	Pulse current
i_{rev}	Reverse current
k_B	Boltzmann's constant
t_{off}	Off time
t_{on}	On time
t_{rev}	Reverse time
$\vec{u}$	Velocity vector
u_0	Aperture plane light amplitude
v_P	Pole voltage
Φ_B	Magnetic flux
α_a	Anodic transfer coefficient
α_c	Cathodic transfer coefficient
μ_0	Vacuum permeability
μ_r	Relative permeability/Large relative permeability value
μ_r'	Small relative permeability value

ϵ_0	Vacuum permittivity
ϵ_r	Relative permittivity
ΔT	Temperature difference
°	Degrees
~ or ≈	Approximately equal to
$°C$	Degree Celsius
μm	Micrometer
Å	Angstrom
Ɛ	Electromotive force
h	Heat transfer coefficient/Hour
$h-line$	405 nanometer wavelength
$\mathrm{N}, \mathrm{W}, \mathrm{S}, \mathrm{E}$	The cardinal directions
κ	Dielectric constant
A	Ampere/Aperture/Area
A, B, C, D, E, F	Cauchy coefficients
Ag	Silver
Al	Aluminum
Au	Gold
B	Magnetic field strength/Boron
C	Coulomb
Co	Cobalt
Cu	Copper
D	Diameter/Diffusion coefficient/Diode/Duty cycle/Dimensional
E	Applied voltage
F	Faraday's constant/Fresnel number/Fluorine
Fe	Iron
G	Gate
H	Henries/Auxiliary magnetic field/Hydrogen
I	Current
$I(z)$	Luminous intensity

J	Joule/Diffusive flux
K	Degree Kelvin/Extinction coefficient
L	Inductor/Inductance/Characteristic length/Large inductance value
L'	Small inductance value
MHz	Megahertz
MX	Metal pitch of X
MY	Man years
N	Complex refractive index/Winding or turn number/Mass transport vector/Nitrogen
$N+$	Negatively doped
$P+$	Positively doped
Nd	Neodymium
Ni	Nickel
O	Occulter/Oxygen
Oe	Oersted
P	Power/Pressure
Pa	Pascal
Pt	Platinum
Q	Transistor/Switch/Quality/Rate of heat transfer
R	Ideal gas constant/Electrical resistance
Re	Reynolds number
S	Siemens/Spacing/Sulfur
Si	Silicon
T	Tesla/Thickness
Ta	Tantalum
Ti	Titanium
U	Attenuated light amplitude
V	Velocity/Volt
W	Watts/Tungsten
Y	Yttrium

Zr	Zirconium
b	Bulb relative intensity spectrum
c	Concentration
cP	Centipoise
cm	Centimeter
d	Edge-broadening magnitude
d, g	Air gap length
dm	Decimeter
e	The constant e
g	Gram
$g - line$	436 nanometer wavelength
i	The ith species/The imaginary unit
$i - line$	365 nanometer wavelength
k	Wavenumber
kHz	Kilohertz
keV	Kiloelectron volt
kg	Kilogram
l	Path length/Cell length
m	Meter
mA	Milliamp
mL	Milliliter
min	Minute
mm	Millimeter
mol	6.022×10^{23} units
n	The nth number/Refractive index
nH	Nanohenry
nm	Nanometer
ns	Nanosecond
pH	Picohenry
ppm	Parts per million

r	Radius/Electrical resistance
s	Second/Solid
t	Time
u	Flow velocity
wt	Weight
x	Radial point/Horizontal direction
y	Direction orthogonal to screen/page
z	Distance from photomask/Vertical direction/Ionic charge
Ω	Electrical resistance
$\nabla\emptyset$	Electric field potential gradient
∇c	Concentration gradient
α	Absorption coefficient
δ	Angle of incidence/Partial derivative
η	Dynamic viscosity/Overpotential
θ	Angle to the vertical line
λ	Wavelength
μ	Kinematic viscosity
π	The constant Pi
ρ	Density/Resistivity
φ	Substrate refraction angle

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Abstract

Next generation microinductors with magnetically enhanced VIA technology hold great promise for power converter applications in broad technology domains such as automotive, space, high-end computing, mobile devices, radio frequency (RF), artificial intelligence (AI) and the internet of things (IoT). Microinductor VIAs enable monolithic 3D device topologies with reduced footprint, increased inductance density and minimal parasitics. These qualities are essential for emerging 2.5/3D packaging architectures that require granular point-of-load (PoL) power delivery to efficiently supply a multitude of heterogeneously integrated devices.

This thesis addresses the challenges of 3D monolithic microinductor design and fabrication, inclusive of magnetically enhanced VIAs comprising a clad laminated soft magnetic core. The current state-of-the-art utilizes 2D microinductor topologies and 2D fabrication methods, therefore significant advancement is required to enable fabrication of a novel 3D monolithic microinductor device comprising vertically oriented integrated magnetics. The major challenges addressed in this thesis fall into two main categories: 1) predictive modeling with computational lithography and computational electrochemistry to enable optimization of the VIA formation process and 2) the design and fabrication of a novel magnetically enhanced monolithic 3D microinductor device.

A major contribution from the computational lithography is the derivation of a novel polychromatic light attenuation equation that is used to produce a succinct formula comprising a complete coupling between resist photochemistry and light diffraction effects. Additionally, new photoresist exposure dose determination methods are presented that negate the need for time consuming and costly in-situ metrology. These equations and methods enable fast and accurate predictive modeling of 3D photoresist VIA latent images, which are verified by comparison to directly corresponding experimental work, with highly positive correlation. These formulas converge quickly on the average modern computer and can be readily integrated into lithography simulators. Photoresist development is then investigated, wherein spin development is identified as the optimal method for wet etching VIA latent images. With computational electrochemistry, the electroforming process of Cu VIAs is explored using the FEM in COMSOL Multiphysics to perform 2D and 3D time-dependent simulation studies. Simulations are then verified by comparison to experimental results, with highly positive correlation. Special attention is given to electroformed surface topographies, which is valuable for sensor and flip chip applications.

The major contributions from the microinductor device design and fabrication first include designing a unique device that meets target specifications for reduced footprint, increased inductance density and minimized parasitics. A novel fabrication process flow is next engineered to enable a vertically meandering current path with a repeating unit cell comprising a bottom interconnect, a first Cu VIA, a top interconnect and a second Cu VIA. This process flow is compatible with conformal deposition of a soft magnetic laminate (e.g., CoZrTa) for formation of a vertically oriented magnetic core clad on the Cu VIAs. Next, a 5-tiered photomask stack is designed and the corresponding SOPs are engineered. This enables fully in-house microinductor device fabrication, after which vital metrology and characterization is performed. The measured inductance density of our prototype magnetically enhanced monolithic 3D microinductor devices is 10.36 nH/mm^2, which is comparable to previously

reported metrics for fabricated 3D microinductors. This metric could be significantly improved in future devices by increasing the magnetic core thickness and/or optimizing the magnetic anisotropy characteristic of the integrated magnetic material and/or reducing the pillar diameter, wherein the VIA fabrication research presented in this thesis will be essential. Therefore, this novel microinductor research holds great promise for applications in next generation power converters.

Chapter 1 - Introduction

A microinductor is a magnetic device that stores electrical energy in the form of a magnetic field. It is an essential component of modern integrated voltage regulators (IVRs), which use a radio frequency (RF) switch such as a metal-oxide-semiconductor field-effect transistor (MOSFET) to enable direct current (DC) voltage source modulation. This thesis investigates the design and fabrication of magnetically enhanced 3D microinductors with reduced footprint for point-of-load (PoL) power conversion in integrated circuits (ICs) and increased compatibility with emerging 2.5D and 3D advanced packaging architectures. These next generation microinductors hold great promise for power converter applications in technology domains such as automotive, space, high-end computing, mobile devices, radio frequency (RF), artificial intelligence (AI) and the internet of things (IoT). To understand the role of the microinductor in a power converter, a buck converter is first presented below.

1.1. Integrated magnetics for efficient DC-DC conversion with a buck converter

By alternating between on and off states, the MOSFET cyclically charges and discharges a microinductor, which powers a load during the MOSFET off state, as shown in Fig. 1.1.

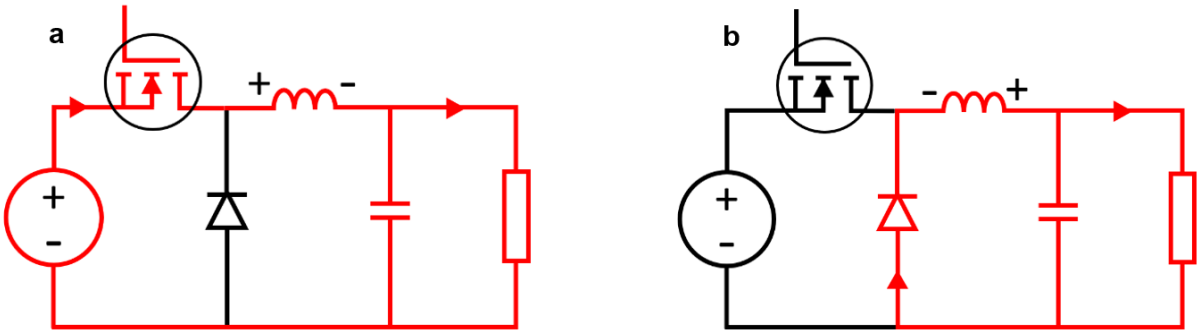

Figure 1.1. Buck converter inductor charging and discharging modes. a On-state. Current flows through the MOSFET and the inductor is charging. **b** Off-state. Current flows through the diode and the inductor is discharging.

The detailed operation of a buck converter is shown in Fig. 1.2, which depicts voltage and current waveforms during the MOSFET on/off states.

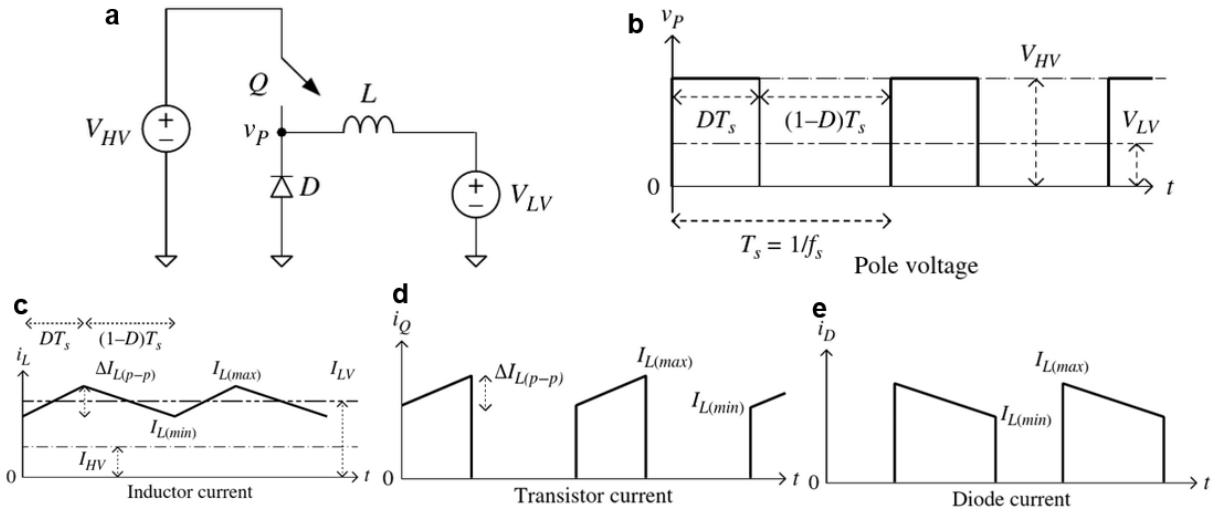

Figure 1.2. Buck converter operation in continuous conduction mode (CCM)[1]. **a** Buck converter schematic, where v_P is the pole voltage. **b** Pole voltage vs. time, where D, the duty cycle defined as $D = V_{LV}/V_{HV}$, sets the output voltage. $DT_s + (1-D)T_s = T_s$ is the switching period in s, which is the inverse of the switching frequency, $f_s = 1/T_s$ in s^{-1}. During DT_s, the switch is closed (MOSFET conducting), $v_P = V_{HV}$ and the inductor is charging. During $(1-D)T_s$, the switch is open (MOSFET not conducting), $v_P = 0$ and the inductor is discharging. **c** Inductor current vs. time. The inductor charges during DT_s and discharges during $(1-D)T_s$, where $I_{L(max)} - I_{L(min)} = \Delta I_{L(p-p)}$ is the current ripple magnitude. **d** MOSFET current vs. time. **e** Diode current vs. time. (**a-e** reprinted from ref. 1 with kind permission from John Wiley & Sons. Copyright 2018 John Wiley & Sons Ltd.)

As opposed to a linear power converter, the buck converter enables high efficiency step down of the supply voltage with minimal Joule heating, which is essential for modern electronic devices[2]. This is made possible by the energy storage capability of the microinductor, which operates by the principle of Faraday's Law of Induction, equation (1.1), where $\mathcal{E}$ is the electromotive force (EMF) in V, N is the number of inductor windings/turns and Φ_B is the magnetic flux in V·s [3].

$$\mathcal{E} = -N\frac{\partial \Phi_B}{\partial t} \tag{1.1}$$

Consequently, a time variant magnetic field induces an EMF with proportion to the number of inductor windings/turns. The magnetic field strength, B in tesla (T) or $kg \cdot s^{-2} \cdot A^{-1}$, as described by equation (1.2), is a function of μ_r, the relative permeability of a material, μ_0, vacuum permeability in $H \cdot m^{-1}$ or $kg \cdot m \cdot s^{-2} \cdot A^{-2}$ and H, the auxiliary magnetic field in $A \cdot m^{-1}$ [4].

$$B = \mu_r \mu_0 H \tag{1.2}$$

The magnetic field strength can be increased by using a material with a relative permeability greater than unity, which in-turn, boosts the induced EMF. As an example, some soft magnetic materials such as Metglas have a relative permeability of 1,000,000[5].

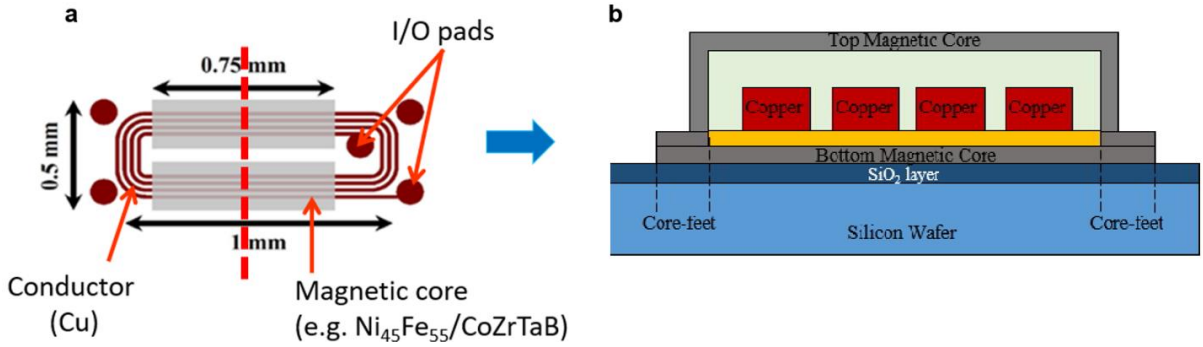

Figure 1.3. Magnetic core microinductor schematic and cross-section. a Top-down schematic of a magnetic core racetrack microinductor with four turns[6]. (Reprinted from ref. 6 with kind permission from IOP Publishing, Ltd. Copyright 2016 IOP Publishing, Ltd.; permission conveyed through Copyright Clearance Center, Inc.) **b** Cross-section of **a**[7]. (Reprinted from ref. 7 under the Creative Commons Attribution 4.0 International License.)

Therefore, in addition to the conductor cross-section and device topology, the energy storage capability of a microinductor is proportional to its size (e.g., the number of windings/turns) and is a function of its material properties. These parameters contribute to inductance (L), as described by equation (1.3), where L in units of henries (H) or $kg \cdot m^2 \cdot s^{-2} \cdot A^{-2}$ is equal to the ratio of the magnetic flux, Φ_B, to the current, I in A[8].

$$L = \frac{\Phi_B(I)}{I} \tag{1.3}$$

Consequently, the inductance is a measure of the energy storage capability of an inductor. An alternative formulation for the induced EMF is equation (1.4), where L is the inductance and I is the current[8].

$$\mathcal{E} = -L\frac{\partial I}{\partial t} \tag{1.4}$$

Since $\mathcal{E} \propto L$, the required inductance value is proportional to the amount of electrical energy that must be stored in the form of a magnetic field. Therefore, a high MOSFET switching frequency can be used with a low transient energy storage requirement, thereby enabling a small inductor footprint for granular PoL power conversion. Equation (1.5) demonstrates the inverse relationship between inductance and switching frequency[1] and Fig. 1.4. depicts a reduction in the inductor footprint as frequency is increased[9,10].

$$\Delta I_{L(p-p)} = \frac{V_{LV}D}{f_S L} \tag{1.5}$$

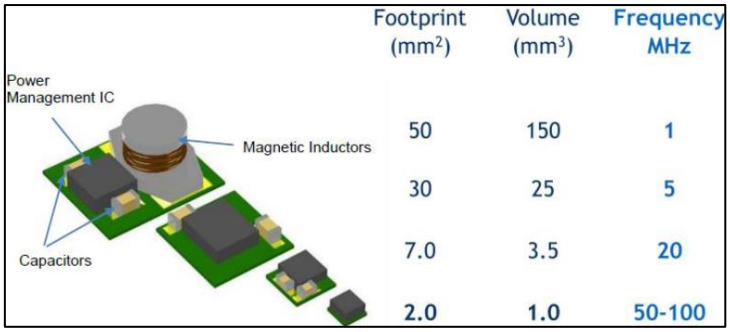

Figure 1.4. Inductor footprint vs. frequency[9,10]**.** (Reprinted from ref. 10 with kind permission from IEEE. Copyright 2010 IEEE.)

In addition to frequency related size reduction, the microinductor footprint can be further reduced by transitioning from a 2D to a 3D winding topology[11,12,13,14,15,16,17,18]. Using an architectural analogy, transitioning from a 2D to a 3D winding topology is equivalent to modifying the microinductor floor area ratio (FAR), whereby the gross floor area (microinductor volume) to plot area (substrate surface area) ratio is significantly increased, which is a core concept behind vertical architecture (e.g., skyscrapers)[19,20]. In 3D microinductors, a vertically meandering current path is enabled by selectively interconnecting an array of Cu pillars or through substrate vias (TSVs), as shown in Fig. 1.5.

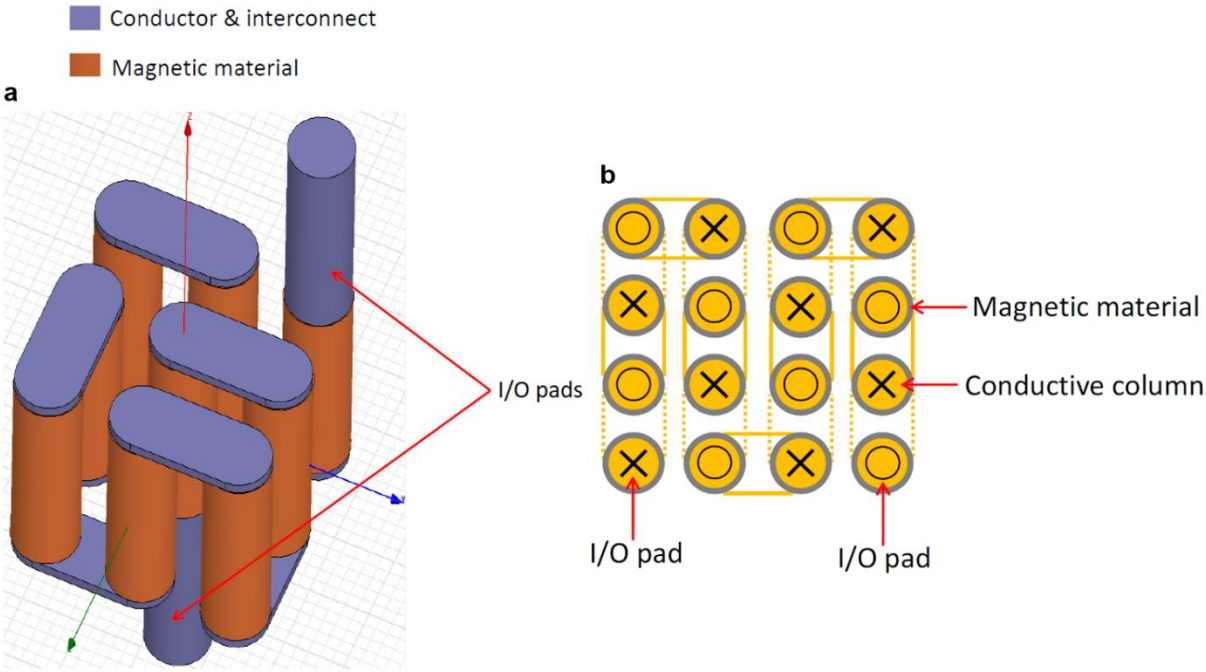

Figure 1.5. 3D microinductor schematics with Cu pillars laminated in a magnetic material[21]**. a** Angled view. **b** Top-down view. Downward traveling current is marked with an "X" and upward traveling current is marked with an "O".

For example, the four turn 2D microinductor depicted in Fig. 1.3a has a footprint of 0.5 mm^2, whereas an equivalent four turn 3D microinductor with 4x100 µm diameter square packed TSVs and a pitch of 200 µm would have a footprint of 0.09 mm^2, which is a size reduction of 5.6x (assuming equivalent device parameters (e.g., inductance, dc resistance, saturation current and operating frequency) and magnetic material parameters (e.g., resistivity, coercivity, saturation magnetization, relative permeability and anisotropy field)). Furthermore, laminating

the Cu pillars in a magnetic material significantly boosts inductance by equation (1.2), while simultaneously functioning as an in-situ shield against electromagnetic interference (EMI)[22,23]. Together, these design options offer a promising solution for next-generation microinductors with reduced footprint, in-situ EMI shielding, high inductance density and enhanced compatibility with emerging 2.5/3D packaging architectures.

1.2. Research goals and challenges

Goals:

1. Conduct a literature review on high-throughput (fast) and cost-effective (inexpensive) vertical interconnect access (VIA) fabrication techniques and reported 3D microinductors, wherein these qualities are essential for modern semiconductor manufacturing process flows.
2. Develop complementary metal-oxide-semiconductor (CMOS) compatible fabrication methods for next generation 3D integrated magnetic devices by incorporating novel magnetic lamination methods into the full device fabrication process flow. Herein, CMOS compatible refers to low-temperature (e.g., <200 °C) cleanroom processing (e.g., silicon wafers that are not contaminated with trace metals such as Ni, Fe, Ag, Au, etc.)[12,13].
3. Demonstrate high-throughput and low-cost scalable processing options for novel 3D micro-magnetic inductor structures, wherein scalability enables integration of small-scale, research laboratory process flows into high-volume industrial manufacturing.

Research challenges related to the achievement of Goals 2 and 3:

1. Diffraction effects degrade VIA mold resolution in photolithography. To address this, computational lithography is required to enable predictive modeling of diffraction effects during photoresist exposure. This entails:
    - Deriving a new polychromatic light attenuation equation for compatibility with broad-spectrum exposure, as is typical in mask aligner photolithography (e.g., with Hg bulbs),
    - Developing novel methods for photoresist cross-link determination, and
    - Using an exact scalar diffraction equation for a circular diffractor.
2. Electroplating is a complex process, wherein tailoring the topography of the electroplated surface (e.g., flat for flip-chip applications) requires knowledge of electroactive species mass transport dynamics and electrode reaction kinetics. To enable this, the finite element method (FEM) in COMSOL Multiphysics is needed to perform computational electrochemistry for predictive modeling of the Cu electroplating process.
3. Feasible 3D microinductor device design topologies that comprise Cu pillars clad in a vertically oriented magnetic material and arranged in a selectively interconnected array have not yet been explored. This design space needs to be investigated to identify promising prototypes, which must be enabled by utilizing wafer level layout for stacked photomask alignment through to tapeout.

4. Wafer transfer from the plating lab to the MEMS fabrication lab at Tyndall requires CMOS compatible Si wafers to enable sputtering of vertically oriented magnetic material on Cu pillars. A CMOS compatible process flow for fabricating Cu interconnects is thus required to enable monolithic microinductors comprising Cu VIAs clad in a laminated soft magnetic material.
5. Standard operating procedures (SOPs) for the novel fabrication process flow do not yet exist and must be engineered.
6. These novel magnetically enhanced 3D microinductors have never before been prototyped and must be fabricated with in-house equipment and processing.

1.3. Thesis scope

This thesis addresses the goals and challenges outlined in section 1.2, wherein the research was conducted at the interface between lithography, electrochemistry and integrated magnetics. The key research focus was to advance the state-of-the-art by transitioning from 2D microinductors to 3D magnetically enhanced monolithic microinductor device topologies for scalable applications in power supply in/on package/chip (PwrSiP/PwrSoC) and 2.5/3D advanced packaging architectures. Fundamental to this goal was the development of a high-throughput and cost-effective VIA fabrication method for use in a novel 3D magnetically enhanced microinductor device design. Notable research requirements included computational lithography, computational electrochemistry, device design, process design, establishing SOPs and performing continuous validation with metrology and characterization. Furthermore, my research culminated in spearheading a full microinductor device fabrication effort, which resulted in fabricated prototypes of novel 3D magnetically enhanced microinductors.

Chapter 2 (Goal 1) first establishes the context of cutting-edge VIA applications in 2.5D and 3D advanced packaging architectures, microelectromechanical systems (MEMS) and emerging microinductor devices. Following this, VIA fabrication methods are discussed, wherein photolithography is identified as a promising fabrication option. A detailed review of thick photoresists is then presented and THB-151N is selected as a suitable photoresist. Finally, reported 3D microinductors with VIAs are reviewed and a microinductor device comprising VIAs clad in magnetic laminations is proposed as a novel design option.

Chapter 3 (Challenge 1) addresses the role of light diffraction effects in photolithography, which can significantly affect the target photoresist relief mold geometry. A new polychromatic light attenuation equation is derived, presented and applied along with an exact scalar diffraction formula to enable predictive modeling of VIA latent image profiles in Wolfram Mathematica. VIA latent image simulations are then compared to directly corresponding experimental work, with highly positive correlation. The mechanism of photoresist development, wherein a latent image is etched into a relief mold, is next investigated and spin development is suggested as a suitable development methodology.

Chapter 4 (Challenge 2) uses the FEM in COMSOL Multiphysics to simulate 3D electrode growth during Cu VIA electroplating. The fundamental mass-transport and reaction kinetics equations are discussed and implemented in four distinct physics modules, which are then combined into a multiphysics time-dependent simulation. Consistency checks are performed between 2D and 3D electrode geometry growth simulations, which are then compared to

directly corresponding experimental work, with highly positive correlation. This study provides insight into the electroforming process of Cu VIAs with special attention to pillar topography.

Chapter 5 (Goals 2-3, Challenges 3-6) describes the target 3D microinductor device design, process design, photomask layout/design, key aspects of the generated SOPs, key fabrication steps and the corresponding characterization and metrology. The target device design is presented in a detailed 2D x-z cross-sectional schematic, which is achieved by a 16-step process flow. The layout designs entail a 5-tiered photomask stack for fabricating 14 discrete 3D microinductor devices on a single 4" wafer. Key aspects of the corresponding SOPs and challenging fabrication steps are then discussed with a special focus on chemical mechanical polishing (CMP). Finally, light microscope, scanning electron microscope (SEM) and X-ray images of the fabricated 3D microinductor devices are presented along with the corresponding metrology and characterization results.

Chapter 6 provides a summary of the thesis and discusses potential future work. A promising future option for high aspect ratio (HAR) VIA fabrication with photolithography is to use an in-situ photomask. This technique eliminates the photomask air gap while simultaneously introducing a long pass (LP) filter, which could prove highly effective for reducing diffraction effects. This fabrication option could first be simulated in Wolfram Mathematica with my VIA latent image model, which would greatly assist in HAR VIA fabrication. Additionally, and for high frequency (HF) applications, a thick dry film could be utilized for thickness uniformity and to enable hollow VIA fabrication with minimal electroplating duration. Both of these VIA fabrication options are promising for realizing advanced 3D microinductors with maximum efficiency, minimum footprint and enhanced compatibility with emerging 2.5/3D packaging architectures. Furthermore, and due to its high-throughput capability, my latent image model could be developed into an on-the-go app for ease of use during experimentation in the laboratory. Finally, and as an alternative to sputtering, Cu pillars clad in a vertically oriented laminated soft magnetic core could be realized by selectively etching Cu in an electroplated $[Ni_{45}Fe_{55}/Cu]_n$ stack and back filling with a low viscosity photoresist for mechanical stability.

Click to skip to next chapter.

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Chapter 2 – State-of-the-art: VIAs in 2.5D and 3D advanced packaging architectures, MEMS and emerging microinductor devices

2.1. Introduction

Omnipresent in the semiconductor industry, Moore's law states that the number of metal-oxide-semiconductor field-effect transistors (MOSFETs) in a microchip doubles every 1.5-2 years[1]. The predictive power of Moore's law held firm throughout the 1970s and well into the 21st century[1]. However due to fundamental limits such as the quantum tunnelling property of electrons causing off-state leakage currents, as required by Heisenberg's uncertainty principle[1], transistor scaling is predicted to slow pace so significantly that in 2015 even Moore himself stated that, "I see Moore's law dying here in the next decade or so"[2]. Correspondingly, the International Roadmap for Devices and Systems (IRDS) More Moore (MM) focus team reported in 2020 that MOSFET scaling is expected to saturate by around 2028 with a half-pitch of 7-8 nm, as shown in Fig. 2.1[3].

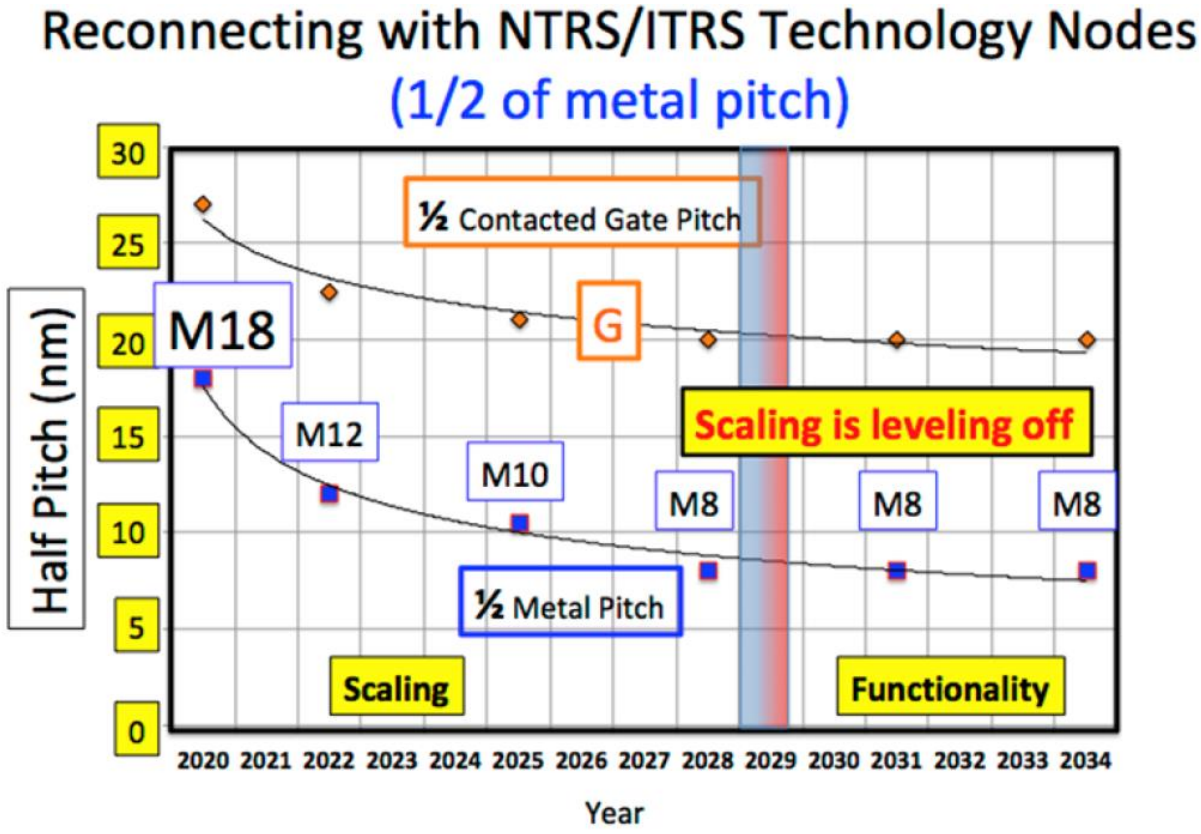

Figure 2.1. CMOS dimensional scaling projection from 2020-2034[4]. (Reprinted from ref. 4 with kind permission from IEEE. Copyright 2020 IEEE.)

With the end of MOSFET scaling on the horizon, demand is nevertheless accelerating for enhanced mobile devices, advanced sensors and high-end computers with increased functionality, minimal power loss and maximum power density. As an example, the semiconductor unit growth from 1978-2020 is shown in Fig 2.2.

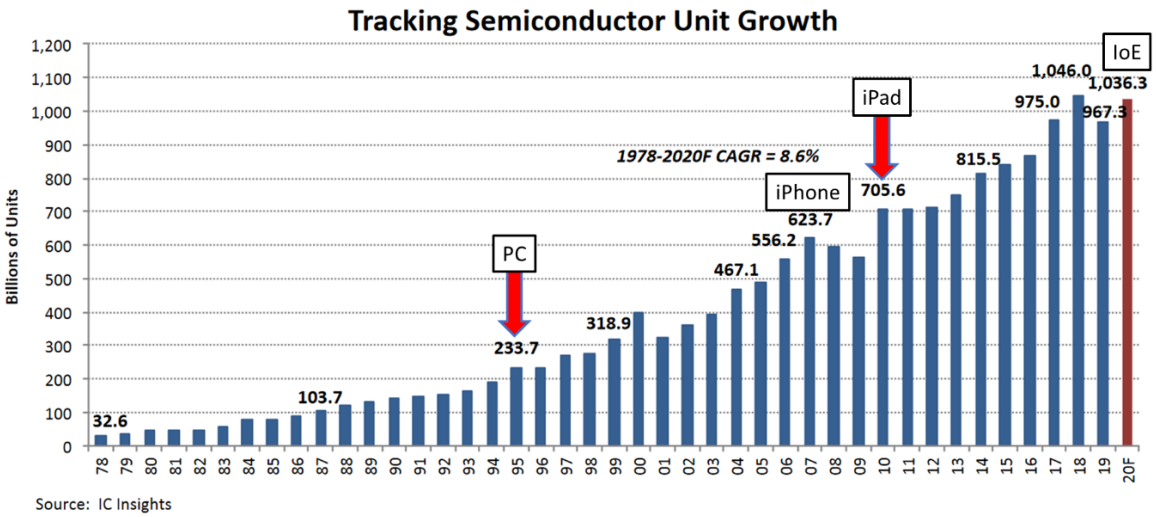

Figure 2.2. Semiconductor units shipped per year from 1978-2020[5]. The CAGR is 8.6%. (Reprinted from ref. 5 with kind permission from IC Insights.)

Accordingly, the number of devices connected to the internet of things (IoT) is expected to increase by a factor of 200 over the next several years[6]. To prepare for this, the International Technology Roadmap for Semiconductors (ITRS) designated the More than Moore (MtM) concept as one of the key focus areas for the semiconductor industry in their 2015 executive report[7]. MtM refers to the system in package (SiP) and system on chip (SoC) integration of non-digital (non-complementary metal oxide semiconductor (CMOS)) devices such as sensors, voltage regulators and energy harvesters that do not scale according to Moore's law. The unique scaling metric of SiP and SoC however, as denoted by compacting increasingly more devices into a constant substrate area, is nonetheless expected to progress at a pace according to Moore's law with a compound annual growth rate (CAGR) of 41% for the next two decades[4]. Due to this, MtM is a promising new technology domain with great potential to fulfil the performance, functionality and power density requirements of cutting-edge semiconductor devices for many years to come.

Enabling MtM requires transitioning from planar devices and planar device arrays to vertical device structures and vertically stacked device architectures. This has been defined as the 3rd age of semiconductor scaling[4]. Densely packed skyscrapers in the metropolis of today are analogue to the 3D microchip packages of the future. Like steel beams that connect successive levels, through substrate vias (TSVs) connect successive chips in a 3D package. A TSV comprises a vertical interconnect access (VIA) conductive material, such as Cu, that interconnects the top and bottom surfaces of a substrate or chip, as depicted in Fig. 2.3.

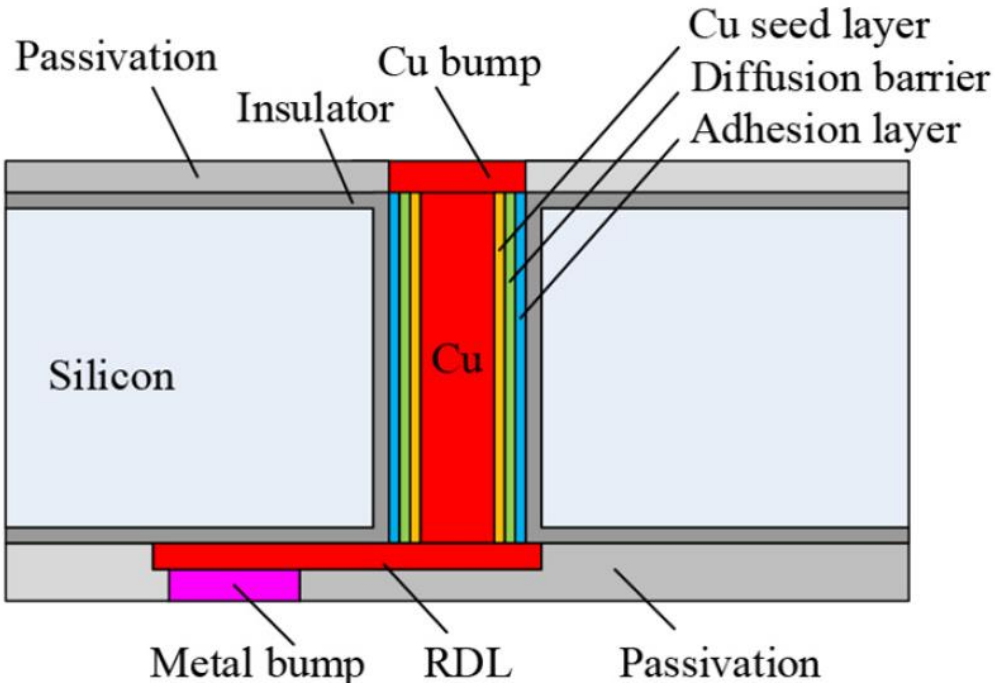

Figure 2.3. Schematic of a TSV cross-section[8]. (Reprinted from ref. 8 with kind permission from Elsevier. Copyright 2019 Elsevier B.V.)

Additionally, VIAs can also be used to create monolithic devices with stacked conductor layers (e.g., meander microinductors[9,10]) for integration with 3D packaging architectures, an x-z cross-section of which is depicted in Fig. 2.4.

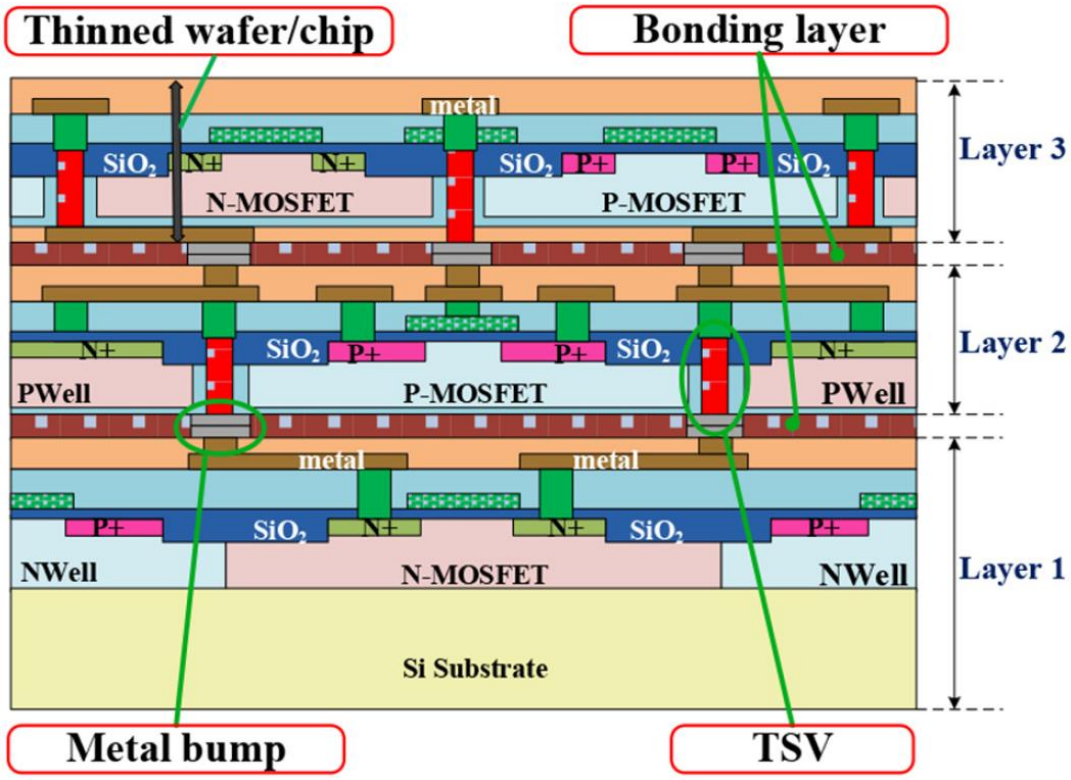

Figure 2.4. Schematic cross-section of a 3D package[8]. VIAs are colored red. (Reprinted from ref. 8 with kind permission from Elsevier. Copyright 2019 Elsevier B.V.)

By using VIAs, heterogeneous chips can be stacked like floors in a building with benefits such as: increased functionality, enhanced design versatility, high efficiency due to minimal interconnect parasitics (e.g., inductance, capacitance and resistance) and increased power density[8,11,12,13,14,15,16,17,18,19,20,21,22,23,24]. Due to this, TSVs are considered as, "the heart of 3D integration"[20]. The benefits of 3D integration are demonstrated in Fig 2.5.

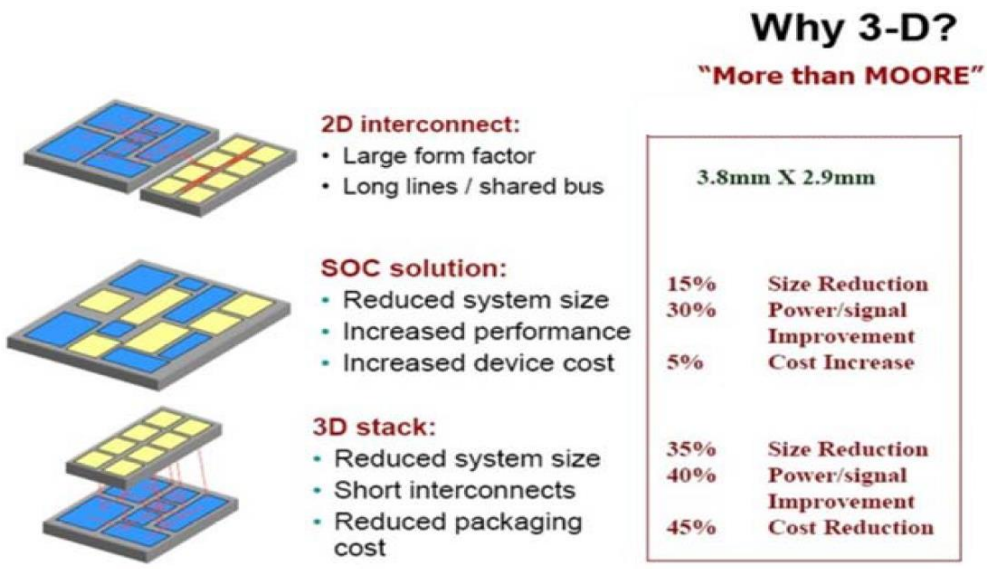

Figure 2.5. The benefits of 3D integration[7]. (Reprinted from ref. 7 with kind permission from the Semiconductor Industry Association.)

Future 3D microchip architectures offer the potential for highly integrated packages that comprise from the top-downwards multiple heterogeneous device and sensor layers, a high bandwidth memory (HBM) stack, a CMOS logic/processor layer, a voltage source and finally a heat sink, where each stacked layer uses VIAs as vertical interconnects. Regarding VIA size, a cutting-edge HBM dynamic random access memory (DRAM) die uses an array of ≈5,000 TSVs with a thickness of 50 µm and a pitch of 50 µm, which corresponds to an aspect ratio (AR) of two with an equal line to space (l/s) ratio[25]. Example VIA dimensions in the device and sensor layers for 3D integration include thickness (T, µm) = 5[26,27], 100[8,28], 200[29,30], 230[31], 300[32] and diameter (D, µm) = 15[30], 20[26,27], 50[32], 80[29], 90[31], 100[28] with ARs ranging from 0.25-13.3.

Whilst 3D microchip packaging offers significant benefits, it can be expensive and technically difficult to realize due to for example, warping during multilayer wafer bonding with heterogeneous materials, excess heat generation and a mismatch of the coefficient of thermal expansion (CTE) between packaged layers/materials that causes stress during operation[8,33,34,35]. To circumvent these difficulties, a simpler and more cost-effective advanced packaging technique has emerged that uses interposer substrates with chips bonded to the surface and VIAs embedded inside for enhanced input/output (I/O) redistribution[8,36,37]. Since this technique uses VIAs but decouples their fabrication from the sensors, devices and CMOS integrated circuits (ICs) on the interposer surface, it acts as a bridge between 2D and 3D technology and is therefore known as 2.5D packaging, as depicted in Fig. 2.6.

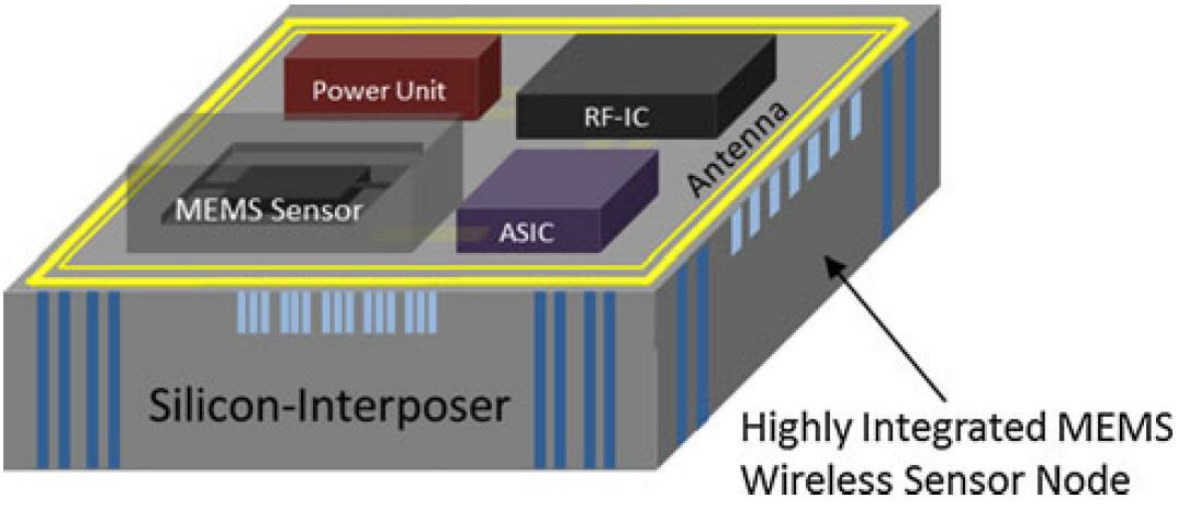

Figure 2.6. Schematic of a 2.5D package[37]. VIAs are colored blue and extend through the Si interposer. (Reprinted from ref. 37 with kind permission from Springer Nature. Copyright Springer-Verlag Berlin Heidelberg 2013.)

In addition to enabling reduced interconnect lengths and reduced form factors, 2.5D packaging has the potential to eliminate CTE mismatch induced stress between adjacent heterogeneous chips by using an interposer material with a low Young's modulus, such as an acrylic polymer, which has already been demonstrated as a stress mitigating dielectric liner in TSVs[38,39,40,41,42]. For a sense of scale, interposers are usually around 100-150 µm thick and comprise thousands of VIAs that typically range from 50-200 µm in diameter (AR=0.75-3)[8,25].

In addition to providing vertical interconnect access, multifunctional TSVs are increasingly being used in emerging devices such as 3D microinductors and enhanced microelectromechanical systems (MEMS) sensors and actuators. For example, in MEMS, it is often necessary to vacuum seal device components (e.g., the electrical wiring) from the surrounding environment to prevent detrimental chemical reactions such as corrosion and erosion from degrading device sensitivity. Wafer level vacuum packaging (WLVP) products have been commercialized that use TSVs as I/O interconnects for vacuum sealed MEMS devices, as depicted in Fig. 2.7, such as inertial sensors[43,44] and RF transceivers[45].

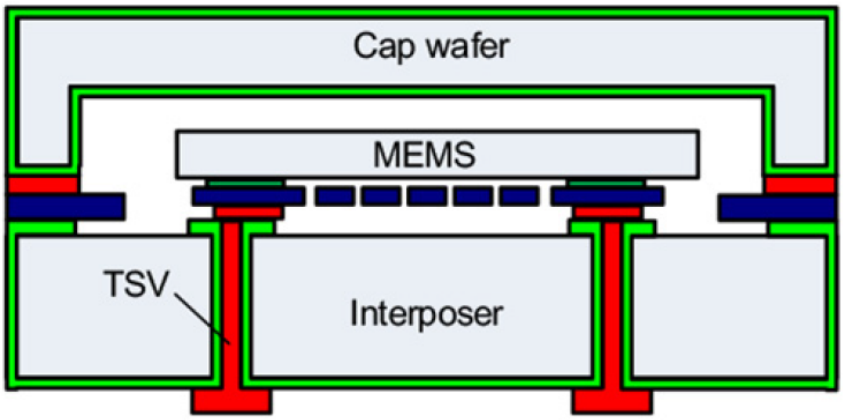

Figure 2.7. MEMS WLVP with TSVs for I/O[8]. (Reprinted from ref. 8 with kind permission from Elsevier. Copyright 2019 Elsevier B.V.)

Using VIAs in WLVP hugely reduces the packaging cost and footprint by about 5-10x when compared to traditional topologies, which has been an essential facilitator of MEMS integration into consumer electronics and mobile devices over the last decade[8]. In 3D microinductors, TSVs enable a vertically meandering current path with a high volume and small footprint while simultaneously providing structural support[46]. Furthermore, microinductor TSVs can be made hyperfunctional by using VIAs with a clad soft magnetic core that significantly boosts inductance and reduces EMI, as depicted in Fig. 2.8[46].

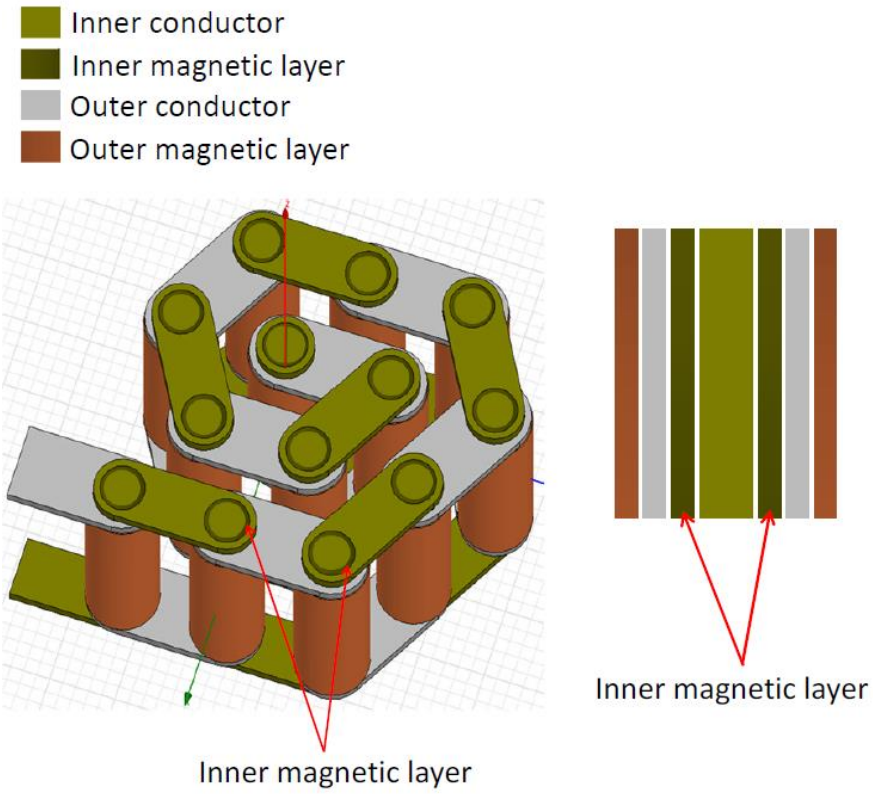

Figure 2.8. Coupled 3D microinductor with hyperfunctional VIAs coated in a laminated soft magnetic material. This schematic is from the Tyndall ADEPT group patent (PCT/EP2019/077978) entitled, "A vertical magnetic structure for integrated power conversion".

Hyperfunctional VIA microinductors directly address the main challenges of power management integrated circuits (PMICs), which are miniaturizing the micro-magnetic components, reducing electromagnetic (EM) leakage and minimizing power consumption[6]. Due to this, TSV enhanced microinductors in next-generation IVRs will be essential for autonomous MEMS and IoT devices[6]. Paving the way for this newly emerging 3D microinductor technology, Tyndall National Institute is a key facilitator of magnetic materials and microinductor research with an abundance of design/process[7,47,48,49,50,51,52,53,54,55,56,57,58,59,60,61,62,63,64,65,66,67,68,69,70,71,72,73,74,75] and review papers[76,77,78,79,80,81] available in the literature.

2.5D and 3D packaging architectures will comprise a plethora of devices, as depicted in Fig. 2.9, that convert energy from the ambient environment to usable electricity by gathering from sources such as light, heat, movement, vibration and radio frequency (RF)[6].

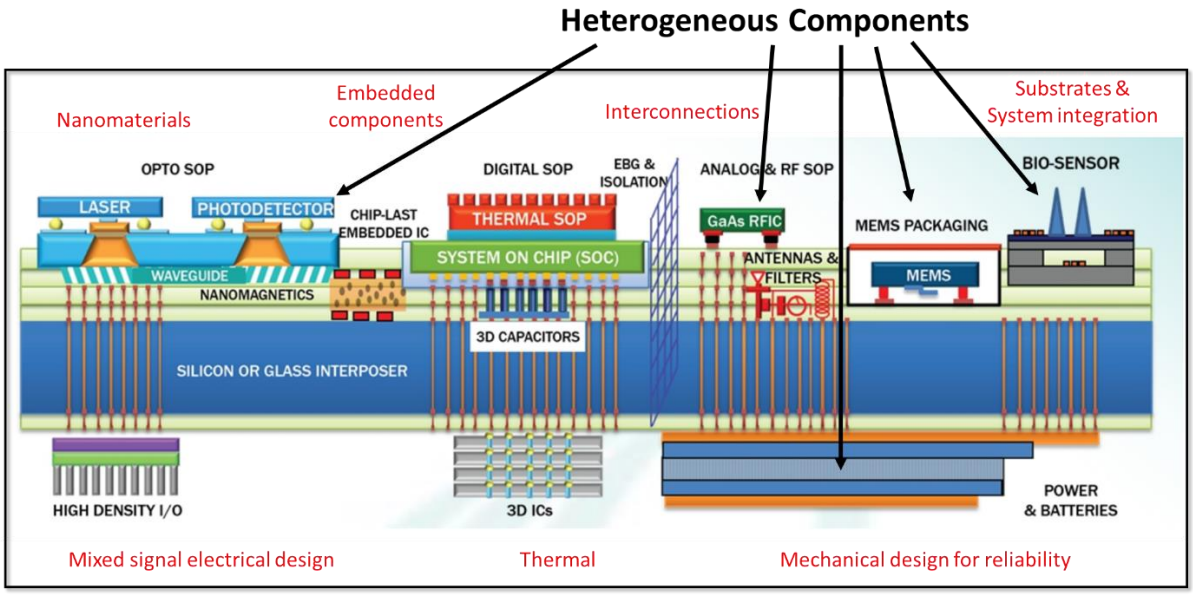

Figure 2.9. 2.5D and 3D packaging with heterogeneous component integration demonstrating high device packing density[82]. (Reprinted from ref 82 with kind permission. Courtesy: www.prc.gatech.edu).

The reduced form factor of TSV enhanced microinductors minimizes parasitics and could enable granular point-of-source (PoS) voltage regulation from each of these devices with very high efficiency (e.g., by using a boost converter), which will be essential for low power energy harvesting. By boosting the input voltage, Joule heating would be significantly reduced as power loss $(P) \propto I^2$, which is especially important for interconnects with high resistance (e.g., small cross-section) in densely packed microcircuits. Furthermore, small footprint buck converters equipped with TSV enhanced microinductors are the key to unlocking granular point-of-load (PoL) power conversion by enabling a unique voltage rail for each of the sensors and devices in a 2.5D/3D package[83]. Reported microinductor VIA dimensions include T (µm) = 100[84,85,86,87], 140[88], 187[89], 200[84], 250[90], 300[91], 350[92,93], 380[94], 500[10,95], 650[96] and 900[10] and D (µm) = 9[86], 10[87], 20[84,85,88,89], 40[88], 50[92,93,95], 60[90], 100[91], 110[96], 260[96] and 345[96], with an AR ranging from 1.88-11.1.

2.2. VIA fabrication methods

2.2.1. Deep reactive ion etching

A common method to punch holes through a Si substrate, deep reactive ion etching (DRIE) comprises three main etching techniques including: 1) time-multiplexing[97], 2) cryogenic steady-state[98], and 3) non-cryogenic steady-state[99]. Of these techniques, the most prevalent is time-multiplexing, also known as the Bosch process[20]. This process entails alternating between a vertically directed isotropic SF_6 plasma etch and a C_4F_8 passivation layer. The overall effect is quasi anisotropic etching of a photoresist patterned Si substrate, which can be used to create high aspect ratio (HAR) TSV molds at selective wafer locations. A detailed discussion of the photoresist patterning design aspects is included in section 2.2.3. Time-multiplexing between isotropic etch and passivation steps creates elliptical scallops on the VIA sidewalls, as shown in Fig 2.10, that are proportionally sized to the etch cycle duration.

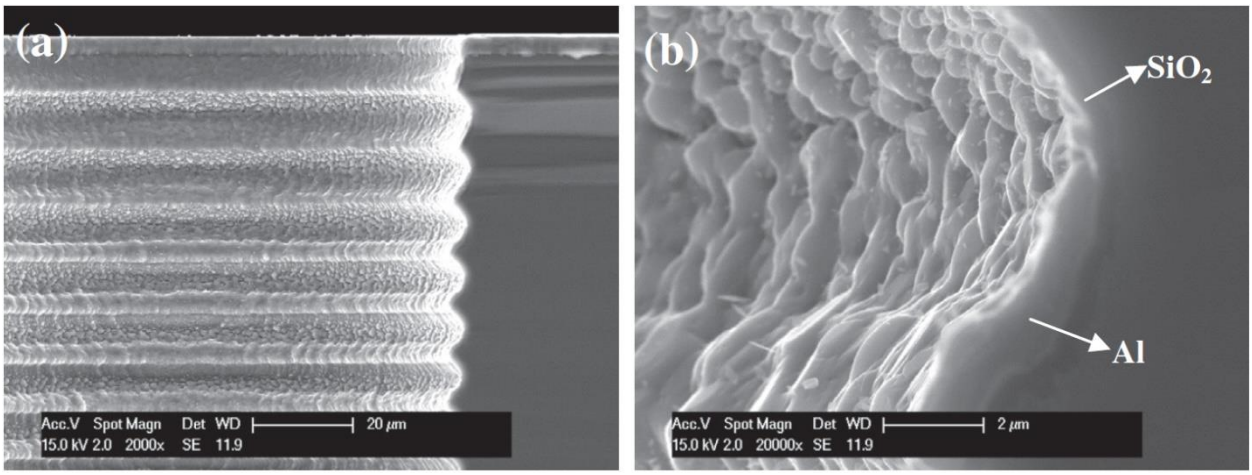

Figure 2.10. TSV scalloping as a result of a time-multiplexed etch (the Bosch process)[100]. a Top view of TSV cross-section. **b** Close up of a scallop from **a**, where the silica passivation layer was deposited by plasma enhanced chemical vapor deposition (PECVD). (**a**-**b** reprinted from ref. 100 with kind permission from Elsevier. Copyright 2015 Elsevier B.V.)

Scalloped (rough) sidewalls induce stress in adjacent materials and exacerbate EMI effects[20,100], which can lead to breakdown of the dielectric liners in TSVs, current leakage through laminated layers and interdiffusion between adjacent layers that degrades material parameters[101]. Due to this, there is a marked tradeoff between TSV etching rate and TSV sidewall roughness[102]. Cutting-edge time-multiplex etching is capable of 50 μm/min etch rates (large etch cycle duration), 5 nm scallops (small etch cycle duration), 100:1 ARs, 90º±0.2º sidewalls and a 100:1 selectivity for Si over patterned photoresist[8].

Once Si etching is complete and the TSV mold is formed, the sidewalls are coated in a dielectric that functions as an insulator between the substrate and any conductive TSV lining/filling materials (e.g., Cu)[20]. Common TSV lining insulators include Silica[103,104,105,106,107,108], silica nitride[20] and polymers[38,39,40,41,42]. Typical deposition methods include chemical vapor deposition (CVD)[104,105,106,107] and atomic layer deposition (ALD)[108,109]. Adhesion and diffusion barrier layers are then sequentially deposited that comprise Ti, Ta or composites such as TiN, TiW and TaN[20]. Following this, a Cu seed layer is finally deposited. Deposition methods include physical vapor deposition (PVD)[110], ALD[111] and CVD[112], however line of sight PVD techniques have limitations on the TSV AR for a conformal deposit.

Most TSVs use Cu as a fill material due to its low resistivity (1.68×10^{-8} Ω·m at 20 °C)[113], its low electromigration characteristic that enhances circuit reliability and its heat dissipation capabilities as a result of a large heat transfer coefficient (HTC, 17.6 ppm/ºC)[8,20]. Electroplating is most widely used to deposit the Cu fill material, however standard electroplating procedures cause current crowding at the TSV entrance which results in substantial thickness variations in the deposit along the TSV length leading to plating voids and mushrooming effects, as shown in Fig. 2.11[114,115,116].

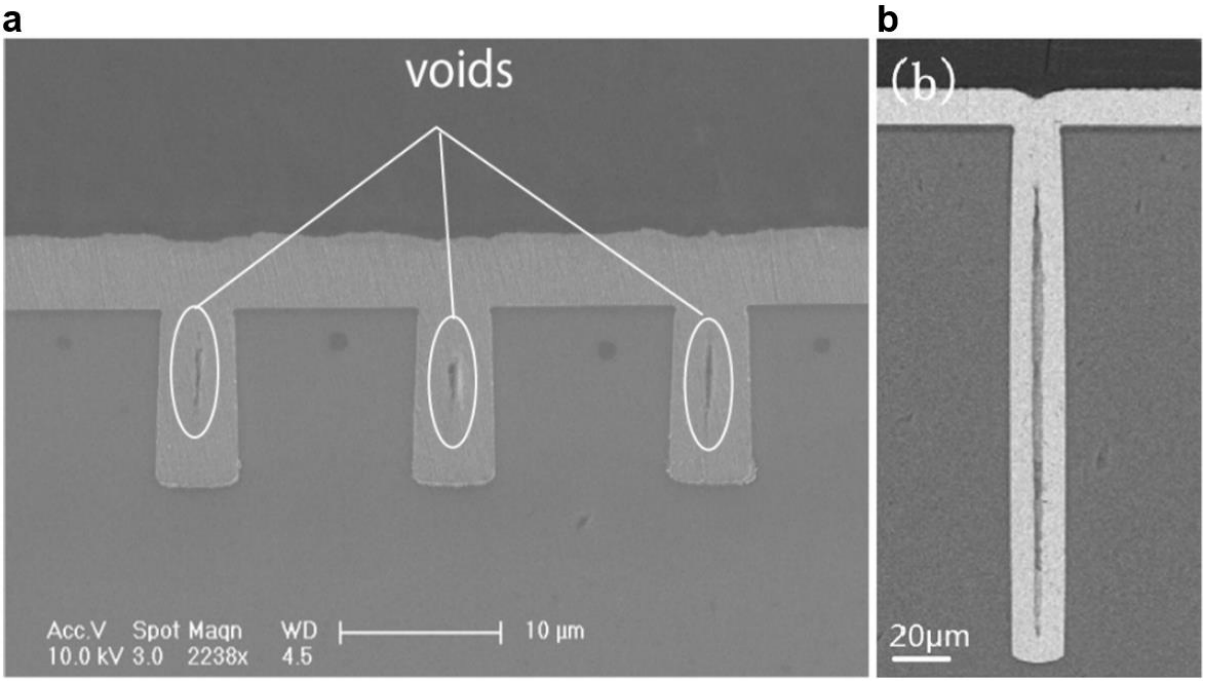

Figure 2.11. Plating voids in TSVs. a Low AR[115]. (Reprinted from ref. 115 with kind permission from IEEE. Copyright 2012 IEEE.) **b** High AR[114]. These are known as blind-TSVs, wherein the substrate has not been completely etched. (Reprinted from ref. 114 with kind permission from Elsevier. Copyright 2016 Elsevier B.V.)

As a solution to this, superconformal[117,118,119,120,121,122,123,124,125,126] and bottom-up[127,128,129,130,131,132,133,134,135] TSV electroplating techniques have emerged that can achieve TSV ARs of 20:1 with a minimum diameter of 1 µm[120]. As depicted in Fig. 2.12, superconformal electroplating exploits the diffusivity, surface adsorption properties and viscosity of chemical additives including accelerators, suppressors and levelers along with a custom current waveform to achieve a homogeneous TSV fill[136,137,138,139,140].

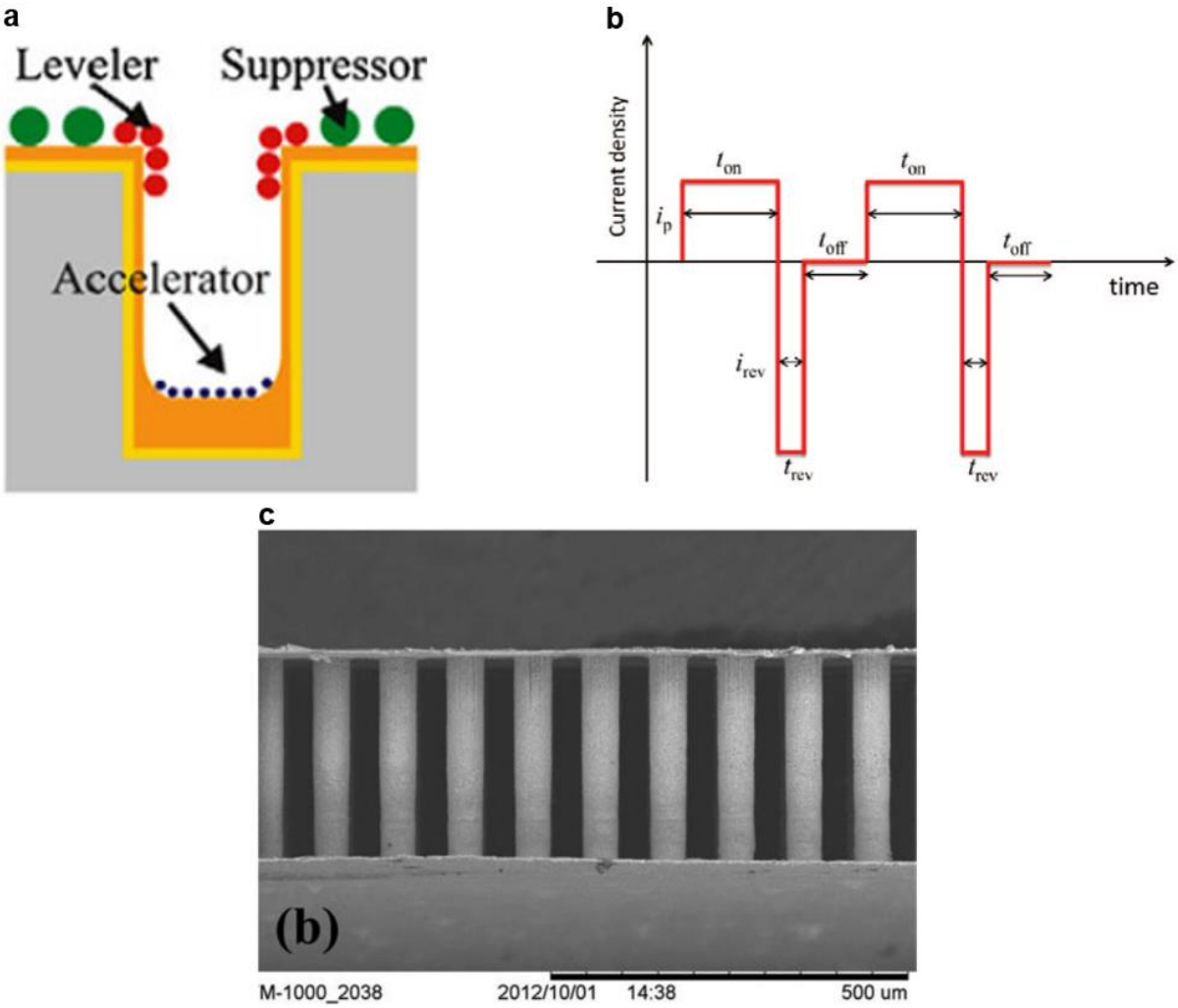

Figure 2.12. Superconformal electroplating. a Additive locations during electroplating[20]. (Reprinted from ref. 20 under the Creative Commons Attribution 4.0 International License.) **b** PPR waveform[141]. **c** Void-free TSVs filled with the waveform in **b**. (**b**-**c** Reprinted from ref. 141 with kind permission from IOP Publishing, Ltd. Copyright 13 The Electrochemical Society; permission conveyed through Copyright Clearance Center, Inc.)

Accelerators are small molecules that have a high diffusion coefficient, which increases their flux through the TSV mold cross-section. Examples are 3-mercapto-1-propanesulfonic acid (MPS) and bis-(3-sulfopropyl) disulfide (SPS)[142]. Conversely, suppressors are relatively larger and have a low diffusion coefficient, whereby they are adsorbed at the TSV entrance. Examples are polypropylene glycol (PPG) and polyethylene glycol (PEG)[143,144]. Finally, levelers with high viscosities adsorb on the deposit surface and reduce the localized accelerator concentration to normalize the plating rate[145,146]. Examples include 1,2,3-Benzotriazole (BTA) and Janus Green B (JGB)[147]. The custom waveform is periodic pulse reverse (PPR), wherein for example, a reducing electrode potential precedes an oxidizing electrode potential, which is then followed by a period of zero overpotential[141,148,149,150]. PPR is needed because even with the complex additive chemistry of superconformal electroplating, Cu nonetheless electroplates faster at the TSV entrance during the reduction pulse. The oxidation pulse compensates for this, as it etches away Cu at the TSV entrance at an increased rate when compared to the TSV center. The zero overpotential pause between pulse cycles enables electroactive Cu^{2+} ions to move along a concentration gradient inside the TSV, which refreshes the electroplating

solution. The net result is a balanced Cu deposition rate along the TSV length, where the integral of the pulse train is positive.

In bottom-up electroplating, as depicted in Fig. 2.13, a Si substrate with TSVs is typically bonded to a Cu-seeded carrier wafer[20]. The bonding adhesive is then selectively etched away, which exposes the electroactive Cu at the bottom of the TSVs for plating[127,128,129,130,131,132,133].

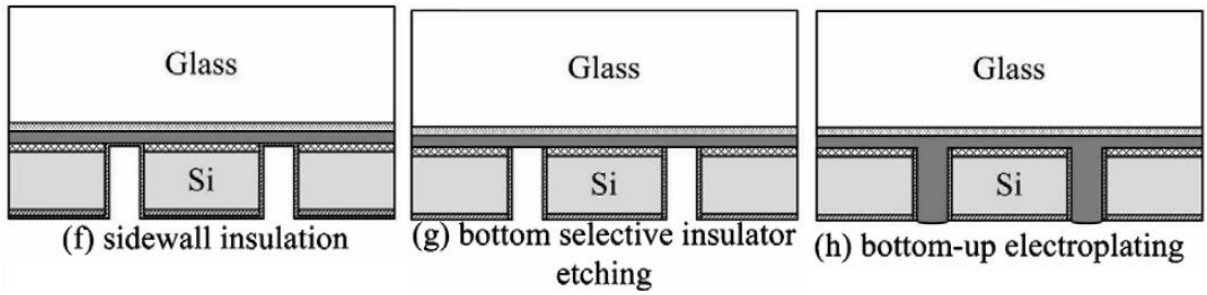

Figure 2.13. Bottom-up electroplating. The glass carrier wafer has a temporary bonding adhesive and a Cu seed layer on the back side[129]. (Reprinted from ref. 129 with kind permission from Elsevier. Copyright 2008 Elsevier B.V.)

A high etchant selectivity for the bonding adhesive is essential, as the barrier layer on the TSV sidewalls must remain intact. Methods to prevent electroplating on the VIA sidewalls include using: 1) a high resistance (e.g., small thickness) metal composite[130], 2) an additional thin film dielectric (e.g., SiN)[131], and 3) a substrate that does not require a barrier layer such as glass[132]. Once electroplating is complete, the carrier wafer is removed by either heating or backside ultraviolet (UV) exposure[151]. This technique can be advantageous over superconformal electroplating, as complex additive chemistry is not required and plating voids pose much less of a challenge[152,153]. ARs of 10:1 have been reported using this method[131,132]. Reported TSV metrics include T (μm) = 20-150 and D (μm) = 2-50 with a corresponding AR ranging from 1-15[154].

2.2.2. Laser ablation

An alternative VIA formation method is laser ablation, whereby a focused laser is directed at a substrate, which etches by either burning or subliming into a gas which further ionizes into a plasma. Nanosecond lasers burn the substrate, whereas femtosecond lasers form a plasma since the typical order of magnitude for phonon-to-electron conversion is on the picosecond scale[8]. Femtosecond laser etching is significantly slower than nanosecond laser etching, which is due to the hugely reduced pulse duration. As a benefit however, VIA sidewall roughness is minimized. Laser ablation is compatible with a variety of substrates including polymers, Si and glass[155,156,157,158,159]. This is a mask-less technique, which potentially reduces processing costs and can increase overall throughput when compared to DRIE, however as they are sequentially etched, the number of VIAs per wafer must be relatively low (e.g., <1000)[160]. Laser ablation also requires a high initial capital investment (e.g., 1.25x more than DRIE and 4x more than UV photolithography)[161]. Furthermore, VIA middle (after transistor fabrication) and VIA last (after interconnect fabrication) options may not be possible with nanosecond laser ablation due to the high temperature which could impact device reliability[20]. As laser ablated TSVs are similar to DRIE TSVs, the process of VIA lining and filling proceeds as previously described. Example TSV metrics include a 10 μm minimum diameter with an AR of 20:1[156], an 88°

sidewall[8] and a 13s/TSV etch rate with hole dimensions 200x300x100 µm (WxLxH) with a 10-picosecond pulse at 20 kHz in fused silica[160]. An example laser ablation setup and a laser-drilled VIA are shown in Fig. 2.14.

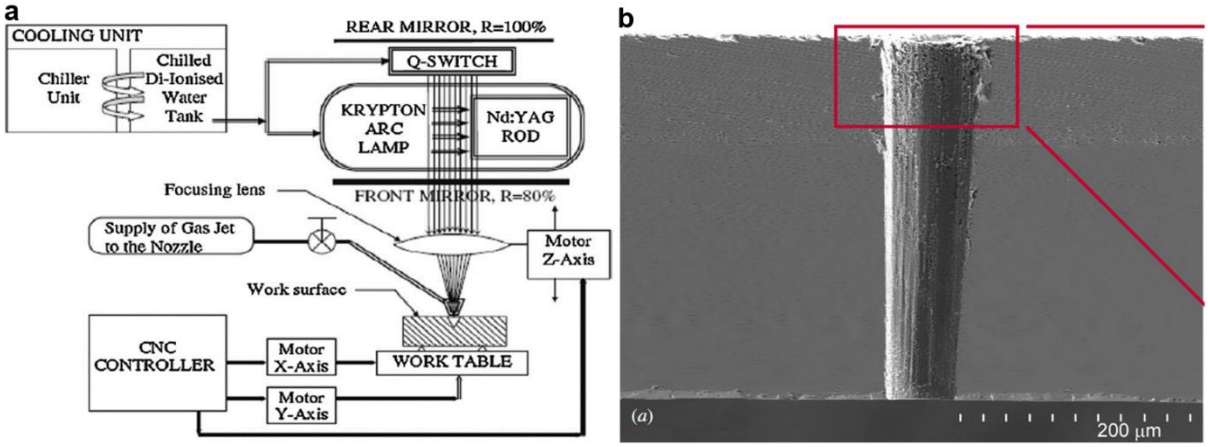

Figure 2.14. Laser ablation. a Example schematic of laser ablation[162]. (Reprinted from ref. 162 with kind permission from Elsevier. Copyright 2005 Elsevier Ltd.) **b** SEM micrograph of a laser-drilled TSV with a 40 ns pulse at 100 kHz[157]. (Reprinted from ref. 157 with kind permission from IOP Publishing, Ltd. Copyright 2012 IOP Publishing, Ltd.; permission conveyed through Copyright Clearance Center, Inc.)

2.2.3. Photolithography

Lithography applications include: various devices in MEMS and nanoelectromechanical systems (NEMS)[163,164], microfluidics[165,166], biosensors[167], photonic materials such as waveguides[168], fibrillar tissue engineering[169], microneedles for transdermal drug delivery[170], flexible force sensors[171], 3D metamaterials[172], micro and nanomold masters and replicas[173] and biomimetic surfaces with lotus-like hydrophobic properties, shark skin-like turbulence reduction and gecko-like surface adhesion[174]. Some example lithography applications are demonstrated in Fig. 2.15.

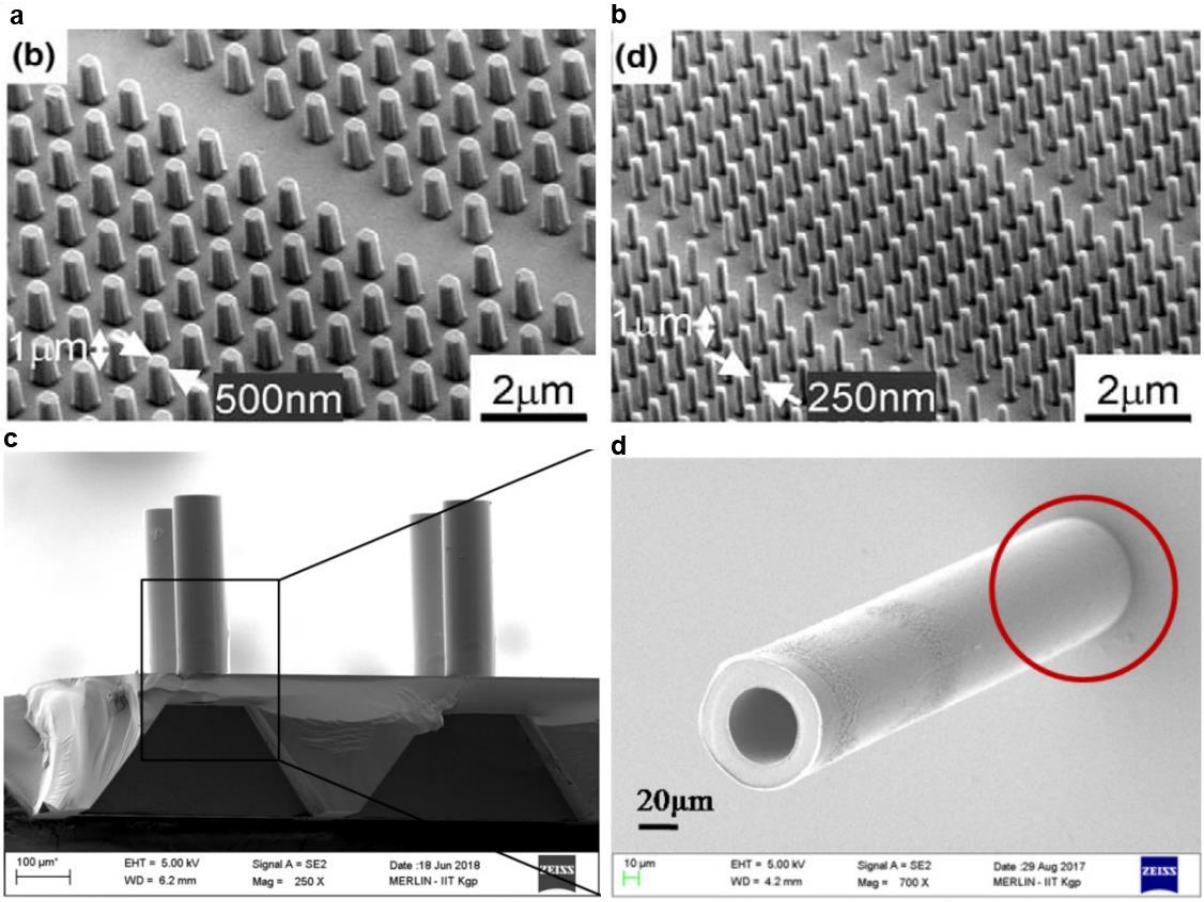

Figure 2.15. Example lithography applications. a. Nanopillar biosensor array with high surface area for enhanced antibody sensitivity[167]. **b** A more densely packed array of nanopillars with a higher surface area than **a**. (**a**-**b** reprinted from ref. 167 with kind permission from Elsevier. Copyright 2004 Elsevier B.V.) **c** Side view of a microneedle array in SU-8 photoresist[170]. **d** Top view of a single microneedle from **c**. (**c**-**d** reprinted from ref. 170 with kind permission from IOP Publishing, Ltd. Copyright 2018 IOP Publishing, Ltd.; permission conveyed through Copyright Clearance Center, Inc.)

3D lithography fabrication methods include: photolithography involving ultraviolet (UV), deep ultraviolet (DUV) and X-ray light patterned through photomasks in mask aligners and steppers involving contact, proximity, inclined[175,176], modulated[177,178] and hierarchical[174,179] photoresist exposure, laser interference lithography[180,181], laser scanning techniques such as stereolithography[182,183] and two-photon lithography[172,184], charged particles in electron beams[185,186], ion beams[187,188] and scanning probes[189], molding techniques including soft-lithography[190], nanoimprinting[165,179] and mesoporous matrix filling[168,191], multistep transfer printing[192] and self-assembly by means of external potential[193] and block copolymers[194,195]. Fig. 2.16 demonstrates some example structures fabricated with 3D lithography techniques.

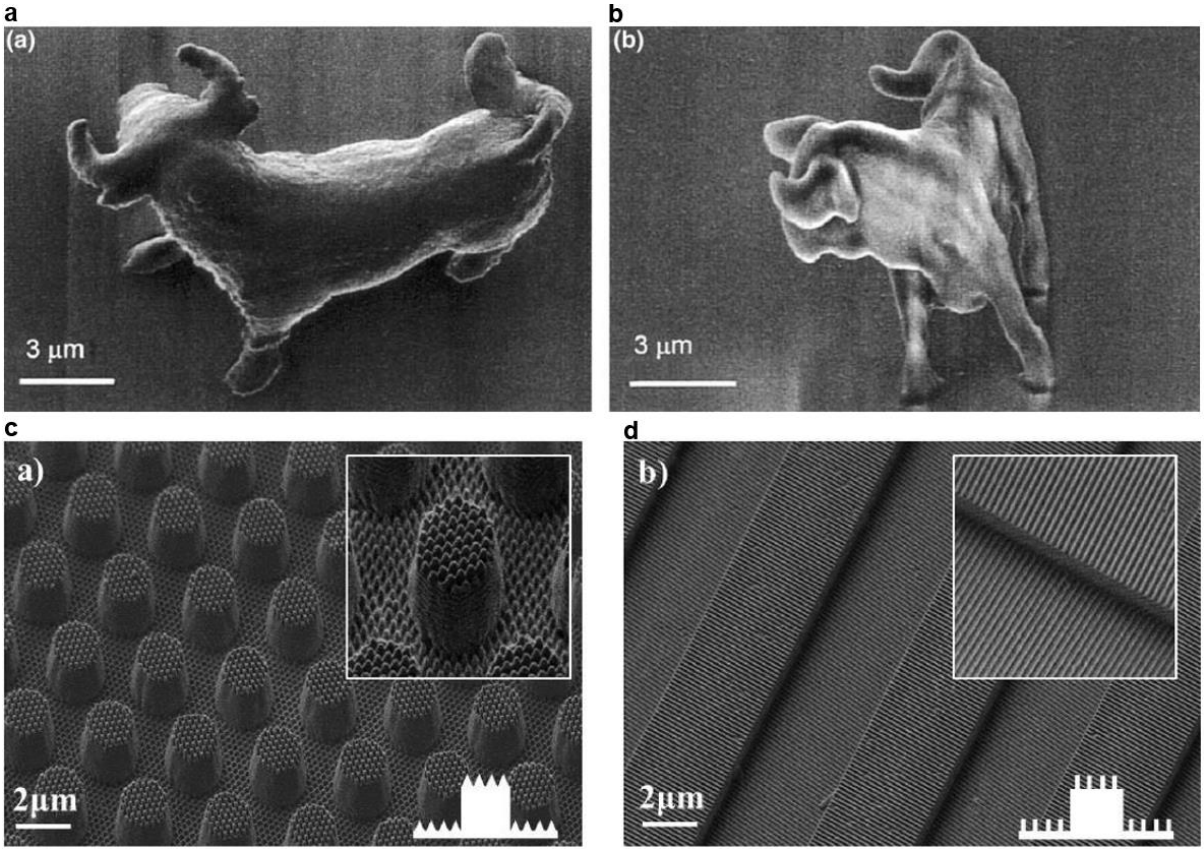

Figure 2.16. Example lithography structures. a Top view of a photoresist micro-bull created with two-photon lithography[165]. **b** Side view. (**a-b** reprinted from ref. 165 with kind permission from Elsevier. Copyright 2004 Elsevier B.V.) **c-d** Second-order hierarchical photolithography structures[179]. (Reprinted from ref. 179 with kind permission from American Chemical Society. Copyright 2019 American Chemical Society.)

Of these, photolithography is the most common method for creating micro and nanopatterned molds[196,197,198]. This is due to its low cost and high-throughput capability, which is essential for modern foundries[161,174]. Furthermore, thick photoresist (>50 µm) has key applications in MEMS and advanced packaging, wherein it can be used to pattern VIAs, as shown in Fig. 2.17[93,199].

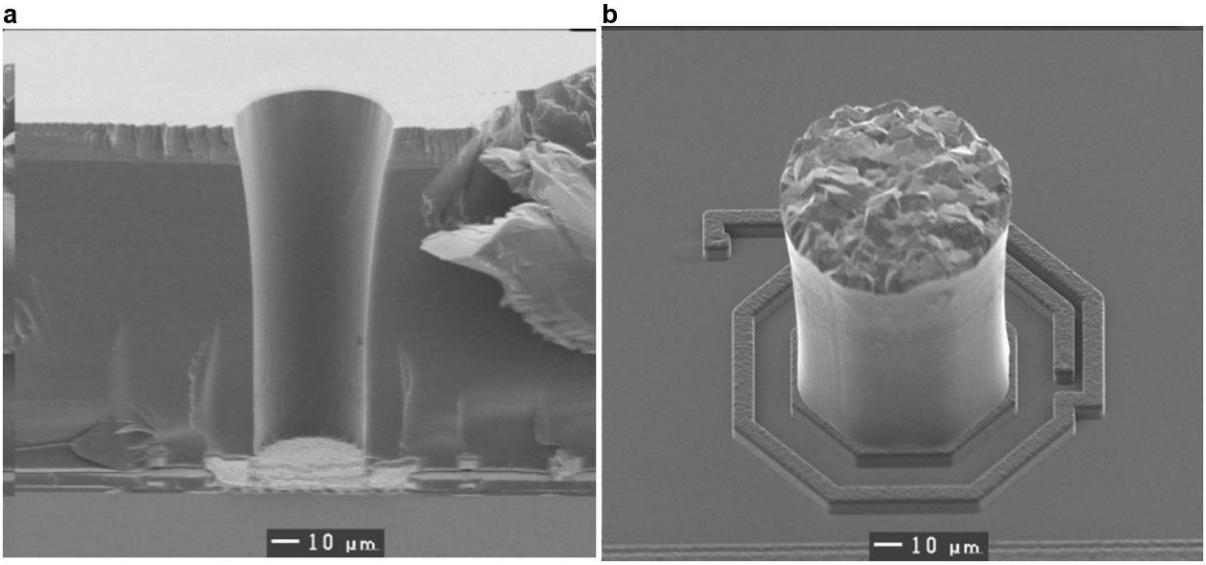

Figure 2.17. Photolithography VIA mold and electroplated micropillar[199]**. a** Cross-section of a VIA mold in 100 µm thick Shin-Etsu SIPR 7120 photoresist. **b** Angled view of an electroplated Cu VIA. (**a**-**b** reprinted from ref. 199 with kind permission from the authors and SPIE. Copyright 2004 SPIE.)

A photoresist is a viscous film comprising a solvent such as propylene glycol monomethyl ether acetate (PGMEA) and solvated molecules such as acrylate monomers and photosensitizers. Patterning a photoresist entails first designing a photomask in a suitable computer aided design (CAD) program such as KLayout[200]. Design aspects to consider are: 1) specifications for component density, device area, pitch and topology, 2) I/O pin locations for testing and operation[201], 3) flip-chip (FC) compatible topologies for chiral structures[202], 4) dicing lanes for easy die removal to enable metrology and characterization as well as package installation[203], 5) unique device identifiers for die to wafer mapping[204], 6) controlling the electroplating density across the entire wafer for plating thickness uniformity[201], 7) ensuring the line/space (l/s) ratio is feasible when accounting for the target photoresist thickness and the exposure wavelength/s with regards to light diffraction effects[205], 8) alignment markers for multiple layer stacking[206], 9) plating rings for electrical contact between the electroactive Cu seed and the wafer holder, 10) profilometer reference points for continuous metrology[207,208], and 11) miscellaneous needs such as reference points for individual layers (e.g., establishing a control sample for sputtered material properties) and using a descending component size with each stacked layer to prevent delamination due to CTE induced stress. Whilst these design aspects are mentioned in this section, many must also be considered to create patterns for DRIE.

The design pattern is then etched onto an optically transparent glass substrate, typically by an electron beam or laser ablation to form a photomask[209]. Photomasks are categorized by either dark or bright field, as typically corresponds to either positive or negative photoresist. An example bright field photomask, which I designed for the ADEPT project, is depicted in Fig. 2.18.

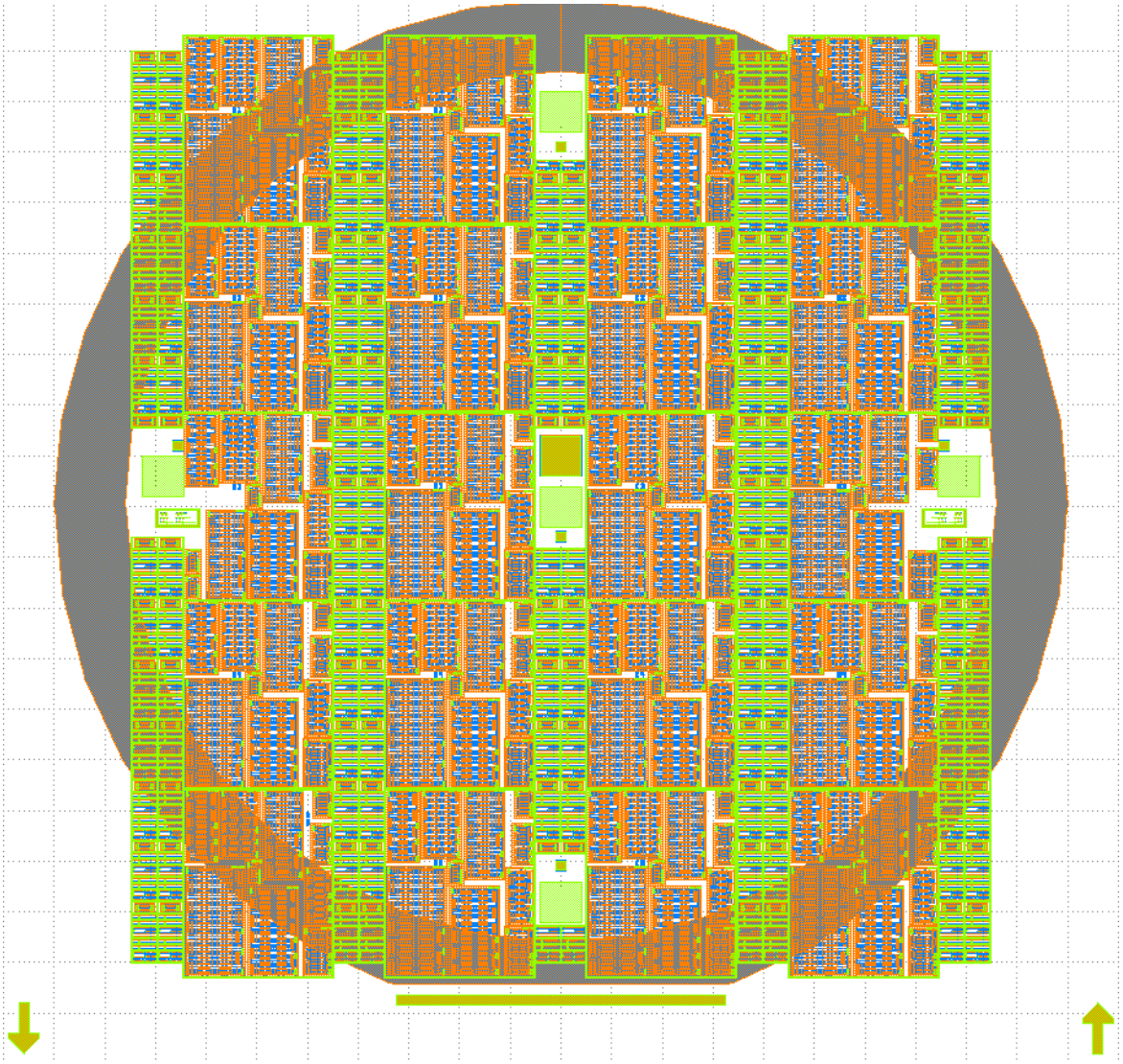

Figure 2.18. Five-tier bright field photomask created in KLayout for making TSV microinductors. The thick circle is a plating ring, which is 7 mm wide and has an outer diameter of 100 mm. The devices have I/O pins for testing and operation and comprise dummy plating areas to normalize the plating density across the wafer. The dies are placed into rows and columns for easy dicing, wherein each comprises a unique identifier. Alignment markers are at the West and East locations. Profilometer and control sample metrology and characterization points are at the North, West, South, East and central locations. The pattern superimposed on and beyond the plating ring does not get transferred to the photomask.

In positive photoresist, light exposure renders the film soluble, whereas in negative photoresist, light exposure cross-links solvated monomers to create an insoluble polymer matrix, as shown in Fig. 2.19a[196,210]. Therefore, selective light exposure with a photomask is used to transfer the target design pattern into a photoresist film which is subsequently developed into a relief mold by wet etching. Photomasks are highly sensitive to contamination by adhered particles that induce aberrations in the target pattern[211]. To mitigate this, foundries use rigorous clean room protocols (e.g., Class 10,000 (ISO 7) in the MEMS fab at Tyndall) to minimize ambient particles, pellicles that reduce particle adherence effects[211] and proximity exposure with a high numerical aperture (NA) to eliminate direct contact between the photomask and the photoresist, which is common in industry (e.g., with a stepper). A high NA system, as depicted in Fig. 2.19b, shrinks the photomask design by a factor of several times, which is essential for modern MOSFET fabrication and is especially effective when using immersion photolithography (e.g.,

193 nm λ for 32 and 18 nm mold resolution)[4,212]. Low NA systems have the highest throughput, however the photomask to photoresist pattern resolution is 1:1[199,213]. The difference between dry and immersion photolithography is depicted in Figs. 2.19c-d.

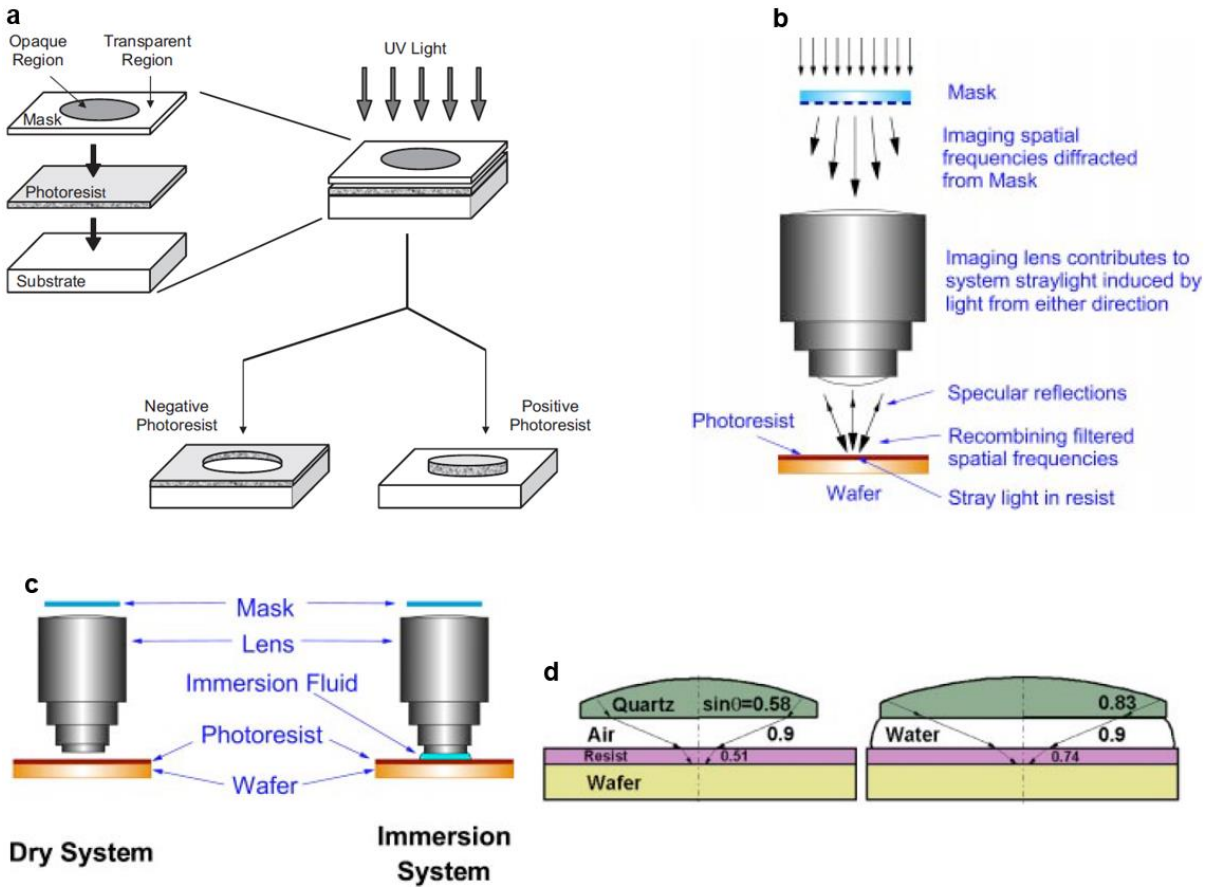

Figure 2.19. Photolithography exposure process. a The difference between positive and negative photoresist[196]. (Reprinted from ref. 196 with kind permission from Dove Medical Press. Copyright 2006 Dove Medical Press.) **b** A plano-convex lens is used to shrink the photomask design in a stepper according to the equation $NA = n \cdot sin\theta$, where n is the refractive index of the lens and θ is the angle to the vertical line. A higher NA is better for dimensional shrink. A mask aligner does not have a lens between the photomask and the wafer[212]. **c** Dry vs. immersion photolithography[212]. **d** Close up of the air/water to photoresist interface in **c**. The incident angle is preserved by matching the refractive index of the lens with an intervening medium such as water, which improves pattern resolution. (**b-d** reprinted from ref. 212 with kind permission from the author and SPIE. Copyright 2004 SPIE.)

Prior to photoresist processing, a photoresist must first be acquired that is suitable to meet the design specification. Photoresist characteristics to consider are: 1) spin thickness, 2) thickness uniformity to ensure a constant air gap or to enable contact exposure[214], 3) substrate adhesion (e.g., SU-8 poorly adheres to Cu)[215], 4) processing times (e.g., exposure and baking duration)[216], 5) developer selectivity[217], 6) resistance to acidic electrolytes for electroplating[33], 7) wavelength sensitivity[217] and ease of removal[33,218,219,220,221]. Typical processing entails: 1) spinning a photoresist puddle at high rotations per minute (rpm) to create a film with a uniform thickness, 2) heating the film above the solvent boiling point to increase film viscosity and the photoactive molecule concentration (pre exposure bake)[222], 3) exposure with a mask aligner or stepper, wherein the photochemical reaction takes place, 4) development in a suitable solvent such as aqueous tetramethylammoniumhydroxide (TMAOH)[217,223], 5) electroplating in a suitable plating solution such as Schloetter's Bright Copper ACG 8 to form conductive features

such as VIAs, and 6) stripping the photoresist in a selective etchant such as TMAOH in an organic solvent (e.g., dimethyl sulfoxide (DMSO))[224].

The two main challenging aspects of photolithography are exposure and development. Exposure is a key resolution limiting factor due to diffraction of collimated light at opaque photomask feature boundaries, as depicted in Fig. 2.20a[225]. Light diffraction creates spherical disturbances that constructively interfere in the target dark zone causing undesired cross-linking. Due to this, custom simulation methods and equations have emerged for predictive modeling of diffraction effects[226,227,228,229,230,231,232,233,234]. Rigorous simulation software is also available[214,235,236,237,238,239], however it can be expensive and require cluster or supercomputing[240]. Development is challenging due to solution dynamics such as mass transport of developer molecules by diffusion and advection[241], developer reaction kinetics[241] and photoresist swelling, which can significantly affect the target mold pattern[242,243,244]. Photoresist swelling is the result of contaminant molecules, such as water, that diffuse through a porous polymer matrix and attach to the polymer chain by Van der Waals forces such as hydrogen bonding, as depicted in Fig. 2.20b[243,244]. This effect can be reduced by increasing the polymer cross-link density (e.g., by overexposure) or decreasing the puddle time.

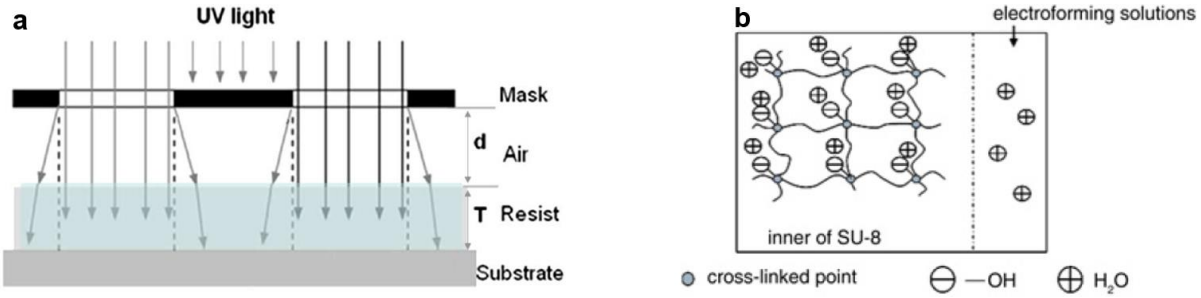

Figure 2.20. Two key challenges in photolithography. a Diffraction at photomask occulter boundaries disrupts the target photoresist pattern[225]. (Reprinted from ref. 225 with kind permission from IEEE. Copyright 2010 IEEE.) **b** Swelling mechanism in SU-8[244]. (Reprinted from ref. 244 with kind permission from IET 2021.)

Temperature directly affects the development rate by influencing diffusion coefficients, rate constants and enhancing convection[241]. Mechanical stirring is used to introduce advection mass transport into the developer bath. A more advanced stirring technique involves submerging ultrasonic/megasonic transducers to induce nanoscale cavitation for cleaning capillary-like structures, where parallel transducer/substrate alignment is the preferred orientation, as depicted in Fig. 2.21a[215]. Electroforming in photoresist molds is achieved by bottom-up electroplating. As compared to electroforming in DRIE, the mold sidewalls in photolithography are insulating and therefore complex additive chemistry is not required. Photolithography can be used to make two types of VIAs, solid conductor[10] and polymer core[10,96]. Most VIAs are solid, however polymer cores, as shown in Fig. 2.21b, are useful for high frequency applications, where the skin depth effect causes a hollow conductor to approximate a solid conductor[10]. This enables significantly faster electroplating times, however resistance is significantly increased in direct current (DC) applications.

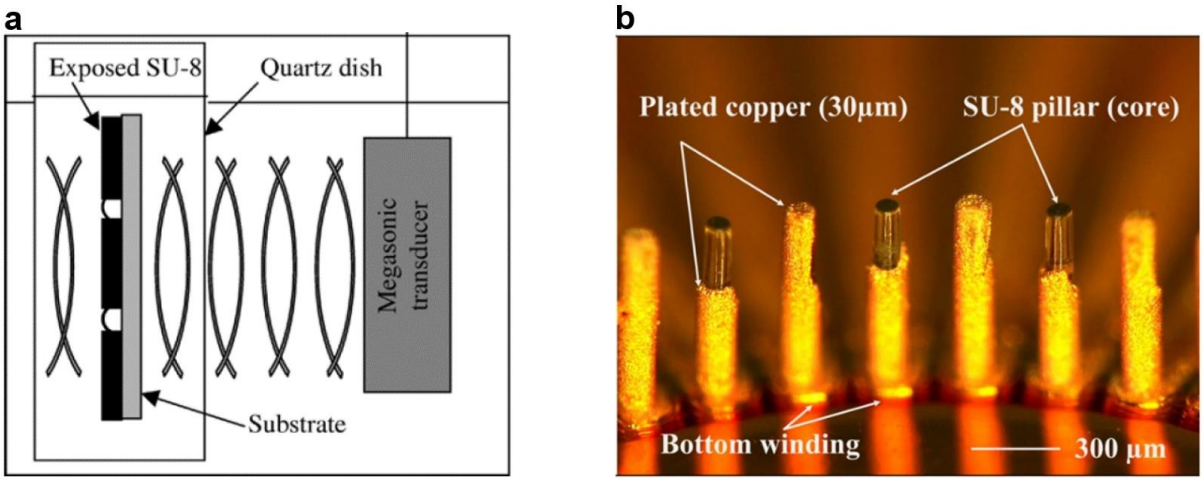

Figure 2.21. Example techniques in photolithography. a Development with a megasonic transducer[215]. Pressure waves impinge upon the patterned substrate at a rate (e.g., 1-10 MHz) that exceeds the photoresist resonant frequency. This enables development of capillary-like molds without inducing vibrations in the bulk photoresist. (Reprinted from ref. 215 with kind permission from Springer Nature. Copyright Springer-Verlag 2004.) **b** Polymer core VIAs[96]. (Reprinted from ref. 96 with kind permission from IOP Publishing, Ltd. Copyright 2013 IOP Publishing, Ltd.; permission conveyed through Copyright Clearance Center, Inc.)

2.2.4. Conclusion

The three main techniques for fabricating VIAs are DRIE, laser ablation and photolithography. DRIE and laser ablation are subtractive techniques, whereby holes are etched into a substrate to form TSVs, which are subsequently filled by super-conformal or bottom-up electroplating. Photolithography is an additive technique, whereby molds are formed on the surface of a substrate that are subsequently electroplated from the bottom-up to form VIAs. The surrounding photoresist can be left in place to function as a supporting dielectric and the underlying substrate can be removed, thereby forming TSVs.

Considerations of DRIE include: 1) high initial capital investment[161], 2) sidewall scalloping that causes stress in adjacent materials and exacerbates EMI effects[20,100], 3) intricate through hole lining processes involving many layers leading up to the seed layer[20,38,39,40,41,42,103,104,105,106,107,108,109,110,111,112], 4) complex additive chemistry that must be maintained at a specific concentration to avoid plating errors[20], and 5) custom PPR waveforms that assist in eliminating plating voids[141,148,149,150]. Considerations of laser ablation include: 1) high initial capital investment[161], and 2) nanosecond laser thermal incompatibility with VIA middle and VIA last fabrication options[20]. Considerations of photolithography include: 1) overcoming diffraction effects[225], and 2) complex standard operating procedures (SOPs) including photoresist development[241,242,243,244]. A cost analysis comparison between DRIE, laser ablation and photolithography is presented in Fig. 2.22.

Table 2 Fixed and variable costs for some microfabrication technologies

Technology	$ to process a single layer							
	Fixed costs (C_F)					Variable costs (C_V)		
	Capital ($)	Amortized (5 years; $/year)	Annual cost (4% × capital; $/year)	Annual maintenance (0.05MY; $/year)	Annual total (cost; $/year)	$/h	$/wafer	Total (inc. $2/wafer consumables; $/wafer)
X-ray LIGA PMMA (Scanner only)	1,050,000	210,000	42,000	2,800	254,800	507	242.6	244.6
X-ray LIGA SU-8 (Scanner only)	1,050,000	210,000	42,000	2,800	254,800	507	6.3	8.3
UV LIGA SU-8	218,750	43,750	8,750	2,800	55,300	7	0.68	2.68
Excimer laser	875,000	175,000	35,000	2,800	212,800	7	0.84	4.34[a]
DRIE	700,000	140,000	28,000	2,800	170,800	7	2.39	5.89[a]
Surface micromachining (lithography only)	218,750	43,750	8,750	2,800	55,300	7	0.25	2.25
Wet bulk micromachining	236,250	47,250	9,450	2,800	59,500	7	0.97	2.97
Wafer bonding	134,750	26,950	5,390	2,800	35,140	7	2	4
Resist processing (deep; thin)	210,000	42,000	8,400	14,000	64,400	7 7	0.93; 0.35	0.93[b]; 0.35[b]
Mask costs								
Optical aligner				700				
Optical stepper				1,500	Per mask	–	–	–
X-ray				3,500				

Number of machines = demand/maximum wafers/year

MY man years

[a] £3.5 additional costs for special gases

[b] 20 wafers/batch

Figure 2.22. Cost analysis of photolithography (UV LIGA), DRIE and laser ablation[161]. (Reprinted from ref. 161 with kind permission from Springer Nature. Copyright Springer-Verlag 2006.)

Whilst DRIE is the most common technique for forming TSVs, especially in foundries[245], photolithography is an attractive alternative. Reported VIA ARs by DRIE exceed the reported metrics of photolithography VIAs, however HAR VIAs are not the target for many next generation packages and devices due to characteristics including: 1) thick VIAs that reduce the overall number of stacked layers in a heterogeneous 3D package 2) power loss by Joule heating as a result of increased resistance with a reduced cross-section, which is especially problematic in energy harvesting devices with extremely low output power signals[8], 3) decreased bandwidth between stacked layers[246], and 4) excess inductance since inductance is inversely proportional to the VIA cross-section[88].

In photolithography, EMI can be minimized or eliminated by coating the VIA circumference in a soft magnetic material such as permalloy ($Ni_{45}Fe_{55}$)[247] or CoZrTaB[248], which significantly boosts VIA inductance to create hyperfunctional TSVs for integrated magnetics applications. Coating VIAs in magnetic material is also possible with DRIE or laser ablation, however magnetic laminations, which are essential to reduce eddy currents at high frequency (e.g., alternating layers of 125-250 nm thick magnetic and 20 nm thick dielectric materials), are very difficult to achieve in subtractive VIA molds. Bottom-up electroplating with insulating mold sidewalls enables use of standard bright Cu electrolyte plating baths, which is highly advantageous due to significantly reduced process complexity. Additionally, since photolithography is an additive technique, material stress due to stepwise CTE variations can be minimized or eliminated by using an elastic photoresist with a low Young's modulus as a supporting material, which is especially applicable to 2.5D interposer applications. Furthermore, photolithography is cost-effective and very high throughput, which is essential to speed track research and development (R&D). Finally, since it has a long and well-established history in the semiconductor industry, novel VIA fabrication methods using conventional photolithography processing tools can be seamlessly integrated into pre-existing foundry process flows. Therefore, this thesis leverages photolithography to explore VIA fabrication for monolithic 3D microinductor devices.

2.3. Thick photoresists

Important thick photoresist characteristics for monolithic 3D device fabrication include: 1) a clear/transparent appearance to enable mask aligner reticle alignment between successive stacked photomask layers, 2) a single spin thickness capability around 100 µm, as corresponds to the typical maximum VIA thickness[8], 3) easy stripping capability for process design versatility[218,219,220,221] and 4) fast processing options to speed-track R&D[216]. SU-8, a negative tone photoresist, is most commonly used in thick film processing[33,228], however the overall processing time can be significantly extended by a necessary post-exposure bake[214]. This is due to a two-part cross-linking mechanism, whereby a strong acid formed during light exposure subsequently initiates cross-linking upon heating[229,231,233,234,249,250,251]. Furthermore, SU-8 is an epoxy based resin, which is normally used for permanent structure applications and is very difficult to remove (e.g., by laser ablation or pyrolysis)[252]. Alternatively, negative tone acrylate based resins are a good option because they are easily stripped and do not require a post exposure bake since they fully cross-link upon exposure[253]. Positive tone photoresists are also appealing as their photochemical reaction fully proceeds during the exposure step and they are easily stripped in a solvent such as acetone[254]. In this thesis, THB-151N, a negative tone acrylate resin, is used to explore 3D device microfabrication options. THB-151N has been readily utilized in the literature for thick film VIA fabrication[218,219,220,221,253,255,256,257,258,259,260,261,262,263,264,265,266,267,268,269,270,271,272,273,274].
Additionally, it was reported that THB-151N has a significantly lower loss tangent than SU-8 in the RF domain[272], and therefore it has promising applications as a permanent dielectric/insulating supporting structure in 2.5D/3D packages. A datasheet of thick photoresists is provided in Table 2.1.

Table 2.1. Thick photoresist datasheet. a Negative tone liquid photoresists. **b** Negative tone dry films. **c** Positive tone liquid photoresists. The minimum single spin thickness requirement is 50 µm. This data was gathered from publicly available manufacturer/supplier datasheets, where a field with the "-" symbol refers to unavailable data. Technical data for the THB-151N photoresist included with kind permission from JSR Micro[275]. Technical data for the NR series photoresists included with kind permission from Futurrex[276]. Reference hyperlinks: 277, 278, 279, 280, 281, 282, 283, 284, 285, 286, 287, 288, 289, 290, 291, 292, 293, 294, 295, 296.

a

Photoresist tone	Photoresist name	Manufacturer/ Supplier	Single spin thickness (µm)	g-, h-, i-line sensitivity ($mJcm^{-2}$)	Viscosity (cP)	Appearance	Developer	Stripper	Solvent	Resin
Negative	THB-151N[275]	JSR Micro	90	1100 (80 µm on Cu)	3900	Clear yellow	TMA238WA	THB-S17	PGMEA	Acrylate
Negative	BPR-100[277]	Shipley, Rohm and Haas	140	900-1100	14000 (19 °C)	Blue	BPR developer	BPR photostripper	PGMEA	Acrylate
Negative	AZ 125nXT-10A[278]	MicroChemicals	120	1800 (60 µm)	5350	Slight amber	2.38% TMAH, 303N	AZ 400T	PGMEA	Acrylate
Negative	NR5-8000[276]	Futurrex	95	21 per µm (i-line)	-	Light yellow	Resist Developer RD6	Resist Remover RR4, acetone	Cyclohexanone	-
Negative	NR29-25000P[276]	Futurrex	110	5 per µm (on Si)	9000-10000 (cSt, 23 °C)	Light yellow	2.38% TMAH	Resist Remover RR41, acetone	γ-butyrolactone	-
Negative	NR26-25000P[276]	Futurrex	110	3.2 per µm	9000-10000 (cSt, 23 °C)	Light yellow	2.38% TMAH or RD8	Resist Remover RR41, acetone	γ-butyrolactone	-
Negative	NR26-40000P[276]	Futurrex	240	3 per µm	15000-20000 (cSt, 23 °C)	-	2.38% TMAH or RD8	-	γ-butyrolactone	-
Negative	NR77-25000P[276]	Futurrex	100	4 per µm (on Si)	10000-14000 (cSt, 23 °C)	Light yellow	2.38% TMAH or RD8	Resist Remover RR41	γ-butyrolactone	-
Negative	KMPR 1025[279]	Kayaku Microchem	67.5	1605-2930 (on Cu)	5760	Pale yellow to clear	2.38% TMAH, SU-8 developer	Remover PG	Cyclopentanone	Epoxy
Negative	KMPR 1035[279]	Kayaku Microchem	87.5	2198-2930 (80 µm on Cu)	10043	Pale yellow to clear	As above	Remover PG	Cyclopentanone	Epoxy
Negative	KMPR 1050[279]	Kayaku Microchem	115	2198-2930 (80 µm on Cu)	15860	Pale yellow to clear	As above	Remover PG	Cyclopentanone	Epoxy
Negative	SU-8 50[280]	Kayaku Microchem	100	300-500 (i-line)	14933	Pale yellow to clear	SU-8 developer, ethyl lactate, diacetone alcohol	Remover PG with Omnicoat, piranha, plasma ash, RIE, laser ablation, pyrolysis	γ- butyrolactone	Epoxy
Negative	SU-8 100[280]	Kayaku Microchem	250	400-700 (i-line)	63500	Pale yellow to clear	As above	As above	γ- butyrolactone	Epoxy
Negative	SU-8 2025[281]	Kayaku Microchem	80	450-1000 (on Cu)	5486	Pale yellow to clear	As above	As above	Cyclopentanone	Epoxy
Negative	SU-8 2035[281]	Kayaku Microchem	110	488-1100 (on Cu)	8589	Pale yellow to clear	As above	As above	Cyclopentanone	Epoxy
Negative	SU-8 2050[281]	Kayaku Microchem	165	570-1240 (on Cu)	17262	Pale yellow to clear	As above	As above	Cyclopentanone	Epoxy
Negative	SU-8 2075[281]	Kayaku Microchem	225	600-1300 (on Cu)	27192	Pale yellow to clear	As above	As above	Cyclopentanone	Epoxy
Negative	SU-8 2100[282]	Kayaku Microchem	260	600-1300 (on Cu)	55665	Pale yellow to clear	As above	As above	Cyclopentanone	Epoxy
Negative	SU-8 2150[282]	Kayaku Microchem	650	900-1200 (550 µm on Cu	99040	Pale yellow to clear	As above	As above	Cyclopentanone	Epoxy
Negative	SU-8 3025[283]	Kayaku Microchem	67.5	225-500 (on Cu)	5029	Pale yellow to clear	As above	As above	Cyclopentanone	Epoxy
Negative	SU-8 3035[283]	Kayaku Microchem	87.5	225-500 (on Cu)	8488	Pale yellow to clear	As above	As above	Cyclopentanone	Epoxy
Negative	SU-8 3050[283]	Kayaku Microchem	115	500 (100 µm on Cu)	13836	Pale yellow to clear	As above	As above	Cyclopentanone	Epoxy

b

Photoresist tone	Photoresist name	Manufacturer/ Supplier	Single spin thickness (µm)	g-, h-, i-line sensitivity ($mJcm^{-2}$)	Viscosity (cP)	Appearance	Developer	Stripper	Solvent	Resin
Negative, dry film	WBR2050, 2075, 2100, 2120[284]	DuPont	120 max	220-520	-	Light green (unexposed), dark blue (exposed)	Na_2CO_3/K_2CO_3:0.6-1.2wt%	EKC 108	-	-
Negative, dry film	AM175[285]	Ordyl, ElgaEurope	75	50-60	-	Light to dark blue	Na_2CO_3/K_2CO_3:0.6-1.2wt%	Ordyl Stripper 5600, NaOH/KOH, 1-3%	-	-
Negative, dry film	Alpha 375[286]	Ordyl, ElgaEurope	75	100-120	-	-	Na_2CO_3/K_2CO_3:0.6-1.2wt%	As above	-	-
Negative, dry film	P50100, P50125[287]	Ordyl, ElgaEurope	125 max	120-180	-	-	Na_2CO_3/K_2CO_3:0.6-1.2wt%	As above	-	-
Negative, dry film	SY 300 Series[288]	Ordyl, MicroChemicals	125 max	100-250 (55 µm on SiO_2)	-	Dark green	SY 300 Developer XFB	MEK, acetone, Developer XFB (long duration)	Ethyl acetate <1%	Acrylate
Negative, dry film	SUEX TDFS[289]	DJ Microlaminates Inc	100-1000	1150 (500 µm on Si, unfiltered i-line)	-	-	PGMEA	NMP based remover (not hard baked), CO_2 laser ablation	-	Epoxy
Negative, dry film	UD975[290]	Laminar, Eternal, Rohm and Haas	75	20-32	-	Green (unexposed), deep blue (exposed)	$K_2CO_{3(aq)}$ 0.85%, $Na_2CO_{3(aq)}$ 1%	NaOH 2-5%	-	Acrylate
Negative, dry film	E9230[291]	Laminar, Eternal, Rohm and Haas	75	78-120	-	Green (unexposed), blue (exposed)	$K_2CO_{3(aq)}$ 0.85%, $Na_2CO_{3(aq)}$ 1%	NaOH 2-5%	-	Acrylate

c

Photoresist tone	Photoresist name	Manufacturer/ Supplier	Single spin thickness (µm)	g-, h-, i-line sensitivity ($mJcm^{-2}$)	Viscosity (cP)	Appearance	Developer	Stripper	Solvent	Resin
Positive	SPR220-7.0[292]	Megaposit, Rohm and Haas	52.5	700-1300 (i-line)	-	Red Amber	MF-26A	MICROPOSIT REMOVER 1165	Ethyl lactate, anisole	Cresol novolak
Positive	SIPR-7120 Series[293]	Shin-Etsu MicroSi	100 max	-	-	Brown transparent	-	-	PGMEA, cyclopentanone	Chemically amplified, polyhydroxystyrene derivatives
Positive	AZ 50XT[294]	AZ Electronic Materials, Integrated Micro Materials	85	2400-3300 (on Cu)	-	Clear, amber-red	AZ 421K, AZ 400K	AZ 400T	PGMEA	Cresol novolak
Positive	AZ 40XT-11D[295]	MicroChemicals	65	400 (i-line, 40 µm on Si)	-	Clear light yellow	2.38% TMAH, AZ 300MIF	AZ 400T	PGMEA	Chemically amplified
Positive	AZ IPS 6050[296]	MicroChemicals	66	1200-1400 (80 µm on Cu)	4300 (cSt)	Light yellow	2.38% TMAH, AZ 726 MIF	Acetone, AZ R100 Remover, PGMEA, TechniStrip P1331	PGMEA	Chemically amplified
Positive	AZ IPS 6090[296]	MicroChemicals	82	1200-1400 (80 µm on Cu, i-line)	4900 (cSt)	Light yellow	As above	As above	PGMEA	Chemically amplified

2.4. 3D microinductors with VIAs

A primary limiting factor inhibiting granular power conversion for 2.5D and 3D packaging applications is the large form factor of microinductors[88]. In addition to increasing the converter switching frequency[297], the microinductor footprint can be significantly reduced by using VIAs to enable a vertically meandering current path, thereby forming a 3D microinductor. A key design factor of 3D microinductors is that they are often embedded in a lossy substrate (e.g., Si), which is especially problematic at high frequency[298]. This is due to the phenomenon described by Lenz's law, whereby the magnetic field of the inductor induces eddy currents in the adjacent material that cause significant resistive losses. To circumvent this, many reported 3D inductors use a toroidal design to confine the magnetic flux in a closed path, which reduces eddy currents and hinders EMI[43,85,92,93,94,96,298,299]. In toroidal microinductor topologies however, the epicenter of the device is not utilized, which comprises as much as 12.5 mm^2 in reported devices[94]. For example, this unutilized area could otherwise fit more than 1800 cutting-edge 3D microinductors[85], which makes this a significant drawback. Furthermore, the winding footprint area of toroidal designs is very large due to packing limitations of concentric VIAs (e.g., 37.7 mm^2)[94,96]. Alternatively, a shielding technique was reported for a solenoid microinductor that minimizes eddy currents in the adjacent substrate, however this technique increased the microinductor volume by a factor of 9[299]. Notably, a magnetic core is known to constrain a magnetic field[87,300]. Therefore, an elegant solution is to wrap the 3D microinductor VIAs in a laminated clad soft magnetic core, thus significantly boosting inductance while eliminating EMI from the VIAs and preventing substrate eddy current losses. This would unlock the full domain of 3D microinductor topologies, which could reduce the device footprint to a minimum and enable meeting the design specifications of next-generation IVRs. Since a device using this technique has not yet been demonstrated in the literature, this thesis investigates the design and fabrication of this novel 3D microinductor device. Example 3D microinductors are shown in Fig. 2.23. A review of reported 3D microinductors is included in Table 2.2 and relevant patents are included in Table 2.3.

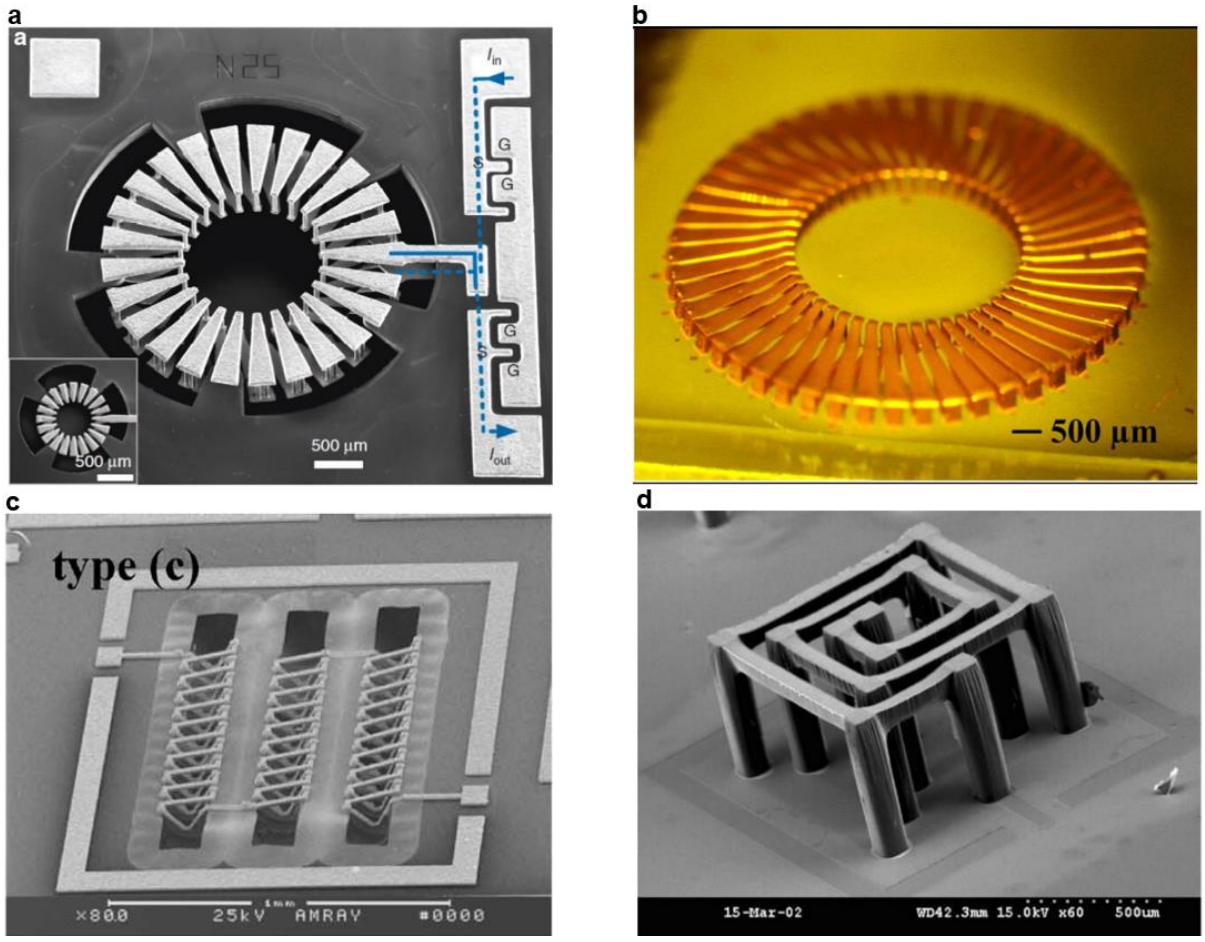

Figure 2.23. 3D microinductors using VIAs. a Toroidal topology 3D microinductor with current path shown in blue[93]. The area is 16 mm^2 with 25 turns. The substrate was removed to reduce eddy current losses. The outer ring comprises two VIAs per turn due to limitations on the packing factor in toroidal designs. (Reprinted from ref. 93 under the Creative Commons Attribution 4.0 International License.) **b** An example of another 3D toroidal microinductor[96]. (Reprinted from ref. 96 with kind permission from IOP Publishing, Ltd. Copyright 2013 IOP Publishing, Ltd.; permission conveyed through Copyright Clearance Center, Inc.) **c** 3D solenoid microinductor with 31 turns[301]. This design does not use VIAs, however trenches are etched in the substrate to enable embedded windings. (Reprinted from ref. 301 with kind permission from IEEE. Copyright 2007 IEEE.) **d** 3D spiral microinductor[10]. (Reprinted from ref. 10 with kind permission from IEEE. Copyright 2005 IEEE.)

Table 2.2. Reported 3D microinductors. a Air core 3D microinductors. **b** Air/magnetic or magnetic core 3D microinductors. The Q-factor equation is $Q = \omega L/R$, where ω is the switching frequency, L is the coil inductance and R is the coil equivalent series resistance[84,87]. The frequency column is a reference for the Q-factor column. Reference hyperlinks: 10, 84, 85, 86, 87, 88, 89, 90, 92, 94, 95, 96, 299, 301, 302.

a

Paper	Core type	Microinductor type	VIA fabrication technique	VIA dimensions (DxT, µm)	Footprint (mm^2)	Inductance (nH)	R_{dc} (Ω)	I_{sat}/I_{max} (mA)	Frequency (MHz)	Q-factor	L/A (nH/mm^2)	L/Rdc (nH/Ω)
Le '18[92]	Air	Toroidal	DRIE	50x350	7	44.6 (air dielectric), 43.7 (Si dielectric)	0.65 (R_{ac}, air dielectric), 1.25 (R_{ac}, Si dielectric at 33MHz)	1000	33.2 (air dielectric), 20 (Si dielectric)	13.3 (peak, air dielectric), 9 (peak, Si dielectric)	6.4 (air dielectric), 6.2 (Si dielectric)	68.6 (R_{ac}, air dielectric), 35.0 (R_{ac}, Si dielectric at 33MHz)
Kung '18[88]	Air	Solenoid	Photolithography	20-40x140	0.18 (D=40 µm)	1-4.5 at 500 MHz (1.5-7.5 turns, D=40 µm), 1.25-14.1 (1.5-14.5 turns, D=20 µm)	0.0595-0.213 (1.5-7.5 turns, D=40 µm), 0.1512-1.0353 (1.5-14.5 turns, D=20 µm)	-	2400	44.6-45.7 (D=40 µm), 34.1-37.8 (D=20 µm)	5.6-25 (D=40 µm)	16.8-21.1 (1.5-7.5 turns, D=40 µm), 8.3-12.6 (1.5-14.5 turns, D=20 µm)
Lee '17[90]	Air	Solenoid	In glass, not discussed	60x250, 8 µm thick Cu liner	5.76	3.5	-	-	1000	60	0.6	-
Tida '14[89]	Air	Toroidal, spiral	Not fabricated	20x≈187	0.0531 (spiral), 0.064999 (toroidal)	1.73 (spiral), 1.72 (toroidal)	0.232 (spiral), 0.17 (toroidal)	600+	200	6.1 (spiral), 8.5 (toroidal)	32.58 (spiral), 26.46 (toroidal)	7.46 (spiral), 10.11 (toroidal)
Kim '13[96]	Air	Toroidal	Electroplate on polymer core	110x650 (inner windings), 260-345x650 (elliptical outer windings)	28.3 (25 turn), 50.3 (50-turn)	76 (25 turn), 200 (50 turn)	1.25 (R_{ac}, 25 turn), 5.5 (R_{ac}, 50 turn)	500	100	35 (25 turn), 24 (50 turn)	2.69 (25 turn), 3.97 (50 turn)	60.8 (R_{ac}, 25 turn), 36.36 (R_{ac}, 50 turn)
Yu '12[94]	Air	Toroidal	DRIE	T=380	50.3	60	0.399	-	70	17.5		
VanAckern '11[95]	Air	Solenoid	DRIE	50x500	-	45 (20 turn)	20 (R_{ac}, 20 turn)	-	798 (1 turn), 732 (20 turn)	11.25 (peak, 1 turn), 4.25 (peak, 20 turn)	-	2.25 (Rac, 20 turn)
Orlandi '09[299]	Air	Toroidal	Not specified, used "empty vias"	-	26.5, 52, 32	143, 149, 150	0.03, 0.0127, 0.0235	-	1	16.6, 22.1, 22.8	5.4, 2.87, 4.7	4766.7, 11732.3, 6383.0
Gu '07[301]	Air	Trench solenoid	Angled rectangular, wet etch then photolithography	T=7, W=15 (7.5 turns), T=9, W=25 (9.5 turns)	0.12 (8.5 turns), 0.24 (9.5 turns)	2.78 (8.5 turns), 2.6 (9.5 turns)	-	-	4500 (8.5 turns), 6000 (9.5 turns)	30 (peak, 8.5 turns), 51 (peak, 9.5 turns)	23.17 (8.5 turns), 10.83 (9.5 turns)	-
Lu '07[84]	Air	Solenoid	Photolithography	20x100, 20x200	0.03 (3 turns), 0.75 (20 turns)	2.15 (3 turns), 28 (20 turns)	-	-	9700 (3 turns), 2000 (20 turns)	72.8 (3 turns), 43 (20 turns)	71.67 (3 turns), 37.33 (20 turns)	-
Yoon '05[10]	Air	Solenoid	Electroplate on polymer core	T=500, 900, 14 µm thick Cu lining	0.06	1.17 (T=900), 0.77 (T=500)	-	-	2600 (T=900), 2500 (T=500)	84 (peak, T=900), 85 (T=500)	19.5 (T=900), 12.83 (T=500)	-

b

Chen '18[85]	Air, magnetic laminate (CoZrTa)/ gapped (2µm)	Toroidal	Not fabricated	20x100	-	1.77 (air), 13.61 (magnetic), 10.56 (gapped)	0.29 (air), 1.78 (magnetic), 1.06 (gapped)	500	200	7.61 (air), 9.57 (magnetic), 12.49 (gapped)	-	6.10 (air), 7.65 (magnetic), 9.96 (gapped)
Krishnamurthy '18[86]	Air, magnetic	Solenoid	Not reported, solid Cu	9x75-100	0.0525	2.2 (air), 5.86 (magnetic)	2.7 (R_{ac})	50	10	-	41.9 (air), 111.62 (magnetic)	0.08-2.17 (R_{ac})
Sun '18[87]	Air, magnetic	Solenoid	Not fabricated	10x100	0.011-0.022 (air)	0.5-8.5 (air), 379 (magnetic)	-	Control by air gap	1000 (air), 200 (magnetic)	2.5-27.5 (air), 39.9 (peak, magnetic)	45.45-300 (air)	-
Selvaraj '20[302]	Magnetic	Solenoid (mostly 2D)	Photolithography	-	0.9	120	0.27	400	15	14.5 (peak)	130	444.4

Table 2.3. Relevant patents for 3D microinductors and VIAs with a clad soft magnetic core. Reference hyperlinks: 46, 303, 304, 305, 306, 307, 308, 309, 310, 311, 312, 313, 314, 315, 316, 317, 318, 319, 320, 321.

Patent ID	Name	Company/assignee
US20170169932A1[303]	Magnetic Material Coated Wire Inductor	Intel
US20140092574A1[46]	Integrated voltage regulators with magnetically enhanced inductors	Intel
US20040157370A1[304]	Inductors for integrated circuits, integrated circuit components, and integrated circuit	Intel
US20150206838A1[305]	Integrated Helical Multi-Layer Inductor Structures	International Business Machines
US20130093032A1[306]	Semiconductor trench inductors and transformers	International Business Machines
US20090126983A1[307]	Method and apparatus to reduce impedance disconuity in packages	International Business Machines
US9406740B2[308]	Silicon process compatible trench magnetic device	International Business Machines
US20170140862A1[309]	Thin film magnet inductor structure for high quality (Q)-factor radio frequency (RF)	Qualcomm
US20150200049A1[310]	Nested through glass VIA transformer	Qualcomm
US20110139497A1[311]	VIA structure integrated in electronic substrate	Qualcomm
JPWO2018043318A1[312]	Inductor parts and power supply module	Murata Manufacturing
WO2018043318A1[313]	Inductor component and power supply module	Murata Manufacturing
EP3364427A1[314]	Power Inductor	Moda-Innochips
US6531945B1[315]	Integrated circuit inductor with a magnetic core	Micron Technology
JPH0314284A[316]	Printed board with embedded noise absorber	Mitsubishi Electric
US20070257761A1[317]	Inductor and electric power supply using it	Ibiden
US20150200050A1[318]	Inductor apparatus and inductor apparatus manufacturing method	Fujitsu
US20140266543A1[319]	Inductor and method for manufacturing the same	Samsung Electro-Mechanics
CN106653318A[320]	Inductive device and interleaved parallel direct current converter	Huawei Tech
JP2002289419A[321]	Soft magnetic alloy thick film, magnetic device, and method for manufacturing them	TDK

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Chapter 3 – Photoresist VIA Relief Mold Formation

This chapter includes material adapted from: Smallwood, D. C., McCloskey, P., O'Mathuna, C., Casey, D. P., Rohan, J. F. Methods for latent image simulations in photolithography with a polychromatic light attenuation equation for fabricating VIAs in 2.5D and 3D advanced packaging architectures. *Microsystems & Nanoengineering* **7**, 39 (2021). Springer Nature.

In chapter 2, photolithography was selected as a promising option for VIA mold fabrication. This chapter investigates key challenges in the photolithography process, wherein diffraction effects can significantly degrade VIA mold resolution. A detailed literature review is presented in this chapter, wherein it is identified that a novel polychromatic light attenuation equation would be highly useful, as it would enable simulation of broad spectrum exposure (e.g., with Hg bulbs). This equation is herein derived from first principles and used to demonstrate new methods in predictive modelling of photolithographic latent images. Following this, spin development is selected as an optimized development method to form photoresist VIA relief molds.

3.1. Abstract

As demand accelerates for multifunctional devices with a small footprint and minimal power consumption, 2.5 and 3D advanced packaging architectures have emerged as an essential solution that use through substrate vias (TSVs) as vertical interconnects. Vertical stacking enables chip packages with increased functionality, enhanced design versatility, minimal power loss, reduced footprint and high bandwidth. Unlocking the potential of photolithography for vertical interconnect access (VIA) fabrication requires fast and accurate predictive modeling of diffraction effects and resist film photochemistry, which is especially challenging for broad-spectrum exposure systems that use for example, Hg bulbs with g-, h-, i-line UV radiation. In this chapter, I present new methods and equations for VIA latent image determination in photolithography that are suitable for broad-spectrum exposure and negate the need for complex and time consuming in-situ metrology. This technique is accurate, converges quickly on the average modern PC and could be readily integrated into photolithography simulation software. I derive a polychromatic light attenuation equation from the Beer-Lambert law, which can be used in a critical exposure dose model to determine the photochemical reaction state. This equation is inserted into an exact scalar diffraction formula to produce a succinct equation comprising a complete coupling between light propagation phenomena and photochemical behavior. A comparative study is then performed between 2D/3D photoresist latent image simulation geometries and directly corresponding experimental data, with highly positive correlation. It is anticipated that this technique will be a valuable asset to photolithography, micro- and nano-optical systems and advanced packaging/system integration with applications in technology domains ranging from space to automotive to the Internet of Things (IoT).

3.2. Introduction

Photolithography is a process whereby a photosensitive film, or photoresist, is exposed to light. Light propagation prediction and modeling enables ambitious photomask designs for film

patterning that drive the cutting-edge of 2.5D and 3D advanced packaging architectures with increased functionality, enhanced design versatility, reduced power consumption, small form factor and high bandwidth[1,2,3,4,5,6,7]. These qualities are essential for next generation technologies in domains such as high-end computing, mobile devices, radio frequency (RF), automotive, space, artificial intelligence (AI), biotechnology and the Internet of Things (IoT)[4,8,9,10,11].

In 2.5D architectures, an array of chips is bonded to an interposer[12]. An interposer is an insulating substrate for I/O redistribution comprising vertical interconnect access (VIA) conductive materials, such as Cu, that interconnect the top and bottom surfaces to form through substrate vias (TSVs)[13]. In 3D architectures, successive chips are bonded to one another in a vertical stack with orientations such as front-to-front, front-to-back and back-to-back, where each chip comprises VIAs that connect the top and bottom surfaces[12,14].

Fig. 3.1a shows a photoresist relief mold array for bottom-up electroplating of Cu VIAs. The corresponding electroplated Cu VIA array is shown in Fig. 3.1b. This VIA array could be used in a build-up interposer in 2.5D, wherein the interposer substrate comprises an elastic material with a low Young's modulus such as an acrylic polymer. This would reduce or eliminate material stress induced by a mismatch of the coefficient of thermal expansion (CTE) between adjacent packaged devices. Furthermore, this VIA array could be used for 3D packaging in via-middle and via-last complementary metal oxide semiconductor (CMOS) processing windows to create for example, high bandwidth memory (HBM)[1,12]. Additionally, VIAs can be monolithically integrated with sensors and devices to form internal or external device/sensor components. For example in Fig. 3.1c, an air-core microinductor device, fabricated in silicon, uses internal VIAs to enable stacked conductor layers in a monolithic format, which can be readily integrated into 2.5D and 3D architectures[15,16]. The microinductor VIAs dramatically reduce the passive device form factor to enable on-chip, granular point-of-load (PoL) power delivery, which will be an essential feature of future microprocessors, complex systems on chip (SoCs) and emerging fully autonomous MEMS devices[17,18]. Fig. 3.1d depicts a cross-section of 2.5D and 3D advanced packaging architectures to demonstrate the versatility of Cu VIA arrays.

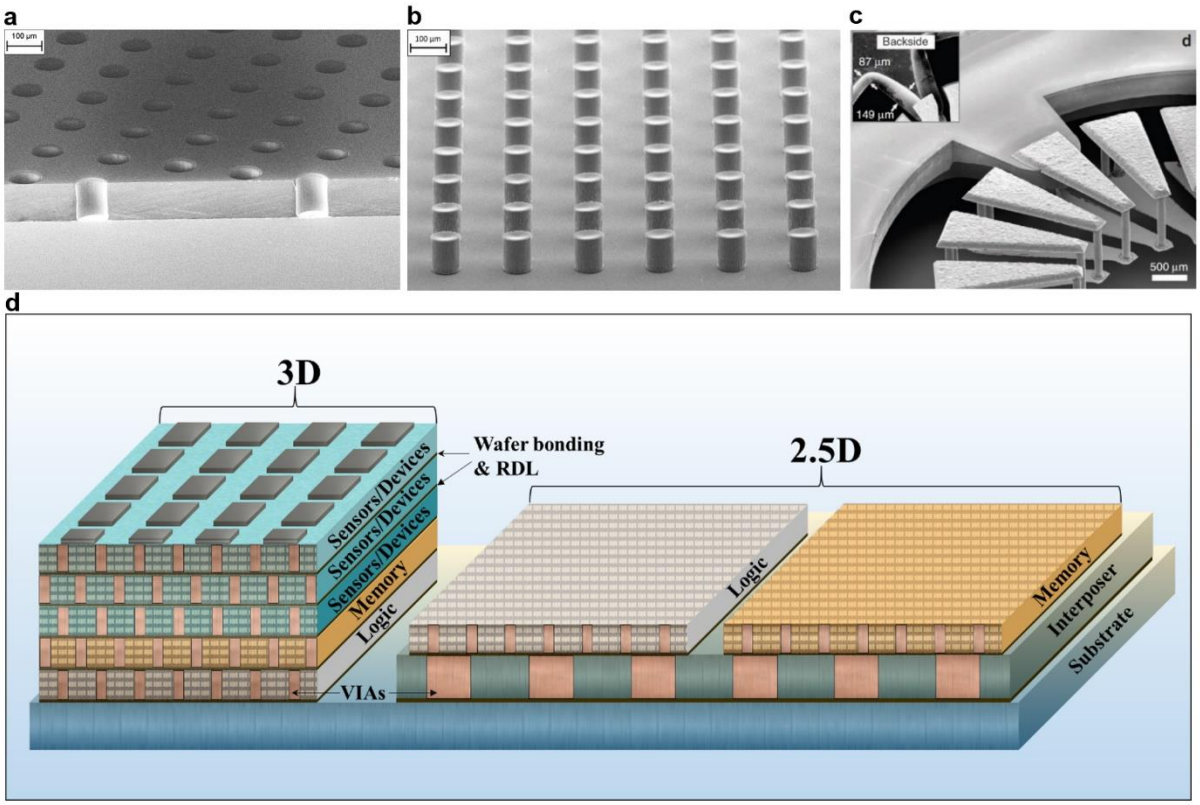

Figure 3.1. VIAs in 2.5D and 3D advanced packaging architectures. a Relief mold array in THB-151N photoresist for bottom-up electroplating of Cu VIAs. **b** Electroplated Cu VIA array from **a**. **c** Angled view of a toroidal microinductor device using VIA technology to create stacked inductor windings (Reprinted without modification from ref 16 under the Creative Commons Attribution 4.0 International License). **d** 2.5D and 3D advanced packaging architectures. An x-z cross-section reveals an array of Cu VIAs that interconnect the top and bottom surfaces of both the chips and the interposer. The chips are integrated in a single stack in 3D, whereas they are placed side by side in 2.5D. A redistribution layer (RDL) is depicted between successive stacked chips and between the chips and the substrate/interposer. The depicted VIAs are similar in size to the example Cu VIAs in **b** (the same order of magnitude)**.** The microinductor device in **c** could be implemented as a discrete layer in the 3D stack to form a power supply in package (PwrSiP), or together with the sensors to form a power supply on chip (PwrSoC)[19].

In photolithography, light exposure initiates chemical reactions at selective sites in a photoresist film, creating a latent image pattern, or an invisible array of shapes that is subsequently rendered visible by photoresist development[20]. An example exposure process for VIA mold formation is depicted in Fig. 3.2.

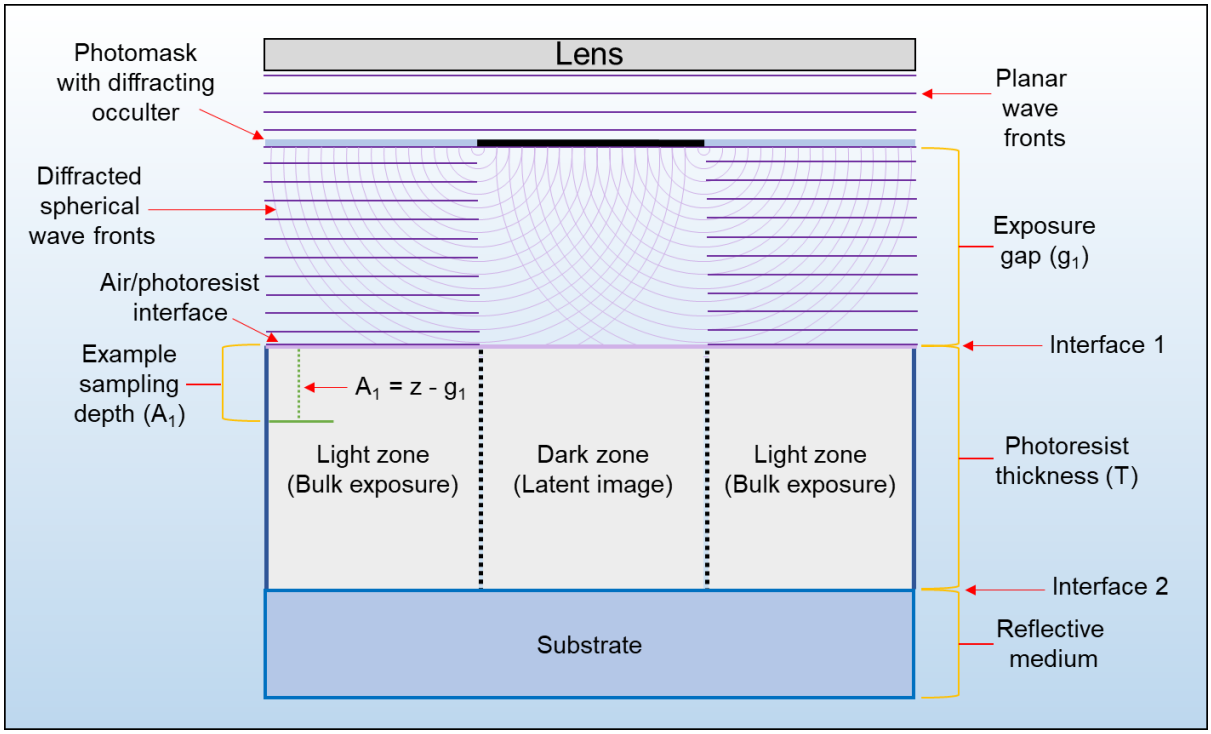

Figure 3.2. Schematic depicting Huygens-Fresnel diffraction of a planar wave front at a photomask occulter boundary. Planar waves diffract into spherical waves at the occulter boundary, where the diffracted wavefronts are superimposed in the figure as concentric rings (x-z cross sections of concentric spheres). Spherical waves initiate photochemical reactions in the dark zone, distorting the target latent image. Diffraction is a function of boundary geometry, boundary spacing and the incident wavelength to boundary size ratio. Latent image distortion is a function of diffraction, the exposure gap length, film thickness, film photosensitivity and various photoresist processing parameters including baking and etching. This schematic can also represent general optical systems comprising stacks of attenuating and non-attenuating layers. The parameters g_1, A_1, and T are referred to throughout this chapter.

The photochemical reaction initiates from the top downwards (or from the bottom upwards in backside exposure), resulting in a depth-dependent exposure dose along the thickness of the photosensitive film. For latent image formation, the exposure dose at the photoresist-substrate interface must be sufficient for the photochemical reaction to fully proceed. Ideally, the photochemical reaction only occurs in the light zone and is completely blocked in the dark zone. In practice however, the design pattern is often degraded by diffraction at aperture and occulter boundaries, causing spherical wavefronts to constructively interfere and initiate undesired photochemical reactions in the target dark zone.

Photoresist latent image simulation thus requires three main quantitative components: 1) the depth-dependent exposure dose along the thickness of the photosensitive film, 2) the critical exposure dose, which is the energy threshold past which the photochemical reaction has fully proceeded, and 3) the intensity profile underneath a photomask diffractor.

In this chapter, the focus is light propagation in photolithography for VIA mold latent image simulations. This requires parameters for diffraction, reflection, transmission and attenuation. Furthermore, accurate modeling demands a coupling between light propagation phenomena and photochemical behavior. Most reported latent image simulation methods use the paraxial approximation for diffraction equations. This introduces significant error for off-axis points in the near aperture/occulter condition, the exception being a long rectangular diffractor.

Consequently, many latent image simulation papers report formulae for aperture geometries including an infinite straight edge[21], a single long slit[22,23,24,25] and a rectangle[26,27,28,29], whilst robust simulation platforms use a range of formulae including versions of the Fresnel, Kirchoff and Rayleigh-Sommerfeld diffraction integrals[30,31,32,33,34]. Reported methods require rectangular geometries in the ultra-near aperture/occulter condition, where the Fresnel number, F, is much greater than one, as is commonly observed in photolithography. A method for a circular geometry at this distance would be highly useful for VIA mold latent image simulation, as the conventional VIA shape is circular[6,12,13].

The Dill method[35] and the enhanced Dill method[36] are frequently used to determine exposure dose information. These methods and several variants thereof are applicable to monochromatic exposure systems[24,25,26,27,28,29,37,38,39,40], whilst some other variants use a lumped analysis technique for polychromatic exposure[22,23,41] that could be suitable for example, in broad-spectrum Hg bulb exposure conditions (g-, h- and i-line). These methods enable determination of exposure dose information, but they are only suitable when a photoresist bleaches upon exposure, meaning a proportionality between resist transparency and exposure duration is required. Additionally, these methods require rigorous metrology and characterization[42], which incurs cost and takes time to perform.

A need is identified for a new method to enable VIA mold latent image simulations for both monochromatic and polychromatic exposure systems that can be performed prior to photoresist processing. This method must be fast, accurate and applicable for any photoresist. This will add great value by: 1) enabling accurate prediction of photolithographic patterning in 2D and 3D geometries for either monochromatic or polychromatic exposure conditions, 2) enabling testing of any number of photoresists before purchase and delivery, 3) avoiding unnecessary wait times for vendor supply chains, 4) eliminating unnecessary cost and time consuming lab work, 5) bypassing long machinery usage queues in busy processing facilities, and 6) enabling 24/7 remote access to safely trial unlimited experiments from any location, which is becoming an ever more important need in the modern world.

Herein, a fast and accurate method for VIA mold latent image simulations is provided that is available prior to photoresist processing, is valid for both monochromatic and polychromatic exposure systems and is applicable for any photoresist. A succinct calculation method is proposed that features a complete coupling between light propagation phenomena and photochemical behavior. This method is presented in the form of a single equation for convenience and ease of use. Additionally, a fast and exact scalar diffraction equation is used that produces accurate solutions for both on and off-axis observation points for circular aperture/occulter geometries, which is valid in the ultra-near field. Whilst the focus is on photolithography for VIA mold fabrication, the polychromatic light attenuation equation and the photoresist exposure methods are presented in a general form for broad applications in photolithography and optical systems.

Simulations and experiments are performed with THB-151N, a negative tone photoresist comprising acrylate monomers and photosensitizers dissolved in a PGMEA solvent. This i-line sensitive resist fully cross-links upon exposure, is highly viscous and well-suited for rapid thick film processing (e.g., 50+ um), as it does not require a post exposure bake and is resistant to acidic electroplating baths. An example polymerization mechanism involves free radicals

created during UV exposure reacting with dissolved acrylate monomers to form a highly crosslinked polymeric matrix[43].

3.3. Results

3.3.1. Polychromatic light attenuation with a simple new equation

A simple formula for polychromatic light attenuation is first derived. This versatile new equation is presented in a generalized form that is valid for single material layers through to stacks of attenuating and non-attenuating media. To do this, the complex refractive index for wavelength species i is first used, as given by (3.1)[44],

$$N_i = n_i + iK_i \tag{3.1}$$

where n_i is real part of the refractive index and K_i, the imaginary part, is the extinction coefficient. Cauchy's transmission equation[45] uses the photometer-measured material Cauchy coefficients, A-F in (3.2) and (3.3), to calculate wavelength-dependent values for n_i and K_i.

$$n_i = A + \frac{B}{\lambda_i^2} + \frac{C}{\lambda_i^4} \tag{3.2}$$

$$K_i = D + \frac{E}{\lambda_i^2} + \frac{F}{\lambda_i^4} \tag{3.3}$$

K_i is used to calculate the absorption coefficient, α_i, in (3.4)[35,44], which is then inserted into the Beer-Lambert law for light attenuation, as given by (3.5), where I_0 is the bulb irradiance, z is the attenuating path length and $I(z)$ is the luminous intensity[37,38,39,44].

$$\alpha_i = \frac{4\pi K_i}{\lambda_i} \tag{3.4}$$

$$I_i(z) = I_0 e^{-\alpha_i z} \tag{3.5}$$

Equation (3.5) neglects reflection and is only sufficient for systems with a single attenuating layer. An improved formulation is (3.6), which is valid for multiple layers and includes reflection. Monochromatic wavelength species λ_i is z distance from the source and the gap-modified z-factors, A_1 (3.7) and A_2 (3.8), compensate for a non-light attenuating medium somewhere along z. As shown in Fig. 3.2, A_1 is the transmitted attenuating path length and A_2 is the internally reflected attenuating path length, where T is the film thickness and g_1 is the non-attenuating path length. R_{i1} and R_{i2} (3.9) are the reflection coefficients at interfaces 1 and 2, respectively, as shown in Fig. 3.2. These are calculated with Fresnel's equations, where $R_{p_{i1,2}}$ (3.10) and $R_{s_{i1,2}}$ (3.11) are the p and s polarized contributions, n_i, the refractive index of species i in the photoresist is calculated with (3.2), δ is the incident angle and θ is the photoresist

refraction angle ($cos\delta, \theta = 1$ for vertical incidence)[25]. Reflection at the photoresist to substrate interface is calculated by using n_i , n_{i+1} , θ and φ, where φ is the substrate refraction angle as calculated from Snell's law.

$$I_i(z) = (1 - R_{i1})I_0[e^{-\alpha_i A_1} + R_{i2}e^{-\alpha_i A_2}] \tag{3.6}$$

$$A_1(z) = z - g_1 \tag{3.7}$$

$$A_2(z) = 2T - A_1 = 2T - z + g_1 \tag{3.8}$$

$$R_{i1,2} = \frac{R_{p_{i1,2}} + R_{s_{i1,2}}}{2} \tag{3.9}$$

$$R_{p_{i1,2}} = \frac{\frac{n_{i-1}}{\cos\delta} - \frac{n_i}{\cos\theta}}{\frac{n_{i-1}}{\cos\delta} + \frac{n_i}{\cos\theta}} \tag{3.10}$$

$$R_{s_{i1,2}} = \frac{n_{i-1}\cos\delta - n_i\cos\theta}{n_{i-1}\cos\delta + n_i\cos\theta} \tag{3.11}$$

To enable calculations for polychromatic light attenuation, a novel method utilizing the aerial (or the unattenuated) relative intensity spectrum of the light source is now introduced. To aid comprehension, (3.12) has been included, which calculates the attenuated light intensity fraction of monochromatic wavelength species λ_i at a distance z from a polychromatic source. Internal reflection, R_{i2}, has been omitted in this example formula for clarity, but is later included in the final formulation. The new parameter, I_{λ_i}, is the aerial relative intensity fraction of species λ_i. This is determined from the intensity spectrum of the source, as provided by the manufacturer, or as measured in-situ with a photometer.

$$I_{i_{A_1}}(z) = (1 - R_{i1})I_0 I_{\lambda_i} e^{-\alpha_i A_1} \frac{e^{-\alpha_i A_1}}{\sum_{i=1}^{n} I_{\lambda_i} e^{-\alpha_i A_1}} \tag{3.12}$$

As an example, the broad-spectrum USH-250D Super High Pressure UV type mercury lamp used in my experiments has g, h, and i-line relative intensities of 0.76, 0.49, and 1.0, respectively. Due to this, it is evident that if the unobstructed total aerial (unattenuated) broad-spectrum intensity is measured with a new bulb, that it would comprise 33.8% g-line, 21.8% h-line, and 44.4% i-line, which occurs in the attenuation factor in (3.12) at $z = g_1$ (interface 1), as required. Inside the attenuating medium, the wavelengths attenuate according to their absorption coefficients, which is accounted for by the formula.

Comprising the sum of all $I_{i_{A_1}}$, (3.13) calculates the transmitted intensity from a polychromatic source at any depth in an attenuating medium by utilizing the first gap-modified z-factor, A_1. Equation (3.14) calculates the internally reflected intensity with R_{i2} and the second gap-modified z-factor, A_2. The total polychromatic attenuated intensity is given by (3.15). This formula is applicable to polychromatic systems involving single materials through to layered stacks comprising highly variable material properties.

$$I_{A_1}(z) = I_0 \frac{\sum_{i=1}^{n} I_{\lambda_i} e^{-2\alpha_i A_1}(1 - R_{i1})}{\sum_{i=1}^{n} I_{\lambda_i} e^{-\alpha_i A_1}} \tag{3.13}$$

$$I_{A_2}(z) = I_0 \frac{\sum_{i=1}^{n} I_{\lambda_i} e^{-2\alpha_i A_2}(1 - R_{i1}) R_{i2}}{\sum_{i=1}^{n} I_{\lambda_i} e^{-\alpha_i A_2}} \tag{3.14}$$

$$I_t(z) = I_{A_1} + I_{A_2} \tag{3.15}$$

The Beer-Lambert law (3.5), has previously been used in photolithography to calculate monochromatic light attenuation using the standard formulation[46,47] and a non-standard version that accounts for a change in the photoresist absorption coefficient during exposure[38,39]. As these pre-existing formulae only account for a single wavelength, they are incompatible with polychromatic light. The equation (3.15) accounts for multiple wavelengths and is thus compatible with polychromatic exposure systems. This is made possible by including for the first time, terms comprising: 1) the relative intensity of each of the incident wavelengths in polychromatic exposure systems and 2) the corresponding absorption coefficient for each wavelength. This equation enables easy calculation and modeling of polychromatic light attenuation for micro- and nano-optical systems.

3.3.2. Advancing methods in photolithography: Depth-selective exposure dose and critical exposure dose determination

The effectiveness of the polychromatic light attenuation equation is now demonstrated with novel methods in photolithography. The standard exposure energy metric in photolithography is the aerial (unattenuated) exposure dose, typically in mJcm^{-2}, as given by (3.16), where t is the exposure time in seconds and I_0 is the bulb irradiance in mWcm^{-2}. Inserting this into (3.6) yields (3.17), which describes the attenuated exposure dose of wavelength species λ_i at a distance z from the photomask.

$$ED = tI_0 \tag{3.16}$$

$$ED_i(z) = ED(1 - R_{i1})[e^{-\alpha_i A_1} + R_{i2} e^{-\alpha_i A_2}] \tag{3.17}$$

Equation (3.17) is only applicable to monochromatic light. It very poorly accounts for broad spectrum exposure due to the exponential dependence on α_i, which can vary by one or more

orders of magnitude when moving from just g to i-line (λ = 436 nm to λ = 365 nm). To account for broad spectrum exposure, (3.16) is inserted into the new attenuation equation (3.15) to produce (3.18).

$$ED(z) = tI_t \tag{3.18}$$

This formula enables quick calculation of the exposure dose (ED) at any thickness in a photoresist film. To determine if the ED is sufficient to trigger the desired photochemical reaction, it must be compared to the critical exposure dose (CED), equation (3.19). This comparison is essential for all types of photolithography, especially for modulated exposure[30,48], as it enables determination of cross-linked sites in negative resist and soluble sites in positive resist. ED_{spec} is the specified aerial ED at a given photoresist thickness, as provided in the photoresist technical data sheet (TDS), or as determined from in-situ experiments. $I_{A_{1,b,T}}$ and $I_{A_{2,b,T}}$ are the transmitted and internally reflected (or substrate reflected) intensity contributions using b, the bulb relative intensity spectrum, as previously discussed, and T, the film thickness.

$$CED = ED_{spec}\left(\frac{I_{A_{1,b,T}} + I_{A_{2,b,T}}}{I_0}\right) \tag{3.19}$$

3.3.3. Exact, fast scalar diffraction equations for the ultra-near field

A fast and exact scalar diffraction equation, approximation-free and derived directly from the Rayleigh-Sommerfeld integral, is now introduced. Equations (3.20) and (3.21) are suitable for circular apertures and occulters, respectively, where (3.22) is the corresponding geometric parameterisation[49]. $U_{A,C}$ stands for the amplitude of the incident light, U, for an aperture, A, or occulter, C. The coefficient U_0 is the square root of the bulb aerial intensity, k is the wavenumber for the first stacked layer, x is a radial point on the observation plane, r is the radius and z is the distance from the diffractor.

$$U_A(x,y,z) = U_0\left[e^{ikz} - \frac{z}{2\pi}\int_0^{2\pi}\frac{e^{ik\sqrt{z^2+c^2(\varphi)}}}{\sqrt{z^2+c^2(\varphi)}}d\varphi\right] \tag{3.20}$$

$$U_C(x,y,z) = -\frac{U_0 z}{2\pi}\int_0^{2\pi}\frac{e^{ik\sqrt{z^2+c^2(\varphi)}}}{\sqrt{z^2+c^2(\varphi)}}d\varphi \tag{3.21}$$

$$c(\varphi) = x_i\, cos\varphi + \sqrt{r^2 - x_i^2\, sin^2\varphi}, \qquad (i = 1,2,\dots,n) \tag{3.22}$$

The radial point step size, Δx_i in (3.22), is arbitrarily specified, which sets the resolution of (3.20) and (3.21), adding great versatility to the equations. Accurate calculation results are obtained even when the step size is greater than the diffracting wavelength/s. This is due to the

integral in (3.20) and (3.21), which explores the region of interest with the infinitesimal angular increment, $d\varphi$, as corresponds to infinitesimal arc lengths (e.g., <<405 nm). Moreover, circular symmetry enables full 2D cross sections of the observation plane, which can be further stacked to create 3D volumetric maps.

Equations (3.20) and (3.21) are easily enabled for photolithography by inserting I_t from (3.15) to create (3.23).

$$I_{A,C}(x,y,z) = I_t\left|U_{A,C}\right| \tag{3.23}$$

It is noted that depending on photoresist absorption coefficients and thickness, the internally (or substrate) reflected intensity contribution, I_{A_2} from (3.15) can sometimes be neglected. This reduces the computational load of (3.23) by more than half and is highly recommended if the dosage calculation error margin is sufficiently small. For example, in CMOS photolithography, very thin films are typically used (e.g., 18 nm half-pitch in 2020)[1]. With high power top downwards exposure for high-throughput manufacturing, the incident wavelengths attenuate little along the thickness of the photoresist film such that the intensity reflected from the substrate is significant. In photolithography for VIA fabrication however, thick films are used (e.g., 50+ μm) that significantly attenuate the incident light along the photoresist thickness. Furthermore, and with an optimized exposure procedure, the ED at the photoresist/substrate interface equals the minimum CED threshold. In these conditions, the reflected intensity is minimal and has little effect on the latent image geometry. For example, the CED of THB-151N is 23.9 mJ/cm^2 when including $I_{A_{2,b,T}}$ and 23.6 mJ/cm^2 without at $T = 100$ μm, a difference of only ≈1% at substrate level, which is the point of maximum of divergence.

Several additional near field diffraction formulae have been provided in section 3.3.4. These formulae converge quickly, are applicable for various diffractor geometries, and include additional terms for refraction and angled incidence. Some useful examples of photolithography applications using these additional equations are included and their range of applicability with an analysis of the approximations made in their derivation is discussed (e.g., the paraxial approximation).

3.3.4. Introducing fast scalar diffraction equations with refraction for apertures and occulters in the near field

3.3.4.1. Square and rectangular geometries

A succinct set of fast and versatile scalar diffraction equations that include factors for refraction, reflection and angled incidence are now introduced[25,27,28,29,50]. Equation (3.24) uses the paraxial approximation to enable calculation of the unattenuated diffracted light intensity at any point (x,y,z) from a rectangular or square aperture. $C(\mu_i, \beta_i)$ and $S(\mu_i, \beta_i)$ are the Fresnel integrals (3.25) and (3.26) for μ_i and β_i. Equations (3.27), (3.28), and (3.29), (3.30) are Fresnel numbers for transmission and internal reflection, respectively, including the gap-modified z-factors, A_1 and A_2, as described in Fig. 3.2, where the refraction angle has been included ($\theta = 0$ for vertical incidence) and λ_1 is the wavelength in the first stacked layer.

To include refraction at interface 1 (see Fig. 3.2), the radiation path length was modified by the parameter, g_2 (3.31), which adjusts g_1 as the ratio of the refractive index for layer two, n_2, to the refractive index for layer one, n_1, where δ is the incident angle and θ is the photoresist refraction angle ($cos\delta, \theta = 1$ for vertical incidence). Intuitively, this equation states that due to Snell's law and when reducing the refraction angle, a longer vertical distance is required for the light to traverse the same horizontal distance as the larger incident angle.

The observation plane (the region of interest after the aperture plane) coordinates are mapped by x and y, where x_i and y_i demarcate the horizontal and vertical aperture boundaries, respectively. The $\tan\theta$ term modifies the observation plane coordinates with angled exposure, where plus and minus coefficients are used for positive and negative translations, respectively.

$$\begin{aligned} I_{re}(x,y,z) = \frac{1}{4} I_0(1-R_{i1})(\{&[C(\mu_2)-C(\mu_1)]^2 \\ &+ [S(\mu_2)-S(\mu_1)]^2\} \times \{[C(\beta_2)-C(\beta_1)]^2 + [S(\beta_2)-S(\beta_1)]^2\} \\ &+ R_{i2}\{[C(\mu_4)-C(\mu_3)]^2 \\ &+ [S(\mu_4)-S(\mu_3)]^2\} \times \{[C(\beta_4)-C(\beta_3)]^2 + [S(\beta_4)-S(\beta_3)]^2\}) \end{aligned} \tag{3.24}$$

$$C(\mu_i, \beta_i) = \int_0^{\mu_i, \beta_i} \cos\left(\frac{\pi}{2}\omega^2\right) d\omega, \qquad (i = 1,2,3,4) \tag{3.25}$$

$$S(\mu_i, \beta_i) = \int_0^{\mu_i, \beta_i} \sin\left(\frac{\pi}{2}\omega^2\right) d\omega, \qquad (i = 1,2,3,4) \tag{3.26}$$

$$\mu_i = \sqrt{\frac{2\frac{n_2}{n_1}\cos\theta}{\lambda_1(z - g_1 + g_2)}}[x_i - x \pm (z - g_1 + g_2)\tan\theta], \qquad (i = 1,2) \tag{3.27}$$

$$\beta_i = \sqrt{\frac{2\frac{n_2}{n_1}\cos\theta}{\lambda_1(z - g_1 + g_2)}}[y_i - y \pm (z - g_1 + g_2)\tan\theta], \qquad (i = 1,2) \tag{3.28}$$

$$\mu_i = \sqrt{\frac{2\frac{n_2}{n_1}\cos\theta}{\lambda_1(2T + g_1 - z + g_2)}}[x_i - x \pm (2T + g_1 - z + g_2)\tan\theta], \qquad (i = 3,4) \tag{3.29}$$

$$\beta_i = \sqrt{\frac{2\frac{n_2}{n_1}\cos\theta}{\lambda_1(2T + g_1 - z + g_2)}}[y_i - y \pm (2T + g_1 - z + g_2)\tan\theta], \qquad (i = 3,4) \tag{3.30}$$

$$g_2 = g_1 \frac{n_2}{n_1} \frac{\cos\,\theta}{\cos\delta} \tag{3.31}$$

By Babinet's principle, whereby a bright field mask is replaced with a dark field mask[49,51,52], (3.24) is easily enabled for an occulter, or an opaque diffractor. This is applied by subtracting the amplitude from one prior to squaring the Fresnel integrals in the brackets above.

3.3.4.2. Circular geometries

Equations applicable to circular diffractors are next presented. Equations (3.32) and (3.34) use the paraxial approximation to enable diffraction amplitude calculations from circular occulters and apertures, respectively[51,53]. As an example, U_{F_O} stands for the amplitude, U, of an occulter, O, in the near field, or Fresnel region, F. V_n (3.33) and W_n (3.35) are Lommel functions, U_0 is the square root of the bulb aerial intensity, $k = 2\pi/\lambda_1$ is the wavenumber, x is a radial point on the observation plane, r is the radius, and u and v (3.36) (3.37) (3.38) and (3.39) are modified Fresnel numbers that include angled incidence and refraction at the photoresist interface, as previously described.

$$U_{F_O}(x,z) = U_0 e^{ikz} e^{\frac{ik}{2z}(x^2+r^2)} [V_0(u_i,v_i) - iV_1(u_i,v_i)] \tag{3.32}$$

$$V_n(u_i,v_i) = \sum_{m=0}^{\infty} (-1)^m \left(\frac{v_i}{u_i}\right)^{n+2m} J_{n+2m}(v_i), \qquad (i = 1,2) \tag{3.33}$$

$$U_{F_A}(x,z) = -U_0 e^{ikz} e^{\frac{ik}{2z}(x^2+r^2)} [W_2(u_i,v_i) - iW_1(u_i,v_i)] \tag{3.34}$$

$$W_n(u_i,v_i) = \sum_{m=0}^{\infty} (-1)^m \left(\frac{v_i}{u_i}\right)^{-(n+2m)} J_{n+2m}(v_i), \qquad (i = 1,2) \tag{3.35}$$

$$u_1 = \left[\frac{kr^2 \frac{n_2}{n_1}\cos\theta}{(z - g_1 + g_2)}\right] \tag{3.36}$$

$$v_1 = \left[\frac{kr \frac{n_2}{n_1}\cos\theta}{(z - g_1 + g_2)}\right] [x \pm (z - g_1 + g_2)\tan\theta] \tag{3.37}$$

$$u_2 = \left[\frac{kr^2 \frac{n_2}{n_1}\cos\theta}{(2T + g_1 - z + g_2)}\right] \tag{3.38}$$

$$v_2 = \left[\frac{kr \frac{n_2}{n_1}\cos\theta}{(2T + g_1 - z + g_2)}\right][x \pm (2T + g_1 - z + g_2)\tan\theta] \tag{3.39}$$

3.3.5. Rapid and accurate latent image calculation with polychromatic exposure including diffraction, reflection, refraction and attenuation

3.3.5.1. Square and rectangular geometries

Equation (3.24) can be used to calculate the unattenuated diffraction pattern from a rectangular or square photomask aperture, inclusive of refraction, reflection and angled incidence, but not attenuation. After combining this with the polychromatic light attenuation equation, a succinct diffraction equation (3.40) is formed, which includes all of the essential latent image simulation parameters: diffraction, reflection, refraction and attenuation.

$$\begin{aligned} I_{re_t}(x,y,z) = \frac{1}{4}(I_{A_1}\{[C(\mu_2) - C(\mu_1)]^2 + [S(\mu_2) - S(\mu_1)]^2\} \times \{[C(\beta_2) - C(\beta_1)]^2 \\ + [S(\beta_2) - S(\beta_1)]^2\} + I_{A_2}\{[C(\mu_4) - C(\mu_3)]^2 \\ + [S(\mu_4) - S(\mu_3)]^2\} \times \{[C(\beta_4) - C(\beta_3)]^2 + [S(\beta_4) - S(\beta_3)]^2\}) \end{aligned} \tag{3.40}$$

3.3.5.2. Circular geometries

By including the polychromatic light attenuation equation, a succinct equation (3.41) is again formed, which includes all of the essential latent image parameters. This equation is applicable to a circular aperture or occulter.

$$I_F(x,y,z) = I_{A_1}\left|U_{F_{u_1,v_1}}\right| + I_{A_2}\left|U_{F_{u_2,v_2}}\right| \tag{3.41}$$

3.3.6. Validity of near field scalar diffraction equations

To ensure accurate simulation results using equations (3.24), (3.32), (3.34), (3.40) and (3.41), it is critical to understand the paraxial approximation validity range, wherein the aperture/occulter and the observation plane are assumed to be small and well separated. To do this, the Fresnel integral is derived from the full Rayleigh-Sommerfeld integral (approximation-free), which is given by (3.42)[54],

$$U(x,y,z) = \frac{1}{\lambda}\iint u_0(s,t)\left(\frac{1}{kl} - i\right)\frac{z}{l^2}e^{ikl}dsdt \tag{3.42}$$

where U and u_0 are the observation and aperture plane amplitudes, respectively, and l is the path length, as given by (3.43).

$$l^2 = (x-s)^2 + (y-t)^2 + z^2 \tag{3.43}$$

First is the Kirchhoff approximation, wherein the aforementioned planes are assumed to be separated by several wavelengths, thus simplifying an integrand amplitude term in (3.44).

$$\frac{1}{kl} - i = \frac{2\pi}{\lambda l} - i \to -i \tag{3.44}$$

Equation (3.45) is found after solving for l and substituting $a = x - s$ and $b = y - t$, which is of the form (3.46).

$$l = z\sqrt{1 + \frac{a^2 + b^2}{z^2}} \tag{3.45}$$

$$l = z\sqrt{1 + w} \tag{3.46}$$

To enable the paraxial approximation, (3.46) is expanded into the corresponding Taylor series, wherein the first three terms are shown in (3.47).

$$l = z\left(1 + \frac{w}{2} - \frac{w^2}{8}\right) \tag{3.47}$$

The paraxial approximation is two-part, and firstly entails the zeroth order approximation of (3.47), which yields $l = z$. This simplifies the remaining amplitude term according to (3.48).

$$\frac{z}{l^2} \to \frac{1}{z} \tag{3.48}$$

Secondly, the first order approximation yields (3.49), which transforms the integrand phase term into (3.50) and results in the Fresnel integral (3.51). It is noted that the first order approximation is taken in the phase term due to the wavenumber multiplier, k, which is typically $\gg 1$.

$$l = z\left(1 + \frac{a^2 + b^2}{2z^2}\right) \tag{3.49}$$

$$kl \to kz + \frac{k}{2z}(a^2 + b^2) \tag{3.50}$$

$$U(x,y,z) = \frac{e^{ikz}}{i\lambda z}\iint u_0(s,t)\, e^{\frac{ik}{2z}[(x-s)^2+(y-t)^2]} dsdt \tag{3.51}$$

The validity standard for (3.51) is (3.52)[44] and I am unaware of any literature that explicitly mentions a specific magnitude difference cut-off point.

$$z^3 \gg \frac{\pi}{4\lambda} max[(x-s)^2+(y-t)^2]^2 \tag{3.52}$$

To be exact, the paraxial approximation assumes (3.53), which is required to neglect the second and higher order phase terms. It is critical to verify (3.53) prior to proceeding with the near field diffraction formulas.

$$e^{-ikz\frac{w^2}{8}} \approx 1 \tag{3.53}$$

3.3.7. Equation validation: simulations and experiments

To verify equations (3.15), (3.18), (3.19) and (3.23), 2D and 3D latent image simulations are first used to make three predictions. Next, these predictions are validated by comparing latent image simulations to directly corresponding experimental data. The simulations were performed in Wolfram Mathematica[55] with (3.23) formulated for an occulter and polychromatic exposure. The THB-151N photoresist material parameters were used with attenuation factors for g-, h- and i-line, which are characteristic of Hg bulbs.

Figs. 3.3a-d show a 10 a µm diameter mold in 100 µm thick THB-151N, which corresponds to an aspect ratio (AR) of ten. Extensive diffraction effects are present, where full cross-linking occurs with both a 1 µm and a 100 µm air gap. Figs. 3.3e-h show a 20 µm diameter mold in 100 µm thick THB-151N (AR=5). This mold is significantly affected by diffraction, where full cross-linking occurs with a 100 µm air gap. Figs. 3.3i-l show that a 50 µm diameter mold is feasible with a 1 µm gap (AR=2), but not with a 100 µm gap. A critical threshold is passed when transitioning to a 100 µm diameter mask feature (AR=1), as shown in Figs. 3.3m-p, where even with 100 µm air gap, only minimal edge broadening is observed at the mold entrance.

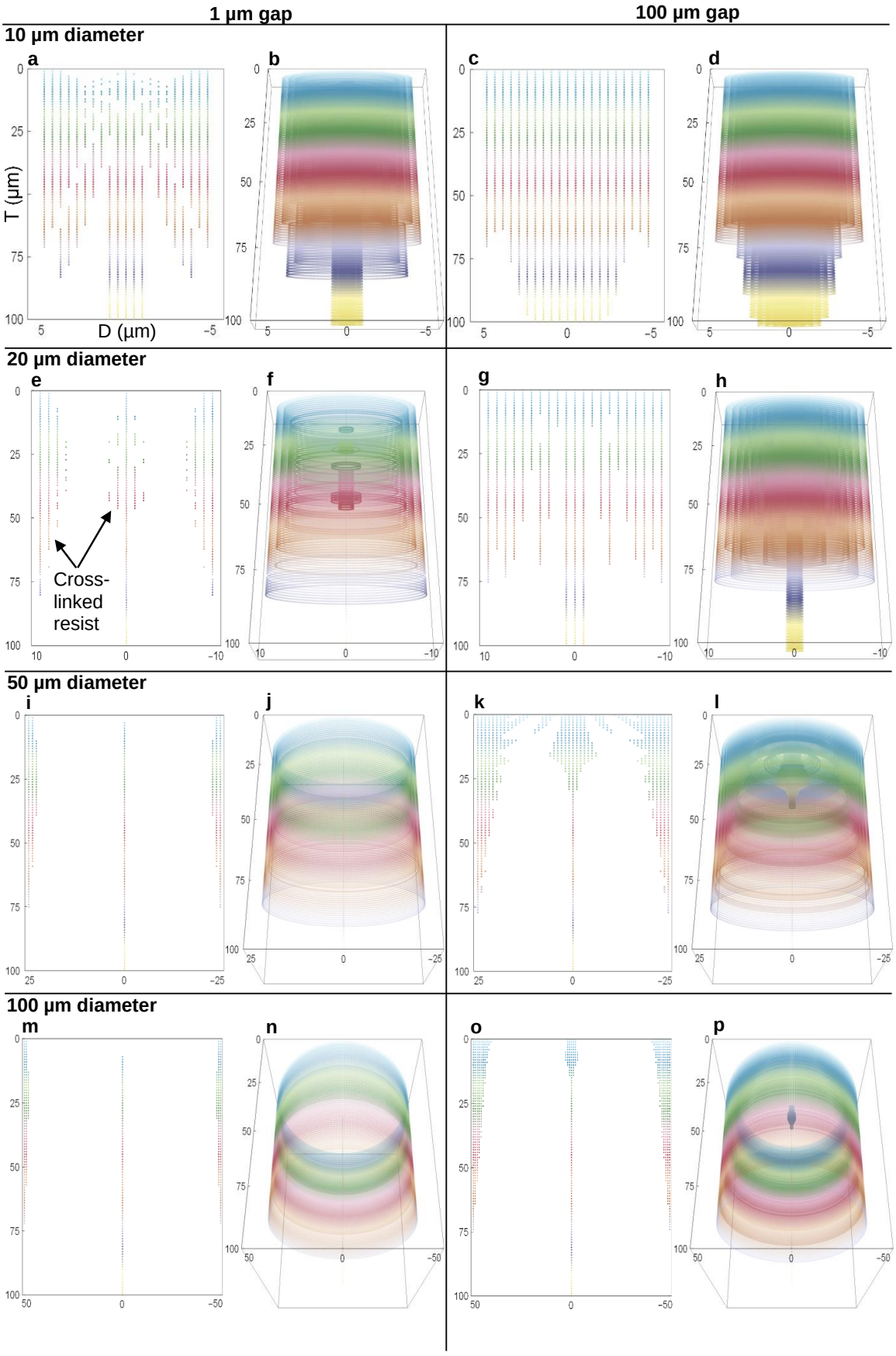
1 µm gap
100 µm gap
10 µm diameter
20 µm diameter
50 µm diameter
100 µm diameter
a
b
c
d
e
f
g
h
i
j
k
l
m
n
o
p
T (µm)
D (µm)
Cross-linked resist

Figure 3.3. Latent image simulations of varying photomask occulter diameters and air gaps. The ordinate is top downwards photoresist thickness, T, (μm) and the abscissa is feature diameter, D, (μm). The unobstructed aerial ED=1700 mJ/cm^2, diffraction λ=405 nm and the simulation resolution is 0.5 μm for **a-d** and 1 μm for **e-p**. Figure color scales with photoresist thickness to differentiate between height levels, where colored data points represent sites of cross-linked photoresist. Rows 1-4 correspond to 10, 20, 50 and 100 μm diameter circular occulters, respectively. Columns 1-2 and 3-4 correspond to air gaps of 1 and 100 μm. **a** 2D x-z photoresist cross-section with D=10 μm and g=1 μm. Light intensity calculation time (t) = 2 s. **b** 3D wrap-around view of **a** with a z-axis of rotation at x=0 and y=0. **c** 2D cross-section with D=10 μm and g=100 μm. t=1 s. **d** 3D wrap-around view of **c**. **e** 2D cross-section with D=20 μm and g=1 μm. t=5 s. **f** 3D wrap-around view of **e**. **g** 2D cross-section with D=20 μm and g=100 μm. t=1 s. **h** 3D wrap-around view of **g**. **i** 2D cross-section with D=50 μm and g=1 μm. t=37 s. **j** 3D wrap-around view of **i**. **k** 2D cross-section with D=50 μm and g=100 μm. t=15 s. **l** 3D wrap-around view of **k**. **m** 2D cross-section with D=100 μm and g=1 μm. t=1 m 41 s. **n** 3D wrap-around view **m**. **o** 2D cross-section with D=100 μm and g=100 μm. t=1 m 1 s. **p** 3D wrap-around view of **o**.

Three predictions are now made: 1) an AR of 1 is feasible in a standard broad-spectrum exposure of thick THB-151N photoresist, 2) development difficulty increases proportionally to mold AR and exposure gap length, and 3) all mold epicentres display a column of cross-linked resist that extends along the entire film thickness, which is due to the well-known Arago spot. The Arago spot is a luminous region in the epicentre of a circular shadow caused by the constructive interference of diffracted light rays with identical path lengths from a circular boundary.

Simulation results are now compared to directly corresponding experimental data. Figs. 3.4a-b are scanning electron microscope (SEM) images of a 25 μm target diameter photoresist mold exposed in 100 μm thick THB-151N (AR=4) with a photomask occulter gap length of 50 μm. These images display a “hard cap”, or a highly cross-linked region of photoresist that is extremely resistant to developer solution. This is predicted by the corresponding latent image simulation Fig. 3.4c, wherein a hard cap is clearly visible as a densely packed set of colored data points at the mold entrance.

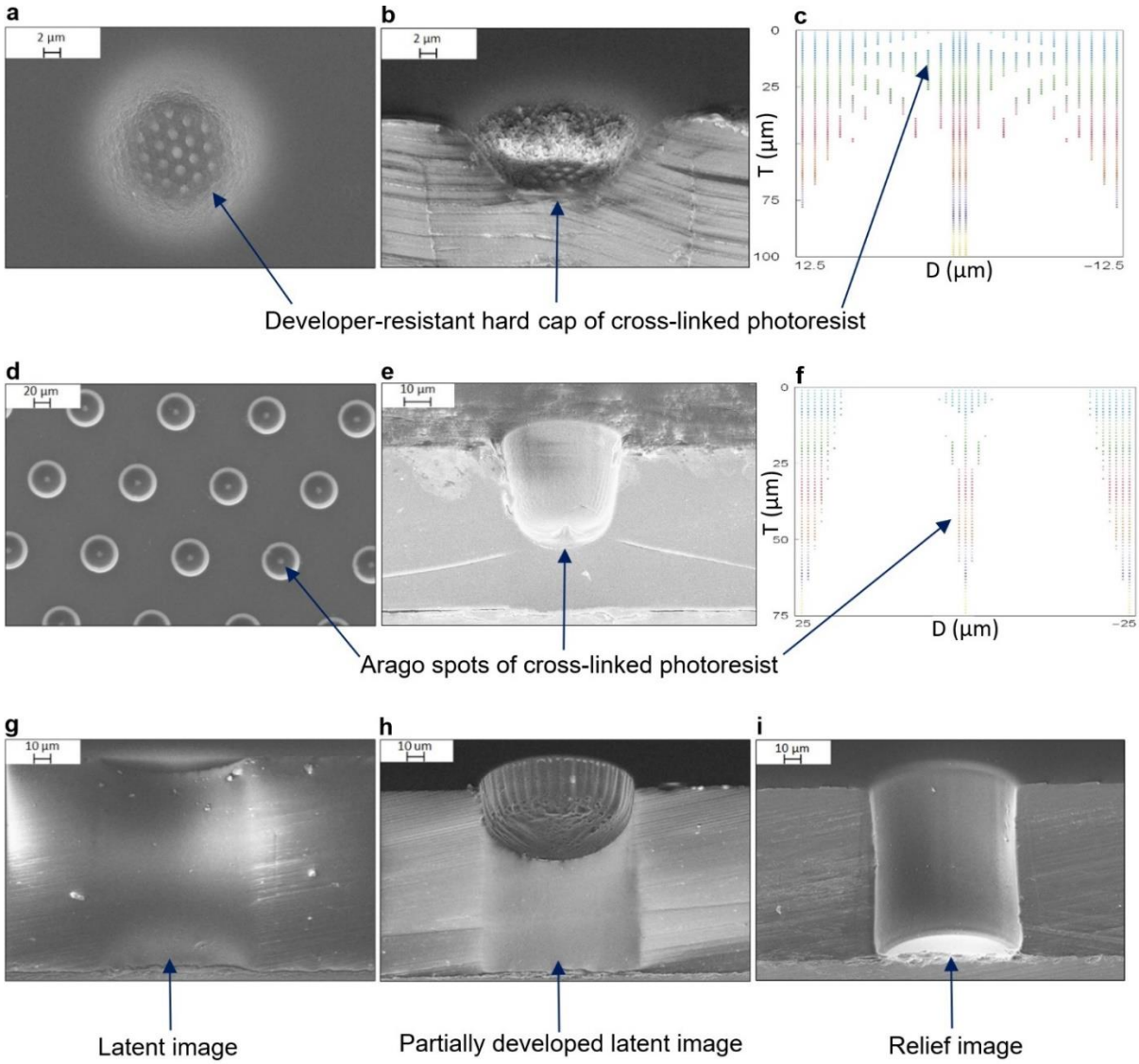

Figure 3.4. Comparison between experimental and simulation work. a Top-down SEM micrograph of a 25 µm target diameter photoresist feature hole displaying a developer resistant hard cap. **b** 68° angled cross-section of **a**. **c** Simulated latent image of **b**, also displaying a hard cap, with a simulation resolution of 1 µm, an ED=1700 mJ/cm^2, diffraction λ=405 nm and a 50 µm air gap. The ordinate is top-down photoresist thickness, T, (µm) and the abscissa is feature diameter, D, (µm). Light intensity calculation time (t) = 2 s. **d** Top-down view of an array of 50 µm target diameter photoresist feature holes demonstrating Arago spots in the feature epicentres. **e** 68° angled cross-section view of **d** with a photoresist thickness of 75 µm. **f** Simulated latent image of **e** with D=50 µm, g=50 µm and an ED=1100 mJ/cm^2, where all other parameters are as previously described. t=19 s. **g** 68° angled cross-section displaying the actual latent image of a 100 µm target diameter feature hole with a photoresist thickness of 125 µm and an exposure gap of 100 µm, as corresonds to simulation Figures 3.3 k and l. **h** Partially developed latent image of **g**. **i** Fully developed relief image of **g** after 90 s wet etch in stock TMAOH developer solution.

Figs. 3.4d-e show partially developed latent images of 50 µm target diameter resist molds exposed with a gap of 50 µm and a film thickness of 75 µm. The epicentre of the molds prominently displays the Arago spot, which is also seen in the corresponding latent image simulation, Fig. 3.4f. This latent image would easily develop under standard conditions with a simple two-part mechanism comprising: 1) the Arago spot creates a thin, ultra-high AR developer-resistant column of resist that nonetheless develops due to a high surface area and

structural instability, and 2) throughout mold development, a low AR transient developer-resistant bump is expected, as seen in Figs. 3.4d-e.

Figs. 3.4g-i show a 100 µm target diameter photoresist mold, exposed with a 100 µm air gap, transitioning from a full latent image, to a partially developed relief image, and to a full relief image, respectively. These molds develop with ease (90 s), as predicted by the corresponding latent image simulation Figs. 3.3k-l.

Figs. 3.4g-i clearly demonstrate that an AR of 1 is feasible in thick THB-151N, validating prediction 1. When taken together, Figs. 3.4a-i demonstrate an obvious proportionality between development difficulty and mold AR, validating prediction 2. Finally, in Figs. 3.4d-f, a developer-resistant bump is depicted in the epicentre of top-down latent image arrays, cross-sections and simulations, thus validating the final prediction.

It is observed in Figs. 3.3-3.4 that diffraction effects are hugely significant across the entire photomask diffractor, even when the incident wavelengths and diffractor sizes differ by more than two orders of magnitude. For example, significant latent image resolution-degrading effects are present in Figs. 3.3g-h with an h-line (405 nm) diffracting wavelength and a 50 µm diameter photomask occulter. This striking result is counter to conventional expectation, which assumes that diffraction effects only cause edge-broadening and are otherwise negligible at this size ratio. As an example, traditional calculations for photolithographic resolution, herein defined as the smallest printable feature size in a mask aligner, use the well-known formula (3.54)[21,56,57],

$$d = \frac{3}{2}\sqrt{\lambda\left(g + \frac{T}{2}\right)} \tag{3.54}$$

where d is the edge-broadening magnitude, λ is the incident wavelength, g is the air gap and T is the photoresist thickness. This equation states that while holding λ and T constant, the resolution degrading factor, d, can be minimized by reducing or eliminating the air gap. This is correct, as the results show, however diffraction effects across the entire target latent image are also hugely significant and must be included. The new succinct latent image formulae offer a significant advancement over this pre-existing equation, as they comprise a complete coupling between light propagation phenomena (including diffraction) and photochemical behavior.

3.4. Discussion

3.4.1 Methods for latent image simulations in photolithography with a polychromatic light attenuation equation for fabricating VIAs in 2.5D and 3D advanced packaging architectures

To enable predictive modeling of polychromatic exposure (e.g., with Hg bulbs) of photoresist films for VIA fabrication, a polychromatic light attenuation equation was derived from the Beer-Lambert law. The equation features novel components comprising, 1) the relative intensity of each of the incident wavelengths in broad-spectrum exposure, and 2) the

corresponding absorption coefficient for each wavelength. This enables novel methods and equations for photoresist ED and CED determination that can be used to produce accurate VIA latent image simulations by use of an exact scalar diffraction equation for circular diffractor geometries in the ultra-near aperture/occulter condition (F>>1). Whilst this method is demonstrated in proximity lithography, it could also be adapted for use in a high numerical aperture condition for projection lithography systems. This would require a diffraction formula that is accurate for off-axis points such as the provided Rayleigh-Sommerfeld scalar diffraction equations (3.20) and (3.21), or any suitable vector diffraction formulae.

This study demonstrates that accurate predictive modeling of diffraction effects is critically important for VIA fabrication in photolithography. Light diffraction can cause extensive undesired cross-linking underneath photomask occulters, leading to a hard cap that prevents relief mold formation. For broad-spectrum exposure, the hard cap effect could be minimized by using a long pass filter to selectively eliminate short wavelengths that would otherwise quickly absorb at the photoresist surface[46]. Additionally, diffraction effects can be reduced by minimizing the exposure gap, as demonstrated in Fig. 3.3. Alternatively, a shorter exposure wavelength (e.g., with monochromatic exposure) could be used that diffracts less due to a reduced wavelength to diffractor size ratio, which would require a photoresist with a suitable absorption characteristic.

The equations converge quickly on a standard modern computer. For example, when using parallelization and circular symmetry, equation (3.21) that was used to produce Fig. 3.3 calculated as much as 388-900x faster than other reported methods for 3D photoresist light intensity simulations[26,58]. The calculation time can be further reduced by increasing the step size between successive radial points, x_i, in (3.22), however this should remain sufficiently small to enable accurate mapping of the region of interest, wherein a minimum mold diameter to step size ratio (D:SS) can be verified and thereafter used as a standard. The minimum D:SS is 25:1 in Fig. 3.4, which was shown to be sufficient to produce accurate results by comparing latent image simulations to directly corresponding experimental work, with highly positive correlation. Therefore, and as a general rule, a D:SS of ≈25:1 with an SS not exceeding 1 μm is recommended. Furthermore, circular symmetry enables full 2D cross sections of the observation plane, wherein the grid density increases with inverse proportion to the wrapping angle step size, which can be made as small as desired without affecting the light intensity calculation time. A further note regarding the overall speed of this method is that it negates the need for time consuming in-situ metrology, which can also speed up the simulation process.

These qualities make this technique highly accessible to photolithography practitioners, whether in research or in manufacturing. Potential applications for this technique include: 1) numerical modeling with computational software such as Wolfram Mathematica, 2) integration into pre-existing photolithography simulators to broaden their computational domain by adding to their input space, and 3) development of a simple app for on-the-go use in mobile devices. VIA fabrication is expected to become increasingly important as demand grows for 2.5D and 3D advanced packaging architectures. These equations and methods leverage photolithography to assist in meeting this demand, which could be a valuable asset to emerging advanced packaging technologies.

3.4.2 Wet etching in photolithography: Development

Photoresist development consists of three main elements: 1) advection, 2) diffusion and 3) reaction kinetics. These elements need to be carefully tuned for maximum effect to successfully formulate an optimized development procedure, which is the focus of this section. The relevant theory is discussed in subsection 3.4.2.1 and an optimized development procedure is presented in subsection 3.4.2.2.

3.4.2.1. Development mechanisms

Following photoresist exposure, development is the process whereby a latent image pattern is transformed into a relief mold, as was shown in Figs. 3.4g-i. This involves submerging a patterned photoresist in a chemical bath comprising a solvent that selectively etches away unexposed photoresist (negative tone) or exposed photoresist (positive tone). In the case of THB-151N, soluble acrylate monomers are physically removed from the latent image with TMAOH developer, which are then transported away into the bulk developer solution. To accomplish this, fresh developer molecules must first diffuse into the regions of unexposed photoresist according to Fick's first law (3.55)[59], where the diffusive flux, J in $molm^{-2}s^{-1}$, is equal to the product of the diffusion coefficient, D in m^2s^{-1}, and the concentration gradient, ∇c in $molm^{-4}$.

$$J = -D\nabla c \tag{3.55}$$

The first parameter, D, is proportional to temperature according to the Stokes-Einstein relation (3.56)[59], where k_B is Boltzmann's constant in JK^{-1}, T is the temperature in K, η is the solution dynamic viscosity in Pa·s and r is the molecular radius.

$$D = \frac{k_B T}{6\pi\eta r} \tag{3.56}$$

Therefore, the diffusive flux can be increased by setting the developer to a limited maximum temperature that safely avoids unnecessary mold deformation and/or thin film delamination due to excessive heat transfer. A caveat to this is Newton's law of cooling (3.57)[60], which states that the developer temperature will change according to its current value, where Q is rate of heat transfer in W, h is the heat transfer coefficient in $Wm^{-2}K^{-1}$, A is the surface area in m^2 and ΔT is the temperature difference in K between the developer and the surrounding air.

$$Q = hA\Delta T \tag{3.57}$$

Due to this, an exponential decrease in developer temperature, and therefore the diffusive flux, will occur upon heat source removal. This condition is optimized by either never removing the heat source or constantly refreshing the bath with a heated solution.

Advection can be exploited to further increase the diffusive flux by forcing the local concentration gradient, ∇c, to a maximum value, as depicted in Fig. 3.5.

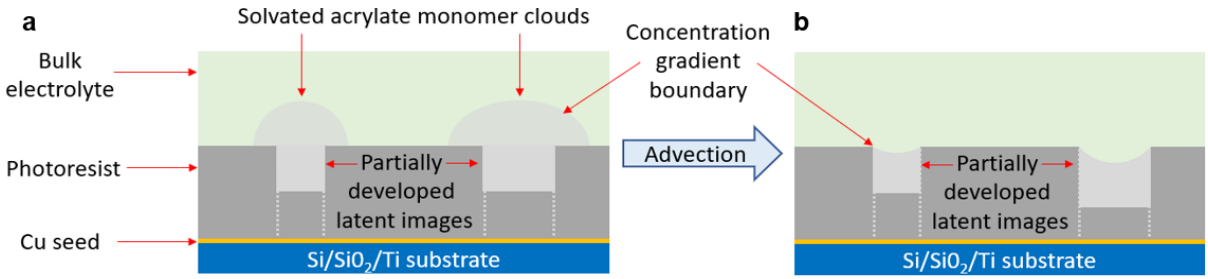

Figure 3.5. The role of advection in increasing diffusive flux. a A bulk solution with no advection. TMAOH developer reacts with acrylate monomers then diffuses away from the resist surface and accumulates in a stagnant bulk solution. Over time, this process creates localized clouds of solvated acrylate monomers above developing resist molds, which reduces the concentration gradient and hinders diffusive flux. **b** Alternative depiction of **a**, but with advection. Advection homogeneously distributes solvated acrylate monomers to drive an isotropic bulk concentration. The bulk solution penetrates deeper into the low aspect ratio mold, increasing the local development rate by reducing the diffusion barrier thickness.

When holding the puddle volume constant, the maximum bulk concentration is reduced over time as the reaction proceeds towards equilibrium. To remedy this, the solution needs to be constantly refreshed to keep the concentration gradient close its initial value at t = 0. Additionally, and when holding the mold aspect ratio constant, strategic placement of the advective source can also be used to further reduce the diffusion barrier thickness.

Once the developer has travelled to the acrylate monomers by diffusion, the reaction kinetics then take over. The reaction speed depends on the rate constant, which exponentially increases with temperature according to the Arrhenius equation (3.58)[61], where A is a coefficient in s^{-1} for a first order reaction, E_a is the activation energy in $Jmol^{-1}$, R is the ideal gas constant in $Jmol^{-1}K^{-1}$ and T is the temperature in K.

$$k = Ae^{\frac{-E_a}{RT}} \tag{3.58}$$

The optimal development procedure should use an increased developer temperature to increase D in Fick's first law (3.55) and k in the Arrhenius equation (3.58). Furthermore, the solution should be constantly refreshed with new puddles and advection to maximize the second and final parameter, ∇c, in (3.55), which synergizes with maintaining a heated developer, as required by the exponential decay of the developer temperature in Newton's law of cooling (3.57). Therefore, an optimized development procedure needs an elevated bath temperature with constantly refreshed puddles and efficient advection to reduce the diffusion barrier thickness to a minimum. The benefit of increasing the developer temperature is demonstrated in Fig. 3.6.

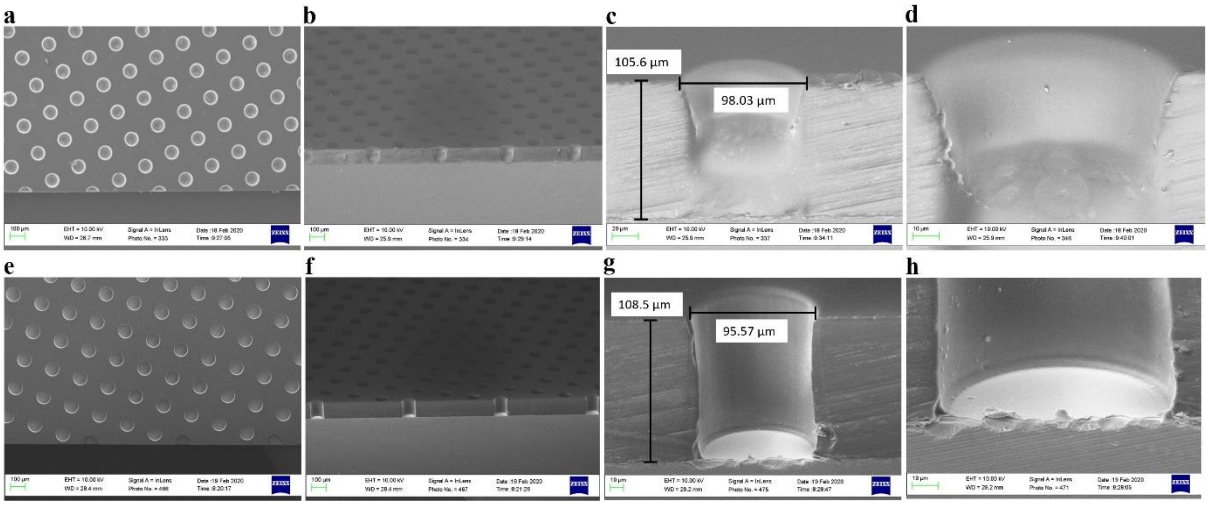

Figure 3.6. Developer temperature efficacy. a Top-down view of a circular mold array in THB-151N developed with a room temperature TMA238WA developer solution (≈20 ºC). **b** 68º angled view of **a**. **c** Magnified view of **b**. The actual film thickness is 105.6/sine(68º) = 113.89 µm. **d** Magnified view of **c** showing the bottom-most developed point, which extends to around half the film thickness (T/2). **e** The same as **a**, processed with identical conditions except for an elevated developer temperature of 60 ºC. **f** 68º angled view of **e. g** Magnified view of **f**. The actual film thickness is 117.02 µm. **h** Magnified view of **g** showing the bottom-most developed point, which fully extends through the photoresist down to the substrate surface.

3.4.2.2. Development methodology

I trialed various development methods, including: 1) submerging in a static receptacle, 2) heating, 3) seesawing, 4) using an impeller, 5) pumping, 6) sonication, 7) plunging and 8) spin developing. A brief description of each follows.

Submerging in a static receptacle is the most basic development method, wherein the convection component is virtually zero. The diffusion barrier thickness is equal to the solution thickness and the reaction rate is baseline. Heating a receptacle creates a temperature differential along the x-z cross-section of the developer solution. This causes developer molecules to rise and fall as heat is transferred from hot to cold, creating a minor convection effect. Seesawing entails manually agitating a receptacle by rocking from left to right, inducing a minor sinusoidal advection effect. An impeller induces circumferentially oriented flow streamlines, wherein low to high Reynolds numbers can be used. Drawbacks are uneven stirring due to impeller placement and solution viscosity causing kinetic energy to dissipate near the resist surface. A pump creates either radially or vertically oriented flow streamlines, however in the latter case, a low flow rate is necessary to prevent mold deformation. In sonication, an electrical current passed through a submerged piezoelectric transducer causes cavitation in the developer solution, liberating loosely bound photoresist monomers. The bubbles are microscopic at the standard frequency of 80 kHz, which makes this technique suitable for cleaning capillaries. In the case of THB-151N however, the bubbles collapse with sufficient energy to damage cross-linked photoresist molds, rendering this method inadequate. Plunging is performed by submerging a substrate in a tall-form receptacle. The developer is forced into vertically oriented streamlines by either raising the substrate up and down via a marionette mechanism or plunging from above in a piston arrangement. Spin development comprises a patterned substrate attached to a spinning vacuum chuck, onto which developer solution is dispensed to create a localized transitory puddle, as depicted in Fig. 3.7.

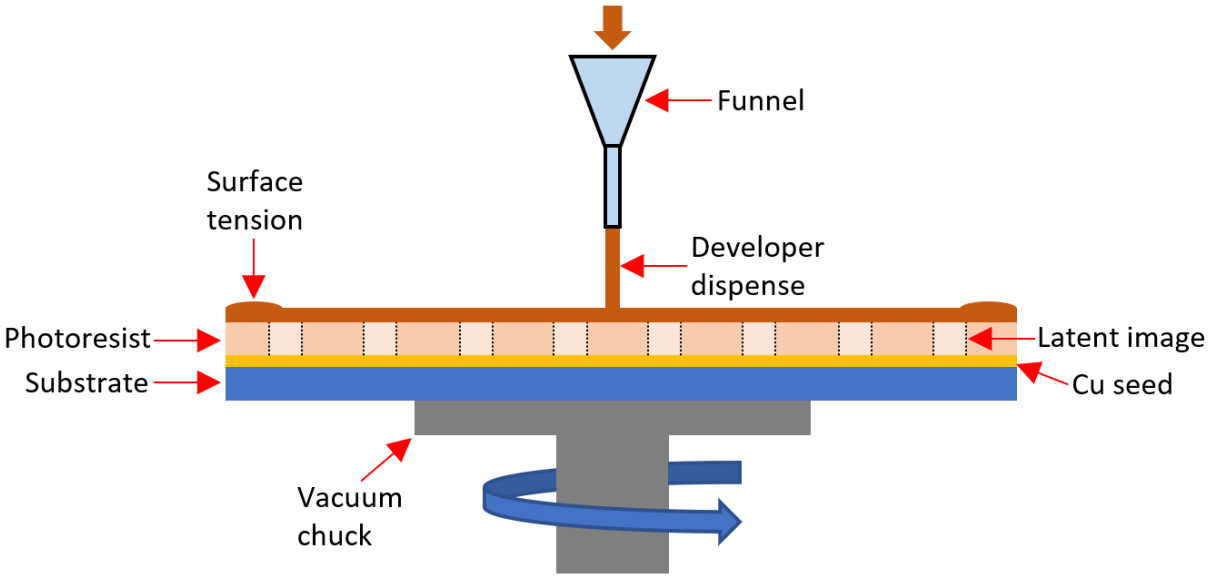

Figure 3.7. Spin development schematic. Developer solution is dispensed through a funnel to create a puddle on a patterned photoresist. The developer sticks to the photoresist due to surface tension, wherein the puddle volume is a function of the developer to resist/substrate contact angle and the substrate spin speed.

A typical puddle volume on a 120 µm thick film of THB-151N patterned on a 100 mm diameter substrate with a 7 mm wide concentric Cu plating ring at 40 rpm is ≈25 mL of TMA238WA developer. Spinning creates force vectors tangential to the substrate's rotational curl which propel solvated acrylate monomers to the outer wafer radius. At 200 rpm and above, angular momentum overwhelms surface tension and the puddle's volume approaches zero as the rotational speed increases. Additionally, sudden changes in the substrate spin speed accelerates developer molecules and alters their angular momentum, which uniquely induces advection inside capillary-like photoresist molds. This can be accomplished, for example, by cycling the spin speed in quick succession from 10-40 rpms. Furthermore, and since the substrate is spun from below, advection streamlines are virtually in contact with the photoresist, which is analogous to placing an impeller infinitely close to the photoresist surface. This reduces the diffusion barrier thickness to a minimum.

Spin development thus offers highly efficient advection, easy control over puddle duration and is compatible with a heated developer dispense. As these qualities perfectly align with the optimized development procedure outlined in the preceding theory section, I used spin development in all my standard operating procedures. An example spin development procedure is provided in Table 3.1.

Table 3.1. Spin development procedure. Steps 1-3 develop the latent images and steps 4-6 rinse the film. Steps 1-3 can be repeated as many times as required, depending on the target mold aspect ratio and the developer temperature. The listed dispense volume is the minimum to form a continuous puddle on a 4" substrate rotating at 40 rpm after an initial wetting volume of 25 mL.

Step	Time (s)	Speed (rpm)	Accel. (rpm/s)	Special	Dispense Type	Quantity (mL)
1	5	100	100	Repeat 2x	Developer	12.5 per pass
2	60	40	100			
3	5	200	100		None	N/A
4	60	200	100	N/A	DI Water	200 total
5	10	300	100			
6	50	500	200		N/A	N/A

3.4.3. Future work

For future work, an aim is to investigate an intriguing periodic photoresist pattern comprising brightly colored bumps that correspond to the nodes of an expanded six-petal rosette. This pattern was observed in separate experiments and across different analysis equipment (light microscope and SEM), as shown in Fig. 3.8. This is an unexpected result, as circular diffractors have rotational symmetry and should only display concentric patterns. A mathematical description of this phenomenon could be useful to diffraction theory.

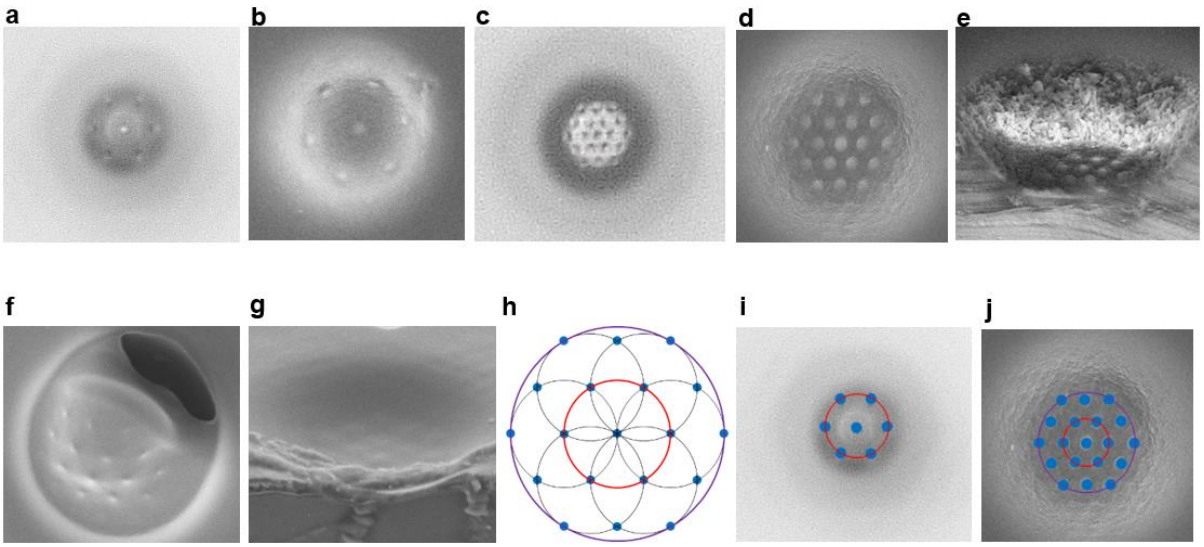

Figure 3.8. Patterned phenomenon in photoresist, observed with different machinery, process parameters and on different dates. a Top-down light microscope image of a hard capped 50 µm target diameter photoresist feature taken on Feb 3, 2020. **b** Top-down SEM micrograph of a hard capped 50 µm target diameter photoresist feature taken on Feb 10, 2020. **c** Top-down light microscope image of a hard capped 25 µm target diameter photoresist feature taken on Feb 3, 2020. **d** Top-down SEM micrograph of a hard capped 25 µm target diameter photoresist feature taken on Feb 13, 2020. **e** 68° angled cross section of **d**. **f** Top-down SEM micrograph of a hard capped 100 µm target diameter photoresist feature taken on Feb 19, 2020. **g** 68° angled cross section SEM micrograph of a partially developed 10 µm target diameter photoresist feature taken on Feb 1, 2018. **h** Expanded six-petal rosette pattern with eighteen highlighted blue intersection points and concentric circles one (red) and two

(purple). **i** Image **a** superimposed with circle one (red) and six intersection points. **j** Image **d** superimposed with circles one (red), two (purple) and all eighteen intersection points.

3.5. Materials and methods

A 100 mm diameter substrate was used with a thickness cross-section from the basal layer upwards of: 525 µm Si, 250 nm $Si0_2$, 20 nm Ti, and 200 nm Cu. The substrate was first submerged for 30 s in a 150 mm x 25 mm glass petri dish from BRAND (Wertheim, Germany) containing a 10:1 volumetric dilution of deionized (DI) water: S20 Cu cleaner, a solution comprising surfactants and sulfuric acid from Schlötter Ireland DAC (Kildare, Ireland). The substrate was then rinsed in DI water, dried with a N_2 gun, baked on a hot plate for 5 min at 110 ℃ to evaporate residual surface-adsorbed H_2O molecules, and then cooled to room temperature (RT). Next, a Laurell (PA, USA) alignment tool was used to attach the substrate's basal layer to a 45 mm diameter press-on mount vacuum chuck in a WS-650MZ-23NPPB Laurell photoresist spinner to prepare for two spins. All photoresist processing was carried out under yellow ambient light to prevent stray UV radiation from causing undesired photoresist cross-linking.

Prior to the first spin, RT THB-151N photoresist from JSR Micro NV (Leuven, Belgium) was manually dispensed onto the top Cu layer and bubbles were removed by suctioning with a disposable pipette to ensure spin uniformity. The first spin comprised six steps: 1) 300 rpm for 25 s to spread out the photoresist, 2) 0 rpm for 30 s to enable reflow, 3) 300 rpm for 10 s as an initial ramp speed, 4) 1,100 rpm for 30 s as the thickness-determining step, 5) 300 rpm for 30 s to enable edge bead removal (EBR) with 15 mL AZ EBR Solvent from Microchem GmbH (Ulm, Germany) dispensed through a pressure-actuated automatic syringe with a 1 mm diameter aperture aimed 7 mm from the substrate edge to ensure suitable bead removal, and finally 6) 1,000 rpm for 2 s to level off the photoresist. The substrate was then soft baked in contact mode for 5 min at 130 ℃ on a hot plate and cooled to RT. The target film thickness was 60 µm. Due to a variability in processing conditions (temperature, humidity, etc.), the standard operating procedures produced thick films with a ±5 µm thickness around the target specification. Film thickness metrology was performed with a KLA-Tencor (CA, USA) P-15 surface profilometer. It is noted that in-situ EBR is superior to scalpel EBR to best preserve the target spin thickness. This is because as photoresist edge beads are removed, the resist flows radially into the newly created circumferential voids, reducing the film thickness. When using a scalpel to perform EBR for example, this mechanism can act more than once, or even several times, significantly reducing the target spin thickness.

The THB-151N application method was used again for the second layer of applied photoresist. The second spin comprised five steps: 1) 300 rpm for 10 s to spread out the photoresist, 2) 0 rpm for 30 s to enable reflow, 3) 800 rpm for 110 s as the thickness-determining step, 4) 300 rpm for 30 s to enable EBR, as was previously described, and 5) 1,000 rpm for 2 s to planarize the photoresist. The substrate was then soft baked a second time in contact mode for 5 min at 130 ℃ on a hot plate and cooled to RT. The final target film thickness of this procedure was 120 µm. It is noted that simply repeating the first spin step twice would not produce a 120 µm thick film. This is due to the decreased contact angle at the resist-to-resist interface, as opposed to the resist-to-Cu interface. Van der Waals forces cause the second spin layer to become more

viscous than it otherwise would be, thus increasing the target spin thickness by about 150% (ex. a 40 µm target second spin thickness is actually about 60 µm). Additionally, an 80 µm target thick film was fabricated with this procedure by using a single spin with a main spin step of 950 rpm for 20 s.

The photoresist was then exposed through a 127 mm^2 Compugraphics (Glenrothes, Scotland) glass photomask with an 86 mm diameter chrome pattern in a Canon (Tokyo, Japan) PLA600F Mask Aligner using a broad-spectrum USHIO (Livingston, UK) USH-250D Super High Pressure UV type mercury lamp with an i-line intensity of 5.3 $mWcm^{-2}$. Aerial exposure doses of 1100 and 1700 $mJcm^{-2}$ were delivered for the 80 and 120 µm target photoresist film thickness, respectively. As a final processing step, the latent image patterned substrate was again attached to the WS-650MZ-23NPPB Laurell photoresist spinner chuck and spin developed. A glass funnel was installed above the substrate and predefined volumes of JSR Micro TMA238WA TMAOH based photoresist developer solution were poured onto the rotating photoresist surface, as described in section 3.4.2.2.

SEM analysis requires a conductive electron substrate. The complex refractive index, by use of equations (3.59) and (3.60)[44] and assuming $\mu_r = 1$, enabled the determination of the relative permittivity (2.48) and resistivity of the THB-151N photoresist used in this chapter (e.g., 1.79 $\times 10^8$ Ωcm at a microinductor switching frequency of 10 GHz for granular switch-mode power supply (SMPS) integrated voltage regulator (IVR) applications). It is noted that n and K were calculated from the THB-151N photoresist Cauchy coefficients.

$$n^2 - K^2 = \epsilon_r \mu_r \tag{3.59}$$

$$\sigma = \frac{2nK\epsilon_0 \omega}{\mu_r} \tag{3.60}$$

To enable SEM imaging, and since the THB-151N is an electrical insulator, the samples were sputtered with ≈10 nm of Au/Pt and scanned with a 10 keV electron beam at low penetration depth. Aerial and latent image simulations were performed in Wolfram Mathematica v11.1 on a computer with 16 GB Corsair (CA, USA) Vengeance DDR4 2666MHz RAM, an Intel (CA, USA) Core i5-9400F CPU @ 2.9 GHz (6 cores/threads), an Nvidia (CA, USA) GeForce GTX1660 Super 6GB GPU and a Samsung (Seoul, South Korea) 970 EVO Plus 500GB SSD (NVMe M.2 form factor).

Click to skip to next chapter.

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Chapter 4 - VIA Electroplating: Metallization in 3D Photoresist Relief Structures

4.1. Introduction

Unlocking the potential of next generation micro- and nano-devices requires effective implementation of 3D conductors. 3D conductors are vertically oriented, which minimizes device footprint area and enables unprecedented metrics for device performance, versatility and efficiency through increased granularity and point-of-load (PoL) power delivery. Ubiquitous in the semiconductor industry, electroplating into wafer scale photoresist mold arrays is a high-throughput technique that can be readily utilized to fabricate 3D micro and nanoconductors, which are otherwise known as VIAs, or vertical interconnect access points. I utilized electroplating to fabricate 3D microconductor VIAs, the setup of which is depicted in Fig. 4.1.

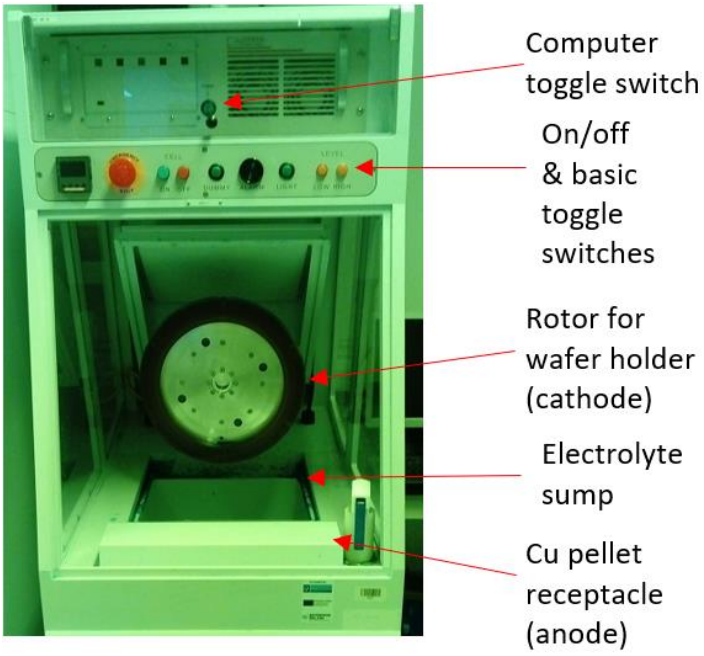

Figure 4.1. Image of our dedicated Cu electroplating setup. This single-cell rotational plating system was manufactured by the Digital Matrix Corporation. The photo is yellow green in color due to the photochemically inert ambient lighting in the plating lab. Once turned on, an acid copper electrolyte fills the sump and is heated to ≈21 ºC. A pump continuously agitates the electrolyte, which is Schloetter's Bright Copper ACG 8 comprising copper salt FG (0.24 g/L), sulfuric acid (3.3% by volume), hydrochloric acid (0.019% by volume), Starter ACG 8 (0.4% by volume) and deionized water (70+% by volume). During operation, a wafer holder clasping a 100 mm diameter photoresist mold patterned Si wafer is placed in the rotor, which then rotates at a user specified rpm. Rotor rpm, current settings and plating duration are inputted into an adjacent computer.

Once the wafer enters the copper sulfate electrolyte, an external voltage is immediately applied across the cathode/anode connections to ensure a sufficient overpotential so that the sputtered Cu seed does not etch. To avoid rough plating topography and discontinuous feature cross-sections, it is critical to specify a sufficient electrochemical cell current to establish a reasonable electroplating current density. Typical current density values are between 1-5 A/dm^2, wherein

the plateable surface area is calculated from the photomask layout and common plating rates range from 0.2-1µm/min. Typical rotor speeds are between 1-10 rpm.

Cu electroplating is ubiquitous in the semiconductor industry due to its high-throughput capability to form interconnects with low electrical resistance, high current density and high electromigration resistance[1]. In the effort to advance understanding of the complex electroplating process and to enable continued line width scaling and optimized processing, various Cu electrodeposition simulation methods have been reported in the literature. Simulations fall into two main categories: 1) continuum models that use partial differential equations to express physical quantities (e.g., charge, mass, momentum) as continuous variables (e.g., using mesh boundaries)[2,3,4,5,6,7,8,9,10,11] and 2) molecular simulation models that treat ions and molecules as discrete particles or groupings of particles (e.g., the kinetic Monte Carlo (KMC) method)[12,13,14,15,16,17,18,19,20,21,22]. Reported continuum models for Cu electroplating use diffusion-consumption[1,23,24,25,26], curvature enhanced accelerator coverage[27,28,29,30,31,32,33,34,35], time-dependent transport[36,37] and hydrodynamic[9,38,39,40,41,42,43] theory[44]. The KMC method treats Cu electrodeposition as a stochastic process, for which statistical mechanics are used[44]. Due to the large amount of computational resources required for molecular resolution simulations, many reported KMC methods also include elements of continuum theory to enable multiscale modeling (e.g., angstrom to microscale)[44].

Superconformal plating is a key focus in the literature, wherein the dynamic interaction of accelerators, suppressors and levelers is investigated to enable void-free plating of Cu trenches and VIAs coated in a conformal seed layer[1,7,12,13,15,16,17,18,25,26,27,28,29,30,31,32,33,34,35,36,37,45]. Significantly less attention has been given to electrode surface morphology in bottom-up electroplating of Cu trenches and VIAs[24,46,47]. The Cu electrode topography was shown to change from flat to concave during trench/VIA electroplating using 2D electrode growth simulations, which is due to vertically collimated Cu^{2+} diffusion streamlines combining with radial Cu^{2+} diffusion streamlines as the electrodeposit approaches the mold boundary[24]. The concave Cu electrode topography was shown to be modifiable by introducing bulk electrolyte flow (advection), wherein the radial location of Cu^{2+} rich eddies is a function of the flow rate[40,41].

To my knowledge, no 3D electrode growth simulations have been reported that investigate Cu electrode topography as a function of the interplay between diffusion and advection in bottom-up electroplating (insulating side walls). Furthermore, a feasible method to achieve a highly convex Cu electrode surface has not yet been reported, which could be very useful for sensor applications wherein a large electrode surface area is known to increase sensitivity limits[48]. Due to the large degrees of freedom in 3D systems comprising many constitutive equations, axisymmetric geometries that exploit circular symmetry are often used to enable dimensional reduction[2]. However, to enable bulk electrolyte flow from one direction (as opposed to everywhere radially), whereby the interplay between diffusion and advection can be investigated, a full 3D simulation geometry is necessary. Enabling a fast-converging, full micron scale 3D simulation (e.g., 200x200x200 µm) comprising many constitutive equations for each of the necessary physics modules involved (e.g., tertiary current distribution and laminar flow with a moving boundary) is a significant challenge, which is addressed in this chapter.

4.2. 3D simulations in COMSOL Multiphysics

Rigorous CAD simulations require detailed theoretical knowledge of the system of interest, which is essential for effective fabrication methodologies. This section utilizes CAD modeling in COMSOL Multiphysics to investigate methods to tailor the topography of electroplated 3D conductive components. This enables meeting the design specifications of flat, convex, or concave substrate-distal electroactive surfaces. Flat conductor surfaces are ideal for microbump soldering and flip-chip fabrication methods and concave/convex designs increase the number of available electrode reaction sites for sensor applications.

I performed 3D COMSOL simulations comprising: 1) electrochemistry modeling with the Nernst-Planck and Butler-Volmer formulations for mass transfer and reaction kinetics, 2) laminar flow of a Newtonion fluid, the standard advection protocol for electrochemical baths, and 3) a deformed geometry physics module to track a growing electrode during electrodeposition. Simulation results of flat and concave surface profiles are compared to directly corresponding experimental work, with positive correlation. By use of virtual mathematical modeling tools, such as COMSOL Multiphysics, crucial insights into the electroplating process are gained.

4.2.1. Fundamental equations

Electroplating models comprise two main constitutive equations for mass transfer and reaction kinetics. Mass transfer entails physically moving the electroactive species from anode to cathode, whereupon the reaction kinetics take over to form an electrodeposit. This is depicted in the copper sulfate electrolytic cell in Fig 4.2.

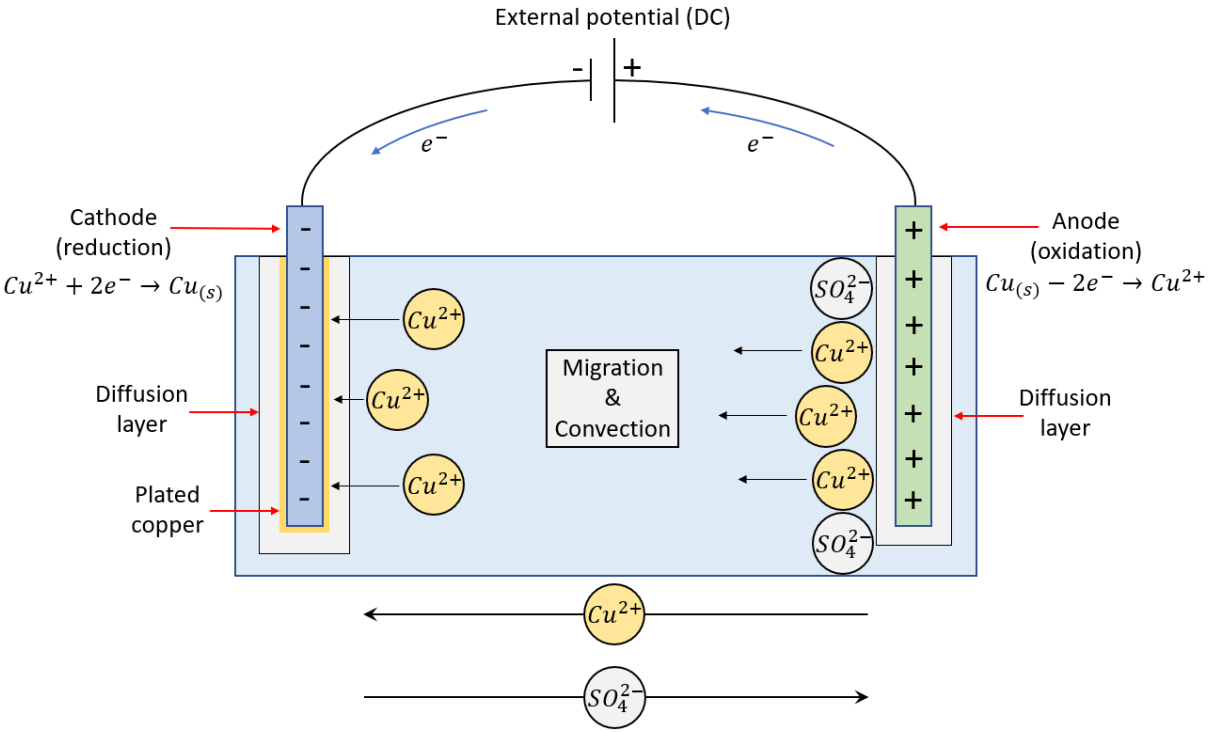

Figure 4.2. Copper sulfate electrolytic cell. An external potential is applied across the electrodes to induce oxidation at the anode and reduction at the cathode. Once ionized to Cu^{2+}, the electroactive species first traverses the anode diffusion layer, then the bulk solution via migration and advection, and then finally the cathode diffusion layer. The reaction is 1:1 for reactants to products and requires a two-electron transfer.

The constitutive equations for this process are discussed in the following sub-sections.

4.2.1.1. Nernst-Planck mass transport

As shown above, mass transfer entails components for diffusion, migration and advection. Diffusion occurs when a substance moves along a concentration gradient. Migration occurs when an electroactive species moves in response to an electric field and advection results from pumping, stirring or otherwise agitating the electrolyte. A formula that accounts for all of these factors is the Nernst-Planck equation for mass transport, as shown in (4.1)[49].

$$N_i = -D_i \nabla c_i - \frac{z_i F D_i c_i}{RT} \nabla \emptyset + c_i \vec{u} \tag{4.1}$$

N_i is the overall transport vector for the *i*th electroactive species in units $molm^{-2}s^{-1}$. The first factor describes diffusion, which entails D_i, the diffusion coefficient in m^2s^{-1} and ∇c_i, the concentration gradient with units of $molm^{-4}$. The second factor accounts for migration, where z_i is the unitless ionic species charge, F is Faraday's constant in $Cmol^{-1}$, R is the ideal gas constant in $Jmol^{-1}K^{-1}$, T is in K and $\nabla \emptyset$ is the field potential gradient in Vm^{-1}. The last factor comprises a flow term, $\vec{u}$ in ms^{-1}, for the advection condition. The corresponding physics module in COMSOL Multiphysics that accounts for all three mass transport mechanisms is the Tertiary Current Distribution (TCD) module which will be described in detail in section 4.2.2.2 below.

4.2.1.2. Butler-Volmer electrochemical kinetics

The governing redox kinetics equation is the Butler-Volmer formula (4.2)[49].

$$i_{loc} = i_0 \left(C_O exp\left(\frac{\alpha_a F \eta}{RT}\right) - C_R exp\left(\frac{\alpha_c F \eta}{RT}\right) \right) \quad (4.2)$$

The localized electrode current density, i_{loc} in units of Am^{-2}, is local in the sense that it varies across the electrode topography. This is an essential quality, as it enables simulating complex 2D and 3D electrode growth by factoring in local deviations in the reaction kinetics with a resolution proportional to the geometry mesh size. As this is a redox equation, it comprises two parts, one for oxidation at the anode (left) and another for reduction at the cathode (right). The exchange current density coefficient, i_0 in Am^{-2}, is the electrochemical cell current density at zero overpotential. The dimensionless factors C_O and C_R are fractions of the time-sensitive oxidized and reduced electroactive species concentrations to the respective reference concentrations at t=0. The dimensionless anodic and cathodic transfer coefficients are α_a and α_c, respectively. The overpotential is η in V $(E - E_{eq})$, and all other parameters are as previously described.

Inserting C_O and C_R into this equation is optional, but doing so forces concentration dependent kinetics, which is essential to accurately model VIA electroplating. This is true even in the case of a perfectly stirred bulk electrolyte providing a quasi-infinite number of electroactive specie at the diffusion barrier due to a two-part transport mechanism comprising: 1) advection streamlines being unable to penetrate high aspect ratio (HAR) vias forcing diffusion mass transport[9], and 2) electroactive specie with low diffusion coefficients traversing elongated diffusion streamlines inside high aspect ratio (thickness/diameter) photoresist mold columns. This creates an ion scarcity at the electrode-electrolyte interface, which must be accounted for in the corresponding kinetics equation. The mechanism is depicted in Fig. 4.3.

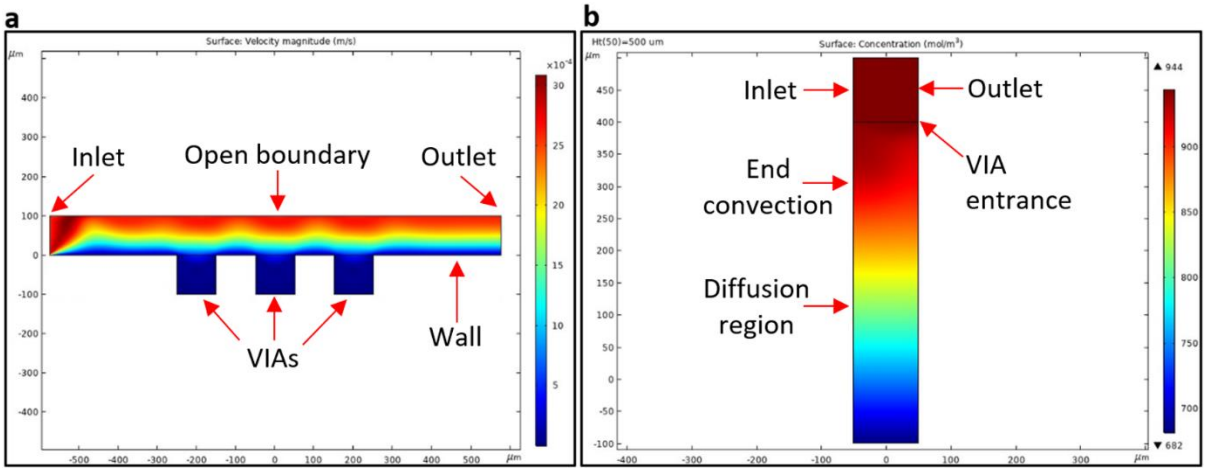

Figure 4.3. VIA flow dynamics. a 2D cross-section of three VIAs, each with an AR of 1, submerged in an aqueous electrolyte (Newtonion) where bulk flow is introduced from the left. The electrolyte is color-mapped according to velocity. The inlet flow speed is 2.62 mms^{-1}, which corresponds to a reference half radial point on a 100 mm diameter Si wafer rotating at 1 rpm, as corresponds to my experiments. The flow profile is laminar due to a low Reynolds number (e.g., <$5x10^5$ for a flat plate), where $Re = \rho u L/\mu$ and ρ is the density in kgm^{-3}, u is the flow rate in ms^{-1}, L is the characteristic length in m and μ is the fluid kinematic viscosity in m^2s^{-1} [50]. The flow

is pinched on the left boundary due to the inlet boundary condition, which then quickly separates from the substrate due to the fluid's viscosity. The key takeaway is that the flow does not penetrate deep into the VIAs, whereby mass transport inside the VIAs does not include an advection term. **b** 2D cross-section of a HAR VIA (5:1) with an inlet on the left, an outlet on the right and an open boundary on top. The electrolyte is color-mapped according to concentration and the reference value, 944 $molm^{-3}$, corresponds to my experiments. The horizontal wall was removed from the geometry to induce maximum flow into the VIA. The key takeaway is that even in the ideal case wherein the horizontal viscosity component is entirely removed, all advection halts inside the VIA around 100 µm down. Beyond this point, elongated diffusion streamlines are present, which significantly reduces the electrolyte concentration at the electrode surface as a function of the diffusion coefficient magnitude.

4.2.2. Solver settings

This section details the geometry and the physics modules I used to simulate 2D and 3D electroplating with COMSOL Multiphysics. It is a robust simulation platform that utilizes the finite element method (FEM) to solve complex problems. The FEM breaks up a simulation geometry into a continuous set of discrete areas (pixels) in 2D and volumes (voxels) in 3D, each of which is demarcated by a set of boundaries. The boundaries are fitted to a fundamental shape, which is typically a triangle in 2D and a tetrahedron in 3D. As an example, and for these shapes, each discrete finite element has three boundaries in 2D and four in 3D. The simulation is computed by solving the set of physics equations at each of the demarcated boundaries in the FEM mesh.

Care must be taken to ensure a sufficiently complex mesh that comprises enough discrete area or volume nodes to accurately model the real-world process with an acceptable margin of error. Timely convergence is also an essential simulation quality, which is key for troubleshooting problems and producing rapid solutions. Solver time is a function of the system's degrees of freedom, which is proportional to the pixel/voxel count and the magnitude/complexity of the physics equation set. Due to this, accuracy and solver speed are diametrically opposed, whereby effective simulations must find a pragmatic compromise.

For typical simulations, the need for cloud or cluster computing can be circumvented with an optimized mesh and a suitable up-to-date computer. With regards to computer hardware, RAM builds the FEM mesh, equations are solved with the CPU and a GPU displays the geometry and enables orientation manipulation (rotating, zooming, etc.). The computer used for this work had 16 GB Corsair Vengeance DDR4 2666MHz RAM, an Intel Core i5-9400F CPU @ 2.9 GHz (6 cores/threads), an Nvidia GeForce GTX1660 Super 6GB GPU and a Samsung 970 EVO Plus 500GB SSD (NVMe M.2 form factor).

4.2.2.1. Geometry

Utilizing 2D geometry is a great starting point for 3D CAD simulations, as it simplifies troubleshooting in complex 3D meshes and establishes a reference point to which 3D results can be compared. Several example geometries, inclusive of the FEM mesh are shown in Fig. 4.4.

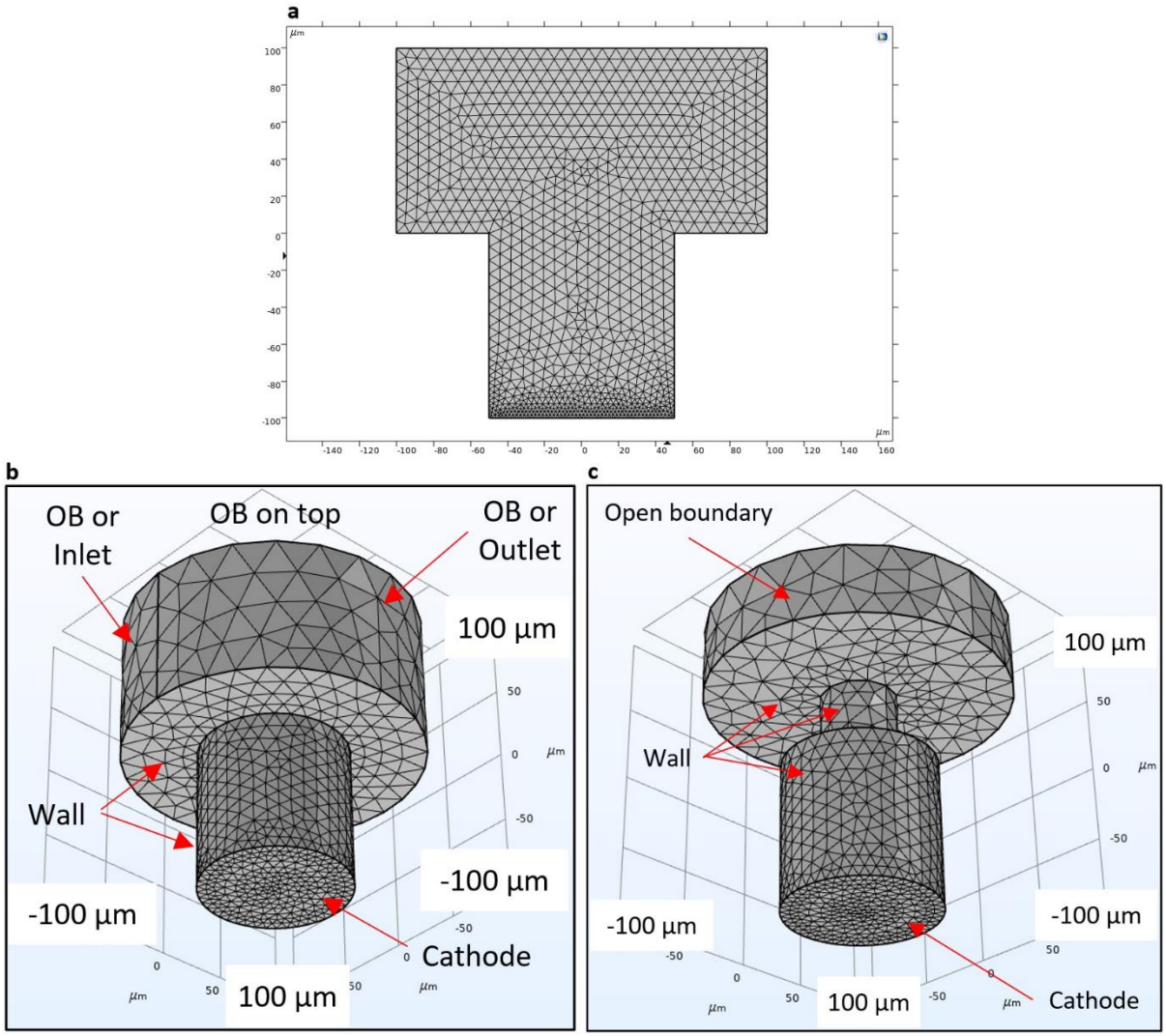

Figure 4.4. Solver geometries and FEM meshes. a 2D VIA mold (bottom rectangle, AR=1) and bulk electrolyte (top rectangle) joined at the internal boundary by COMSOL's Union function. The wall and electrode locations are as previously labelled in Fig. 4.3. The mesh size is finer everywhere except for the electrode (cathode) boundary, which is extremely fine to enable small local topography changes during electrode growth. **b** 3D version of **a** with a z-axis axis of rotation at (0,0), where OB stands for open boundary. The mesh resolution from the top-down is coarse, fine and extra fine at the bulk electrolyte, VIA walls and cathode, respectively. **c** The same as **b**, but with a vertical cylindrical wall added on top of the VIA. This forces current crowding at the electrode center, which is demonstrated later in this section.

COMSOL Multiphysics simulations first require drawing a geometry, then inputting numbers and settings into a set of discrete physics modules, and then finally performing a study, which is typically either stationary (steady-state) or time-dependent. The following subsections discuss the latter two steps.

4.2.2.2. Physics module 1: Tertiary Current Distribution (TCD)

As previously mentioned, this physics module is compatible with the full Nernst-Planck equation for mass transport. It also supports the Butler-Volmer equation for electrochemical reaction kinetics. As such, the following discussion covers the relevant parameters for these equations as well as the boundary conditions for the corresponding study.

The supporting electrolyte setting was used, which is suitable for our electroplating setup, whereby the quasi-infinite electroactive species condition was enabled by a small bath loading factor (electroplating area to electrolyte volume ratio) along with excess anode material. This enables simplification of the redox process to a half-cell reaction comprising the Cu^{2+} reduction alone. The reduction of the Cu^{2+} ion consists of two steps, as shown in (4.3) and (4.4)[9,11,51,52].

$$Cu^{2+} + e^- \rightarrow Cu^+ \tag{4.3}$$

$$Cu^+ + e^- \rightarrow Cu \tag{4.4}$$

The first step (4.3) is the rate determining step, which is 1000 times slower than (4.4)[9,11]. Due to this, the kinetics can be further simplified by utilizing a one electron transfer process.

The Cu^{2+} ion diffusion coefficient in a copper sulfate electrolyte is provided in the literature[51,53] and was also calculated with the Warburg coefficient equation[54] to be 4.12x10^{-11} m^{2}s^{-1}. The manufacturer's specification sheet was used to calculate the Cu^{2+} ion concentration (944 molm^{-3}), which was set as the initial electrolyte concentration as well as the inlet and open boundary conditions. A no flux/insulation boundary condition was specified for all walls.

The electrolyte conductivity of several copper sulfate baths is provided in the literature[10,51,53,55]. The range is highly variable between 5-50 Sm^{-1}, implying this parameter is hugely dependent upon the unique composition of the electrochemical bath. To ensure accuracy for this parameter, cyclic voltammetry was utilized to generate impedance plots (Z' vs. Z'') for 12 test samples from which the average y-intercept was taken as the resistance metric (2.72 Ω), as shown in Fig. 4.5. Pouillet's law was then used to determine the resistivity, where $r = \rho l/A$ and r is the cell resistance in Ω, ρ is the resistivity Ω·m, l is the length in m and A is the cross-sectional area in m^2, which was then inverted to arrive at the electrolyte conductivity of 5.60 Sm^{-1} [56].

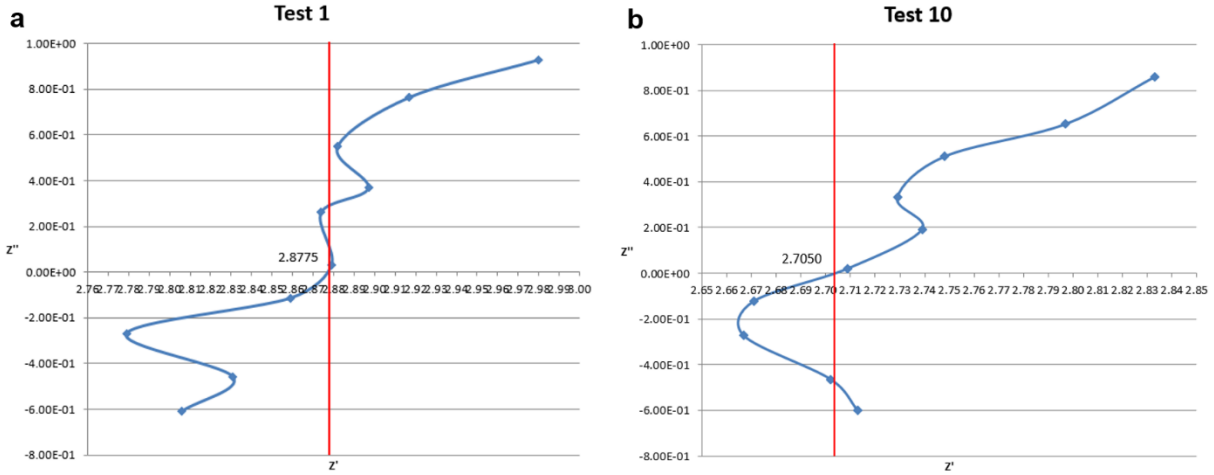

Figure 4.5. Example impedance plots for electrolyte resistance determination. a Test 1 of 12, where $Z'' = 0$ is the real part, as marked by the vertical red line. **b** Test 10 of 12.

The exchange current density and the cathodic transfer coefficients were taken from the literature, which are 0.5 Am^{-2} [11,55,57] and 0.5[11,53], respectively. The bulk electrolyte potential

was specified as 0 V vs. the electrode potential of -0.346 V, a common experimental value. STP was used for temperature and pressure settings and the fluid velocity was either 0 in all directions for diffusion controlled conditions, or derived from the Laminar Flow (LF) physics module in a multiphysics format, which is described in the next subsection.

4.2.2.3. Physics module 2: Laminar Flow (LF)

For fluid mechanics formulas, the reference fluid density was taken from copper sulfate pentahydrate (2286 kgm^{-3})[58] and the dynamic viscosity of deionized water (0.00089 Pa·s) was utilized due to the 70+% by volume concentration of DI in the electrolyte. While using these parameters along with the half-radial point rotation speed on a 0.1 m diameter Si substrate rotating at 1 rpm (0.0026 ms^{-1}), the Reynolds number is 672.4, which is significantly less than the turbulent region cut-off point[59]. Due to this, the LF physics module was chosen as a sufficient model. Incompressible flow was utilized and all parameters and studies were at STP.

In laminar flow, the flow profile cross-section of a Newtonian fluid through a pipe is a bell curve with zero velocity at the walls and maximum velocity at the center. To satisfy this constraint, a no slip condition was set for the boundaries of all walls, which corresponds to zero tangential movement of surface-adsorbed electrolyte molecules. The inlet speed was set to the previously mentioned half-radial point velocity, where only a single photoresist mold VIA was meshed and simulated to enable timely solution convergence. The no viscous stress condition was specified on open boundaries, which was complimented with a pressure point constraint of 101,325 Pa to ensure sufficient degrees of freedom in the constitutive flow equations.

To couple the TCD physics module to the LF module, the velocity field (spf) condition was specified in the TCD module under the electrolyte convection setting. This setup was sufficient to simulate both flow and current densities inside the mold VIA. To enable electrode growth simulations, an additional physics module had to be introduced and coupled into this arrangement, which is discussed in the next section.

4.2.2.4. Physics module 3: Deformed Geometry (DG)

The deformed geometry (DG) physics module enables specifying a normal mesh velocity on the cathode, and once coupled to the TCD physics module, it can use the local electrode current density as an input to simulate electrode growth. To enable this, the automatic from frame condition was specified under wall movement in the wall section of the LF physics module. Prescribed mesh displacement was specified as zero in all directions for the substrate and bulk electrolyte geometry boundaries. The vertical walls of the VIA mold were free to deform in the axial direction but not in the normal direction, which was set to zero, as corresponds to electrically insulating photoresist walls.

After setting up and successfully coupling the TCD, LF and DG physics modules, an electrode growth study could be configured. The main study type is time dependent, however due to the complexity of the triple multiphysics couple, initial values were established in two stationary (steady state) sub-studies comprising first a current distribution initialization step for the TCD module and second both the TCD and LF modules coupled together.

Once the initial values are established, the full time dependent electrode growth simulation can be performed. For this study to converge, it is critically important to enable automatic remeshing under the study extension section. This setting monitors the mesh quality as the electrode grows and automatically remeshes the geometry once the mesh quality drops below a user specified value (an example mesh quality expression is provided below). The mesh quality setting is specified under the study → solver configurations → time-dependent solver → automatic remeshing input node. A default mesh quality expression exists in COMSOL, which is a good reference point, however this equation often needs to be optimized to fit each simulation.

A poorly optimized remesh condition results in inverted mesh elements that quickly diverge and terminate the solver. Inverted mesh elements are the result of severe local topographical differences across the cathode that cause the discrete finite elements to not fit together correctly. Specifically, the constitutive equations that are solved on the boundary of the finite elements must not overlap. Typical equations for flow and electroplating simulations are quadratic along the boundary, which results in inverted mesh elements once the mesh becomes sufficiently compressed so that the constitutive equations begin to overlap. Once this happens, the continuity condition across adjacent boundaries is violated and the solver fails. Even with linear constitutive equations, inverted mesh elements still occur on badly deformed meshes.

Arriving at the correct mesh quality expression entails running a simulation on repeat and monitoring when and where it fails, and each time adding or subtracting from the previous mesh quality expression to eventually arrive at a suitable remesh condition. As an example, the optimized mesh quality expression for one of my 3D simulations is comp1.material.minqual-0.03 (the default minus 0.03). This method works best for 3D simulations, however for 2D, the following equation seems to work best, which is described in an example file in the COMSOL model library: min(comp1.material.minqual-0.2,min(comp1.material.minqual-0.4,min(comp1.material.minqual-0.4,min(comp1.material.minqual-0.4,min(comp1.material.minqual-0.4,min(comp1.material.minqual-0.4,comp1.material.minqual-0.4))))))).

In addition to optimizing the mesh quality expression, inverted mesh elements can be reduced by enabling moving boundary smoothing in the prescribed normal mesh velocity node of the DG module. As remeshing is performed, this setting decreases the gradient between adjacent finite elements to lessen their skew. The overall effect is a smoother and more gradual gradient across the growing electrode, which greatly assists in circumventing time consuming remeshing and aids in optimizing new meshes. The default smoothing value is 0.5, which I have reduced by an order of magnitude or more in some cases to increase the effect.

Up until now, advection simulations utilized a bulk flow component that entered through an inlet and exited through an outlet or an open boundary. This setup approximates the flow dynamics in a VIA placed on a rotating substrate, but in real experiments however, the flow is always changing directions. In the effort to enable this, a moving mesh physics module was introduced, which is discussed in the next subsection.

4.2.2.5. Physics module 4: Moving Mesh (MM)

In the previously discussed study setup, the TCD module is coupled to the LF module, which is then coupled to the DG module. With this subsection, the LF module is further coupled to the moving mesh (MM) module. I used the rotating domain option and specified a 1 rpm constant rotational velocity with a z-axis of rotation located -0.025 m (radius/2) from the mesh geometry. The experimental and simulation setup is depicted in Fig. 4.6.

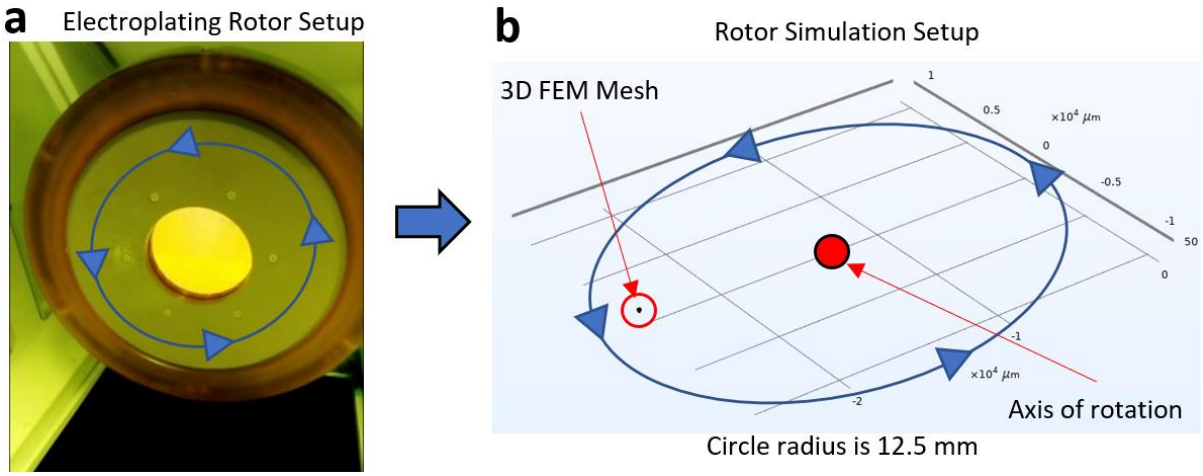

Figure 4.6. Lab and COMSOL rotor setup. **a** Picture of the Digital Matrix rotor. The sump is filled with copper sulfate electrolyte and the wafer holder is locked in place with an outward facing patterned Cu seeded Si substrate (the cathode). For reference, the exposed substrate diameter is around 90 mm. **b** COMSOL simulation setup for **a**. The full 3D geometry rotates around the axis of rotation at 1 rpm. In this example, the radial distance was set to radius/4, which somewhat increased convergence for troubleshooting purposes.

Following an extensive simulation effort and after discussing with the COMSOL Multiphysics support team, I discovered that this simulation setup is not currently feasible. Once optimized for timely convergence, this quadruple coupled simulation works well until the first automatic remesh, after which time the solver slowly diverges and terminates.

As shown above and with the MM module, the solver physically moves the geometry around the rotation axis point in simulation space. My best guess for why it fails to converge is that when remeshing occurs, the solver resets the geometry back to the start point, which creates discontinuities in the constitutive equations. I attempted to circumvent this by performing a series of studies that stored the solution and the mesh geometry in small time increments (e.g., 1 s). When each study inevitably failed, the last valid solution and the corresponding geometry/mesh were inputted as initial conditions into a successive study to circumvent divergence. After 6+ successive studies, this method eventually failed due to an extremely small time step (on the order of picoseconds), which made the problem virtually intractable. In the future, cluster or cloud computing or supercomputer rental could be used to further troubleshoot this simulation.

4.2.2.6. Consolidated simulation parameters

Table 4.1. Simulation parameters for physics modules 1-4.

Parameter	Value	Source
Participating electrons, stoichiometric coefficient, chemical species number (half-cell)	1	Refs. 9, 11, 51, 52
Cu^{2+} ion diffusion coefficient	4.12×10^{-11} m^2s^{-1}	Refs. 51, 53, 54
Bulk electrolyte Cu^{2+} ion concentration	944 $molm^{-3}$	Manufacturer data sheet
Electrolyte conductivity	5.60 Sm^{-1}	Lab measurements
Exchange current density	0.5 Am^{-2}	Refs. 11, 55, 57
Cathodic transfer coefficient	0.5	Refs. 11, 53
Bulk electrolyte potential	0 V	Experiments
Cathode potential	-0.346 V	Experiments
Electrolyte temperature and pressure	STP (293.15 K & 101,325 Pa)	Experiments
Electrolyte density	2286 kgm^{-3}	Ref. 58
Electrolyte dynamic viscosity	0.00089 Pa·s	Ref. 58
Bulk electrolyte flow rate	0 or 0.0026 ms^{-1}	Experiments
Substrate rotation rate	1 rpm	Experiments

4.2.3. Validating 3D simulations with experimental work

Successful 2D and 3D simulations were performed with the TCD, LF and DG physics modules. Consistency checks were enabled by comparing 2D and 3D simulations, which were then validated by comparing to experimental work, with highly positive correlation. The TCD and DG physics modules are coupled in subsection 4.2.3.1. and all three are coupled in subsection 4.2.3.2.

4.2.3.1. Diffusion and migration mass transport

With just the TCD and DG module, a diffusion controlled electroplating condition was established, as shown in Fig. 4.7.

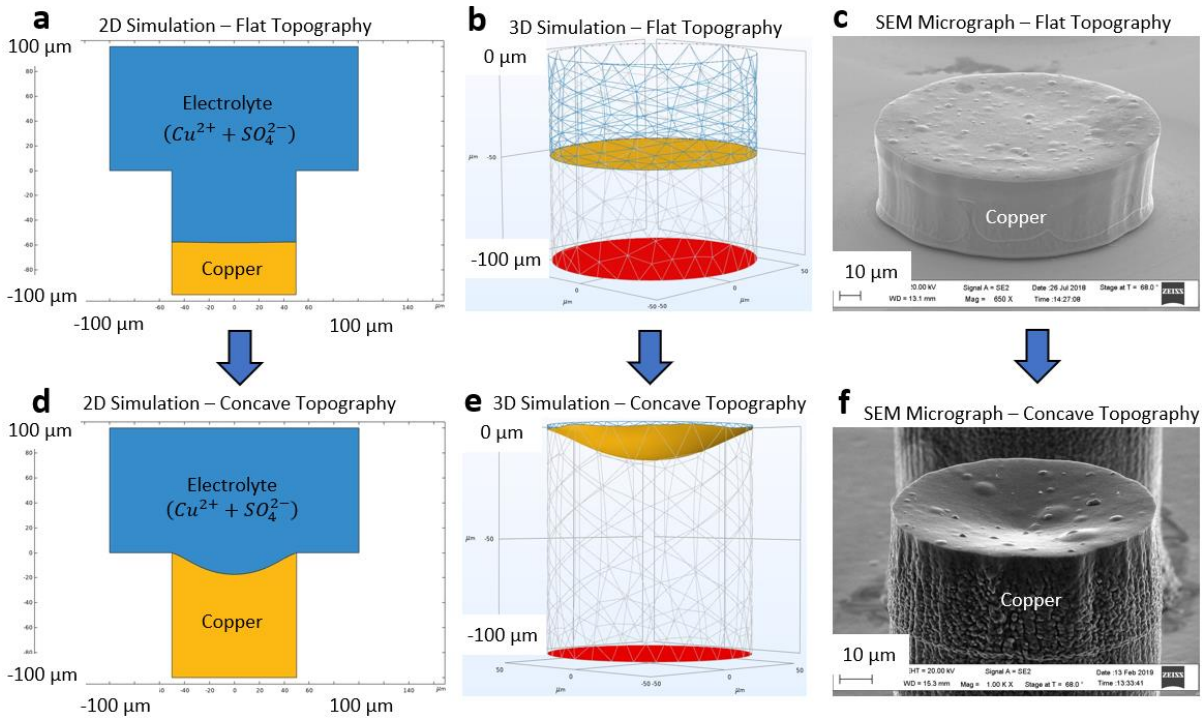

Figure 4.7. 2D and 3D simulations with corresponding experimental work for concave topographies. a 2D VIA mold cross-section with an AR of 1. The electroplated topography is virtually flat due to vertically oriented isotropic diffusion streamlines deep inside the mold cavity. **b** 3D version of **a**, where the red base is the electroplating start point, the grey mesh is electroplated Cu and the blue mesh is the copper sulfate electrolyte. **c** Experimental work displaying a flat topography, as predicted by the corresponding simulations **a** and **b**. **d** The same simulation as **a**, but at a later time stamp where the electroplated Cu has just reached the top of the mold cavity. The topography is notably concave due to both horizontally and vertically oriented diffusion streamlines causing current crowding at outer radial points, which results in an anisotropic diffusion streamline profile across the VIA mold. **e** 3D version of **d**. **f** Experimental work displaying a concave topography, as predicted by the corresponding simulations **d** and **e**.

In the effort to provide a fabrication processing option for convex electroplated topographies, a smaller columnar VIA mold was superimposed on top of the original, as shown in Fig. 4.8. This mold geometry could be fabricated by modulated exposure of a second thin film after exposing the bottom VIA mold pattern. A single or a dual development process could then be utilized, depending on developer selectivity.

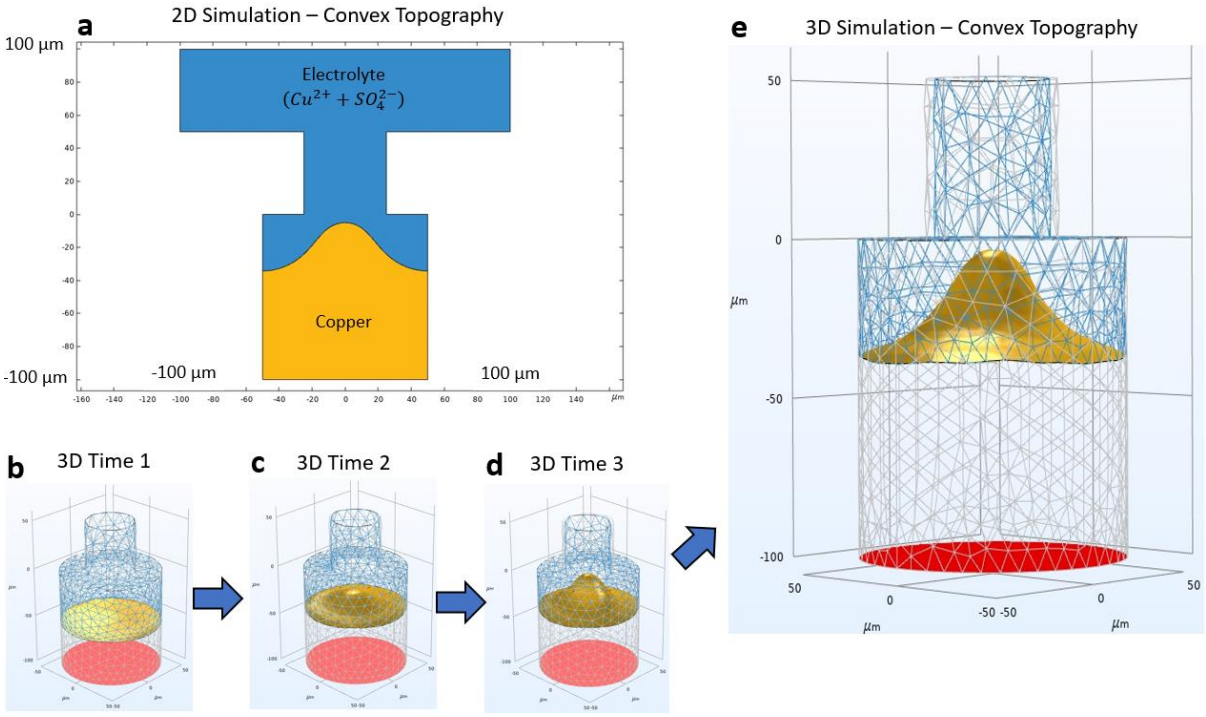

Figure 4.8. 2D and 3D simulations for convex topographies. a 2D VIA mold cross-section with a columnar VIA mold superimposed on top. The electroplated topography is highly convex due to current crowding at the superimposed VIA mold exit. **b** 3D version of **a** at an earlier time stamp, where the topography is virtually flat. **c** A subsequent time stamp from **b** displaying a moderately convex topography. **d** 3D version of **a** displaying a highly convex topography. This is the final time stamp just before the growing electrode enters the superimposed VIA mold. **e** Enlarged version of **d**.

From the above, I deduce that the diffusion controlled electroplating condition is a highly versatile fabrication processing option which can be utilized to form flat, concave or convex substrate-distal electroactive surface topographies.

4.2.3.2. Diffusion, migration and advection mass transport

Next, the TCD, LF and DG modules were coupled to simulate the full Nernst-Planck mass transport condition, as shown in Fig. 4.9.

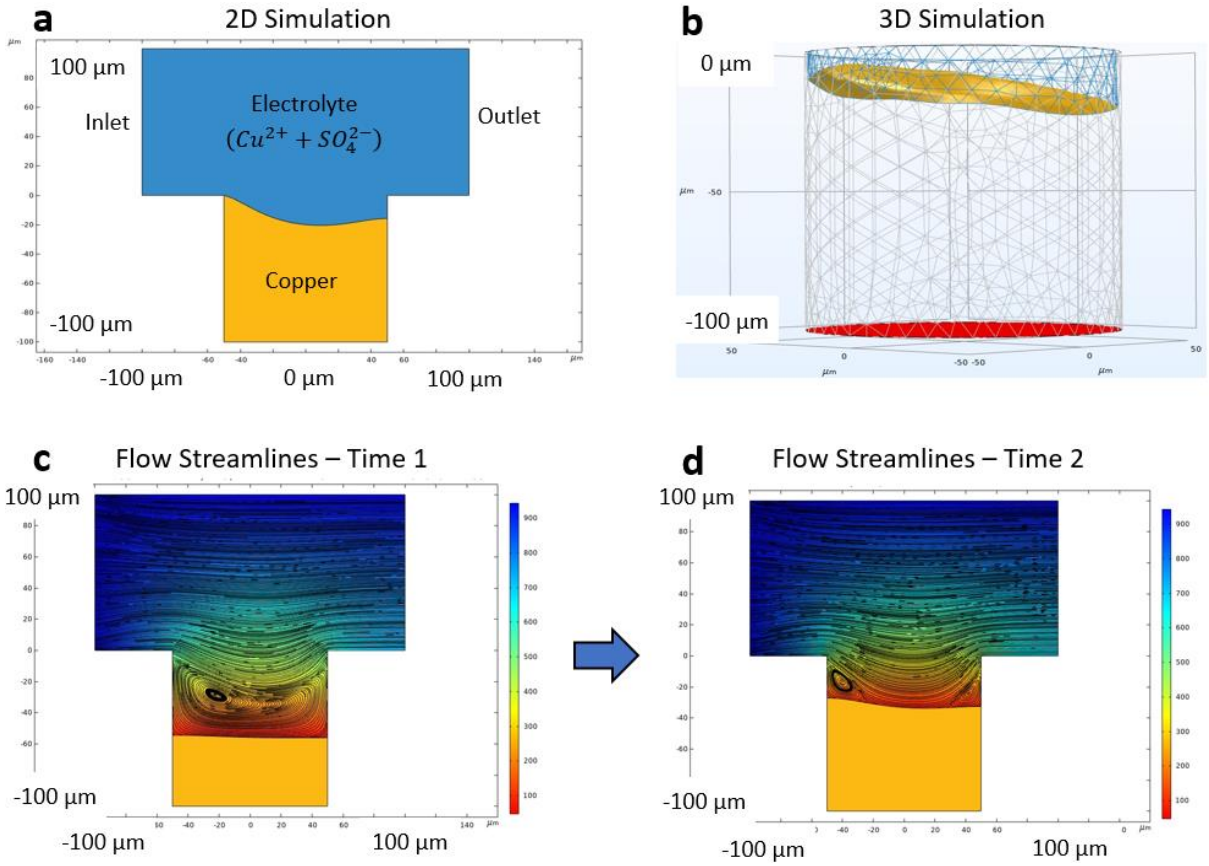

Figure 4.9. 2D and 3D simulations with advection. a 2D via mold cross section with an inlet on the left, an outlet on the right and an open boundary on top. When contrasted to Fig. 4.7d, it is evident that the laminar flow condition planarizes the electroplated Cu topography on the outlet-adjacent side. **b** 3D version of **a**. **c** Flow streamline analysis of **a**. An electrolyte dense eddy is depicted on the inlet-adjacent side of the mold cavity. The eddy constantly refreshes the electroactive Cu^{2+} ion concentration, which increases the localized plating rate. **d** A subsequent time stamp from **c**, whereby the eddy is significantly more localized at the inlet-adjacent side, which further increases the plating rate.

A first look at this figure suggests that laminar flow decreases the localized plating rate on the outlet-adjacent side. I investigated this counterintuitive result with a flow streamline analysis, wherein it became evident that laminar flow instead increases the plating rate on the inlet-adjacent side due to localized eddies that constantly refresh the solution. This mechanism works to create the illusion that the outlet-adjacent plating rate has decreased. This implies that the constantly changing advection condition of a rotor setup could be exploited to enable flat electroactive surface topographies at the top of the VIA mold, which is demonstrated with experimental work in the following section.

4.3. Experimental results

4.3.1. Cu VIA electroplated thickness progression

Through substrate via (TSV) thicknesses are typically less than 100 µm in 3D ICs[60] and range from 50-200 µm in 2.5D interposers[61]. To align with these metrics, my aim was to fabricate 100+ µm thick Cu pillars in the plating lab. Significant in-house lithography electroplating and

molding (LIGA) process development was required to enable this, the progression of which is shown in Fig. 4.10.

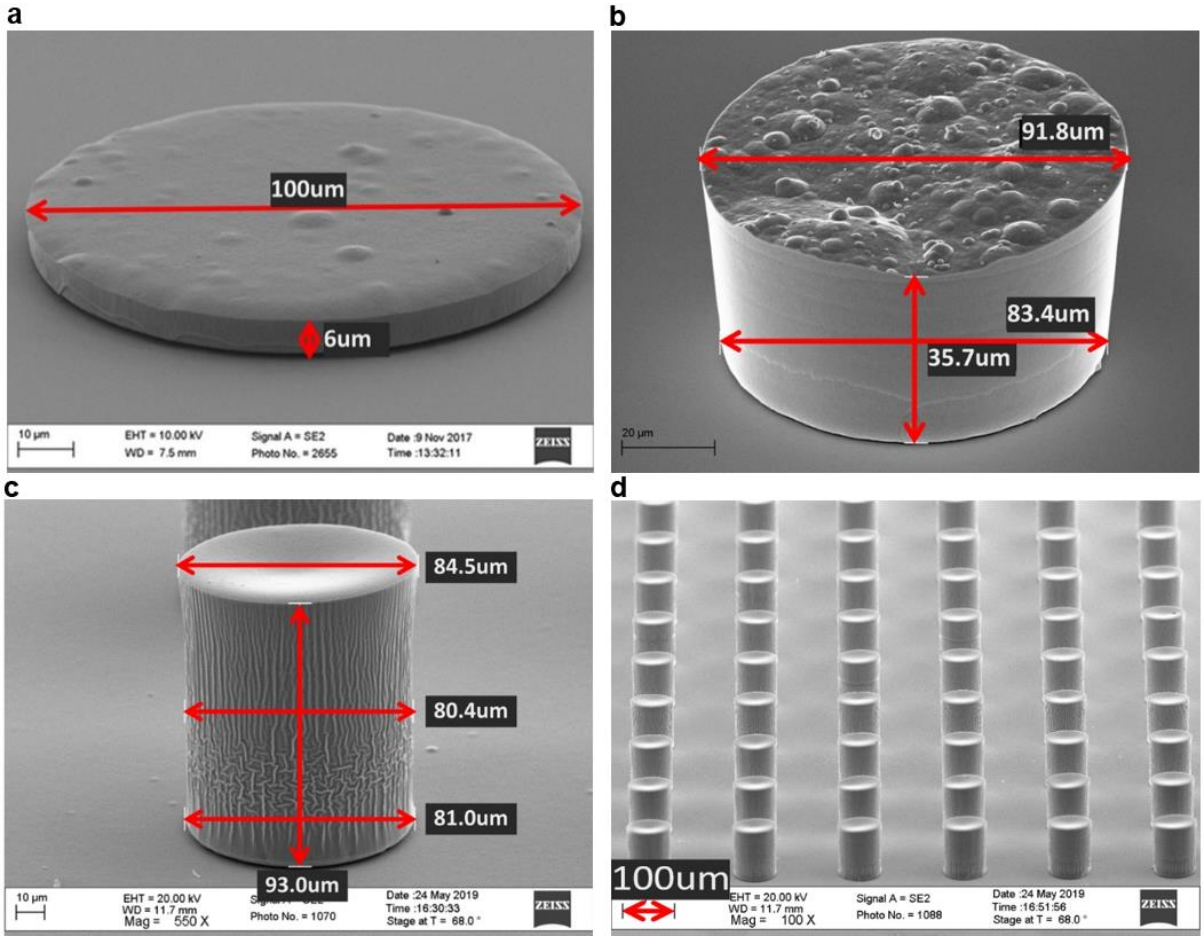

Figure 4.10. Cu VIA electroplating thickness progression. a 68º angled SEM micrograph of a 100x6 µm (diameter x thickness) electroplated Cu pillar. The actual pillar thickness is calculated as 6/sine(68º) = 6.45 µm. **b** 68º angled SEM micrograph of a 91.8(top)x35.7 µm electroplated Cu pillar with negatively sloped sidewalls. The actual pillar thickness is 38.4 µm. The circumferential ring around the pillar bottom was caused by removing the wafer from the electroplating bath for step height metrology and plating rate determination to enable controlled electrodeposition to the target thickness of 40 µm. **c** 68º angled SEM micrograph of an 84.5(top)x93.0 µm electroplated Cu pillar with nearly vertical sidewalls. The actual pillar thickness is 100.3 µm, which exactly aligns with the target thickness. **d** Lower magnification view of **c** showing a densely packed square array of Cu pillars with a 200 µm photomask design pitch. All processing was performed with THB-151N photoresist.

It is clear to see that significant advancements were made in the Cu pillar fabrication process. The Cu pillars from Fig. 4.10a were a first demonstrator that I had successfully carried out the full LIGA process in the plating lab. The aspect ratio (AR) of these pillars was however very low (0.0645).

I spun much thicker photoresist in Fig. 4.10b, which resulted in nearly 40 µm thick Cu pillars with an AR of 0.42 (top reference diameter) and 0.46 (bottom). These pillars were characterized by smooth negatively sloped wall profiles (from top to bottom) and a very rough surface topography. A single spin created the smooth sidewalls, where the photoresist was solely adhered to the substrate and was otherwise free to deform in the x-y directions. It is likely that during development, the molds stretched to relieve interfacial tension, which resulted in the negatively sloped gradient. Additionally, constant exposure to fresh developer solution could

have contributed to this effect by causing a slight over etching at the mold entrance. The rough topography was due to anisotropic diffusion streamlines caused by a high electroplating current density (>3 Adm^{-2}), whereby excess electroactive Cu^{2+} at discrete cathode surface locations enabled localized spherical plating growth inside the VIA mold. This mechanism corresponds to the x-y-z direction spherical plating growth dynamic that is characteristic of over-plated Cu VIAs protruding into the bulk electrolyte.

The ≈100 µm thick Cu pillar in Fig. 4.10c was the result of a double spin with an AR of 1.2 (top reference diameter) and 1.25 (bottom). This pillar exactly matches the target thickness (100 µm) and is characterized by a smooth and nearly flat substrate-distal topography and nearly vertical sidewalls with a medium circumferential roughness. A rotor at 1 rpm was utilized for this procedure along with a current density of 1.37 Adm^{-2}, where the reduced current density resulted in a smooth substrate-distal surface. This Cu pillar and the corresponding square array were plated to within ≈90% of the total photoresist film thickness. This bolsters the implication of the above simulation work by suggesting that a constantly changing advection condition can be exploited to produce flat substrate-distal topographies at electroplated thicknesses close to the total film thickness.

The circumferential roughness was likely the result of a complex sheer stress dynamic inside the photoresist due to the dual spin. This deposition entailed a sequence of spin layer one → soft bake → spin layer two → soft bake, which created two interfacial boundary regions inside the photoresist. The first interface was between layer one and the substrate and the second interface was between layer one and layer two, as depicted in Fig. 4.11.

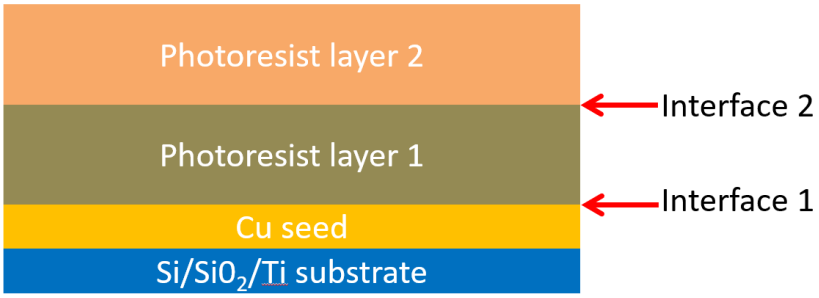

Figure 4.11. Internal interfaces inside a double-spun photoresist. First, layer 1 adheres to the Cu seed and second, layer 2 adheres to layer 1. Layer 1 is sandwiched between the Cu seed and layer 2, which causes sheer stress at both interfaces.

Stock THB-151N photoresist comprises 30-50% PGMEA solvent by volume, two-thirds of which evaporates during the soft bake[62]. Solvent evaporation causes the thin film to contract, creating significant internal stress. This is partially counterbalanced by an elevated soft bake temperature that increases solution mobility and encourages molecular alignment via Van der Waals forces, which also boosts adhesion. This counterbalancing effect is detrimental during the second soft bake however, due to molecules at interface 2 again aligning via localized Van der Waals forces that further induce random sheer stresses which proliferate throughout both photoresist layers. This mechanism predicts increased sheer stress in photoresist layer 1 when compared to layer 2, which corresponds to the observed circumferential roughness in Fig. 4.10c. Future work could further validate and troubleshoot this mechanism with the aim of reducing its effect (e.g., exploiting surface area dependent etch rates with ammonium persulfate), as the ideal Cu pillar has zero circumferential roughness to facilitate precise control over magnetic domain alignment in vertically oriented sputtered magnetic material.

4.3.2. Cu VIA electroplating technical challenges

The key challenge was to adapt pre-existing processing methods for Cu tracks into successful methods for Cu VIA fabrication. Several key difficulties arose during this process, which are briefly discussed in this section. As was demonstrated in Chapter 3, circular photomask occulters are highly prone to diffraction effects that significantly reduce photoresist mold resolution. Additionally, columnar mold latent image development difficulty increases proportionally to mold aspect ratio due to diffusion-dominant mass transport limitations, as was also discussed in Chapter 3. Limited advection in columnar molds also affects electroplating, which causes localized current crowding that results in a large surface roughness and/or pitting. Examples of Cu VIA electroplating technical challenges are presented in Fig. 4.12.

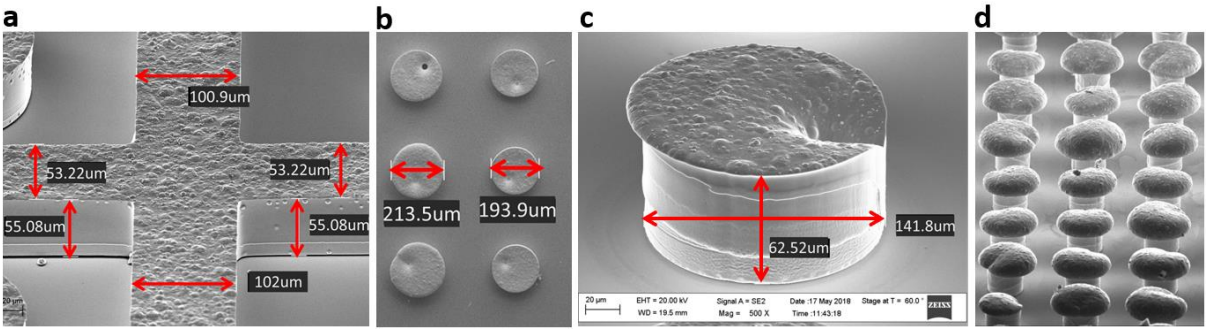

Figure 4.12. Cu VIA electroplating technical challenges. a Cu tracks fabricated with pre-existing in-house processing methods. Other than a medium surface roughness due to a high plating density, these tracks are pristine with an AR of ≈0.59. **b** 200 µm target diameter Cu pillars fabricated by the same pre-existing procedure and on the same exact wafer as **a**. The pillar diameter is highly variable. Pitting is clearly visible and a hole is present in the top left pillar. **c** 60º angled view of another pillar from the same wafer as **a** and **b**. A large pit is seen on the right-hand side. The AR is 0.53. **d** A separate wafer patterned with the same photomask as **a-c**, where the Cu pillar array has been significantly over-plated. As discussed in the previous section, electroplating occurs in all x-y-z directions once the electroactive surface protrudes into the bulk solution, causing "mushrooming".

The above problems with pitting and mushrooming were solved by hugely lowering the current ramp speed during electroplating (e.g., from 3 min to 60 or 120 min depending on the mold AR). In brief, this slow ramp speed permits diffusion streamlines to stabilize and become isotropic. This is discussed in more detail in Appendix IX, where the detailed standard operating procedures (SOPs) are presented for several photomasks comprising several different electroplating procedures.

4.4. Achievements and conclusions

2D and 3D electroplating simulations were completed in COMSOL Multiphysics, which were successfully validated against directly corresponding experimental work. This required setting up an experimentally isomorphic geometry with a custom FEM mesh that minimized the error margin with sufficiently small elements where appropriate, while also limiting the degrees of freedom for swift study convergence. Four physics modules were utilized in a multiphysics format comprising: 1) Tertiary Current Distribution (TCD), 2) Laminar Flow (LF), 3) Deformed Geometry (DG) and 4) Moving Mesh (MM). The parameters for the relevant constitutive equations in each of these four distinct physics modules were researched both in

the literature and in the laboratory. All of this was integrated into a highly optimized simulation package that extended from drawing a geometry through to custom equations for mesh element growth quality, which were essential for robust 2D and 3D electroplating simulations.

I have shown that diffusion and migration-controlled mass transport is sufficient for electroplating flat, convex and concave substrate-distal electrode topologies. Flat topologies have utility in flip chip applications and concave/convex surfaces are useful in sensors due to an increased surface area. In diffusion and migration mass transport conditions, a flat surface is only feasible when the mold cavity is plated to about half of the film thickness. Alternatively, the advection mass transport condition can be introduced via a rotor to enable flat electrode surfaces close to the full film thickness. As simple electroplating methodologies were proposed and explored, these findings enable tailored and scalable surface topography processing options, which can be readily integrated into pre-existing research and industry SOPs.

100+ µm Cu pillars that meet the thickness specifications of 2.5D interposers and 3D ICs were successfully patterned and electroplated. An electrode sidewall gradient analysis was performed and surface roughness mechanisms were investigated for the top surface and the circumference of columnar electrodes. Successful Cu pillar fabrication required significant process development to overcome technical challenges in nearly all aspects of lithography and electroplating including: 1) significant diffraction during photoresist exposure, 2) ineffective mass transport in diffusion controlled conditions during columnar mold development, and 3) anisotropic diffusion streamlines during electroplating causing pitting and over-plating. The fabrication effort culminated in a highly repeatable SOP to electroplate 81.0x100.3 µm (diameter x thickness) Cu pillar arrays with an AR of 1.25. This high-throughput, highly repeatable and cost-effective method for producing the fundamental VIA component of 2.5D interposers and 3D ICs has great potential for key applications in next generation micro- and nano-devices.

Click to skip to next chapter.

4.5. References

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Chapter 5 - Fabrication of Novel 3D Microinductors for Next Generation Integrated Magnetics

5.1. Target device

My goal was to fabricate vertically oriented magnetic core microinductors for power supply on chip (PwrSoC) applications. The target device comprised interconnected Cu pillars coated in magnetic material, as shown in Fig. 5.1.

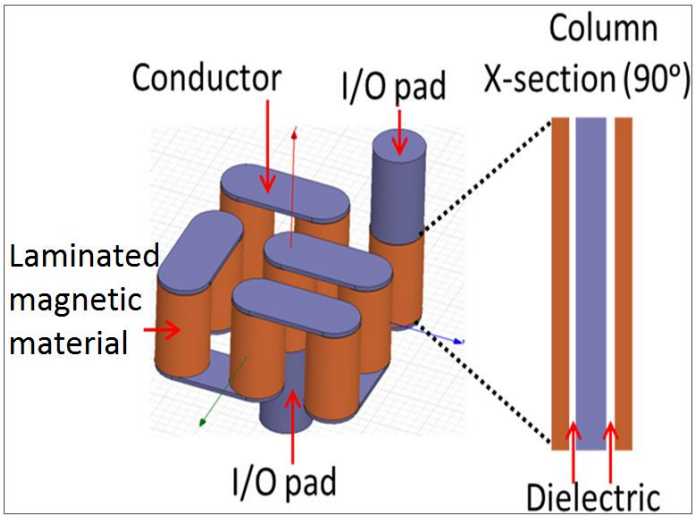

Figure 5.1. 3D schematic of the target microinductor device. Cu pillar arrays are monolithically integrated with alternating top and bottom interconnects to form a vertically meandering current pathway. Magnetic material coats the Cu pillars to increase the inductance density.

The aim was to produce a proof of concept device on silicon that demonstrates the key novelty of the SFI ADEPT project, vertically oriented Cu pillars surrounded in magnetic laminations. A detailed schematic is shown in Fig. 5.2.

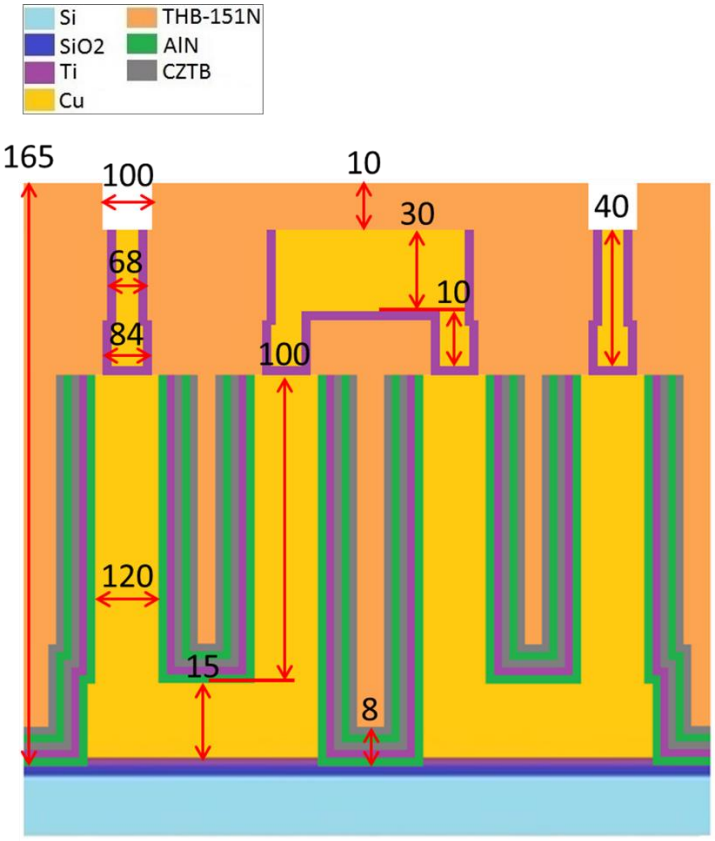

Figure 5.2. 2D x-z cross section of the target inductor device. Schematic not to scale and device dimensions in μm. A thermal oxide (silica) coats the silicon wafer to act as a diffusion barrier layer. Ti is used as an adhesion layer for both electroplated Cu and sputtered magnetic material. A low-κ dielectric, AlN, surrounds the Cu pillars to minimize anomalous losses and to prevent undesired short circuits while also isolating the magnetic material. CoZrTa is used as magnetic material due to its superior material properties: high resistivity, high magnetic saturation and low coercivity. The lamination thickness is less than the skin depth at our target frequency range (10-100 MHz) to minimize eddy current losses. Cu was utilized as the conductor due to its low electromigration characteristic, low resistivity and its compatibility with high-throughput electrodeposition techniques. THB-151N creates a patterned a solder mask and provides structural support with low-κ dielectric properties.

Only two magnetic laminations are shown in this schematic, but many more (32) were used in the actual device process flow. This enables a high inductance density due to the large self-inductance of Cu pillars coated in thick magnetic material. Furthermore, the concentric magnetic material minimizes EMI and enables significant freedom in design topology. Some excess magnetic material is also deposited horizontally on the bottom interconnect and the substrate during conformal physical vapor deposition (PVD or sputtering). This material is expected to contribute little to the overall inductance however, as large air gaps exist along the magnetic path. The unprecedented fabrication process flow for this novel device is detailed in the next section.

5.2. Process design

Traditional 2D fabrication methods were used as a springboard for novel 3D fabrication techniques. Specifically, a 90º rotation from a horizontally to a vertically oriented conduction pathway was required. The following figures detail the fabrication process flow. The standard

operating procedures and the photomasks used to accomplish these steps are detailed in proceeding sections.

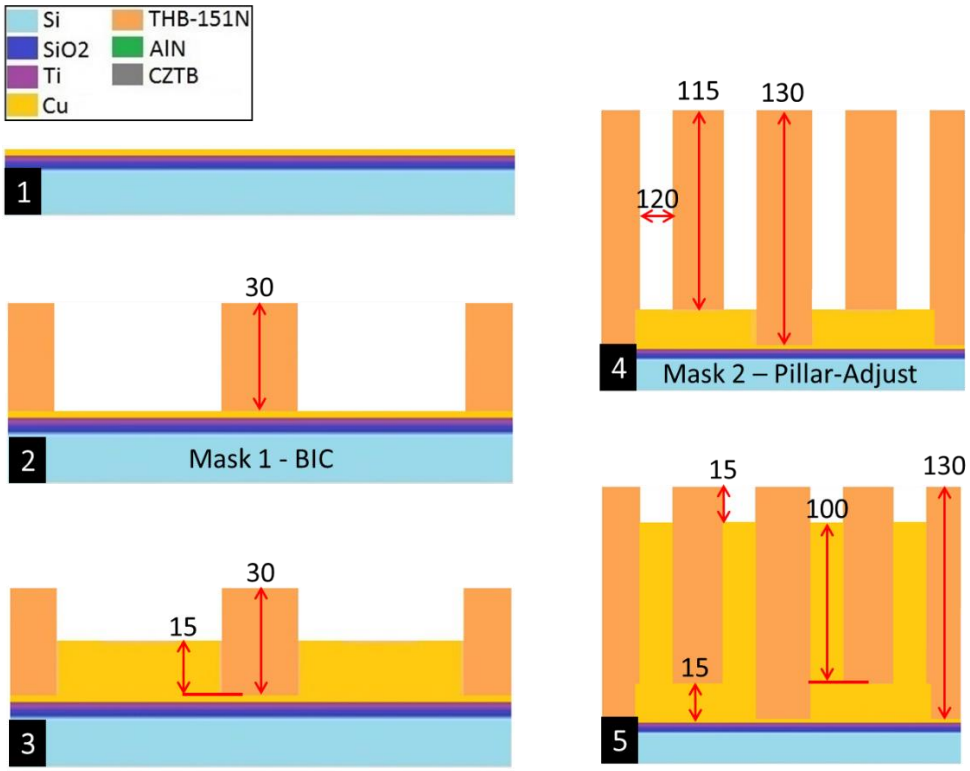

Figure 5.3. Steps 1-5 of the fabrication process flow. 1 A 250 nm thick thermal oxide is grown on a 100 mm diameter and 525 µm thick Si wafer, which is then sputtered with 20 nm Ti and 200 nm Cu. **2** 30 µm THB-151N is patterned using photomask 1. **3** 15 µm thick Cu is electroplated to form the bottom interconnect. **4** 115 µm THB-151N is patterned with mask 2 to create the Cu pillar molds. **5** 100 µm thick Cu pillars are electroplated.

The mold thickness is kept greater than the electroplating thickness to avoid over-plating and mushrooming, which would otherwise result in undesired short circuits and feature deformities. Optically transparent THB-151N permits reticle alignment between successive photomasks.

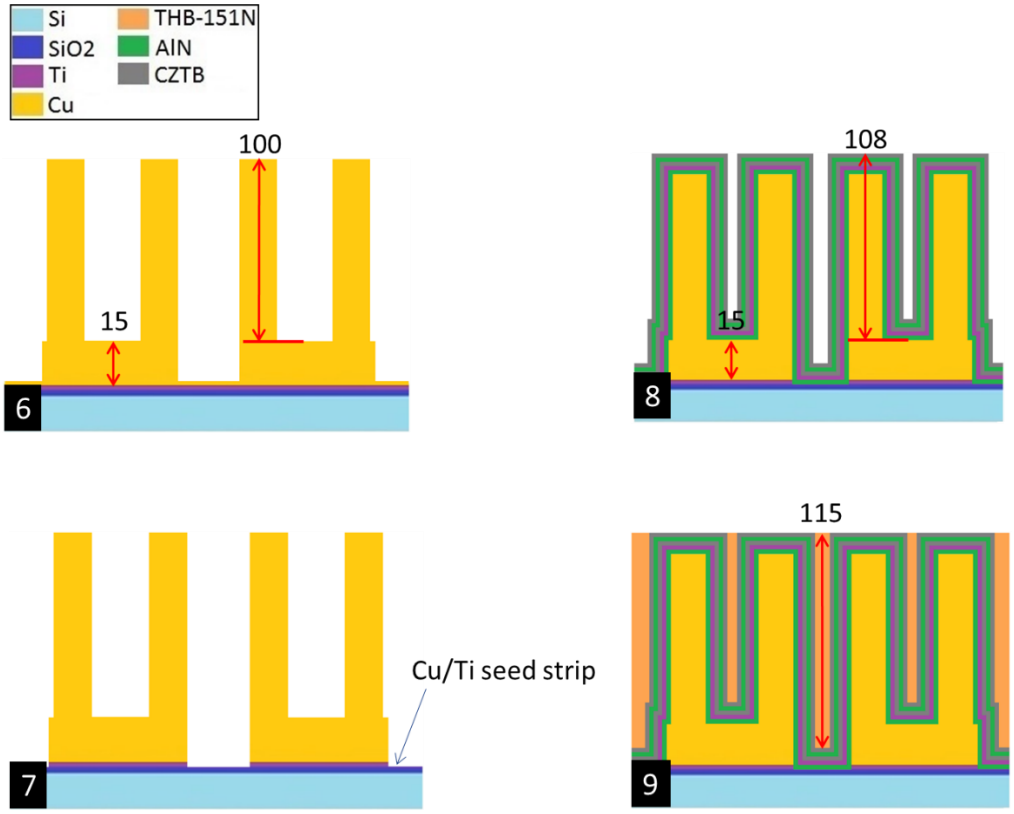

Figure 5.4. Steps 6-9 of the fabrication process flow. 6 THB-151N is stripped in THB-S17 solution. **7** The Cu/Ti seed is stripped in ammonium persulfate and buffered oxide etch (dilute HF), respectively. This eliminates undesired short circuits between adjacent bottom interconnects. **8** 32 laminations of 250 nm thick CoZrTa are sputtered to form an 8 µm thick horizontally oriented magnetic layer, whereby only 4 µm of magnetic material was deposited in the vertical direction due to the line-of-sight bias of PVD techniques. Additional sputtered material horizontal thicknesses: the first AlN layer is 50 nm thick, the Ti layer is 20 nm and successive layers of AlN are 20 nm thick. **9** A thick film of THB-151N is patterned to act as a structural support for a proceeding chemical mechanical polishing (CMP) step.

If desired, the device depicted in step 8 can be annealed in the presence of a vertically oriented magnetic field. This could create a beneficial magnetic anisotropy by tending to bias the magnetic domains in the vertical direction, orthogonal to the magnetic flux around the Cu pillars, which could reduce losses and increase the saturation current of the device.

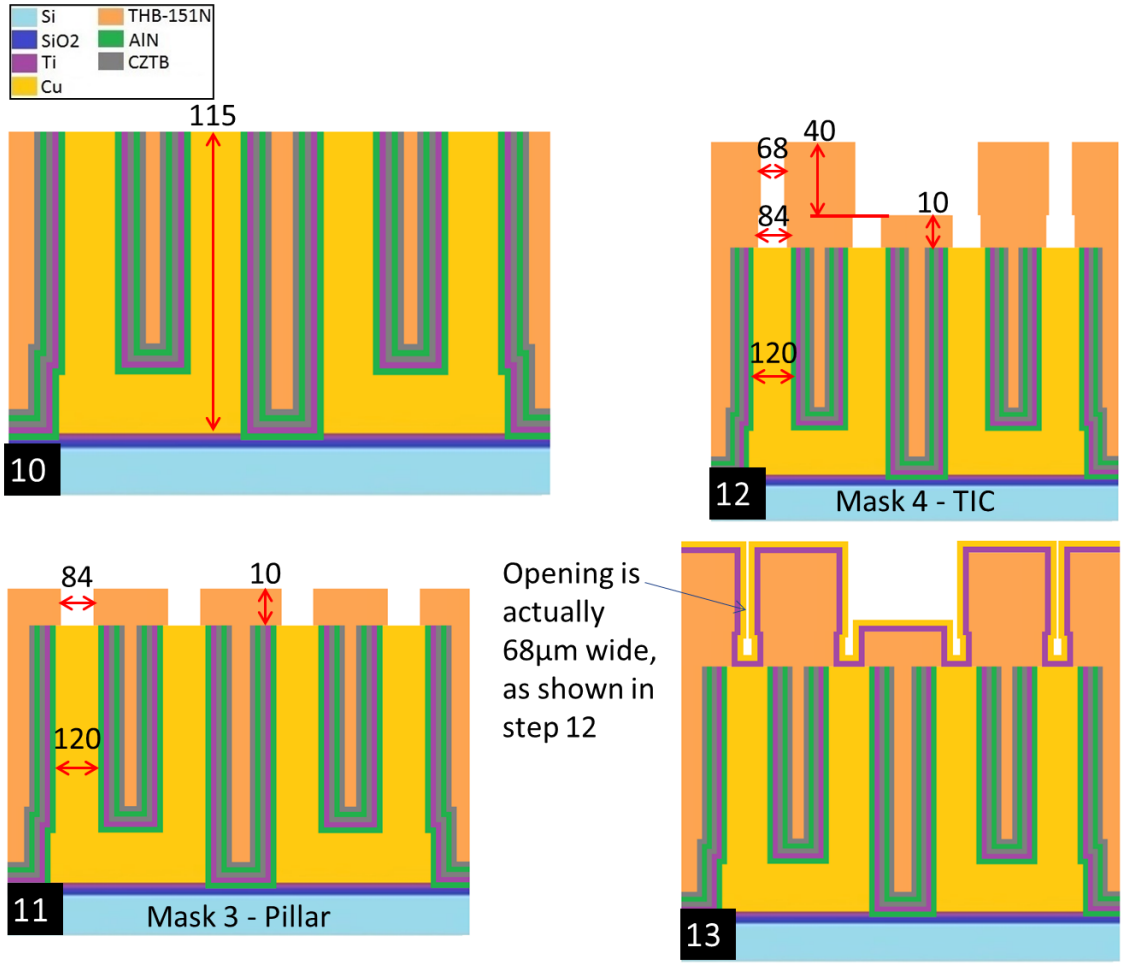

Figure 5.5. Steps 10-13 of the fabrication process flow. 10 A CMP is performed on the substrate distal Cu pillar surface, removing the undesired horizontally oriented magnetic material. This challenging step is described in a proceeding section. **11** A third photomask is used to passivate specific conduction sites (e.g., the magnetic material). **12** The electroplating mold for the top interconnect is created with a fourth photomask. **13** Ti/Cu adhesion/seed layers are sputtered with 50 nm and 400 nm thicknesses, respectively.

Traditional 2D processing utilizes a substrate adjacent Cu seed as a conduction pathway for electroplating, as depicted in step 3. In the case of the device depicted in step 13 however, the original Cu seed was etched and a new Cu seed was sputtered on top of the photoresist, distal to the substrate. It is critical that this new seed thickness is sufficient to create an unbroken current path along the 3D wafer topography, or the entire device may delaminate during electroplating. Therefore, the 0.5 vertical to horizontal sputtering thickness aspect ratio was accounted for by doubling the traditional sputtering thickness of the Ti/Cu layers. Additionally, a slow current ramp speed was used to circumvent undue stress along the topographically complex conduction path.

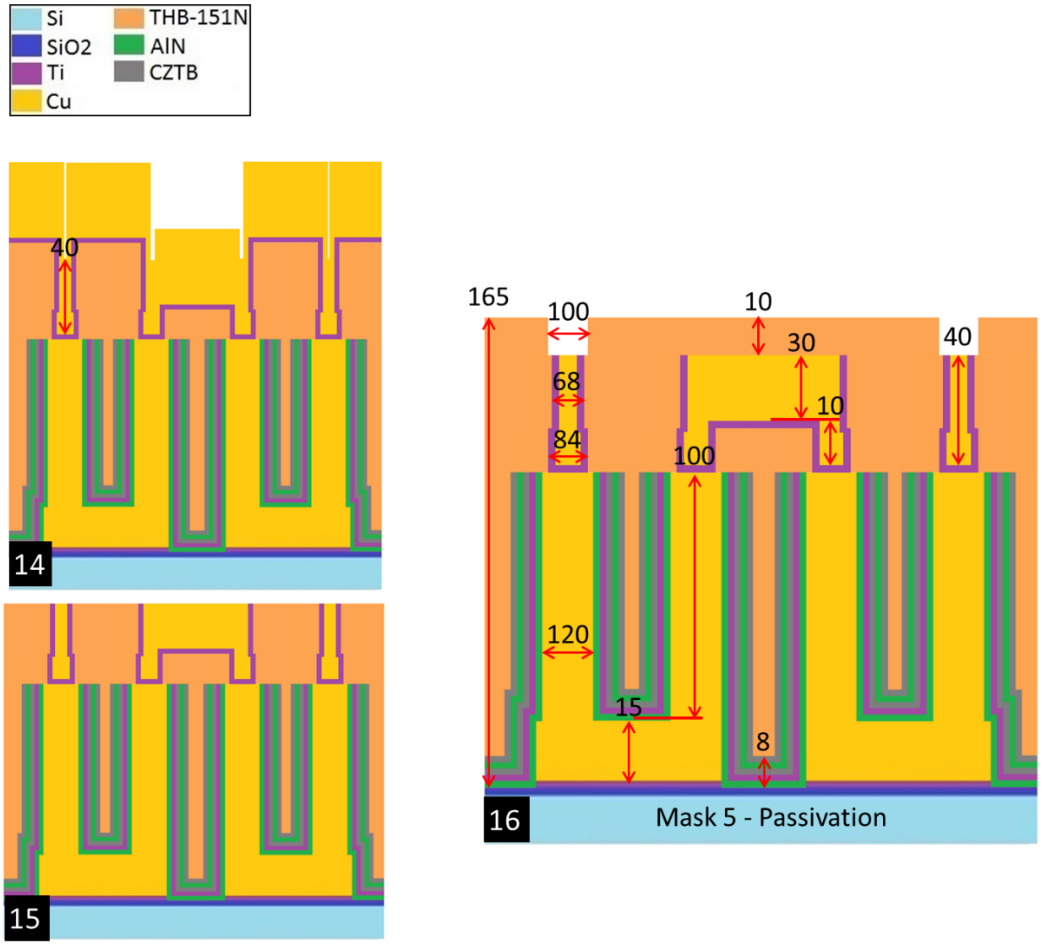

Figure 5.6. Steps 14-16 of the fabrication process flow. 14 The top interconnect is electroplated. High aspect ratio cavities fill in due to nucleation sites proliferating in the x and y directions, creating a blanket of electroplated Cu on top of the device. **15** A second CMP is performed to remove excess Cu and eliminate undesired short circuits. **16** The final photomask, mask 5, is utilized to create a solder ball mold.

In the preceding schematics, the cross section decreases when transitioning to successive vertically oriented electroplated layers (e.g., step 4 ➡ 11 ➡ 12). This "wedding cake" design compensates for mask alignment errors and ensures that successive alignments are on target. From experiments, I found that due to edge broadening, a 120 µm diameter photomask occulter produced a ≈110 µm diameter THB-151N photoresist mold with a thickness of 100 µm. To eliminate any potential processing issues, this 10 µm error was further increased to 20 µm, which resulted in a Cu pillar design diameter of 100 µm. An 8 µm error was allotted in every direction for successive alignments, hence the reduction from 100 µm ➡ 84 µm ➡ 68 µm in steps 4-12. This explains the thickness increase from the bottom interconnect to the top interconnect, whereby the top interconnect is doubled in thickness to compensate for a reduction in width by half (rectangular interconnects). The solder mask diameter was increased back to 100 µm in step 16 to enable easy fitting of 80 µm diameter solder balls for flip chip applications.

5.3. KLayout photomask designs

5.3.1. Plating density normalization

A key target outcome of device fabrication was to determine the inductance (nH) per magnetically enhanced Cu pillar. This value could easily be reduced to inductance per unit length (μm), which would not only enable us to validate our simulation work, but would also open up the design space for tailoring the inductance density of the microinductor device.

To enable this, our ADEPT die comprised 10 different devices with five different pitches. Varying the pitch while holding the Cu pillar dimensions constant permits determination of the Cu interconnect contribution to both inductance and DC/AC resistance. The interconnect contribution is then subtracted from the total quantitative measurement to yield data for just the magnetically enhanced Cu pillars.

The pitch between two adjacent interconnected Cu pillars is 2r + S, where r is the pillar radius and S is the spacing. We chose pitch dimensions of 200, 400, 600, 800 and 1000 μm to force a linear variance between devices. Furthermore, the number of pillars was varied at each pitch to enable fitting a trendline to multiple data points. The design permitted six measurements with GSGSG sensing points at each pitch (G=ground and S=source) for 20, 28, 36, 42, 54 and 66 Cu pillars in series. Due to the large number of Cu pillars per device, the device footprint area was minimized by utilizing both 9x4 and 11x6 (row by column) array topologies. Therefore, we utilized two unique devices at each pitch, the first comprising a 9x4 array with sensing points for 20, 28 and 36 Cu pillars in series, and the second comprising an 11x6 array with sensing points for 42, 54 and 66 Cu pillars in series.

The result was a huge variability in the conductor density across the ADEPT die. Since a large electroactive cross-section electroplates significantly slower than a small electroactive cross-section, it follows that a large density of Cu pillars electroplates significantly slower than a small density of Cu pillars. It was critically important to overcome this design issue, as several of our key process constraints required a tight control over the electroplated thickness across the entire ADEPT die. Notable process constraints included photoresist film thickness control, a highly variable CMP rate between CoZrTa and Cu and the inelasticity of the GSGSG sensing probes.

To overcome this critical design issue, I normalized the electroplating density across the entire ADEPT die by dividing the most densely packed microinductor device into fundamental unit cells. This created an electroplating density reference point that was calculated as the unitless ratio of electrically active to electrically inactive surface area inside the fundamental unit cells. This normalization ratio was maintained throughout the remainder of the devices by adding “dummy” electroactive surfaces inside otherwise less densely packed unit cells. The process is depicted in Fig. 5.7.

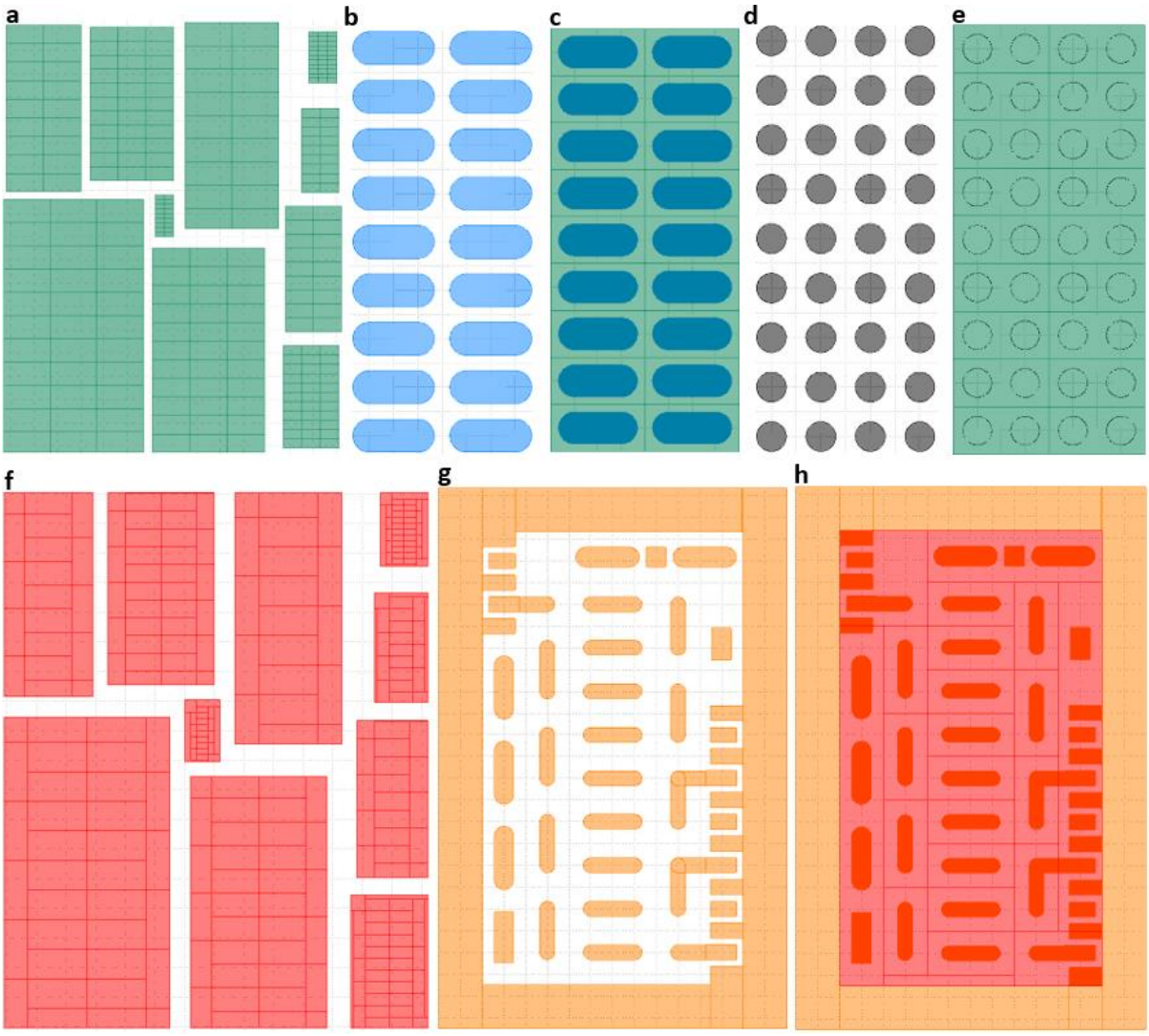

Figure 5.7. Current density normalization scheme for controlling the electroplated thickness across the entire ADEPT die. a The full ADEPT die showing the unit cell layout for all ten unique devices (devices not shown). This was used for the first two electroplating steps. The reference unit cells are located in the center of the die. **b** Magnified view of the reference device showing the bottom interconnect photomask design. This is the first electroplating step. **c** Fundamental unit cells superimposed over **b**, from which the electroplating density reference ratio was calculated for the bottom interconnect photomask. **d** Magnified view of the reference device showing the Cu pillar photomask design. This is the second electroplating step. **e** Fundamental unit cells superimposed over **d**, from which the electroplating density reference ratio was calculated for the Cu pillar photomask. **f** The full ADEPT die showing the unit cell layout for the final electroplating step. **g** Magnified view of the reference device showing the top interconnect photomask design. **h** Fundamental unit cells superimposed over **g**, from which the electroplating density reference ratio was calculated for the top interconnect photomask.

5.3.2. Mask 1

The fabrication process utilized a total of five photomasks. Since THB-151N is a negative photoresist, all of these masks are bright field, whereby the depicted design features demarcate the actual target mold topology.

In addition to the ten unique ADEPT devices, I integrated four additional devices into these photomasks by using the topology specifications from a partner group. These additional devices are henceforth called the power management integrated circuit (PMIC) devices. The PMIC die was arranged in a columnar format on either side of the ADEPT die, which is omitted in the following figures for simplicity, but nonetheless is showcased at the end of section 5.3. The first mask is shown in Fig. 5.8.

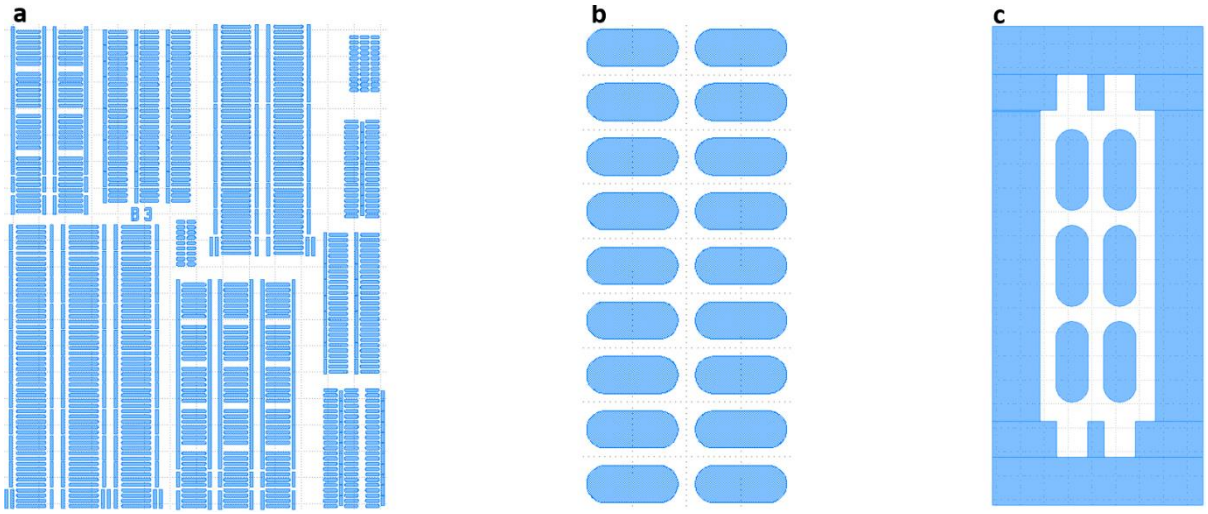

Figure 5.8. The bottom interconnect photomask. a A full ADEPT die with unique identifier B3. These molds are electroplated to form the bottom interconnect, which corresponds to steps 2-3 of the process schematic. **b** Magnified view of the central device. **c** Magnified view of an example PMIC device. An electroplating frame was included in this design to compensate for a low plating density caused by device spacing requirements.

5.3.3. Mask 2

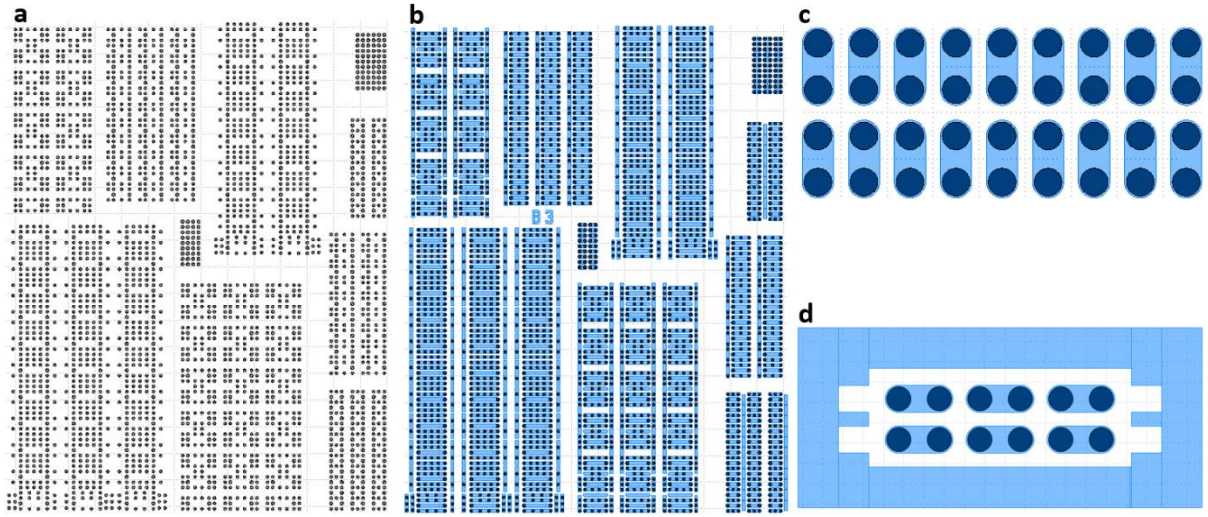

Figure 5.9. The Cu pillar photomask. a The full ADEPT die for mask 2. These molds are electroplated to form the Cu pillars, which corresponds to steps 4-5 of the process schematic. **b** The full ADEPT die showing the two-tiered photomask stack. **c** Magnified view of the two-tiered central device. **d** Magnified view of the two-tiered example PMIC device.

5.3.4. Mask 3

Normalizing the electroplating density for mask 2 required adding a significant number of dummy Cu pillars, which were next passivated with mask 3. Specifically, the aim of this mask was to bury the excess Cu pillars in photoresist while leaving the substrate distal surface of the current-carrying Cu pillars exposed for further processing.

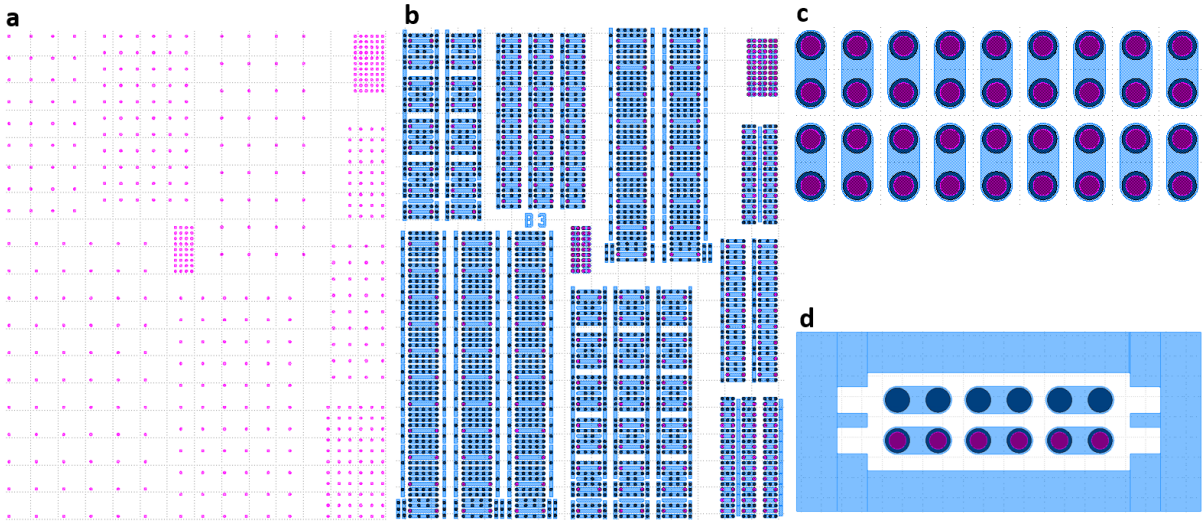

Figure 5.10 The Cu pillar selective activation photomask. a The full ADEPT die for mask 3. This corresponds to step 11 of the process schematic. **b** The full ADEPT die showing the three-tiered photomask stack. **c** Magnified view of the three-tiered central device. As this is the reference device, all pillar tops remain exposed. **d** Magnified view of the three-tiered example PMIC device. The four top-most pillars are electrically inactive.

5.3.5. Mask 4

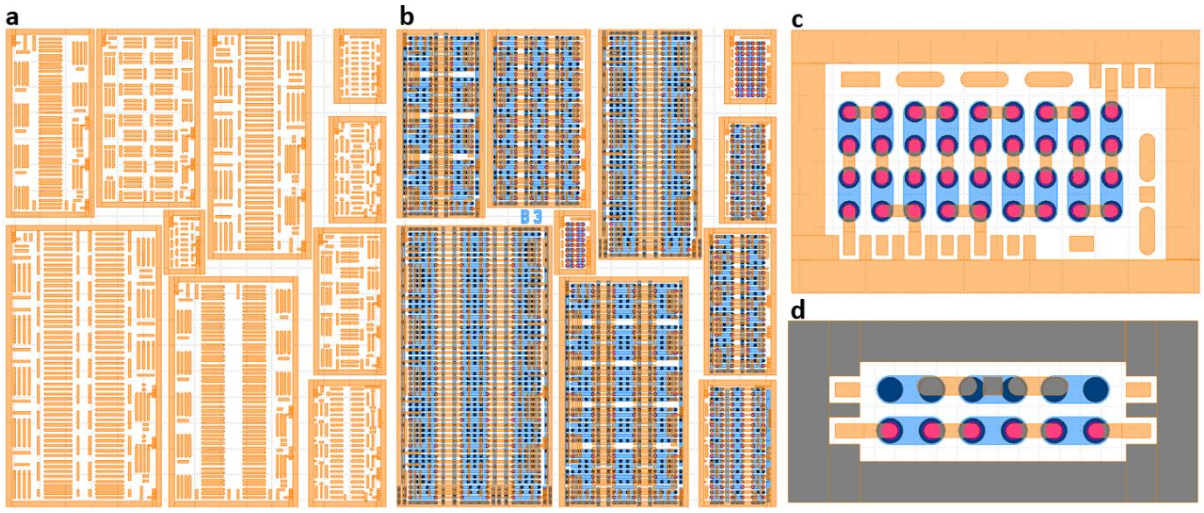

Figure 5.11. The top interconnect photomask. a The full ADEPT die for mask 4. These molds are electroplated to form the top interconnect, which corresponds to steps 12-14 of the process schematic. **b** The full ADEPT die showing the four-tiered photomask stack. **c** Magnified view of the four-tiered central device. **d** Magnified view of the four-tiered example PMIC device.

5.3.6. Mask 5

The aim of the final photomask was to passivate the entire wafer with a continuous blanket of photoresist while leaving selective spots open for solder ball molds and GSGSG test probes. This mask also adds a unique identifier to every ADEPT device in the format of: rows x columns – pillar pitch (µm).

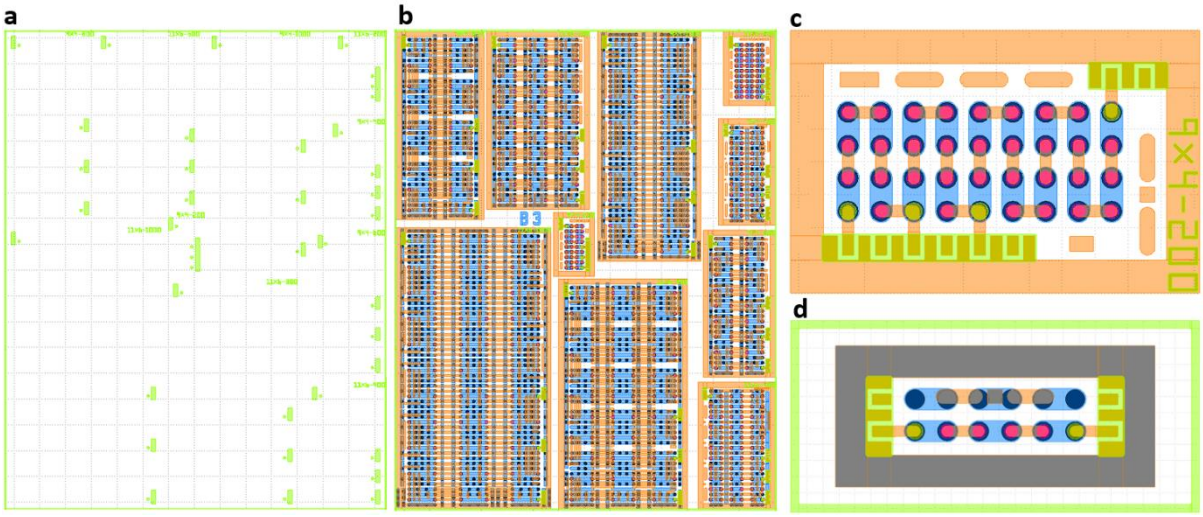

Figure 5.12. The GSGSG probe point and solder ball mold photomask. a The full ADEPT die for mask 5, where the border marks a dicing lane. This corresponds to step 16 of the process schematic. **b** The full ADEPT die showing the five-tiered photomask stack. **c** Magnified view of the five-tiered central device. The GSGSG probe points and solder ball molds are green. **d** Magnified view of the five-tiered example PMIC device with a dicing lane marker.

5.3.7. Full wafer layout

The full wafer photomask design comprised the ADEPT and PMIC dies arranged in rows and columns to enable easy die partitioning with continuous full-wafer dicing lanes (lane width=100 µm). Every photomask included profilometer reference points at all N, W, S, E and central wafer locations along with W and E alignment reticles. Test sample areas were also included at all wafer locations to enable easy determination of the sputtered CoZrTa material properties with a standard Helmholtz coil (aka B-H looper). Finally, a 7 mm wide plating ring was included to enable EBR and to ensure electrical contact with the wafer holder.

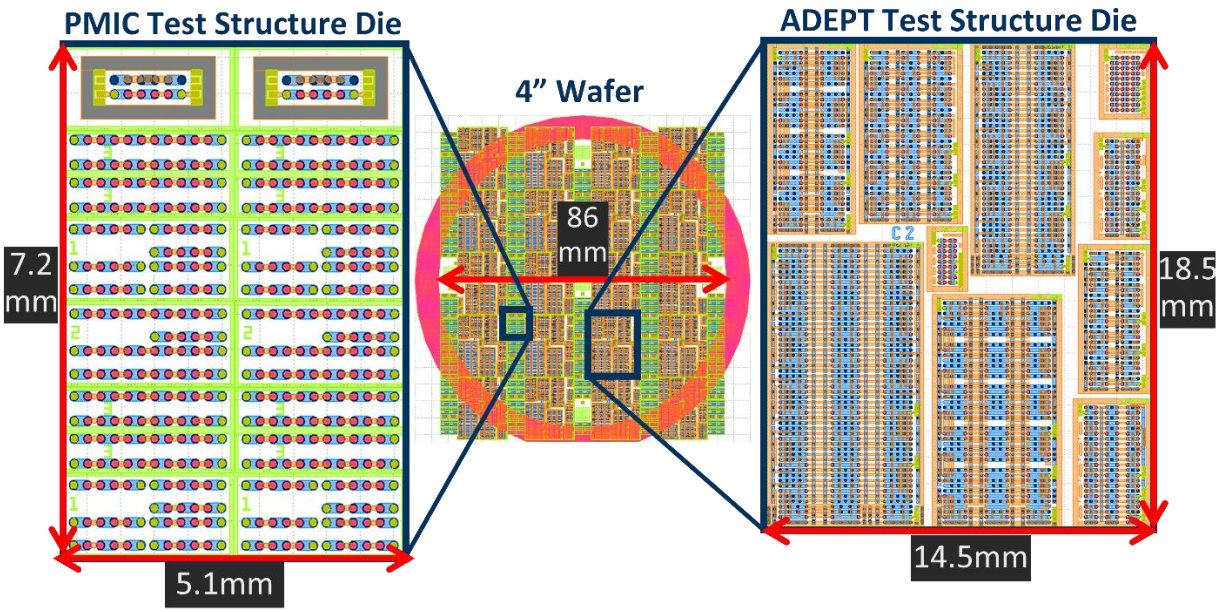

Figure 5.13. Full wafer layout of the five-tiered photomask stack. From left to right: the PMIC die (left), the full 4” (100 mm) wafer layout (middle) and the ADEPT die (right). From the bottom-up, the PMIC die is arranged in a repeating sequence of the unique devices: 1, 3, 3, 2, 1, 3, 3, 4, where 4 is the example device featured throughout this section. This arrangement was chosen according to device demand and dicing lane location.

5.4. Standard operating procedures

I created, provided, explained and demonstrated all SOPs to our processing support team prior to commencement of any device fabrication work. All processing was performed in the plating lab except for steps 1 (Cu seed preparation), 8 (CoZrTa sputtering) and both 10 and 15 (the CMP steps). Step 8 strictly required a CMOS compatible wafer that was not contaminated with additional trace metals such as: Ni, Fe, Ag, Au, etc. This was due to the location of the sputtering tool, which was in the cleanroom class 10,000 (ISO 7) MEMS fabrication lab. A significant effort was undertaken to enable this, as the plating lab is not traditionally CMOS compatible. A detailed description of this process is provided in Appendix VI. In short, processing steps 2-7 were performed in a new CMOS compatible fume hood that included dedicated glassware, hot plates and a photoresist spinner. A dedicated mask aligner chuck was also used and all electrical plugs were kept under lock and key. For the remainder of the steps after step 9, standard non-CMOS processing was performed, as the CMP machine (step 10) was a non-CMOS compatible tool.

Detailed SOPs for photomasks 1-5 are provided and discussed in Appendix IX.

5.5. Chemical mechanical polishing

CMP comprises a corrosive slurry that is dispensed at a specified flow rate onto the rough surface of a rotating polishing pad. The back of the wafer is adhered to a separately rotating carrier head, which presses the wafer face-down onto the polishing pad below. This results in CMP. Our setup utilized a peristaltic pump and a plastic tube to enable compatibility with acidic slurries. An image of our setup is provided in Fig. 5.14.

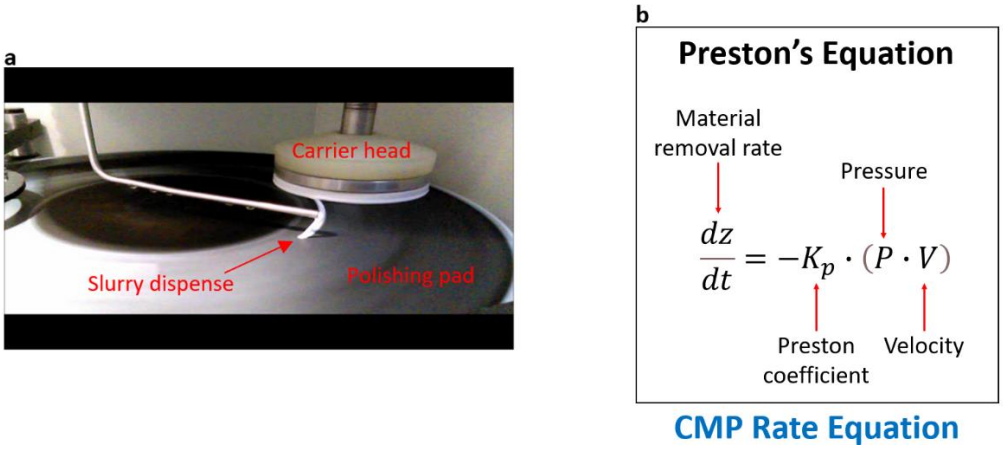

Figure 5.14. CMP setup and rate equation. a The white slurry is Ultra-Sol 200A from Eminess which consists of aqueous 0.1 µm alumina particles at a solids content of 20 g/L with a pH of 4. We used a Suba 1200 polishing pad, also from Eminess, which had a felt base with a hardness of 80 Pa. Example process parameters for CoZrTa: pad/carrier at 120 rpm, carrier pressure 5 psi and slurry flow rate at 220 mL/min. **b** The standard CMP rate equation. The polishing rate is directly proportional to the carrier head pressure and the pad/carrier rpms. In common practice, the carrier head is set to the same rotation speed as the polishing pad, which is sufficient for mechanical polishing due a differential in the axis of rotation.

CMP was performed by the Silicon/E-Beam Process and Product Development group. Several challenges were experienced during the CMP, which proved to be by far the riskiest fabrication process step. Two of four device wafers broke during the first CMP alone, as corresponds to process schematic steps 9-10, wherein the planar CoZrTa is removed from the top of the Cu pillars. This was due to a poor adhesion between the back of the wafers and the carrier head, which caused the wafers to dislodge onto the quickly spinning polishing pad during carrier head to polishing pad contact and separation. Several things were done to troubleshoot this: 1) the carrier head wafer backing pad was cut perfectly to size, 2) both the backing pad and the back of the wafer were wetted prior to press on contact, which increased adhesion, and 3) the polishing pad and the carrier head were only contacted and separated at 0 rpms and only gradual changes in rpms were permitted.

Of the two wafers that made it through the first CMP, one was significantly over-polished. This was due to a highly variable polishing rate between CoZrTa and Cu, which was exacerbated by a small differential in the electroplated Cu pillar thickness from r=0 to r=50 mm (±5 µm) caused by current crowding at the wafer holder boundary. Due to this, and during CMP, substrate-distal Cu was exposed in the form of concentric rings that proceeded chronologically from the outer radius inward, resulting in a radially decreasing pillar height gradient. Our final wafer was successfully polished by performing metrology and characterization at regular intervals (180 s), with off-center wafer reference points.

During the 2nd and final CMP, as corresponds to process schematic steps 14-15, one of the wafers broke in half due to a process engineer operating error and the other dislodged from the carrier head, as was previously described. It is unknown whether the previously mentioned adhesion troubleshooting methods were utilized for this wafer or not, however if CMP was to be repeated in a future fab, a good solution would be to use double sided dicing tape to eliminate this problem.

Following this, the broken wafers were etched in ammonium persulfate (a Cu etchant) to remove the over-plated Cu blanket covering the top interconnect, as shown in process

schematic steps 14-15. This successfully liberated the microinductor devices for imaging and testing. As an alternative Cu blanket etching method, mechanical polishing with sandpaper was also trialed[1], wherein the grit ranged from very fine to ultra fine (P240-P2000+) on the Federation of European Producers of Abrasives (FEPA) rating scale. A very fine grit was initially used to enable quick polishing of the thick blanket Cu, which was then followed by increasingly finer grit sizes. Fig. 5.15 describes some of the CMP successes and challenges.

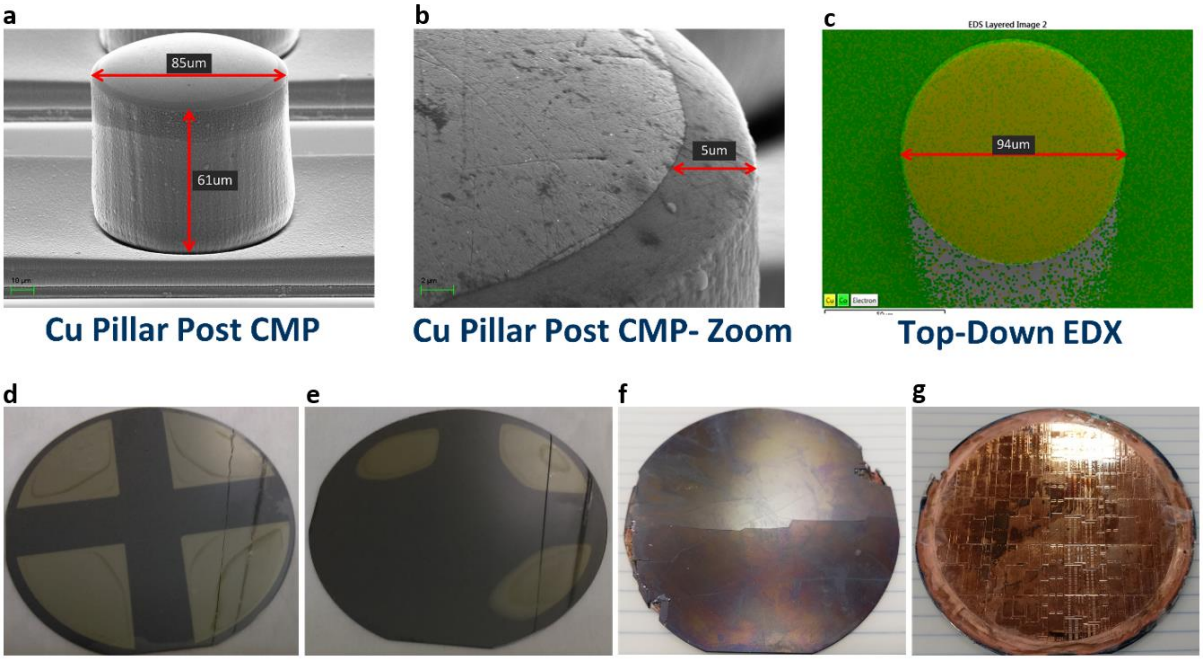

Figure 5.15. CMP results. a A Cu pillar after the 1st CMP with the bottom interconnect shown. The pillar top is dome shaped due to a proportionality between the slurry flow rate and Cu pillar radial points. **b** Magnified view of **a** showing the interface between Cu and the magnetic material. **c** Top-down energy dispersive X-ray (EDX) of a Cu pillar after the 1st CMP. Elemental analysis shows that the planar magnetic material was successfully removed from the top of the Cu pillar, where yellow is Cu and green is Co. The gray area at the bottom of the image is a result of a line-of-sight analysis with an angled beam. **d** CoZrTa sputtered test wafer with Si substrate level reference strips to enable step height measurements for CMP etch rate determination. **e** Uneven polish rates across the wafer are a result of slurry crowding at the linear and "cliff-like" CoZrTa boundary. **f** Backside of the broken wafer from the 2nd CMP step. **g** Top-side view of **f**. The continuous Cu blanket across the wafer was subsequently removed to liberate distinct microinductor devices.

5.6. Fabricated devices

5.6.1. High-resolution light microscope images

Fully fabricated dies and devices are showcased in this section. Figs. 5.16e-n show all ten discrete ADEPT devices, which are ordered by increasing size.

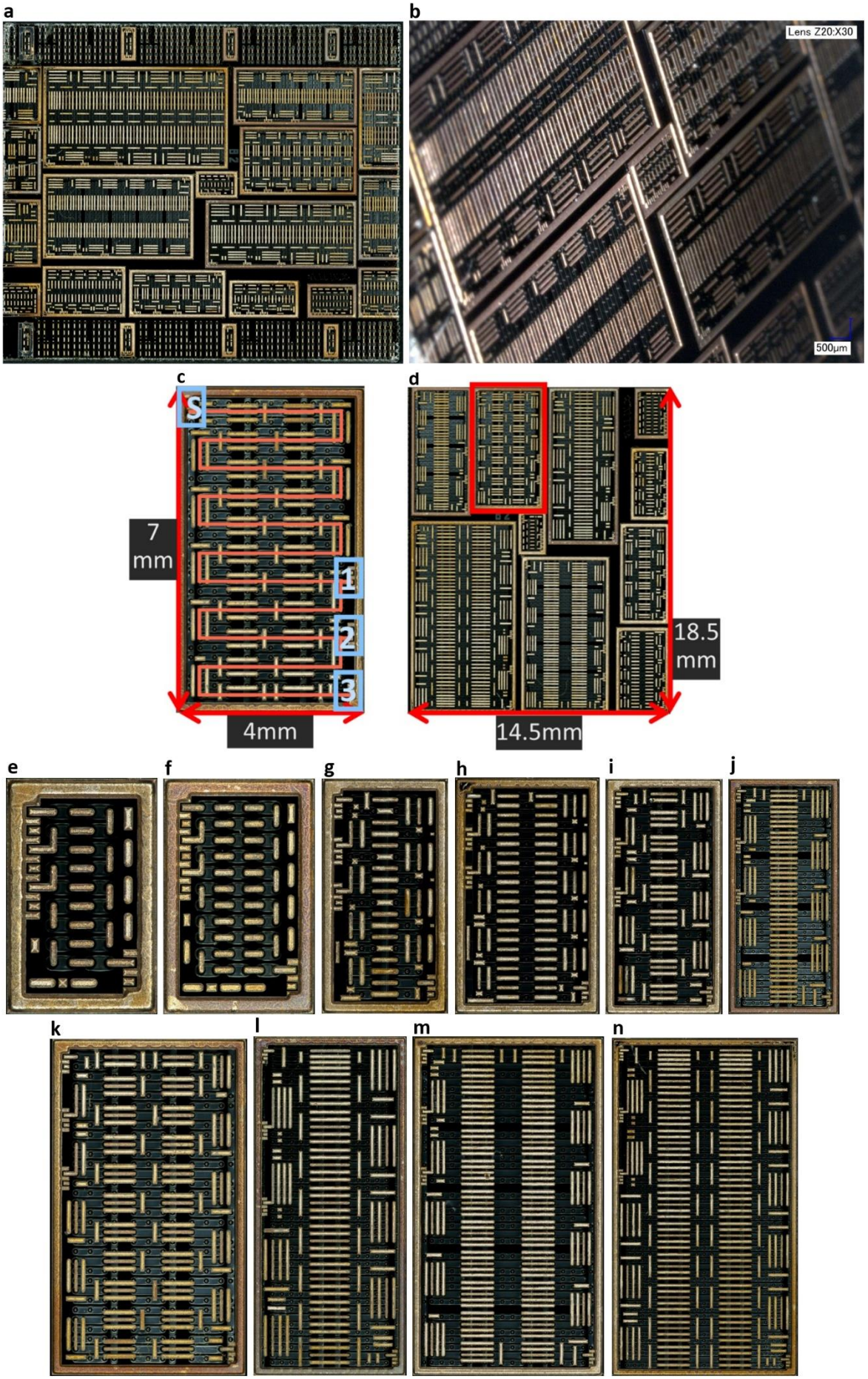
a
b
Lens Z20:X30
500µm
c
S
1
2
3
7
mm
4mm
d
18.5
mm
14.5mm
e
f
g
h
i
j
k
l
m
n

Figure 5.16. High-resolution images of the ADEPT and PMIC dies with all ten unique ADEPT microinductor devices. a Top-down view of the ADEPT and PMIC dies. Laser dicing was utilized to partition this section. **b** Angled view of the partitioned ADEPT die. **c** Magnified view of an ADEPT device showing the spatial dimensions. The current-carrying path is highlighted in red and the GSGSG probe points are blue, where S is the current source and 1-3 are the probe sensing points. In addition to the previously mentioned number of target Cu pillars for in series parameter testing (20, 28, 36, 42, 54 and 66), GSGSG probe points 1 and 2 and 1 and 3 also make a full circuit. This yields additional test options for 9, 13, 17 and 29 in series Cu pillars. **d** Full ADEPT die spatial dimensions with the device from **c** highlighted. **e** The centrally located ADEPT device that was featured throughout this chapter with a spatial dimension size rating of 1/10. **f** The top-right most device in **d** with spatial dimension size rating 2/10. **g** The 2nd device from the top in the right-hand column with size rating 3/10. **h** The bottom-right most device with size rating 4/10. **i** The 3rd device from the top in the right-hand column with size rating 5/10. **j** The top-left most device with size rating 6/10. **k** The highlighted device with size rating 7/10. **l** The device to the right of **k** with size rating 8/10. **m** The device under **l** with size rating 9/10. **n** The largest device in the bottom left.

5.6.2. X-ray images

X-ray images were also taken which demonstrate the 3D nature of the device, as shown in Fig. 5.17.

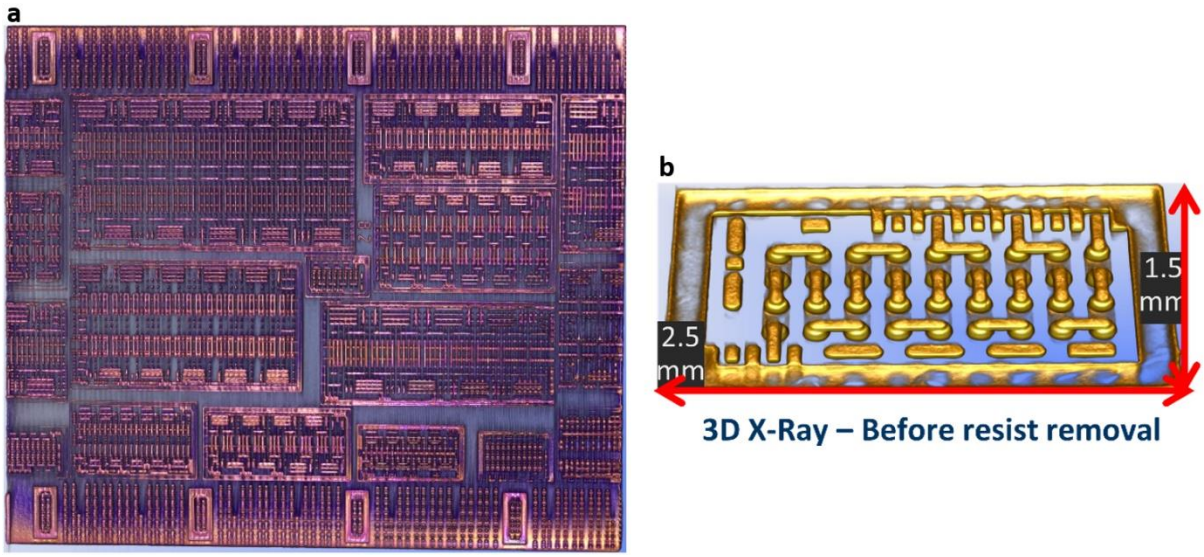

Figure 5.17. X-ray images. a Top-down view of the ADEPT and PMIC dies. **b** High-resolution X-ray of the smallest ADEPT device with vertical interconnects clearly visible.

5.7. Device characterization: results and analysis

5.7.1. Focused ion beam SEM micrographs

GSGSG testing probe efforts were successful in making physical contact with the target probe points, however an electrical signal was not successfully received at sensing points 1-3. This implied an open circuit somewhere along the current carrying path. The most likely place for this to occur was at the interface between the Cu pillars and the top interconnect. This is because an electrical connection through the bottom interconnect was required to electroplate the Cu pillars, however only a sputtered Cu seed was needed on the substrate distal photoresist to electroplate the top interconnect. To troubleshoot this, one of our process engineers used a

focused ion beam to get a cross-section of the top interconnect to Cu pillar interface, which was then imaged with an SEM, as shown in Fig. 5.18.

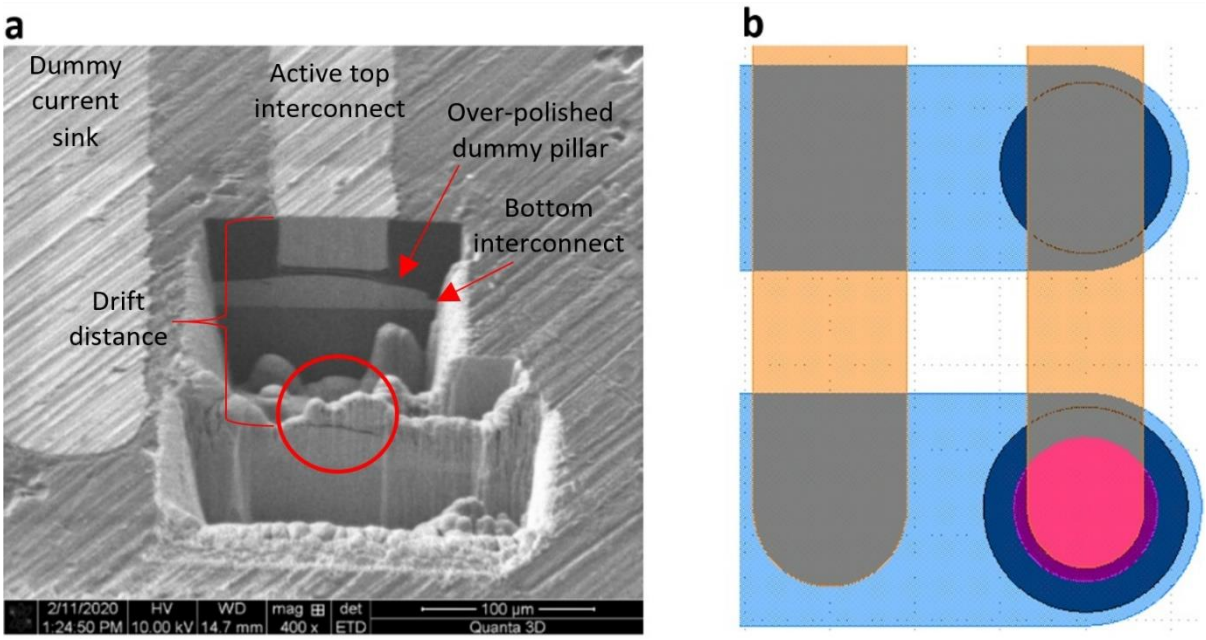

Figure 5.18. FIB cut of the Cu pillar to top interconnect interface. a Angled SEM micrograph of the FIB cut with a dummy top interconnect on the left and an electrically active top interconnect in the middle. The ion beam drifted significantly upwards during the long etching time (≈8 h), which obscured the point of interest, where the red circle marks the location of the target Cu pillar. This sample was taken from the wafer that was significantly over-polished during the 1st CMP, which resulted in a low aspect ratio for the dummy Cu pillar. This pillar notably displays the dome shaped topography that is characteristic of the post-CMP Cu pillars. The ion beam drift was persistent throughout several more FIB attempts and unfortunately, the fix to this problem requires a new FIB that can tolerate such long cutting times. The rough surface of this sample is due to mechanical polishing of the top interconnect with sandpaper, which was performed in lieu of ammonium persulfate chemical etching. **b** The corresponding KLayout photomask schematic of **a**.

To circumvent open circuits in a future fab, the SOPs for the selective Cu pillar mask (mask 3) and the top interconnect mask (mask 4) must be strictly adhered to. During processing for this fab, it was discovered that an exposure dose of 1622 mJ/cm^2 was erroneously utilized for both of these photomasks, which is 6.0 and 2.7 times the recommended doses in the provided corresponding SOPs (271 and 595 mJ/cm^2, respectively). Such a significant overexposure causes undesired cross-linking in the target dark zone due to constructive interference of spherical wavefronts at photomask occulter boundaries. As a reference point, the aspect ratio of the molds is only 0.1 in mask 3 and 0.6 in mask 4, which is highly feasible in THB-151N without use of a long pass UV filter or special processing (e.g., an in-situ photomask, as described in Chapter 6). Recall that one of the main outputs from the rigorous latent image simulation work of Chapter 3 was that an aspect ratio of 1 is highly feasible in THB-151N.

5.7.2. Photoresist stripping and SEM micrographs

In the effort to verify that the open circuits were located at the interface between the Cu pillars and the top interconnect, the blanket photoresist from process schematic step 15 was stripped in THB-S17. This caused the top interconnect to fully delaminate due to a lack of adhesion

between the top interconnect and the Cu pillars. This implied that the Cu pillar to top interconnect interface was likely filled with cross-linked photoresist as a result of the overexposure that occurred with mask 3. Furthermore, electrical testing was performed on the bottom interconnect to Cu pillar interface to verify this hypothesis, which is discussed in the following subsection. Fig. 5.19 shows images of the Cu pillars and the bottom interconnect.

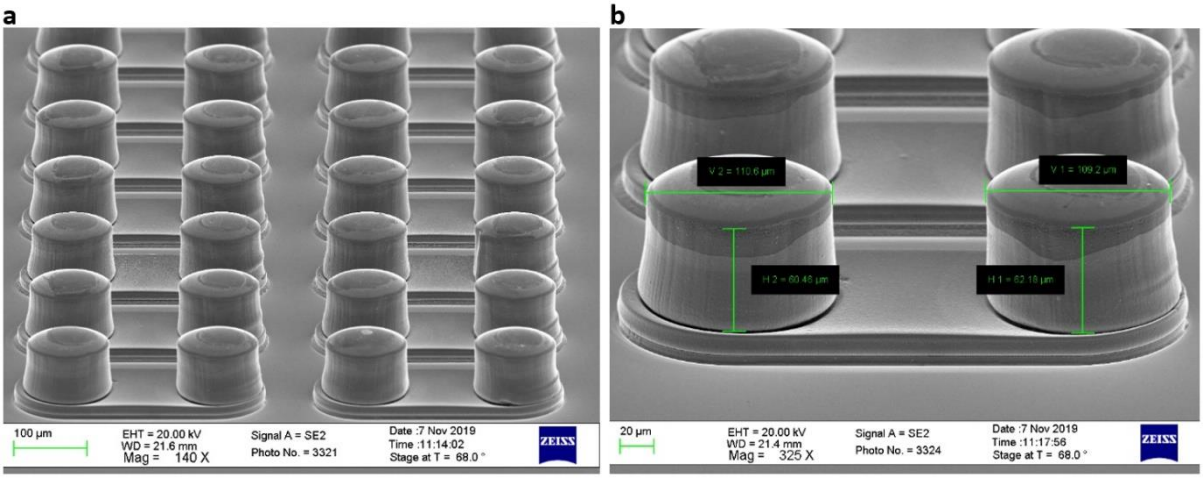

Figure 5.19. SEM micrographs of the Cu pillars and the bottom interconnect. a 68º angled view of the Cu pillar and bottom interconnect array. The top interconnect fully delaminated after stripping the photoresist blanket in THB-S17, which has a high selectivity for THB-151N over Cu. **b** Magnified view of **a**. These pillars are shorter (e.g., 62.18/sin(68º)=67 µm) than the target thickness of 100 µm, as this was originally a test wafer.

5.7.3. LCR meter electrical testing

LCR meter electrical tests were successful for the ternary in series current pathway comprising Cu pillar to bottom interconnect to Cu pillar[2]. Results are shown in Fig. 5.20.

a

Device zone ID	9x4-200	9x4-400	11x6-600	9x9-800	11x6-1000
Pillar spacing (µm)	90	290	490	690	890
Number of inductance measurements	4	7	5	6	7
Average inductance at 1 MHz (nH)	0.415	1.133	1.422	1.688	2.074

b

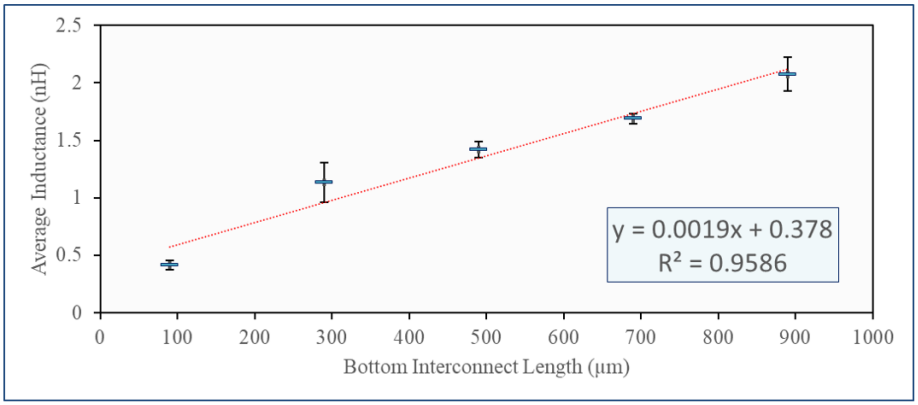

Figure 5.20. LCR electrical characterization results. a Inductance data for the ADEPT devices. The Device ZoneID is in the format of row x column – pillar pitch. **b** Graph of **a** (rows 2 & 4) with linear trendline data in the

bottom right. The error bars correspond to 95% confidence intervals using the arithmetic mean and t-table coefficients.

As expected, there is a linear relationship between Cu pillar pitch and inductance. From the above, we can extrapolate back to zero and divide by two to discern that the inductance of a single 110 µm diameter Cu pillar with a thickness of 67±5 µm coated in 4 µm of CoZrTa comprising 32x125 nm thick laminations is 0.189 nH. This results in an inductance to unit length ratio of 2.82 pH/µm for the Cu pillars. Furthermore, the inductance per unit length of the bottom interconnect is determined by subtracting the y-intercept from the inductance values in Fig. 5.20, which results in an average of 2.13 pH/µm for the bottom interconnect. Therefore, 4x110x100 µm (DxT) Cu pillars with 4 µm of vertical CoZrTa laminations would have an inductance of 1.70 nH. With a 200 µm pitch (e.g., 90 µm spacing) and square packing device topology, this results in an inductance density of 16.85 nH/mm^2, which is comparable to previously reported fabricated 3D microinductor devices[3,4,5,6].

5.7.4. Magnetic anisotropy investigation

Ideally, the vertically oriented magnetic material surrounding the Cu pillars would comprise a circumferentially directed magnetic hard axis that is concentric with the induced magnetic field. This would be highly beneficial, as it could broaden the working frequency domain and increase the saturation current of the 3D microinductor device. Therefore, the magnetic anisotropy of the fabricated device was investigated. First, a sample corresponding to process schematic step 10 (Fig. 5.5) comprising 110x67 µm (DxT) Cu pillars and 4 µm of CoZrTa with 32x125 nm thick vertical magnetic laminations was suspended in an epoxy mold. The sample was then cured at RT over a period of 24 h. Next, the sample was polished with sandpaper, as described in section 5.5, which removed all horizontally oriented magnetic material while leaving the vertically oriented magnetic material intact. Finally, in-plane (horizontal) and out-of-plane (vertical) B-H loop measurements were taken with a superconducting quantum interference device (SQUID). The results are shown in Fig. 5.21.

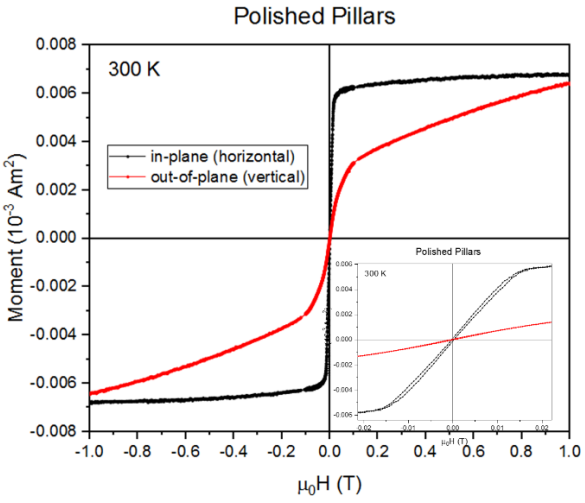

Figure 5.21. B-H loop of the isolated vertically oriented magnetic material[1]. The two loops demonstrate magnetic anisotropy. The external magnetic field was larger than the sample volume in both measurements and the coercivity is ~8-9 Oe in both directions[1].

Preferably, the easy axis would be directed in the out-of-plane (vertical) direction, which would imply either a circumferential or a radial hard axis. However, the in-plane (horizontal) direction appears as the easy axis in Fig. 5.21, which might imply either a radial or a circumferential anisotropy.

To further investigate this, LCR meter data was compared to corresponding simulation work. ADEPT group Ansys Maxwell simulations predict $L = 0.0141\ nH$ for an air core 100x67 µm (DxT) Cu pillar and $L = 0.513\ nH$ for the same Cu pillar coated in 4 µm of vertically oriented CoZrTa with a $\mu_r = 500$[7]. According to Fig. 5.20 and as discussed in section 5.7.3, the inductance of a 110x67 µm (DxT) Cu pillar coated in 4 µm of CoZrTa comprising 32x125 nm thick vertical magnetic laminations was measured to be 0.189 nH at 1 MHz. When approximating equal diameters (e.g., 110≈100 µm) and assuming a stable broad frequency response, the relative permeability of the magnetic material in the fabricated 3D microinductor is 184.37=(0.189/0.513)*500 (equation format $\mu_r' = (L'/L)\mu_r$, where μ_r', μ_r and L', L are the small and large relative permeability and inductance values, respectively). Since L=0.0141<0.189<0.513 nH, and since it is known that $\mu_r = 1$ for the easy axis at 1 MHz[8], wherein μ_r=1<184.37<500, it is implied that the magnetic anisotropy may be directed in both the vertical and the horizontal directions.

Therefore, it is likely that the as-deposited magnetic material in the fabricated 3D microinductor comprises a mixture of magnetic anisotropies (e.g., vertical and/or circumferential and/or radial). However as previously mentioned, a circumferential hard axis is ideal. Enabling this could be the focus of future integrated magnetics research, wherein for example, post sputtering magnetic annealing or in-situ magnets during sputter deposition could be used.

5.7.5. Microinductor footprint reduction investigation

As discussed in chapter 1, a key motivating factor for prototyping a 3D microinductor device is the potential to significantly reduce the device footprint by transitioning from horizontal conductor windings (2D) to vertically meandering conductor windings (3D). An example footprint reduction of 5.6x was given by comparing a 4-turn 3D microinductor to a reported 4-turn 2D microinductor[9], when assuming equivalent device parameters (e.g., inductance, dc resistance, saturation current and operating frequency) and magnetic material parameters (e.g., resistivity, coercivity, saturation magnetization, relative permeability and anisotropy field). Following 3D microinductor device prototyping and electrical characterization, the potential footprint reduction is now investigated. Table 5.1 displays Ansys Maxwell simulation data for various 3D microinductor topologies along with fabricated 3D microinductor metrics.

Table 5.1. Ansys Maxwell simulation data and 3D microinductor device metrics. The interconnect inductance contribution was not included in the simulation work, however the experimentally determined interconnect inductance per unit length metric (2.13 pH/µm) is included in the last two rows of the table. The parameter list is on the left-hand side, followed by simulation data and then metrics for the fabricated 3D microinductor prototypes. Where a 3D microinductor topology comprises more than 2 Cu pillars, square packing was used to calculate the device footprint area. The "Actual device parameters" column directly corresponds to the LCR meter electrical test data and the "Calculated device parameters" columns are extrapolated using the measured inductance per unit length metric for the Cu pillars (2.82 pH/µm). The inductance value in the right-most column was upwardly adjusted by 400/184.37=2.17x (equation format $\mu_r' = (L'/L)\mu_r$, as previously discussed) to enable comparing

simulations to directly corresponding experimental data (the salmon-colored columns). Simulation data provided by a colleague at Tyndall, excepting the Area, both L/A and the L (with interconnect) rows[7].

	Ansys Maxwell simulations							Prototyped 3D microinductor device		
Parameter	Value							Actual device parameters	Calculated device parameters	
Pillar diameter (µm)	150	100	75	50	25	10	100	110	110	110
Pillar thickness (µm)	200	200	200	200	200	200	100	67	100	100
Pillars in series	2	3	4	4	5	6	6	2	6	6
Pitch (µm)	226	196.5	125	158	161	188	200	200	200	200
Core thickness (µm)	13	8	6	6	5	4	4	4	4	4
Relative permeability	300	200	150	100	50	20	400	184.37	184.37	400
Area (mm^2) (square packing)	0.071	0.071	0.045	0.048	0.044	0.081	0.156	0.038	0.165	0.165
L (nH) (no interconnect)	4.04	3.75	3.90	3.84	3.97	4.05	3.75	0.38	1.69	3.67
L/A (nH/mm^2) (no IC)	57.10	53.08	86.77	79.34	89.41	49.90	23.97	10.07	10.27	22.28
L (nH) (with interconnect)	4.20	4.16	4.22	4.53	5.13	5.95	4.82	0.57	2.65	4.63
L/A (nH/mm^2) (with IC)	59.39	58.91	93.90	93.63	115.56	73.31	30.79	15.19	16.10	28.12

Upwardly adjusting the relative permeability of the fabricated 3D microinductor device from 184.37 to 400 (e.g., 2.17x, final column) corresponds to a hypothetical change in the magnetic material parameters (e.g., the anisotropy field). When using data in the salmon-colored columns to compare simulated values to directly corresponding experimental results (no interconnect), the inductance (nH) and inductance density (nH/mm^2) values differ by only 2.1% and 7.0%, respectively. Therefore, the simulated data is highly accurate and can be used as a predictive tool to explore the 3D microinductor design space.

When including the inductance per unit length metric for the interconnect in the simulation data (final two rows), a comparison to a state-of-the-art 2D microinductor reported by Tyndall researchers[10] can be performed, as shown in table 5.2.

Table 5.2. Example comparison between reported state-of-the-art 2D microinductors and simulated/prototyped 3D microinductors. Two inductance density metrics were reported and both are used in the comparison.

		Simulated		Prototyped device		
Data source	Anthony et. al.[10]	Max	Min	Actual (µr=184.37)	Calculated (µr=184.37)	Calculated (µr=400)
L/A (nH/mm^2)	10.75	115.56	30.79	15.19	16.10	28.12
	12.5					
Inductance density ratio	1	10.75	2.86	1.41	1.50	2.62
	1	9.25	2.46	1.22	1.29	2.25

The inductance density of the simulated and prototyped 3D microinductors exceeds that of the example reported state-of-the-art 2D microinductors by 2.46-10.75x, 1.22-1.50x ($\mu_r = 184.37$) and 2.25-2.62x ($\mu_r = 400$), respectively. Therefore, when using a constant inductance in this example comparison, the simulated/prototyped 3D microinductors enable a footprint reduction of 1.22-10.75x. The largest inductance density (115.56 nH/mm^2) was simulated using a VIA AR of 8 (200/25), which is feasible using photolithography, as a VIA AR of 9 was reported by researchers using THB-151N and an in-situ photomask[11].

These 3D microinductor simulations/prototypes represent a small sample of the total 3D microinductor design space, wherein significantly greater inductance density metrics could be achieved. For future 3D microinductor device prototypes/simulations, the inductance density could be significantly improved by increasing the magnetic core thickness and/or optimizing

the magnetic anisotropy characteristic of the integrated magnetic material and/or reducing the pillar diameter, wherein the VIA fabrication research presented in this thesis will be essential. Due to this, our magnetically enhanced 3D microinductor research holds great promise for applications in next generation power converters.

5.8. Achievements and conclusions

In this chapter, CMOS compatible fabrication methods for next generation integrated magnetics were demonstrated. In short, this entailed utilizing novel processing methods to rotate the traditional horizontally oriented microinductor current pathway 90º to enable vertically oriented 3D microinductors. A key advantage of this orientation is that it minimizes the microinductor device footprint while leaving excess substrate surface area for placement of additional circuitry and devices. Furthermore, vertically oriented microinductors bring value to 3D IC technology by expanding the domain of microinductor topology to offer a single magnetically enhanced VIA all the way to complex arrays of tightly packed EMI-free through substrate vias (TSVs) that hide invisibly in the substrate.

In this effort, novel magnetic lamination processing methods were incorporated into the full device fabrication process flow. This first required conformal PVD (sputtering) of CoZrTa magnetic laminations onto Cu pillars that were selectively interconnected with bottom interconnect to form the basis of a vertically oriented meandering current pathway. This was found to be an effective way to deposit magnetic material on the vertical surface of thick conductor structures (100+ µm) to form magnetically enhanced VIAs. Next, CMP was utilized to remove the horizontally oriented magnetic material from the top of the Cu pillars. This freed up the substrate distal pillar surface for selective electroplating of a top interconnect to complete the vertically meandering current pathway in a wire bond free monolithic design.

As it is a discrete device complete with a supporting structure (a blanket of low-κ THB-151N), the vertically oriented microinductor is compatible with high-throughput pick-and-place transfer printing technologies. A solder ball mask is also easily enabled for flip-chip applications. Additionally, the microinductor process fabrication method utilizes processing tools that are commonly available in both the research lab and the manufacturing process line. Therefore, scalable processing options were demonstrated for novel 3D micro-magnetic inductor structures.

Finally, fabrication of an ambitious 5-tiered photomask design stack comprising 14 unique devices on a single wafer was successfully demonstrated. This multifaceted design specification called for various device topologies comprising a multitude of spacing requirements. To avoid significant mushrooming and short circuits during electroplating due to large current density differentials across the wafer, a novel unit cell normalization technique was adopted. This technique was proven to be highly effective, wherein step height metrology revealed only a ±5 µm height differential across the entire wafer for 100+ µm thick electroplated Cu pillars.

Click to skip to next chapter.

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Chapter 6 – Summary and Future Work

6.1. Summary

VIA enhanced microinductors with a small footprint and minimal parasitics enable granular PoL power delivery with a distinct voltage rail for each of the unique devices in a highly dense IC[1]. This is essential for emerging next generation technologies in domains such as high-end computing, mobile devices, RF, automotive, space, AI, biotechnology and the IoT[2,3,4,5,6]. The aim of this thesis was to investigate the design and fabrication of novel 3D microinductors with magnetically enhanced VIAs for applications in MEMS, IVRs, 2D packages and 2.5/3D advanced packaging architectures.

Chapter 1 presented an introduction to microinductor functionality in a DC-DC buck converter. The microinductor stores electrical energy in the form of a transient magnetic field to power a load during the switch off state[7]. As opposed to linear power conversion, this converter topology offers high efficiency performance with minimal Joule heating[8]. The amount of energy stored is a function of the conductor cross-section, the microinductor device topology, the number of windings/turns, the relative permeability of the adjacent magnetic material and the magnetic material thickness[9,10]. The microinductor footprint can be reduced by increasing the switching frequency, thereby reducing the required inductance value. The footprint can also be significantly reduced by transitioning from a 2D to a 3D winding topology, which for example, can result in a footprint size reduction of 5.6x. Furthermore, a VIA clad in a laminated magnetic material significantly boosts inductance while reducing eddy currents and simultaneously functioning as an EMI shield[11,12]. Key research goals and challenges were introduced. Finally, the thesis chapters were outlined and the corresponding goals/challenges were identified.

Chapter 2 presented a detailed literature review on VIA applications, VIA fabrication methods, thick photoresists for VIA fabrication and reported 3D microinductors with VIAs, inclusive of patents and simulation only work. VIA applications are myriad and comprise for example, vertical interconnects in 2.5/3D packages[13], I/O pads for WLVP MEMS devices[14] and enabling a vertically oriented meandering current path for emerging 3D microinductor devices[15,16,17,18]. Notable VIA fabrication methods are time-multiplexed etching with the Bosch process[13], laser ablation with pulsed beams[14] and photolithography[19]. Of these, photolithography was identified as a promising VIA fabrication method due to its low cost, high-throughput and scalability. A survey of 30+ thick film photoresists was performed and THB-151N was selected due to its clear appearance for multi-tiered photomask alignment in a contact/proximity mask aligner, high-throughput processing capability (e.g., no post exposure bake (PEB) required), 90+ µm single spin thickness, low-loss tangent for permanent dielectric applications and ease of stripping[20,21]. Reported 3D microinductors using VIAs comprise toroidal, solenoid and spiral topologies, wherein fabricated Cu VIAs comprising a clad soft magnetic core were not reported[15,16,17,18]. As a result, and due to the many potential benefits of VIAs clad in soft magnetic material, this design option was selected as a key target component of novel magnetically enhanced 3D microinductors.

Chapter 3 examined the photoresist exposure process with special attention to diffraction effects, which are a major resolution limiting factor in photoresist VIA relief mold formation. A novel polychromatic light attenuation equation was derived from the Beer-Lambert law and presented in a general form for broad applications in optical systems. This formula significantly extends the previously reported work by including novel terms for the relative intensity of each of the incident wavelengths in broad spectrum exposure systems and the corresponding absorption coefficients for each wavelength. This equation was then inserted into an exact Rayleigh-Sommerfeld diffraction integral that is valid for circular aperture and occulter geometries in the ultra-near field condition (F>>1), which is typical of the mask aligner exposure process[22]. This resulted in a succinct formula comprising a complete coupling between resist photochemistry and diffraction effects. To enable alternate VIA geometries, additional diffraction equations, derived using the paraxial approximation, were also presented for square and rectangular aperture/occulter geometries, wherein their range of validity was rigorously discussed[23]. 2D and 3D photoresist latent image simulations were compared to directly corresponding experimental work, with highly positive correlation. These equations are accurate, converge quickly on the average modern computer and negate the need for costly and time consuming in-situ metrology[24]. Due to this, these formulae could add significant value to the lithography sector. Potential applications include: 1) numerical modeling with computational software such as Wolfram Mathematica, 2) integration into pre-existing photolithography simulators to broaden their computational domain by adding to their input space, and 3) development of a simple app for on-the-go use in mobile devices. Finally, various photoresist development mechanisms and methods were investigated. Spin development was selected as the optimal procedure for photoresist VIA relief mold formation due to highly efficient advection, easy control over puddle duration and compatibility with a heated developer dispense. My custom Wolfram Mathematica code for latent image simulations is provided in Appendix II.

Chapter 4 used the FEM in COMSOL Multiphysics to enable predictive modeling of 2D and 3D electrode growth during the VIA metallization process. Key fundamental equations comprised: 1) the full Nernst-Planck mass transport formula with terms for diffusion, migration and advection and 2) the Butler-Volmer formula for the electrochemical reaction kinetics. These formulae were discussed in detail and then implemented in a multiphysics simulation comprising as many as four simultaneously coupled physics modules consisting of Tertiary Current Distribution, Laminar Flow, Deformed Geometry and Moving Mesh. Various control volumes were modeled in separate time-dependent studies, wherein a comparison analysis was performed between corresponding 2D and 3D simulation geometries for cross-verification, which yielded identical results. Furthermore, 2D and 3D electrode growth simulations were then compared to directly corresponding experimental work, with highly positive correlation. A special focus was given to electrode topographies, which provided useful insights into the electroforming process with potential applications in flat surface fabrication for FC process compatibility and high surface area surfaces with convex or concave topographies for advanced sensor applications.

Chapter 5 first introduced the target 3D microinductor device with Cu VIAs clad in a laminated soft magnetic core and monolithic top and bottom interconnects. A detailed schematic depicting an x-z unit cell cross-section of the 3D microinductor device was provided and proceeded by a 16-step process schematic. Following this, a 5-tier photomask design using

KLayout was described. Specifics of the device topology and key aspects of the photomask design process were then discussed. As 14 discrete 3D microinductor devices were required to be simultaneously fabricated on a single 4" wafer, a key design challenge was normalizing the electroplating density between highly differentiated microinductor device topologies. This was performed at the device level using a unit cell approach. Next, key aspects of the SOPs were discussed. CMP emerged as a key challenge during the fabrication process, which was troubleshooted in detail. As an alternative to CMP, two methods were proposed and enacted to enable etching of the final electroplated Cu blanket, thereby realizing fully fabricated prototypes of novel 3D microinductor devices. Metrology and characterization were performed with a light microscope, SEM, X-rays, FIB and an LCR meter. The prototype microinductor electrical performance indicated that the electrical connection between the monolithic top interconnect and the Cu pillars was not established. During processing for this fab, it was discovered that an exposure dose of 1622 mJ/cm^2 was erroneously utilized for both of these photomasks, which is 6.0 and 2.7 times the recommended doses in the provided corresponding SOPs (271 and 595 mJ/cm^2, respectively). This would be very easily avoided in a sequential device run. Whilst the top interconnect was an open circuit, the bottom interconnect functioned as designed. LCR measurements performed between adjacent interconnected Cu pillars showed an inductance to unit length ratio of 2.82 pH/µm for the Cu pillars and 2.13 pH/µm for the bottom interconnect, wherein 4x110x100 µm (DxT) Cu pillars comprising 4 µm of clad CoZrTa soft magnetic vertical laminations would have an inductance of 1.70 nH. When utilizing a 200 µm pitch and square packing, this corresponds to an inductance density of 16.85 nH/mm^2. Whilst this value is similar to previously reported metrics for 3D microinductors[15,16,17,18], it can be significantly improved by increasing the magnetic core thickness and/or optimizing the magnetic anisotropy characteristic of the integrated magnetic material. Additionally, the pillar diameter can be reduced to increase the inductance per unit length metric, wherein the VIA fabrication research presented in this thesis will be an essential asset. Therefore, this magnetically enhanced 3D microinductor research holds great promise for applications in next generation power converters.

6.1.1. Main contributions of this work

1. An extensive literature review of state-of-the-art VIA applications, VIA fabrication methods, thick photoresists for VIA fabrication and reported 3D microinductors with VIAs, inclusive of patents and simulation only work.
2. A novel polychromatic light attenuation equation, presented in a general form for broad applications in optical systems that includes for the first time, the relative intensity of each of the incident wavelengths in broad spectrum exposure systems and the corresponding absorption coefficient for each wavelength.
3. Novel exposure dose and critical exposure dose determination methods using the polychromatic light attenuation equation.
4. Integration of these novel equations and methods with an exact scalar diffraction equation, valid for the ultra-near aperture/occulter condition (e.g., a 1 µm gap), that enables rapid 3D latent image simulations, wherein circular symmetry is exploited to minimize computation time.

5. The discovery that diffraction effects are significant and must be accounted for during the photoresist exposure process, even when the photomask diffractor size and the incident wavelength(s) differ by more than two orders of magnitude.
6. Performed 2D and 3D time-dependent FEM studies in COMSOL Multiphysics to accurately model concave, flat and convex electrode topographies with the Tertiary Current Distribution, Laminar Flow, Deformed Geometry and Moving Mesh physics modules.
7. Discovered that diffusion and advection mass transport conditions can be utilized to enable tailored electrode topographies for flip chip and sensor applications.
8. Designed and fabricated 14 novel 3D microinductor device prototypes with unique cross-sections comprising monolithic Cu pillars clad in a vertically oriented laminated soft magnetic material. The Cu pillars are selectively interconnected in the form of unit cells comprising a top interconnect, a first Cu pillar, a bottom interconnect and a second Cu pillar all connected in series.
9. The 3D microinductor devices were achieved by a novel fabrication process flow utilizing novel SOPs and novel photomask designs. The mask designs used a unit cell approach to compensate for highly variable device topologies, thereby normalizing the current density across the full wafer Si to enable simultaneous fabrication of 14 unique 3D microinductor devices.
10. Demonstrated the feasibility of fabricating the proposed 3D microinductor using photolithography as the VIA fabrication method, wherein the design space was explored to highlight promising options that could significantly improve device performance metrics for future fabrication efforts.
11. Established a highly detailed step-by-step protocol for fabricating prototypes of the target 3D microinductor device, which will be essential for future fabrication efforts that aim to investigate the full potential of this device design space for applications in next generation integrated magnetics.

6.2. Future work

6.2.1. In-situ photomask

As described in chapter 3, key resolution limiting factors during the photoresist exposure process are the photomask to photoresist air gap and light diffraction at photomask occulter boundaries. Since THB-151N is an i-line sensitive photoresist, a long pass filter could be used to attenuate shorter wavelengths, which would reduce or eliminate the skin effect, as has been reported with SU-8[25]. This would make THB-151N more compatible with HAR thick film processing, as its sensitivity to the broad-spectrum UV light from an Hg bulb would be significantly reduced, thereby enabling a more linear absorption vs. photoresist thickness characteristic. Furthermore, elimination of the air gap would be highly advantageous, however this is very difficult to achieve with standard processing due to variations in the photoresist topography for highly viscous thick films[26]. An elegant solution to these problems has been reported with THB-151N, wherein an in-situ photomask was used, as depicted in Fig. 6.1.

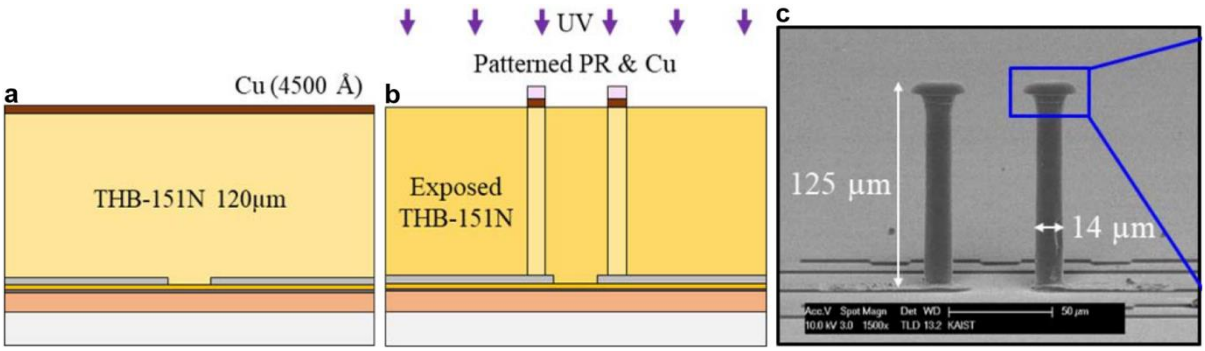

Figure 6.1. In-situ photomask process and corresponding HAR Cu pillar SEM micrograph[19]. a A thick layer of THB-151N is spun and pre-exposure baked to evaporate the PGMEA solvent, thereby significantly increasing its viscosity and forming a quasi-solid thick film. A 0.45 µm thick layer of Cu is then sputtered onto the substrate-distal surface of the unexposed THB-151N. **b** A thin photoresist film (e.g., THB-151N) is then spun, baked, exposed and developed on top of the sputtered Cu seed. If a negative photoresist is used, a dark field photomask would be needed to enable selective etching of the sputtered Cu blanket (e.g., with ammonium persulfate). Once the selective Cu etching is complete and the in-situ photomask is established, the thick THB-151N is then flood exposed. **c** Electroplated Cu pillars with an AR of ≈9 fabricated from THB-151N VIA molds using the method of **a**-**b**. (**a**-**c** reprinted from ref. 19 with kind permission from IEEE. Copyright 2018 IEEE.)

This method is highly advantageous as it: 1) eliminates the air gap by selectively etching a Cu seed sputtered directly on top of a thick layer of unexposed THB-151N to form an in-situ photomask and 2) introduces a long pass filter situated directly on top of the in-situ photomask. Due to these significant advantages, this method holds great promise for HAR VIA fabrication in next generation 3D microinductors.

6.2.2. Polymer core VIAs

A method to significantly reduce the electroplating duration for thick Cu pillars is to use a polymer core VIA design, as has been reported with SU-8[15,17].

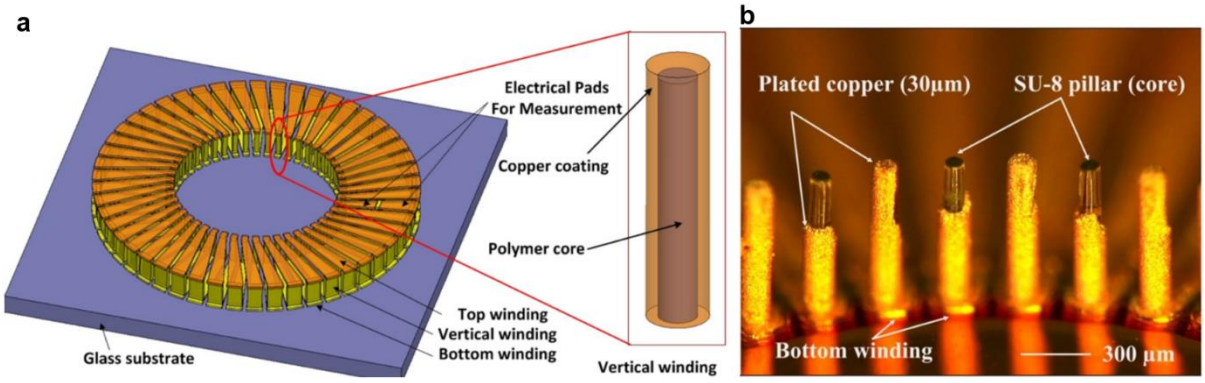

Figure 6.2. 3D microinductor using polymer core VIAs[17]. a A 3D toroidal microinductor schematic. The VIA polymer core is 650 µm thick and 110 µm in diameter. The electroplated Cu is ≈30 µm thick. **b** Optical image of the polymer core VIAs from **a** with the electroplated Cu partially removed. (**a**-**b** reprinted from ref. 17 with kind permission from IOP Publishing, Ltd. Copyright 2013 IOP Publishing, Ltd.; permission conveyed through Copyright Clearance Center, Inc.)

This would be highly advantageous for example, if very HF MOSFET switching was used in an IVR, wherein due to Lenz's law, the skin effect would cause a solid conductor to approximate a hollow conductor[15]. Furthermore, HAR VIA mold fabrication would be

simplified by using a dark field photomask and a negative photoresist. With a dark field photomask, light diffracted at photomask aperture boundaries would diverge into the photomask dark zone with significantly reduced irradiance due to minimal constructive interference. The opposite occurs with a bright field photomask, wherein light diffracted at photomask occulter boundaries converges in the photomask dark zone with significantly increased irradiance due to constructive interference, leading to undesired cross-linking.

6.2.3. Electroplating soft magnetic laminations

During 3D microinductor device fabrication, sputtering vertical soft magnetic laminations was difficult due to: 1) the requirement of the MEMS laboratory for wafers uncontaminated with metals other than Cu (e.g., NiFe) and 2) a long sputtering duration (e.g., 1µm/h). As an alternative to sputtering, a method for electroplating a laminated permalloy (e.g., $Ni_{45}Fe_{55}$) was reported in the literature, as shown in Fig. 6.3[27,28,29].

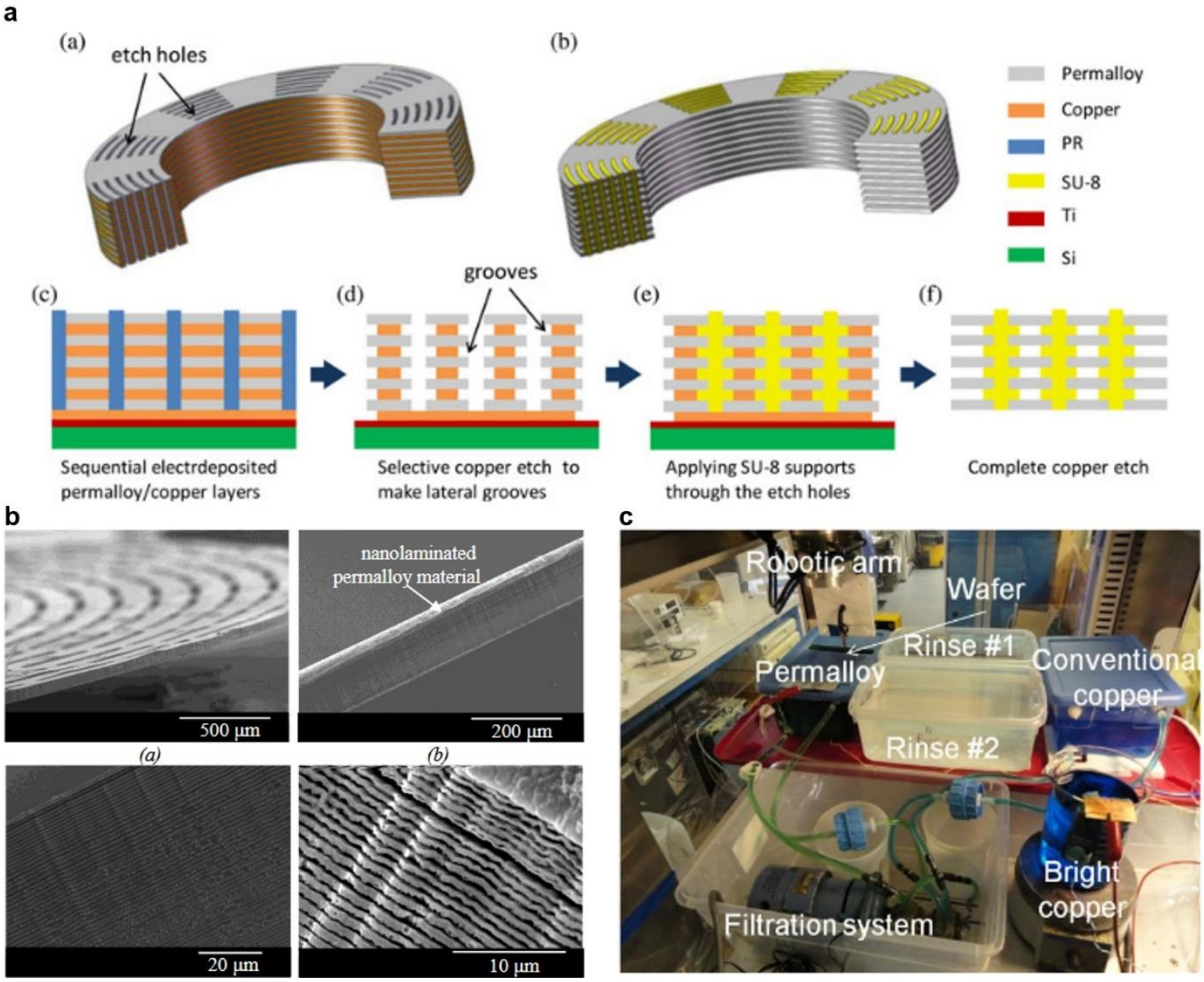

Figure 6.3. Alternative method for soft magnetic core deposition. a Schematic of a toroidal magnetic core with horizontal laminations, inclusive of the corresponding process schematic[27]. (Reprinted from ref. 27 with kind permission from IEEE. Copyright 2013 IEEE.) **b** SEM micrographs of a laminated magnetic core fabricated in a similar manner to **a**[29]. **c** High-throughout electrodeposition setup for fabricating the magnetic laminations in **b**. A robotic arm is used to quickly submerge the wafer in the bright Cu beaker for Cu electrodeposition. The wafer is then rinsed in a first water bath. Next, the wafer is submerged in the permalloy bath for permalloy electrodeposition. Finally, the wafer is submerged in a second water bath in the effort to avoid cross-contamination. This dipping cycle is repeated until *n* laminations are electrodeposited. A robotic arm is used for

high-throughput processing and to ensure electroplating thickness uniformity in the laminated stack. (**b**-**c** reprinted with kind permission from the authors.)

Since electroplating is used, this method could potentially be significantly faster than sputtering. Furthermore, this method circumvents the need for lab-to-lab wafer transfer for permalloy deposition, thereby avoiding the non-contaminated wafer requirements of certain laboratories. Although this method was demonstrated with horizontal laminations, it could be adapted to fabricate vertically oriented laminations by using a Cu pillar patterned substrate. Alternatively, horizontal magnetic laminations could be advantageous with Cu pillars in a 3D microinductor topology. This is due to the minimization of eddy currents, which would be directed orthogonal to the lamination axis, thereby limiting the eddy current path length for efficient power conversion.

Click to skip to Appendix I.

6.3. References

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on SU-8 negative thick photoresist by air gap elimination. *Microsystem Technologies* **8**, 308–313 (2002).

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Appendix I: Patents, publications and awards

Patents

O'Mathuna, C. et. al. A Vertical Magnetic Structure for Integrated Power Conversion. Patent Application PCT/EP2019/077978, (2020).

Publications

Smallwood, D. C., McCloskey, P., O'Mathuna, C., Casey , D. P., Rohan, J. F. Methods for latent image simulations in photolithography with a polychromatic light attenuation equation for fabricating VIAs in 2.5D and 3D advanced packaging architectures. *Microsystems & Nanoengineering* **7**, 39 (2021). https://doi.org/10.1038/s41378-021-00266-x

Smallwood, D. C., O'Mathuna, C., McCloskey, P., Rohan, J.F. Mathematical modelling of diffusion and convection in MEMS electroplating for energy and sensor technologies. *71st Annual ISE Meeting*, Belgrade, Serbia, (2020). Poster presentation.

Awards

Masood, A. et al. A novel sustainable electric motor using high-grade permanent magnets based on common metallic elements. SFI Innovator Prize Phase 1 Award, (2019).

Imec ASCENT project Ref. No. 145. Proposal and success story, (2018).

Vulcan. Tyndall Scientific Image Competition Winner, (Dec. 2020).

Oculus. Tyndall Scientific Image Competition Winner, (Aug. 2020).

Micro Circuit Metropolis. Tyndall Scientific Image Competition Winner, (Sept. 2020).

Icy Comet Nucleus. Tyndall Scientific Image Competition Winner, (May 2019).

Mushroom Man. Tyndall Scientific Image Competition Winner, (2018).

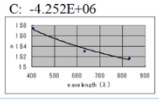
Appendix II: Wolfram Mathematica code

The following is my custom code from Wolfram Mathematica that uses the equations from chapter 3. This example is for a 50 µm diameter circular occulter with an exposure gap of 100 µm, as corresponds to Fig. 3.3g-h.

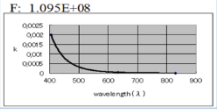
Constants

Cauchy Coefficients for THB-151N

$n=A+B/\lambda^2+C/\lambda^4$
A: 1.499E+00
B: 1.240E+04
C: -4.252E+06



$k=D+E/\lambda^2+F/\lambda^4$
D: 3.466E-04
E: -3.949E+02
F: 1.095E+08



```
In[1]:= A = 1.499;
        B = 12400;
        Cc = -4252000;
        Dd = 0.0003466;
        Ee = -394.9;
        F = 109500000;
```

Wavelengths

```
In[7]:= λ1 = 365; "I-line";
        λ2 = 405; "H-line";
        λ3 = 436; "G-line";
```

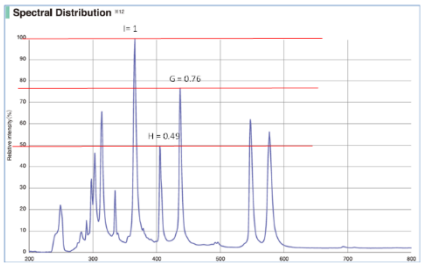
Refractive indexes

```
In[10]:= n0 = 1; "air";
         n1 = A + B / λ1^2 + Cc / λ1^4;
         n2 = A + B / λ2^2 + Cc / λ2^4;
         n3 = A + B / λ3^2 + Cc / λ3^4;
         nCuλ1 = 1.3621`200;
         nCuλ2 = 1.3009`200;
         nCuλ3 = 1.2473`200;
```

Absorption coefficients

```
In[17]:= k1 = Dd + Ee / λ1^2 + F / λ1^4;
         k2 = Dd + Ee / λ2^2 + F / λ2^4;
         k3 = Dd + Ee / λ3^2 + F / λ3^4;

         α1 = 4 * π * k1 / 0.365`200;
         α2 = 4 * π * k2 / 0.405`200;
         α3 = 4 * π * k3 / 0.436`200;
```

Reflection coefficients



In[23]:=
```
I01 = 1;
I02 = 0.49`200;
I03 = 0.76`200;

d = 0; "Refraction angle in air";
θ = 0; "Refraction angle in PR";

R1pA = ((n0 / Cos[d] - n1 / Cos[θ]) / (n0 / Cos[d] + n1 / Cos[θ]))^2; "P polarized";
R1sA = ((n0 * Cos[d] - n1 * Cos[θ]) / (n0 * Cos[d] + n1 * Cos[θ]))^2; "S polarized";
R1A = (R1pA + R1sA) / 2; "Air to PR";

R1pB = ((n1 / Cos[d] - nCuλ1 / Cos[θ]) / (n1 / Cos[d] + nCuλ1 / Cos[θ]))^2;
R1sB = ((n1 * Cos[d] - nCuλ1 * Cos[θ]) / (n1 * Cos[d] + nCuλ1 * Cos[θ]))^2;
R1B = (R1pB + R1sB) / 2; "PR to Cu substrate";

R2pA = ((n0 / Cos[d] - n2 / Cos[θ]) / (n0 / Cos[d] + n2 / Cos[θ]))^2; "P polarized";
R2sA = ((n0 * Cos[d] - n2 * Cos[θ]) / (n0 * Cos[d] + n2 * Cos[θ]))^2; "S polarized";
R2A = (R2pA + R2sA) / 2; "Air to PR";

R2pB = ((n2 / Cos[d] - nCuλ2 / Cos[θ]) / (n2 / Cos[d] + nCuλ2 / Cos[θ]))^2;
R2sB = ((n2 * Cos[d] - nCuλ2 * Cos[θ]) / (n2 * Cos[d] + nCuλ2 * Cos[θ]))^2;
R2B = (R2pB + R2sB) / 2; "PR to Cu substrate";

R3pA = ((n0 / Cos[d] - n3 / Cos[θ]) / (n0 / Cos[d] + n3 / Cos[θ]))^2; "P polarized";
R3sA = ((n0 * Cos[d] - n3 * Cos[θ]) / (n0 * Cos[d] + n3 * Cos[θ]))^2; "S polarized";
R3A = (R3pA + R3sA) / 2; "Air to PR";

R3pB = ((n3 / Cos[d] - nCuλ3 / Cos[θ]) / (n3 / Cos[d] + nCuλ3 / Cos[θ]))^2;
R3sB = ((n3 * Cos[d] - nCuλ3 * Cos[θ]) / (n3 * Cos[d] + nCuλ3 * Cos[θ]))^2;
R3B = (R3pB + R3sB) / 2; "PR to Cu substrate";
```

Attenuation equations

In[46]:=
```
zmax = 100; "Set PR thickness";
gap = 100; "Set gap thickness";

zadjA[z_] := z - gap; "Depth in PR";
zadjB[z_] := 2 * zmax + gap - z; "Reflection travel length in PR";

absA[z_] := ((1 - R1A) * I01 * e^(-2*α1*zadjA[z]) + (1 - R2A) * I02 * e^(-2*α2*zadjA[z]) + (1 - R3A) * I03 * e^(-2*α3*zadjA[z])) / (I01 * e^(-α1*zadjA[z]) + I02 * e^(-α2*zadjA[z]) + I03 * e^(-α3*zadjA[z]));
absB[z_] := ((1 - R1A) * R1B * I01 * e^(-2*α1*zadjB[z]) + (1 - R2A) * R2B * I02 * e^(-2*α2*zadjB[z]) + (1 - R3A) * R3B * I03 * e^(-2*α3*zadjB[z])) / (I01 * e^(-α1*zadjB[z]) + I02 * e^(-α2*zadjB[z]) + I03 * e^(-α3*zadjB[z]));
```

Critical exposure dose for THB-151N

In[52]:=
```
ED = 1100; "At T=100um. From the THB-151N TDS";
CED = ED * (absA[200] + absB[200]);
```

Wave number

In[54]:=
```
k = 2 * π / 0.405`200; "Integrate with H-line";
```

Rayleigh-Sommerfeld diffraction equation (Dubra-Ferrari)

Misc.

In[55]:=
```
zR[z_] := 2 * zmax + 2 * gap - z; "Total reflection travel length";
```

Axial points

In[56]:=
```
axial1[R_, z_] := -z * e^(i*k*(z^2+R^2)^(1/2)) / (z^2 + R^2)^(1/2);
axial2[R_, z_] := -zR[z] * e^(i*k*(zR[z]^2+R^2)^(1/2)) / (zR[z]^2 + R^2)^(1/2);
```

Radial points

In[58]:=
```
c[x_, R_] := x * Cos[φ] + (R^2 - x^2 * (Sin[φ]^2))^(1/2)
radial1[x_, R_, z_] := -z / (2 * π) * NIntegrate[(e^(i*k*(z^2+c[x,R]^2)^(1/2))) / (z^2 + c[x, R]^2)^(1/2), {φ, 0, 2 * π}, AccuracyGoal → 4, PrecisionGoal → 4, WorkingPrecision → 4];
radial2[x_, R_, z_] := -zR[z] / (2 * π) * NIntegrate[(e^(i*k*(zR[z]^2+c[x,R]^2)^(1/2))) / (zR[z]^2 + c[x, R]^2)^(1/2), {φ, 0, 2 * π}, AccuracyGoal → 4, PrecisionGoal → 4, WorkingPrecision → 4];
```

Calculations

Axial points

Manual

In[61]:=
```
apt1A = Parallelize[Table[axial1[25, 100], 1]]; "Input R,z. Normal depth";
apt1B = Re[apt1A]^2 + Im[apt1A]^2;
apt1C = absA[100] * apt1B
```

Out[63]= {0.893773}

Automatic

```
apt1Ae = Parallelize[Table[axial1[25, n], {n, 100, 200}, 1]];
apt1Be = Re[apt1Ae]^2 + Im[apt1Ae]^2;
apt1Ce = Table[absA[n], {n, 100, 200}, 1];
apt1De = apt1Be * apt1Ce
```

Automatic saved data

```
apt1DeSave = {{0.8937733397443967`}, {0.8274720602697407`}, {0.7694101687377379`}, {0.7184429174013544`}, {0.6735741393448129`}, {0.6339389898960305`},
   {0.5987884957775599`}, {0.5674757249273505`}, {0.5394434130106169`}, {0.5142129024233191`}, {0.4913742663945182`}, {0.4705775049659246`},
   {0.451524711819928`}, {0.43396312011728294`}, {0.4176789457020645`}, {0.4024919510981651`}, {0.3882506616555686`}, {0.37482816979570904`},
   {0.362118468423075`}, {0.35003325898450327`}, {0.33849918378767 4`}, {0.3274554360852199`}, {0.3168517051425556`}, {0.3066464170656142 4`},
   {0.29680523558191496`}, {0.2872997902456833 6`}, {0.2781066026685441`}, {0.2692061843512824`}, {0.2605822824979242`}, {0.2522212528206176`},
   {0.24411154078454098`}, {0.2362432549914847`}, {0.2286078184574373 3`}, {0.2211976854053542`}, {0.2140061128742340 4`}, {0.2070269779471798 4`},
   {0.20025463273381278`}, {0.1936837904172272`}, {0.1873094367050758 8`}, {0.1811267619188557 7`}, {0.1751311097330173 8`}, {0.1693179392391538 6`},
   {0.16368279758345156`}, {0.1582213009096813`}, {0.1529291217511502 3`}, {0.1478019813608556 5`}, {0.1428356457587496 9`}, {0.1380259245164213`},
   {0.13336867149955555`}, {0.1288597869534743 6`}, {0.1244952204522845 7`}, {0.1202709743423661 4`}, {0.1161831074002005 2`}, {0.1122277384963547`},
   {0.10840105011478254`}, {0.1046992916220195 6`}, {0.1011178221646901`}, {0.0976559135156065`}, {0.0943071517600745`}, {0.0910690396295512 1`},
   {0.08793819767700396`}, {0.0849113252936274 5`}, {0.0819852019441310 9`}, {0.0791566865401549 1`}, {0.0764227185729208 5`}, {0.0737803174381501 8`},
   {0.07122658213750158`}, {0.0687586906645457 9`}, {0.0663738992037869 6`}, {0.0640695411671328 2`}, {0.0618430260905655`}, {0.0596918384120943 4`},
   {0.05761353615022584`}, {0.0556057495005095 95`}, {0.0536661793659508 75`}, {0.0517925958354728 4`}, {0.0499828366230585 4`}, {0.0482348054787596 1`},
   {0.046546470581422826`}, {0.0449158629217575 2`}, {0.0433410746832454 6`}, {0.0418202576273809`}, {0.0403516214888097 8`}, {0.0389334323851157 1`},
   {0.03756401124526564`}, {0.0362417322600743 36`}, {0.0349650213574680 6`}, {0.0337323547048182 1`}, {0.0325422572401667 9`}, {0.0313933012337733 74`},
   {0.03028410488107266 5`}, {0.0292133309278340 86`}, {0.0281796853280603 18`}, {0.0271819159349407 9`}, {0.0262188112249825 3`}, {0.0252819905533354 3`},
   {0.024391945453992047`}, {0.0235259534428574 02`}, {0.0226901618930138 68`}, {0.0218835444119381 65`}, {0.0211051082620696 86`}};
```

Radial points

Manual

```
rpt1A = Parallelize[Table[radial1[x, 25, 100], {x, 1, 25}]]; "Input R,z. Normal depth";
rpt1B = Re[rpt1A]^2 + Im[rpt1A]^2;
rpt1C = absA[100] * rpt1B
```

Out[71]= {0.144768, 0.0626334, 0.0128064, 0.00156157, 0.0152273, 0.0269448, 0.0225037, 0.00944935, 0.00302858, 0.00855293, 0.0180563, 0.0213364, 0.0161827, 0.00957903, 0.00943188, 0.0171498, 0.0276719, 0.0350669, 0.0375892, 0.0385857, 0.0463837, 0.0687003, 0.111467, 0.176892, 0.270374}

Automatic

```
rpt1Ae = Parallelize[Table[radial1[x, 25, n], {n, 100, 200}, {x, 1, 25}]];
rpt1Be = Re[rpt1Ae]^2 + Im[rpt1Ae]^2;
rpt1Ce = Table[absA[n], {n, 100, 200}, 25];
rpt1De = rpt1Be * rpt1Ce
```

Automatic saved data

```
rpt1DeSave = {{0.14476826915015856`, 0.062633371655921 66`, 0.012806385099334641`, 0.0015615701113955572`, 0.015227293166445643`, 0.026944840842143148`,
    0.022503685267784 44`, 0.009449351872784 78`, 0.003028580071028967`, 0.008552928375553501`, 0.0180563325414701`, 0.021336411653139403`, 0.016182679994294073`,
    0.009579025562580609`, 0.009431881373294773`, 0.017149792902613 39`, 0.027671923519902743`, 0.035066883002978 73`, 0.037589184372856 59`, 0.038585744418465`,
    0.046383688848059977`, 0.068700268023003 91`, 0.111467445178747 56`, 0.176892468997254 97`, 0.270374343812247 8`},
   {0.13321414127189 92`, 0.062139363558807 6`, 0.016473573277232617`, 0.001035067331790853`, 0.009334924437149672`, 0.021893575315667678`, 0.023488781178663726`,
    0.014206251250314453`, 0.004789034843049 67`, 0.004055415966290703`, 0.011252005334328746`, 0.018616327724065986`, 0.019810600277947 28`, 0.015261676381680878`,
    0.010355302942793318`, 0.010721675742135473`, 0.017771922626068 37`, 0.028629280497782 65`, 0.038890225090999 72`, 0.046838176816091 39`, 0.053538495902 29549`,
    0.06540828284655106`, 0.091807579970521 5`, 0.145048524864005 5`, 0.231500371391120 23`},
   {0.12282137799180161`, 0.061170385524443004`, 0.019943177724131775`, 0.001869089161172491`, 0.004982102763907199`, 0.016269608797133843`, 0.022035171246642 68`,
    0.017733281275121804`, 0.008727333201230366`, 0.003429011389200353`, 0.005682457437341067`, 0.012673409547156008`, 0.018265763259989864`,
    0.019437883140517 25`, 0.015910612624702853`, 0.012201482353896115`, 0.012476181399482459`, 0.018645644512688 01`, 0.029850646924357693`, 0.043738277793016 23`,
    0.058518689998329 61`, 0.074724611298714 73`, 0.097035435017538 63`, 0.133691158705205 2`, 0.200205515853609 05`},
   {0.11345734525254172`, 0.059807730436177486`, 0.023067329802334606`, 0.003702734129785555 6`, 0.002270557583809142`, 0.010915227921207133`,
    0.018717224018727 58`, 0.019098967917135164`, 0.012940428323526416`, 0.005969936555596403`, 0.003529814164635308`, 0.007368585113247654`, 0.013365638943133 03`,
    0.018358163779770592`, 0.019762716973737 02`, 0.017853493063263 12`, 0.015319299853133 43`, 0.015395564177205 326`, 0.020672610002885 81`, 0.031932107827206 93`,
    0.049474070429031104`, 0.072248904822775 38`, 0.102265519942406 82`, 0.142790709947510 2`, 0.201672015479344 96`},
   {0.10499981945285 08`, 0.058121400601317 54`, 0.025747712345266 13`, 0.006191225767588456`, 0.001127882317263846`, 0.006438939067438755`, 0.014317821444579415`,
    0.018116717861128007`, 0.015822253090827052`, 0.009959386822594 9`, 0.004967582762991508`, 0.004047058546285827`, 0.007502360029849991`, 0.013127093892777 55`,
    0.018332210970196 93`, 0.021030273331641 35`, 0.020971343076686 63`, 0.020067014852238402`, 0.020686050678207 79`, 0.025445919430765622`, 0.036849114188047614`,
    0.05719996518512964`, 0.088150995382688 09`, 0.136268498594186 2`, 0.203472695823 01`},
   {0.09733778958447 65`, 0.056170874964110 07`, 0.027924387240112 71`, 0.009027004565180163`, 0.001353531265829829 8`, 0.003256449471386801 4`, 0.009728750968942476`,
    0.015254105943578 92`, 0.016484520313841903`, 0.013422943360241 22`, 0.008553542697968649`, 0.004951023889327314`, 0.004603719080503594`, 0.007638308881512801`,
    0.012826172975756452`, 0.018199230529340315`, 0.022428365448428 63`, 0.025063273097207274`, 0.026799921537536273`, 0.029448819583907347`, 0.035483960079660 41`,
    0.04821943245475934`, 0.072217748429051 29`, 0.113317235279656 08`, 0.179623718161832 26`},
   {0.00151828522681 36`, 0.003466030979520069`, 0.000186653656011 3916`, 0.001236512801140 5636`, 0.001051700016645 7091`, 0.000147080802019 16306`,
    0.001157762784982 8208`, 0.000305178039866 7695`, 0.000548968107260561`, 0.000855370865516 4775`, 0.000189517722550 61536`, 0.000907471911511 67899`,
    0.000526901496342938`, 0.000534284007166 9367`, 0.001057799055014 1242`, 0.000482687619373 02724`, 0.001168851469798 318`, 0.001125296969517 799`,
    0.001073614927403 9742`, 0.002002705765010564`, 0.001665466290776 6784`, 0.002777825729508 1065`, 0.003570335952483 4476`, 0.003852846347364 9945`, 0.006435383561831465`}};
```

Reflection

Axial reflection (Negligible)

```
apt2A = Table[axial2[25, 100], 1]; "Input R,z. Reflected length";
apt2B = Re[apt2A]^2 + Im[apt2A]^2
apt2C = absB[100] * apt2B
apttotal = apt1C
```

Radial reflection (Negligible)

```
rpt2A = Table[radial2[x, 25, 25], {x, 1, 25}]; "Input R,z. Reflected depth";
rpt2B = Re[rpt2A]^2 + Im[rpt2A]^2
rpt2C = absB[100] * rpt2B
rpttotal = rpt1C
```

Figure making

Aerial images

```
rdata = Reverse[rpt1B];
jdataA = Join[rdata, apt1B, rpt1B]; "For ListLinePlot";
jdataB = Join[apt1B, rpt1B];
int = ListInterpolation[jdataB, {0, 25}];
```

Latent images

Exposure dose data

```
In[81]:= EDose = 1700;
         jdata2 = Join[apt1DeSave, rpt1DeSave, 2] ;
         Etable = EDose * jdata2 / CED ;
         Etable2 = EDose * jdata2 - CED;
```

EptsX

```
In[85]:= EptsX = UnitStep[Etable2];
         Eptse = Table[n - 1, {n, 11, 111}, 26];
         Eptsr = EptsX * (Eptse) - 10;
```

zTables

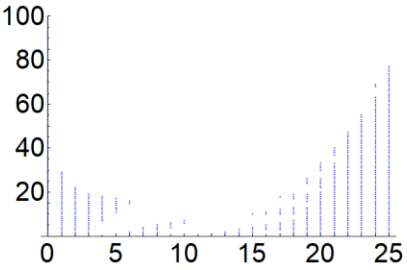
```
In[88]:= rm = RotationMatrix[1. Degree, {0, 0, 1}];
         xycomp = Range[0, 25] * 2^(1/2) / 2;

         xyptsA = Table[{xycomp[[n]], xycomp[[n]]}, {n, 1, 26}];
         xyptsB = Table[xyptsA, 101];
         EptsA = Partition[Eptsr, {1, 1}];
         Cmb1A = Join[xyptsB, EptsA, 3];
         Cmb1B = Partition[Flatten[Join[xyptsB, EptsA, 3]], 3];
```

Latent Images

2D Plot

```
In[95]:= LI2D = ListPlot[Eptsr, PlotRange → 100, DataRange → {0, 25}, PlotStyle → Blue, ImageSize → 450, AxesStyle → Black, TicksStyle → Directive[FontSize → 30], AxesOrigin → {0, 0}]
```

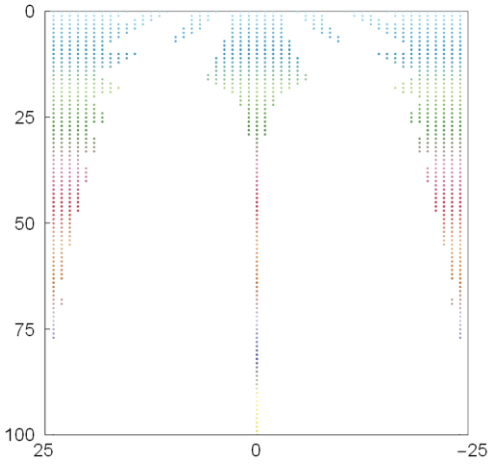
Out[96]=



3D Plot

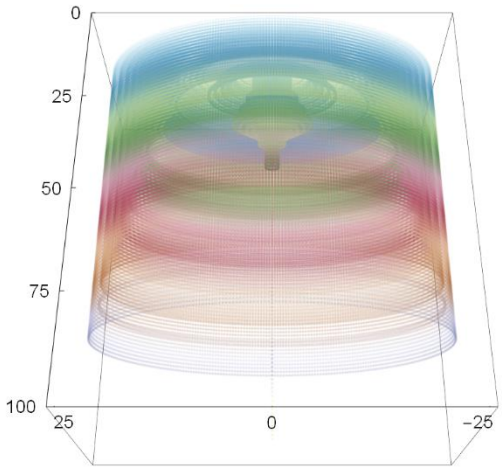
```
In[96]:= LI3DA = ListPointPlot3D[Join @@ NestList[#.rm &, Cmb1B, 359], BoxRatios → Automatic, AxesLabel → {Style["", FontSize → 20], Style["", FontSize → 20], Style["", FontSize → 20, Bold]},
         PlotRange → {{-26, 26}, {-0.1, 0.1}, {0, 100}}, ImageSize → 550, AxesStyle → Black, ColorFunctionScaling → False, ColorFunction → (ColorData[{"DarkBands", {0, 100}}][#3] &),
         AxesEdge -> {{-1, 1}, None, {1, -1}}, TicksStyle → Directive[FontSize → 20], Ticks → {{-25, 0, 25}, {}, {0, 25, 50, 75, 100}}, ViewPoint → Front,
         ViewVertical → {0, 0, -1}, AspectRatio → 1]
```

Out[96]=



```
In[97]:= LI3DB = ListPointPlot3D[Join @@ NestList[#.rm &, Cmb1B, 359], BoxRatios → Automatic, AxesLabel → {Style["", FontSize → 20], Style["", FontSize → 20], Style["", FontSize → 20, Bold]},
  PlotRange → {{-26, 26}, {-26, 26}, {0, 100}}, ImageSize → 550, AxesStyle → Black, ColorFunctionScaling → False, ColorFunction → (ColorData[{"DarkBands", {0, 100}}][#3] &),
  AxesEdge -> {{-1, 1}, None, {1, -1}}, TicksStyle → Directive[FontSize → 20], Ticks → {{-25, 0, 25}, {}, {0, 25, 50, 75, 100}}, ViewPoint → {0, -2, 1},
  PlotStyle → Directive[Opacity[0.25]], ViewVertical → {0, 0, -1}, AspectRatio → 1]
```

Out[97]=

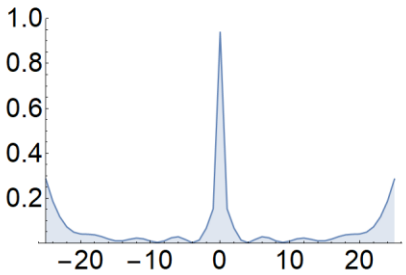


Aerial Images (Single Height)

2D Plot

```
In[98]:= AI2D = ListLinePlot[jdataA, DataRange → {-25, 25}, PlotRange → 1, Filling → Axis, ImageSize → 450, AxesStyle → Black, AxesLabel → {Style["", FontSize → 20], Style["", FontSize → 20]},
  TicksStyle → Directive[FontSize → 30], AxesOrigin → {-25, 0}, Ticks → {Automatic, 5}]
```

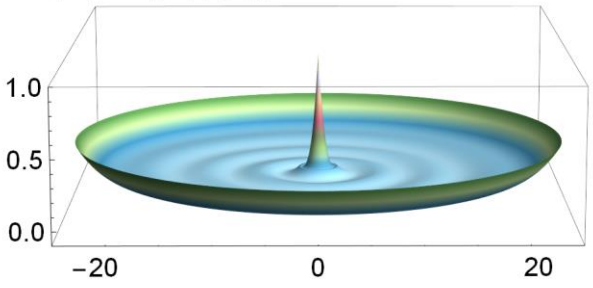
Out[98]=



3D Plot

```
In[99]:= AI3D = RevolutionPlot3D[{int[x]}, {x, 0, 25}, PlotRange → {{-25, 25}, {-25, 25}, {-0.1, 1}}, ImageSize → 650, AxesStyle → Black,
  AxesLabel → {Style["", FontSize → 20], Style["", FontSize → 20], Style["", FontSize → 20, Bold]}, TicksStyle → Directive[FontSize → 30], Mesh → None,
  PlotPoints → 150, ColorFunctionScaling → False, ColorFunction → (ColorData[{"DarkBands", {0, 1}}][#3] &), ViewPoint → {0, -5, 1}, Axes → True,
  AxesEdge -> {Automatic, None, {-1, -1}}]
```

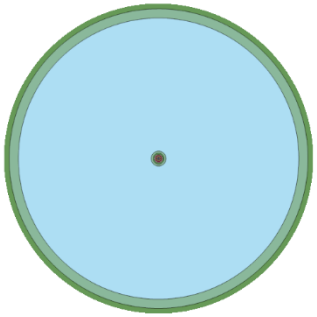
Out[99]=



2D Contour

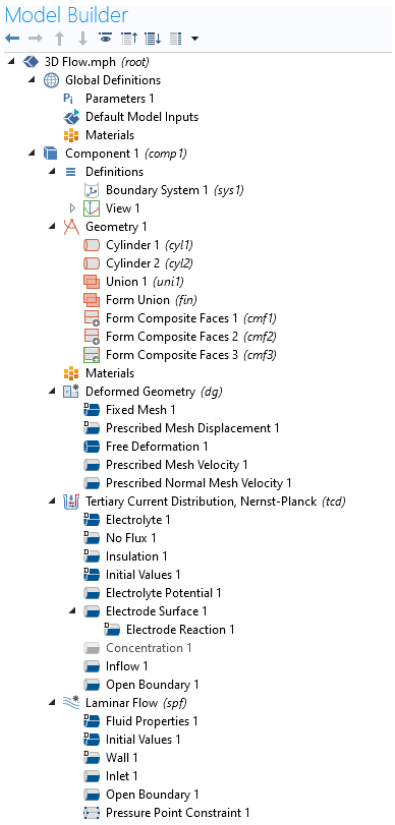
```
In[100]:= ListContourPlot[AI3D[[1, 1]], ColorFunctionScaling → False, ColorFunction → (ColorData[{"DarkBands", {0, 1}}]), PlotRange → All, Frame → False]
```

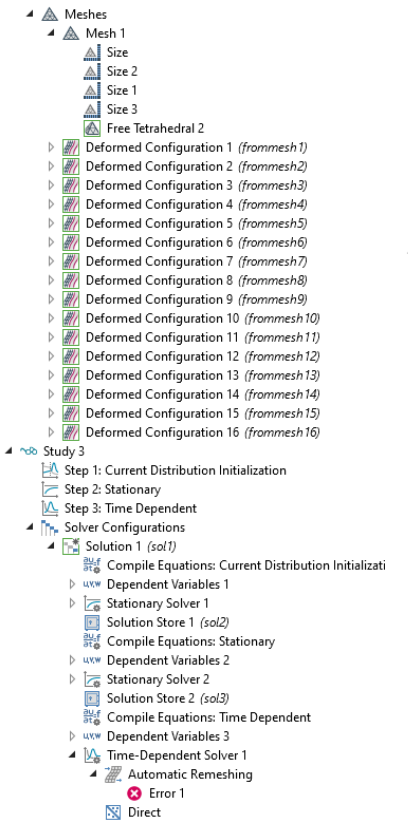
Out[100]=

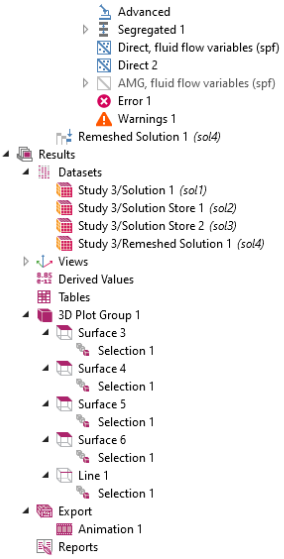


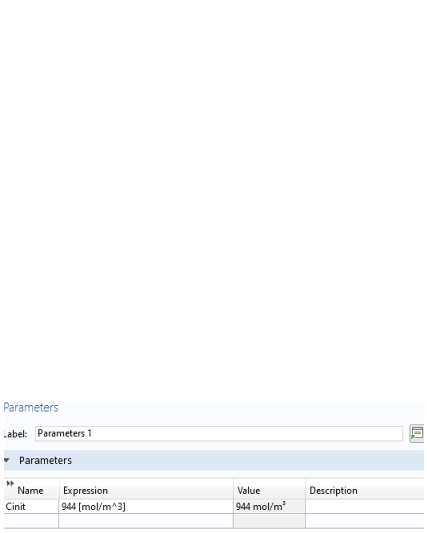
Appendix III: COMSOL simulations

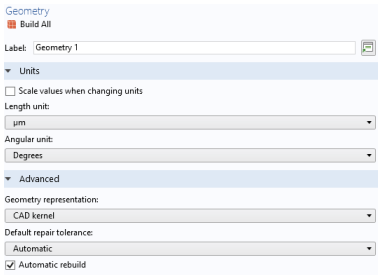
This section shows the settings that I used in COMSOL Multiphysics. This example is for a multiphysics couple between the TCD, LF and DG physics modules. The model builder is first presented, which is followed by the detailed settings for each module option. Where relevant, the geometry has also been included.



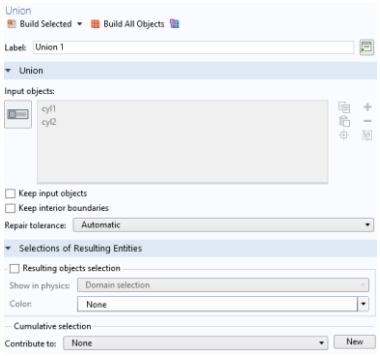




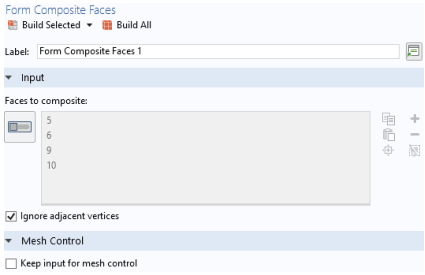


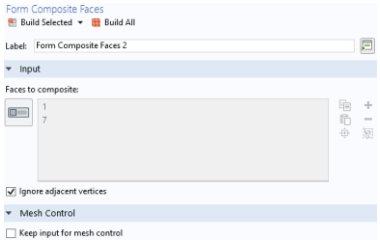


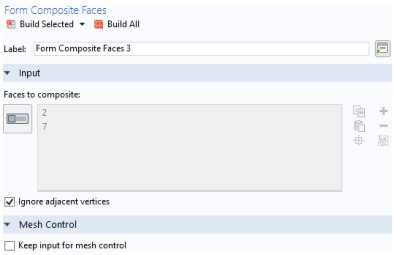

Cylinder
Build Selected
Build All Objects
Label: Cylinder 2
Object Type
Type: Solid
Size and Shape
Radius: 50 µm
Height: 100 µm
Position
x: 0 µm
y: 0 µm
z: -100 µm
Axis
Axis type: z-axis
Rotation Angle
Rotation: 0 deg
Coordinate System
Work plane: xy-plane
Layers
Selections of Resulting Entities
Resulting objects selection
Show in physics: Domain selection
Color: None
Cumulative selection
Contribute to: None
New

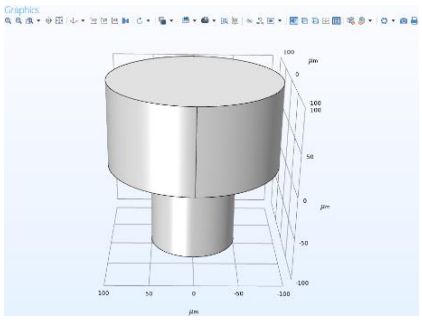

Union
Build Selected
Build All Objects
Label: Union 1
Union
Input objects:
cyl1
cyl2
Keep input objects
Keep interior boundaries
Repair tolerance: Automatic
Selections of Resulting Entities
Resulting objects selection
Show in physics: Domain selection
Color: None
Cumulative selection
Contribute to: None
New

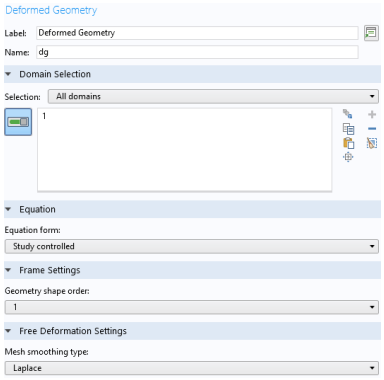

Form Union/Assembly
Build Selected
Build All
Label: Form Union
Form Union/Assembly
Action:
Form a union
Repair tolerance:
Automatic

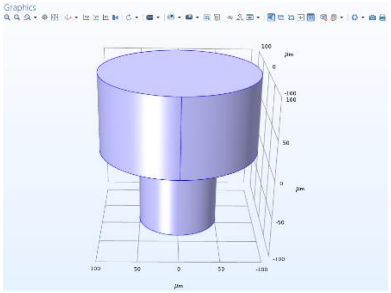

Form Composite Faces
Build Selected
Build All
Label: Form Composite Faces 1
Input
Faces to composite:
5
6
9
10
Ignore adjacent vertices
Mesh Control
Keep input for mesh control


Form Composite Faces
Build Selected
Build All
Label: Form Composite Faces 2
Input
Faces to composite:
1
7
Ignore adjacent vertices
Mesh Control
Keep input for mesh control

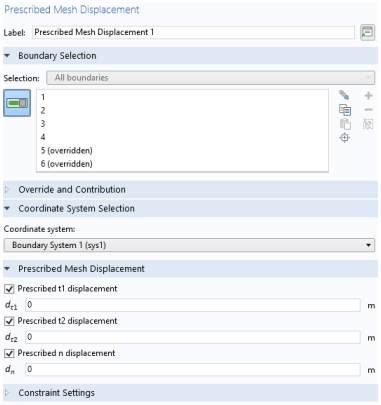

Form Composite Faces
Build Selected
Build All
Label: Form Composite Faces 3
Input
Faces to composite:
2
7
Ignore adjacent vertices
Mesh Control
Keep input for mesh control

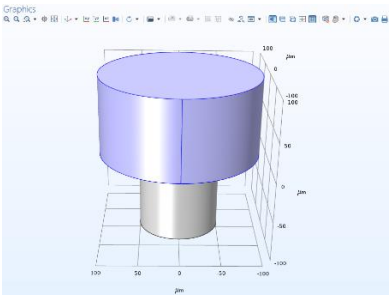

Graphics

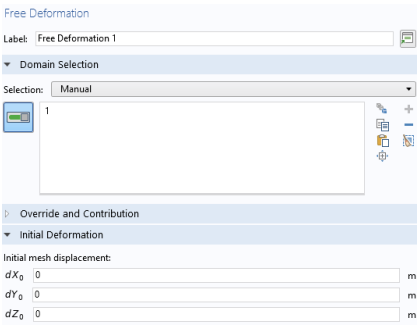

Deformed Geometry
Label: Deformed Geometry
Name: dg
Domain Selection
Selection: All domains
1
Equation
Equation form:
Study controlled
Frame Settings
Geometry shape order:
1
Free Deformation Settings
Mesh smoothing type:
Laplace

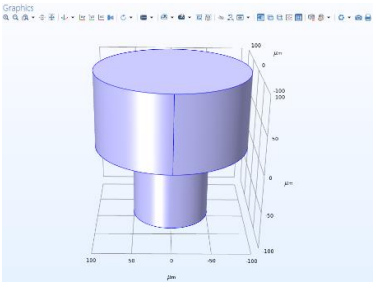

Graphics

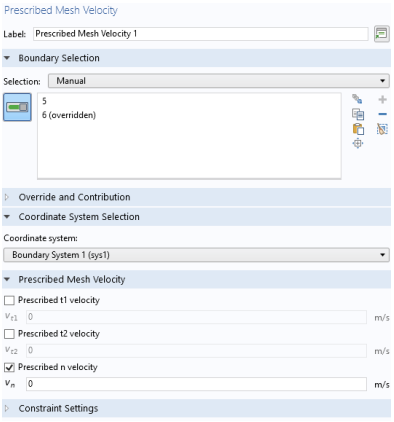

Fixed Mesh
Label: Fixed Mesh 1
Domain Selection
Selection: All domains
1 (overridden)
Override and Contribution

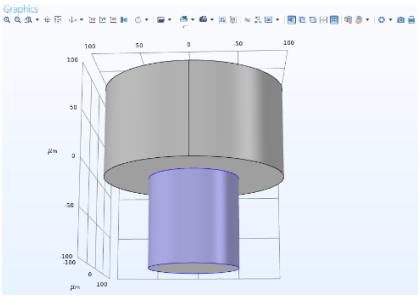

Prescribed Mesh Displacement
Label: Prescribed Mesh Displacement 1
Boundary Selection
Selection: All boundaries
1
2
3
4
5 (overridden)
6 (overridden)
Override and Contribution
Coordinate System Selection
Coordinate system:
Boundary System 1 (sys1)
Prescribed Mesh Displacement
Prescribed t1 displacement
Prescribed t2 displacement
Prescribed n displacement
Constraint Settings

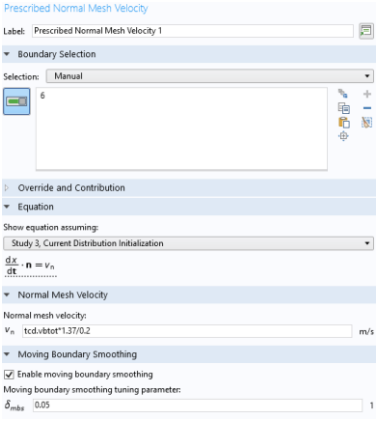

Graphics

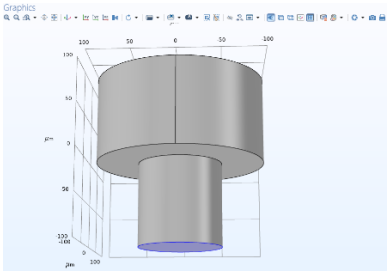

Free Deformation
Label: Free Deformation 1
Domain Selection
Selection: Manual
1
Override and Contribution
Initial Deformation
Initial mesh displacement:


Graphics


Prescribed Mesh Velocity
Label: Prescribed Mesh Velocity 1
Boundary Selection
Selection: Manual
5
6 (overridden)
Override and Contribution
Coordinate System Selection
Coordinate system:
Boundary System 1 (sys1)
Prescribed Mesh Velocity
Prescribed t1 velocity
Prescribed t2 velocity
Prescribed n velocity
Constraint Settings


Graphics


Prescribed Normal Mesh Velocity
Label: Prescribed Normal Mesh Velocity 1
Boundary Selection
Selection: Manual
6
Override and Contribution
Equation
Show equation assuming:
Study 3, Current Distribution Initialization
Normal Mesh Velocity
Normal mesh velocity:
tcd.vbtot*1.37/0.2
Moving Boundary Smoothing
Enable moving boundary smoothing
Moving boundary smoothing tuning parameter:
0.05


Graphics

Tertiary Current Distribution, Nernst-Planck

Label: Tertiary Current Distribution, Nernst-Planck
Name: tcd

Domain Selection
Selection: All domains
1

Equation

Electrolyte Charge Conservation
Charge conservation model:
Supporting electrolyte

Consistent Stabilization
Electrolyte equations
Streamline diffusion
Crosswind diffusion
Crosswind diffusion type:
Do Carmo and Galeão
Equation residual:
Approximate residual
Species transport on boundaries
Streamline diffusion

Inconsistent Stabilization
Electrolyte equations
Isotropic diffusion
Species transport on boundaries
Isotropic diffusion

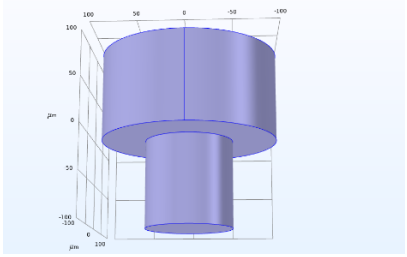
Advanced Settings
Convective term:
Nonconservative form

Discretization
Concentration:
Quadratic
Compute boundary fluxes
Apply smoothing to boundary fluxes
Electrolyte potential:
Quadratic
Compute boundary fluxes
Apply smoothing to boundary fluxes
Electric potential:
Quadratic
Compute boundary fluxes
Apply smoothing to boundary fluxes
Value types when using splitting of complex variables

Dependent variable	Value type
Concentration	Complex
Electrolyte potential	Complex
Electric potential	Complex

Dependent Variables
Number of species: 1
Concentrations: c1
Electrolyte potential: phil
Electric potential: phis

Graphics



Electrolyte

Label: Electrolyte 1

Domain Selection
Selection: All domains
1

Override and Contribution
Equation

Model Input
Temperature:
T User defined
293.15[K] K

Coordinate System Selection
Coordinate system:
Global coordinate system

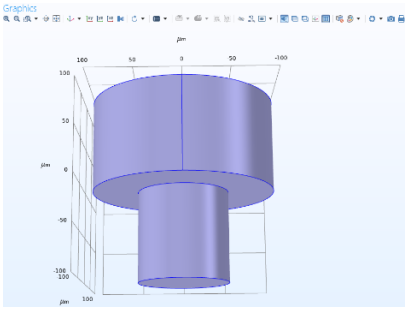
Convection
Velocity field:
u Velocity field (spf)

Diffusion
Material:
None
Diffusion coefficient:
D_{c1} User defined
4.2E-11 m²/s
Isotropic

Migration in Electric Field
Mobility:
Nernst-Einstein relation
$u_{m,i} = \frac{D_i}{RT}$
Charge number:
z_{c1} 1 1

Electrolyte Current Conduction
Electrolyte conductivity:
σ_l User defined
5.591 S/m
Isotropic

Graphics



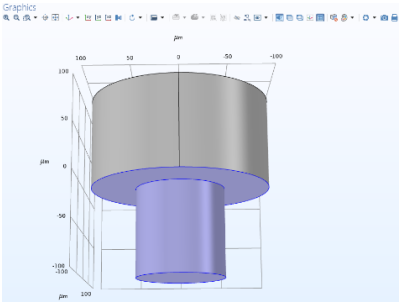
No Flux

Label: No Flux 1

Boundary Selection
Selection: All boundaries
1 (overridden)
2 (overridden)
3
4 (overridden)
5
6

Override and Contribution
Equation
Convection
Include

Graphics

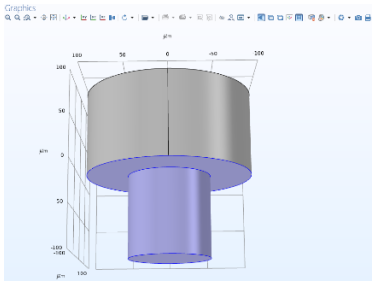


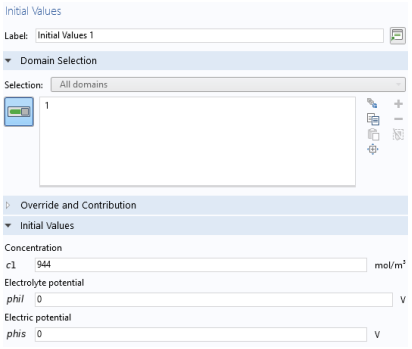
Insulation

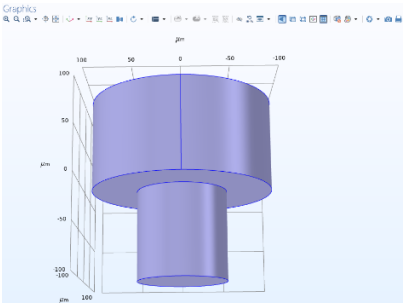
Label: Insulation 1

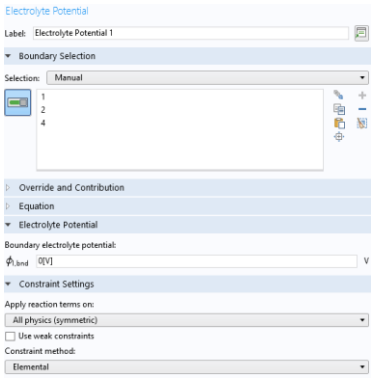
Boundary Selection
Selection: All boundaries
1 (overridden)
2 (overridden)
3
4 (overridden)
5
6 (overridden)

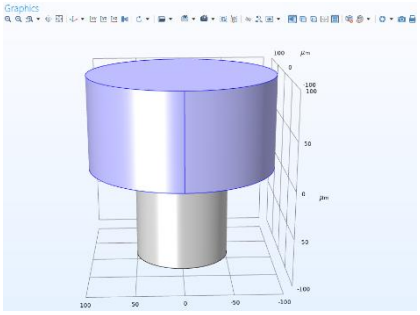
Override and Contribution
Equation

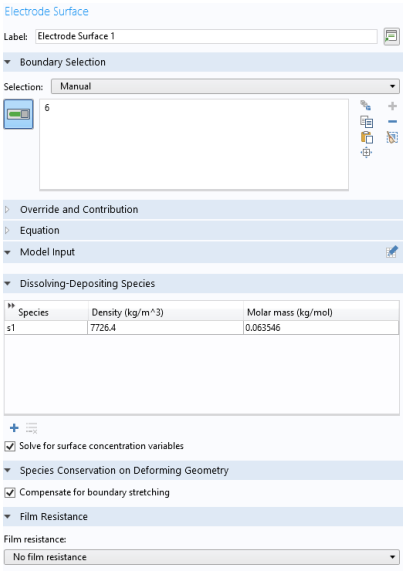


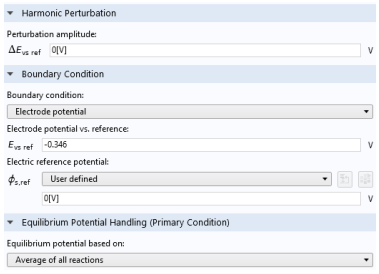

Initial Values
Label: Initial Values 1
Domain Selection
Selection: All domains
1
Override and Contribution
Initial Values
Concentration
c1 944 mol/m³
Electrolyte potential
phil 0 V
Electric potential
phis 0 V

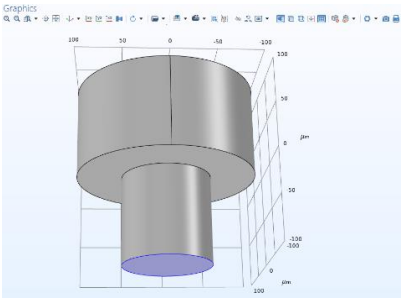


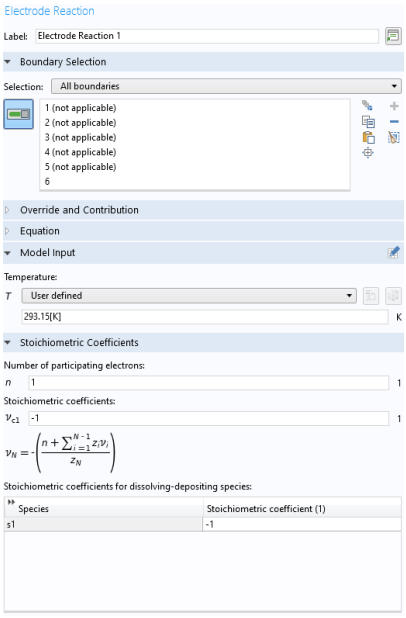

Electrolyte Potential
Label: Electrolyte Potential 1
Boundary Selection
Selection: Manual
1
2
4
Override and Contribution
Equation
Electrolyte Potential
Boundary electrolyte potential:
0[V] V
Constraint Settings
Apply reaction terms on:
All physics (symmetric)
Use weak constraints
Constraint method:
Elemental

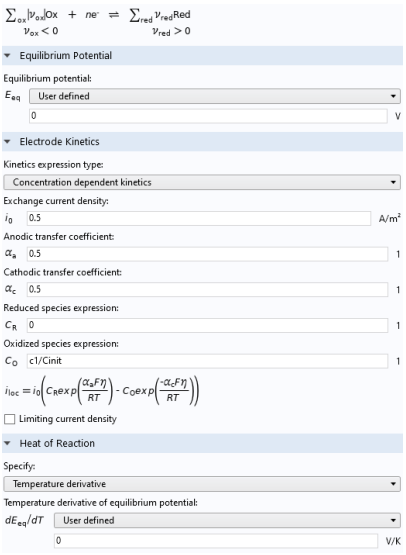


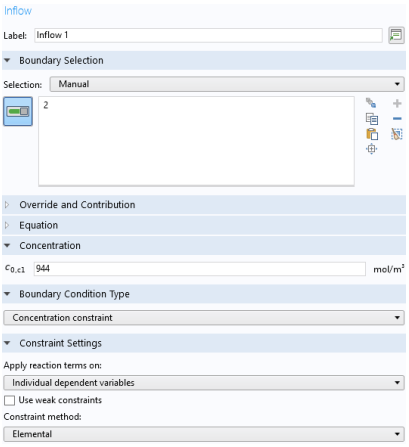

Electrode Surface
Label: Electrode Surface 1
Boundary Selection
Selection: Manual
6
Override and Contribution
Equation
Model Input
Dissolving-Depositing Species
Species | Density (kg/m^3) | Molar mass (kg/mol)
s1 | 7726.4 | 0.063546
Solve for surface concentration variables
Species Conservation on Deforming Geometry
Compensate for boundary stretching
Film Resistance
Film resistance:
No film resistance

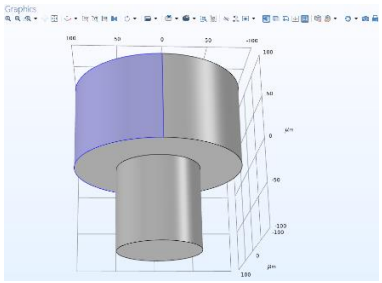

Harmonic Perturbation
Perturbation amplitude:
ΔE_vs ref 0[V] V
Boundary Condition
Boundary condition:
Electrode potential
Electrode potential vs. reference:
E_vs ref -0.346 V
Electric reference potential:
φ_s,ref User defined
0[V] V
Equilibrium Potential Handling (Primary Condition)
Equilibrium potential based on:
Average of all reactions

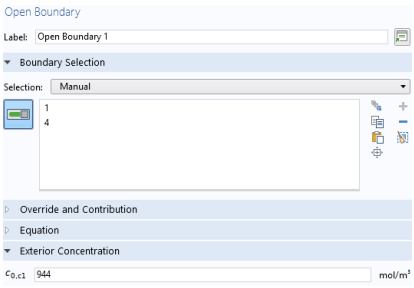


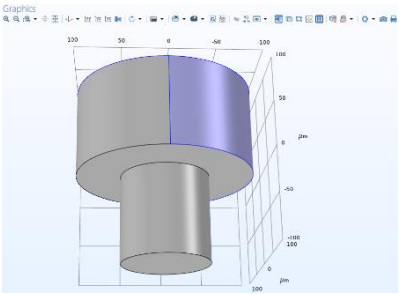

Electrode Reaction
Label: Electrode Reaction 1
Boundary Selection
Selection: All boundaries
1 (not applicable)
2 (not applicable)
3 (not applicable)
4 (not applicable)
5 (not applicable)
6
Override and Contribution
Equation
Model Input
Temperature:
T User defined
293.15[K] K
Stoichiometric Coefficients
Number of participating electrons:
n 1 1
Stoichiometric coefficients:
ν_c1 -1 1
ν_N = -((n + Σ_{i=1}^{N-1} z_i ν_i) / z_N)
Stoichiometric coefficients for dissolving-depositing species:
Species | Stoichiometric coefficient (1)
s1 | -1

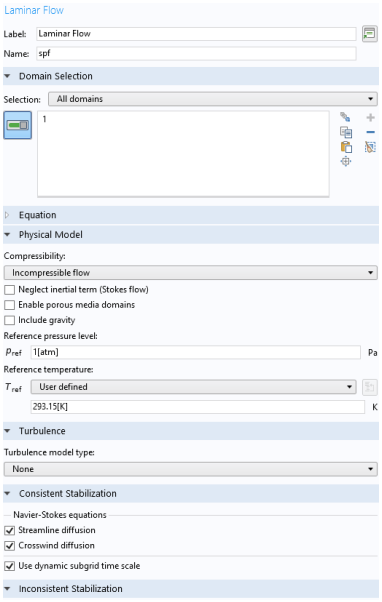

Equilibrium Potential
Equilibrium potential:
User defined
0
V
Electrode Kinetics
Kinetics expression type:
Concentration dependent kinetics
Exchange current density:
0.5
A/m²
Anodic transfer coefficient:
0.5
Cathodic transfer coefficient:
0.5
Reduced species expression:
0
Oxidized species expression:
c1/Cinit
Limiting current density
Heat of Reaction
Specify:
Temperature derivative
Temperature derivative of equilibrium potential:
User defined
0
V/K

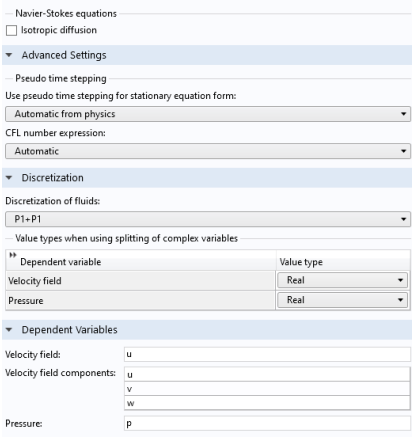

Inflow
Label: Inflow 1
Boundary Selection
Selection: Manual
2
Override and Contribution
Equation
Concentration
944
mol/m³
Boundary Condition Type
Concentration constraint
Constraint Settings
Apply reaction terms on:
Individual dependent variables
Use weak constraints
Constraint method:
Elemental

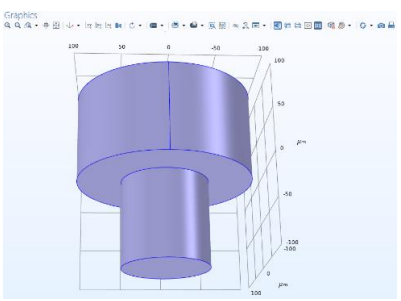

Graphics

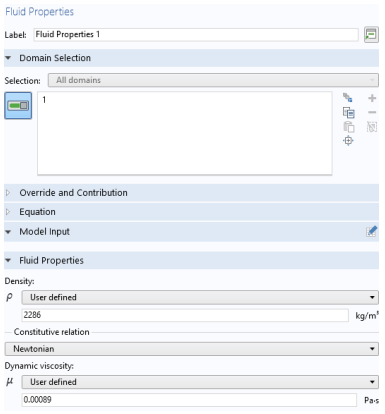

Open Boundary
Label: Open Boundary 1
Boundary Selection
Selection: Manual
1
4
Override and Contribution
Equation
Exterior Concentration
944
mol/m³

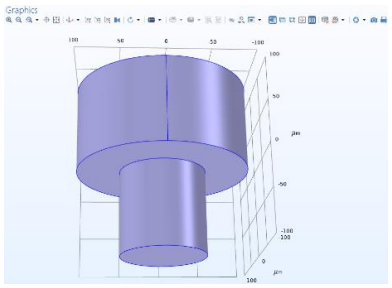

Graphics

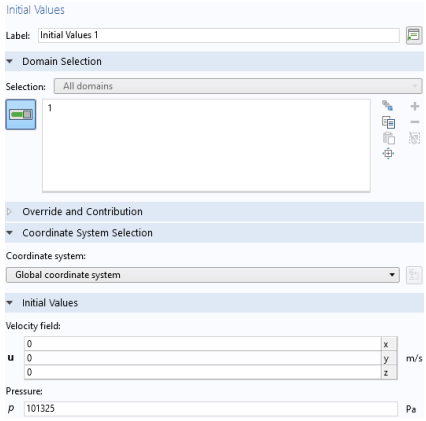

Laminar Flow
Label: Laminar Flow
Name: spf
Domain Selection
Selection: All domains
1
Equation
Physical Model
Compressibility:
Incompressible flow
Neglect inertial term (Stokes flow)
Enable porous media domains
Include gravity
Reference pressure level:
1[atm]
Pa
Reference temperature:
User defined
293.15[K]
K
Turbulence
Turbulence model type:
None
Consistent Stabilization
Navier-Stokes equations
Streamline diffusion
Crosswind diffusion
Use dynamic subgrid time scale
Inconsistent Stabilization

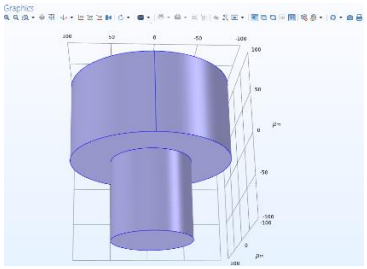

Navier-Stokes equations
Isotropic diffusion
Advanced Settings
Pseudo time stepping
Use pseudo time stepping for stationary equation form:
Automatic from physics
CFL number expression:
Automatic
Discretization
Discretization of fluids:
P1+P1
Value types when using splitting of complex variables
Dependent variable
Value type
Velocity field
Real
Pressure
Real
Dependent Variables
Velocity field:
u
Velocity field components:
u
v
w
Pressure:
p

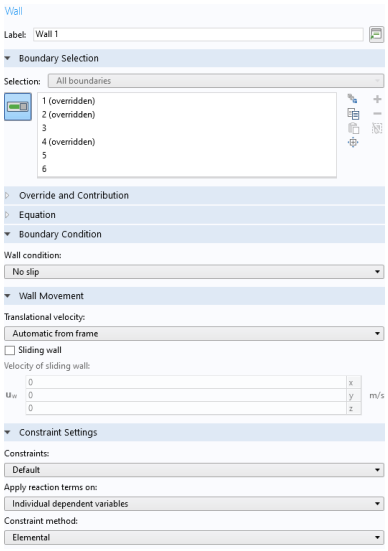

Graphics

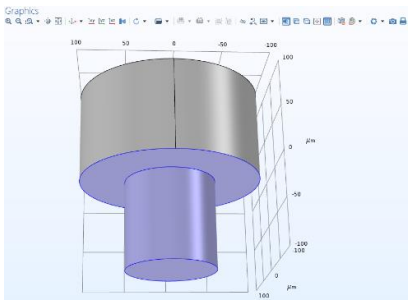

Fluid Properties
Label: Fluid Properties 1
Domain Selection
Selection: All domains
1
Override and Contribution
Equation
Model Input
Fluid Properties
Density:
User defined
2286
kg/m³
Constitutive relation
Newtonian
Dynamic viscosity:
User defined
0.00089
Pa·s

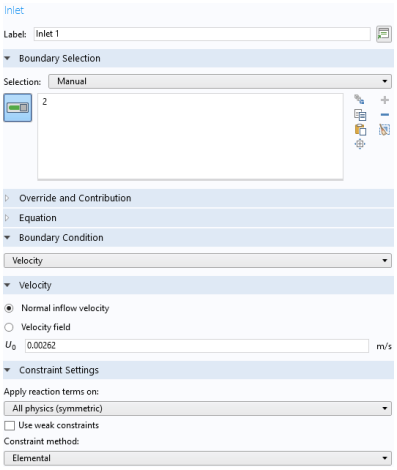


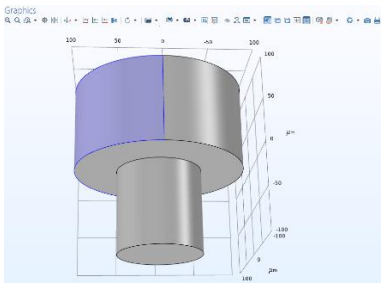

Initial Values
Label: Initial Values 1
Domain Selection
Selection: All domains
1
Override and Contribution
Coordinate System Selection
Coordinate system:
Global coordinate system
Initial Values
Velocity field:
u
m/s
Pressure:
p
101325
Pa

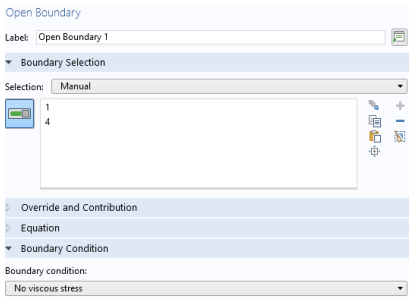


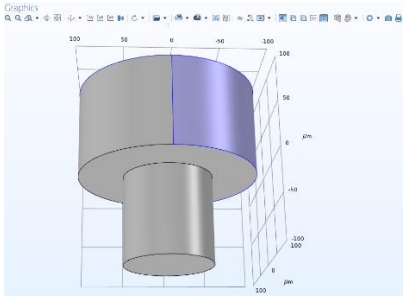

Wall
Label: Wall 1
Boundary Selection
Selection: All boundaries
1 (overridden)
2 (overridden)
3
4 (overridden)
5
6
Override and Contribution
Equation
Boundary Condition
Wall condition:
No slip
Wall Movement
Translational velocity:
Automatic from frame
Sliding wall
Velocity of sliding wall:
m/s
Constraint Settings
Constraints:
Default
Apply reaction terms on:
Individual dependent variables
Constraint method:
Elemental

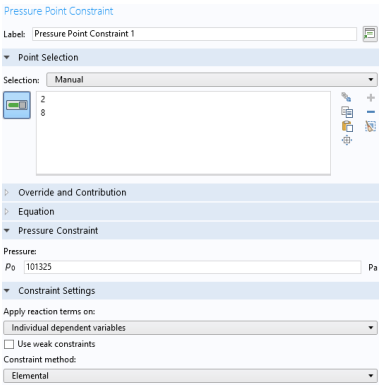


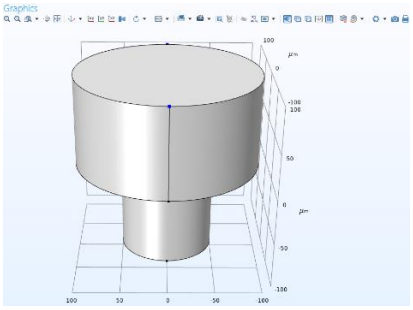

Inlet
Label: Inlet 1
Boundary Selection
Selection: Manual
2
Override and Contribution
Equation
Boundary Condition
Velocity
Velocity
Normal inflow velocity
Velocity field
U_0
0.00262
m/s
Constraint Settings
Apply reaction terms on:
All physics (symmetric)
Use weak constraints
Constraint method:
Elemental

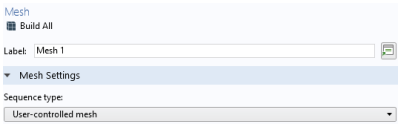


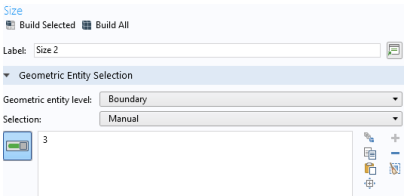

Open Boundary
Label: Open Boundary 1
Boundary Selection
Selection: Manual
1
4
Override and Contribution
Equation
Boundary Condition
Boundary condition:
No viscous stress

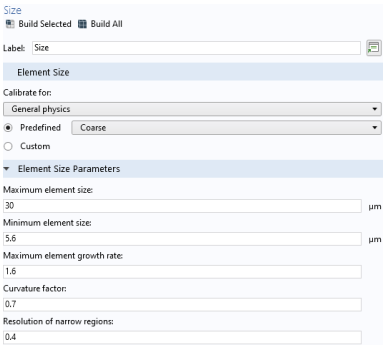


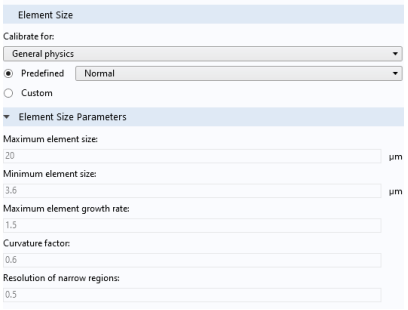

Pressure Point Constraint
Label: Pressure Point Constraint 1
Point Selection
Selection: Manual
2
8
Override and Contribution
Equation
Pressure Constraint
Pressure:
p0 101325 Pa
Constraint Settings
Apply reaction terms on:
Individual dependent variables
Use weak constraints
Constraint method:
Elemental

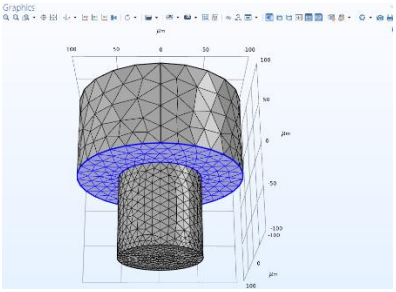

Graphics

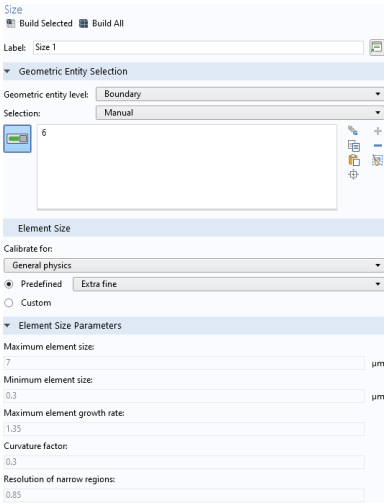

Mesh
Build All
Label: Mesh 1
Mesh Settings
Sequence type:
User-controlled mesh

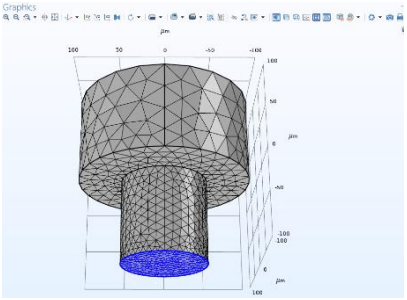

Size
Build Selected
Build All
Label: Size 2
Geometric Entity Selection
Geometric entity level: Boundary
Selection: Manual
3

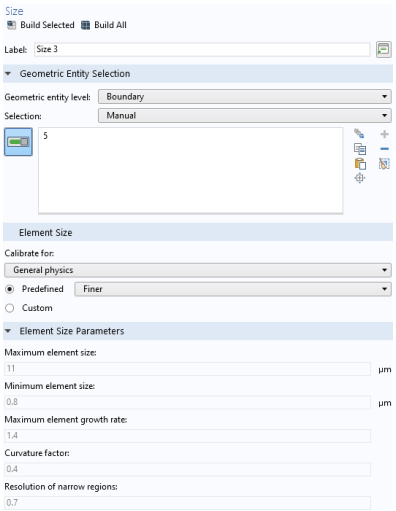

Size
Build Selected
Build All
Label: Size
Element Size
Calibrate for:
General physics
Predefined
Coarse
Custom
Element Size Parameters
Maximum element size:
30 µm
Minimum element size:
5.6 µm
Maximum element growth rate:
1.6
Curvature factor:
0.7
Resolution of narrow regions:
0.4

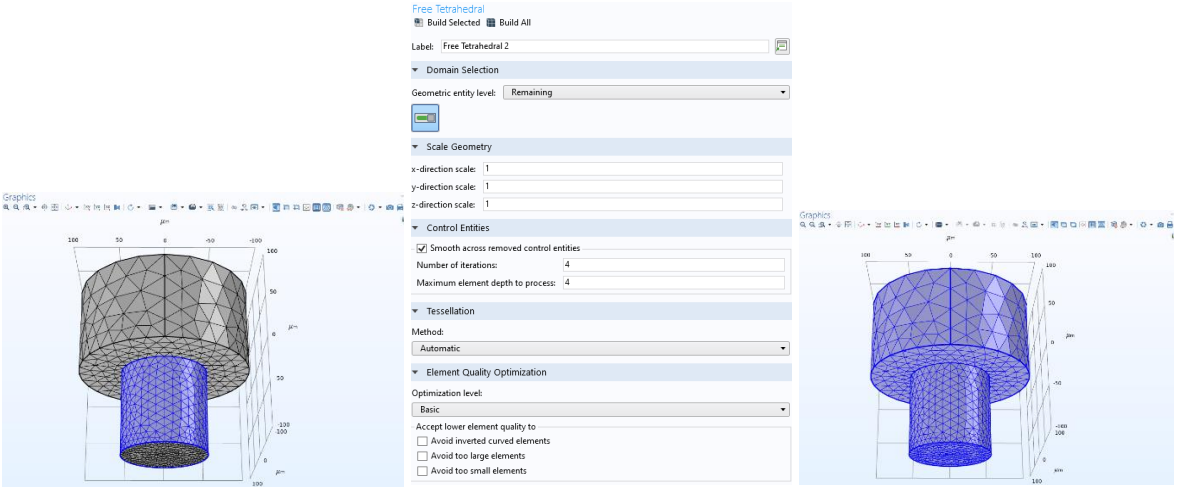

Element Size
Calibrate for:
General physics
Predefined
Normal
Custom
Element Size Parameters
Maximum element size:
20 µm
Minimum element size:
3.6 µm
Maximum element growth rate:
1.5
Curvature factor:
0.6
Resolution of narrow regions:
0.5

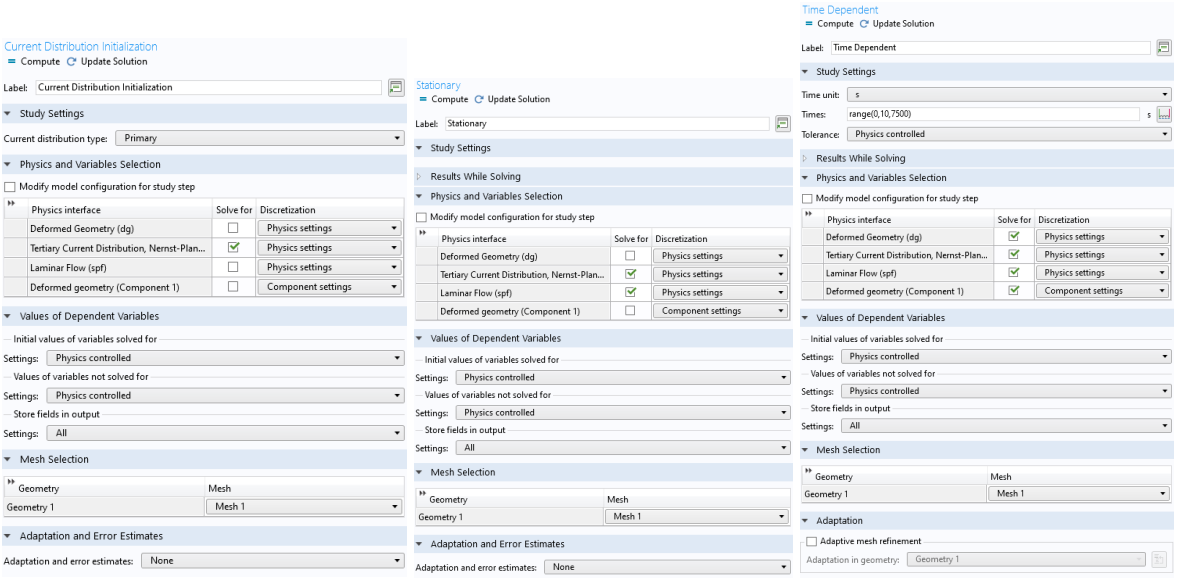

Graphics

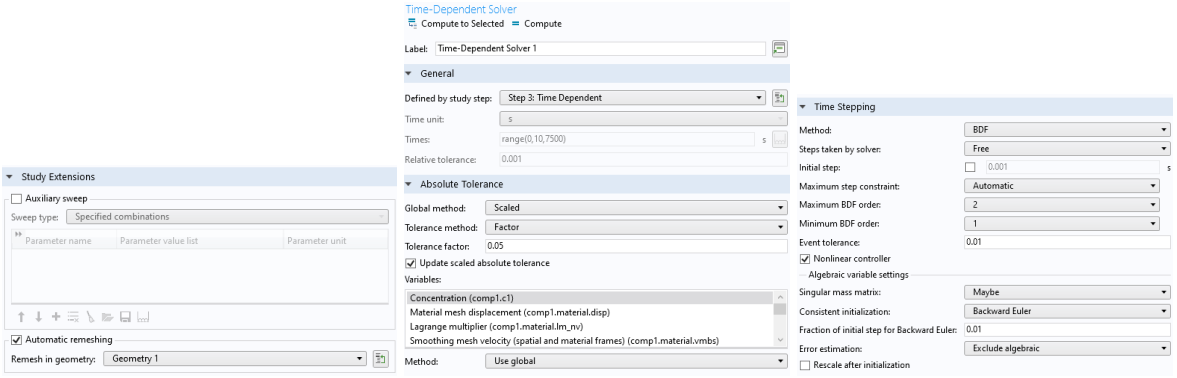

Size
Build Selected
Build All
Label: Size 1
Geometric Entity Selection
Geometric entity level: Boundary
Selection: Manual
6
Element Size
Calibrate for:
General physics
Predefined
Extra fine
Custom
Element Size Parameters
Maximum element size:
7 µm
Minimum element size:
0.3 µm
Maximum element growth rate:
1.35
Curvature factor:
0.3
Resolution of narrow regions:
0.85

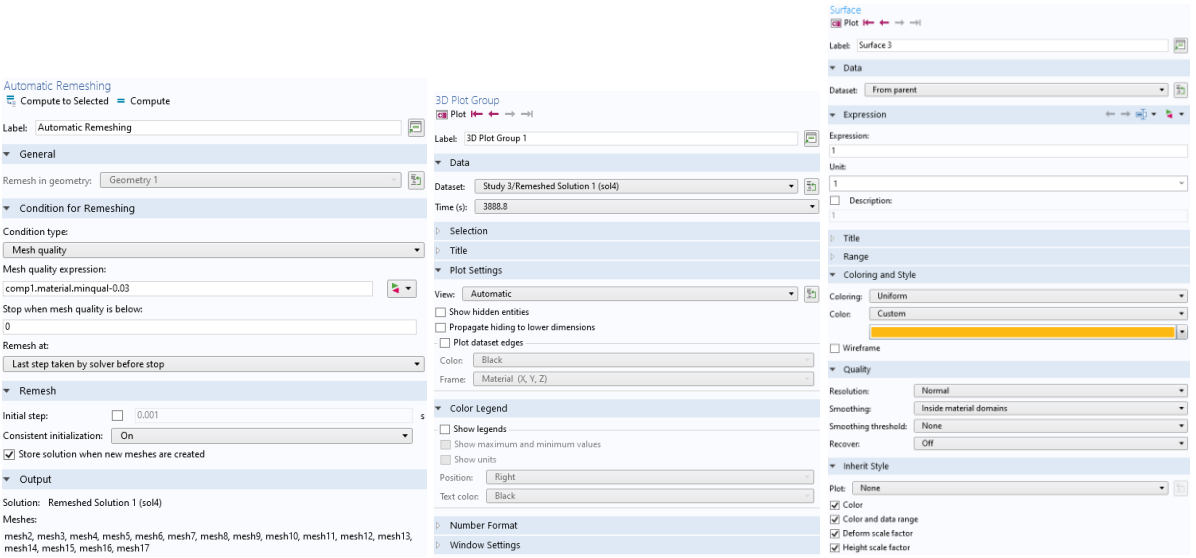

Graphics

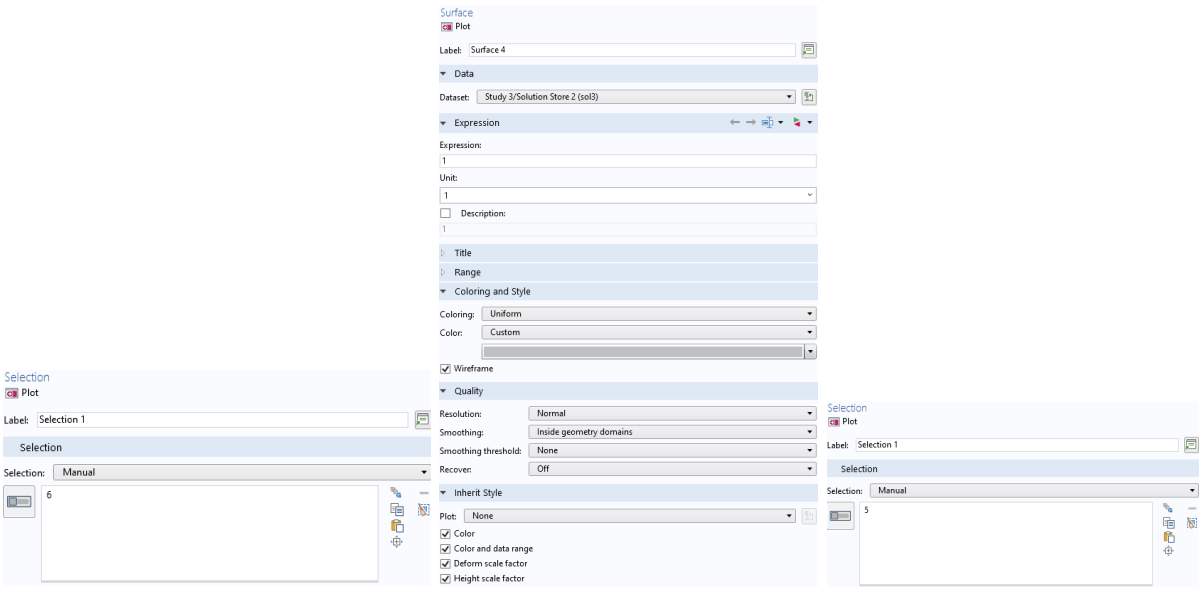

Size
Build Selected
Build All
Label: Size 3
Geometric Entity Selection
Geometric entity level: Boundary
Selection: Manual
5
Element Size
Calibrate for:
General physics
Predefined
Finer
Custom
Element Size Parameters
Maximum element size:
11 µm
Minimum element size:
0.8 µm
Maximum element growth rate:
1.4
Curvature factor:
0.4
Resolution of narrow regions:
0.7

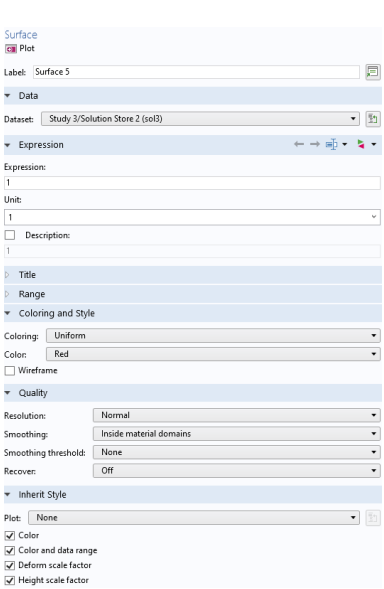

Free Tetrahedral
Build Selected
Build All
Label: Free Tetrahedral 2
Domain Selection
Geometric entity level: Remaining
Scale Geometry
x-direction scale: 1
y-direction scale: 1
z-direction scale: 1
Control Entities
Smooth across removed control entities
Number of iterations: 4
Maximum element depth to process: 4
Tessellation
Method:
Automatic
Element Quality Optimization
Optimization level:
Basic
Accept lower element quality to
Avoid inverted curved elements
Avoid too large elements
Avoid too small elements
Graphics
Graphics


Current Distribution Initialization
Compute
Update Solution
Label: Current Distribution Initialization
Study Settings
Current distribution type: Primary
Physics and Variables Selection
Modify model configuration for study step
Physics interface
Solve for
Discretization
Deformed Geometry (dg)
Physics settings
Tertiary Current Distribution, Nernst-Plan...
Physics settings
Laminar Flow (spf)
Physics settings
Deformed geometry (Component 1)
Component settings
Values of Dependent Variables
Initial values of variables solved for
Settings: Physics controlled
Values of variables not solved for
Settings: Physics controlled
Store fields in output
Settings: All
Mesh Selection
Geometry
Mesh
Geometry 1
Mesh 1
Adaptation and Error Estimates
Adaptation and error estimates: None
Stationary
Compute
Update Solution
Label: Stationary
Study Settings
Results While Solving
Physics and Variables Selection
Modify model configuration for study step
Physics interface
Solve for
Discretization
Deformed Geometry (dg)
Physics settings
Tertiary Current Distribution, Nernst-Plan...
Physics settings
Laminar Flow (spf)
Physics settings
Deformed geometry (Component 1)
Component settings
Values of Dependent Variables
Initial values of variables solved for
Settings: Physics controlled
Values of variables not solved for
Settings: Physics controlled
Store fields in output
Settings: All
Mesh Selection
Geometry
Mesh
Geometry 1
Mesh 1
Adaptation and Error Estimates
Adaptation and error estimates: None
Time Dependent
Compute
Update Solution
Label: Time Dependent
Study Settings
Time unit: s
Times: range(0,10,7500)
s
Tolerance: Physics controlled
Results While Solving
Physics and Variables Selection
Modify model configuration for study step
Physics interface
Solve for
Discretization
Deformed Geometry (dg)
Physics settings
Tertiary Current Distribution, Nernst-Plan...
Physics settings
Laminar Flow (spf)
Physics settings
Deformed geometry (Component 1)
Component settings
Values of Dependent Variables
Initial values of variables solved for
Settings: Physics controlled
Values of variables not solved for
Settings: Physics controlled
Store fields in output
Settings: All
Mesh Selection
Geometry
Mesh
Geometry 1
Mesh 1
Adaptation
Adaptive mesh refinement
Adaptation in geometry: Geometry 1


Time-Dependent Solver
Compute to Selected
Compute
Label: Time-Dependent Solver 1
General
Defined by study step: Step 3: Time Dependent
Time unit: s
Times: range(0,10,7500)
s
Relative tolerance: 0.001
Absolute Tolerance
Global method: Scaled
Tolerance method: Factor
Tolerance factor: 0.05
Update scaled absolute tolerance
Variables:
Concentration (comp1.c1)
Material mesh displacement (comp1.material.disp)
Lagrange multiplier (comp1.material.lm_nv)
Smoothing mesh velocity (spatial and material frames) (comp1.material.vmbs)
Method: Use global
Time Stepping
Method: BDF
Steps taken by solver: Free
Initial step: 0.001
s
Maximum step constraint: Automatic
Maximum BDF order: 2
Minimum BDF order: 1
Event tolerance: 0.01
Nonlinear controller
Algebraic variable settings
Singular mass matrix: Maybe
Consistent initialization: Backward Euler
Fraction of initial step for Backward Euler: 0.01
Error estimation: Exclude algebraic
Rescale after initialization
Study Extensions
Auxiliary sweep
Sweep type: Specified combinations
Parameter name
Parameter value list
Parameter unit
Automatic remeshing
Remesh in geometry: Geometry 1


Automatic Remeshing
Compute to Selected
Compute
Label: Automatic Remeshing
General
Remesh in geometry: Geometry 1
Condition for Remeshing
Condition type:
Mesh quality
Mesh quality expression:
comp1.material.minqual-0.03
Stop when mesh quality is below:
0
Remesh at:
Last step taken by solver before stop
Remesh
Initial step:
0.001
s
Consistent initialization:
On
Store solution when new meshes are created
Output
Solution: Remeshed Solution 1 (sol4)
Meshes:
mesh2, mesh3, mesh4, mesh5, mesh6, mesh7, mesh8, mesh9, mesh10, mesh11, mesh12, mesh13, mesh14, mesh15, mesh16, mesh17
3D Plot Group
Plot
Label: 3D Plot Group 1
Data
Dataset: Study 3/Remeshed Solution 1 (sol4)
Time (s): 3888.8
Selection
Title
Plot Settings
View: Automatic
Show hidden entities
Propagate hiding to lower dimensions
Plot dataset edges
Color: Black
Frame: Material (X, Y, Z)
Color Legend
Show legends
Show maximum and minimum values
Show units
Position: Right
Text color: Black
Number Format
Window Settings
Surface
Plot
Label: Surface 3
Data
Dataset: From parent
Expression
Expression:
1
Unit:
1
Description:
Title
Range
Coloring and Style
Coloring: Uniform
Color: Custom
Wireframe
Quality
Resolution: Normal
Smoothing: Inside material domains
Smoothing threshold: None
Recover: Off
Inherit Style
Plot: None
Color
Color and data range
Deform scale factor
Height scale factor


Surface
Plot
Label: Surface 4
Data
Dataset: Study 3/Solution Store 2 (sol3)
Expression
Expression:
1
Unit:
1
Description:
Title
Range
Coloring and Style
Coloring: Uniform
Color: Custom
Wireframe
Quality
Resolution: Normal
Smoothing: Inside geometry domains
Smoothing threshold: None
Recover: Off
Inherit Style
Plot: None
Color
Color and data range
Deform scale factor
Height scale factor
Selection
Plot
Label: Selection 1
Selection
Selection: Manual
6
Selection
Plot
Label: Selection 1
Selection
Selection: Manual
5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Color: Red
Wireframe
Quality
Resolution: Normal
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Color
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Height scale factor


Selection
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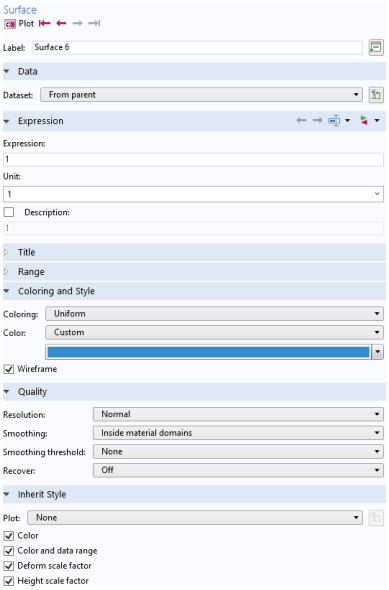
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Color
Color and data range
Deform scale factor
Height scale factor


Selection
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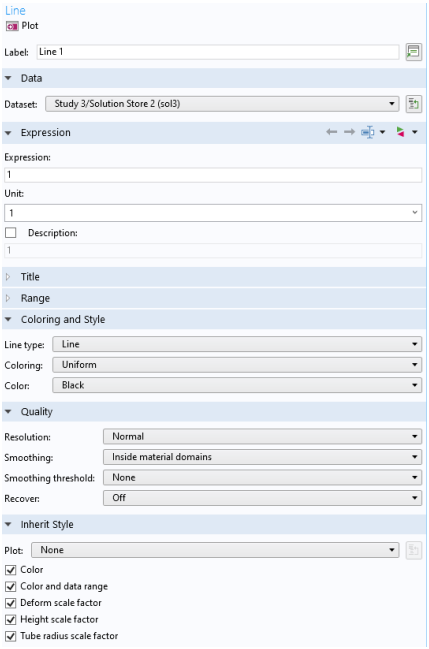
5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8
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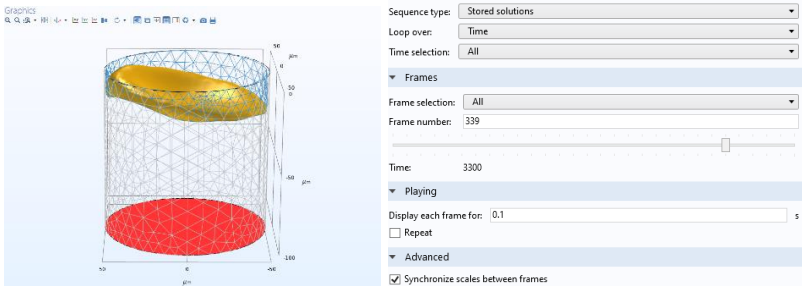
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Target
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Frames
Frame selection: All
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Time: 3300
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Repeat
Advanced
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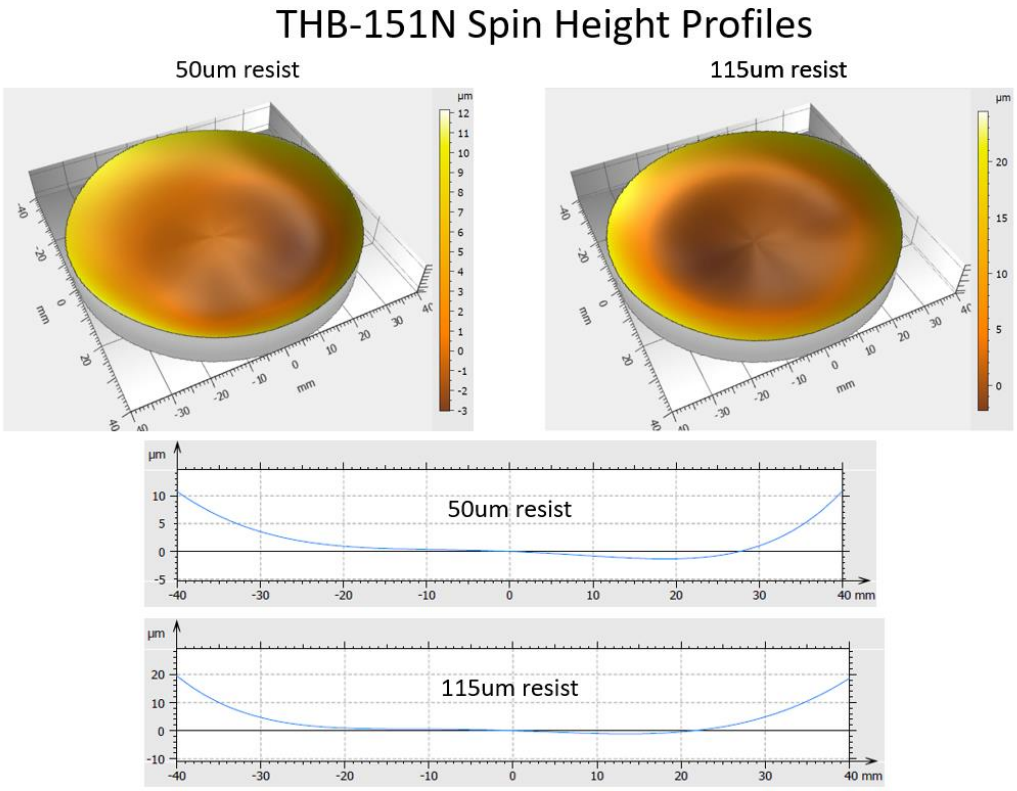
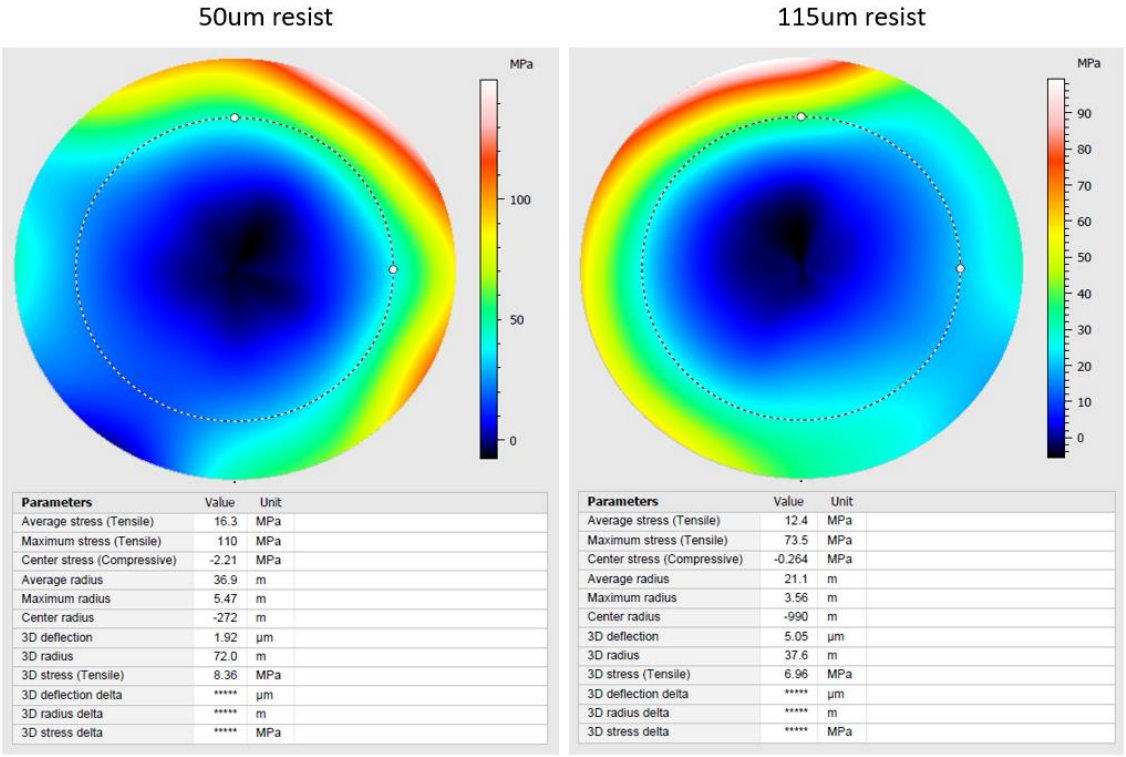
Appendix IV: THB-151N profilometer metrology

This wafer-scale metrology was performed with a Tencor P-17 Stylus Profiler.





Parameters	Value	Unit
Average stress (Tensile)	16.3	MPa
Maximum stress (Tensile)	110	MPa
Center stress (Compressive)	-2.21	MPa
Average radius	36.9	m
Maximum radius	5.47	m
Center radius	-272	m
3D deflection	1.92	µm
3D radius	72.0	m
3D stress (Tensile)	8.36	MPa
3D deflection delta	*****	µm
3D radius delta	*****	m
3D stress delta	*****	MPa

Parameters	Value	Unit
Average stress (Tensile)	12.4	MPa
Maximum stress (Tensile)	73.5	MPa
Center stress (Compressive)	-0.264	MPa
Average radius	21.1	m
Maximum radius	3.56	m
Center radius	-990	m
3D deflection	5.05	µm
3D radius	37.6	m
3D stress (Tensile)	6.96	MPa
3D deflection delta	*****	µm
3D radius delta	*****	m
3D stress delta	*****	MPa

Appendix V: ADEPT patent application

The ADEPT project PCT patent application entitled, “A vertical magnetic structure for integrated power conversion” (No. PCT/EP2019/077978) is included in this section. My contributions to this patent application entail conception, design and description of claims, figures and embodiments. The specification is first included, which is followed by the figures.

Title

A vertical magnetic structure for integrated power conversion

Field

The present invention relates to inductors, coupled inductors and transformers in integrated power converters.

Background

There are many different techniques which are currently being used to fabricate power supplies. Emerging solutions include power supply-in-package (PSiP) and power supply-on-chip (PwrSoC). One such technique is integrated voltage regulator (IVR) technology. IVR technology involves the integration of the power supply with the load either monolithically, in 2.5D/3D, in package or in substrate. IVRs improve the efficiency of power delivery, through elimination of parasitics and a faster transient response. Through miniaturization and integration of magnetic components, the technology removes the need for discrete and bulky magnetics, thereby dramatically reducing the form-factor and footprint of the power conversion circuitry. IVRs also provide the further advantage of a reduced requirement for decoupling capacitors. In addition, IVRs can provide power supply granularity, which can result in a significant increase in power system efficiency.

The major roadblock in realizing an ever increasing number of small integrated dc-dc switching regulators needed in microelectronics applications is due to the size (profile and footprint) of the magnetic passive components. Typically, the micro-fabricated magnetic passive components use four different types of planar structures, namely stripline, spiral, toroid and solenoid. These planar structures are typically fabricated using thin-film processing of magnetic cores and conductor windings.

It is an object of the present invention to provide an inductor structure which overcomes at least one of the above mentioned problems.

Summary

According to one aspect of the invention there is provided, as set out in the appended claims, a transformer or a coupled inductor device comprising:
two interconnected columns of conductive material embedded in a supporting structure, the two interconnected columns comprising a first column and a second column spaced apart from the first column, each column comprising an inner column portion and an outer column portion concentric with the inner column portion,
the outer column portion and the inner column portion each having a first end and a second end, wherein the first end of the first inner column portion and the first outer column portion each comprise an input terminal or an output terminal and the first end of the second inner column portion and the second outer column portion each comprise an input terminal or an output terminal, and wherein the second end of the first inner column portion is conductively coupled to the second end of the second inner column portion by an inner interconnecting track of conductive material, and wherein the second end of the first outer column portion is conductively coupled to the second end of the second outer column portion by an outer interconnecting track of conductive material.

According to another aspect of the invention there is provided a transformer or a coupled inductor device comprising:
three or more interconnected spaced apart columns of conductive material embedded in a supporting structure, the three of more columns comprising an input column, an output column, and at least one intermediate column, each column comprising an inner column portion and an outer column portion concentric with the inner column portion, the outer column portion and the inner column portion each having a first end and a second end, wherein the first end of each intermediate inner column portion is conductively coupled to the first

end of a first adjacent inner column portion by a first inner interconnecting track of conductive material and isolated from the first end of a second adjacent inner column portion, and the second end of each intermediate inner column portion is conductively coupled to the second end of the second adjacent inner column portion by a second inner interconnecting track of conductive material and isolated from the second end of the first adjacent inner column portion; and

wherein the first end of each intermediate outer column portion is conductively coupled to the first end of a first adjacent outer column portion by a first outer interconnecting track of conductive material and isolated from the first end of a second adjacent outer column portion, and the second end of each intermediate outer column portion is conductively coupled to the second end of the second adjacent outer column portion by a second outer interconnecting track of conductive material and isolated from the second end of the first adjacent outer column portion;

wherein each end of an inner column portion and an outer column portion which is not connected to an intermediate column comprises an input terminal or an output terminal.

In one embodiment, the device further comprises a first magnetic layer surrounding each outer column portion.

In one embodiment, the device further comprises a second magnetic layer surrounding each inner column portion.

According to yet another aspect of the invention there is provided an inductor device comprising:

one or more interconnected columns of conductive material embedded in a supporting structure, wherein the one or more columns comprise an input terminal and an output terminal; and wherein each column is surrounded by a first magnetic layer.

In one embodiment, the device further comprises an intervening dielectric layer electrically isolating each column from its first magnetic layer.

In one embodiment, the device further comprises a single column, wherein the column comprises a first end and a second end, and wherein the first end comprises the input terminal and the second end comprises the output terminal.

In one embodiment, the device further comprises a first column and a second column spaced apart from the first column, each column comprising a first end and a second end; wherein the first end of the first column comprises the input terminal and the first end of the second column comprises the output terminal, and wherein the second end of the first column is interconnected to the second end of the second column by a track of conductive material.

In one embodiment, the device further comprises three or more spaced apart columns, the three or more columns comprising an input column, an output column, and at least one intermediate column, each column comprising a first end and a second end, and wherein the columns are interconnected at their ends by tracks of conductive material.

In one embodiment, the first end of each intermediate column is conductively coupled to the first end of a first adjacent column by a first interconnecting track of conductive material and isolated from the first end of a second adjacent column, and the second end of each intermediate column is conductively coupled to the second end of the second adjacent column by a second interconnecting track of conductive material and isolated from the second end of the first adjacent column, and wherein the end of the input column which is not connected to an intermediate column comprises the input terminal and the end of the output column which is not connected to an intermediate column comprises the output terminal.

In one embodiment, the device comprises a single column comprising an inner column portion and an outer column portion concentric with the inner column portion, the outer column portion and the inner column portion each having a first end and a second end, wherein the first end of the inner column portion and

the outer column portion each comprise an input terminal and the second end of the inner column portion and the outer column portion each comprise an output terminal, wherein the inner column portion and the outer column portion are separated by an insulation layer.

In one embodiment, the device comprises a first column and a second column spaced apart from the first column, each column comprising an inner column portion and an outer column portion concentric with the inner column portion, the outer column portion and the inner column portion each having a first end and a second end, wherein the first end of the first inner column portion and the first outer column portion each comprise an input terminal or an output terminal and the first end of the second inner column portion and the second outer column portion each comprise an input terminal or an output terminal, and wherein the second end of the first inner column portion is conductively coupled to the second end of the second inner column portion by an inner interconnecting track of conductive material, and wherein the second end of the first outer column portion is conductively coupled to the second end of the second outer column portion by an outer interconnecting track of conductive material.

In one embodiment, the device comprises three or more spaced apart columns, the three of more columns comprising an input column, an output column, and at least one intermediate column, each column comprising an inner column portion and an outer column portion concentric with the inner column portion, the outer column portion and the inner column portion each having a first end and a second end, wherein the first end of each intermediate inner column portion is conductively coupled to the first end of a first adjacent inner column portion by a first inner interconnecting track of conductive material and isolated from the first end of a second adjacent inner column portion, and the second end of each intermediate inner column portion is conductively coupled to the second end of the second adjacent inner column portion by a second inner interconnecting track of conductive material and isolated from the second end of the first adjacent inner column portion; and

wherein the first end of each intermediate outer column portion is conductively coupled to the first end of a first adjacent outer column portion by a first outer interconnecting track of conductive material and isolated from the first end of a second adjacent outer column portion, and the second end of each intermediate outer column portion is conductively coupled to the second end of the second adjacent outer column portion by a second outer interconnecting track of conductive material and isolated from the second end of the first adjacent outer column portion; and

wherein each end of an inner column portion and an outer column portion which is not connected to an intermediate column comprises an input terminal or an output terminal.

In one embodiment, the device further comprises a second magnetic layer provided between each inner column portion and outer column portion.

In one embodiment, the degree of coupling between the inner column portion and the outer column portion is tuned by varying the thickness of the first and/or second magnetic layers.

In one embodiment, the second magnetic layer comprises a plurality of vertical laminations comprising alternating magnetic and dielectric layers.

In one embodiment, the first magnetic layer comprises a plurality of vertical laminations comprising alternating magnetic and dielectric layers.

In one embodiment, the supporting structure comprises a non-conductive and non-magnetic material.

In one embodiment, the supporting structure comprises the first magnetic layer.

In one embodiment, the first magnetic layer comprises magnetic particles suspended in a polymer matrix.

In one embodiment, the first magnetic layer and/or the second magnetic layer comprise magnetic particles suspended in a polymer matrix.

In one embodiment, the first magnetic layer comprises a plurality of rings of magnetic material, each column surrounded by one ring, and further comprising an insulation layer between each of the rings.

In one embodiment, the rings are arranged in a hexagonally-packed topology.

In one embodiment, the rings are arranged in a square-packed topology.

In one embodiment, the first magnetic layer comprises a plurality of horizontal laminations comprising alternating magnetic and dielectric layers.

In one embodiment, the supporting structure and the columns together comprise an interposer.

In one embodiment, the supporting structure and the columns together comprise a printed circuit board.

In one embodiment, the supporting structure and the columns together comprise a functional substrate.

In one embodiment, the tracks of conductive material are on the surface of the supporting structure.

In one embodiment, the tracks of conductive material are embedded in the supporting structure.

In one embodiment, the tracks of conductive material are coated with a magnetic material.

In one embodiment, a partial coating of the magnetic material is provided beneath and/or over the tracks of conductive material.

In one embodiment, the magnetic material is electrically isolated from the tracks of conductive material by an intervening dielectric layer.

In one embodiment, the magnetic material has in-plane magnetic anisotropy in the X-Y plane.

In one embodiment, the magnetic material comprises horizontal laminations with intervening dielectric layers.

In one embodiment, one or more of the magnetic layers have in-plane magnetic anisotropy in the Z plane, making a vertical easy-axis and an annular hard-axis.

In one embodiment, the first magnetic layer and/or the second magnetic layer have magnetic anisotropy such that the hard-axis is oriented circumferentially to the columns.

This arrangement boosts the inductance of the device at high frequency.

In one embodiment, each column is solid.

In one embodiment, each column is hollow.

In one embodiment, the inductor device comprises one of: an inductor, a coupled inductor, a transformer, or a magnetic sensor.

In one embodiment, the device further comprises a support substrate.

In another embodiment there is provided a method for fabricating an inductor device comprising the steps of:

depositing one or more columns of conductive material on a first support substrate, the one or more columns comprising an input terminal and an output terminal;

depositing a first magnetic layer around each column;

depositing a fill material around and between each column to create a supporting structure; and

depositing an input pad on the input terminal and an output pad on the output terminal.

In one embodiment, the inductor device comprises a single column comprising a first end and a second end,

wherein the step of depositing an input pad on the input terminal and an output pad on the output terminal comprises depositing an input pad on the first end and depositing an output pad on the second end.

In one embodiment, the inductor device comprises a first column and a second column spaced apart from the first column, each column comprising a first end and a second end,

wherein the step of depositing an input pad on the input terminal and an output pad on the output terminal comprises depositing an input pad on the first end of the first column and depositing an output pad on the first end of the second column; and wherein the method further comprises the step of:

interconnecting the second end of the first column to the second end of the second column by a track of conductive material.

In one embodiment, the inductor device comprises three or more spaced apart columns, the three of more columns comprising an input column, an output column and at least one intermediate column, each column comprising a first end and a second end, wherein the method further comprises the step of interconnecting the columns by the steps of:

depositing a first set of tracks of conductive material such that the first end of each intermediate column is conductively coupled to the first end of a first adjacent column and not coupled to the first end of a second adjacent column;

and depositing a second set of tracks of conductive material such that the second end of each intermediate column is conductively coupled to the second end of a second adjacent column and not coupled to the second end of the first adjacent column; and

wherein the step of depositing an input pad on the input terminal and an output pad on the output terminal comprises depositing an input pad on the end of the input column which is not connected to an intermediate column and depositing an output pad on the end of the output column which is not connected to an intermediate column.

In one embodiment, the step of depositing a first magnetic layer around each column comprises the steps of:

coating the exposed surfaces of the columns and the first support substrate with a magnetic layer such that the magnetic layer extends along the first end of each column, distal to the first support substrate, along the vertical surface of each column, and along the surface of the first support substrate in between each column.

In one embodiment, the method further comprises:

planarizing the surface of the supporting structure to remove the first magnetic layer deposited on the first end of each column.

In one embodiment, the method further comprises the steps of:

after performing the step of depositing the first set of tracks of conductive material, mounting a second support substrate to the first set of tracks of conductive material;

inverting the supporting structure;

removing the first support substrate;

planarizing the surface of the second end of each column to remove the first magnetic layer that extends between the columns; and

performing the step of depositing the second set of tracks of conductive material.

In one embodiment, the method further comprises prior to depositing a fill material around and between each column to create a supporting structure, performing the steps of:

coating the exposed surfaces of the first magnetic layer with a second layer of conductive material such that the second layer of conductive material is on the first magnetic layer that extends along the first end of each column, distal to the first support substrate, along the vertical surface of the columns, and along the surface of the first support substrate in between the columns; and

depositing a second layer of magnetic material on the second layer of conductive material such that the second layer of magnetic material extends the length of the second layer of conductive material;

such that each column comprises an inner column portion and a concentric outer column portion, wherein the inner column portion and the outer column portion are separated by an insulation layer;

and wherein the step of depositing the first set of tracks of conductive material is such that:

the first end of each intermediate inner column portion is conductively coupled to the first end of a first adjacent inner column portion by a first inner interconnecting track of conductive material and isolated from the first end of a second adjacent inner column portion, and the first end of each intermediate outer column portion is conductively coupled to the first end of a first adjacent outer column portion by a first outer interconnecting track of conductive material and isolated from the first end of a second adjacent outer column portion; and

wherein the step of depositing the second set of tracks of conductive material is such that:

the second end of each intermediate inner column portion is conductively coupled to the second end of the second adjacent inner column portion by a second inner interconnecting track of conductive material and isolated from the second end of the first adjacent inner column portion; and

the second end of each intermediate outer column portion is conductively coupled to the second end of the second adjacent outer column portion by a second outer interconnecting track of conductive material and isolated from the second end of the first adjacent outer column portion; and

wherein each end of an inner column portion and an outer column portion which is not connected to an intermediate column comprises an input terminal or an output terminal.

In one embodiment, the method further comprises removing the second support substrate.

In one embodiment, the method further comprises prior to depositing the columns of conductive material on a first support substrate, performing the steps of:
depositing a plurality of spaced apart lengths of a first insulating material on the first support substrate;
depositing the first set of tracks of conductive material, wherein the tracks are deposited on those portions of the first support substrate which are not in contact with the spaced apart lengths of the first insulating material; and
depositing a plurality of spaced apart columns of the first insulating material on the spaced apart lengths of the first insulating material and on selective portions of the first set of tracks of conductive material.

In one embodiment, the method further comprises depositing the input or output pad while depositing the first set of tracks of conductive material.

In one embodiment, the method further comprises prior to depositing the first magnetic layer performing the steps of:
removing the first insulating material; and
depositing a second insulating material on the planar surfaces of the columns and the first support substrate; and
wherein the step of depositing the first magnetic layer around each column comprises coating the exposed vertical surface of the columns with the first magnetic layer.

In one embodiment, the method further comprises removing the second insulating material from the planar surface of the columns; and

performing the step of depositing the second set of tracks of conductive material.

In one embodiment, the method further comprises removing the second support substrate.

In one embodiment, the magnetic layers comprise a plurality of vertical laminations comprising alternating magnetic and dielectric layers.

In one embodiment, the method further comprises prior to depositing the first magnetic layer around each column performing the steps of:
coating the exposed surfaces of the columns with a layer of insulating material that extends along the first end of each column, distal to the support substrate, and also along the vertical surface of the columns; and
wherein the step of depositing a fill material around and between each column to create a supporting structure comprises depositing the first magnetic layer around and between each column such that it extends continuously from column to column.

In one embodiment, the method further comprises:
etching the first magnetic layer into separate rings concentric to each column, where the etched voids vertically extend from the top of the first magnetic layer to the surface of the first support substrate; and
filling the etched voids with a dielectric material.

In one embodiment, the method further comprises the steps of:
removing the insulating material from the planar surface of the columns;
performing the step of depositing the first set of tracks of conductive material;
mounting a second support substrate to the first set of tracks of conductive material;
inverting the supporting structure;
removing the first support substrate; and

performing the step of depositing the second set of tracks of conductive material.

In one embodiment, the method further comprises coating the tracks of conductive material with magnetic material.

In one embodiment, the method further comprises providing a partial coating of the magnetic material beneath and/or over the tracks of conductive material.

In one embodiment, the method further comprises electrically isolating the magnetic material from the tracks of conductive material by an intervening dielectric layer.

In one embodiment, the magnetic material is deposited in the presence of a magnetic field and has in-plane magnetic anisotropy in the X-Y plane.

In one embodiment, the magnetic material comprises horizontal laminations with intervening dielectrics in between.

In one embodiment, the one or more magnetic layers are deposited in the presence of a magnetic field, which induces magnetic anisotropy in either the X-Y and/or the Z planes.

In another embodiment there is provided a method for fabricating an inductor device comprising the steps of:
depositing a magnetic layer on a first support substrate to create a supporting structure; embedding one or more columns of conductive material in the magnetic layer, the one or more columns comprising an input terminal and an output terminal; depositing an input pad on the input terminal and an output pad on the output terminal.

In one embodiment, the inductor device comprises a single column comprising a first end and a second end,

wherein the step of depositing an input pad on the input column and an output pad on the output column comprises depositing an input pad on the first end and depositing an output pad on the second end.

In one embodiment, the inductor device comprises a first column and a second column spaced apart from the first column, each column comprising a first end and a second end,
wherein the step of depositing an input pad on the input column and an output pad on the output column comprises depositing an input pad on the first end of the first column and depositing an output pad on the first end of the second column; and wherein the method further comprises the step of:
interconnecting the second end of the first column to the second end of the second column by a track of conductive material.

In one embodiment, the inductor device comprises three or more spaced apart columns, the three of more columns comprising an input column, an output column and at least one intermediate column, each column comprising a first end and a second end, wherein the method further comprises the step of interconnecting the columns by the steps of:
depositing a first set of tracks of conductive material such that the first end of each intermediate column is conductively coupled to the first end of a first adjacent column and not coupled to the first end of a second adjacent column; and depositing a second set of tracks of conductive material such that the second end of each intermediate column is conductively coupled to the second end of a second adjacent column and not coupled to the second end of the first adjacent column; and
wherein the step of depositing an input pad on the input column and an output pad on the output column comprises depositing an input pad on the end of the input column which is not connected to an intermediate column and depositing an output pad on the end of the output column which is not connected to an intermediate column.

In one embodiment, the method further comprises prior to the step of embedding the columns of conductive material in the magnetic layer;
etching the magnetic layer into discrete columns of magnetic material, with etched voids in between the columns of magnetic material and columnar voids in the centre of and concentric with each column of magnetic material, wherein the voids vertically extend from the top of the magnetic layer to the surface of the first support substrate;
filling the etched voids with a dielectric material;
coating the exposed surfaces of the columns of magnetic material and the first support substrate with a first layer of insulating material that extends along the first end of each column of magnetic material, distal to the support substrate, along the vertical surface of the columns of magnetic material, and along the surface of the first support substrate in the columnar voids concentric with the columns of magnetic material;
mounting a second support substrate to the first end of the columns of magnetic material; inverting the supporting structure;
removing the first support substrate; and
wherein the step of embedding the columns of conductive material in the magnetic layer comprises depositing the columns of conductive material in the columnar voids in the centre of and concentric with the columns of magnetic material.

In one embodiment, the magnetic layer extends continuously from column to column of conductive material, the method further comprising prior to the step of embedding the columns of conductive material in the magnetic layer;
etching the magnetic layer to form columnar voids, wherein the voids vertically extend from the top of the magnetic layer to the surface of the first support substrate;
coating the exposed surfaces of the magnetic material and the first support substrate with a first layer of insulating material that extends along the end of the magnetic material distal to the support substrate, along the vertical surface of the magnetic material, and along the surface of the first support substrate in the columnar voids;

mounting a second support substrate to the first end of the magnetic material;
inverting the supporting structure;
removing the first support substrate; and
wherein the step of embedding the columns of conductive material in the magnetic layer comprises depositing the columns of conductive material in the columnar voids.

In one embodiment, the magnetic layer comprises a plurality of horizontal laminations comprising alternating magnetic and dielectric layers; and wherein if the top surface of the magnetic layer is not a dielectric, depositing a second layer of insulating material on the exposed second end of the magnetic material prior to embedding the columns of conductive material in the magnetic layer.

In one embodiment, the method further comprises prior to embedding the columns of conductive material in the magnetic core, depositing a second layer of insulating material on the exposed second end of the magnetic material.

In one embodiment, the method further comprises:
performing the step of depositing the first set of tracks of conductive material;
mounting a third support substrate to the first set of tracks of conductive material;
inverting the supporting structure;
removing the second support substrate; and
performing the step of depositing the second set of tracks of conductive material.

In one embodiment, the method further comprises:
coating the tracks of conductive material with a magnetic material.

In one embodiment, the method further comprises:
providing a partial coating of the magnetic material beneath and/or over the tracks of conductive material.

In one embodiment, the method further comprises:
electrically isolating the magnetic material from the tracks of conductive material by an intervening dielectric layer.

In one embodiment, the magnetic material comprises horizontal laminations with intervening dielectrics in between.

In one embodiment, one or more of the magnetic layers are deposited in the presence of a magnetic field, which induces magnetic anisotropy in either the X-Y and/or the Z planes.

In yet another aspect of the invention there is provided an inductor device comprising:
at least two interconnected columns of conductive material embedded in a supporting structure, wherein the columns are interconnected by tracks of conductive material, wherein the at least two columns comprise an input terminal and an output terminal; and wherein each column is surrounded by a first magnetic layer.

In one embodiment, the supporting structure comprises a non-semiconductive, non-glass, non-PCB material.

In one embodiment, the supporting structure comprises the tracks of conductive material.

In one embodiment, the supporting structure comprises a magnetic material.

In one embodiment, the supporting structure comprises a non-conductive and non-magnetic material.

In one embodiment, the supporting structure comprises a non-conductive and non-magnetic material and the tracks of conductive material.

In one embodiment, the at least two interconnected columns of conductive material embedded in the supporting structure are separated by an interstitial medium.

In one embodiment, the interstitial medium comprises a gas.

In one embodiment, the interstitial medium comprises a magnetic material.

In one embodiment, the interstitial medium comprises a non-conductive and non-magnetic material.

In one embodiment, the first magnetic layer comprises a plurality of rings of magnetic material, each column surrounded by one ring, and further comprising an insulation layer between each of the rings.

In one embodiment, each column is solid.

In one embodiment, each column is hollow.

In one embodiment, each column comprises an inner column portion and an outer column portion concentric with the inner column portion, wherein the first magnetic layer surrounds each outer column portion and a second magnetic layer surrounds each inner column portion.

In one embodiment, the first magnetic layer and/or the second magnetic layer comprise a plurality of vertical laminations comprising alternating magnetic and dielectric layers.
In one embodiment, the coupling factor between the columns of conductive material is tuneable by adjusting the width of the dielectric layer.

In one embodiment, the supporting structure comprises the first magnetic layer; and wherein the first and/or second magnetic layer comprise magnetic particles suspended in a polymer matrix.

In one embodiment, the first magnetic layer and/or the second magnetic layer have magnetic anisotropy such that the hard-axis is oriented circumferentially to the columns.

In one embodiment, the magnetic anisotropy is a function of the aspect ratio of the columns of conductive material.

In one embodiment, the inductor device comprises a discrete, self-supporting device.

Brief Description of the Drawings

The invention will be more clearly understood from the following description of an embodiment thereof, given by way of example only, with reference to the accompanying drawings, in which:-

Figure 1a shows one embodiment of the inductor device of the present invention;

Figure 1b shows another embodiment of the inductor device of the present invention;

Figure 2 shows the main steps in the fabrication process of the vertical magnetic structure of the inductor device of the present invention;

Figure 3 shows a detailed schematic of one fabrication process of the vertical magnetic structure of the inductor device shown in Figure 1b;

Figure 4 shows a detailed schematic of another fabrication process of the vertical magnetic structure of the inductor device shown in Figure 1b;

Figure 5 shows four alternative embodiments of the inductor device of the present invention;

Figure 6 shows a detailed schematic of an embodiment of the fabrication process to obtain the vertical magnetic structure of the inductor device shown in Figure 5b;

Figure 7 shows a detailed schematic of an embodiment of the fabrication process to obtain the vertical magnetic structure of the inductor device shown Figure 5d;

Figure 8 shows a 3D view of the inductor device of Figure 1a;

Figure 9a shows an embodiment of the invention where the inductor device comprises a coaxial vertical magnetic structure;

Figure 9b shows a 90° cross-sectional view of a coaxial column of conductive material of the same structure as that of Figure 9a, and

Figure 10 shows a detailed schematic of the fabrication process of the inductor device of Figure 9;

Figure 11 shows another embodiment of the inductor device of the present invention where the passivation layer is far greater than the width of the magnetic layer;

Figure 12 shows another embodiment of the inductor device of the present invention, where the supporting structure comprises a combination of the interconnecting tracks of conductive material and a passivation layer;

Figure 13 shows another embodiment of the inductor device of the present invention, where the supporting structure comprises the interconnecting tracks of conductive material;

Figure 14 shows a top down view of the inductor array of Figure 8;

Figure 15 shows a further embodiment of the inductor device of Figure 5a;

Figure 16 shows how the width of the dielectric material can be adjusted to tune the coupling between inductors to a desired value; and

Figure 17 illustrates the difference in magnetic anisotropy between conductive columns of different aspect ratios.

Detailed Description of the Drawings

The present invention comprises an inductor device in the form of a vertical magnetic structure for an integrated power converter. The inductor device comprises one or more columns of conductive material embedded in a supporting structure, wherein the one or more columns comprise an input terminal and an output terminal. Each column is surrounded by a magnetic layer.

One embodiment of the inductor device of the invention is shown in Figure 1a. In this embodiment, the inductor device 1 comprises three columns 2 of conductive material embedded in a supporting structure 3, with a magnetic layer in the form of a magnetic core 4 surrounding each column 2. The columns comprise an input column 5, an output column 6, and an intermediate column 7. An input/output pad 8 is connected to the input column to form the input terminal of the inductor and an input/output pad 8 is connected to the output column to form the output terminal of the inductor. The columns are alternately interconnected at their ends by means of conductive tracks. In the embodiment shown, a first set of tracks 9a extend along the bottom surface of the supporting structure 3 and a second set of tracks 9b extend along the top surface of the supporting structure 3. However, in other embodiments, the tracks can be embedded inside the supporting structure.

In the embodiment of Figure 1a, the magnetic core 4 comprises alternating layers of magnetic 10 and dielectric materials 11, where the core itself has the quality of being either magnetically isotropic or magnetically anisotropic. As is shown in Figure 1a, the inductor device has been released from an underlying support substrate, wherein it will be appreciated that this quality may be attributed to any other embodiment of the invention. In one embodiment of the invention, the magnetic core is in the form of a vertically-oriented laminated thin film composed of a soft magnetic alloy, where the laminations have in-plane magnetic anisotropy with an easy-axis in the vertical direction.

The magnetic core 4 and the columns 2 both may be deposited by any suitable means and may also comprise any suitable materials. Some suitable deposition methods are chemical vapour deposition (CVD), physical vapour deposition (PVD) and electrodeposition. Some suitable magnetic materials are CZT, CZTB, FINEMET, CoP, NiFe and CoNiFe. Some suitable dielectric materials are AlN, SiO2, Si3N4, Si2N2O, SiC, Si, SiLK, polyimide, parylene, benzocyclobutene (BCB), polybenzoxazole (PBO), tetraethylorthosilicate (TEOS), fluorinated TEOS (FTEOS), doped glass (BPSG, PSG, BSG), organo-silicate glass (OSG),

fluorinated glass (FSG), spin-on glass (SOG) and Al2O3. Some suitable conductive materials are Cu, Al, Ag and Au.

It will be appreciated that any number of columns 2 may be embedded in the supporting structure 3, depending on the requirements of the circuitry with which the inductor device is to be used. In embodiments where the inductor device comprises more than three columns, the vertical magnetic structure comprises a single input column to which the input/output pad forming the input terminal is connected at one end, a single output column to which the input/output pad forming the output terminal is connected at one end, and a plurality of intermediate columns. Where the inductor device comprises two columns, the vertical magnetic structure simply comprises an input column and an output column. The input/output pad forming the input terminal is then connected to one end of the input column and the input/output pad forming the output terminal is connected to the same end of the output column. Where the inductor device comprises only one column, the input/ output pads forming the respective input and output terminals are connected to opposite ends of the same column.

As previously mentioned, the columns of conductive material are alternately connected with interconnecting tracks of conductive material. In the embodiment where the inductor device comprises three or more columns, this is achieved by a first end of each intermediate column being conductively coupled to a first end of a first adjacent column and isolated from a first end of a second adjacent column and a second end of each intermediate column being conductively coupled to a second end of a second adjacent column and not coupled to a second end of the first adjacent column. The I/O pad for wire bonding/flip chip is then connected to the end of the input column and the end of the output column that is not connected to an intermediate column.

Figure 1b shows another embodiment of the inductor device of the present invention. This embodiment comprises the same features as Figure 1a, except that it further includes a support substrate 12 coupled to the first set of tracks 9a

of conductive material. The supporting structure 3 of the embodiment of Figure 1b comprises a passivation layer. The passivation layer comprises a non-conductive and non-magnetic material. One example of such a material is a photoresist such as SU-8, or any light-sensitive material used in lithography. The supporting structure and the columns together may comprise a PCB, a functional substrate, a package or an interposer. The supporting structure may comprise any suitable magnetic material, such as ferrite or NiFe.

In one embodiment of the invention, the first and second interconnecting tracks of conductive material are coated with a magnetic material. This magnetic material may comprise alternating laminations of any suitable magnetic and dielectric materials. This coating can be achieved in a number of different ways. In a first embodiment, the coating of magnetic material completely wraps the tracks, forming a closed core. In a second embodiment, the magnetic material partially coats the tracks such that it is only located beneath the tracks. In a third embodiment, the magnetic material partially coats the tracks such that it is only located over the tracks. In a fourth embodiment, the magnetic material partially coats the tracks such that it is located both beneath and over the tracks.

Figure 2 shows the main steps in the fabrication process to obtain the inductor device of the present invention. In step 200, one or more columns of conductive material are deposited on a support substrate, the one or more columns comprising an input terminal and an output terminal. In step 205, a magnetic layer in the form of a magnetic core is deposited around each column. In step 210, a fill material is deposited around and between each column to provide a supporting structure. In step 215, the columns are selectively interconnected with tracks of conductive material and I/O pads are deposited on the input terminal and the output terminal.

In the case where the inductor device comprises three or more columns comprising an input column, an output column and a plurality of intermediate columns, the selective interconnection of the columns with tracks of conductive material is such that the first end of each intermediate column is conductively

coupled to the first end of a first adjacent column and isolated from the first end of a second adjacent column and the second end of each intermediate column is conductively coupled to the second end of the second adjacent column and not coupled to the second end of the first adjacent column. The I/O pad for wire bonding/flip chip is then connected to the end of the input column and the end of the output column that is not connected to an intermediate column.

Figure 3 shows a detailed schematic of one fabrication process to obtain the inductor device of the present invention, where the device comprises an input column, an output column and at least one intermediate column. In the first step of the fabrication process, spaced apart columns of conductive material are deposited on a first support substrate (step 300). In step 305, a first magnetic layer in the form of a magnetic core comprising alternating laminations of magnetic and dielectric materials is conformally deposited on and in between each column. This involves coating all of the exposed surfaces of the columns and the first support substrate with the magnetic core such that the magnetic core is deposited vertically around each column, horizontally on the first support substrate between each column, and horizontally on a first end of each column distal to the first support substrate. In step 310, a fill material is deposited around and in the gaps between each column to provide a supporting structure. In step 315, the surface of the supporting structure is planarized to remove the horizontal magnetic core deposited on the first end of each column. In step 320, the intermediate columns are connected with a first set of conductive tracks such that the first end of each intermediate column is conductively coupled to the first end of a first adjacent column and isolated from the first end of a second adjacent column. I/O pads for wire bonding/flip chip may also be connected at this stage. In step 325, a second support substrate is mounted to the first set of tracks of conductive material and the structure is inverted. In step 330, the first support substrate is removed. In step 335, the surface of a second end of each column is planarized in order to remove the horizontal magnetic core between each column. In step 340, the intermediate columns are connected with a second set of interconnecting conductive tracks such that the second end of each intermediate column is conductively coupled to the second

end of the second adjacent column and not coupled to the second end of the first adjacent column. A second I/O pad for wire bonding/flip chip may also be connected at this stage.

Figure 4 shows a detailed schematic of another fabrication process to obtain the inductor device of the present invention, where the device comprises an input column, an output column and at least one intermediate column. In the first step of the fabrication process, a plurality of lengths of a first insulating material are deposited on a support substrate, where a first set of tracks of conductive material are then deposited on those portions of the support substrate which are not in contact with the first insulating material. I/O pads may also be deposited at this stage (step 400). In step 405, further first insulating material is deposited on the plurality of lengths of the first insulating material and also on selective portions of the first set of tracks of conductive material in order to form a plurality of spaced apart columns of the first insulating material. In step 410, columns of conductive material are deposited between the plurality of spaced apart columns of insulating material such that a second end of each intermediate column is conductively coupled to the second end of a first adjacent column by the first set of tracks of conductive material and isolated from the second end of a second adjacent column. In step 415, the first insulating material is removed. In step 420, a thin film of a second insulating material is deposited on both the planar surfaces of the conductive columns and the support substrate. A first magnetic layer in the form of a magnetic core is then deposited around each column. In step 425, a fill material is deposited around and in the gaps between each conductive column to form a supporting structure. In step 430, the second insulating material on a first end of the conductive columns is removed. In step 435, the intermediate columns are connected with a second set of interconnecting conductive tracks such that the first end of each intermediate column is conductively coupled to the first end of the second adjacent column and not coupled to the first end of the first adjacent column. I/O pads for wire bonding/flip chip may also be connected at this stage.

Figure 5 shows four additional alternative embodiments of the inductor device of the present invention. In the embodiment of Figure 5b, each column is embedded in a magnetic layer formed by a magnetic core, which also acts as a supporting structure. The magnetic core comprises a solid sheet of magnetic material.

Figures 5a and 5c shows a top down and a side view respectively of an alternative embodiment to Figure 5b, where the magnetic core comprises a plurality of rings concentric to each column, with a vertically-oriented intervening dielectric in between the rings. Figure 5e shows a side view of yet another embodiment, where the magnetic core comprises a plurality of rings concentric to each column of alternating horizontal laminations of magnetic and dielectric materials, with a vertically-oriented intervening dielectric in between the rings.

Figure 5d shows an embodiment similar to Figure 5b, but where the magnetic core comprises a laminated solid sheet of alternating horizontal laminations of magnetic and dielectric materials.

Figure 6 shows a detailed schematic of an embodiment of the fabrication process to obtain the inductor device of the type shown in Figure 5b, where the device comprises an input column, an output column and at least one intermediate column. In the first step of the fabrication process, a plurality of spaced apart columns of a first insulating material are deposited on a first support substrate (600). In step 605, columns of conductive material are then deposited between the plurality of spaced apart columns of the first insulating material. In step 610, the first insulating material is removed. In step 615, a second layer and a third layer of the same insulating material are deposited on the first support substrate. The second layer of insulating material makes contact with the support substrate and extends between the columns of conductive material. The third layer of insulating material is located on a portion of the surface of second layer of insulating material. In step 620, a thin film of a fourth insulating material of a different type to the second and third layers of insulation is deposited on both the planar surfaces of the conductive columns

and the second and third insulating layers. In step 625, the second and third layers of insulating material are removed. In step 630, a fifth insulation layer is deposited around the vertical sidewalls of the conductive columns. In step 635, a magnetic layer is deposited in the spaces between the conductive columns so as to form a magnetic core and act as a supporting structure. The thickness of the magnetic core is equal to the thickness of the conductive columns. As previously explained, the magnetic core can be in the form of a solid sheet or take the form of rings which are concentric to each column, with a vertically-oriented dielectric in between the rings. In step 640, the fourth insulating material is removed from the conductive columns. In step 645, a sixth and a seventh layer of insulation is deposited on the surface of the magnetic core distal from the first support substrate. In step 650, a seed layer is deposited on top of the sixth and seventh layers of insulation. In step 655, the columns are connected with a first set of interconnecting conductive tracks such that a first end of each intermediate column is conductively coupled to the first end of a second adjacent column and not coupled to the first end of a first adjacent column. I/O pads for wire bonding/flip chip may also be connected at this stage. In step 660, the surface of the first end of each column is planarized in order to remove the excess material. In step 665, a second support substrate is mounted to the first set of tracks of conductive material and the structure is inverted. In step 670, the first support substrate is removed. In step 675, the columns are connected with a second set of interconnecting conductive tracks such that a second end of each intermediate column is conductively coupled to the second end of the first adjacent column and not coupled to the second end of the second adjacent column. I/O pads for wire bonding/flip chip may also be connected at this stage.

Steps 600a to 630a show an alternative technique which can be performed in place of steps 600 to 630. In this technique, a plurality of spaced apart conductive columns are deposited on a first support substrate (600a). In step 605a, a dielectric is deposited on all of the exposed surfaces of the columns and the first support substrate such that the dielectric is deposited vertically around each column, horizontally on the first support substrate between each column,

and horizontally on a first end of each column distal to the first support substrate. In step 610a, a second support substrate is mounted to the columns and the structure is inverted. In step 615a, the first support substrate is removed. In step 620a, second and third layers of insulation material are deposited on the first support substrate. In step 625a, a dielectric is deposited on the horizontal surfaces of the columns and the second and third layers of insulation material. In step 630a, the second and third layers of insulation material are removed. The process then continues at step 635, as previously described.

Figure 7 shows a detailed schematic of one embodiment of the fabrication process to obtain the inductor device of the type shown in Figure 5d, where the device comprises an input column, an output column and at least one intermediate column. In the first step, a magnetic layer in the form of a magnetic core, which is in the form of a planar sheet comprising a plurality of alternating horizontal laminations of magnetic and dielectric materials, is deposited on a first support substrate (700). In step 705, a selective etch creates discrete columnar voids in the magnetic core. In step 710, a first insulation layer is deposited conformally, covering both the planar and vertical surfaces of the magnetic core. In step 715, a second support substrate is mounted to the magnetic core and the structure is inverted. In step 720, the first support substrate is removed. In step 725, columns of conductive material are deposited into the discrete columnar voids in the magnetic core. The process then continues to step 645 of Figure 6 until step 670 of Figure 6. Then, in step 730 the columns are connected with a second set of interconnecting conductive tracks such that a second end of each intermediate column is conductively coupled to the second end of the second adjacent column and not coupled to the second end of the first adjacent column. I/O pads for wire bonding/flip chip may also be connected at this stage.

In the embodiment shown in Figure 7, the magnetic core is in the form of a solid sheet. However, as previously explained in relation to Figure 5, in another

embodiment, the magnetic core can take the form of rings which are concentric to each columnar void, with a vertically-oriented dielectric in between the rings.

Figure 8 shows a 3D view of the inductor device of Figure 1a along with a 90° cross-sectional view of a column of conductive material from that same structure (the supporting structure is not shown for clarity purposes). The column of conductive material is surrounded by a first magnetic layer in the form of a magnetic core, where the magnetic core may comprise laminations of alternating magnetic and dielectric materials.

Figure 9a shows a 3D view of another embodiment of the inductor device of the present invention where the structure comprises a coaxial or concentric structure (the supporting structure is not shown for clarity purposes). This concentric structure provides a coupling of 0.9, as well as a perfect dc flux cancelation in the core. If the Re-Distribution Layer (RDL) top and bottom traces are placed on top of each other, a transformer with ultra-low leakage inductance and excellent coupling is achieved. A 90° cross-sectional view of a concentric column of conductive material from that same structure is also shown in Figure 9b, where each concentric column comprises two individual columns of conductive material that are electrically insulated from one another, where each individual column of conductive material may be further surrounded by a magnetic layer in the form of a magnetic core. In one embodiment, the magnetic core comprises alternating vertical laminations of magnetic and dielectric materials.

Figure 10 shows a detailed schematic of the fabrication process of the inductor device shown in Figure 9, where the device comprises an input column, an output column and at least one intermediate column. In the first step of the fabrication process, a first set of conductive columns is deposited on a first support substrate (1000). In step 1005, a first magnetic layer in the form of a magnetic core is conformally deposited on both the planar and vertical surfaces of the conductive columns and on the surface of the first support substrate between the columns. In step 1010, a layer of conductive material is conformally

deposited on top of the first magnetic core, to form a second set of conductive columns concentric to the first set of conductive columns. In step 1015, a second magnetic layer in the form of a magnetic core is conformally deposited on top of the second set of conductive columns. In step 1020, a fill material is deposited around and in the gaps between the columns to provide a supporting structure. In step 1025, the surface of a first end of each column distal to the first support substrate is planarized in order to remove excess material on top of and between each column. In step 1030, a first set of interconnecting tracks of conductive material are deposited such that the first end of each intermediate column of the first set of columns is conductively coupled to the first end of a first adjacent column of the first set of columns and isolated from the first end of a second adjacent column of the first set of columns and the first end of each intermediate column of the second set of columns is conductively coupled to the first end of a first adjacent column of the second set of columns and isolated from the first end of a second adjacent column of the second set of columns, where the first set of interconnecting tracks of conductive material for the second set of conductive columns are electrically insulated from the first set of interconnecting tracks of conductive material for the first set of conductive columns. I/O pads for wire bonding/flip chip may also be connected at this stage. In step 1035, a second support substrate is mounted to the first set of tracks of conductive material and the structure is inverted. In step 1040, the first support substrate is removed. In step 1045, the surface of a second end of each column is planarized in order to remove the horizontally-oriented material between each column. In step 1050, the columns are connected with a second set of interconnecting conductive tracks such that a second end of each intermediate column of the first set of columns is conductively coupled to the second end of the second adjacent column of the first set of columns and not coupled to the second end of the first adjacent column of the first set of columns and a second end of each intermediate column of the second set of columns is conductively coupled to the second end of the second adjacent column of the second set of columns and not coupled to the second end of the first adjacent column of the second set of columns, where the second set of interconnecting tracks of conductive material for the second set of conductive columns are

electrically insulated from the second set of interconnecting tracks of conductive material for the first set of conductive columns. I/O pads for wire bonding/flip chip may also be connected at this stage.

In the embodiment shown, each of the first and the second magnetic cores comprise alternating layers of magnetic and dielectric materials. However, it will be appreciated that in an alternative embodiment, the magnetic core may simply comprise a sheet of magnetic material.

In the embodiments of the invention shown in Figures 8 and 9, the conductive columns are located on square vertices. However, any other suitable arrangement of columns could equally well be used. For example, to pack columns more densely, the columns could be arranged in a honeycomb structure or connected in double helix form where the I/O pads are on adjacent columns to ease routing in the electrical circuit. A double helix form corresponds to two interleaved inductor devices that wind around each other like individual strands of deoxyribonucleic acid (DNA). The double-helical strands will ideally have a spiral topology, winding from a common centre outwards. The double-helical topology would have a reduced cross-sectional area, as opposed to a conventional toroidal structure, and the cross-section itself would consist of either an air core or a magnetic core, which would be in addition to the magnetic core which may or may not surround each of the individual columns. This double-helical form would result in the highest inductance with regards to topology. Additionally, a space-filling arrangement of the columns, such as for example, a curve, could also be used in order to ease routing.

The inductor device of the present invention provides a number of advantages over conventional planar structures. Firstly, and if considered as an inductor, the inductor device achieves high performance because of excellent coupling (that is, extremely low leakage inductance) and high efficiency. The structure has been found to offer 40% higher inductance for the same coil length when compared to existing V-groove inductors. For example, the inductor structure of Figure 8 with one $Ni_{45}Fe_{55}$ lamination with a 10 µm thick RDL layer achieves

L=5.9nH, L/DCR=0.39nH/mΩ and L/Footprint=31.9nH/mm^2 at the frequency of 100 MHz, with a Q-factor of 7. The saturation current of this structure is 0.8A, which gives a current density of 4.3A/mm^2. In this regard, it should be noted that increasing the diameter of the conductive columns reduces the copper resistance and inductance of the columns, both, thus increasing the saturation current. In the embodiment where the top and bottom conductive tracks are coated with magnetic thin film, a 12% inductance boost is also achieved.

Furthermore, if the inductor of the present invention is implemented using copper columns embedded in magnetic material laminate, as per several of the described embodiments of the invention, the inductance is increased by more than an order of magnitude (approximately 16 times).

Where a laminated magnetic core is used, there is no dielectric material on the flux path, which reduces core losses. Furthermore, copper losses are significantly reduced with vertical current flow, which leads to higher inductor efficiency. In addition, there is no flux crowding, due to the smooth core shape.

In addition, as the first generation of integrated power converter products are based on 2.5D and 3D stack integration technologies, the present invention facilitates achieving efficient, high density in-package IVRs.

When the inductor structure of the present invention is integrated into an integrated voltage regulator circuit, the interconnections between different components on the circuit are being used to act as passive devices in the form of inductors. This results in a fully integrated VR solution where the active circuitry is either monolithically built or packaged with the passive devices, that is the inductors and capacitors. Further, the inductor structure uses its magnetic core to improve the power density and efficiency of the IVR circuit.

Figure 11 shows another embodiment of the inductor device of the present invention. In this embodiment, the supporting structure comprises a passivation layer, as was the case for Figure 1a and 1b. However, in Figure 1a and 1b the

width of the passivation layer was much smaller than the width of the magnetic layer, whereas in the embodiment of Figure 11, the passivation layer is far greater than the width of the magnetic layer.

Figure 12 shows another embodiment of the inductor device of the present invention, where the supporting structure comprises a combination of the interconnecting tracks of conductive material and a passivation layer. It should be noted that the interconnect can support the device due to the short distance (small volume) between the conductive columns.

Figure 13 shows another embodiment of the inductor device of the present invention, where the supporting structure comprises the interconnecting tracks of conductive material and the conductive columns. In this embodiment, air is used as a dielectric. However, it should be noted that this device is not an air core inductor. This embodiment is discrete and self-supporting, as the small length of the interconnecting tracks results in tiny voids between the columns of conductive material, which overall closely approximates a solid structure with a continuous cross-section.

Figure 14 shows a top down view of the inductor array of Figure 8. It can be seen that in this embodiment, the columns of conductive material embedded in the supporting structure (not shown) are separated by an interstitial medium. In this regard it should be understood that the supporting structure comprises the material which provides the mechanical strength of the device. A mechanically strong device is synonymously described as being either discrete or self-supporting, or both. A discrete and/or self-supporting device is thus able to "stand on its own" without being supported by any external forces or bodies, such as for example a semiconducting substrate or a printed circuit board.

The interstitial medium comprises the material that fills the vertically-oriented space between the columns of conductive material. It should be noted that the supporting structure and the interstitial medium may or may not be the same material, depending on the embodiment. Thus, Figures 5 and Figures 11 to 13

also comprise columns of conductive material embedded in a supporting structure and separated by an interstitial medium. The interstitial medium may be a gas, a magnetic material or a non-conductive and non-magnetic material. For example, the interstitial medium comprises a gas in the embodiment of Figure 13, while the supporting structure comprises the interconnecting tracks of conductive material and the columns of conductive material. However, in the embodiment of Figure 11, the supporting structure and the interstitial medium both comprise the same material, which is a non-conductive and non-magnetic material.

Figure 15 comprises a variation of the embodiment of Figure 5a. In this embodiment, the rings of magnetic material comprise magnetic particles suspended in a polymer matrix.

It will be appreciated from the embodiments of Figures 11 to 15 that the supporting structure of the present invention is not a conventional substrate. Therefore, the supporting structure is not a semiconductor, glass or a PCB material.

The coupling factor between two inductors can be tuned by varying the width of the adjoining dielectric. For example, the width of the dielectric material shown in Figure 16 can be adjusted to tune the coupling between the inductors to a desired value.

In the device of the present invention, the magnetic anisotropy direction is partially a function of the aspect ratio (AR) of the conductive columns, i.e. the ratio of the height of a conductive column to the diameter of a conductive column. This difference in magnetic anisotropy is illustrated for a conductive column having a first aspect ratio in Figure 17a and for a conductive column having a second higher aspect ratio in Figure 17b.

The three different orientations of magnetic anisotropy are shown in the Figure: circumferential easy-axis (curling counter-clockwise arrow), radial, and axial

(vertical), with probable orientations being shown in green while improbable orientations are shown in red. Thus, it can be seen that for a high aspect ratio, the axial direction becomes much more likely, as shown in Figure 17b. It has been found that at AR=2 and beyond, the magnetic anisotropy orientation shown in Figure 17b becomes increasingly probable.

In the specification the terms "comprise, comprises, comprised and comprising" or any variation thereof and the terms "include, includes, included and including" or any variation thereof are considered to be totally interchangeable and they should all be afforded the widest possible interpretation and vice versa.

The invention is not limited to the embodiments hereinbefore described but may be varied in both construction and detail.

Claims

1. A transformer or coupled inductor device comprising:
two interconnected columns of conductive material embedded in a supporting structure, the two interconnected columns comprising a first column and a second column spaced apart from the first column, each column comprising an inner column portion and an outer column portion concentric with the inner column portion,
the outer column portion and the inner column portion each having a first end and a second end, wherein the first end of the first inner column portion and the first outer column portion each comprise an input terminal or an output terminal and the first end of the second inner column portion and the second outer column portion each comprise an input terminal or an output terminal, and wherein the second end of the first inner column portion is conductively coupled to the second end of the second inner column portion by an inner interconnecting track of conductive material, and wherein the second end of the first outer column portion is conductively coupled to the second end of the second outer column portion by an outer interconnecting track of conductive material.

2. A transformer or coupled inductor device comprising:
three or more interconnected spaced apart columns of conductive material embedded in a supporting structure, the three of more columns comprising an input column, an output column, and at least one intermediate column, each column comprising an inner column portion and an outer column portion concentric with the inner column portion, the outer column portion and the inner column portion each having a first end and a second end, wherein the first end of each intermediate inner column portion is conductively coupled to the first end of a first adjacent inner column portion by a first inner interconnecting track of conductive material and isolated from the first end of a second adjacent inner column portion, and the second end of each intermediate inner column portion

is conductively coupled to the second end of the second adjacent inner column portion by a second inner interconnecting track of conductive material and isolated from the second end of the first adjacent inner column portion; and

wherein the first end of each intermediate outer column portion is conductively coupled to the first end of a first adjacent outer column portion by a first outer interconnecting track of conductive material and isolated from the first end of a second adjacent outer column portion, and the second end of each intermediate outer column portion is conductively coupled to the second end of the second adjacent outer column portion by a second outer interconnecting track of conductive material and isolated from the second end of the first adjacent outer column portion;

wherein each end of an inner column portion and an outer column portion which is not connected to an intermediate column comprises an input terminal or an output terminal.

3. The device of Claim 1 or Claim 2 further comprising:
a first magnetic layer surrounding each outer column portion.

4. The device of claim 3, further comprising a second magnetic layer surrounding each inner column portion.

5. The device of claim 4, wherein the degree of coupling between the inner column portion and the outer column portion is tuned by varying the thickness of the first and/or second magnetic layers.

6. The device of claim 4 or claim 5 wherein the second magnetic layer comprises a plurality of vertical laminations comprising alternating magnetic and dielectric layers.

7. The device of any of the preceding claims, wherein the first magnetic layer comprises a plurality of vertical laminations comprising alternating magnetic and dielectric layers.

8. The device of any of the preceding claims, where the supporting structure comprises a non-conductive and non-magnetic material.

9. The device of any of the preceding claims, wherein the supporting structure comprises the first magnetic layer.

10. The device of any of claims 3 to 9, wherein the first magnetic layer and/or the second magnetic layer comprise magnetic particles suspended in a polymer matrix.

11. The device of claim 10, wherein the first magnetic layer comprises a plurality of rings of magnetic material, each column surrounded by one ring, and further comprising an insulation layer between each of the rings.

12. The device of any of the preceding claims, wherein each column is solid.

13. The device of any of claims 1 to 11, wherein each column is hollow.

14. The device of any of claims 3 to 13, wherein the first magnetic layer and/or the second magnetic layer have magnetic anisotropy such that the hard-axis is oriented circumferentially to the columns.

15. An inductor device comprising:
at least two interconnected columns of conductive material embedded in a supporting structure, wherein the columns are interconnected by tracks of conductive material, wherein the at least two columns comprise an input terminal and an output terminal; and wherein each column is surrounded by a first magnetic layer.

16. The inductive device of Claim 15, wherein the supporting structure comprises a non-semiconductive, non-glass, non-PCB material.

17. The inductive device of Claim 15 or Claim 16, wherein the supporting structure comprises the tracks of conductive material.

18. The inductive device of Claim 15 or Claim 16, wherein the supporting structure comprises a magnetic material.

19. The inductive device of Claim 15 or Claim 16, wherein the supporting structure comprises a non-conductive and non-magnetic material.

20. The inductive device of Claim 15 or Claim 16, wherein the supporting structure comprises a non-conductive and non-magnetic material and the tracks of conductive material.

21. The inductor device of any of Claims 15 to 20, wherein the at least two interconnected columns of conductive material embedded in the supporting structure are separated by an interstitial medium.

22. The inductor device of Claim 21 wherein the interstitial medium comprises a gas.

23. The inductor device of Claim 21, wherein the interstitial medium comprises a magnetic material.

24. The inductor device of Claim 21, wherein the interstitial medium comprises a non-conductive and non-magnetic material.

25. The inductor device of any of claims 15 to 24, wherein the first magnetic layer comprises a plurality of rings of magnetic material, each column surrounded by one ring, and further comprising an insulation layer between each of the rings.

26. The inductor device of any of claims 15 to 25, wherein each column is solid.

27. The inductor device of any of claims 15 to 25, wherein each column is hollow.

28. The inductor device of any of Claims 15 to 27, wherein each column comprises an inner column portion and an outer column portion concentric with the inner column portion, wherein the first magnetic layer surrounds each outer column portion and a second magnetic layer surrounds each inner column portion.

29. The inductor device of any of Claims 15 to 28, wherein the first magnetic layer and/or the second magnetic layer comprise a plurality of vertical laminations comprising alternating magnetic and dielectric layers.

30. The inductor device of any of Claims 25 to 29, wherein the coupling factor between the columns of conductive material is tuneable by adjusting the width of the insulation layer.

31, The inductor device of Claims 15, 16, 18, 21, 23 and 25 to 30, wherein the supporting structure comprises the first magnetic layer; and wherein the first and/or second magnetic layer comprise magnetic particles suspended in a polymer matrix.

32. The inductor device of any of Claims 15 to 31, wherein the first magnetic layer and/or the second magnetic layer have magnetic anisotropy such that the hard-axis is oriented circumferentially to the columns.

33. The inductor device of Claim 32, wherein the magnetic anisotropy is a function of the aspect ratio of the columns of conductive material.

34. The inductor device of any of claims 15 to 33, wherein the device comprises a discrete, self-supporting device.

Abstract

A vertical magnetic structure for integrated power conversion

The present invention provides an inductor device comprising one or more interconnected columns of conductive material embedded in a supporting structure, wherein the one or more columns comprise an input terminal and an output terminal; and wherein each column is surrounded by a first magnetic layer.

[Figure 1a]

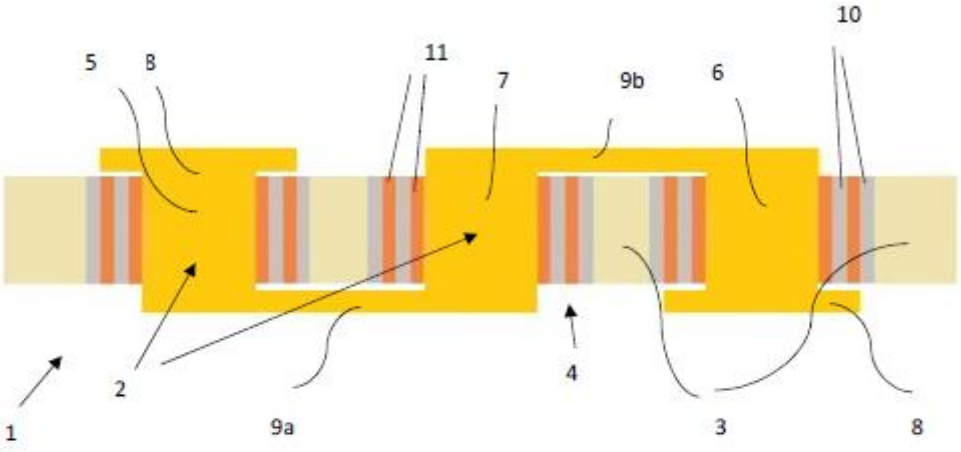


Figure 1a

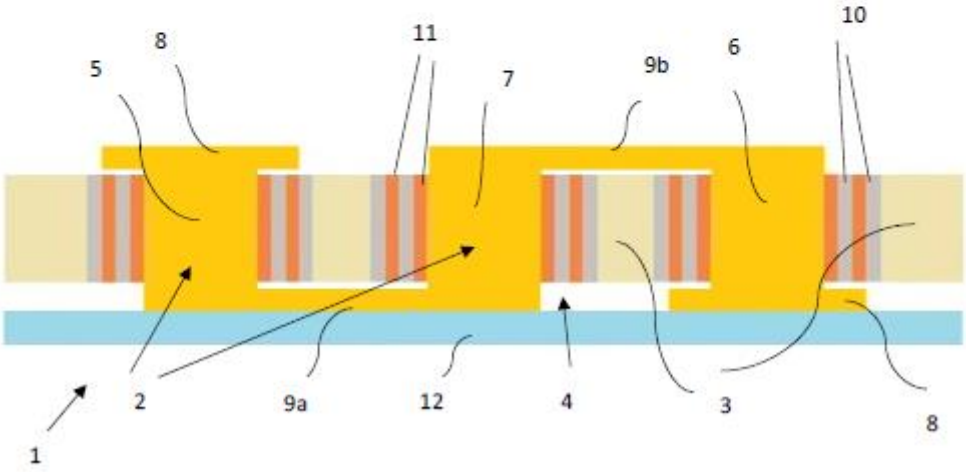


Figure 1b

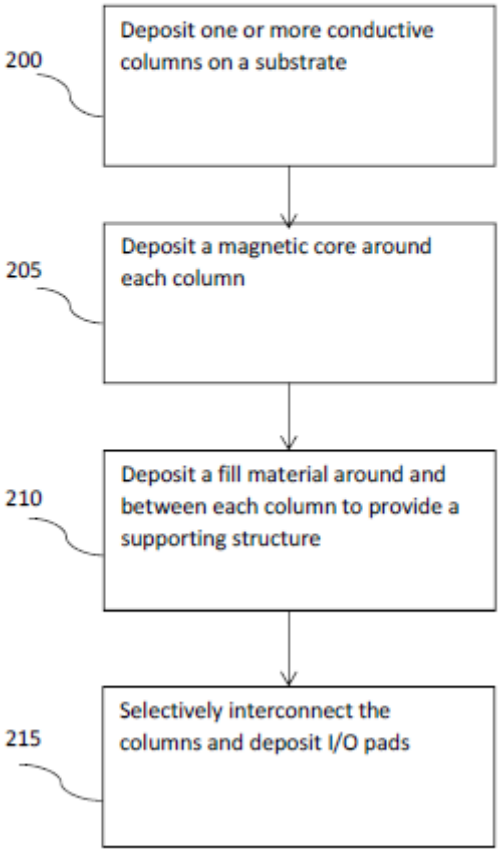
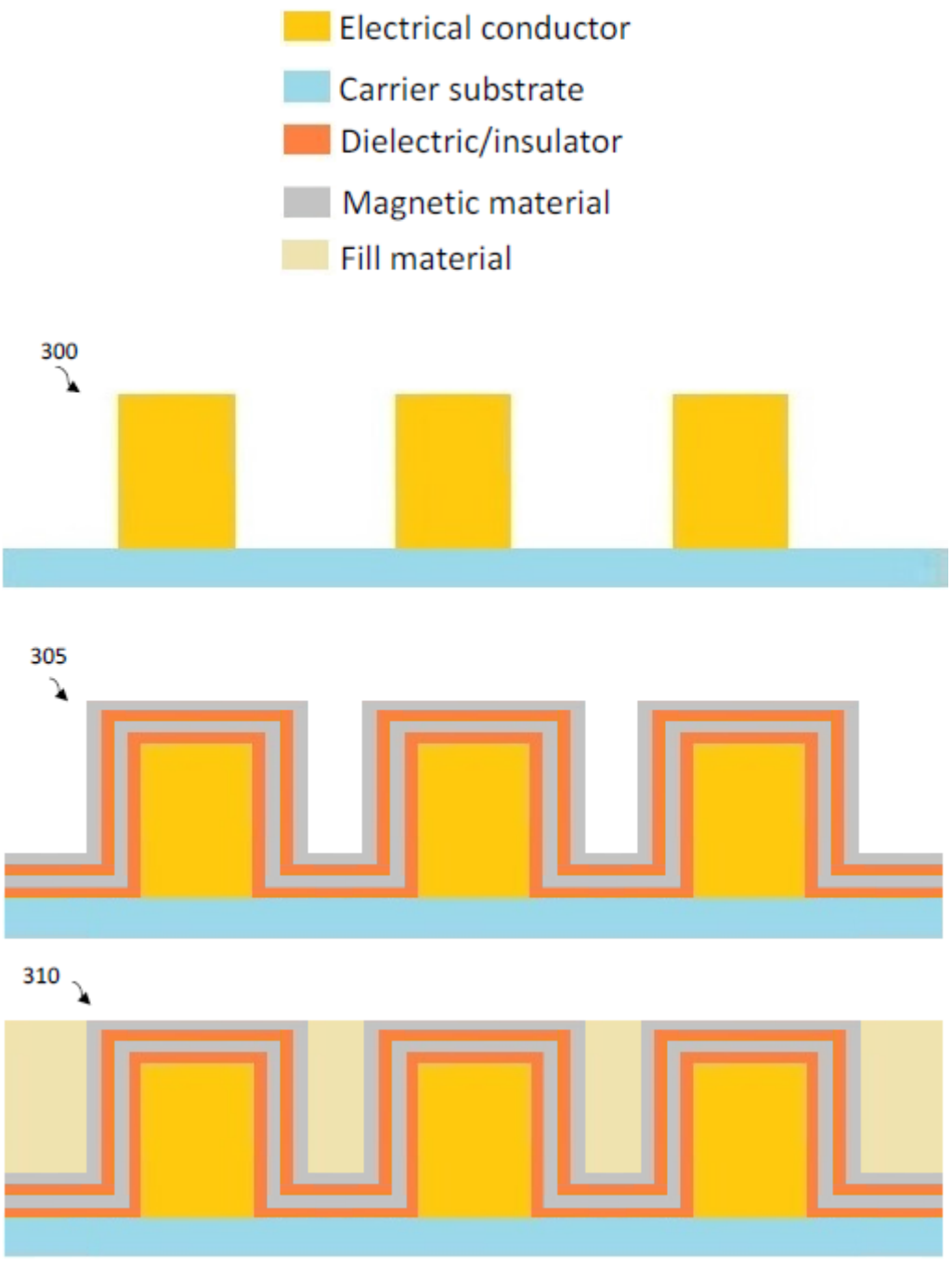
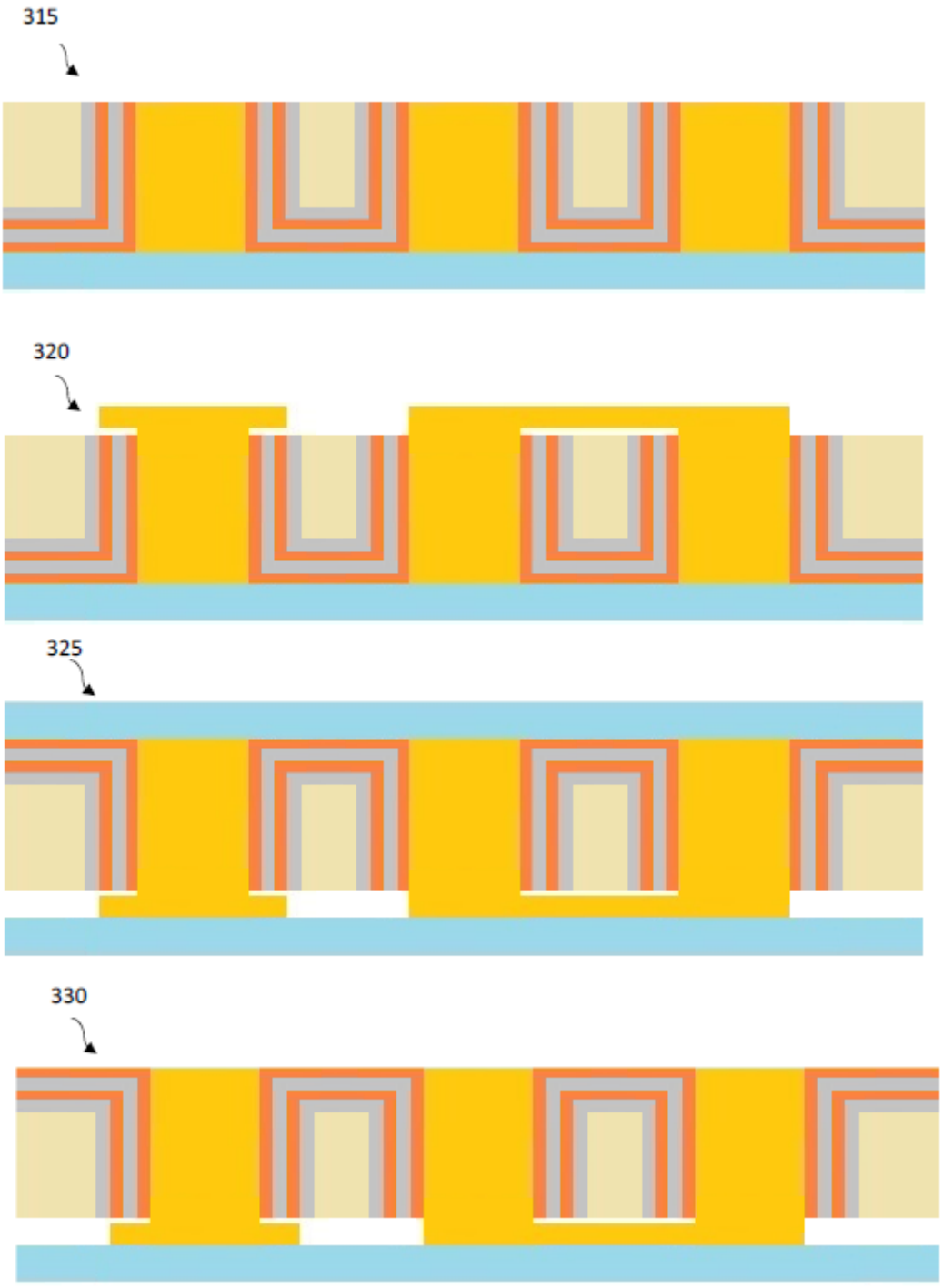

200
Deposit one or more conductive columns on a substrate
205
Deposit a magnetic core around each column
210
Deposit a fill material around and between each column to provide a supporting structure
215
Selectively interconnect the columns and deposit I/O pads

Figure 2


Electrical conductor
Carrier substrate
Dielectric/insulator
Magnetic material
Fill material
300
305
310


315
320
325
330

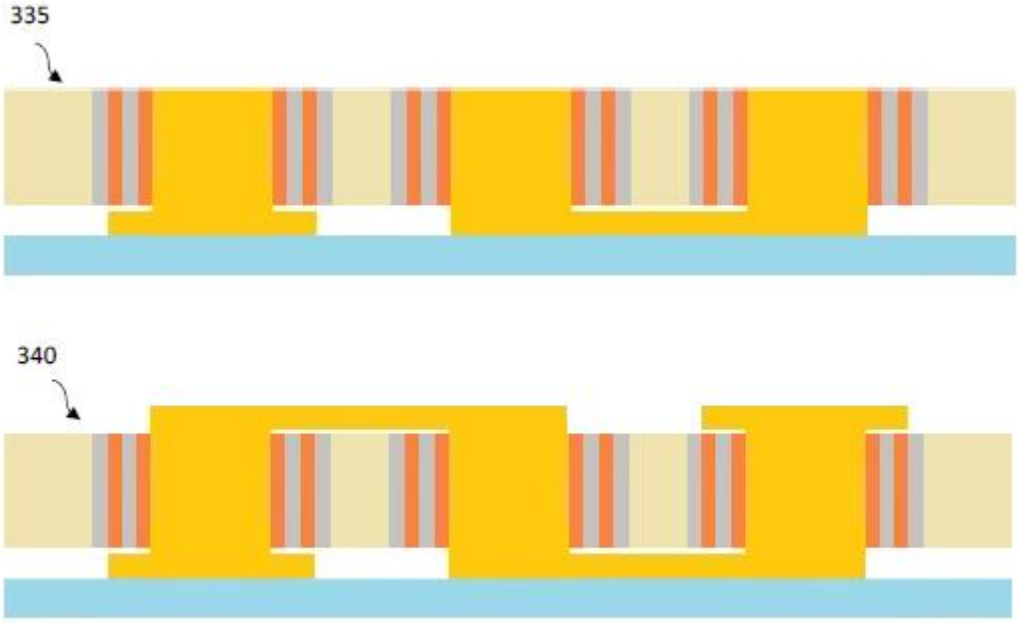
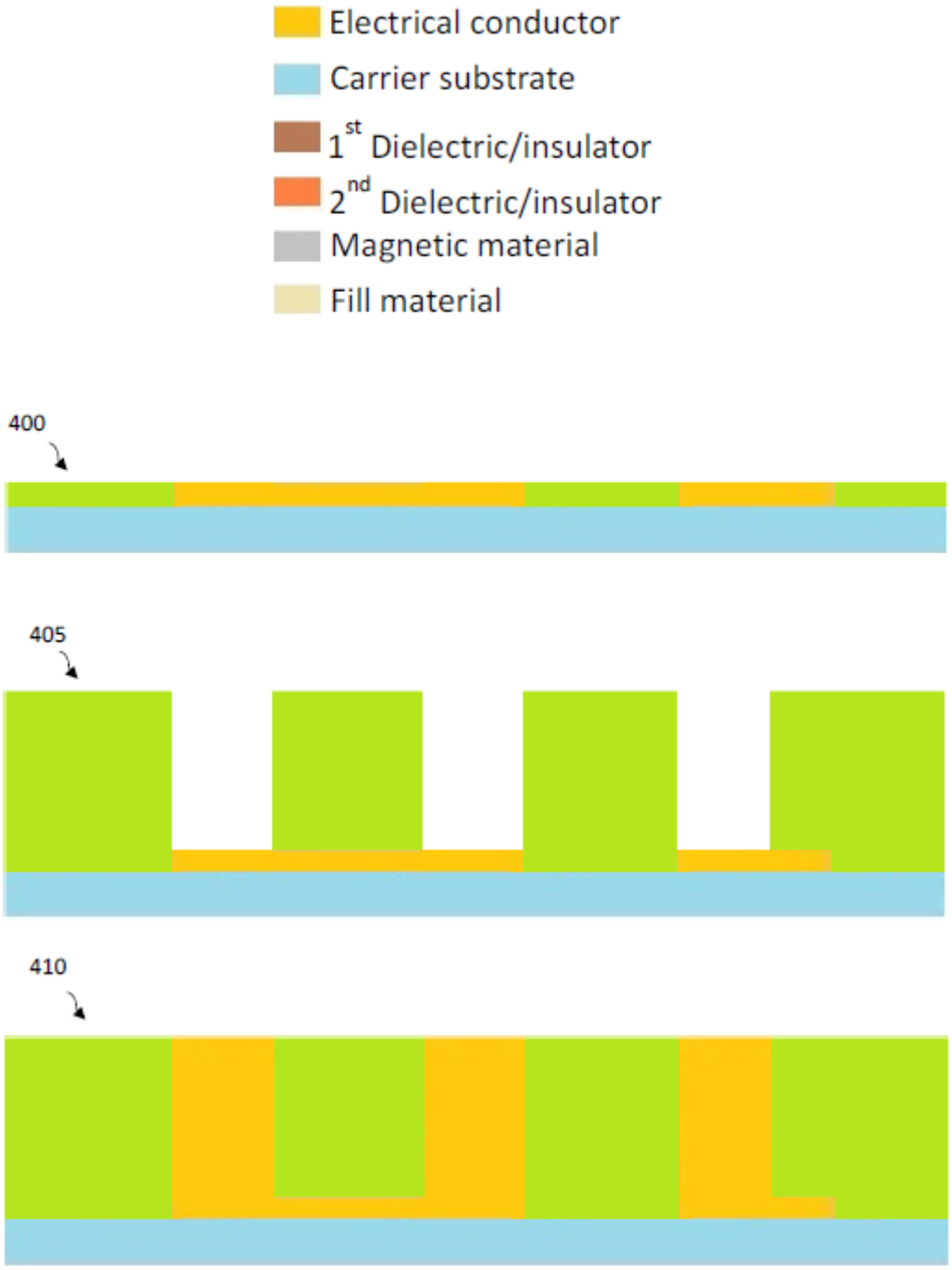
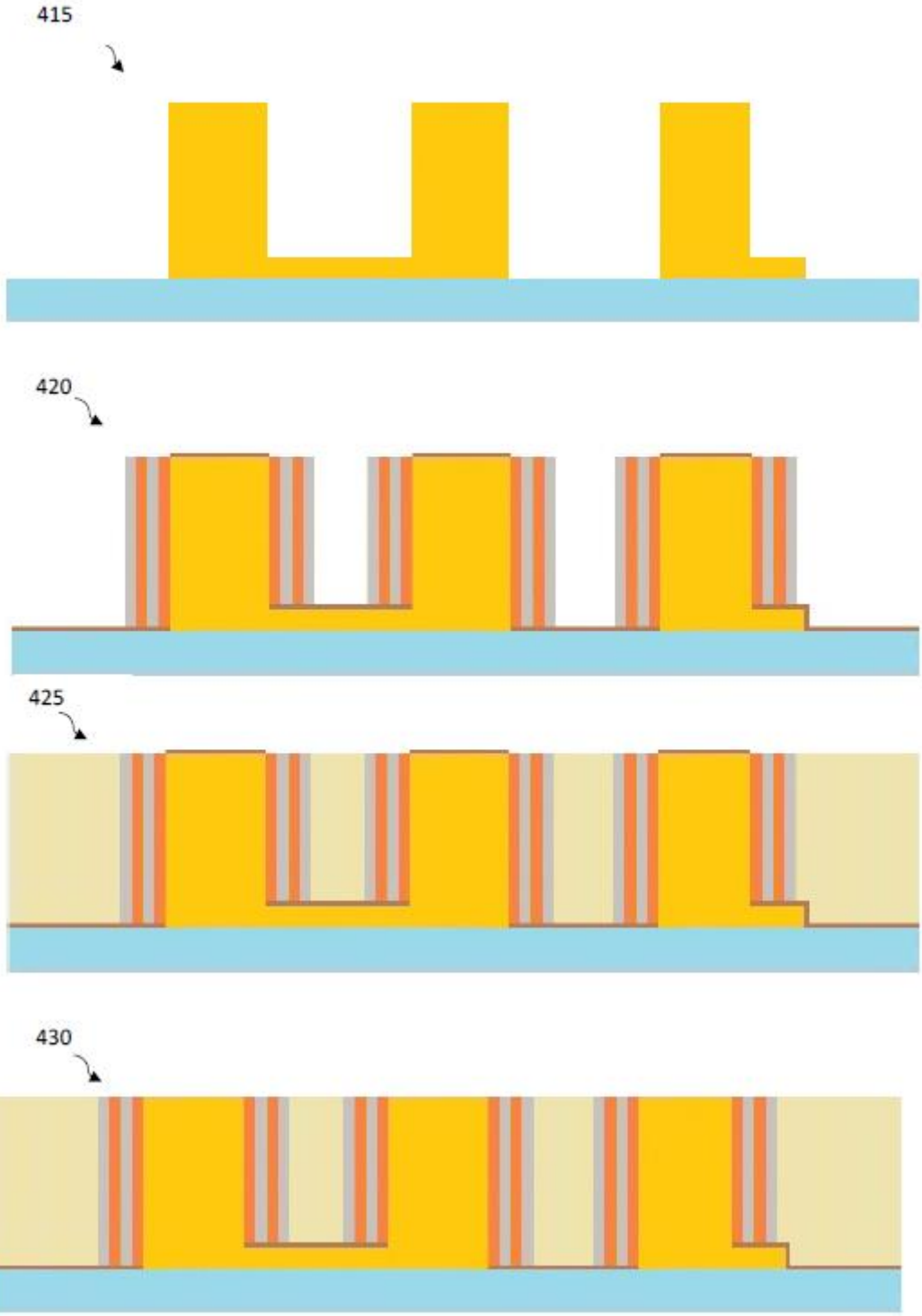


Figure 3


Electrical conductor
Carrier substrate
1st Dielectric/insulator
2nd Dielectric/insulator
Magnetic material
Fill material
400
405
410


415
420
425
430

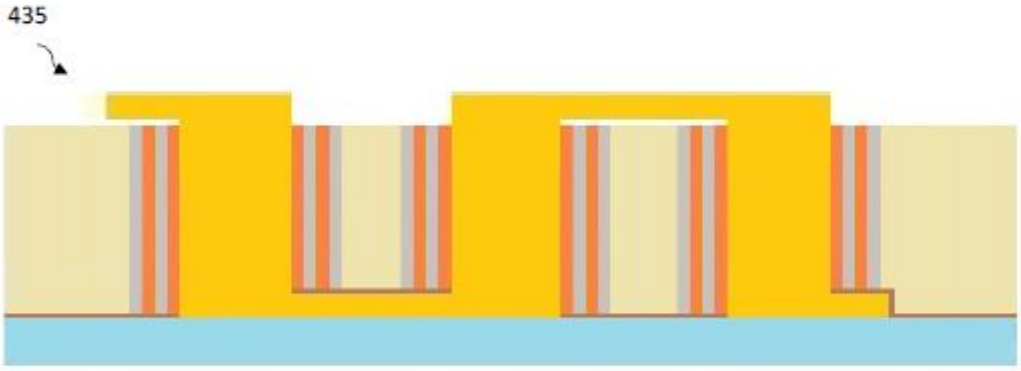
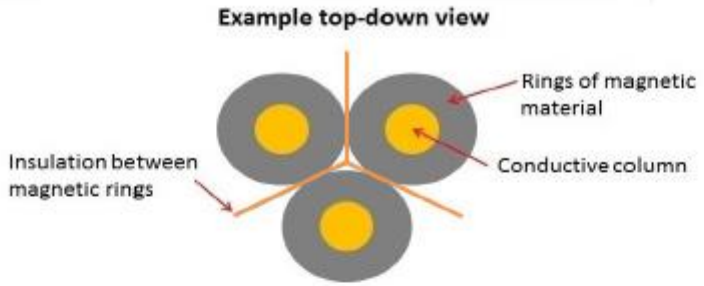


Figure 4



(a)

Side view

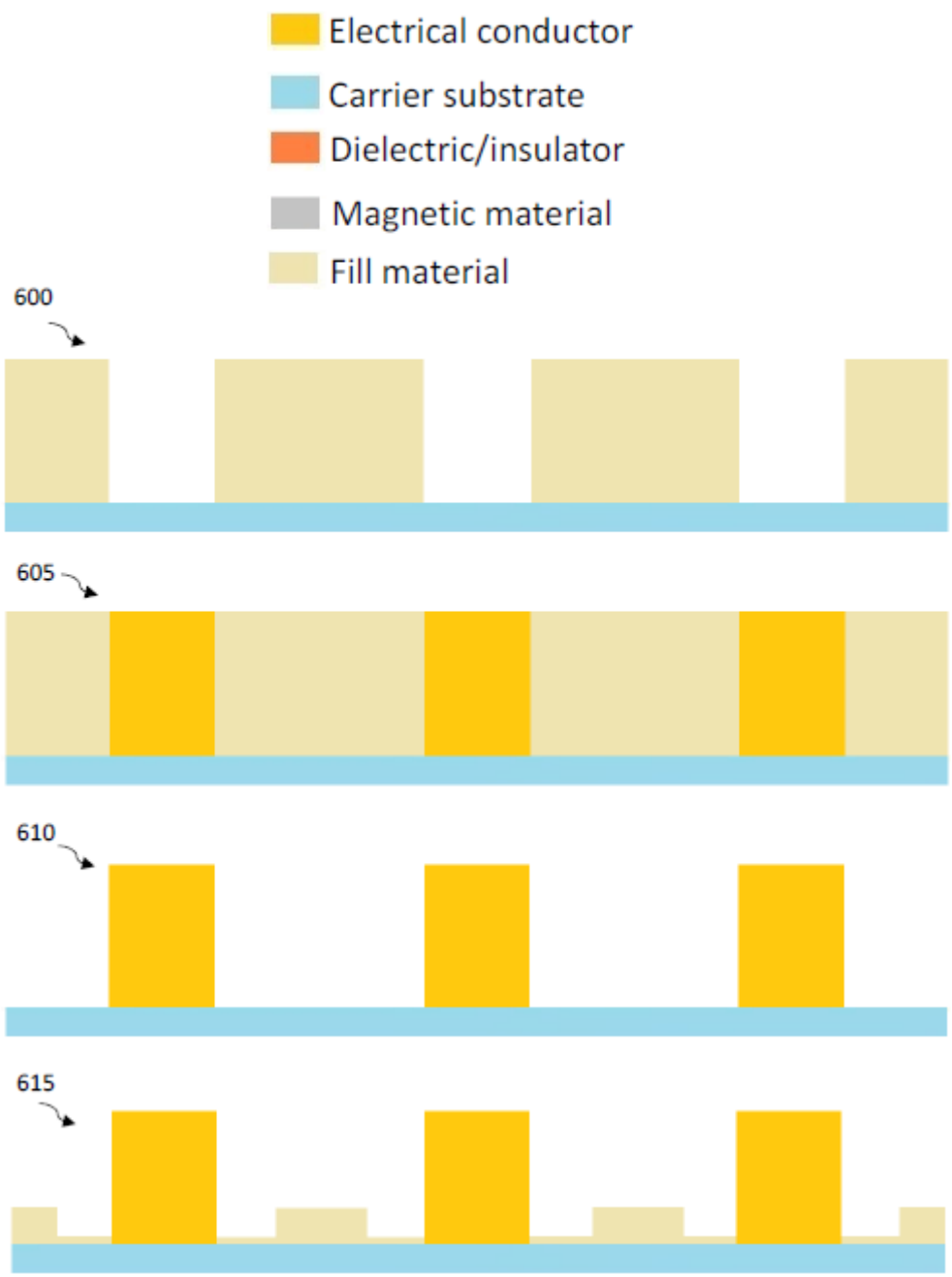
A solid sheet of magnetic material surrounds the columns and acts as a supporting structure (b)

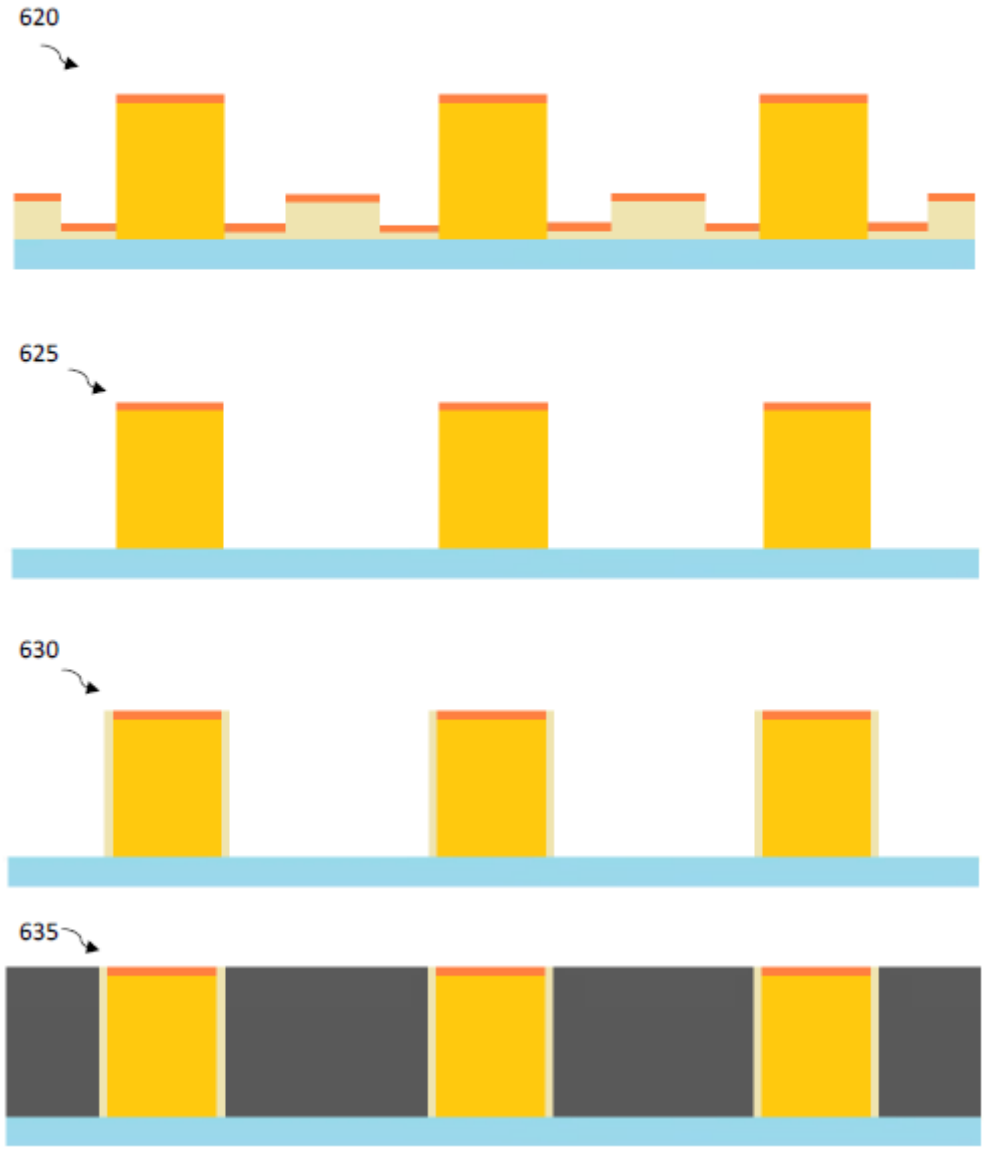
Solid rings of magnetic material surround the columns (c)

A laminated solid sheet of magnetic material surrounds the columns (d)

Laminated rings of magnetic material surround the columns (e)

Figure 5


Electrical conductor
Carrier substrate
Dielectric/insulator
Magnetic material
Fill material
600
605
610
615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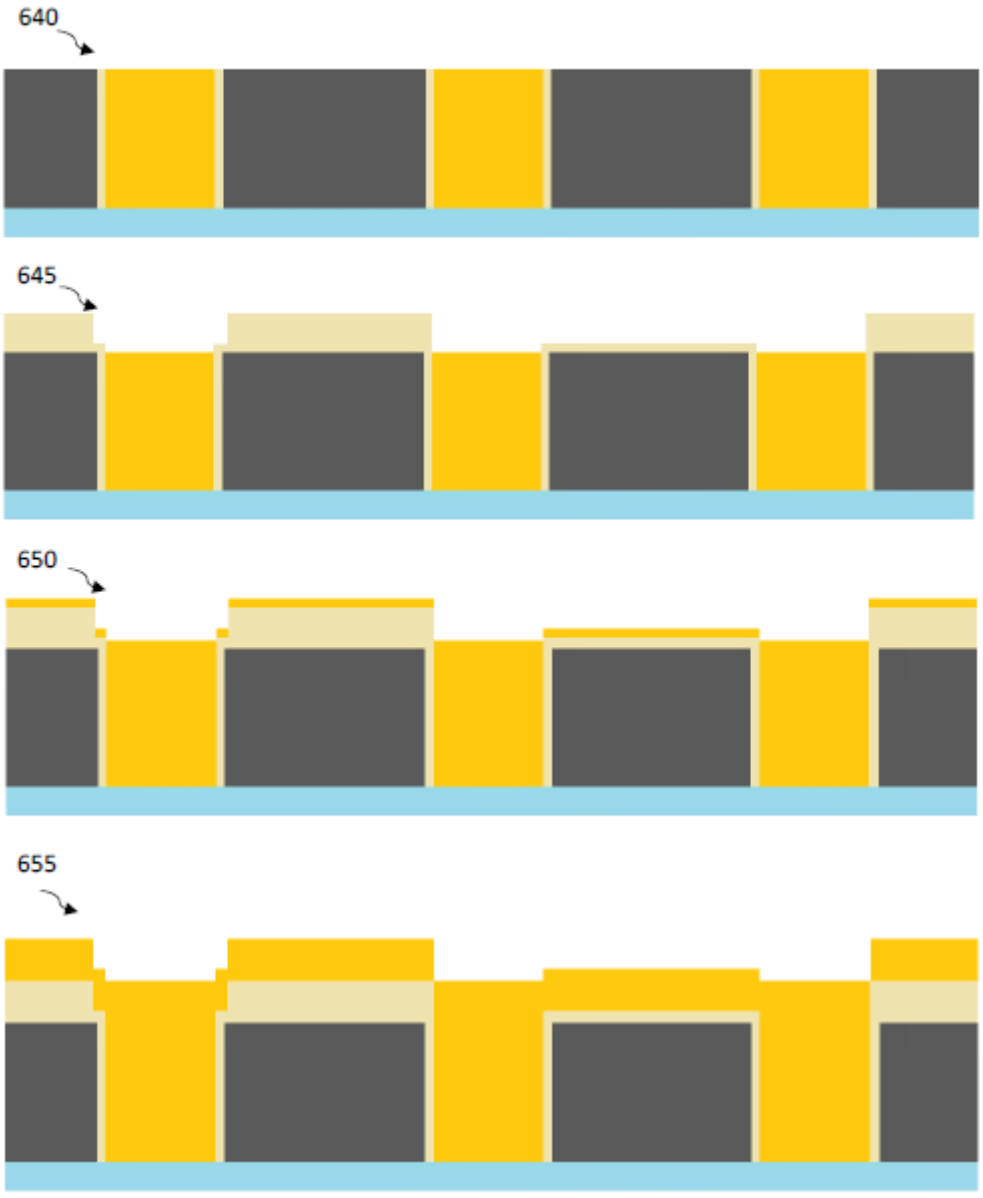
630
635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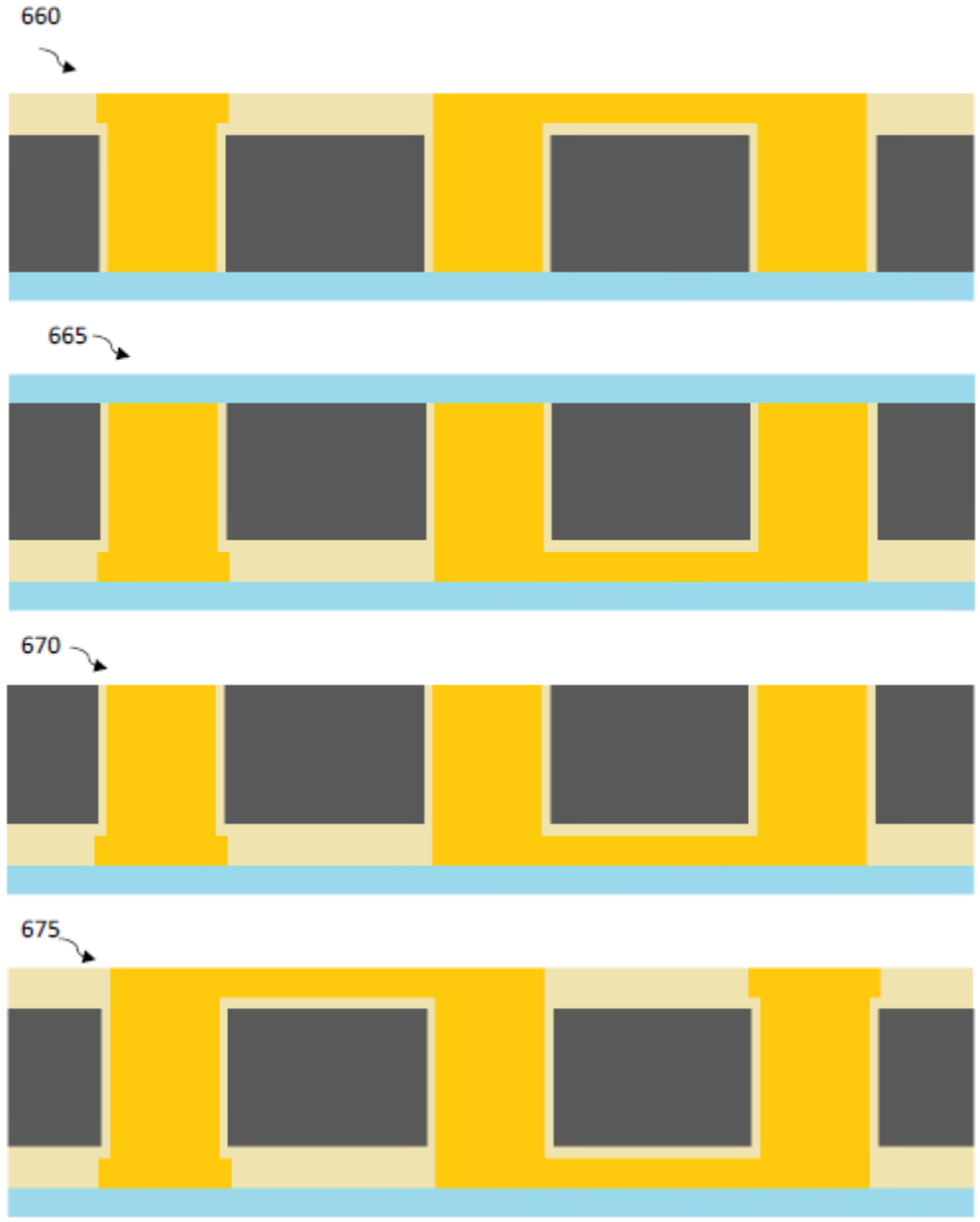
650
655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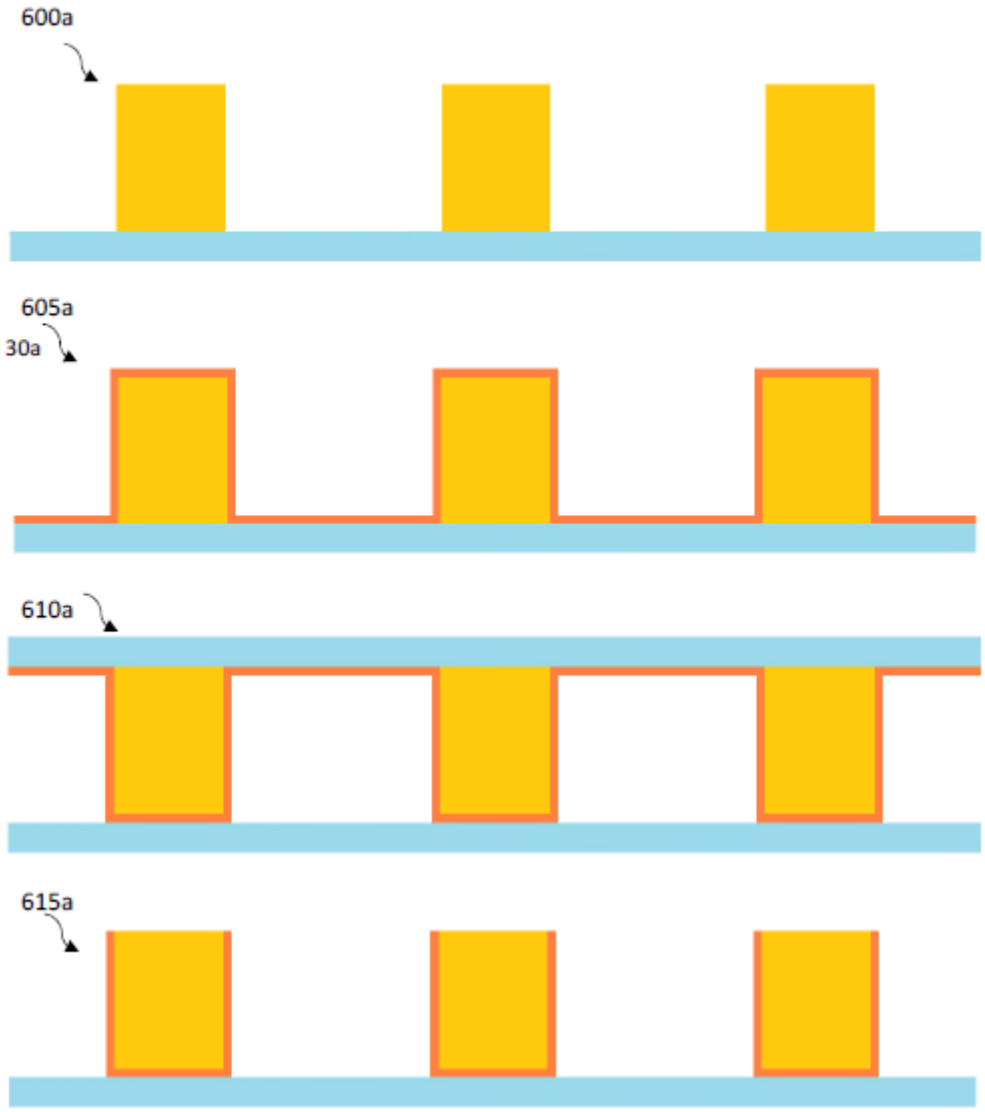
600a
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30a
610a
615a

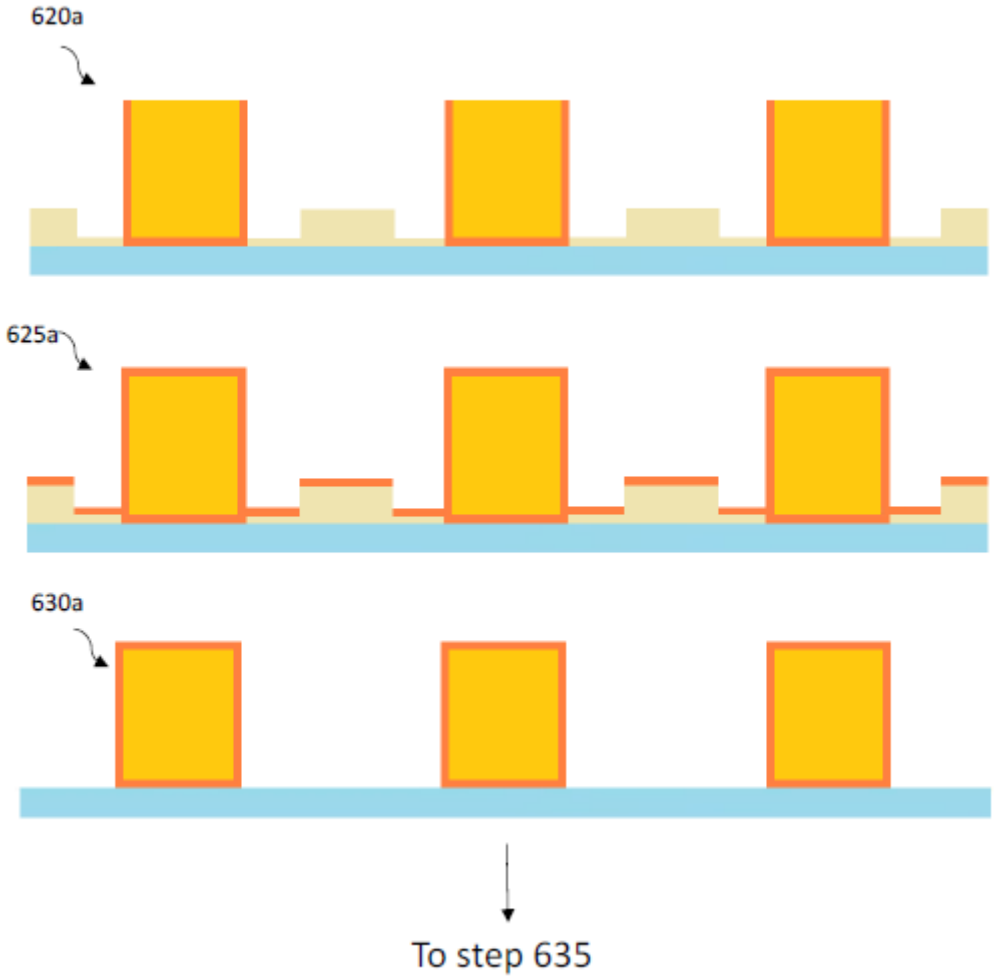
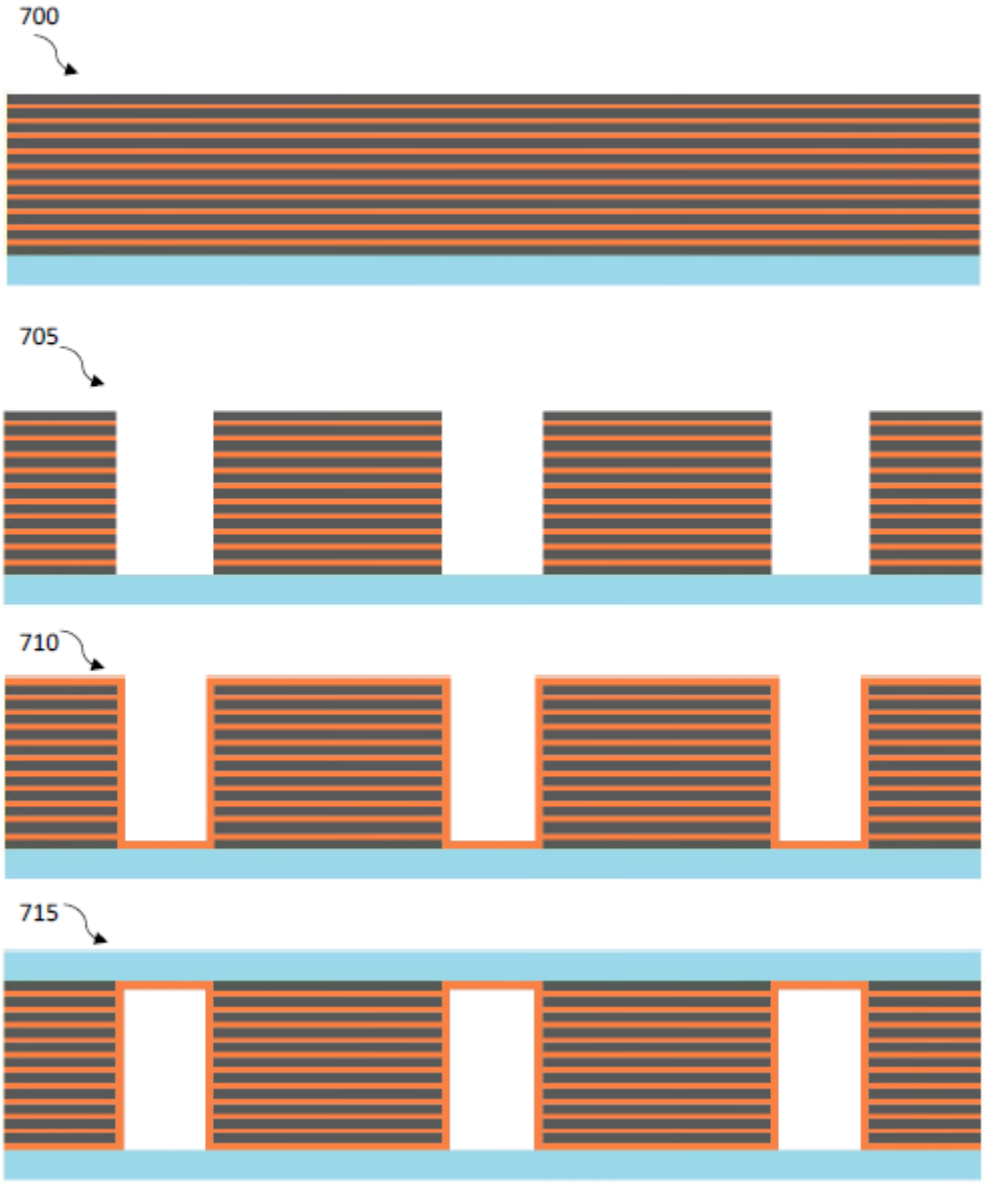


Figure 6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705
710
715

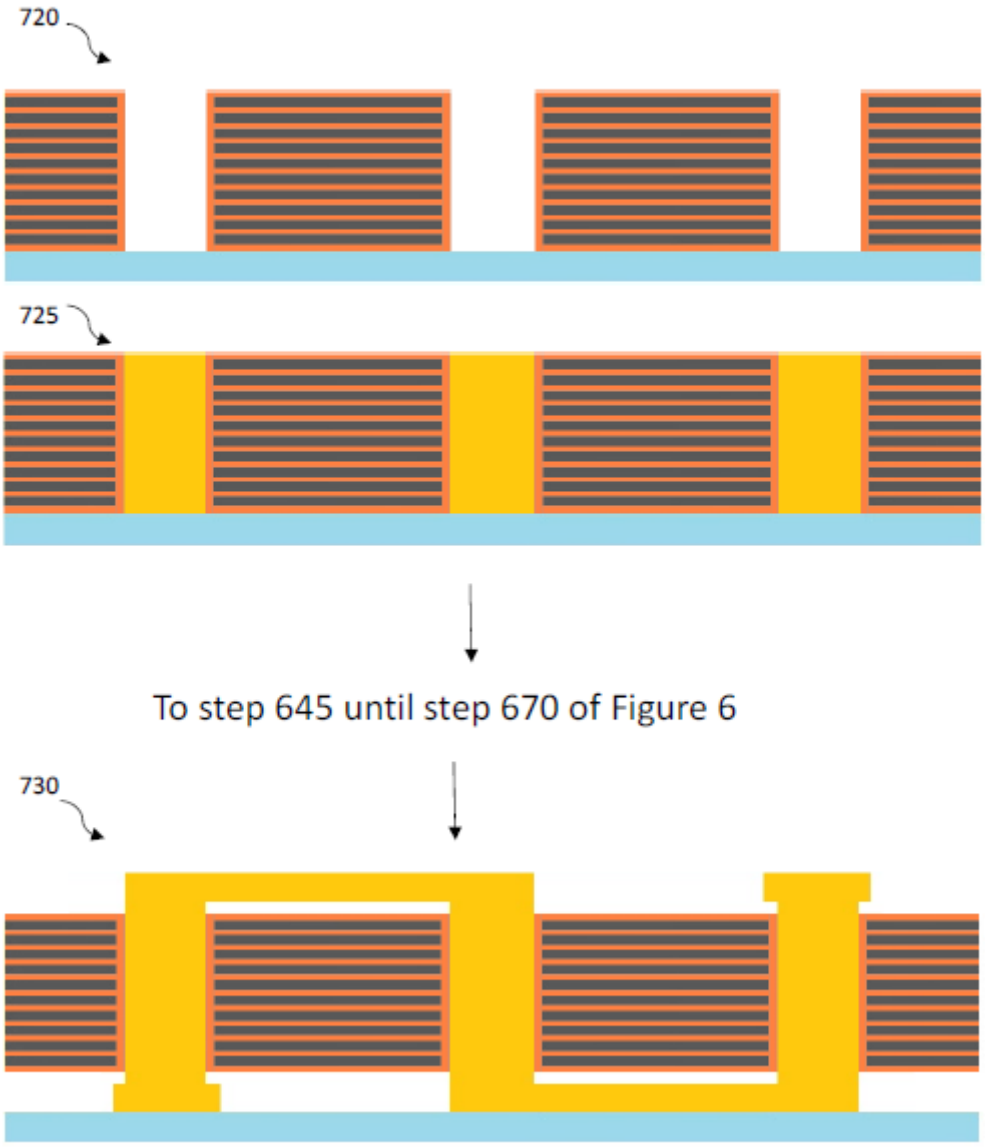
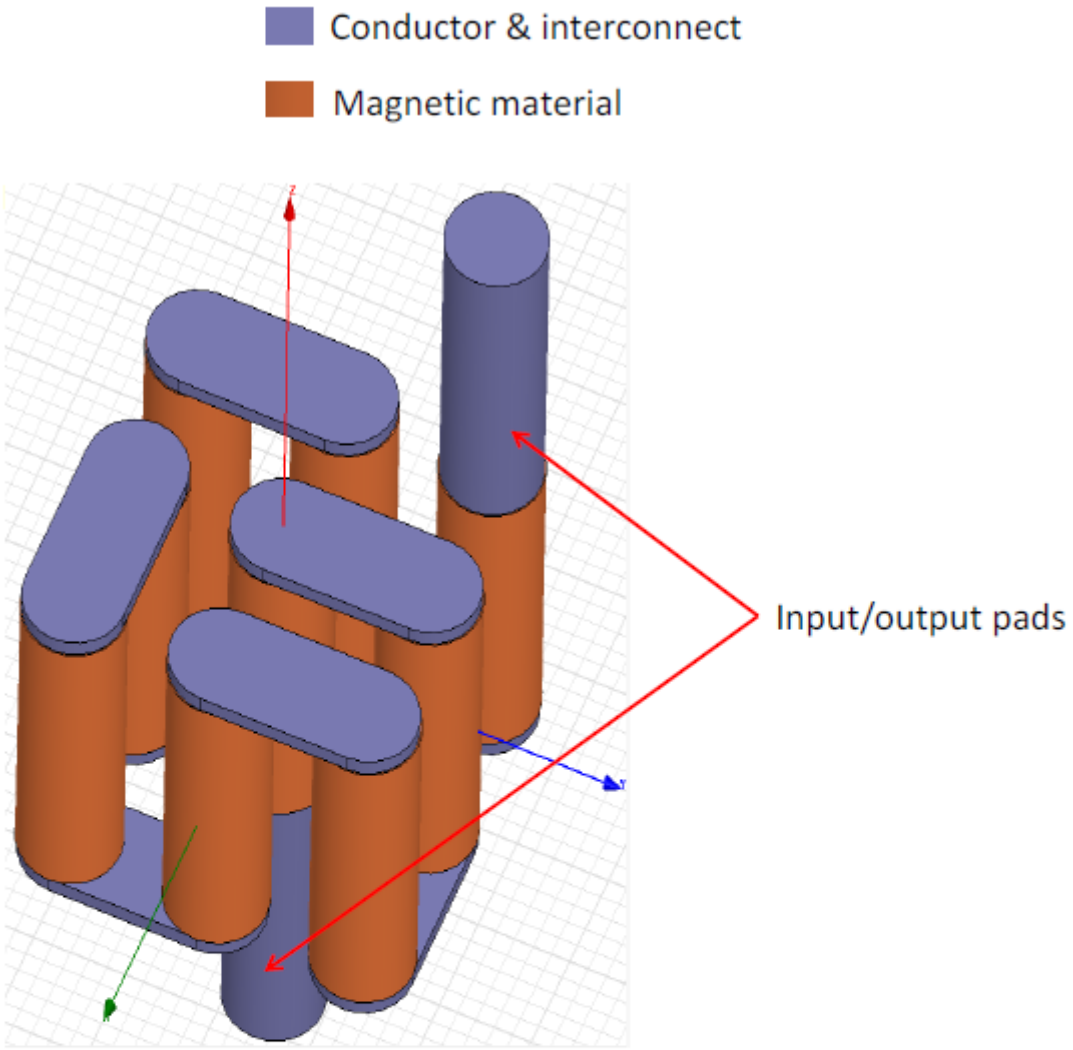


Figure 7



Pillar cross section - 90° angled view

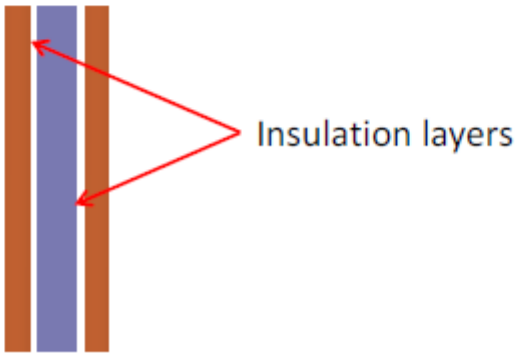


Figure 8

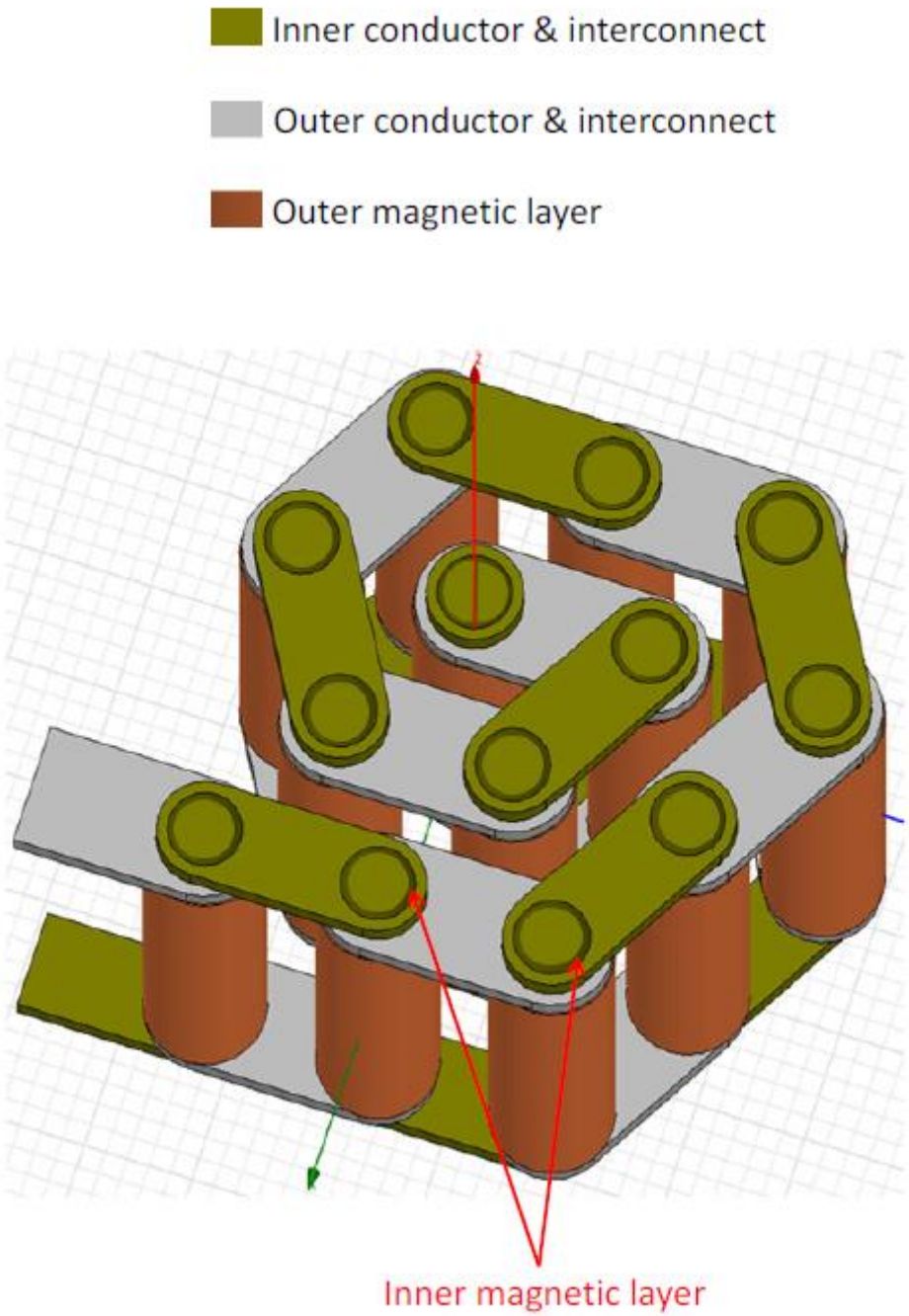

Inner conductor & interconnect
Outer conductor & interconnect
Outer magnetic layer
Inner magnetic layer

Figure 9a

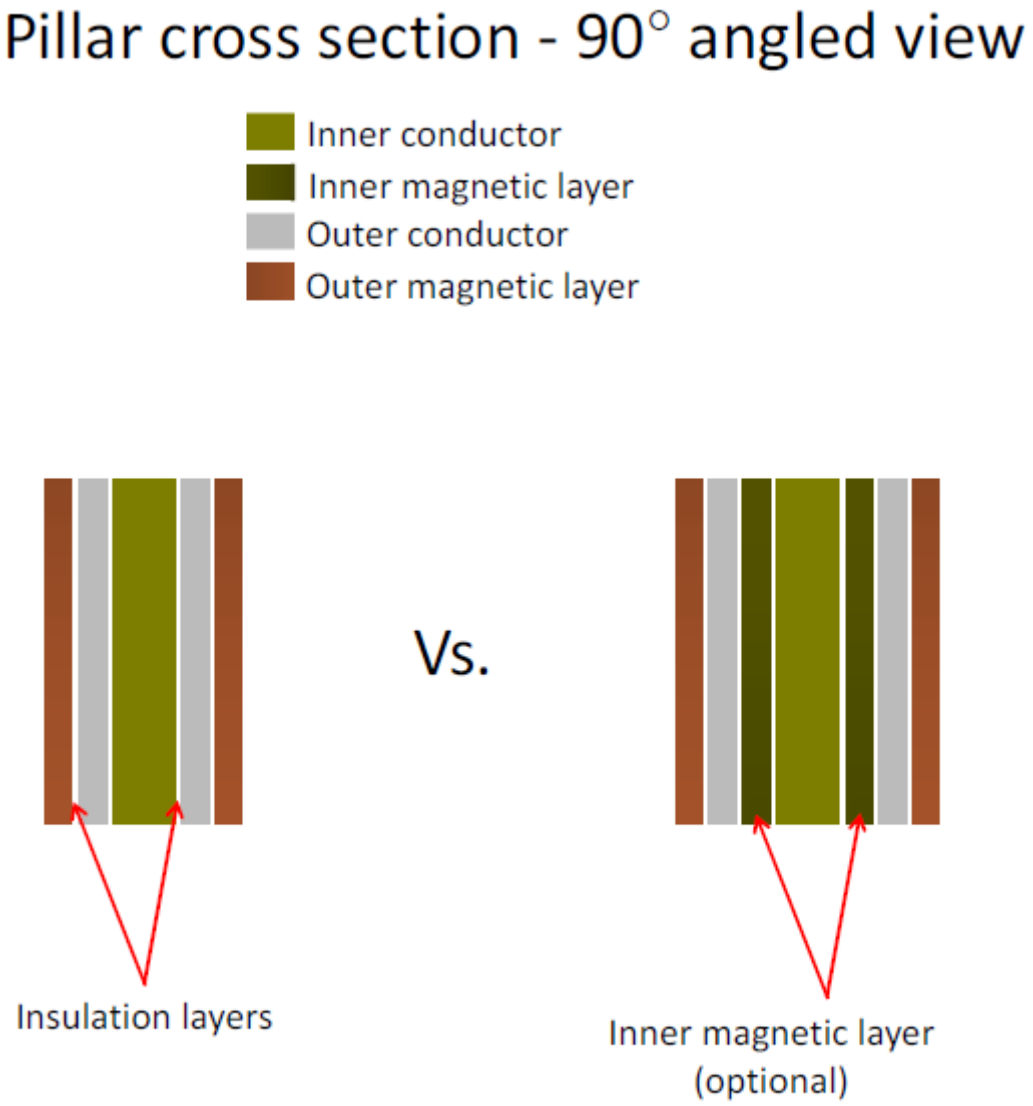
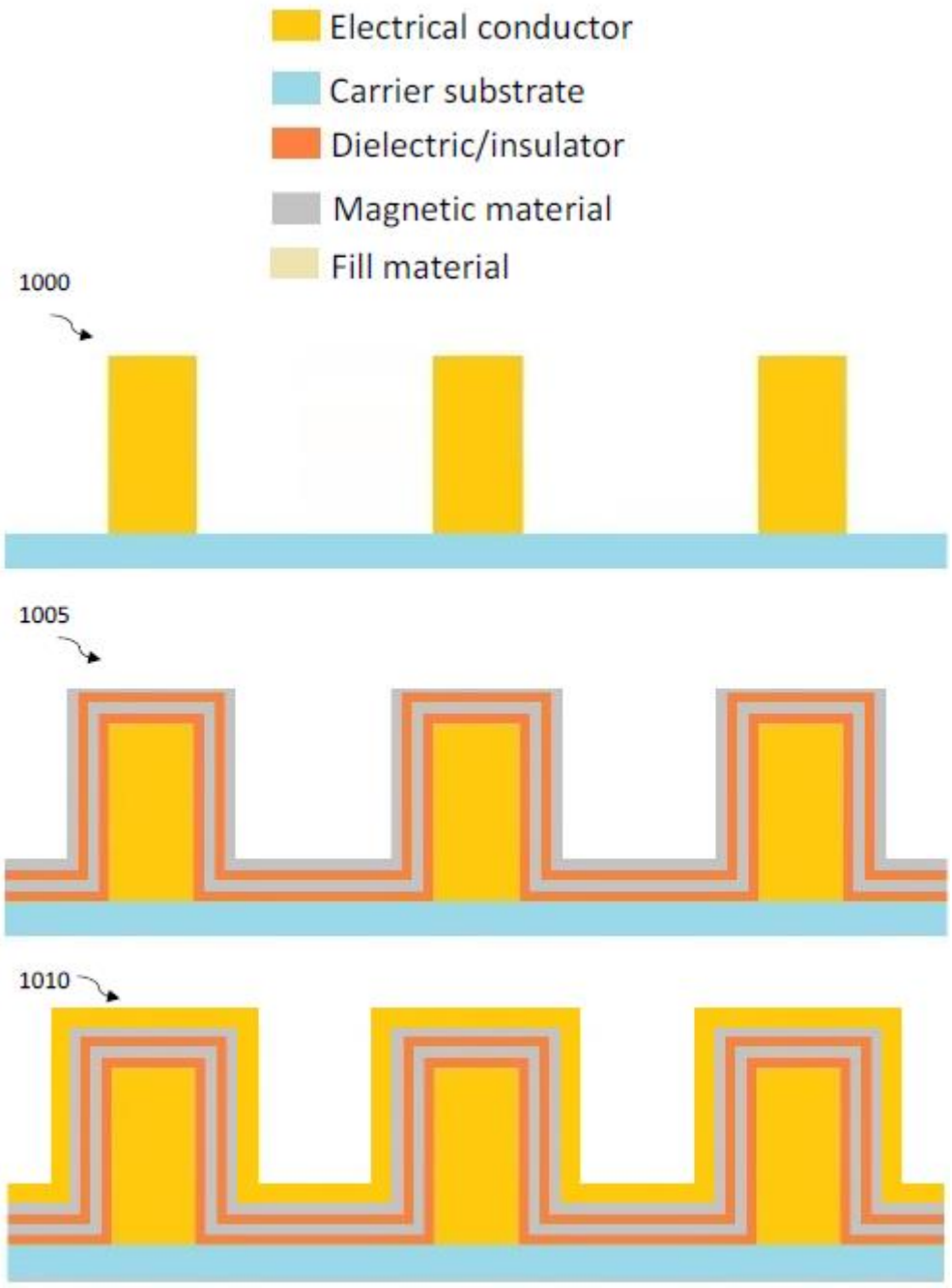

Pillar cross section - 90° angled view
Inner conductor
Inner magnetic layer
Outer conductor
Outer magnetic layer
Vs.
Insulation layers
Inner magnetic layer
(optional)

Figure 9b

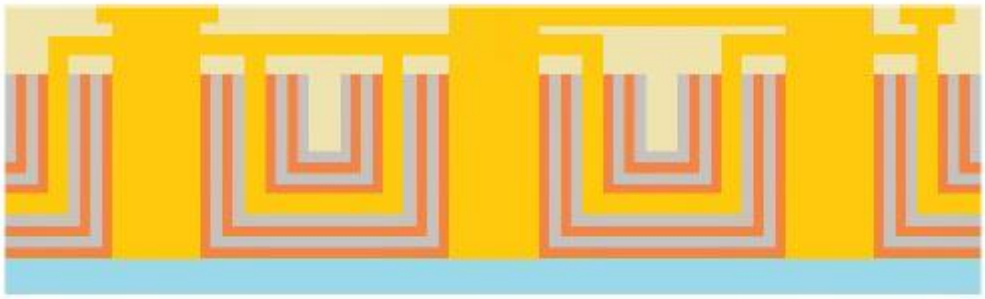

Electrical conductor
Carrier substrate
Dielectric/insulator
Magnetic material
Fill material
1000
1005
1010

1015

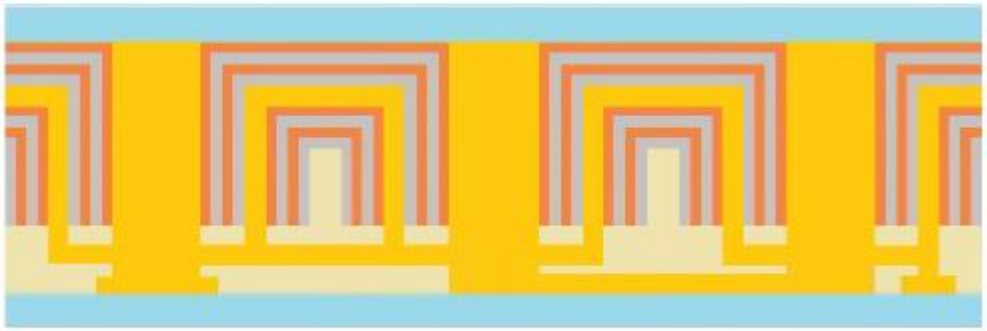
1020

1025

1030



1035



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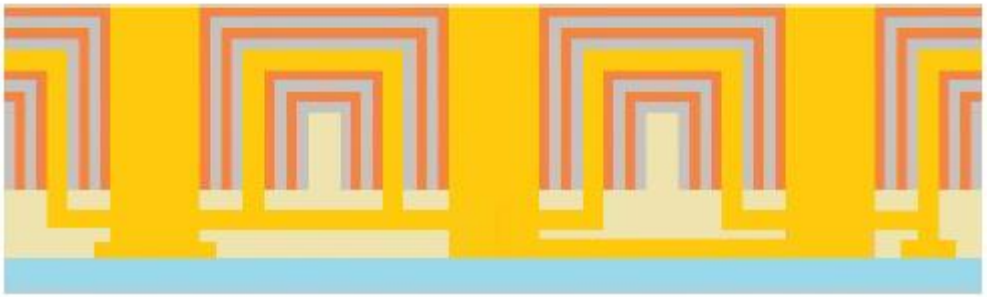


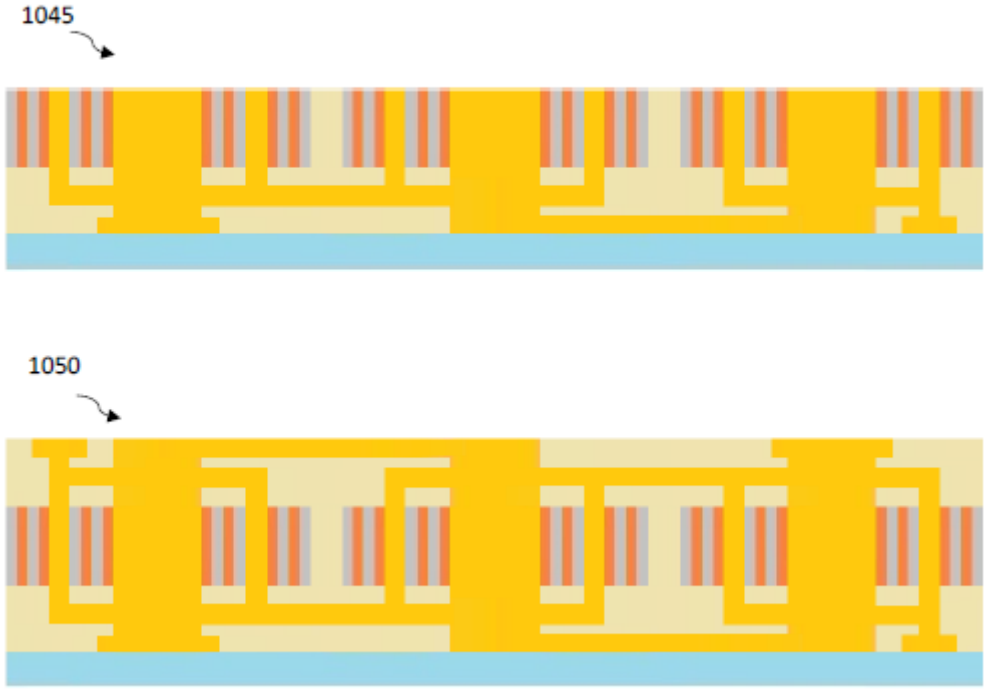


Figure 10

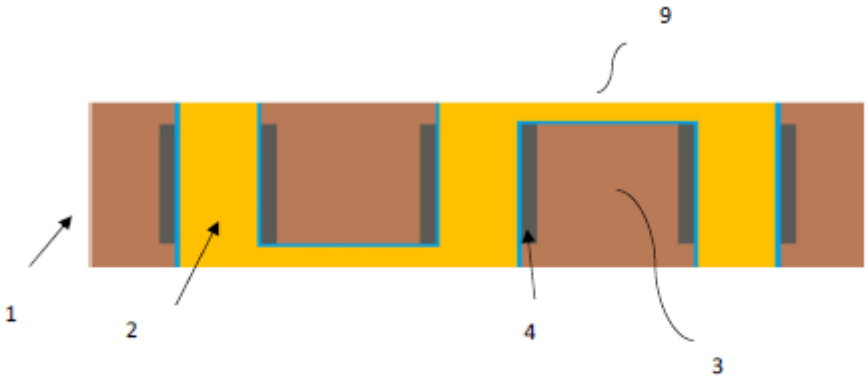


Figure 11

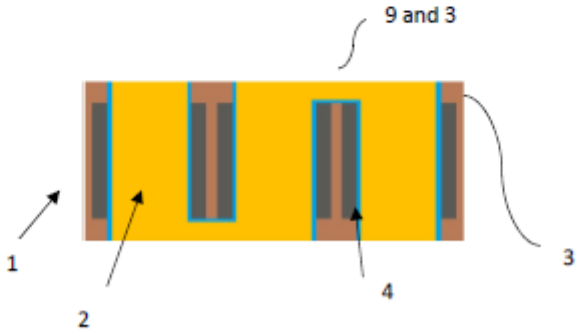


Figure 12

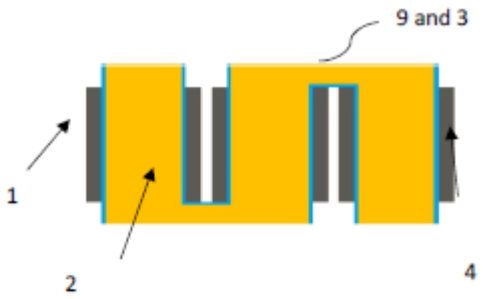


Figure 13

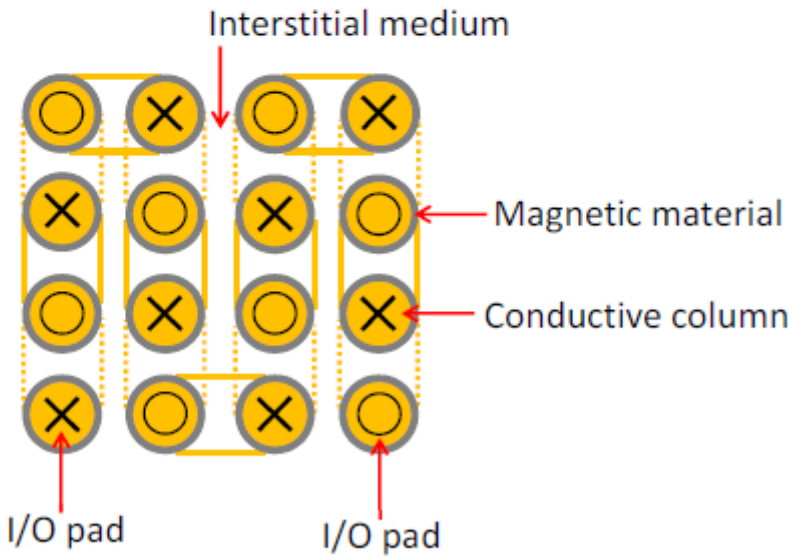


Figure 14

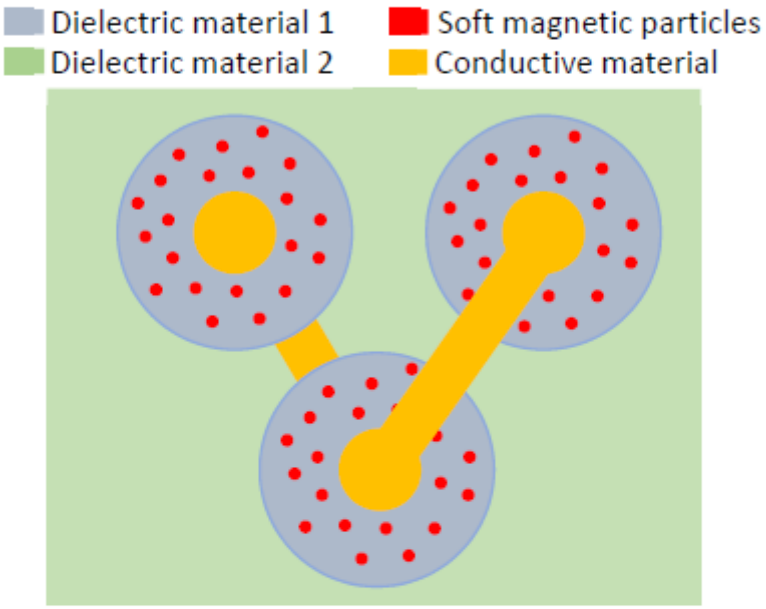


Figure 15

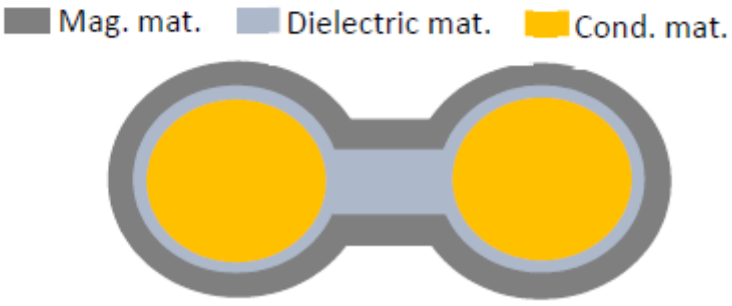
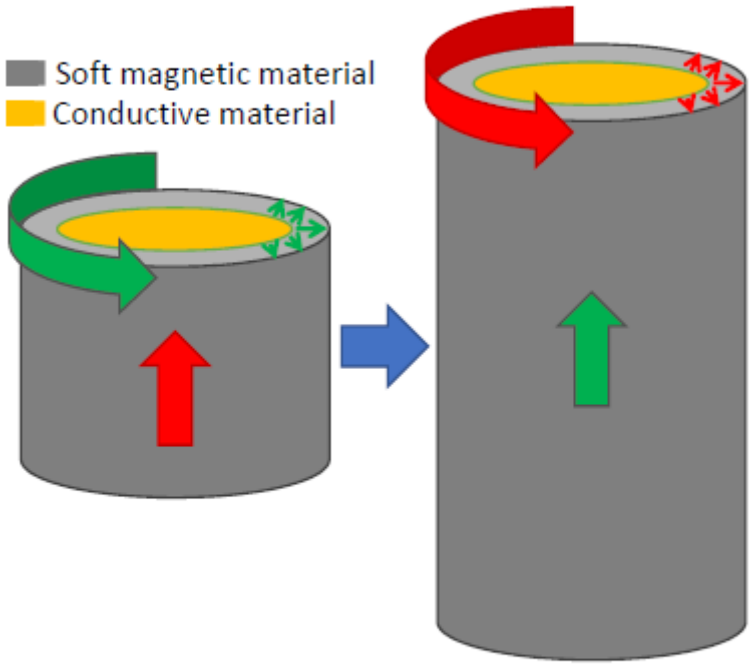


Figure 16



(a) (b)

Figure 17

Appendix VI: Enabling CMOS compatibility in the plating lab

Project Title

Advanced Integrated Power Magnetics Technology- From Atoms to Systems (ADEPT)

Project ID No.

15/IA/3180

Report Title

Enabling CMOS Compatible Processing in the Plating Lab

Report Date

3 December 2018

Author's Name

Daniel Smallwood

Table of Contents

List of Figures

1 Executive Summary

A section of the plating lab was converted and reserved for complementary metal-oxide-semiconductor (CMOS) compatible processing. This enables fabrication work carried out in the plating lab to be transferred directly to the microelectromechanical systems (MEMS) fab, a CMOS compatible facility, for further processing. Specifically, copper (Cu) pillars can now be fabricated in the plating lab via a process that is entirely free of contaminant elements such as gold (Au), iron (Fe) and silver (Ag). Once the plating lab process flow is complete, the wafers are then transferred to the MEMS fab for sputter deposition in a state-of-the-art sputtering machine. During this step, a magnetic core is deposited around the copper pillars, where the magnetic core is in the form of alternating laminations of thin layers of aluminium nitride (AlN) and cobalt-zirconium-tantalum-boron (CZTB). In short, this conversion process has enabled vertically-oriented magnetic device fabrication research to be investigated by additional members of the SFI ADEPT team, which will significantly accelerate our research progress.

2 Methods

A dedicated fume hood was commissioned in the plating lab for this CMOS compatible work. Fume hood installation entailed installing an exhaust vent for the extract, DI water lines for the sink input and drain, and pressurized nitrogen for drying wafers. The fume hood itself was acquired from the e-beam lab for free, which was a huge cost savings. The fume hood came complete with two lockable panel doors, which are used to safely store generic lab supplies like wafer tweezers, lint-free tissues, petri dishes, etc. to ensure that these things stay CMOS compatible. When not in use for this work, the power plug for the fume hood is locked to ensure that it remains CMOS compatible.

In addition to the fume hood, uncontaminated machinery was also acquired. A Laurell Technologies spin coater was transferred from the MEMS fab, which was originally purchased through a previous project entitled Carricool. This particular spin coater has a syringe dispense mechanism installed on the top for doing edge bead removal (EBR), which is very important feature for enabling uniformity with thick photoresist.

A dual hotplate, also purchased during the Carricool project, was also transferred from MEMS. Since it has two different plates, this dual hotplate is perfect for quickly performing baking and cool off steps during lithographic processing.

An Elmasonic P30H ultrasonic bath was acquired for assisting with the development step. Current simulations show that ideal copper pillar dimensions are 50um X 100um (diameter X height). To enable this, the ultrasonic bath is used at 80kHz to induce nano-scale cavitation inside micron-sized feature holes, which dramatically increases developer efficacy.

A Grant Instruments PS-M3D orbital rotator was acquired for assisting with resist stripping. According to the technical datasheet (TDS) for the resist we are currently working with, THB-151N, the stripping process requires 30 mins of constant agitation in puddle mode. The stripper is tetramethylammonium hydroxide (TMAOH) based and is acutely toxic, flammable, corrosive and is also a health hazard. As such, manual agitation, which often involves spillage, especially after a long duration in a petri dish in puddle mode, is far from ideal. The orbital rotator thus enables a repeatable, dependable and safe way to strip our thick photoresist.

A Canon PLA600F broad spectrum mask aligner was acquired from the MEMS fab and installed in the plating lab, which was another huge cost savings. This mask aligner has a CMOS compatible chuck and a duplicate chuck that we had machined in-house for non-CMOS compatible work, if necessary. When not in use for this work, the power plug for the mask aligner is locked to ensure that it remains CMOS compatible.

Additional glassware was needed to be purchased for this work, as all of the pre-existing glassware in the plating lab was likely contaminated with either or all of Au, Ag and Fe. The list of glassware is: 2X 500 mL polymethylpentene (PMP) graduated cylinders for performing fine volumetric measurements, 1X borosilicate glass storage bottle for storing S20 Cu cleaner, 2X Teflon evaporating dishes for buffered oxide etch (BOE), 2X borosilicate glass crystallization dishes for developer solution, 10X borosilicate glass petri dishes with lids for puddle work, 2X 1L borosilicate glass beakers for additional puddle work and resist development, and a micro spoon and spatula kit.

Additional chemicals were also acquired: THB-151N photoresist (PR) – 1Q, TMA238WA developer - 4x5L, THB-S17 PR stripper – 5L, AZ EBR solvent – 5L, AZ IPS-6050 PR – 1L, TechniStrip P1331 PR stripper – 5L, AZ 726 MIF developer – 5L, a free sample of AZ 40XT PR – 100 mL, and 99.5% acetone – 1L.

All of the above, the chemicals, the generic lab supplies, the small machinery, etc. is too much to fit in the fume hood and the lockable fume hood panel doors. As such, a cabinet in the plating lab that was left over from the Carricool project was cleaned and dedicated for CMOS compatible equipment/materials storage.

3 Process Flow and Description

The process flow has been approved by both the head of the Process and Product Development Group, as well as the engineering supervisor for the MEMS fab. Figure 1 shows the fabrication process, which entails all of the CMOS compatible work leading up to and ending just before the magnetic core sputtering step in the MEMS fab: (1) Add a thermal oxide onto silicon (Si) wafers to create a few micron thick film of silica (SiO_2), then sputter on 20nm of titanium (Ti) followed by 200nm of Cu. (2) Transfer the wafers from MEMS to the storage cabinet in the plating lab in CMOS compatible wafer receptacles. (3) Electroplate a 10um blanket of Cu onto the Cu seeded wafer to enable electrical characterisation at a much later stage and also to simulate electroplating Cu pillars directly onto Cu interconnect (IC), which is needed for the final device with regards to the most up-to-date process schematic (submitted in SFI Adept deliverable D5.1). This step requires first cleaning the Cu seed with S20 Cu cleaner and then de-scumming in a plasma asher. (4) Clean the wafer in DI and dry in N_2 then bake on a hot plate for 5 mins at 110 °C to evaporate any residual water on the wafer surface (5) Spin coat photoresist onto the wafer, with an initial target thickness of 80um and enable EBR to optimize resist uniformity. Ensure the photoresist is warmed to room temperature (RT) prior to spinning the resist, as this is paramount to controlling the viscosity of the PR and attaining the desired film thickness. (6) Perform a soft bake of the wafer on the dual hot plate, which evaporates the resist solvent, which is slightly hydrophilic, thus increasing resist adhesion, as the PR is hydrophobic, and also increases the efficacy of the UV light (broad spectrum, i-line sensitivity), as the solvent absorbs and refracts light. (7) Expose the PR in the mask aligner and ensure the calculated exposure time uses an up-to-date measurement for the bulb intensity. (8) Perform a post-exposure bake, which further evaporates the resist solvent and increases adhesion. (9) Develop the features in a beaker submerged in the ultrasonic bath, use 80kHz to enable nano-scale cavitation. (10) Electroplate the Cu pillars and use optimized plating parameters. This involves cleaning the feature holes in S20 to remove Cu_2O on the wafer surface, perform a plasma ash to de-scum and soak in the Cu_2SO_4 plating back in a petri dish puddle to activate the feature holes. (11) Strip the PR in puddle mode with the orbital rotator, permit 30 mins. (12) Move the wafer with a blanket seed and Cu pillars back to MEMS in a CMOS compatible receptacle.

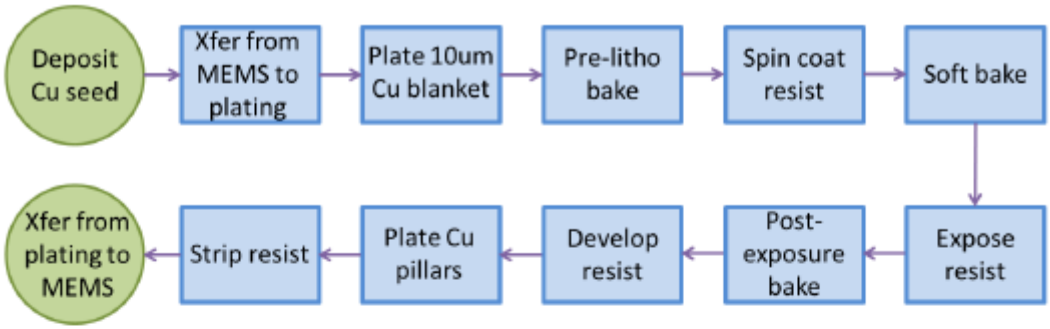
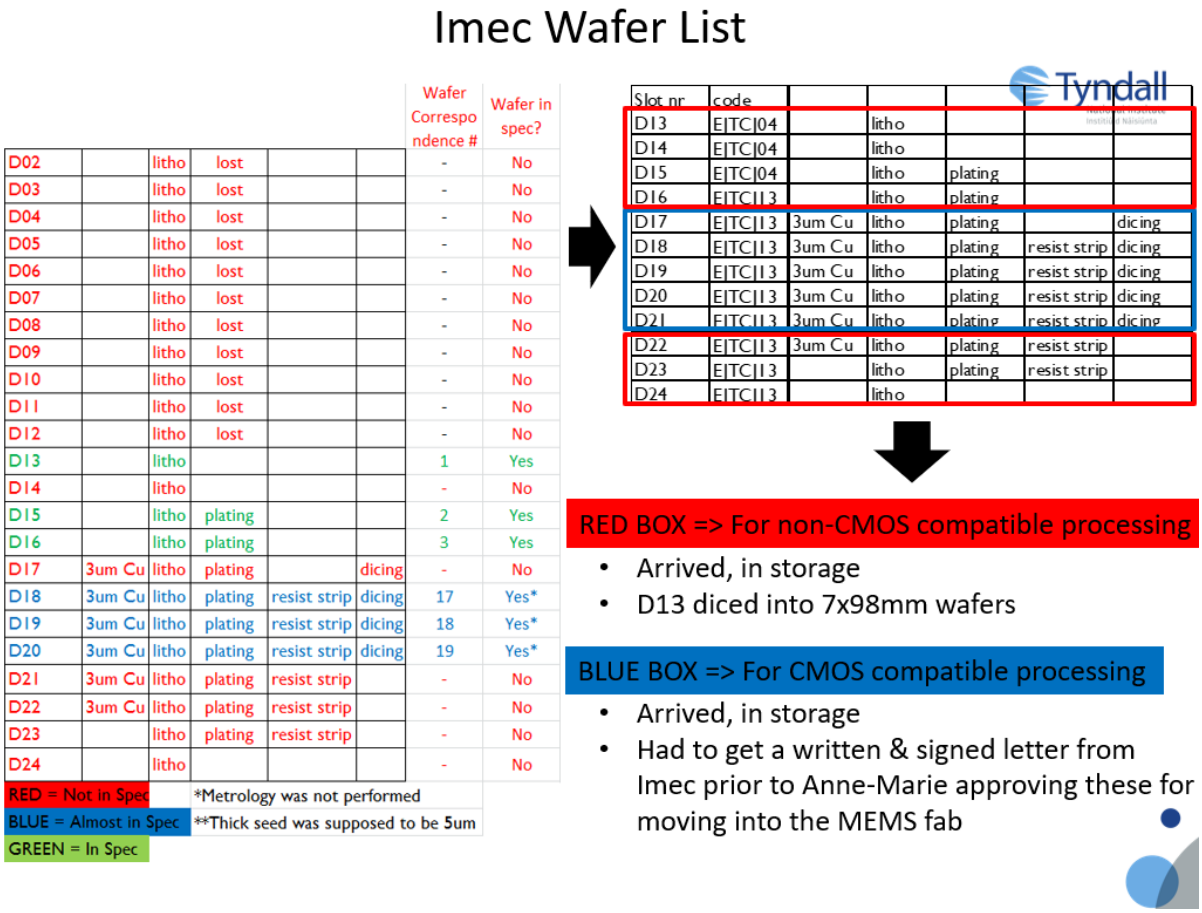


Figure 1: Process flow chart highlighting the main fabrication steps leading up to and ending just before the magnetic core sputtering on the Cu pillars in the MEMS fab.

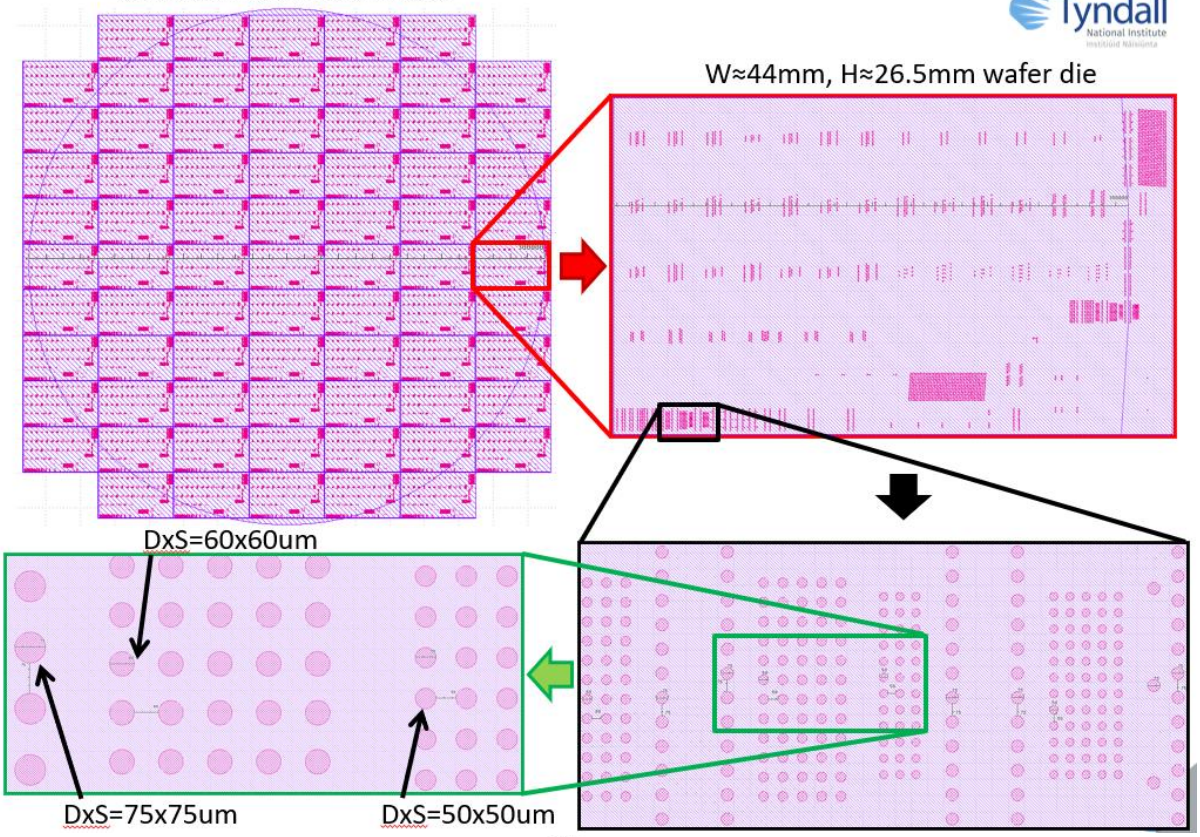
Appendix VII: imec ASCENT work package

I submitted a successful proposal on behalf of the Integrated Magnetics (IM) group for acquisition of Cu pillar wafers from the imec ASCENT project. The aim was to provide the IM group with test wafers for vertically oriented magnetic material sputtering experiments. The proposal specification is first provided, which is followed by the delivered specification, then a schematic of the photomask, then metrology and characterization. Finally, the success story from the imec ASCENT website is provided.

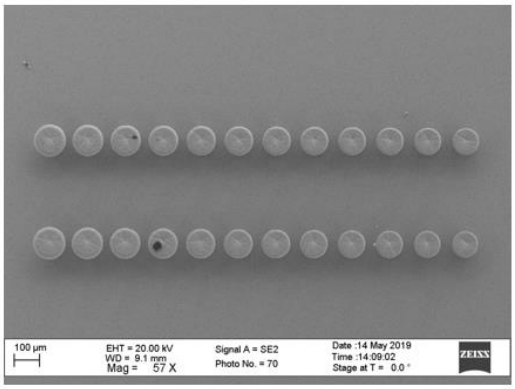


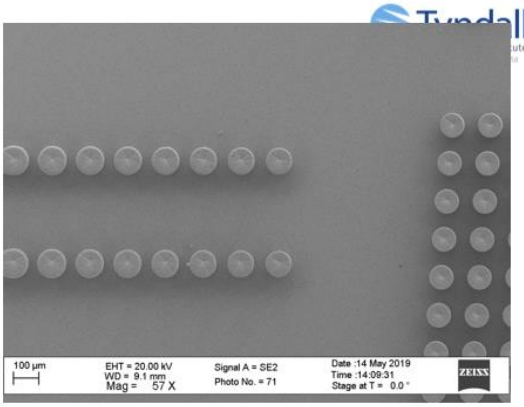
Imec Photomask – Cu Pillar Height = 110-140um

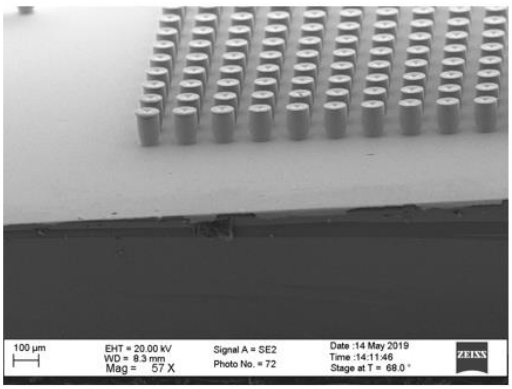
D=300mm wafer schematic

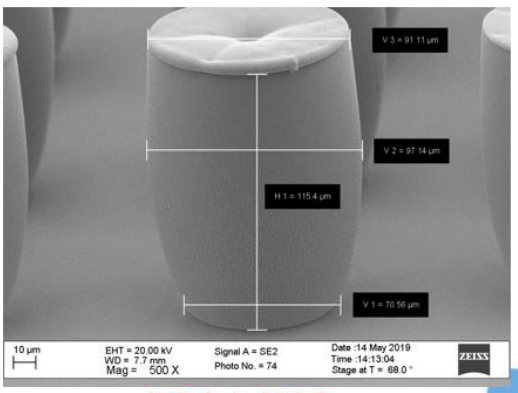


Imec Cu Pillar SEM Images



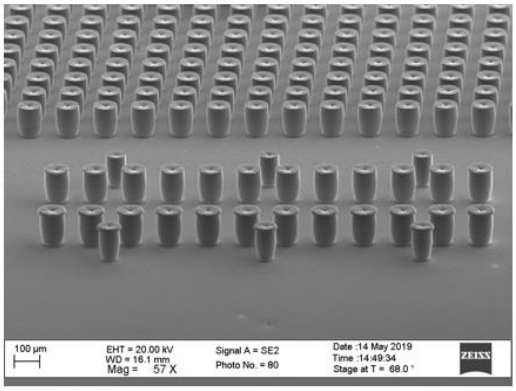


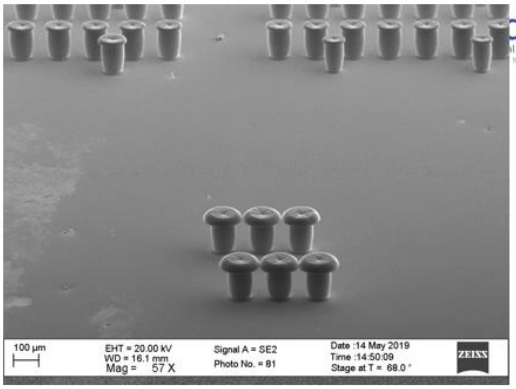


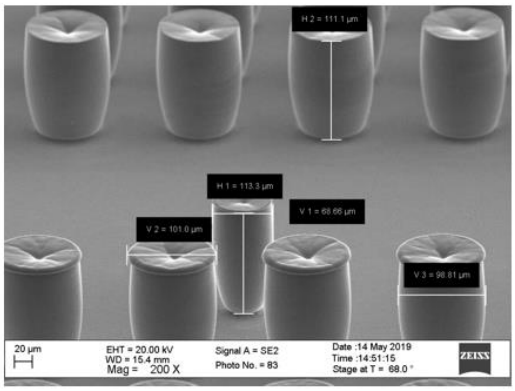


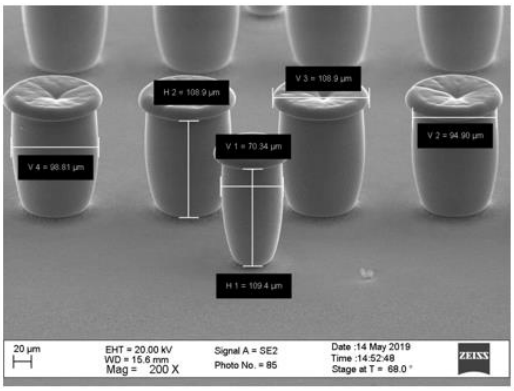
115.4 => 124.5um

Imec Cu Pillar SEM Images



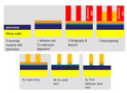
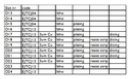
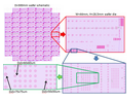
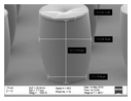
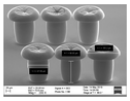
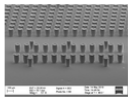






Ascent Project Ref No

145

User

Daniel Smallwood

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Description

The main goal of the project was to develop an optimized process for utilising Cu pillars in lieu of through substrate vias (TSVs), or to enable the additive deposition of TSV technology. This method removes the need for deep reactive ion etching (DRIE) of the substrate, where the side walls of DRIE etched TSVs are scalloped and the via cross sections have gradated diameters along their axial length. Electrochemically depositing Cu into TSVs is difficult, as current crowding at the via entrance causes heterogeneous deposition rates, often resulting in a dual pyramidal shape of the deposited material. Conversely, electrochemically depositing Cu into feature holes created by lithographic processing is free from all of the aforementioned problems. Lithographic processing is ideal, as the process can be tuned to create a vertical and non-gradated resist profile along the axial length of the feature holes and additionally, current crowding is a non-issue because the deposition is uniaxial in the z-direction.

The first results comprise SEM micrographs of the diced wafers, which have been investigated for pillar side wall and height profiles, as well surface roughness. The pillar side walls were found to be retrograde, with significant variability in the cross-sectional diameter from substrate contact to pillar apex (ex. 70-97µm). In the case of the Cu pillars being used as interconnects, the electrical resistance ($R \propto A^{-1}$) will be increased according to the magnitude of the cross-sectional variance.

The pillar height is variable across the wafer, which is due to a changing current density across the die, as corresponds to a variable local feature density. Images were taken with $\theta = 68°$, which corresponds to an actual pillar height of 124µm. The apex of the pillars is over-plated, indicating the photoresist was spun to ≈124µm.

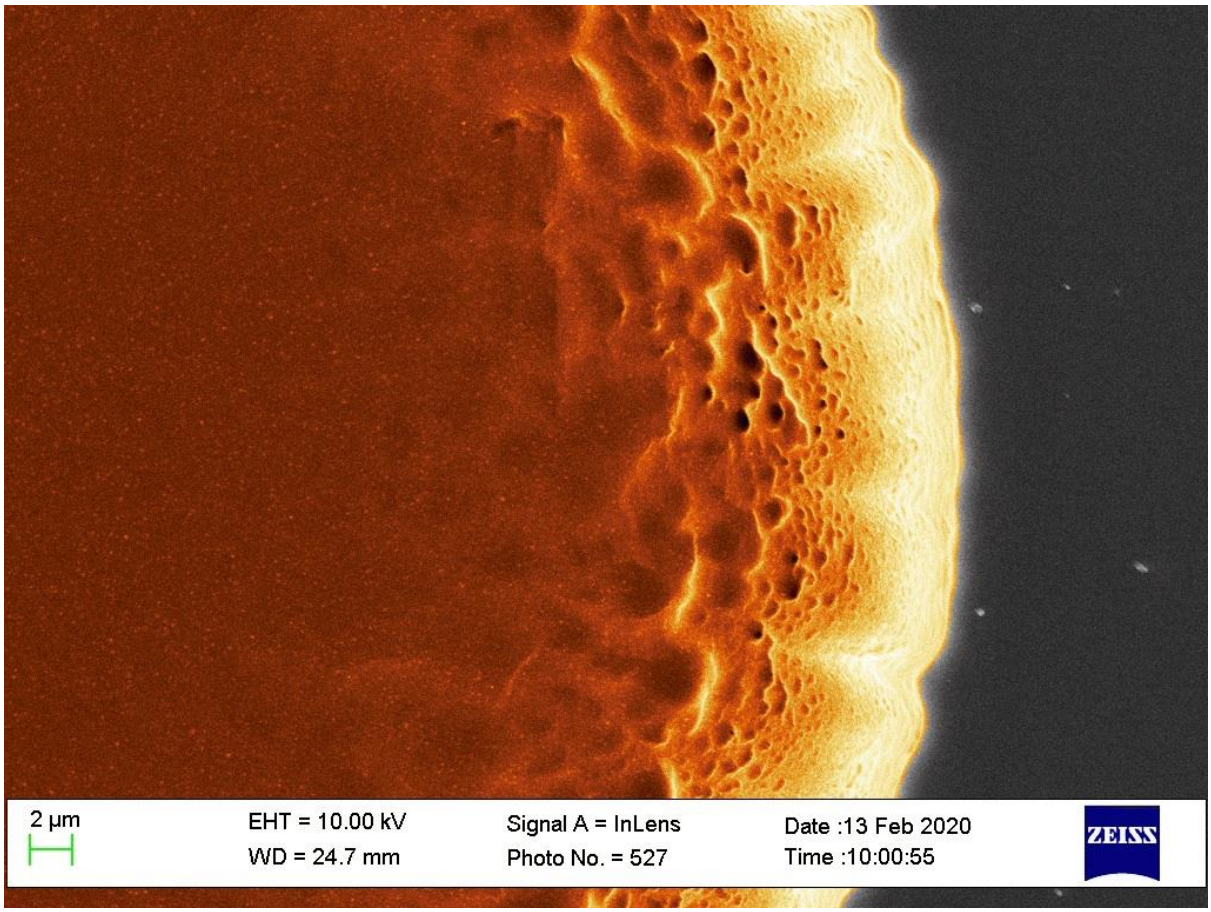
Future plans involve utilizing CMP to remove the over-plated material and/or the retrograde side-walls to improve pillar performance by eliminating undesired short circuits and reducing pillar size for increased integrability, whilst maintaining a constant resistance along the axial length.

Pillar circumferential roughness is low (single-digit µm to nanoscale regime), contrary to the conventionally very rough scalloped profile formed as a result of utilising DRIE for via fabrication.

The above description from: https://www.ascent.network/community/success-stories/

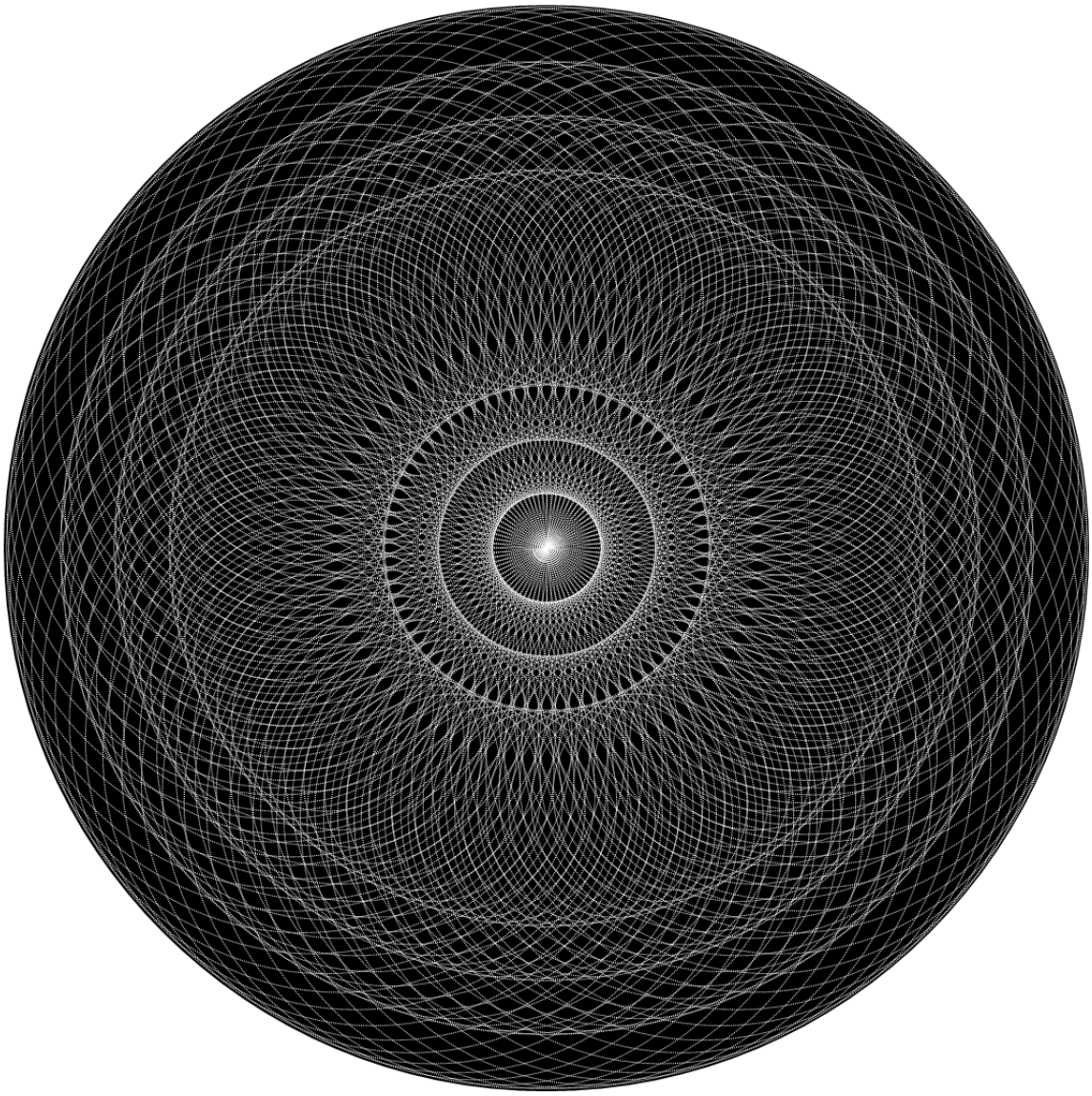
Appendix VIII: Scientific image competitions

Vulcan – Tyndall scientific image competition winner. December 2020.



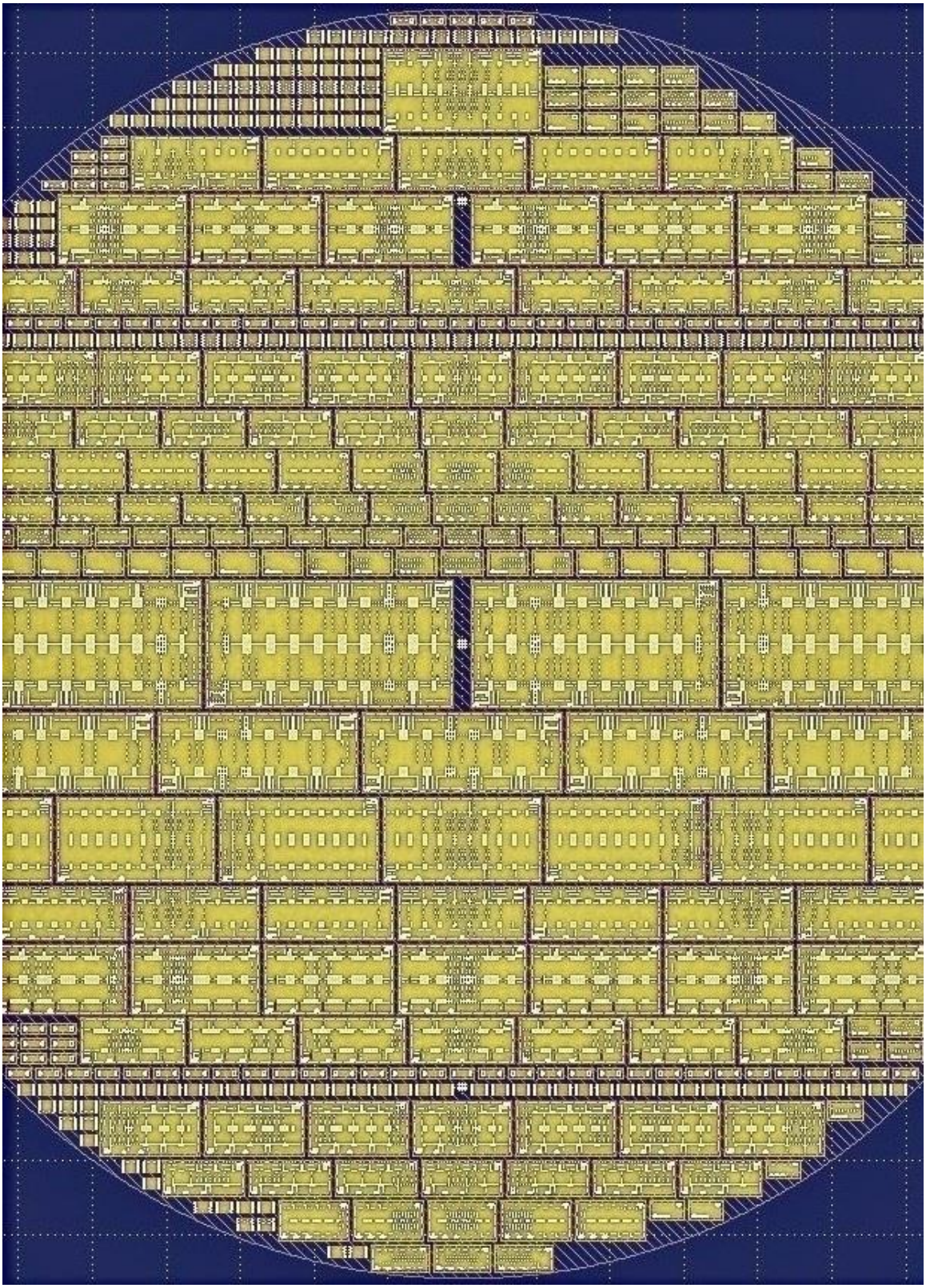
Through the lens of the SEM, we glimpse the rippled surface of an etched photoresist Cu pillar micromold. When coloured in vibrant orange and yellow, the micromold appears to warp across time and space and morph into the fiery planet Kepler-10b. Once suggested to be unofficially named "Vulcan" after the hypothetical planet, this exoplanet is located a staggering 560 light-years from Earth. These micromolds enable vertical interconnect access points (VIAs) for next generation MEMS devices with 2.5D and 3D System on Chip (SoC) and System in Package (SiP) applications. This technology is expected to hold great promise in spearheading the future of the microelectronics industry. Spock himself would be proud! This work is part of the SFI ADEPT project No. 15/IA/3180 "Advanced Integrated Power Magnetics Technology - From Atoms to Systems".

Oculus – Tyndall Scientific image competition winner. August 2020.



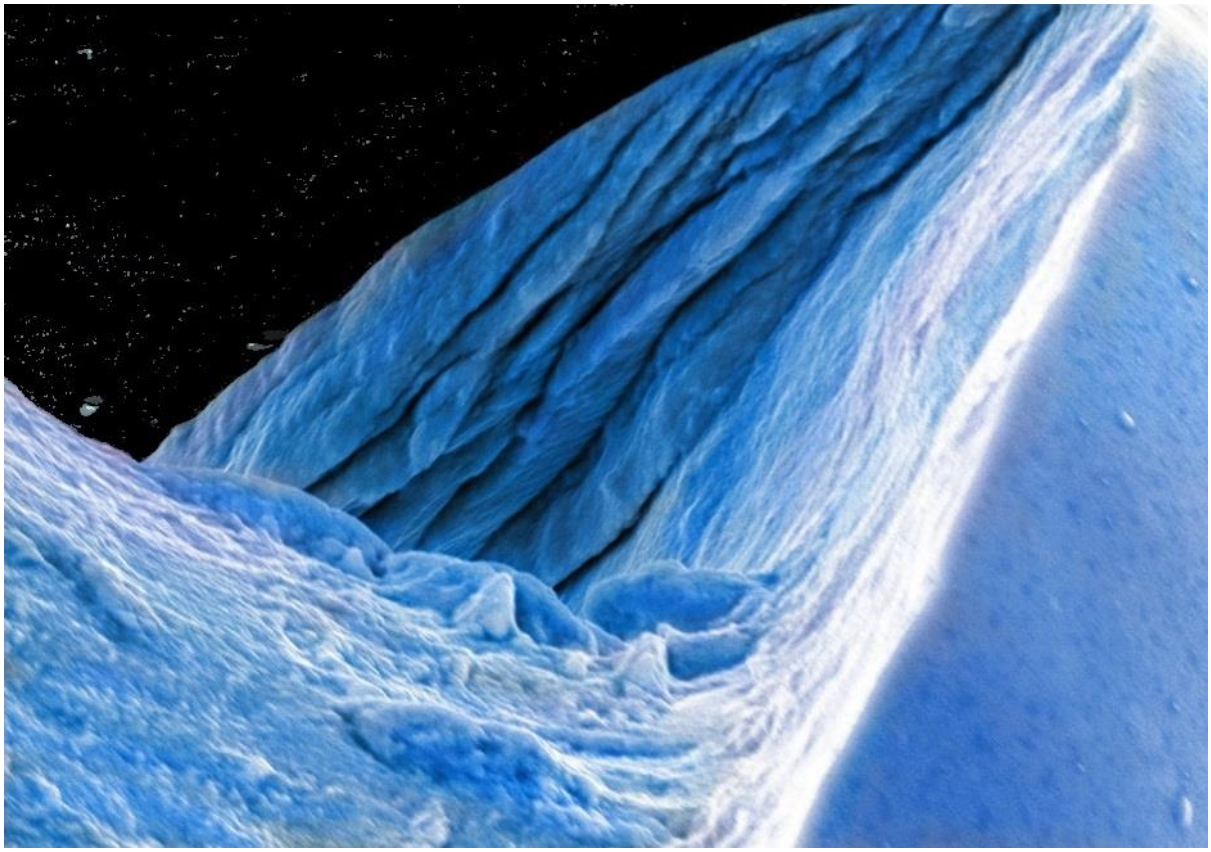
This mesmerizing image captures the diffraction pattern from a circular photomask occulter, with UV light rays propagating according to the Huygens-Fresnel principle. This exemplifies monochromatic light, wherein the time domain is neglected and additionally, the z-dimension has been projected into x-y space. This phenomenon is observed in photolithography, which is essential for high aspect ratio photoresist relief image fabrication. This work is part of the SFI Adept project.

Micro Circuit Metropolis – Tyndall Scientific image competition winner. September 2019.



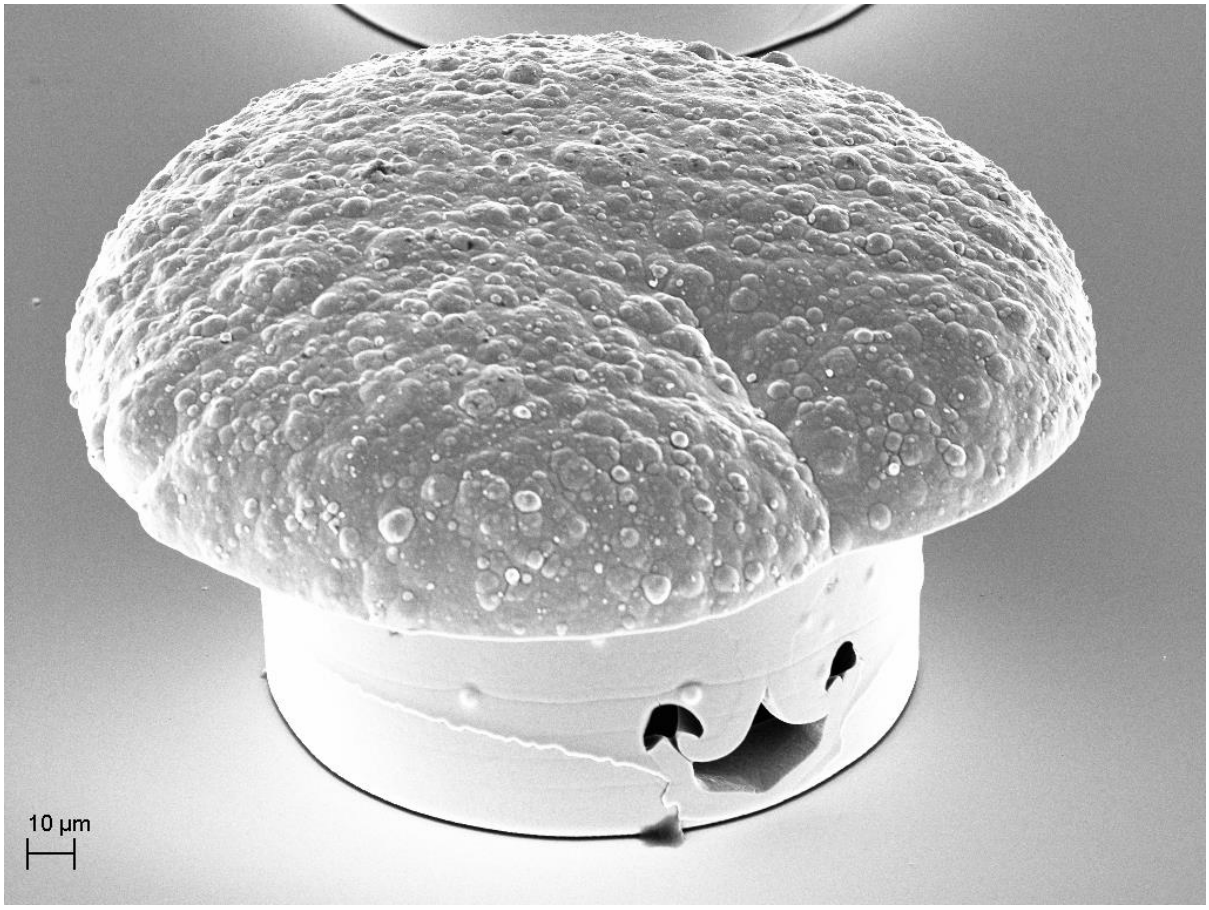
This is an image of a multi-tiered photomask design, where multiple devices are simultaneously fabricated on the same wafer. Vertical stacking and horizontal dicing lanes, when coupled with the complexity of the design, create the effect of a sprawling micro-metropolis. This research is part of the SFI Adept project.

Icy Comet Nucleus – Tyndall Scientific image competition winner. May 2019.



SEM micrograph of an electroplated micro-wire. The wire's surface roughness creates the impression of a jagged icy slope with an undulating frozen backdrop. The frozen landscape is contrasted against a dark substrate in the background, which appears as the star-lit void of deep space. This research is part of the SFI Adept project.

Mushroom Man – Tyndall Scientific image competition winner. 2018



This is an SEM micrograph of an over-plated copper pillar on a silicon substrate. Variable plating rates created a void at the copper-silicon interface, which was partially filled in by neighboring nucleation sites of electroplated copper. The void then forced the copper to quickly plate up past the target thickness, which enabled the copper to balloon outward in every direction. The dynamic result was the magical smiling face of a micro-sized mushroom! This research is part of the SFI Adept project.

Appendix IX: SOPs for photomasks 1-5

Photomask 1

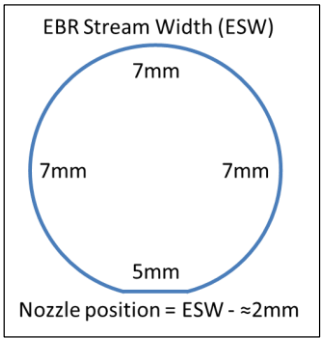
The SOP for the bottom interconnect (BIC) mask is shown below.

SOP - BIC (Process Steps 2-3)

- **(1) Turn on DM/computer, mask aligner, fume hood, take THB-151N out of fridge & cool at RT for 1 hr**
- **(2) Wafer clean**
  1. S20 puddle/30s
  2. Heat wafer to 110°C/5min & let cool (Power cycle hot plate at 110°C to prevent temp overshoot)
  3. Ramp hot plate to 120°C for soft bake
- **(3) Spin coat (target = 31um)**
  1. Program #7:
     - 300rpm/25s, 0rpm/30s, 300rpm/10s, 1650pm/30s, 300rpm/30s (EBR), 1000rpm/2s
  2. Heat at 120°C/5min & let cool fully before inserting into mask aligner
- **(4) Exposure**
  1. Follow repeat exposure SOP
     a. Ensure proximity mode, 49um
     b. ED = 538mJ/cm2, T = 102s, 2X51s exposures
  2. Push reload button
  3. Store light integral at 79.2
- **(5) Spin develop**
  1. Program #8 – procedure on 2nd page
  2. Get reference height w/ profilometer
- **(6) Wafer clean and activation**
  1. S20 puddle/2min & tweezer agitation, 3x rotations
  2. Turn on asher:
     a. Power sockets, AC power buttons , vacuum button, O_2 flow valve
        - Wait for vacuum
        - Press gas 1 and set regulator to 3
        - Wait for stabilization and ensure full power
     b. Press RF key, ash 1min
  3. Turn off:
     a. RF, gas 1, O_2 valve, vacuum
     b. Wait for door to open
     c. AC buttons & power sockets
- **(7) Cu plating**
  1. Select program: *Dan 60um*
     - 1RPM, 0.3ADC, 3min ramp, Hold 51 min
  2. Get reference height w/ profilometer

Repeat Exposure SOP

- Put wafer in loading cassette
- Set light integral dial to 73, press reset, then press start
- When the wafer is on the chuck, set light integral dial to the desired number
- Press align, then expose
- Keep pressing expose for repetitions
- Press reload to send wafer to collector cassette



In this section, the SOP for photomask 1 is described. For successive photomasks, significant modifications to the original procedure are solely discussed, wherein this discussion and the corresponding SOPs for photomasks 2-5 are provided in the proceeding sections.

This SOP is highly optimized for fast wafer processing. SOP step 1 is a preparatory step, where DM stands for Digital Matrix (the electroplating tool) and RT is room temperature. This step permits time for the DM to circulate the copper sulfate electrolyte while the mask aligner Hg bulb heats up and the viscosity of the THB-151N reduces to a sensible value. In step 2, a thin oxide film is removed from the Cu seed with an industrial Cu cleaner, S20, and any surface-adsorbed moisture is evaporated. The photoresist is manually dispensed in step 3 and all air bubbles are removed by suction with a disposable pipette. The bottom schematic depicts the essential EBR information. It is critical to let the photoresist cool to room temperature after the soft bake to ensure the wafer does not stick in the mask aligner. Step 4 requires a repeat exposure procedure due to the high exposure doses required by THB-151N and the maximum single exposure time limit of 59.9 s on our CANON PLA600F Mask Aligner. Proximity mode is used to stop the photoresist from sticking to the photomask

during exposure. The exposure dose energy in all SOPs is set at a conservatively high value to ensure full cross-linking at the lower film surface. A custom spin development procedure is utilized in step 5, which was detailed in Chapter 3. The wafer is again cleaned in S20 in step 6. The duration of this step is a function of the mold aspect ratio, whereby high aspect ratio molds resist solvent flow and hinder the reaction rate. The following plasma etching step cleans the substrate and makes the Cu seed hydrophilic for electroplating. Throughout this SOP, ongoing metrology is performed with a profilometer and a light microscope to ensure processing quality.

Photomask 2

In addition to the conduction path Cu pillars, this mask selectively creates a multitude of dummy Cu pillars to upwardly adjust the electroplating density of the larger devices, hence the SOP name "Pillar-Adj."

SOP - Pillar-Adj (Process Steps 4-6)

- **(1) Turn on DM/computer, mask aligner, fume hood, take THB-151N out of fridge & cool at RT for 1 hr**
- **(2) Wafer clean**
  1. S20 puddle/30s
  2. Heat wafer to 110°C/5min & let cool (Power cycle hot plate at 110°C to prevent temp overshoot)
  3. Ramp hot plate to 130°C for soft bakes
- **(3) Spin coat (target = 115um)**
  1. Program #4:
     - 300rpm/25s, 0rpm/30s, 300rpm/10s, 1100rpm/30s, 300rpm/30s (EBR), 1000rpm/2s
  2. Heat at 130°C/5min & let cool
  3. Program #6:
     - 300rpm/10s, 0rpm/30s, 800rpm/110s, 300rpm/30s (EBR), 1000rpm/2s
  4. Heat at 130°C/5min & let cool fully before inserting into mask aligner
- **(4) Exposure**
  1. Follow repeat exposure SOP
     a. Ensure proximity mode, 49um
     b. Mask alignment
     c. ED = 1750mJ/cm2, T = 330s, 6X55s exposures
  2. Push reload button
  3. Store light integral at 79.2
- **(5) Spin develop**
  1. Program #5 – procedure on 2nd page
  2. Get reference height w/ profilometer
- **(6) Wafer clean and activation**
  1. S20 puddle/4min & tweezer agitation, 3x rotations
  2. Turn on asher:
     a. Power sockets, AC power buttons , vacuum button, O_2 flow valve
        - Wait for vacuum
        - Press gas 1 and set regulator to 3
        - Wait for stabilization and ensure full power
     b. Press RF key, ash 1.5min
  3. Turn off:
     a. RF, gas 1, O_2 valve, vacuum
     b. Wait for door to open
     c. AC buttons & power sockets
- **(7) Cu plating**
  1. Select program: *Dan 60um*
     - 0.1ADC, 1RPM, 180min ramp - TBD
  2. Get reference height w/ profilometer
- **(8) Resist strip**
  1. THB-S17 in orbital rotator for 60 min
     - Use crystallizing dish

In this and the following SOPs, I have removed the EBR and repeat exposure schematics, which were nonetheless used during processing. A notable change in this SOP is step 3, where the

target spin thickness has drastically increased to 115 µm. This requires a double spin that accounts for Van der Waals forces at the photoresist-to-photoresist interface that significantly increase the viscosity of the THB-151N, as described in Chapter 3. It is critical to use a slow current ramp speed in step 7 to avoid uneven pillar topography as a result of anisotropic Cu^{2+} rich electrolyte diffusion streamlines along the tubular mold cross-section. An automatic advection tool, the orbital rotator, is used to strip the photoresist. Due to the high selectivity of THB-S17 for THB-151N over Cu, the stripping time is set at a conservative value to ensure all resist is fully removed.

Blanket spin

In this step, THB-151N is cured as a full wafer blanket to act as a supporting structure during CMP.

SOP – Litho Blanket (Process Step 9)

- **(1) Turn on mask aligner, fume hood, take THB-151N out of fridge & cool at RT for 1 hr**
- **(2) Spin coat (target = 115um)**
    1. Ramp hot plate to 130°C for soft bakes
    2. Program #4:
        - 300rpm/25s, 0rpm/30s, 300rpm/10s, 1100rpm/30s, 300rpm/30s (EBR), 1000rpm/2s
    3. Heat at 130°C/5min & let cool
    4. Program #6:
        - 300rpm/10s, 0rpm/30s, 800rpm/110s, 300rpm/30s (EBR), 1000rpm/2s
    5. Heat at 130°C/5min & let cool fully before inserting into mask aligner
- **(3) Exposure**
    1. Follow repeat exposure SOP
    a. Ensure proximity mode, 49um
    b. ED = 1750mJ/cm2, T = 330s, 6X55s exposures
    2. Push reload button
    3. Store light integral at 79.2

Photomask 3

This is the Cu pillar selective activation step, whereby dummy pillars are buried in cured THB-151N photoresist.

SOP - Pillar (Process Step 11)

- **(1) Turn on mask aligner, fume hood, take THB-151N out of fridge & cool at RT for 1 hr**
- **(2) Spin coat (target = 10um)**
    1. Ramp hot plate to 120°C for soft bake
    2. Program #: TBD
        - 300rpm/25s, 0rpm/30s, 300rpm/10s, 5000pm/30s, 300rpm/30s (EBR), 1000rpm/2s
    3. Heat at 120°C/5min & let cool fully before inserting into mask aligner
- **(3) Exposure**
    1. Ensure proximity mode, 49um
    a. Mask alignment
    b. ED = 271mJ/cm2, T = 51s
    2. Push reload button
    3. Store light integral at 79.2
- **(4) Spin develop**
    1. Program #: TBD – procedure on 2nd page
    2. Get reference height w/ profilometer

Photomask 4

The top interconnect (TIC) is now electroplated. A slow current ramp speed is used to ensure isotropic plating along the topographically complex electroactive wafer surface.

SOP - TIC (Process Steps 12-14)

- **(1) Turn on DM/computer, mask aligner, fume hood, take THB-151N out of fridge & cool at RT for 1 hr**
- **(2) Wafer clean**
    1. S20 puddle/30s
    2. Heat wafer to 110°C/5min & let cool (Power cycle hot plate at 110°C to prevent temp overshoot)
    3. Ramp hot plate to 130°C for soft bake
- **(3) Spin coat (target = 40um)**
    1. Program #6:
        - 300rpm/10s, 0rpm/30s, 800rpm/110s, 300rpm/30s (EBR), 1000rpm/2s
    2. Heat at 130°C/5min & let cool fully before inserting into mask aligner
- **(4) Exposure**
    1. Follow repeat exposure SOP
        a. Ensure proximity mode, 49um
        b. Mask alignment
        c. ED = 595mJ/cm2, T = 112s, 2X56s exposures
    2. Push reload button
    3. Store light integral at 79.2
- **(5) Spin develop**
    1. Program #: TBD– procedure on 2nd page
    2. Get reference height w/ profilometer
- **(6) Sputter Ti =50nm and Cu = 400nm**
- **(7) Wafer clean and activation**
    1. S20 puddle/4min & tweezer agitation, 3x rotations
    2. Turn on asher:
        a. Power sockets, AC power buttons , vacuum button, O_2 flow valve
            - Wait for vacuum
            - Press gas 1 and set regulator to 3
            - Wait for stabilization and ensure full power
        b. Press RF key, ash 1.5min
    3. Turn off:
        a. RF, gas 1, O_2 valve, vacuum
        b. Wait for door to open
        c. AC buttons & power sockets
- **(8) Cu plating**
    1. Select program: *Dan 60um*
        - 0.75ADC, 1RPM, 60min ramp - TBD
    2. Get reference height w/ profilometer

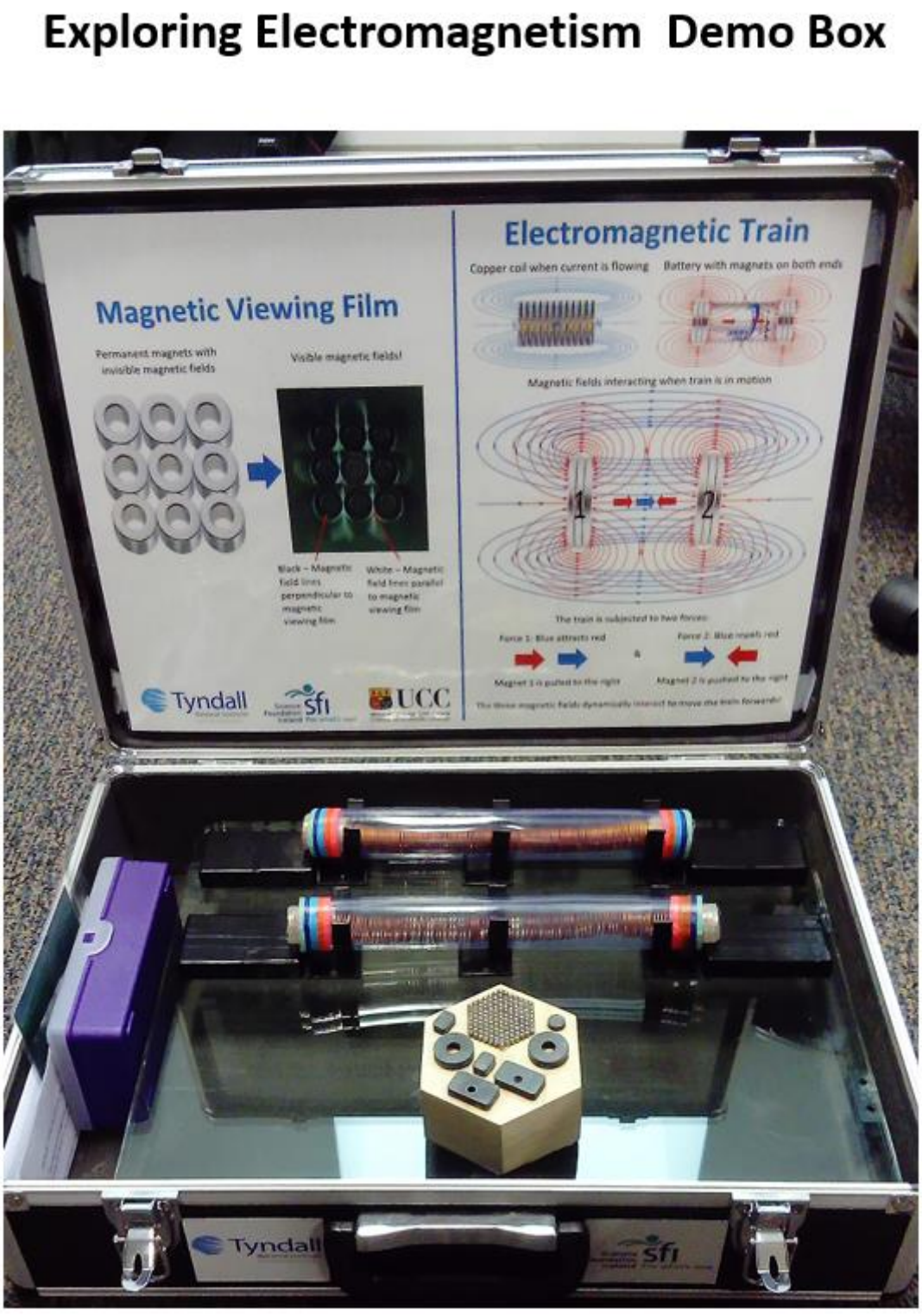
Photomask 5

SOP - Passivation (Process Step 16)

- **(1) Turn on mask aligner, fume hood, take THB-151N out of fridge & cool at RT for 1 hr**
- **(2) Spin coat (target = 10um)**
    1. Ramp hot plate to 120°C for soft bake
    2. Program #: TBD
        - 300rpm/25s, 0rpm/30s, 300rpm/10s, 5000pm/30s, 300rpm/30s (EBR), 1000rpm/2s
    3. Heat at 120°C/5min & let cool fully before inserting into mask aligner
- **(3) Exposure**
    1. Ensure proximity mode, 49um
        a. Mask alignment
        b. ED = 271mJ/cm2, T = 51s
    2. Push reload button
    3. Store light integral at 79.2
- **(4) Spin develop**
    1. Program #: TBD – procedure on 2nd page
    2. Get reference height w/ profilometer

Appendix X: Electromagnet outreach project

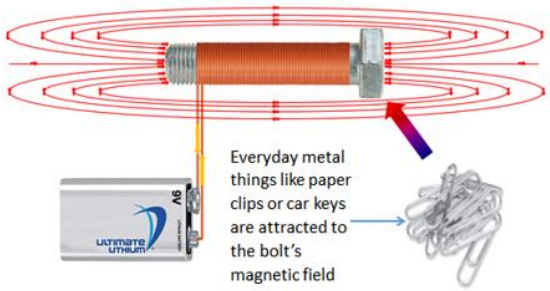
The electromagnet demo box that I created for outreach is featured below. Various design iterations included an electromagnetic bolt and coil, magnetic viewing film and an electromagnetic train. Group photo credit: Guannan Wei.



Outreach – EM Box Laminate Schematics

Electromagnetic Bolt & Coil

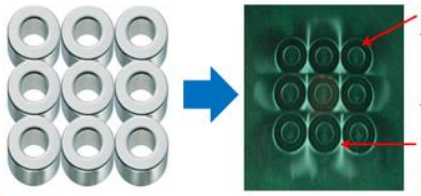
Magnetic field around iron bolt when current is flowing in the copper wire



Magnetic Viewing Film

Permanent magnets with invisible magnetic fields

Visible magnetic fields!

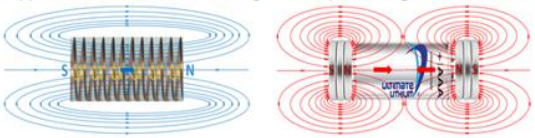


Tyndall National Institute

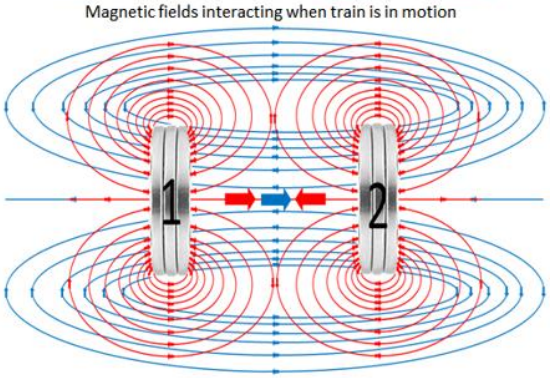
Electromagnetic Train

Copper coil when current is flowing

Battery with magnets on both ends



Magnetic fields interacting when train is in motion



The train is subjected to two forces:

Force 1: Blue attracts red

Magnet 1 is pulled to the right

&

Force 2: Blue repels red

Magnet 2 is pushed to the right

The three magnetic fields dynamically interact to move the train forwards!