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HIGH SPEED IC DESIGNS FOR LOW POWER SHORT REACH OPTICAL LINKS

SHIYU ZHOU

A THESIS SUBMITTED TO

THE NATIONAL UNIVERSITY OF IRELAND, CORK

FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

PHOTONICS SYSTEMS GROUP,

TYNDALL NATIONAL INSTITUTE AND DEPARTMENT OF

ELECTRICAL AND ELECTRONIC ENGINEERING,

NATIONAL UNIVERSITY OF IRELAND



MAY 2017

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RESEARCH SUPPORTED BY TYNDALL NATIONAL INSTITUTE

High Speed IC Designs for Low Power Short Reach Optical Links

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MSc

Thesis submitted for the degree of
Doctor of Philosophy

NATIONAL UNIVERSITY OF IRELAND, CORK

SCHOOL OF ENGINEERING

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List of Publications

- Journal Papers
  - **Shiyu Zhou**, Hsin-Ta Wu, Khosrov Sadeghipour, Carmelo Scarcella, Cormac Eason, Marc Rensing, Mark J. Power, Cleitus Antony, Peter O'Brien, Paul D. Townsend and Peter Ossieur, "Optimization of PAM-4 transmitters based on Lumped Silicon Photonic MZMs for High-Speed Short-reach Optical Links", Optics Express, vol. 25, issue: 4, pp. 4312-4325, Feb 2017
  - **S. Zhou**, H. Wu, K. Sadeghipour, C. Scarcella, C. Eason, M. Rensing, M. Power, C. Antony, P. O'Brien, P. Townsend and P. Ossieur, "Driver Circuit for a PAM4 Optical Transmitter using 65nm CMOS and Silicon Photonic Technologies", Electronics Letters, vol.55, issue: 23, pp.1939 - 1940, Nov 2016
  - Nicola Pavarelli, Jun Su Lee, Marc Rensing, Carmelo Scarcella, **Shiyu Zhou**, Peter Ossieur, Peter A. O'Brien, "Optical and Electronic Packaging Processes for Silicon Photonic Systems", Journal of Lightwave Technology (invited paper), vol. 33, issue: 5, pp. 991-997, Feb 2015

I, Shiyu Zhou, certify that this thesis is my own work and has not been submitted for another degree at University College Cork or elsewhere.



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Abstract

In the last decade, we have witnessed the emergence of large, warehouse-scale data centres which have enabled new internet-based software applications such as cloud computing, Video on Demand (VoD), social media, online gaming etc. Such data centres consist of large collections of servers interconnected using short-reach (fibre reach up to a few hundred meters) optical interconnect. Today, this interconnect between servers is under severe pressure, and data centre operators such as Google and Facebook have expressed a need for links with capacities of at least 400Gb/s, compared to today's state-of-the-art 100Gb/s links. One example is the emerging 400Gb/s Ethernet standard.

New technology focused on achieving low-power and high integration density are required to achieve such capacities. One promising approach is to use Silicon Photonics to densely integrate the electro-optic functions, combined with 3D transceiver electronics. High-capacity links use space or wavelength division multiplexing of many sub-channels. While increasing the capacity of a link can be done by simply multiplexing more links this is challenging from a power and integration point-of-view. The alternative is then to use more advanced modulation formats beyond simple non-return to zero modulation used widely in short-reach applications today. A first attractive candidate is 4-level pulse amplitude modulation (PAM-4).

Against this background, a new CMOS electronic driver integrated circuit has been proposed, realized and successfully tested in this thesis. The CMOS driver chip was designed specifically for driving lumped Silicon Photonic modulators to realize a PAM-4 signal. To increase the bandwidth of the resulting PAM-4 transmitter, a switched capacitor based circuit approach is proposed for the first time for high-speed optical links. This scheme enables driving the lumped Mach-Zehnder modulator (MZM) at high speed with less power consumption compared to the conventional approach of driving high speed MZMs (with transmission line based electrodes) with an RF power amplifier. Optimization of the DC-bias of the modulator has been explored with a view to maximizing the achievable optical budget, trading off extinction ratio against insertion loss of the modulator.

The driver chip has been designed and fabricated using a 65nm CMOS technology, the Silicon Photonic chip was designed and fabricated using a Silicon Photonic Multiproject Wafer (ISIPP25G process technology) run from IMEC. A

new method to design and realize the broadband (DC to 20GHz) high-speed electrical IO was proposed and experimentally verified. The PAM-4 transmitter consisting of the Silicon Photonic chip onto which the CMOS driver was flip-chipped was assembled into a test module together with surrounding RF ceramic substrate and PCB to transfer the high-speed signals. Eye diagram and bit-error rate (BER) measurements showed that the PAM-4 transmitter can generate a PAM-4 signal with a bitrate up to 36Gb/s (18Gbaud). The electronic driver chip has a core area of $0.11mm^2$ and consumes 236mW from 1.2V and 2.4V supply voltages. This corresponds to an energy efficiency of 6.55pJ/bit including Gray encoder and retiming, or 5.37pJ/bit for the driver circuit only. This compares well against the state-of-the-art designs.

Chapter 1

Introduction

1.1 Background

In the last five years, we have witnessed the rapid emergence of new Web and internet based applications such as internet of things, social networking, search engines, cloud-computing, on-demand video services. These applications are nowadays supported by large-scale datacentres, also called warehouse scale computers. As shown conceptually in Fig. 1.1, such datacentres consist of racks of servers, connected together using a hierarchical network. In this network, the servers in a single rack typically connect to switches, which for example are located at the top of each rack (and hence are known as top of rack switches). The rapidly growing demand of the above mentioned applications means that data-centres need to handle ever-increasing amounts of data, which is putting significant strain on the network and its constituent links [1].

The links in datacentre networks nowadays typically consist of optical fibres (multimode, but sometimes single mode, and commonly referred to as "short-reach interconnect"), with transceivers at either end. The transceivers convert back and forward between the electrical and optical domain. These links may take the form of so-called active optical cables, or could take the form of "pluggable" transceivers using for example SFP/SFP+ (Small Form-factor Pluggable) from QuagWire (http://www.quagwire.com/), see Fig. 1.2 .

Today, the large majority of the fibre-optic transceivers deployed in datacentres use 850nm VCSELs (Vertical Cavity Surface Emitting Laser), OM-3/OM-4 (Optical Mode) multimode fibres (reach up to 100m) and GaAs photodetectors.

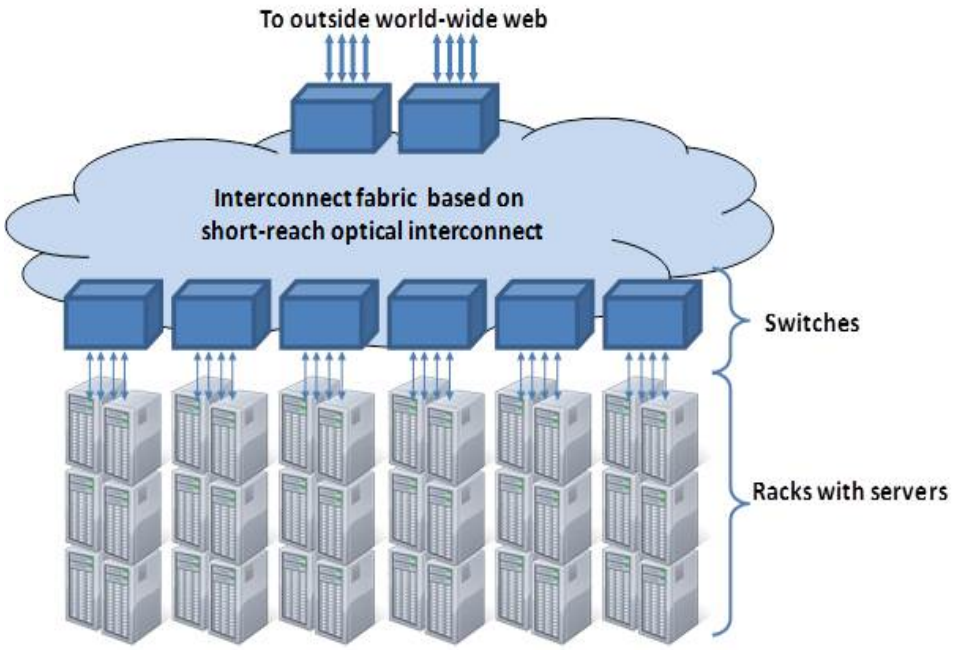


Figure 1.1: Conceptual view of a datacentre

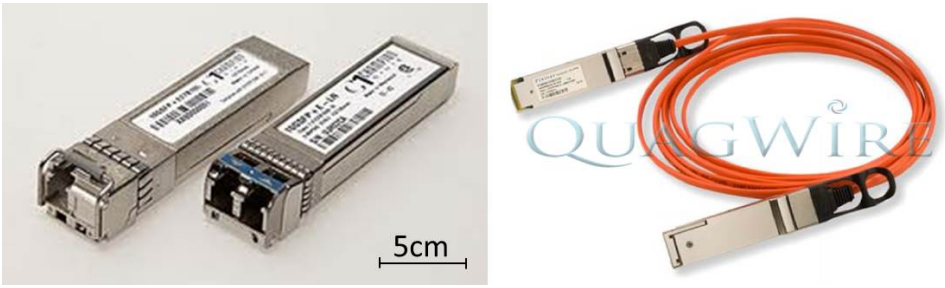


Figure 1.2: SFP+ transceiver module (left) and active optical cable (right)

State-of-the-art transceivers feature bitrates ranging from 10Gb/s to 40Gb/s and up to 100Gb/s. Interestingly, the 40Gb/s and 100Gb/s transceivers invariably make extensive use of space-division or (coarse) wavelength division multiplexing of lower-rate channels. For example, Table 1.1 gives an overview of a number of relevant IEEE Ethernet 802.3ah standards: 10x10Gb/s and 4x25Gb/s transceivers are now commercially available.

The modulation format is always simple non return-to-zero (NRZ) modulation, in which a pulse of light signifies a digital '1' and the absence of a pulse a digital '0'. Typical fibre lengths for the multimode fibre (MMF) based transceivers are maximum 100meters. Power consumption of a state-of-the-art 100Gb/s transceiver module is about 3W. An important figure-of-merit here is the so-called energy-efficiency, which is the required energy to transmit a single bit. Typical numbers nowadays are 30picoJoule/bit. This conventional VCSEL and

Table 1.1: Short overview of 40Gb/s and 100Gb/s IEEE802.3 standards

Standard Designation	Bitrates and channels	Physical layer technology
40GBASE-SR4	4x 10Gb/s	100m over OM3 MMF 125m over OM4 MMF 850nm VCSEL
100GBASE-SR10	10x 10Gb/s	100m over OM3 MMF 125m over OM4 MMF 850nm VCSEL
40GBASE-LR4	4x 10Gb/s	10km over SMF 4 wavelengths around 1310nm
100GBASE-LR4	4x 25Gb/s	10km over SMF 4 wavelengths around 1310nm
100GBASE-ER4	4x 25Gb/s	40km over SMF 4 wavelengths around 1310nm

multimode fibre based technology has a number of serious limitations:

- It is very challenging to operate the VCSEL at bit-rates beyond 25Gb/s. While some research groups and SMEs have demonstrated such VCSELSs [2] [3], a major issue is reliability. Indeed to maintain the same light output, but increase the speed, the VCSEL device must decrease in size (device diameter) to reduce the parasitic capacitance. To keep the same light output, the current cannot scale accordingly, which means that the current density increases with increasing bit-rate. This has a detrimental effect on reliability [4].
- Energy-efficiency: it is estimated that for future sustainable datacentres, energy efficiency must improve to less than 1pJoue/bit [5]. This is true for datacentres (already the largest consumers of electricity with resulting large carbon footprint), but even more so for high-performance supercomputers [6].
- Physical reach: new generations of datacentres will require opical links that can achieve up to 2km length [1]. This is extremely difficulty for multimode fibre due to dispersion limitations.
- Need for high reliability and cost reductions: future datacentres may require high volumes (hundreds of thousands) of optical links, high performance supercomputers will soon require millions of such links [7]. In this

case, cost/module is an important parameter as well as reliability. Both can be improved by further integration.

These limitations are a serious issue for datacentre operators, who anticipate a need for Terabit/s class optical links (400Gb/s system and beyond) in the next five years [8]. It is a huge challenge for the currently deployed technology to meet such requirements.

One alternative that is now receiving significant interest for short-reach optical links is Silicon Photonics. In this technology, optical functions such as modulation, detection, wavelength filtering, multiplexing and demultiplexing are integrated into a Si SOI (Semiconductor on Insulator) chip. Several research groups around the world have worked on this (notably Ghent University/IMEC, University California Santa Barbara, IME ASTAR in Singapore, and large multinationals such as Intel, IBM, and famously also CISCO [6]). As shown in Fig. 1.3, a transceiver could then consist of a Si Photonic SOI die containing the photonic functions, onto which an electrical IC with the drive, receive and control electronics is flip-chipped. Note how the light source is not integrated in the Si Photonic die: indeed as Silicon is an indirect bandgap material, it is very difficult to generate light directly from Silicon. Therefore, it is currently widely anticipated that the light source will be fabricated into a suitable III-V material, and then integrated (in whatever manner) with the Si Photonic die and electronics into a single transceiver module.

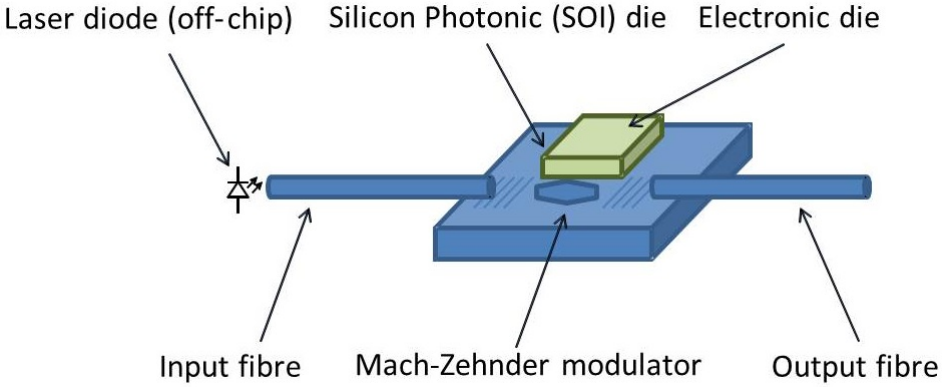


Figure 1.3: Conceptual view of a Si Photonics transceiver

To integrate the required electronics, two routes are pursued worldwide:

- In some cases the electronics are monolithically integrated onto the same die as the photonic functions [9]. Although this promises the ultimate performance in terms of power savings, integration and cost reduction, there

are many conflicting requirements between optimized photonics performance and electronic performance for deep submicron (<65nm) technology.

- In other cases, one can for example flip-chip the electronic chip onto the Si Photonics SOI chip (which is usually quite large compared to the electronic chip if the latter contains only driver and receiver circuits). This is known as hybrid integration.

Significant transceiver energy savings are now possible due to a number of reasons:

- Si (Mach-Zehnder) modulators require less drive voltage compared to conventional $LiNbO_3$ or InP modulators. Note how power consumption scales with the square of the drive voltage. A typical Si modulator may require a few Volts swing (typically less than 2V), while$LiNbO_3$ modulators may require close to 4V swing [10].
- Si modulators under the form of microring resonators are very small and have very small capacitance (in the order of 10s of femtofarads). This means very low power consumption is required to drive such components, energy efficiencies significantly less than 1picoJoule/bit have been reported [11]. Microring resonators however are very temperature sensitive and require extra control circuits. Therefore it may not be a practical solution.
- Tight integration of electronics and photonics: the use of Si Photonics tightly integrated with the drive electronics can lessen driver power consumption, for example through careful co-optimization of the electrodes of the Si Photonic Mach-Zehnder modulator (MZM) with the electronics, or through elimination of the termination resistor [12].

It is anticipated that energy efficiencies as low as a few picoJoules/bit can be achieved.

In addition, Si Photonic MZMs in combination with the use of single-mode fibres and a suitable laser light source can achieve transmission distances of several tens of kilometres over standard single-mode fibre (depending of course on the bit-rate and wavelength window), exceeding the 2km requirement for next generation datacentres. Additionally, Si Photonics do not exhibit the same reliability problems encountered when scaling the bitrate of VCSELs. Finally,

Si Photonics can leverage the massive manufacturing capability of the highly mature IC foundries to drive down costs. This is especially important as future datacentres may require millions of links, equipped with Terabit/s class links. For these reasons, Si Photonics is widely believed to provide an answer to the needs of new data centres.

Naturally, Si Photonics also still faces significant challenges:

- Foremost are the packaging requirements: indeed as Si Photonic waveguides are very small (typical cross section of a rectangular Si Photonic waveguide is a few 100nanometer each side), special focussing and alignment techniques are still being developed worldwide (and also in Tyndall!) to couple light from the single-mode fibre to the Si Photonic waveguide (and vice-versa). There are also challenges to be addressed to cost-effectively integrate together with the external laser source, as well as the drive/receive electronics.
- Despite promises of energy-savings, we are still short of the 1picoJoule/bit target.
- Bit-rates: even though bit-rates can be more readily scaled compared to VCSEL and multimode technology, achieving Terabit/s links cannot be done using today's technology in a single serial stream of bits. Multiplexing will still be required. Note however that to achieve a Terabit/s, one would for example need 40x 25Gb/s modulators (with drive electronics) and 40x 25Gb/s photodetectors (with receive electronics). These would all need to be integrated into more or less the same physical volume as today's 100Gb/s transceivers (to ensure that the front-panels of the switches do not explode in size). Clearly, simple adding of multiplexed channels is not practicable. Therefore, it will also be necessary to increase the individual bit-rates per channel.

1.2 State-of-the-art solutions

The development of silicon photonic technology in past ten years are presented in the book [6] published in 2016. In this section, I would like to focus on the latest and most advanced solutions for both monolithic and hybrid integrations.

1.2.1 Monolithic integration

In 2016, IBM presented their latest monolithic silicon photonic transmitters for both NRZ and 4-level pulse amplitude modulation (PAM4). In [9], the MZM has been designed and fabricated based on special process known as IBM's sub-100nm CMOS integrated nano photonic technology (CMOS9WG). The layout of the MZM is shown in Fig. 1.4. The two arms of the MZM are curved into an S shape. Therefore, the electrode is divided into two parts, the 180 degree turns curves (which do not have any electrode connected to the PN junction), and the straight lines where the metal electrode is connected to the PN junction. From the electromagnetic (EM) perspective, the 180 degree curves act like capacitors, and the straight lines with metal electrode act like inductors. Therefore, an LC ladder is formed and acts as a transmission line. The thermally tuned coupler is also added to couple the laser light in-and-out of the chip. On-chip 50Ω resistors are placed at the end of the electrode for impedance matching. So, for one electrode, the total length of 180 turning curve is $2.04mm$ and straight line is $2.8mm$ [9].

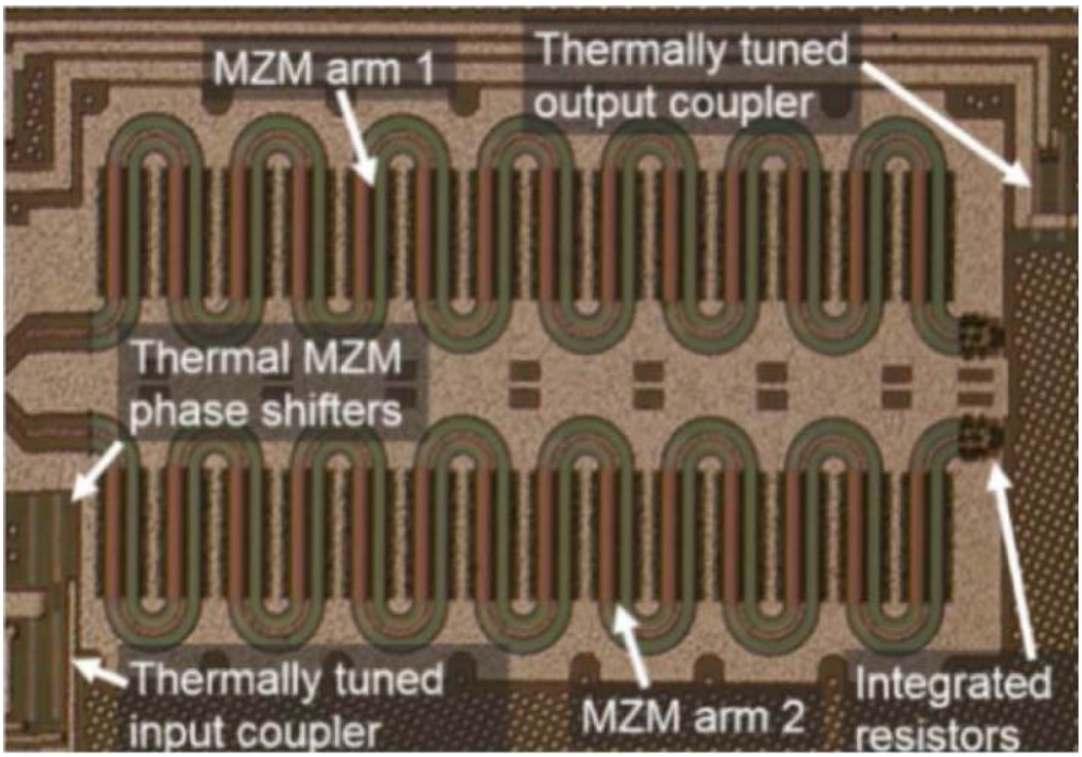


Figure 1.4: Micrograph of a silicon photonic TW MZM

The overall design including the CMOS driver is shown in Fig. 1.5. The CMOS driver and MZM are integrated on the same die [9]. The CMOS driver IC con-

sists of three stages of current mode logic (CML) differential amplifiers as pre-driver, and a 50Ω power amplifier with digitally controlled current tail. The output of this transmitter is 32 Gb/s NRZ signal with a bit error rate (BER) $< 10^{-12}$ and the overall energy efficiency is 4.4pJ/bit. [9]

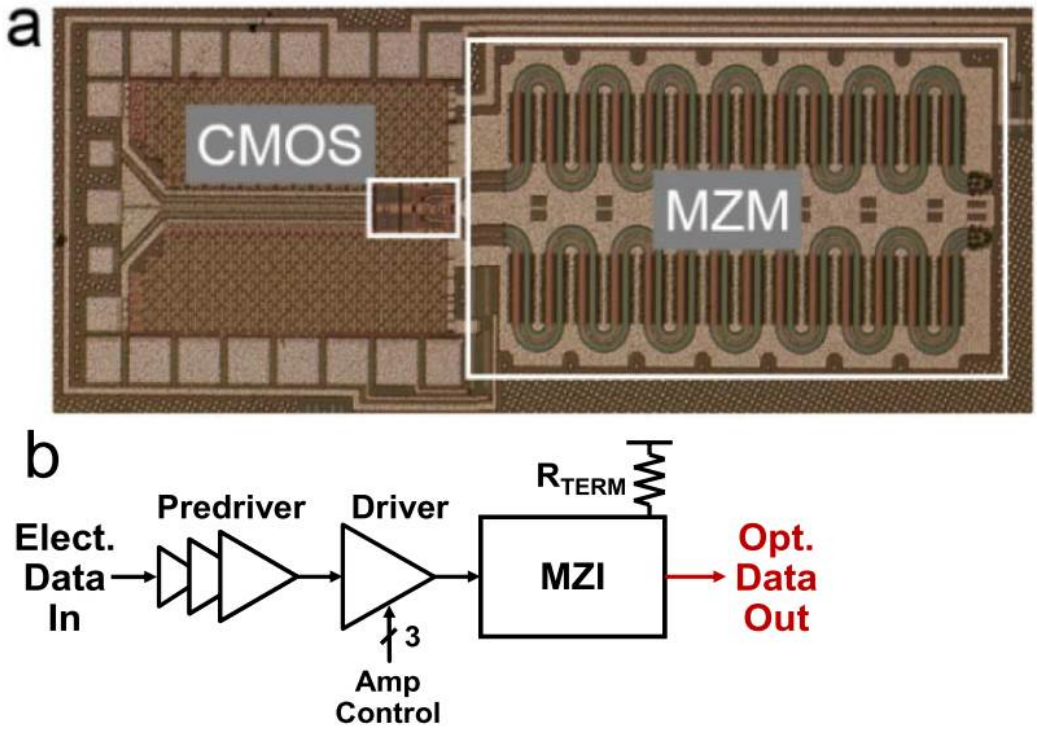


Figure 1.5: (a) Micrograph of a monolithic MZM transmitter, (b) schematic of the CMOS driver circuit

By using the same process (CMOS9WG), a PAM4 transmitter was also designed and fabricated [13]. In Fig. 1.6, the CMOS driver in [9] has been reused in this design marked by yellow squares. Each arm of the MZM is divided into two segments with 1mm and 2mm length respectively, and both segments are designed as transmission lines. The most significant bit (MSB) data drives the 2mm segment and the least significant bit (LSB) drives the 1 mm segment. By doing so, the binary weight electro-optical DAC are formed and the PAM4 signal is generated. Each segment is terminated by 50Ω for impedance matching. The monolithic PAM4 transmitter achieves 56 Gb/s PAM4 data rate with BER $< 10^{-12}$. Its overall efficiency is 4.8 pJ/bit. [13]

In summary, TWMZMs have been integrated monolithically on the same die as the CMOS driver. 32 Gb/s NRZ and 56Gb/s PAM4 are achieved and the overall efficiency is 4.4 pJ/bit and 4.8 pJ/bit respectively. However, the drawback is the special process (CMOS9WG). [9] [13]. Note that investment to transfer the

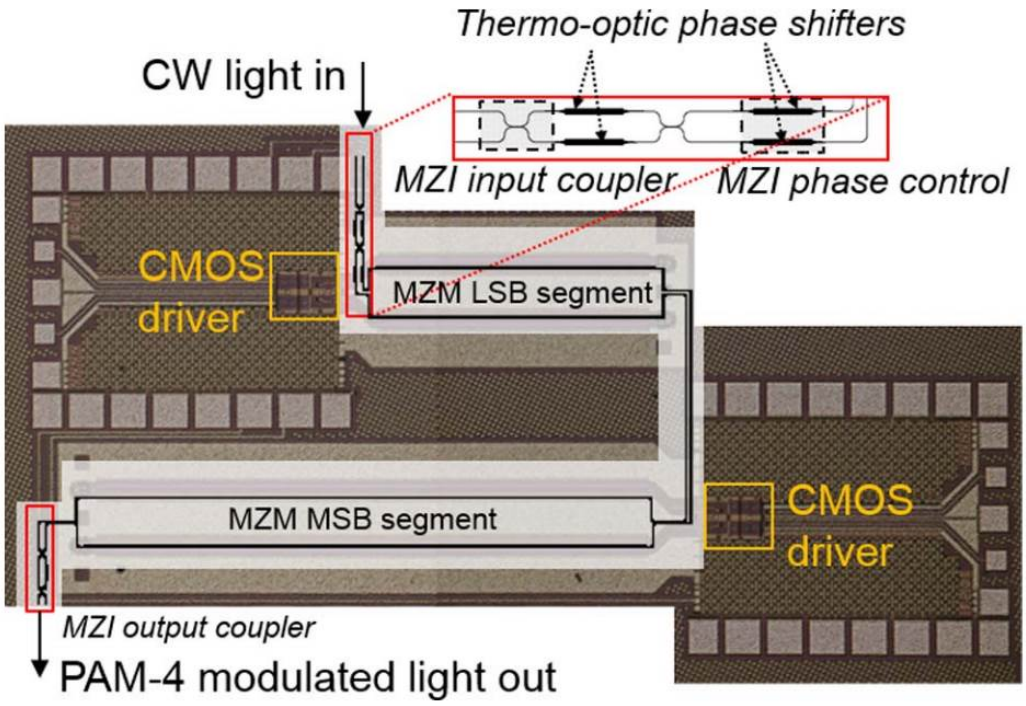


Figure 1.6: Micrograph of a monolithic MZM PAM4 transmitter

optical functions to a next node (65nm, 40nm, 28nm) could be substantial and may not be economic, which is another advantage of hybrid integration.

1.2.2 Hybrid integration

Unlike the monolithic integration, in hybrid integration the electronic driver IC and silicon photonic IC are realized in different chips using different processes and are then connected together through for example the flip-chip process. So, the standard commercial CMOS or BiCMOS process are available for electronic driver IC, which means the functionality of the driver IC can be more complex. From the silicon photonic perspective, the stand-alone process is optimized for optical performance only and no compromises are necessary to ensure good performance of the transistors. However, the drawback is obvious: now the packaging is a big challenge. Additional parasitic capacitance, inductance and resistance associated with the packaging methodology may limit bandwidth and energy efficiency of the driver.

In 2015, Finisar, one of the world leading companies in optical communications, presented a complete solution of an optical transceiver based on the silicon photonic and BiCMOS technologies using hybrid integration [10]. The

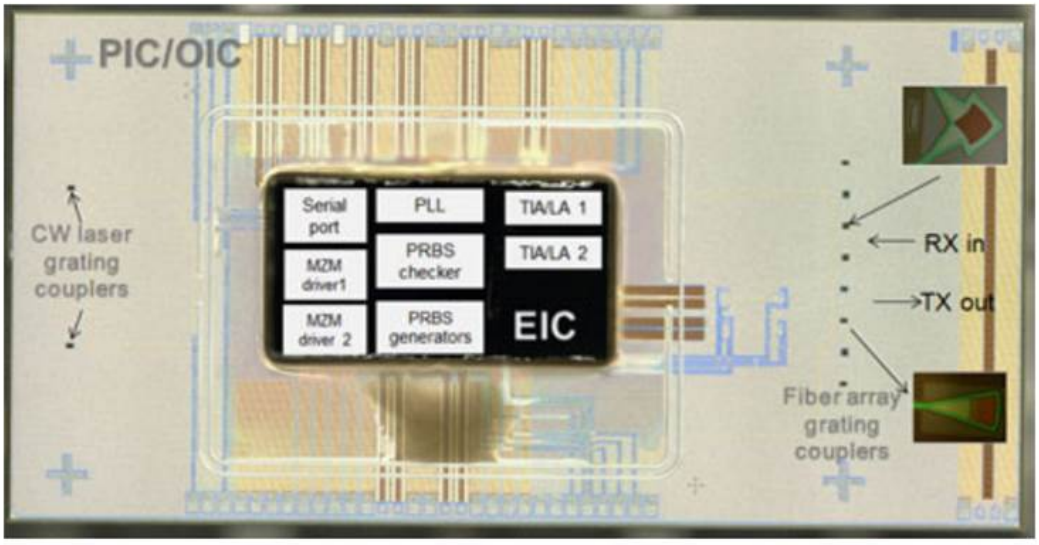


Figure 1.7: Micrograph of Finisar hybrid silicon photonic transmitter

overall design is shown in Fig. 1.7. The electronic IC (EIC) is flip-chipped on top of the silicon photonic IC (PIC/OIC). The electronic IC includes MZM drivers, trans-impedance amplifiers (TIAs) and linear amplifiers (LAs), a phase lock loop (PLL) for clock and data recovery (CDR) and synchronization, and PRBS generators and checkers for the calibration. For the PIC, on the left side, the external continues wave (CW) laser signal is coupled into the PIC through the grating couplers. The modulated optical data is sent out or received through the other grating couplers on the right side of PIC. [10]

The schematic is shown in Fig. 1.8. The travelling-wave MZMs and germanium photodetectors (Ge PD) are integrated on the PIC, functioning as the optical transmitter and optical receiver respectively. On the EIC, the MZM driver transfers the digital data from PRBS generator into travelling-wave MZMs and the TIA/LA translates the optical digital signal into the electronic domain [10]. The overall power consumption is shown in Fig. 1.9. It can be seen how the MZM driver stage consumes the most power of the entire system, 30% of the total power. 430mW is dissipated to transfer the data at 56Gb/s, which is 7.68pJ/bit in terms of power efficiency [10]. From the system perspective, improving the power efficiency of the driver stage is the key to increase the overall efficiency of the entire transceiver.

One way to increase the efficiency of MZM driver stage is using advanced BiCMOS technology. The process used in [10] is 130nm SiGe BiCMOS technology. One research group from University Pavia used the latest 55nm SiGe BiCMOS

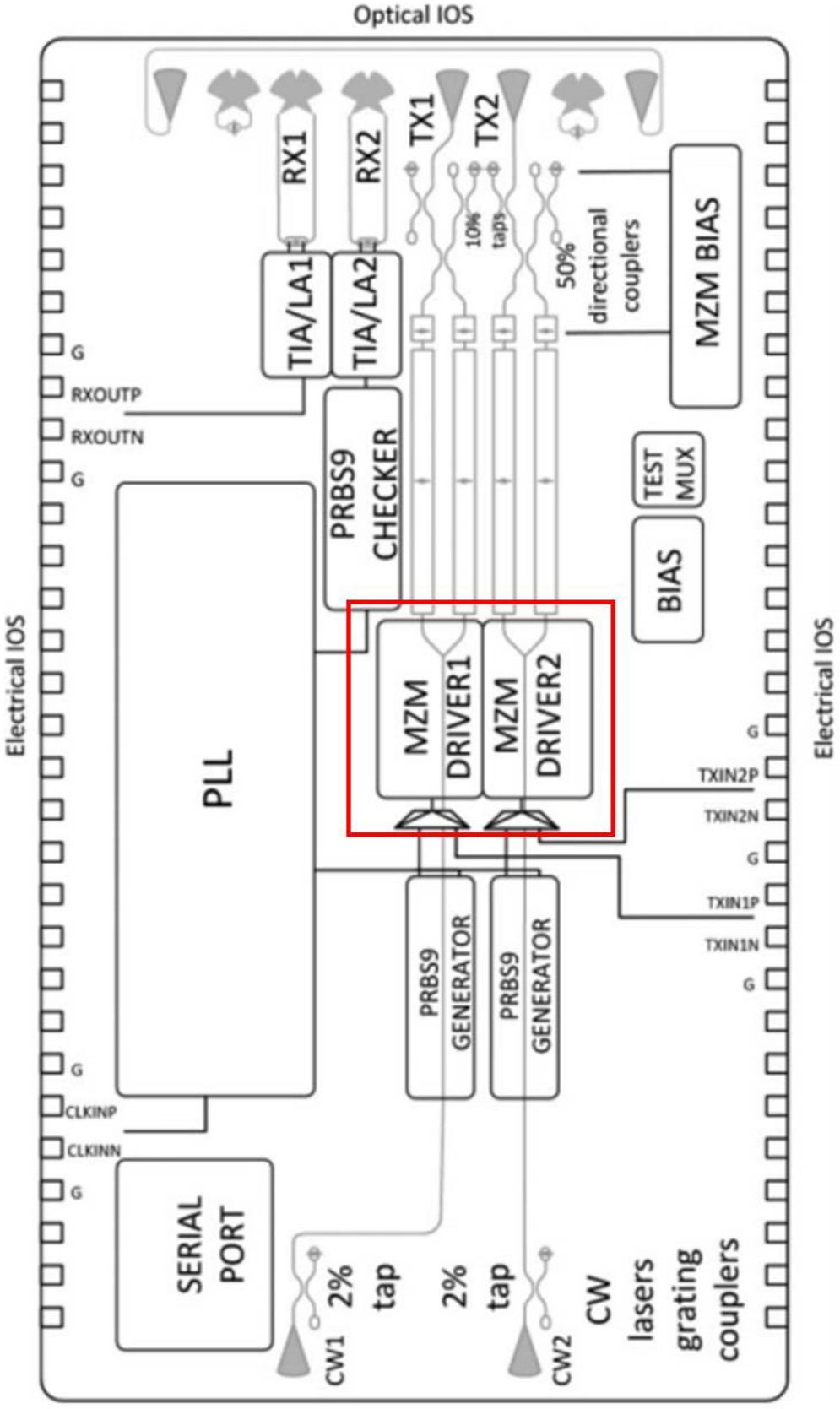


Figure 1.8: Schematic of Finisar hybrid silicon photonic transmitter

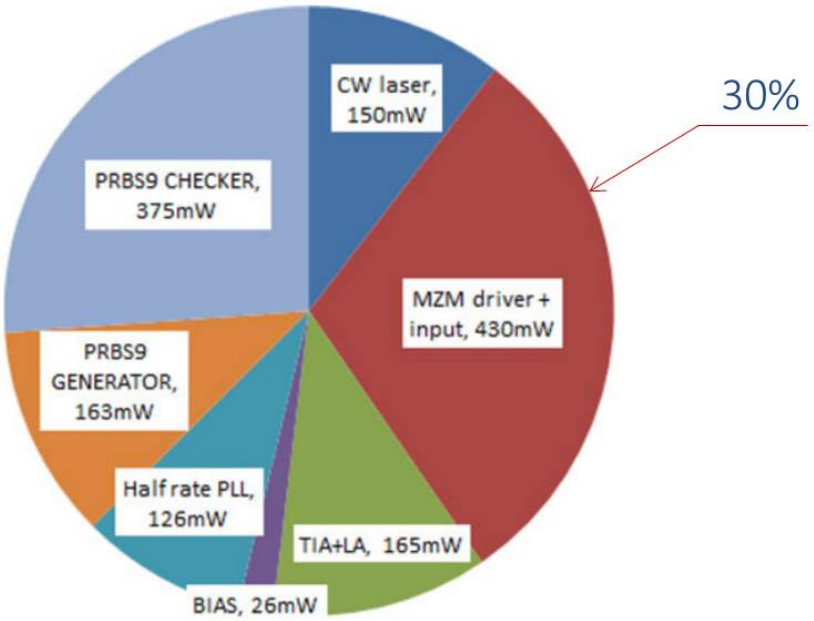


Figure 1.9: Power consumption of Finisar hybrid silicon photonic transmitter

process to increase the power efficiency of the driver stage [14]. The overall design is shown in Fig. 1.10. The BiCMOS driver IC (EIC) is flip-chipped on top of the silicon PIC, which is similar as the [10]. The travelling-wave MZM is also used on PIC as the optical modulator.

The schematic is shown in Fig. 1.11. The input stage is an emitter follower, which enhances the external high speed data signal generated from instruments and send the data into pre-driving stage. The pre-driving stage is designed as two emitter-coupled logic (ECL) pairs with different input filters, which divides the input data into low frequency band and high frequency band. By tuning the tail currents, both variable gain amplifier (VGA) and equalization functions are realized. The high and low frequency bands are combined together through the common-base transistors as the final output. The shunt peaking inductors and series resistors are connected to the collectors of the transistors. For the driving stage, to increase the driving efficiency of the ECL pair, AC coupling capacitors are used to provide fast current switching. From the MZM perspective, the output resistance of driving stage (R_{out}), the characteristic impedance of the MZM's electrodes (Z_0), and the termination resistance (R_L) are the same for maximum power transfer. In addition, large de-coupling capacitors (C_C and C_L) and resistor (R_B) are used to provide the DC biasing for MZM. This modulator can be operated at 56Gb/s NRZ signal with 5.36pJ/bit. [14]

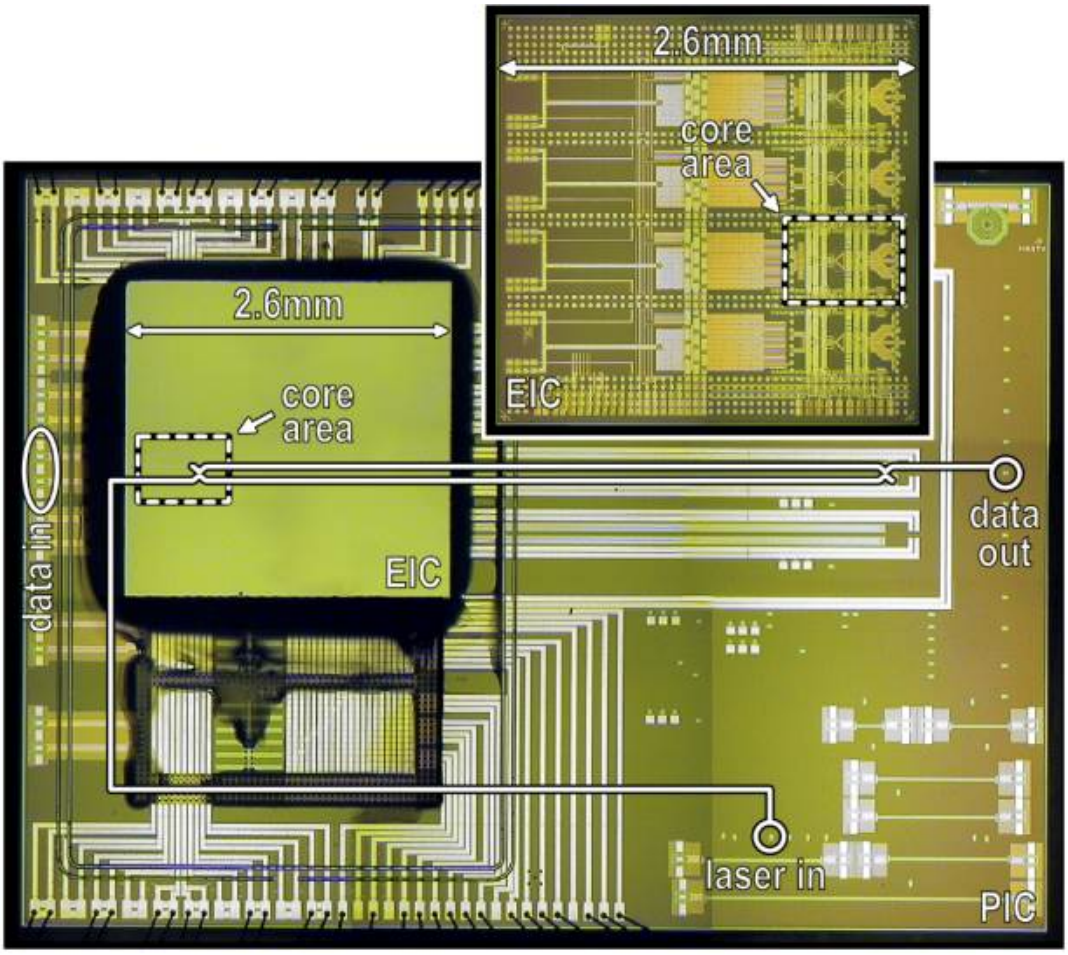


Figure 1.10: Micrograph of the hybrid silicon photonic transmitter design by University of Pavia

From the discussion of monolithic and hybrid integration above, we see that the overall energy efficiency range between 4.4pJ/bit and 5.4pJ/bit for the tier of 2016 regardless the integration approach. The power efficiency improves ∼2.5 pJ/bit compared to the tier of 2015 (7.68pJ/bit). $\sim 30\%$ improvement has been achieved due to more advanced CMOS/BiCMOS processes. However, the fundamental driving scheme is the same in past two years. Everything is based on the standard 50Ω RF system. So, eventually, power limitations will put an end to further increasing capacity, if we keep using the same 50Ω RF system for future designs, because the power for a given voltage swing is fixed for the 50Ω RF system. In addition, the 50Ω does not scale down with more advanced CMOS/BiCMOS processes. One alternative approach was presented in 2014 known as the segmented lumped MZM in [15]. The overall power efficiency (1∼2 pJ/bit) is better than the TW MZM. However the data rate (20Gb/s PAM4) is much slower than the designs discussed previously. The

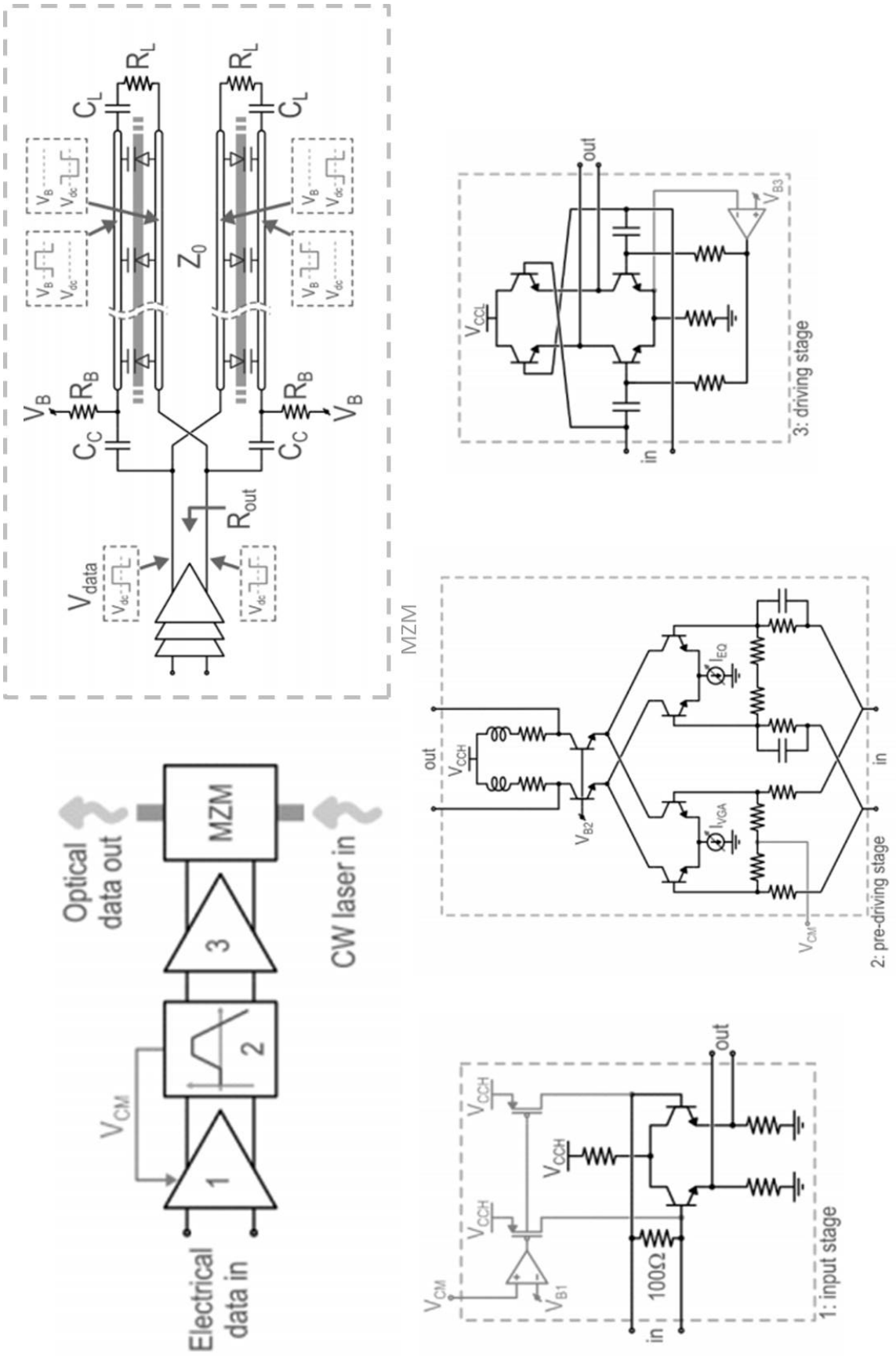


Figure 1.11: Schematic of the hybrid silicon photonic transmitter design by University of Pavia

main reason is that the MZM is now a capacitor instead of a transmission line and the overall bandwidth is heavily limited by the RC constant. In a nutshell, new driving schemes are required if we want to achieve the 1pJ/bit target at high data rates.

1.3 PhD research objective

Against the above discussions, my PhD research has the following objectives:

- Design and fabrication of a driver circuit for multilevel modulation formats. Specifically, the target is to:
  - Use a PAM-4 modulation format.
  - Achieve a bit-rate between 20Gb/s and 56Gb/s (10 Gbaud/s to 28 Gbaud/s, depending upon the modulator bandwidth).
  - Include several innovative circuit techniques to overcome bandwidth limitations of the modulator and the packaging parasitics.
  - Include the required binary to Gray encoder (see also below).
  - Use deep submicton CMOS process (for example here 65nm CMOS from STMicroelectronics was used due to high f_t [16])
- Test of the driver, after assembly with the required Si Photonics optical chip. This optical chip will be developed in collaboration with the SFI-funded I-PIC project, and will consist of the required grating couplers as well as the Mach-Zehnder modulator structure.

The schematic and package of proposed PAM-4 modulator driver are shown in Fig. 1.12. The hybrid integration approach has been chosen as it allows to make optimum technology choices for both photonics and electronics using the processes available under the form of multi project wafer services. The driver IC (EIC) is flip-chipped on top of the silicon photonic MZM (PIC). From the packaging perspective, the high speed PCB and ceramic board are necessary for coupling the high speed data and clock signals from external instruments to the EIC. An external continues-wave laser provides the light source for the silicon photonic MZM (PIC). The modulated optical signal will be captured by a standard commercial PD and TIA. The measurement results will be displayed

by high speed oscilloscope. All details shown in Fig. 1.12 will be discussed later. The following challenges will be addressed during this design work:

- Achieving high energy-efficiency. This will be addressed through:
  - Using driver structures with high power efficiency, as used for example in UWB applications (class A, class AB, class B power amplifiers), as well as optimized digital gates for driving the MZM (especially in its lumped version, the electrical equivalent of an MZM is a capacitor). In case power amplifiers are the optimum structure, three challenges need to be addressed when using such amplifiers for broadband optical applications: 1) achieving required broadband operation,and 2) ensuring that any passive components required for broadband impedance matching can be integrated on-chip.
  - Optimizing the structure of the driver together with the Si Photonic modulator. In particular, the performance of purely distributed structures (whereby the MZM electrodes are under the form of transmission lines) and lumped driver (splitting up the MZM into sections driven by individual drivers) will be studied in detail.
- Achieving the required voltage swing despite the low breakdown voltage of the CMOS transistors. Indeed 65nm CMOS transistors have gate-source/drain breakdown voltages in the order of 1V, moreover the drain-to-source voltages cannot exceed much beyond 1V as well. As a result special stacked driver structures will be required, depending on the exact drive requirements for the MZM. Here it will be important to study different driving schemes, such as push-pull operation as well single-ended vs differential drive.
- Maintaining the driver performance despite large process spread of the 65nm CMOS transistors. The very fine lithography, gate oxide thickness and small active regions of the 65nm CMOS transistors mean that these exhibit large spreads in their characteristics (e.g. threshold voltage and mobility). This will require the use of e.g. equalization structures to circumvent bandwidth limitations in “slow” process corners.
- Achieving the required speed: this may require e.g. inductive peaking techniques. An FIR-based filter structure may also be added to address bandwidth limitations. Careful modelling of the interconnect parasitics will also be done to facilitate accurate simulations.

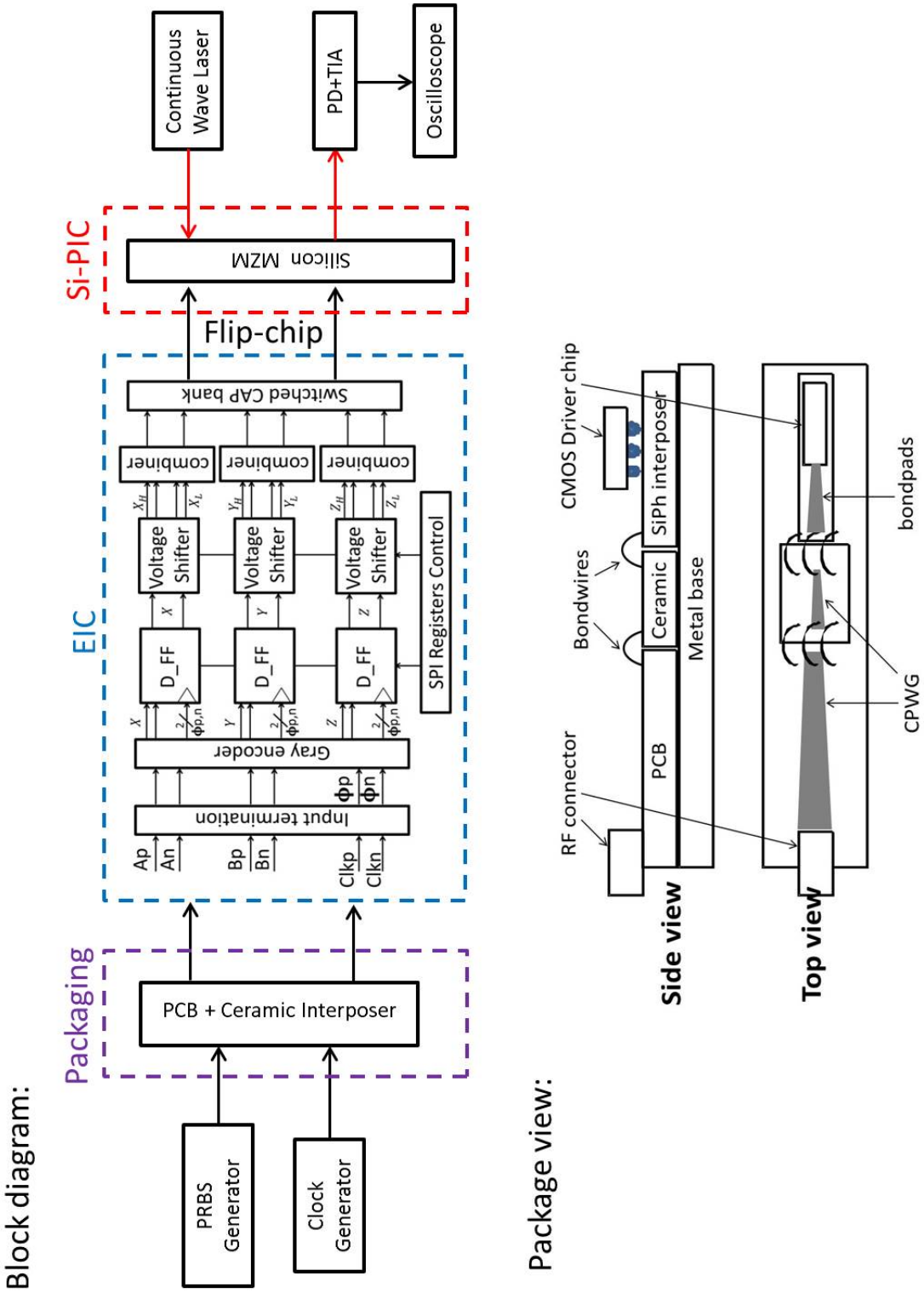


Figure 1.12: Top-level block diagram and package view of the proposed PAM-4 modulator driver

1.4 Summary

In this chapter, I have discussed the background information about the next generation short reach optical link for data centres and reviewed the latest state-of-the-art designs. My PhD research objectives are listed following the discussion.

Chapter 2

Silicon Photonic Mach-Zehnder Modulator

Before diving into the CMOS driver IC design, I would like to discuss about the optical device the Mach-Zehnder Modulator (MZM) first. The fundamental principle of MZM can be found in the textbook [17]. In this chapter, I focus on the silicon photonic MZM device. Comparing with the traditional $LiNbO_3$ based MZM presented in [17], the silicon photonic technology miniaturizes MZM dramatically. From the reference [18], the size is within millimeter range. This brings several advantages and challenges for MZM design. And the performance between TW-MZM and Lumped MZM should be re-considered with silicon photonic technology for short reach optical communication system. First, I will discuss the DC characteristics of the silicon photonic MZM (IMEC iSIPP25G). And then I will give the analysis comparing TW-MZM and Lumped MZM, Finally, the bandwidth enhancement technique will be presented for Lumped-MZM.

2.1 DC characteristics of Silicon Photonic MZM

Based on [19], the normalized electro-optical transfer function of a MZM is shown in formula (2.1), where V_1 and V_2 are RF signals applied on each MZM electrode respectively; V_{DCbias} is the sum of the biasing voltages applied on both electrodes of the MZM and V_π is the voltage that can change the phase in one modulator arm by 180 degree, thereby letting the MZM switch from full transmission to full extinction [19]. In this thesis, the MZM is always driven in

push-pull configuration. Conventionally, an interferometric MZM is biased at its so-called quadrature point of its transfer function. By applying push pull drive signals on both arms with a swing equal to half V_π, the modulated extinction ratio (defined as the ratio of the highest power to the lower power after the MZM when applying the drive signal) can then in principle be as high as the DC extinction ratio which is typically of the order of 20dB. Although in practice, as explained below it is difficult to achieve modulated extinction ratios as high as this due to practical drive amplitude limitations.

$$P_{optical} = |T_E(V_1, V_2)|^2 = \cos^2\left[\frac{\pi}{2} \times \left(\frac{V_1 - V_2 - V_{DCbias}}{V_\pi}\right)\right] \tag{2.1}$$

For transceivers intended for short-reach optical links, low power consumption and process technology suitable for high volume production are important requirements. Therefore it is advantageous to realize the driver circuit in a deep submicron CMOS process node. However usually the CMOS transistors in such a process node cannot withstand voltage swings beyond $1V$ to $2V$ without breaking down. Even when using more complex SiGe BiCMOS processes, careful consideration must be paid to the breakdown voltage of the high-speed heterojunction bipolar transistors (HBTs), which can be as low as $1.5V$. Such low breakdown voltages are challenging when attempting to drive MZMs whose V_π may exceed those voltages. Indeed for example modulators available from the ISIPP25G technology can have an $V_\pi \times L$ product of $12V \times mm$. A $1.5mm$ long MZM then has a V_π of $8V$ [20]. Even when using circuit techniques to increase the available voltage swing from drivers realized using deep submicron CMOS processes, typically no more than a few Volt swing is available. Therefore, transmitters based upon Silicon Photonic MZMs which use drivers realized in deep submicron CMOS or SiGe BiCMOS typically have poor extinction ratio ($\sim$2.6dB) ($\sim$50Gb/s) [10] [14]. A push pull driving scheme whereby both arms are modulated in anti-phase helps by halving the required driver voltage swing for a given V_π, however even then in our particular example a driver with $4V$ swing is required which is highly challenging for deep submicron CMOS and SiGe BiCMOS technologies.

Therefore here we consider the optical link performance when modulating the MZM with a swing less than V_π. Fig. 2.1 shows the transfer curve of an MZM with $V_\pi = 8V$ according to (2.1). We consider modulation of the MZM with a push-pull voltage swing of $2V$, which is achievable using a deep submicron CMOS driver circuit [21]. Clearly, to improve the ER with this limited voltage

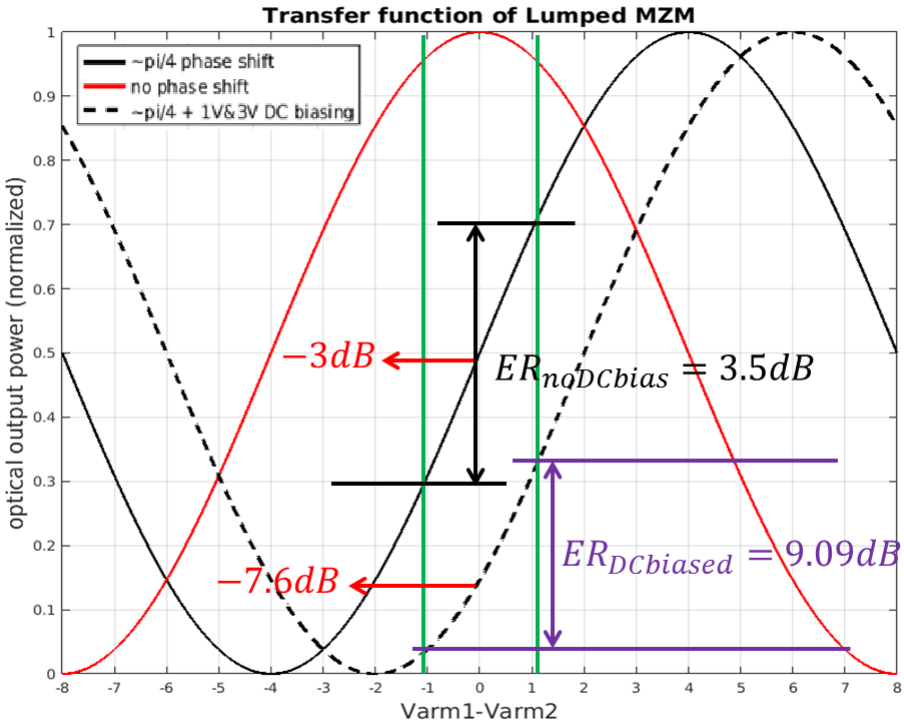


Figure 2.1: Electro-optical transfer function of MZM

swing one can choose the DC bias point of the Silicon Photonic MZM below its quadrature point. For example by biasing the MZM at 6V, 9dB ER can be achieved. However, two challenges arise.

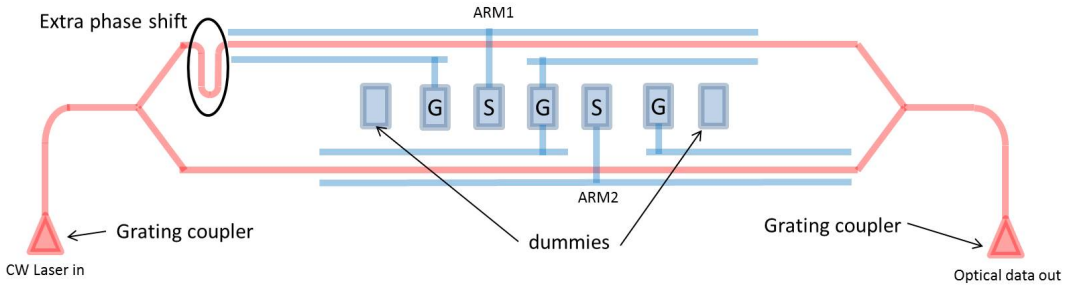


Figure 2.2: Asymmetrical MZM

The first challenge is how to provide the DC bias to the modulator. To compensate for random process and temperature variations in the MZM transfer curve, this DC bias must be actively controlled [22]. To realize dense integration such control circuit is preferably integrated together with the driver IC, which can then be flip-chipped on top of the silicon photonic IC [23]. However handling voltages as high as $6V$ is difficult on standard deep submicron CMOS technologies: for example while capacitive coupling could be used (see next Chapter

how this can be done), the breakdown voltage of on-chip capacitors is typically no higher than ∼5V for 65nm CMOS process [24], leaving little to no room for the RF signal itself. Based on [20], the solution is to use an asymmetrical MZM as shown as Fig.2.2: a length difference is introduced between the two optical paths, whose phase difference is the same as applying a half V_π shift in the transfer curve (2.1). The new transfer function is shown as (2.2) and plotted as the black curve in Fig.2.1. The quadrature point has been shifted to 0V thus reducing the required bias voltage for a given extinction ratio. For example the asymmetrical MZM only needs 2V DC bias voltage to achieve 9dB ER (black dots curve in Fig.2.1) instead of 6V for the symmetrical MZM (red curve in Fig. 2.1). Of course note that active bias control remains necessary due to unavoidable process variations, however with the π phase shift the maximum required bias voltage can be significantly reduced.

$$P_{optical} = |T_E(V_1, V_2)|^2 = \cos^2\left[\frac{\pi}{2} \times \left(\frac{V_1 - V_2 - V_{DCbias}}{8V}\right) - \frac{\pi}{4}\right] \tag{2.2}$$

The second challenge is the trade-off between the extinction ratio on one hand and modulation loss on the other hand, as a function of the used RF swing. The modulation loss is defined as:

$$ML = 10log_{10}\left(\frac{P_{high} + P_{low}}{2P_{CW}}\right) \tag{2.3}$$

where P_{CW} is the power at the input to the modulator (i.e. the power from the laser minus the coupling and waveguide losses). P_{high} and P_{low} are the maximum respectively minimum optical powers after the modulator when the RF signal is applied. This trade-off is shown for an assymetrical MZM on Fig. 2.3 for three different voltage swings ($V_\pi = 8V$). The curves show the achieved modulation loss and extinction ratio for a particular bias setting. Note that the trade-off between insertion loss and extinction is especially severe for RF swings small compared to V_π. For example for an RF swing of $1.0V$ (the voltage applied to a single arm in a push pull drive scheme), 10dB extinction ratio incurs a modulation loss of ∼8dB. Reduced modulation loss can be achieved at the expense of a significantly worse extinction ratio, for example 2dB modulation loss would result in an extinction ratio of 4dB. Obviously, such trade-off has an impact on the achievable optical budget.

To analyze this impact and determine the optimum bias point, optical budget

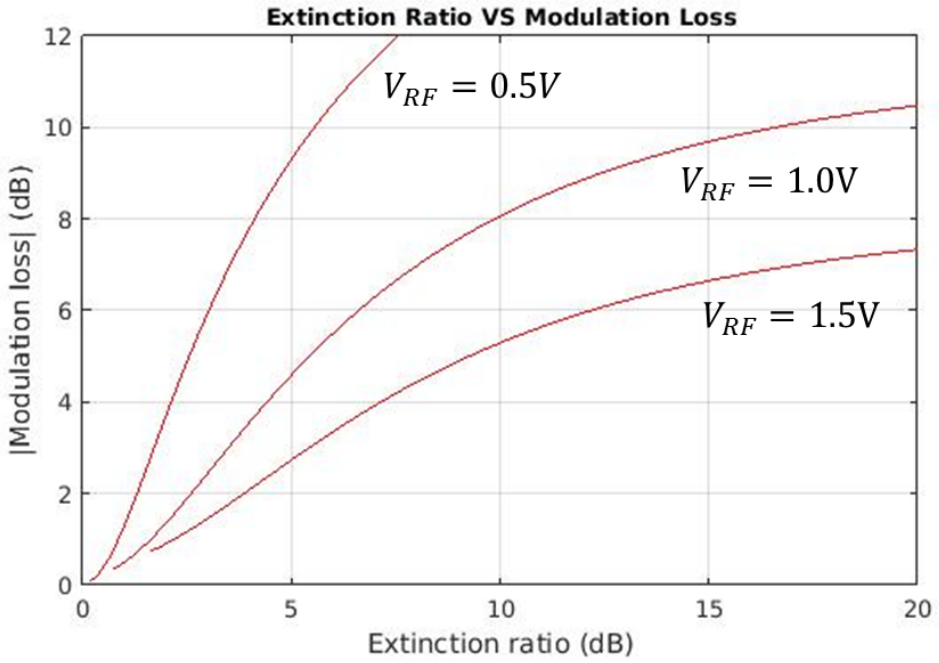


Figure 2.3: The trade-off between insertion loss of the modulator and extinction ratio for different applied voltage swings (V_{RF} is the voltage applied to a single arm in a push pull scheme) ($V_\pi = 8V$).

calculations were performed assuming a link consisting of a laser (launch power from the laser is assumed to be +10dBm), coupled via a grating coupler and routing waveguide to the Silicon Photonic MZM, and back out using a second grating coupler. The total loss of the two grating couplers, the routing waveguides and the modulator waveguides was assumed to be 11.9dB [20]. The receiver was modeled using a fourth order Bessel-Thomson filter with a 3dB bandwidth of 20GHz; its total input referred noise current was $2.9\mu A_{rms}$. Fig. 2.4 shows the available optical budget (defined as the difference between the power launched after the second grating coupler into the fibre and the receiver sensitivity for the realized extinction ratio, at a bit-error ratio of 10^{-3}) for PAM4 modulation format based on the asymmetrical MZM: each curve was generated by sweeping the bias voltage of the modulator, calculate the resulting additional modulation loss and extinction ratio and then determine the achievable optical budget for a bit-error rate of 10^{-3}. The extinction ratio is defined as the ratio of the power of the highest PAM4 symbol to the lowest PAM4 symbol. Equidistant PAM4 symbols are also assumed, which can be done by pre-compensating the driver voltage levels (see Chapter 3). The bias voltage was swept such that each time the full S-curve of the modulator is covered.

Fig. 2.4 shows the achievable optical budget for four different voltage swings

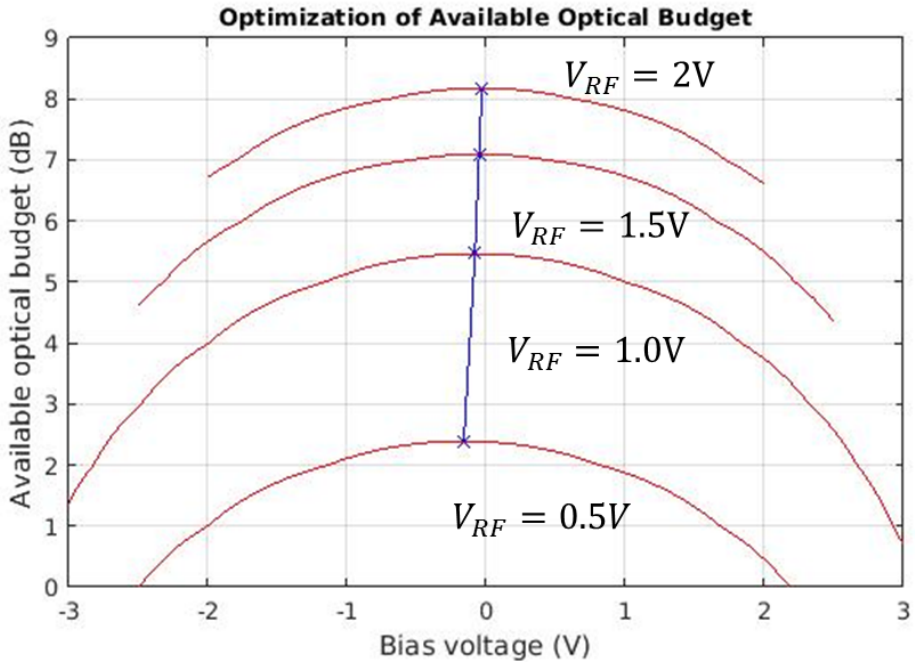


Figure 2.4: Available optical budget ($V_\pi = 8V$) for different applied voltage swing (V_{RF} is the voltage applied to a single arm in a push pull scheme). The locus of optimum bias voltages is shown as well

as a function of bias voltage. It can be seen how even at reduced RF swings, the optimum bias point to maximize the optical budget remains close to the MZM quadrature point. For bias voltages less than this optimum bias point, the extinction ratio improves, however this is more than offset by the worse modulation loss reducing the overall achievable optical budget. Conversely, for bias voltages higher than this optimum bias point, the modulation loss is improved, which then however is offset by a worsening extinction ratio thus again reducing optical budget compared to the maximum achievable optical budget. This trade-off is significant for low RF swings with ∼5dB difference between the optimum bias point and the worst-case bias. For increasing RF swings this trade-off becomes less severe. It is also important to point out that sufficient optical budget is available to support a link with 5.5dB optical budget at an RF swing of 1V, which corresponds to the achieved value in our proposed PAM-4 transmitter, see Section 2.3.

2.2 Travelling wave MZM VS Lumped MZM

Based on the textbook [17] and [25], the electrodes of a high speed MZM are conventionally implemented as transmission lines which distributes the capacitance and inductance over the entire length of the device, which enhances the modulation efficiency over a large bandwidth . In addition, impedance matching of microwave and optical anti-reflection are desired. The microwave attenuation of TW electrode and optical loss should be minimized. To achieve the optimal performance for TW-MZM, the microwave group velocity should be matched with the optical group velocity [26] [27].Any walk-off between the RF and optical signals reduces the effective bandwidth of the modulator. As Silicon Photonic modulators have a length of only a few millimeter, the penalty due to velocity mismatch can be reduced.

2.2.1 Velocity mismatch of TW-MZM

Based on the reference [19] [25] [26] [27], we can derive the expression of the optical power transfer function of a TW-MZM as a function of modulation frequency f as (2.4)by assuming no microwave attenuation of the electrodes, perfect impedance matching and no optical loss in the waveguide. In addition, it is assumed that the TW-MZM is biased at its V_π point with $2V_\pi$ peak-to-peak voltage swing of one electrode arm and the second electrode grounded. n_0 is the optical refractive index. n_{RF} is the equivalent microwave refractive index which can be calculated as $n_{RF} = 1/\sqrt{\varepsilon\mu}$ where ε is dielectric constant and μ is the relative permeability of the electrode. L is the length of the electrode and c is the speed of light in the vacuum. The function (2.4) shows the relationship between the optical mismatch ($n_0 - n_{RF}$) and normalized optical output power of the MZM at a certain frequency of electrical signal (f). Note how the mismatch between n_{RF} and n_0 is multiplied by the length of electrode (L).

$$P_{TWMZM(norm)} = \cos^2\left\{\frac{\pi}{2}\cdot\left|\frac{sin\left[f\pi L\left(\frac{n_{RF}-n_0}{c}\right)\right]}{f\pi L\left(\frac{n_{RF}-n_0}{c}\right)}\right| - \frac{\pi}{2}\right\} \tag{2.4}$$

If the microwave signal and optical signal match perfectly ($n_{RF} = n_0$), the optical transfer would be one. The length of Silicon Photonic MZMs can be as short as a few millimeter, allowing significant mismatch before attenuation of the modulated optical signal: Fig. 2.5 shows the optical power transfer as

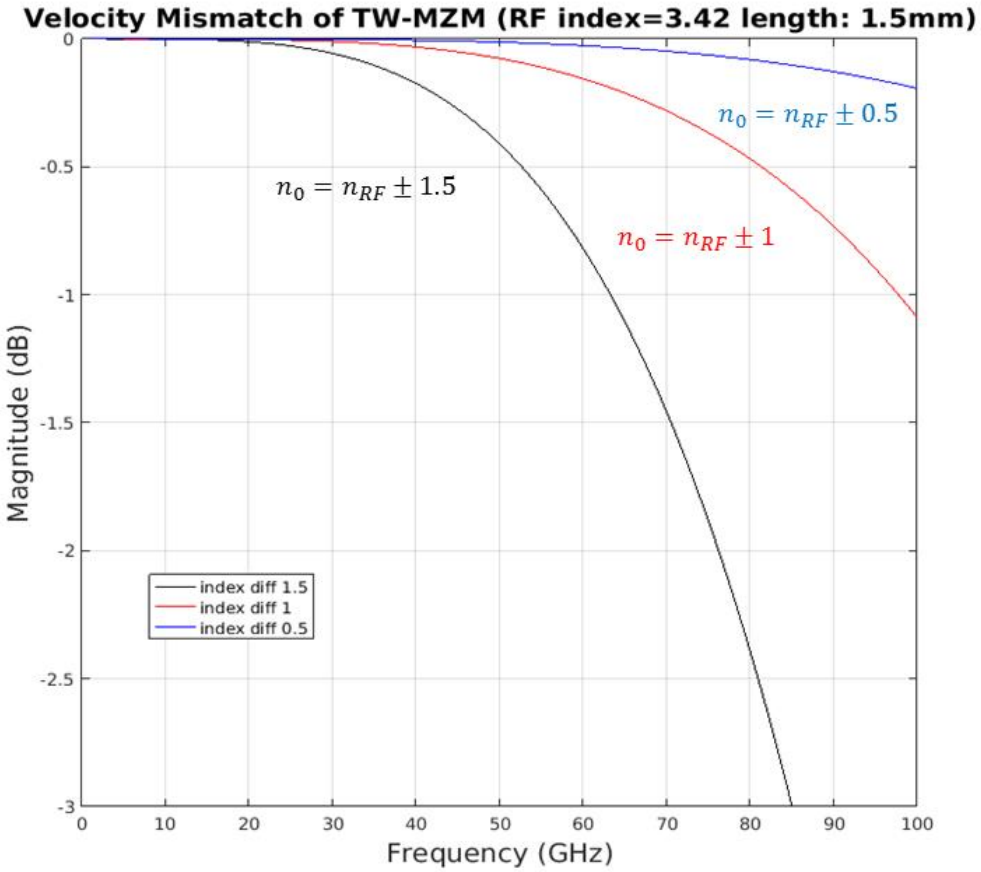


Figure 2.5: Velocity mismatch

a function of modulation frequency for a modulator with length $1.5mm$. The optical power transfer has been plotted for three mismatch ($n_0 - n_{RF}$) cases. Even for a large 50% mismatch ($n_0 - n_{RF} = \pm 1.5$), the -1dB bandwidth (purely due to velocity mismatch, hence not taking into account any RC limitations) is over 35GHz. Normally, the dielectric constant of silicon is around 11.68, therefore, the microwave refractive index is 3.42 which is close to the optical index of silicon. Hence, the expected -1dB bandwidth limitation due to the velocity mismatch is beyond 60GHz, more than sufficient for our application.

2.2.2 Effective electrical length of transmission line

As the length of the electrodes of a Silicon Photonic TW-MZM can be as short as a few millimeters, it is interesting to know untill what modulation frequency the electrodes can be considered to be electrically “short” or lumped devices and hence do not need to be implemented as transmission lines anymore. A

"long" electrode is generally considered to be one where the source's AC signal waveform completed at least a quarter-cycle (90 degree phase rotation) before the propagating signal reaches the end of the electrode, which means the signal at the start of the electrode is out of phase compared to the signal at the end of the electrode at a given time. In this case, the electrode of the MZM needs to be treated as a transmission line. The frequency where this happens is called the boundary frequency and can be calculated from [28], pages 59-61:

$$f_{\frac{\lambda}{4}} = \frac{c}{4Ln_{RF}} \tag{2.5}$$

Based on the discussion above, the boundary frequency can be derived as (2.5), where c is the speed of light in the vacuum, L is the electrical length of electrode, and n_{RF} is the microwave refractive index of the electrode. In Fig. 2.6, we are assuming a total electrode length of MZM is $1.5mm$. If we locate the signal source in the middle, the effective length to be taken into account halves to $750\mu m$. Based on (2.5), the boundary frequency for Lumped-MZM in Fig. 2.6 is 29.2GHz; and boundary frequency for the connection of TW-MZM is 14.6GHz, assuming the effective dielectric constant n_{RF} is 3.42. Therefore, as long as the Silicon Photonic MZM with a $1.5mm$ electrode is operated within a bandwidth ranging from DC to 29.3GHz, the electrode is electrically equivalent to a capacitor instead of a transmission line.

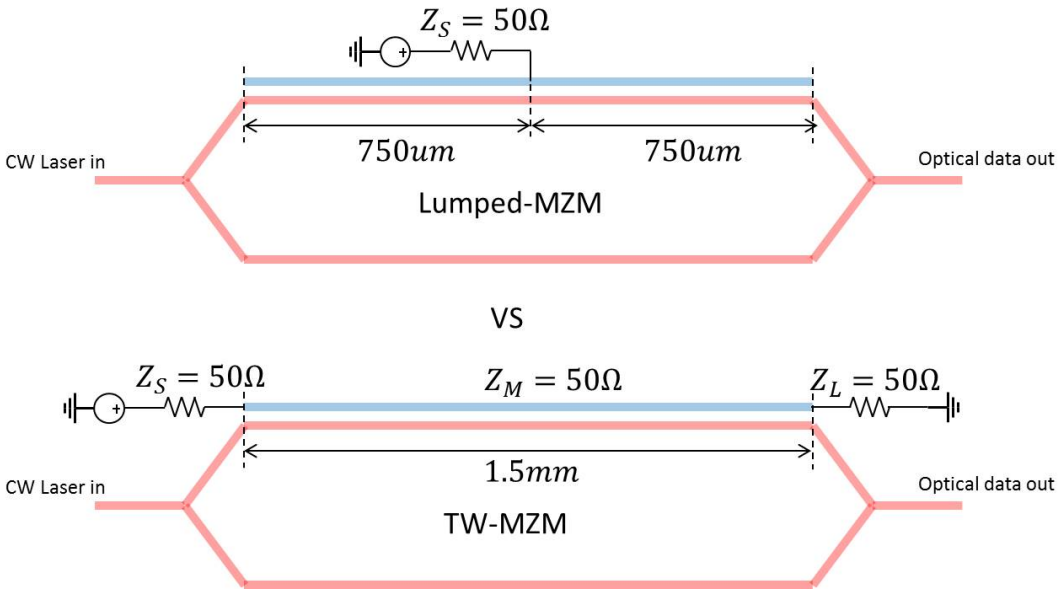


Figure 2.6: Electrical length of Lumped MZM and TW-MZM

For ease of testing, typically TW-MZM use transmission lines with a character-

istic impedance of 50Ω for the electrodes. To deliver the signal from the input of the transmission line to the end with maximum power transfer, the signal source impedance and termination impedance should then also be 50Ω, the same as the characteristic impedance of the electrode in TW-MZM [28]. The required matching networks need to have a large bandwidth (e.g. >20GHz for 25Gbaud optical links), which necessitates the use of resistive low-Q matching. Significant power is required to drive such a 50Ω termination transmission line [28].

In summary, for short reach optical link with DC-25GHz bandwidth of interest, the penalty of mismatch between microwave group velocity and optical group velocity can be ignored. The silicon photonic based asymmetrical MZM with $1.5mm$ length electrode could be characterized as a capacitive load (Lumped-MZM connection) instead of transmission line. From the electro-optical transfer function perspective, the asymmetrical MZM can reduce the DC biasing voltage. However, with limited RF swing, the trade-off between the ER and modulation loss cannot be achieved simultaneously. The optimal DC biasing point has been found based on the available optical budget.

2.3 Bandwidth enhancement for Lumped MZM

As pointed out in the previous section and [29] , a Silicon Photonic MZM with electrode length up to $\sim 1.5mm$ (assuming it is driven from the midpoint of each electrode) can be considered as the capacitor from the electrical point-of-view. When driving such a lumped MZM from the conventional 50Ω signal source, the bandwidth of the lumped MZM will be severely limited due to the low-pass filter formed by the 50Ω signal source and termination resistors, which can be calculated from (2.6) [29]. An alternative driving scheme with significantly larger bandwidth is presented here.

$$f_{-3dB} = \frac{1}{2 \cdot \pi R_{\Sigma} C_1} \tag{2.6}$$

The equivalent circuit model of a lumped MZM driven from a 50Ω signal source impedance and a 50Ω termination resistor is shown in Fig. 2.7(a). From the IMEC technology book [20] and packaging process in [23], the inductance of the interconnect between the driver and lumped MZM is negligible and par-

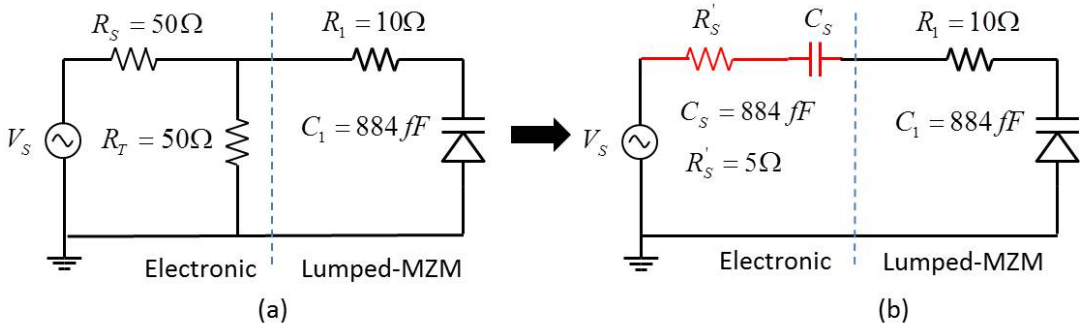


Figure 2.7: (a)The equivalent circuit model of Lumped-MZM and (b) bandwidth enhancement scheme

asitic resistance is 10Ω. The double termination halves the effective available voltage swing over the lumped MZM. For a lumped MZM with a capacitance of $884fF$ (corresponding to the load of a fabricated device, see Chapter 5), the bandwidth in the double terminated scheme is 5.1GHz. The obvious bandwidth limitations stemming from the 50Ω double matching can be overcome by driving the lumped MZM with a much lower signal source resistance (5Ω in this case) and eliminating the termination resistor, because the overall RC time constant is decreased. The bandwidth can be further enhanced by including a series capacitor with the lumped MZM, as shown in Fig. 2.7(b). If the value of this series capacitor is chosen the same as the lumped MZM, the effective voltage across the lumped MZM is the same as the 50Ω matching method (assuming the same signal source voltage), however now the bandwidth is 24GHz, more than sufficient for 25Gbaud signalling.

Another advantage of the proposed driving scheme using a series capacitor is that it can be readily extended to multilevel modulation formats such as 4 levels Pulse Amplitude Modulation (PAM4). In Fig. 2.7(b), the series source resistor (R_S') and capacitor (C_S) can be extend into three resistors with value of $3R_S'$ and three capacitors with value of $C_S/3$. The proposed PAM4 driving scheme for the silicon photonic Lumped-MZM will be presented in Chapter 3.

2.4 Summary

In this chapter, the silicon photonic MZM has been analyzed. From DC perspective, the large V_π would not be an issue, because the link budget is enough based on the standard model of the receiver, even the MZM is biased below

quadrature point with limited RF swing. From the bandwidth perspective, the velocity mismatch does not impact the high speed performance as long as the operational frequency below 30GHz for a TW-MZM with 1.5mm length electrodes. In addition, If the device is operated below 25GHz, the 1.5mm electrode of the MZM should be modelled as the capacitor (Lumped-MZM) instead of transmission line (travelling wave MZM). A bandwidth enhancment scheme for lumped MZM has been proposed to overcome RC limitation. The overall -3dB bandwidth is upto 24GHz, enough for 25Gbaud per second signal.

Chapter 3

PAM-4 driver design for Lumped MZM

In this chapter we address the design of a PAM-4 driver circuit intended to drive a lumped MZM. The circuit uses a novel switched capacitor approach to generate the PAM-4 signal. The operation and design decisions are described in detail. The circuit was implemented and fabricated using a 65nm CMOS process; measurement results can be found in Chapter 5.

3.1 PAM-4 modulation and coding scheme

Before diving into the details of design, the PAM-4 coding scheme is discussed first. Unlike like the NRZ signaling format, a PAM4 signal has four levels, each encoding two digital bits. Therefore, potentially, the symbol error rate (SER) is not equal to the bit error rate (BER). For the NRZ signaling format, let's assume the highest optical power (the "highest" symbol) represents a digital 1 and the lowest optical power (the "lowest" symbol) represents a digital 0: hence the SER equals the BER. For the PAM4 signaling format, there are now four optical power levels or symbols, each symbol representing two digital bits, therefore the BER may not be equal to the SER. Here we present two coding schemes to transfer two binary data streams into a PAM4 format. The first one is called the binary weighted scheme shown in Table 3.1, the other one is known as gray and thermometer scheme shown in Table 3.2.

For binary weighted coding, on bit stream (A) is chosen as the most signifi-

Table 3.1: Binary weighted coding scheme

A	B	$X = A \times 2$	$Y = B$	$PAM - level$
0	0	0	0	1
0	1	0	1	2
1	0	2	0	3
1	1	2	1	4

Table 3.2: Gray and thermometer coding scheme

A	B	$X = A \bigoplus B$	$Y = A$	$Z = A \bigotimes \overline{B}$	$PAM - level$
0	0	0	0	0	1
0	1	1	0	0	2
1	1	1	1	0	3
1	0	1	1	1	4

cant bit (MSB), the other bit stream (B) is the least significant bit (LSB). The weighting number of MSB is two times of LSB. Therefore, based on Table 3.1, the highest "symbol" (PAM4) represents the two bits "11"; the lowest "symbol" represents the two bits "00" (PAM1), and the two levels of "symbols" in the middle (PAM2 and PAM3) represent "10" and "01" respectively. For sufficiently low symbol error rate, only symbol errors between adjacent symbols or levels will occur. Note that if we transmit a PAM2 symbol and mistakenly receive it for a PAM3 symbol (or vice versa), a single symbol error will lead to two bit errors. So, the overall bit error rate is higher than symbol error rate.

The gray and thermometer coding shown in Table 3.2 is one solution to avoid having a single symbol error leading to multiple bit errors. In Table 3.2, if any PAM symbol is mistakenly decided as another adjacent symbol it will only lead to a single bit error, as adjacent bit strings differ in only one single bit position. Symbol errors due to non-adjacent symbols are usually negligible for the error rates considered in most communication systems (here for example better than 10^{-3}). So, the BER and SER are same for gray and thermometer coding scheme, which has been applied for this design.

3.2 Design methodology

The standard design flow is shown in Fig.3.1, which demonstrates the methodology of designing integrated circuits (IC) in CMOS technology. In this case,

the PAM4 driver IC is designed from the final output stage back to the input stage. The reason is that the load of the driver (its equivalent circuit model) is fixed (see IMEC document [20]), thus creating a logical starting point for initiating the design. In this way, the transistors of the driver stage can be sized such that they can drive the capacitive load presented by the lumped MZM. As the size of these transistors is now known, topologies and transistors for the pre-driver circuits such as the voltage doubler, level shifter and logic for the gray and thermometer coder can be selected and dimensioned. Therefore, the transistor level schematic design for each block is created. Then, each block is tested with various set of standard simulations which are the process, voltage and temperature (PVT) variations.

For next step, all blocks are connected together as the system. And the system is tested with the same set of simulation process. If the simulation results meet the requirement, then the next step is to start the layout design and extract the parasitic of interconnections (resistance and capacitance). Simulations with the parasitic extraction netlists are then executed and the circuit schematic and layout are fine-tuned to meet the requirement. The target of the bandwidth for this design is from DC to 20GHz or higher. For such high bandwidth, the inductance of metal trace for the high speed interconnections can not be ignored and should be characterized by electromagnetic (EM) simulator. In addition, parasitics of IC package need to be taken into account for the high speed signal paths. The EM simulation results for high speed interconnections (both chip-level and package-level) are connected to the rest part of the circuits for the full chip post layout simulation. The blocks which fail to meet the requirement is then redesigned again. After all the verifications are done, the chip is sent for fabrication. Since the complexity of the design process, only the final post layout simulation results are shown for each block in the following part of this chapter. By the way, it is obvious to see that the verification plays critical role to ensure that the specification is achieved during the design process.

Industrial standard design softwares were used during the design process. Cadence Virtuoso 6.1.5 was used for the IC design. Keysight Advanced Design System (ADS) was used for EM simulation. The CMOS transistor model used here is from STMicroelectronics 65nm CMOS process design kits (PDK).

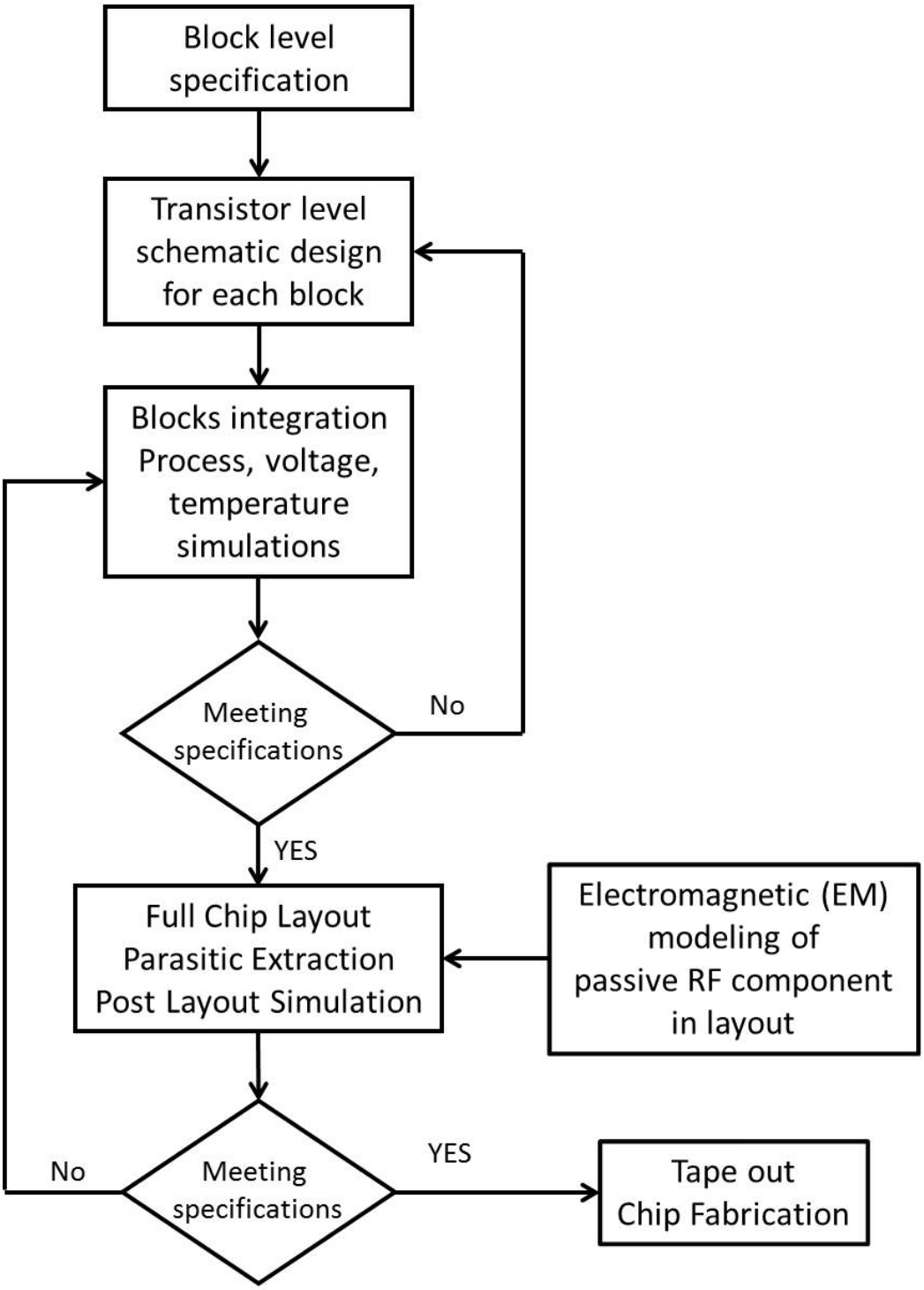


Figure 3.1: Integrated circuit design flow chart

3.3 System overview

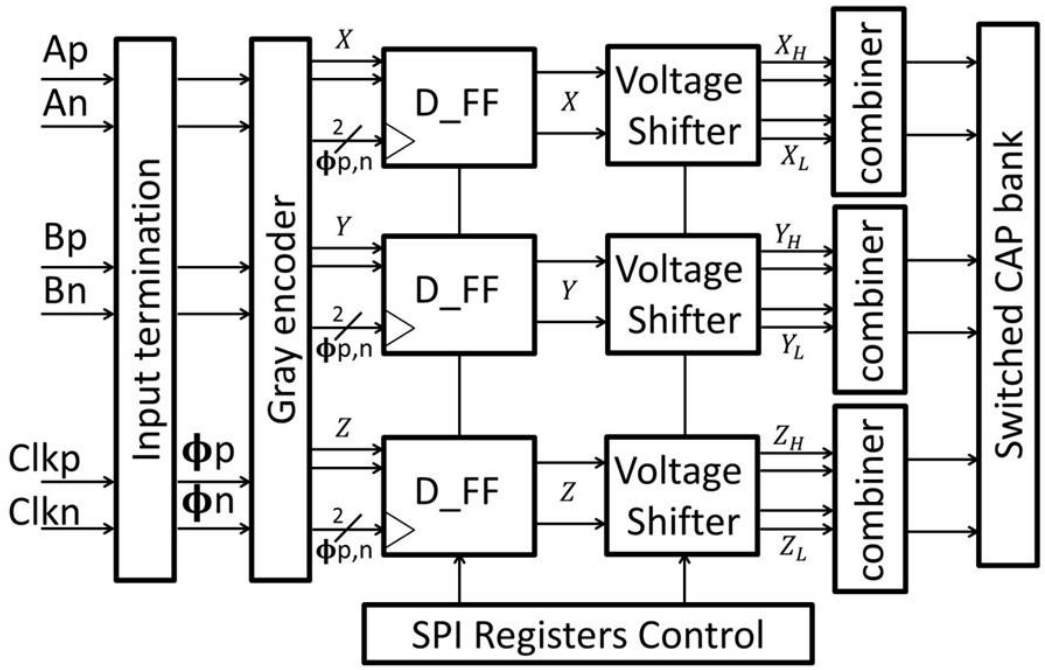


Figure 3.2: System view of PAM4 CMOS driver

Fig. 3.2 shows the block diagram of the CMOS driver: it receives two non-return to zero (NRZ) bit streams in the form of differential signals (A_p, A_n) and (B_p, B_n). An input matching network provides low return loss, after which the two bit streams are Gray and thermometer encoded using current-mode logic (CML used here to ensure the high-speed operation) gates according to the logic relations from Table 3.2. Next, a set of three CML D-flipflops (DFFs) retimes the three differential outputs of the Gray and thermometer encoder, resulting in three differential signals (X_p,X_n), (Y_p,Y_n) and (Z_p,Z_n). This eliminates delay differences in the different Gray and thermometer logic gates and the input termination network. These three differential signals are now used to drive two sets of three on-chip capacitors. In each set, the top plates are connected together to one of the electrodes of the lumped MZM, while the bottom plates are connected to (X_{D_p},Y_{D_p},Z_{D_p}) and (X_{D_n},Y_{D_n},Z_{D_n}) respectively, thus realizing a push-pull MZM drive signal. If the on-chip capacitors are sized properly (taking into account the value of the MZM electrode capacitance and capacitance from the ESD diode and bondpads), the peak-to-peak drive voltage at a single MZM electrode will be half the peak-to-peak drive voltage at the output of the chip itself. To realize a 1V swing on a single electrode, a 2V swing will be required at the bottom plates of the on-chip capacitors as explained. To achieve this in

a 65nm CMOS technology, additional level shifter and voltage doubler circuits are added between the outputs of the D-FFs and the capacitor banks, see next section for a detailed explanation. It is important to note that an MZM has a raised cosine voltage-to-optical power transfer function. To pre-compensate for this non-linearity, the on-chip capacitors are sized such that the optical output levels of the PAM-4 constellation are spaced evenly. Finally using two resistors, a DC bias voltage can be applied to each electrode. The value of these resistors was chosen to be sufficiently large that the RF signal is not affected.

3.4 Switched capacitor bank

The final output stage of the driver IC is switched capacitor bank. To understand how the switched capacitor bank is used to generate a PAM-4 signal, refer to Fig. 3.3. The three signals X, Y and Z drive three capacitors C_X, C_Y and C_Z. The capacitance C_{ARM} of the reverse biased PN junction of the silicon photonic Lumped-MZM is combined with these on-chip capacitors C_X, C_Y, and C_Z, to form the switched capacitors bank as shown in Fig.3.3. Based on the charge balance principle, the following equation (3.1) can be derived, where X, Y, and Z are digital signals derived from the two input bit streams according to Table 3.2.

$$C_X(V_X \cdot X - V_{PAM}) + C_Y(V_Y \cdot Y - V_{PAM}) + C_Z(V_Z \cdot Z - V_{PAM}) = C_{ARM} \cdot V_{PAM} \quad (3.1)$$

As a result, a PAM-4 signal is developed across C_{ARM} shown as (3.2).

$$V_{PAM} = \frac{C_X V_X \cdot X + C_Y V_Y \cdot Y + C_Z V_Z \cdot Z}{C_X + C_Y + C_Z + C_{ARM}} \quad (3.2)$$

The voltage of each PAM level is determined by the voltage swing of V_X, V_Y and V_Z, and the ratio between the on-chip capacitors (C_X, C_Y, and C_Z) and the MZM capacitance C_{ARM}. As explained in the previous chapter, a DC-bias voltage also needs to be applied via the driver to the MZM. Here this is done using a $120k\Omega$ resistor which isolates the high speed PAM signal from the DC biasing. If we assume that the values of C_X, C_Y, and C_Z is equal to $1/3C_{ARM}$ and the voltage swing of V_X, V_Y and V_Z is equal to $2 \times V_{DD}$, the output voltage is

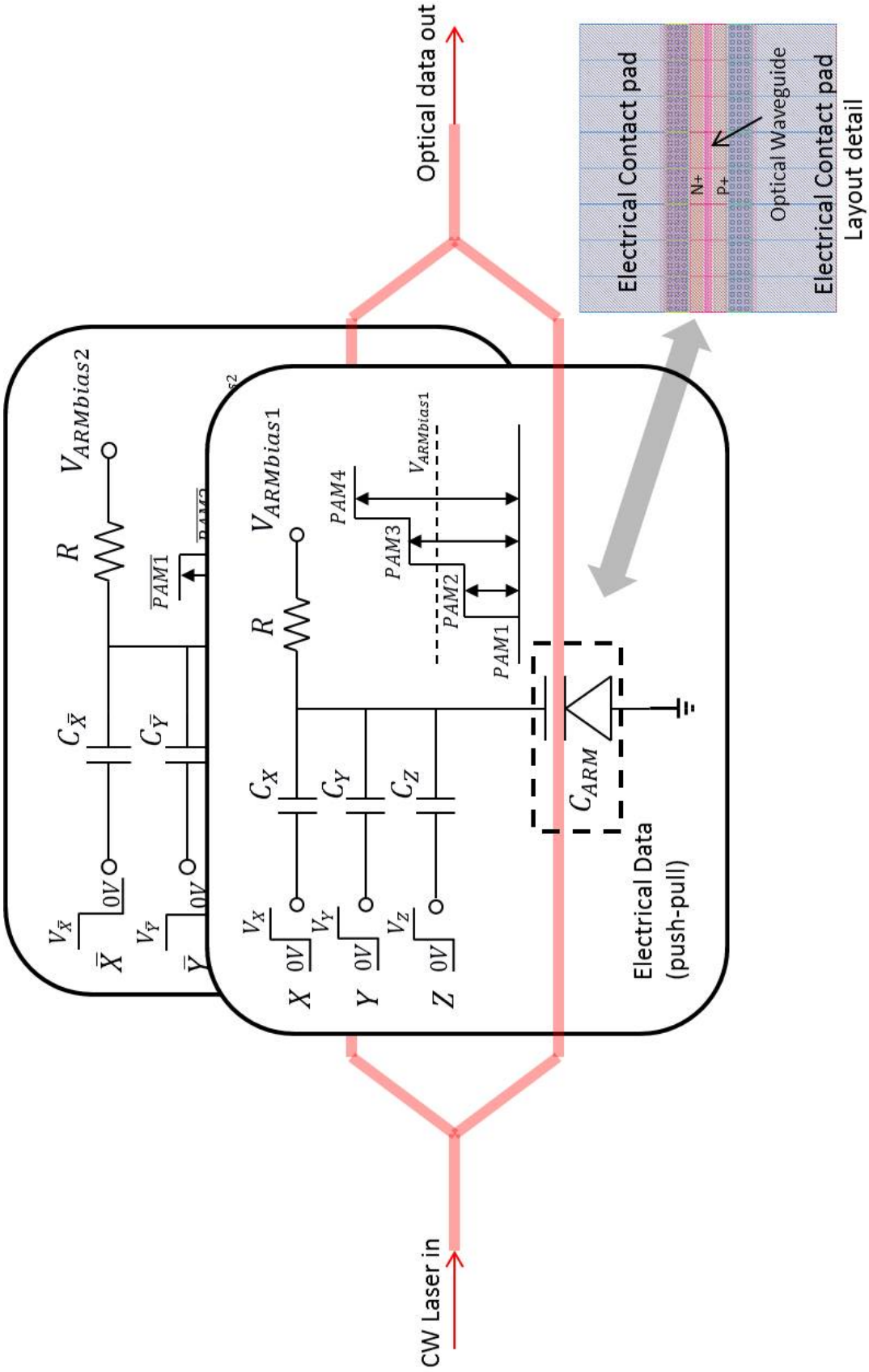


Figure 3.3: Switched capacitors' bank

Table 3.3: PAM4 output voltage

$PAM-level$	X	Y	Z	V_{PAM}
1	0	0	0	0
2	1	0	0	$0.33V_{DD}$
3	1	1	0	$0.67V_{DD}$
4	1	1	1	V_{DD}

shown in Table 3.3 based on the equation (3.3). For this design, $220fF$ metal-insulator-metal (MIM) capacitors are chosen from PDK to realize C_X, C_Y, and C_Z.

The simulation results are shown in Fig 3.4. The X, Y and Z in (3.2) are created by gray coding two 20GB/s PRBS data streams A and B according to the truth table shown in Table 3.2. The voltage swings of V_X, V_Y and V_Z are 2.4V. In Fig 3.4, the blue, black and red curves are X, Y and Z respectively. After applying a 0.5V DC bias voltage, the final PAM4 output is the pink curve in Fig. 3.4. The peak-to-peak swing is around 1V. In addition, to achieve push-pull operation, the logic inverse of X, Y and Z are applied via a second set of capacitors to the second arm of the lumped MZM.

This approach is also known as class-G switched capacitors power amplifier [30], which has been originally applied for narrow band wireless communication system but introduced into optical communication system for the first time. Due to the broadband nature of the signals, however, unlike a real Class G amplifier, no inductors can be used here. The class-G switched capacitors power amplifier can also be applied for other advanced modulation format which are more complex than PAM-4, as explained in Chapter 6.

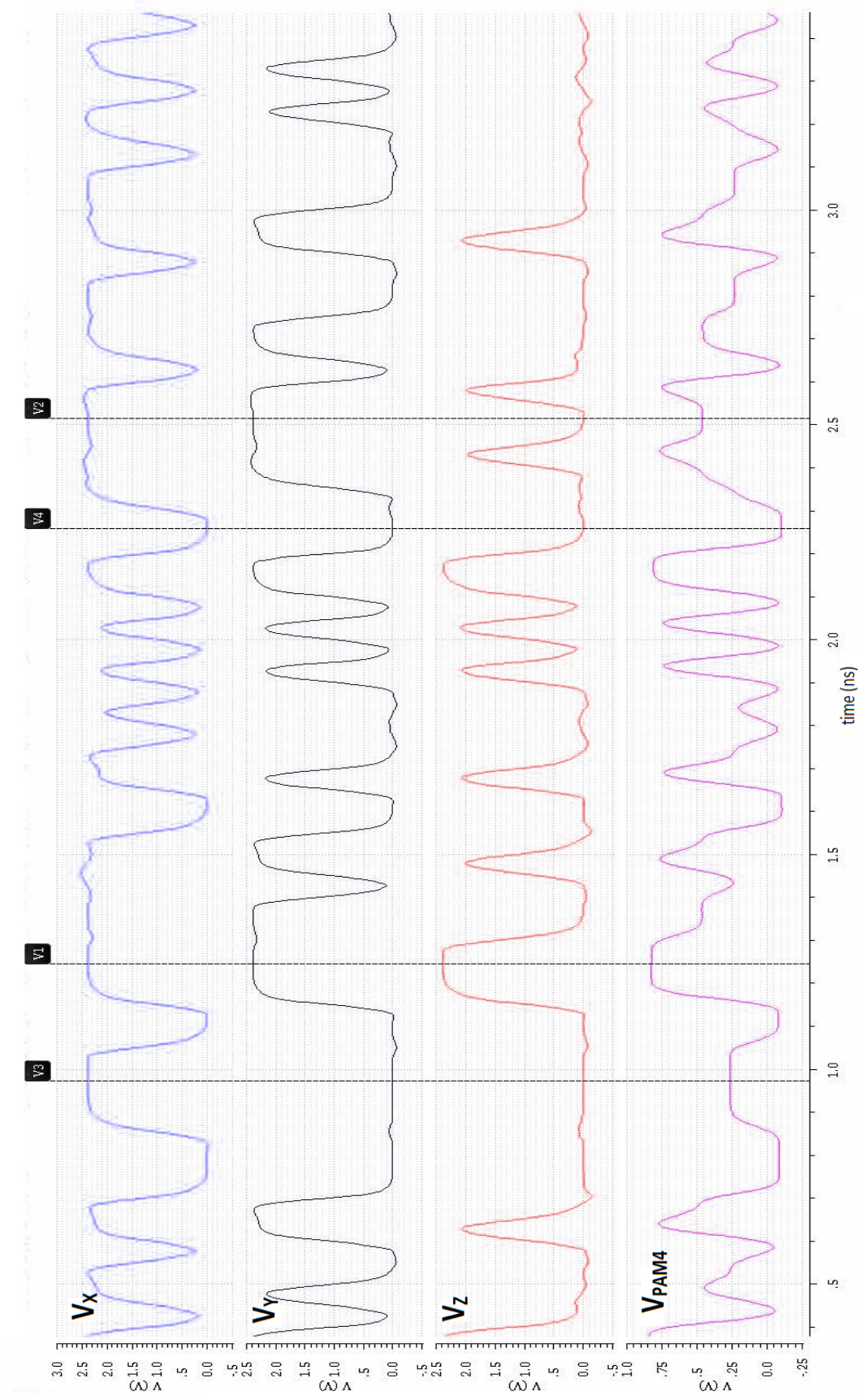


Figure 3.4: Simulation Results of the Switched Capacitors' bank

3.5 Voltage combiner

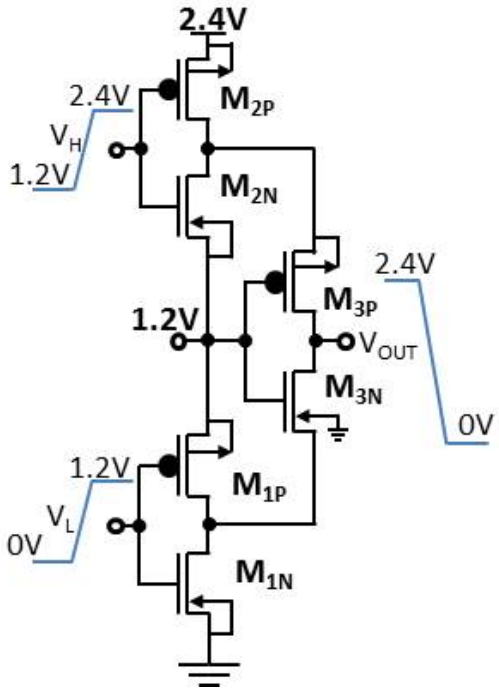


Figure 3.5: Static biased cascode voltage doubler

The voltage combiner is the stage that drives the switched capacitor bank. As mentioned above, the signal X, Y and Z should have 2.4V to drive the three on-chip capacitors. This is achieved by using the static biased cascode voltage doubler circuit [31] shown in Fig. 3.5. Note that this circuit requires two sets of full swing CMOS inputs: the first set (V_L) swings from 0V to V_{DD} (1.2V), the second set (V_H) swings from V_{DD} (1.2V) to V_{DD2} (2.4V). In Fig. 3.5, when the input signals (V_L and V_H) are 0V and 1.2V, transistors M_{1N} and M_{2N} are turned off and M_{1P} and M_{2P} are turned on. Therefore, the source voltage of M_{3N} is 1.2V and the source voltage of M_{3P} is 2.4V. The gate voltage of M_{3N} and M_{3P} are fixed to 1.2V. Hence, the voltage difference between the gate of M_{3N} and the source of M_{3N} is 0V. Transistor M_{3N} is turned off. For M_{3P}, the gate voltage is 1.2V and source voltage is 2.4V. Hence, transistor M_{3P} is turned on and the output is 2.4V. When the input signals (V_L and V_H) are 1.2V and 2.4V, transistors M_{1N} and M_{2N} are turned on and transistors M_{1P} and M_{2P} are turned off. Therefore, the source voltage of M_{3N} is 0V and the source voltage of M_{3P} is 1.2V. Since the gates of M_{3P} and M_{3N} are biased at 1.2V, transistor M_{3N} is turned on and M_{3P} is off. Hence the output voltage is 0V. In this way, the full 0V$\sim$2.4V voltage swing is realized. In addition, M_{2N} is put inside a separate

Table 3.4: Transistors' size of voltage combiner

	$M_{1N} \sim M_{3N}$	$M_{1P} \sim M_{3P}$
W	$24\mu m$	$60\mu m$
L	$65nm$	$65nm$

well (connected to $V_{DD} = 1.2V$) to prevent gate-body breakdown and minimize the body voltage effect. The size of each transistor can be found in Table (3.4). The minimum channel length of transistors has been chosen in order to achieve maximum gain. And the width of the transistor is determined by the current of charge and discharge of the capacitor banks.

The simulation results are shown as Fig. 3.6. The purple curve and gray curve are two identical gray coded PRBS data streams operating at 1.5V$\sim$2.2V and 0.25V$\sim$1.1V respectively. The red curve is the output signal swinging from $\sim$0V to $\sim$2.4V. Note that the bits have been logically inverted by the circuit, however this does not affect the operation.

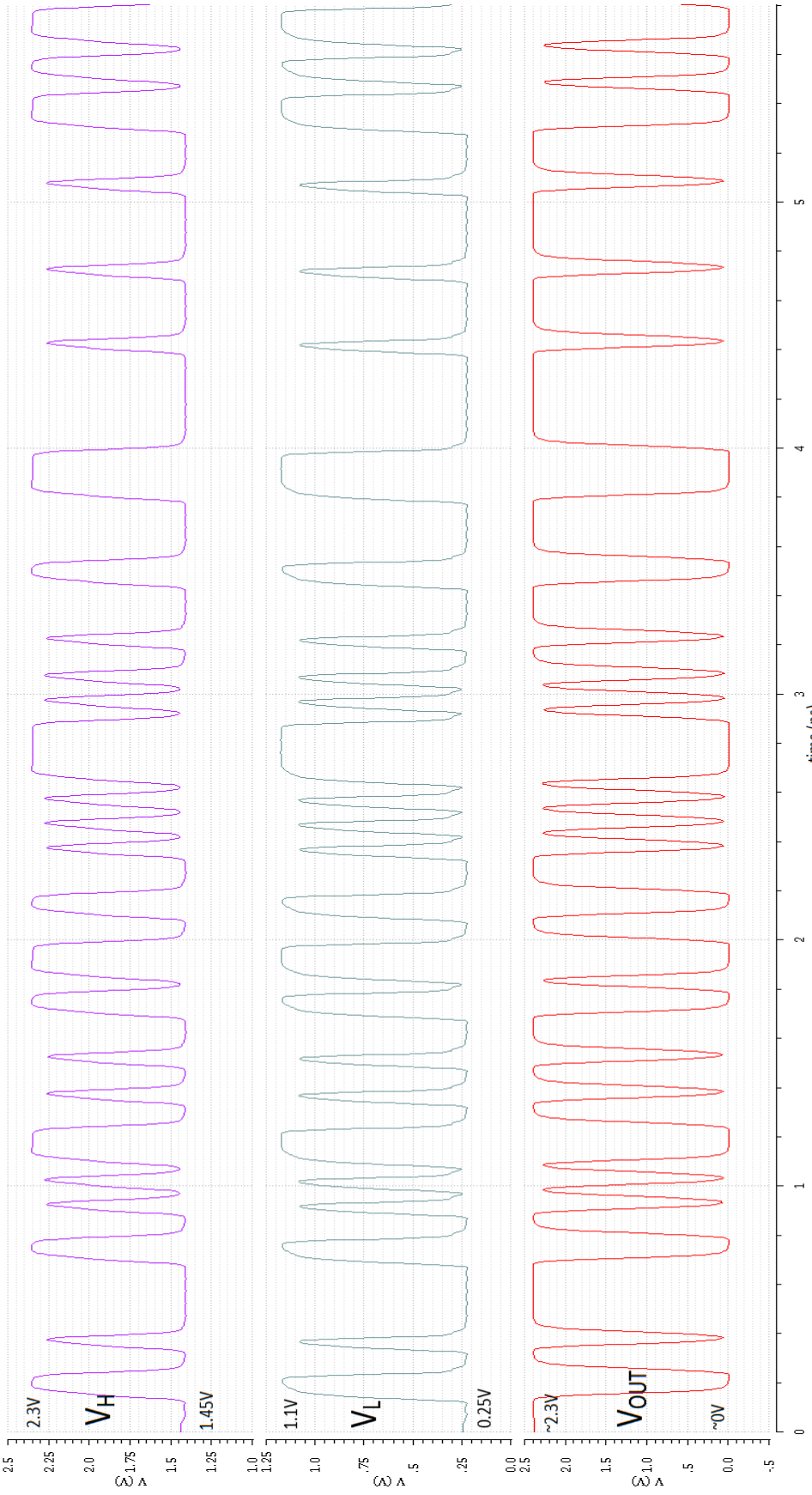


Figure 3.6: Simulation result of voltage doubler

3.6 Voltage Level Shifter

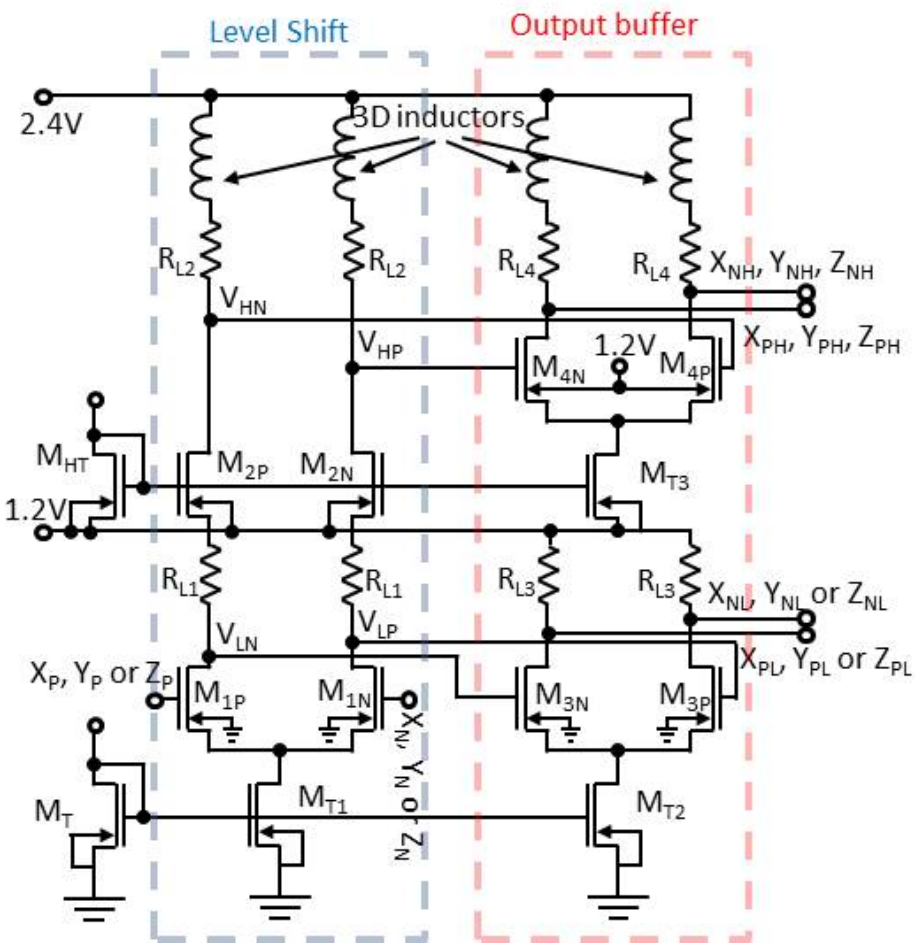


Figure 3.7: Level Shifter circuit

To drive the voltage doubler, a level shifter circuit is required between the output of the current-mode logic (CML) D-flipflops and the input of the voltage doubler circuit. This circuit is shown in Fig. 3.7 [31]:a first differential amplifier M_{1P}, M_{1N} with load resistors R_{L1} simultaneously buffers the CML D-flipflop outputs, and also steers its drain currents via common-gate devices M_{2P}, M_{2N} to a second set of load resistors R_{L2}. The input signals (X, Y, or Z) are duplicated and enhanced into V_{LP}, V_{LN} for the lower set of outputs (swinging between 0V and 1.2V) and V_{HP}, V_{HN} as the upper set of the outputs (swinging between 1.2V and 2.4V). Both signals are then connected to a output buffer stage, a stacked set of differential amplifiers M_{3P}, M_{3N} and M_{4P}, M_{4N}, to provide sufficient drive power for the next stage. To ensure sufficiently fast transition times, 3D inductors were used, which will be discussed later. All the transistors in the signal path have minimum length to maximize speed. To prevent transistors'

Table 3.5: Components' value of voltage level shifter

	M_{1P}, M_{1N}	M_{2P}, M_{2N}	M_{3P}, M_{3N}	M_{3P}, M_{3N}	
W	$16\mu m$	$16\mu m$	$36\mu m$	$36\mu m$	
L	$65nm$	$65nm$	$65nm$	$65nm$	
	M_T	M_{T1}	M_{T2}	M_{HT}	M_{T3}
W	$3\mu m$	$30 \times 3\mu m$	$60 \times 3\mu m$	$4\mu m$	$20 \times 4\mu m$
L	$65nm$	$65nm$	$65nm$	$65nm$	$65nm$
	R_{L1}	R_{L2}	R_{L3}	R_{L4}	$3D - inductor$
	180Ω	160Ω	92Ω	92Ω	$910pH$

gate-to-body break down, M_{2P}, M_{2N} and M_{4P}, M_{4N} are placed in a separate well biased at 1.2V. The details of each transistor, resistor, and 3D inductor can be found in Table (3.5). Since M_{4P} and M_{4N} are connected with 3D inductor, the differential pair can achieve surficient bandwidth with small biasing current. Therefore, the transistor's size of M_{T3} is smaller than M_{T2}.

The simulation results are shown in Fig.3.8. The differential PRBS data synchronized by the previous D flipflop stage are plotted as the green and blue curves, and are the inputs for the voltage level shifter. The voltage swing of the inputs is from 0.3V to 1V. The "upper" outputs are plotted as brown and red curves with 1.3V$\sim$2.2V swing, and the blue and pink curves are the "lower" outputs with 0.25V$\sim$1V swing. The main reason for not having a rail-to-rail voltage swing (from 0V to1V) is that all transistors in Fig. 3.7 must be operated at saturation region in order to maximize the switching speed. Therefore, the voltage level of "0" should be above V_{SAT}. The level shifter duplicates the input data into two sets of the differential outputs successfully. From the simulation results, it can also be seen that transient noise due to crosstalk from the clock in the previous D flipflops have been suppressed.

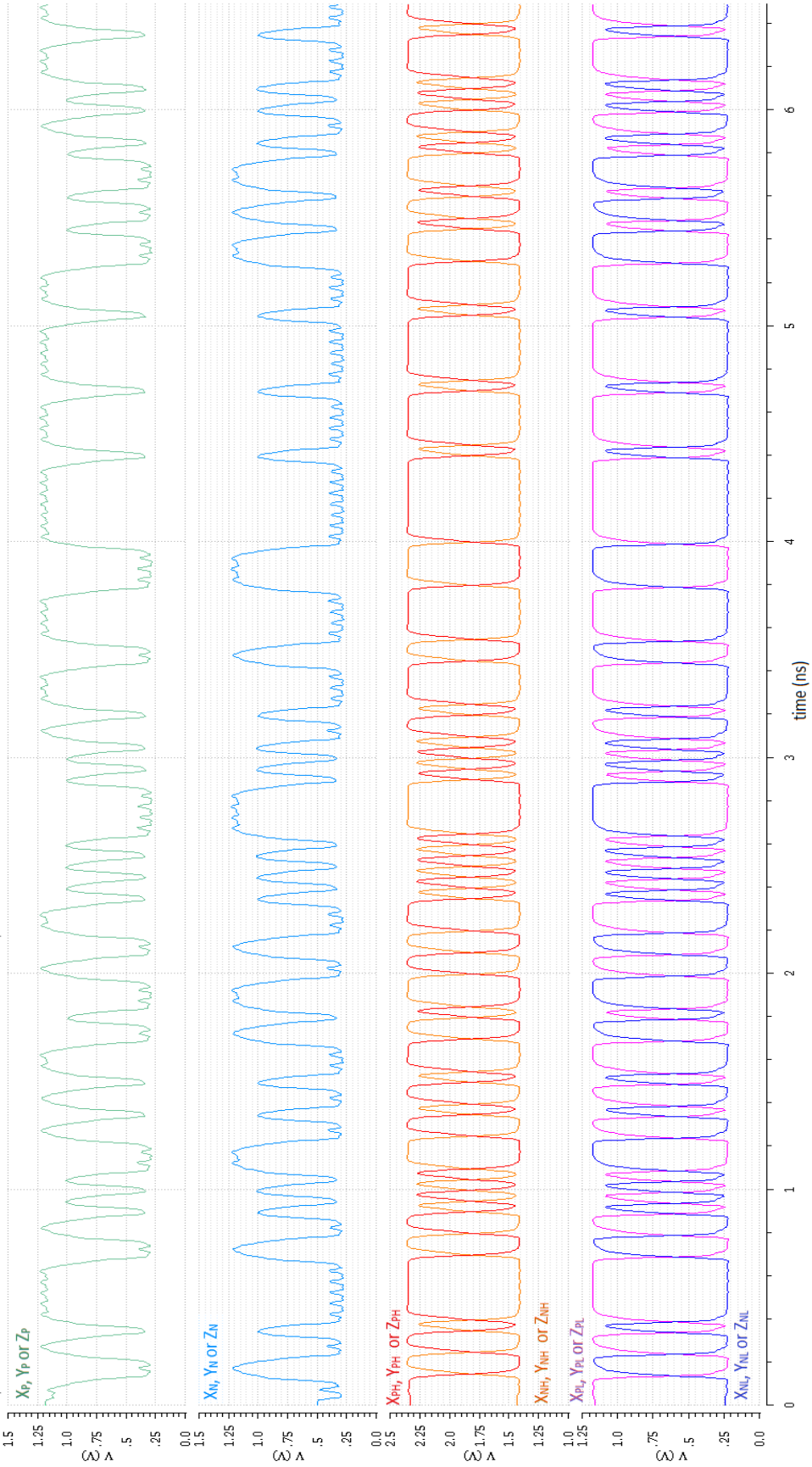


Figure 3.8: Simulation results of the level shifter

3.7 CML high speed D flip-flop

Before sending the gray coding data streams into voltage level shifter, the D flipflop is required for synchronization. The D flipflop is constructed from two CML latches (master slave latches) connected in cascade as shown in Fig. 3.9 [32]. For the first latch, the positive and negative phase clock signals are connected to M_{C1P} and M_{C1N} respectively. For the second latch, the logical connection for the positive and negative clock phases is inverted compared to the first latch, and they are connected to M_{C2N} and M_{C2P} respectively. This facilitates the master slave operation. The transistors M_{C1P}, M_{C1N}, M_{C2P}, and M_{C2N} are biased in class-A mode with minimum channel length in order to have maximum f_T. The data signals control another set of differential pairs formed by transistors M_{1P}, M_{1N} (first latch), and M_{3P}, M_{3N} (second latch): these transistors are biased in class-AB push-pull mode and act as switches in Fig.3.9. The cross-coupled pairs M_{2P}, M_{2N} and M_{4P}, M_{4N} latches and enlarges the output voltage swing from each input stage of the first and second latches using positive feedback. The channel width of cross pairs is three times wider than the input differential pairs, which enhances the drive power of the latch. To ensure sufficiently fast transition times, 3D inductors are used as well.

The D flipflop circuit operates as follows. When the positive clock goes high, transistors M_{C1P}, M_{C2N} are turned on, and transistors M_{C1N}, M_{C2P} are turned off. Hence, the input differential pair (M_{1P} and M_{1N}) of the first latch reads the data of current state. When the positive clock goes low, transistors M_{C1P}, M_{C2N} are turned off, and M_{C1N}, M_{C2P} are turned on. In this way, the cross-coupled pairs (M_{2P} and M_{2N}) store the data read by the input differential pair (M_{1P} and M_{1N}) and deliver it to the input (M_{3P} and M_{3N}) of the second latch. Since M_{C1P} is off, transistors M_{1P} and M_{1N} are also cut off and non-active. Whatever changes occur on the input data at this moment, can not change the data stored by cross-coupled pairs (M_{2P} and M_{2N}). Next, when the positive clock goes high again, the cross-coupled pairs of the second latch (M_{4N} and M_{4P}) load the data from M_{2P}, M_{2N}, M_{3P} and M_{3N} and deliver it as the final output. Meanwhile, the input of the first latch (M_{1P} and M_{1N}) read the data of the next state since M_{C1P} has turned on again. The details of each transistor, resistor, and 3D inductor can be found in Table (3.6).

The simulation results are shown in Fig.3.10. The voltage swing of differential input data is from 0.4V to 1.2V shown as the blue and green curves. The clock

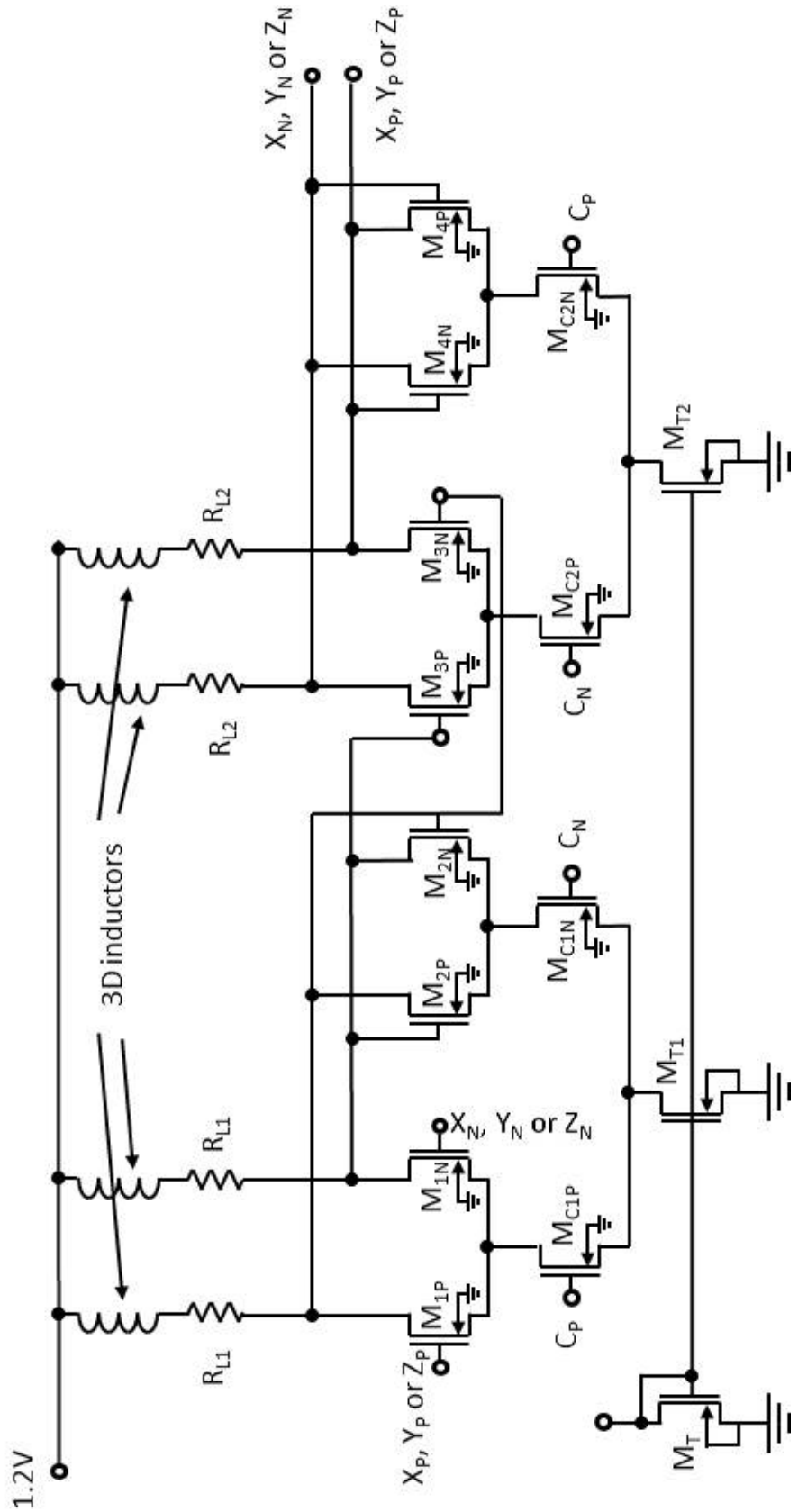


Figure 3.9: D flipflop circuit

Table 3.6: Components' value of D flip-flop

	M_{1P}, M_{1N}	M_{2P}, M_{2N}	M_{3P}, M_{3N}	M_{4P}, M_{4N}
W	$3\mu m$	$10\mu m$	$3\mu m$	$10\mu m$
L	$65nm$	$65nm$	$65nm$	$65nm$
	M_{C1P}, M_{C1N}	M_{C2P}, M_{C2N}	M_T	M_{T1}, M_{T2}
W	$10\mu m$	$10\mu m$	$3\mu m$	$24 \times 3\mu m$
L	$65nm$	$65nm$	$65nm$	$65nm$
	R_{L1}	R_{L2}	$3D - inductor$	
	250Ω	250Ω	$910pH$	

signal is a 20GHz sinusoidal signal swinging between 0.5V and 0.95V shown as the red curve in Fig.3.10. The output signals are plotted as the brown and blue curves. In order to sample the data correctly, there is a time delay between the clock signal and input data, avoiding setup and hold violations. Note how the output signal of the D flipflop has one clock cycle delay compared to the input data (marker: V1, V2 and V3, V4 in Fig.3.10). Note that there is a periodic transient ripple appearing in the output signal. Since the CML latch topology is close to the classic active mixer circuitry, the clock signal has been mixed into the data signal.

From a system perspective, the reason for using the D flipflops is to synchronize the (X_p, X_n), (Y_p, Y_n) and (Z_p, Z_n) signals generated by previous gray coding stage. From Table 3.2, the gray coding includes an OR gate, an AND gate, and a Buffer gate, each implemented using current-mode logic gates. The propagation delay of each gate is different. After overlapping the eye diagrams of X_p, X_n, Y_p, Y_n and Z_p, Z_n in Fig. 3.11 (a), the eye is heavily closed and the overall deterministic jitter is around 20ps. By introducing the D flipflops to synchronize X_p, X_n, Y_p, Y_n and Z_p, Z_n, the overlapped eye diagram is shown as Fig. 3.11 (b), where the eye is fully open and the overall jitter has been reduced to around 5ps. The D flipflops not only help to synchronize the data but also help to eliminate errors introduced by the gray coding circuits, which is discussed in the following.

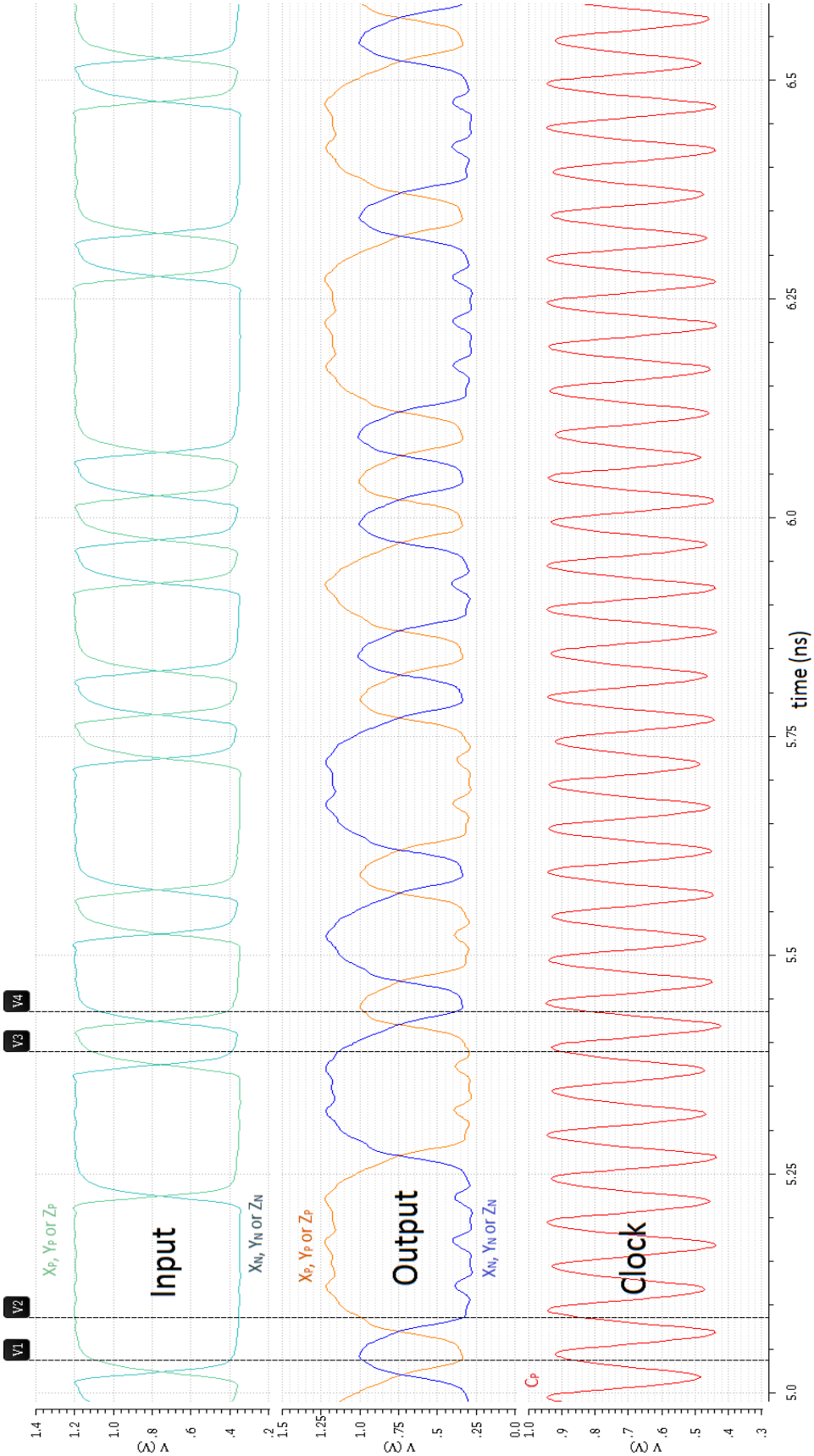


Figure 3.10: Simulation result of D flipflop

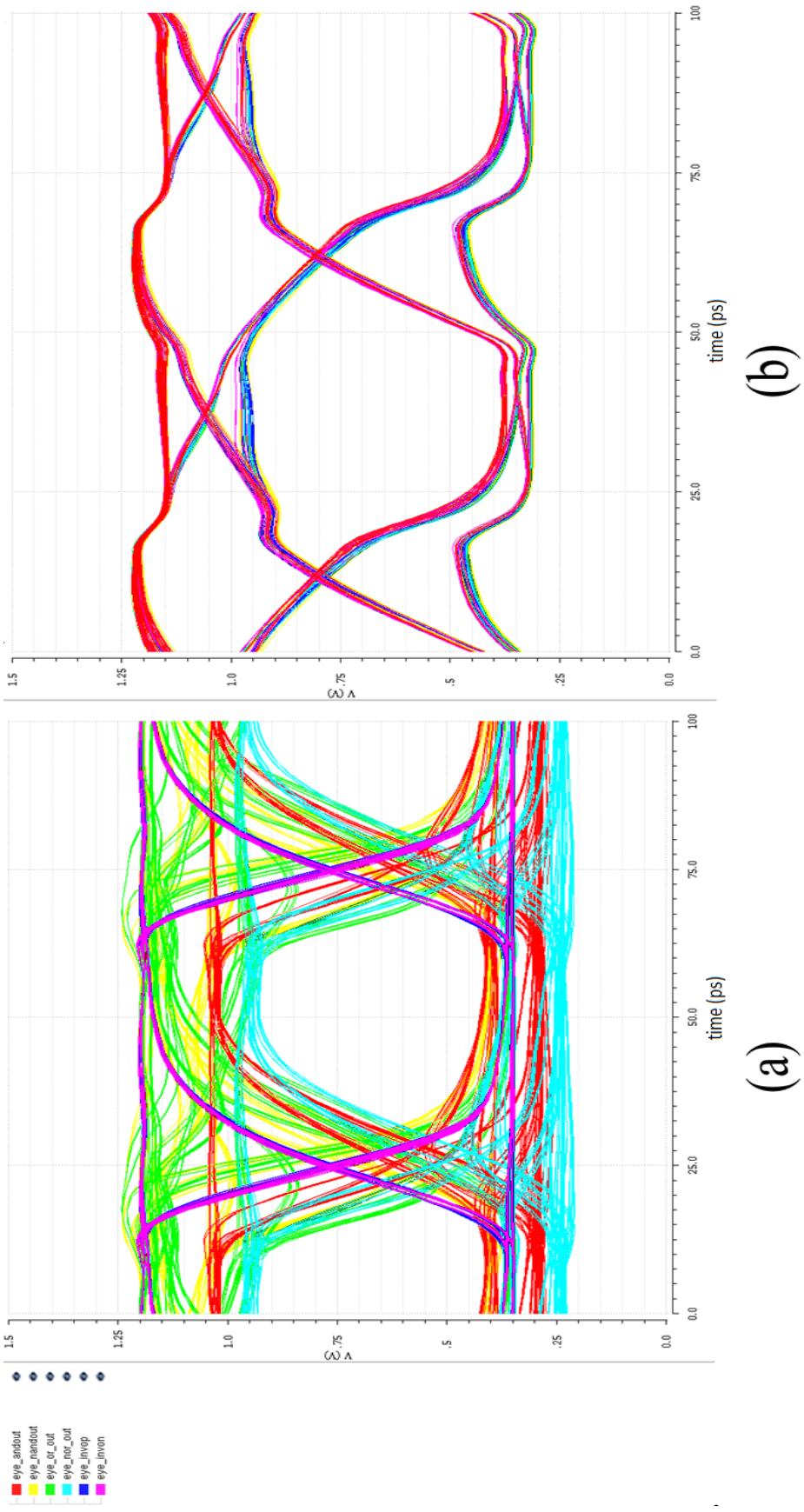


Figure 3.11: Synchronization (a) before the D flipflop and (b) after the D flipflop

3.8 Gray and thermometer coding

The input stage is gray and thermometer coding circuit. As mentioned previously, the X, Y, and Z signals (see Fig. 3.3) are generated by a Gray coding circuit, implemented according to Table 3.2. The Gray coding circuitry includes an AND, OR, and buffer (inverter) gate. Fig. 3.12 shows the schematics of the CML logic gates for an AND, OR, and Buffer function respectively [33]. The topology of the AND and OR gates are similar except the connection of inputs; the Buffer is a simple differential pair. For the AND and OR gates in Fig. 3.12 (a) (b), the transistors M_{1P}, M_{2P}, and M_3 are biased in class-A mode. The operating region of M_{1N} and M_{2N} depends on the input of the M_3. If M_3 is turned on, the tail bias current flows through M_3 and the drain voltage of the M_3 would be very low, therefore the M_{1N} and M_{2N} are operated in the triode region. If M_3 is turned off, the current flowing through M_3 is zero and the drain voltage of M_3 depends on transistors M_{1N} and M_{2N}. In this case, transistors M_{1N} and M_{2N} are biased also in class-A mode. From an analog perspective, the outputs of Fig. 3.12 (a) (b) are not truly differential signals due to the asymmetrical topology of the circuits. However, from a logical perspective, the outputs are differential. For the Buffer gate in Fig. 3.12 (c), M_{1P} and M_{1N} are biased in class-AB mode. The details of each transistor and resistor can be found in Table (3.7). The inverter stage only has 2 transistors in stack comparing to the and gate and or gate (3 transistors in stack). Therefore, the channel length of the tail transistors (M_{T2} and M_{T3}) in inverter stage has increased in order to achieve same output swing as other logic gates.

The simulation results are shown in Fig.3.13. The 20Gb/s differential PRBS input data stream A has been plotted as the first and second waveforms from the top, and the 20Gb/s differential PRBS input data stream B has been plotted as the third and fourth waveform from the plot. The voltage swing of differential input A is from 0.3V to 0.9V and the swing of differential input B is from 0.5V to 1.1V. The outputs of Buffer, OR, and AND gates are shown as the traces below that. For the Buffer gate, it is a standard differential pair with output voltage swing from $\sim$0.4V to $\sim$1.1V. For the OR and AND gates, the circuit states according to their respective inputs, transistors operating region, and outputs are listed in Table 3.8. For example, for the OR gate, when $A = 0.3V$, $\overline{A} = 0.9V$, $B = 0.5V$, and $\overline{B} = 1.1V$, transistors M_{1P}, M_{1N}, and M_{2P} are turned on and M_{2N} and M_3 are turned off (see Fig. 3.12(b)). Since M_{1P} and M_{2P} are turned on, the output nodes X are connected to the virtual ground and the

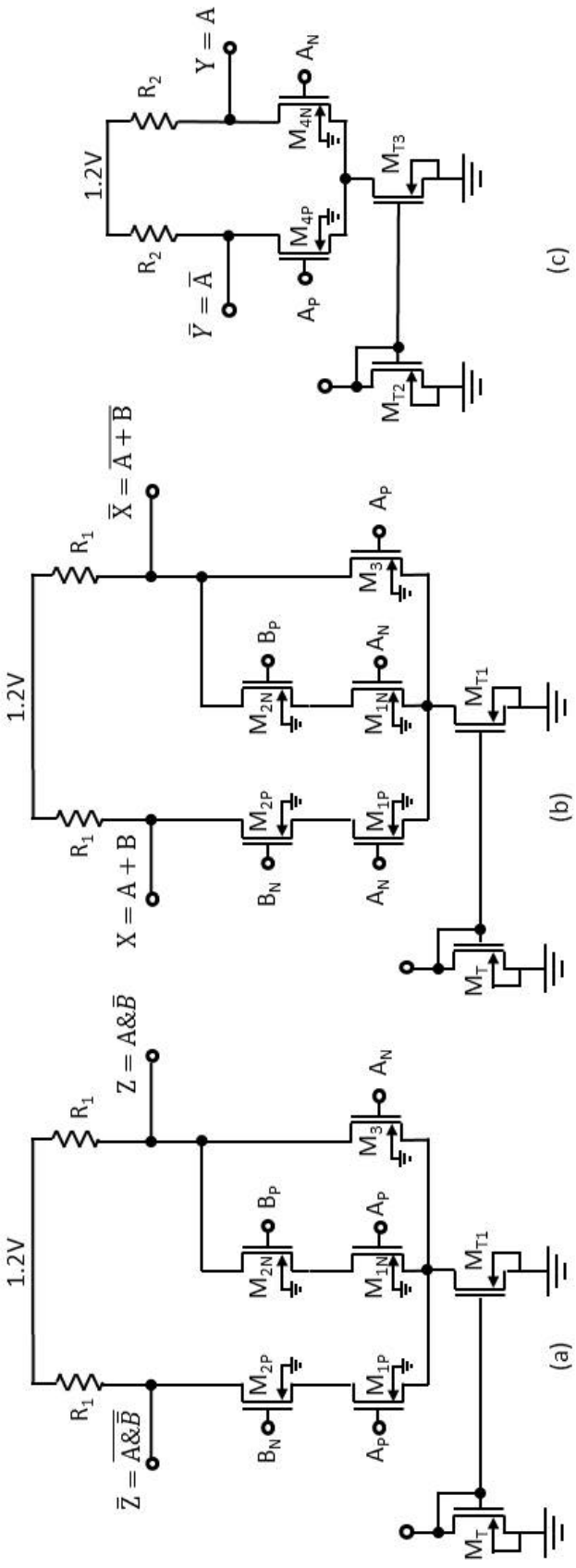


Figure 3.12: Gray coding (a) and gate (b) or gate and (c) inverter

Table 3.7: Components' value of gray coding logic gates

	M_{1P}, M_{1N}	M_{2P}, M_{2N}	M_3	M_{4P}, M_{4N}
W	$40\mu m$	$24\mu m$	$40\mu m$	$20\mu m$
L	$65nm$	$65nm$	$65nm$	$65nm$
	M_T	M_{T1}	M_{T2}	M_{T3}
W	$2\mu m$	$16 \times 2\mu m$	$3\mu m$	$8 \times 3\mu m$
L	$65nm$	$65nm$	$80nm$	$80nm$
	R_{L1}	R_{L2}		
	248Ω	327Ω		

Table 3.8: Transistors' operation states of OR, AND

OR					AND				
A	0.3V	0.3V	0.9V	0.9V	A	0.3V	0.3V	0.9V	0.9V
B	0.5V	1.1V	1.1V	0.5V	B	0.5V	1.1V	1.1V	0.5V
$\overline{A}$	0.9V	0.9V	0.3V	0.3V	$\overline{A}$	0.9V	0.9V	0.3V	0.3V
$\overline{B}$	1.1V	0.5V	0.5V	1.1V	$\overline{B}$	1.1V	0.5V	0.5V	1.1V
M_{1P}	ON	ON	OFF	OFF	M_{1P}	OFF	OFF	ON	ON
M_{1N}	ON	ON	OFF	OFF	M_{1N}	OFF	OFF	ON	ON
M_{2P}	ON	OFF	OFF	ON	M_{2P}	ON	OFF	OFF	ON
M_{2N}	OFF	ON	ON	OFF	M_{2N}	OFF	ON	ON	OFF
M_3	OFF	OFF	ON	ON	M_3	ON	ON	OFF	OFF
X $(A \bigoplus B)$	0.4V	1.1V	1.1V	1.1V	Z $(A \bigotimes \overline{B})$	0.4V	0.4V	0.4V	1.1V
$\overline{X}$ $(\overline{A \bigoplus B})$	1.1V	0.4V	0.4V	0.4V	$\overline{Z}$ $(\overline{A \bigotimes \overline{B}})$	1.1V	1.1V	1.1V	0.4V

output voltage is ∼0.4V. In addition, M_3 and M_{2N} are turned off, so the current for both paths are off. Therefore, the voltage of node $\overline{X}$ in Fig. 3.12 (b) is close to the supply voltage, ∼1.1V in this case.

One point to note is that in the output waveforms of the OR and AND gates (see Fig. 3.13), there are several "sharp" glitches in the output node $X = A \bigoplus B$ for the OR gate and $\overline{Z} = \overline{A \bigotimes \overline{B}}$ for the AND gate. The main reason for these glitches drops is the transistors M_{1P} and M_{2P} in Fig. 3.12 (a) (b) have been turned on simultaneously during the data transitions. These glitches can be eliminated by using successive retiming flipflops. As an example, consider the output node $X = A \bigoplus B$ of the OR gate, see Fig.3.14. The glitches can be observed when the input signal A (blue curve) switches from 0.3V to 0.9V and the input signal B (green) switches from 1.1V to 0.5V. Considering the circuit in Fig. 3.12 (b), transistors M_{1P} switches from its ON state to its cut-off state and transistor M_{2P} switches from its cut-off state to an ON state. During this

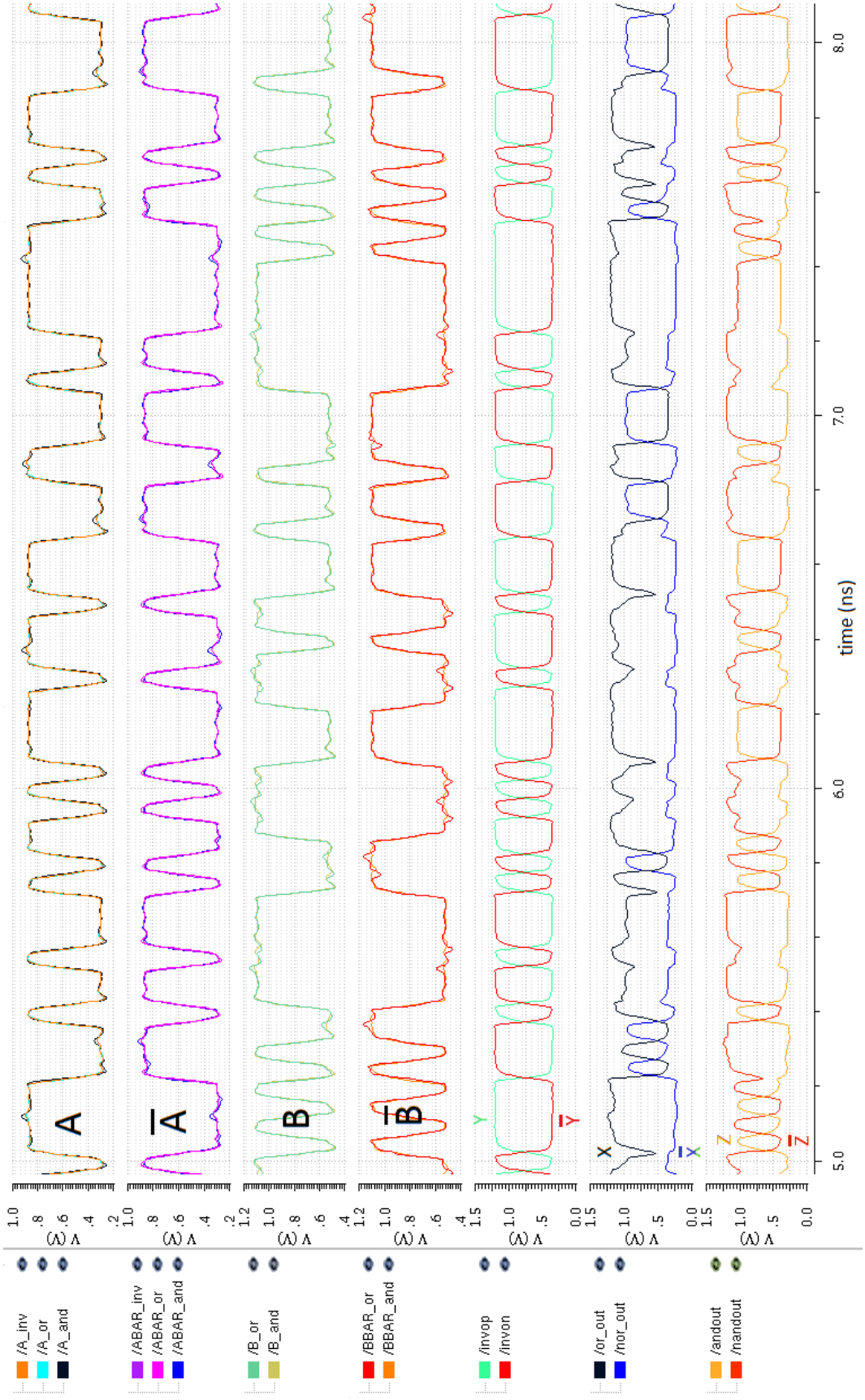


Figure 3.13: Simulation results of AND gate, OR gate, and Inverter

transition, there is a moment in the time where both M_{1P} and M_{2P} are turned on, effectively shorting the drain voltage of M_{2P} (node X) and lowering it dramatically (white curve in Fig. 3.14). When the data transition has finished, transistor M_{1P} is turned off and no current flows through this path anymore, bringing the voltage of node X back to 1.1V. This also explains the voltage drop of node $\overline{Z} = \overline{A \otimes \overline{B}}$ in the AND gate during some data transitions. To eliminate glitches, a D flipflop can be used. By aligning the clock signals to the moments that the logic gate outputs are stable, the D flipflop would only sample the data when transitions are finished. For example, the plots of X and $\overline{X}$ (blue and yellow curve at the bottom of Fig. 3.14) are the outputs of the D flipflop connected to the OR gate. Comparing to the direct output of OR gate, the glitches have been eliminated successfully. For the AND gate, the same technique has been applied to eliminate the glitches. In Fig.3.11 (b), the outputs' eye diagram AND, OR, and Buffer are overlapped without any voltage drop error.

As a final point, the glitch problem has only been observed on node $X = A \oplus B$ for the OR gate and $\overline{Z} = \overline{A \otimes \overline{B}}$ for the AND gate. For node $\overline{X} = \overline{A \oplus B}$ in the OR gate and $Z = A \otimes \overline{B}$ in the AND gate, there are no such glitches during any input data transitions. The reason for this is that transistor M_3 dominates the voltage of these nodes, and the input data of M_3 are always reversed compared to the input data of M_{1N} in Fig. 3.12 (a) (b). So, whenever transistor M_{1N} switches from ON to OFF and M_{2N} switches from OFF to ON (or transistor M_{1N} switches from OFF to ON and transistor M_{2N} switches from ON to OFF) the drain voltage of M_3 locks the node voltage during the data transition, as $V_{DS(M_3)} < V_{DS(M_{1N})} + V_{DS(M_{2N})}$. In addition, when transistor M_{1N} switches from ON to OFF and M_{2N} switches from OFF to ON, transistor M_3 switches from OFF to ON, the nodes of $\overline{X} = \overline{A \oplus B}$ and $Z = A \otimes \overline{B}$ can only be pulled down and can not swing to high voltage level, even if transistor M_{1N} is OFF at the end of the transition. Hence no glitches will occur in this case.

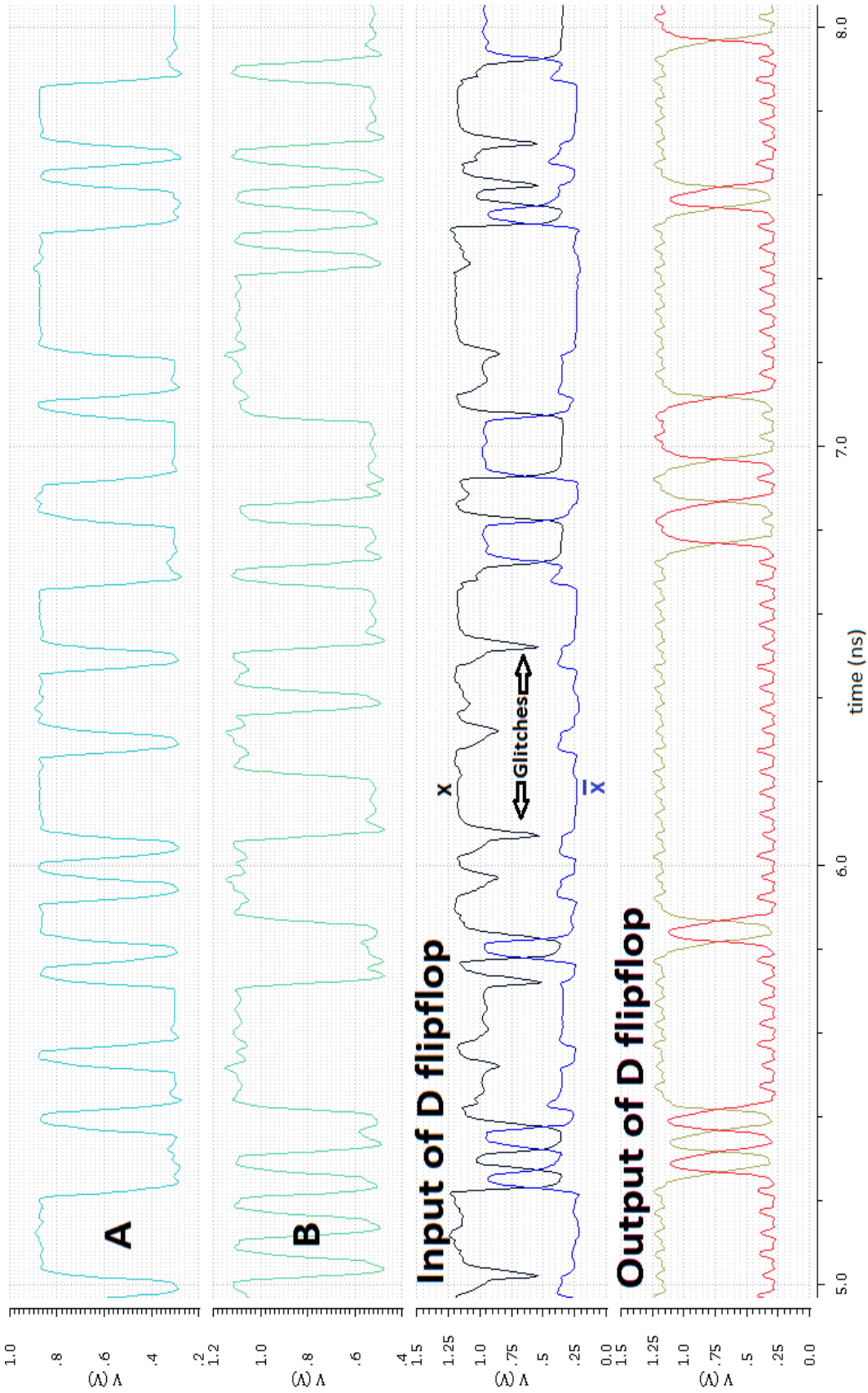


Figure 3.14: Elimination of glitches by D flipflop

3.9 3D Inductors

To increase the transition speed (and hence maximum achievable bitrate), peaking inductors have been used in the level shifter (section 3.6) and D flipflops (section 3.7). The main function of these inductors is to increase the shunt impedance at the drains of the transistors in the high frequency range. By doing so, the gain of the level shifter and D flipflop are enhanced in the high frequency range [34]. Unlike traditional inductors used in VCOs, the Q factor of such peaking inductors does not need to be high (>10). Indeed as shown the peaking inductors are normally connected in series with the load resistors, hence the "loaded" Q of the inductor would be low anyhow due to these load resistors [34]. More critical thing is the area used by these inductors.

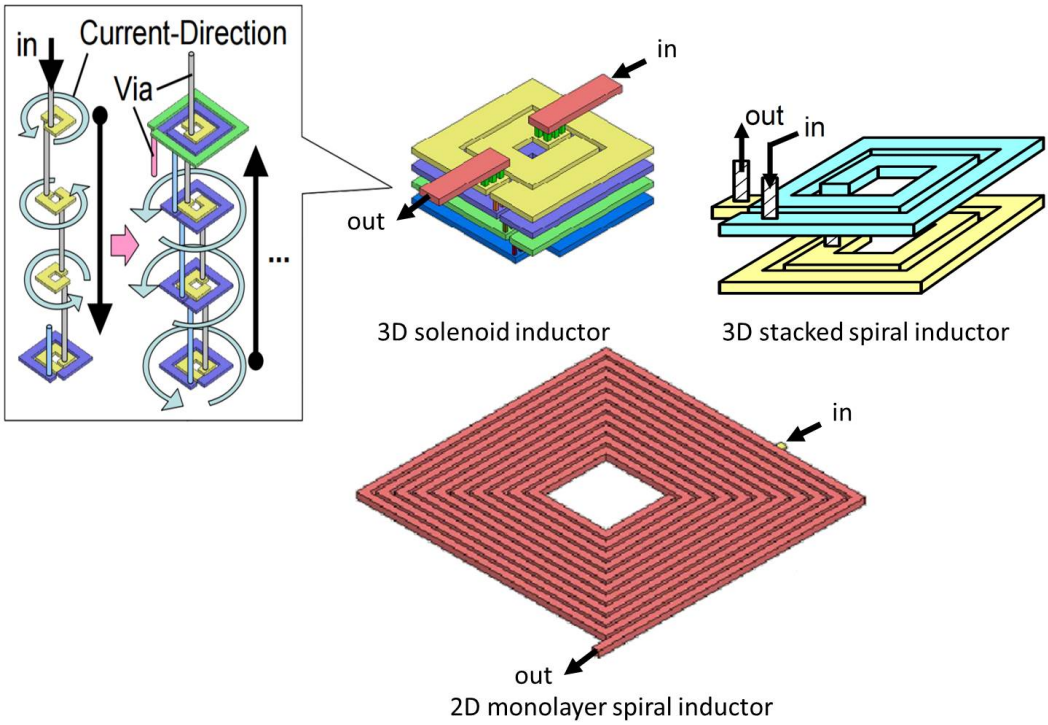


Figure 3.15: Metal trace winding of 3D solenoid inductor, 3D steaked spiral inductor, and 2D monolayer spiral inductor

There are three types of the winding schemes of peaking inductors, demostrated in Fig. 3.15 [35]. The area of 3-dimensional (3D) solenoid inductor and 3D spiral inductor are 80% smaller compared to a conventional 2D monolayer spiral inductor. Compared to a 3D stacked spiral inductor, the parasitic capacitance of 3D solenoid inductor is reduced by 30%; operating frequencies from DC up to 40GHz have been reported for such inductors [35]. For the PAM4 driver,

the operation frequency is from DC to 20GHz, which is much smaller than the bandwidth of 3D solenoid inductor (DC-40GHz). Therefore, I used a 3D steaked spiral inductor (named as 3D inductor in following part of the thesis).

To design the 3D inductors, several challenges need to be addressed. Firstly, the metal stack of advanced CMOS technologies such as the 65nm technology used in this design is highly complicated: for example it includes no less than seven metal layers. Additionally, the dielectric between two successive metal layers is not a single dielectric layer. Indeed, there are typically two or three dielectric layers between two metal layers, each with its specific dielectric properties. Such structures are difficult to handle by the EM (electromagnetic) solvers, which are heavily used during the design process of the 3D inductors. EM simulations with a complex substrate and metal stack requires high computing power, large memory and disk space. The simulation time increases exponentially with the number of layers in the metal stack. In order to increase the performance and speed of the EM simulator, simplification of metal stack definition in the design software is necessary.

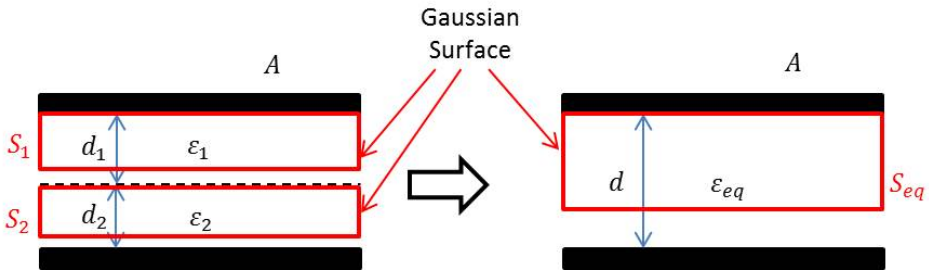


Figure 3.16: Equivalent dielectric constant

The simplification of two dielectric layers within two metal layers is demonstrated in Fig.3.16 as an example. In Fig. 3.16 left, the area of the two metal layers is A and the thicknesses of the dielectric layer with relative permittivity of ε_1 and the dielectric layer with relative permittivity of ε_2 are d_1 and d_2 respectively. Gaussian Surfaces have been selected along the edge of the top surface of the dielectrics shown as S_1, S_2 and S_{eq}in Fig. 3.16. Using Gauss's Law, following expressions can be derived [36]:

$$\oint_{S_1} E_1 ds = A \cdot \frac{V_1}{d_1} = \frac{Q}{\varepsilon_1} \tag{3.3}$$

$$\oint_{S_2} E_2 ds = A \cdot \frac{V_2}{d_2} = \frac{Q}{\varepsilon_2} \tag{3.4}$$

where E_1 is electrical field in dielectric layer ε_1; d_1 is the thickness of dielectric layer ε_1 ; V_1 is the potential difference between the top surface and bottom surface of dielectric layer ε_1; and Q is the total charge at the top surface of S_1. In formula (3.4), E_2 is electrical field in dielectric layer ε_2; d_2 is the thickness of dielectric layer ε_2 ; V_2 is potential difference between the top surface and bottom surface of dielectric layer ε_2; and Q is the total charge at the top surface of S_2. The total charge within S_1 and S_2 are the same based on the charge balance rule and the total voltage drop between two metal layers is $V_1 + V_2$. Hence, we can derive the equation for the right part of Fig. 3.16 as following:

$$\oint_{S_{eq}} E_{eq} ds = A \cdot \frac{V_1 + V_2}{d} = \frac{Q}{\varepsilon_{eq}} \tag{3.5}$$

where E_{eq} is electrical field in the equivalent dielectric layer ε_{eq}; $V_1 + V_2$ is the total potential difference between the top and bottom of the equivalent dielectric layer ε_{eq}; and Q is the total charge at the top surface of S_{eq}. Based on the charge balance rule, the total charge Q is equal to the charge within S_1 which is also same as the charge within S_2. Using (3.3) and (3.4), the following equation can then be derived:

$$V_1 = \frac{d_1 Q}{A\varepsilon_1} \tag{3.6}$$

$$V_2 = \frac{d_2 Q}{A\varepsilon_2} \tag{3.7}$$

Plugging (3.6) and (3.7) into equation (3.5), the following formula can be derived:

$$A \cdot \frac{\frac{d_1 Q}{A\varepsilon_1} + \frac{d_2 Q}{A\varepsilon_2}}{d} = \frac{Q}{\varepsilon_{eq}} \tag{3.8}$$

$$\frac{\frac{d_1}{\varepsilon_1} + \frac{d_2}{\varepsilon_2}}{d} = \frac{1}{\varepsilon_{eq}} \tag{3.9}$$

$$\frac{d_1}{\varepsilon_1} + \frac{d_2}{\varepsilon_2} = \frac{d}{\varepsilon_{eq}} \tag{3.10}$$

where d is the thickness of equivalent dielectric layer ε_{eq} and $d = d_1 + d_2$.

Appling same principle, the equivalent Relative Permittivity of three dielectric layers is following:

$$\frac{d_1}{\varepsilon_1} + \frac{d_2}{\varepsilon_2} + \frac{d_3}{\varepsilon_3} = \frac{\sum_{i=1}^{3} d_i}{\varepsilon_{eq}} \tag{3.11}$$

This formula can be used to replace the different stacked dielectric with a single dielectric, whose equivalent thickness and relative permittivity can be calculated using (3.10) and (3.11). Based on the reference [16] and equation (3.11), the substrate of CMOS 65nm technology can be simplified as Fig. 3.17.

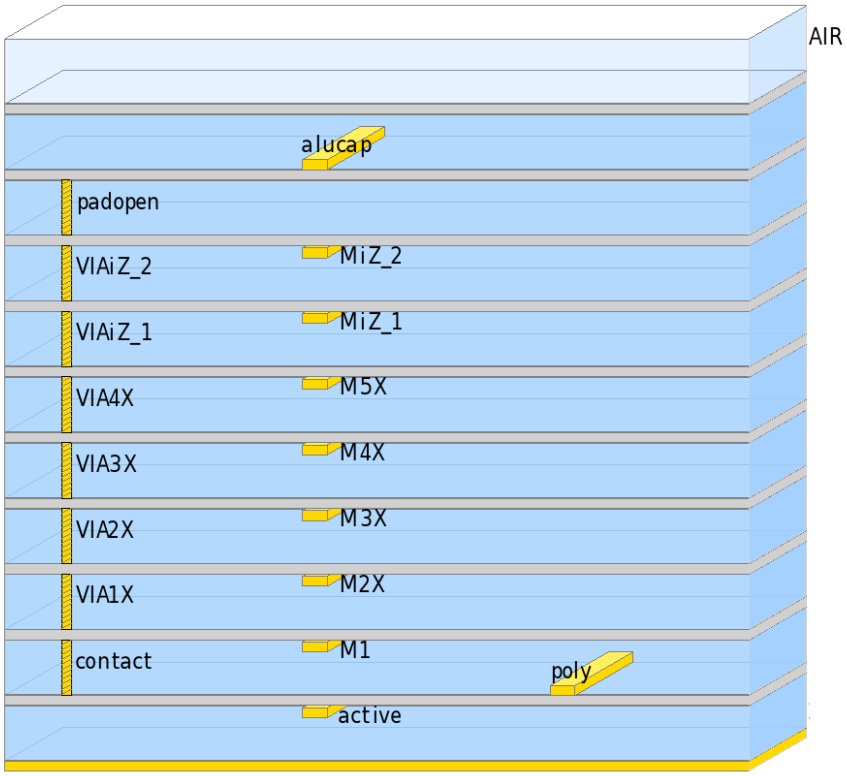


Figure 3.17: Substrate setup of EM simulation

The physical layout of the 3D inductor is shown in Fig. 3.18. In the left part of Fig. 3.18, the 3D inductor is located in the middle with an area of $18\mu m$ by $18\mu m$. The width of routing trace is $2\mu m$ and the gap between the traces is $2\mu m$ as well. The routing trace starts from the top metal layer and winds two turns to the center, and then drops one metal layer through a set of vias. In this next metal layer, the trace is now winding from the center to the outside by two turns, and then drops down to the fifth metal layer through another set of vias. This is repeated down to the third metal layer, with the trace ending in the centre of the inductor. At this point, the trace is connected to the second metal

layer through a final set of vias and is routed to the edge of the 3D inductor. The 3D view of the inductor is shown in the right part of Fig. 3.18.

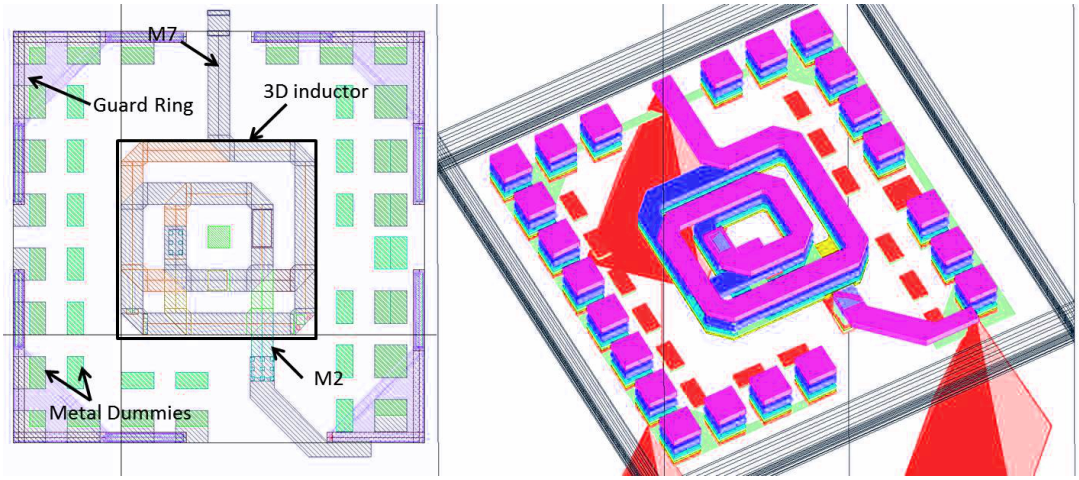


Figure 3.18: 3D inductor

From the EM point-of-view, a critical point is crosstalk to adjacent circuits. Indeed, the EM field is coupled into the substrate underneath the 3D inductor and can then travel to other parts of the circuit and cause the interference. To avoid this, an additional guard ring around the 3D inductor is required to minimize the interference. The main function of the guard ring is to isolate the substrate under the 3D inductor from the remainder of the substrate. In the left part of Fig. 3.18,the guard ring is placed outside of the 3D inductor, its size is $38\mu m$ by $38\mu m$ and hence the guard ring is $10\mu m$ away from the 3D inductor. The guard ring itself consists of a $P+$ doping layer and is connected to the first metal layer using a large amount of contacts. The guard ring is connected to the clean signal ground of the chip. In addition, to prevent potential oscillation and circular currents due to coupled interference, the guard ring structure is not a closed loop: there is a gap on each side of the ring.

To ensure that the metal layers are sufficiently flat, chemical mechanical planarization (CMP) steps are used during the fabrication process of the chip. Successful CMP and sufficient flatness requires a minimum metal density (i.e. the proportion of the area of the chip covered with metal to the area of the complete chip, as well as sub-rectangular areas inside the chip itself) requirement on each metal and via layer. In order to achieve such metal density requirements, dummy “tiles” of each metal layer have to be inserted into the space between the center 3D inductor and the guard ring. Those extra metal tiles could potentially impact the performance of the 3D inductors, as such metal tiles can increase the parasitic capacitance of 3D inductors. To minimize the

impact, metal tiles with large size and multiple metal layers are placed along the guard ring in order to keep the maximum distance from the center inductor. Tiles with smaller size in the lower metal layers are placed near the inductor. In the right part of Fig. 16, dummy tiles for the entire metal stack are located along the guard ring. Only dummy tiles for the first and second metal layers (red rectangle) are placed close to the 3D inductor itself.

The EM simulation results are shown in Fig. 3.19. Based on the topology of the level shifter and the D flipflop, one port of the 3D inductor is connected to the positive power supply. From an RF point-of-view and assuming a sufficiently clean power supply, one port of the 3D inductor is connected to the AC ground and the other port is connected to the AC signal path. Therefore to characterize the 3D inductor, one port of the inductor is connected to ground and the impedance (Z_{11}) has been calculated by looking into the other port. Eventually, the imaginary part of Z_{11} at low frequencies represents the inductance of 3D inductor. The real part of Z_{11} is the parasitic resistance of the inductor. The quality factor (Q) of the inductor is the imaginary part of Z_{11} divided by the real part of Z_{11}.

In the top left of the Fig. 3.19, the inductance is calculated by dividing the imaginary part of Z_{11} by $2\pi f$. For sufficiently low frequency, the impact of the parasitic capacitance is negligible, assuming the equivalent circuit model in the bottom right of Fig. 3.19. An inductance around $900pH$ has been realized. Furthermore the inductance increases with increasing frequency as shown in the top left of Fig. 3.19. Here is the explanation. Let us assume the R_p is very small to simplify the problem. Then, the Z_{11} can be derived as following:

$$imag(Z_{11}) \approx j\omega L || \frac{1}{j\omega C} = j\omega \frac{L}{1-\omega^2 LC} \tag{3.12}$$

By increasing frequency, the denominator of (3.12) is reduced which increases the imaginary part of Z_{11}. Hence, in the frequency range of interest ($DC \sim 30GHz$), the inductance increases from $900pH$ to $1050pH$. The real part of Z_{11} is equivalent to the parasitic resistance of the inductor which is around 18Ω. However, for increasing frequency, the L and C_P impact the real part of Z_{11} dramatically based on the equivalent circuit model in Fig. 3.19 and the skin effect can not be ignored as well. Therefore, it is resulting in an increasing overall resistance. Hence, in the frequency range of interest, the parasitic resistance increases from 18Ω to 55Ω. The quality factor (Q) has been plotted in the top

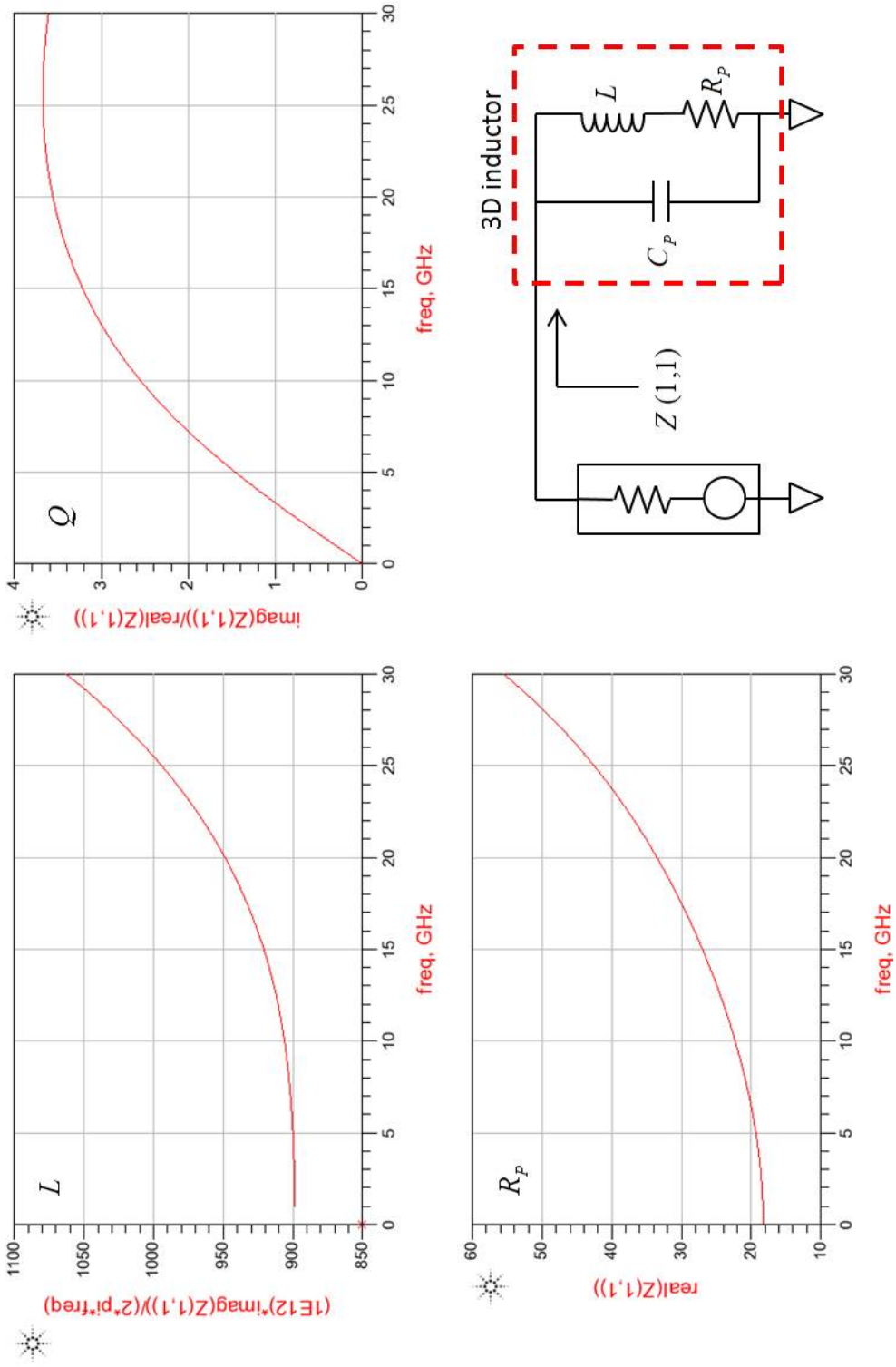


Figure 3.19: Simulation results of 3D inductor, inductance (left top), Q (right top), resistance (left bottom), and equivalent circuit model (right bottom)

right of Fig. 3.19. Q is an important parameter, which indicates the behavour of the 3D solenoid-shaped coil. In low frequency range, Q increases following the frequency. This indicates the 3D solenoid-shaped coil acts as an inductor. When frequency goes up, the parasitic capacitance becomes dominant and the increase of Q is reduced, till the curve becomes flat. Beyond this frequency the parasitic capacitance dominates and the 3D coil acts as a capacitator, with the Q factor becoming negative. In this case, the Q plotted as top right in Fig.3.19 indicates the 3D coil is acting as inductor in the frequency range $DC \sim 30GHz$.

The EM simulation results of 3D inductor have been exported by the EM simulator (ADS2014) as S-parameter file (*.s2p). In Cadence, the S-parameter file is read by the "nport" cell from "analogLib" library. For the co-simulation, the 3D inductor would not appear in schematic and layout directly. Extra ports are added for the inter-connection between the "nport" and rest part of the circuits. The postlayout extraction has been only applied for the circuits except the 3D inductor. After the extraction, the "nport" cells with S-parameter of 3D inductor and postlayout extraction results would be placed into one schematic and connected through the ports for the final co-simulation.

3.10 Biasing circuitry

In addition to the main data path, biasing circuits have been designed to ensure the CML Gray coding circuit, high speed D flipflops and level shifter circuits work properly across process, temperature and supply voltage variations. The used bias circuits include two parts. Firstly a so-called constant transconductance (gm) circuit generates a current minimizing process dependence of the biased circuits, and secondly current mirrors are used to distribute the constant gm currents to the various blocks, see Fig. 3.20. The design of the constant gm and current mirror are following the "textbook" design procedures, the interested reader is referred to the many existing books on these topics. One particular aspect of the constant gm circuitry in Fig. 3.20 warrants some additional analysis as it differs from the more conventional approaches.

In Fig. 3.20, assuming the opamp is ideal and that transistors MN_1 and MN_2 have identical geometries, the width of MN_4 is chosen to be four times wider compared to MN_3 and the channel length of transistors MN_4 and MN_3 are the same. The precision resistor R_S is outside the driver chip. Since the opamp is

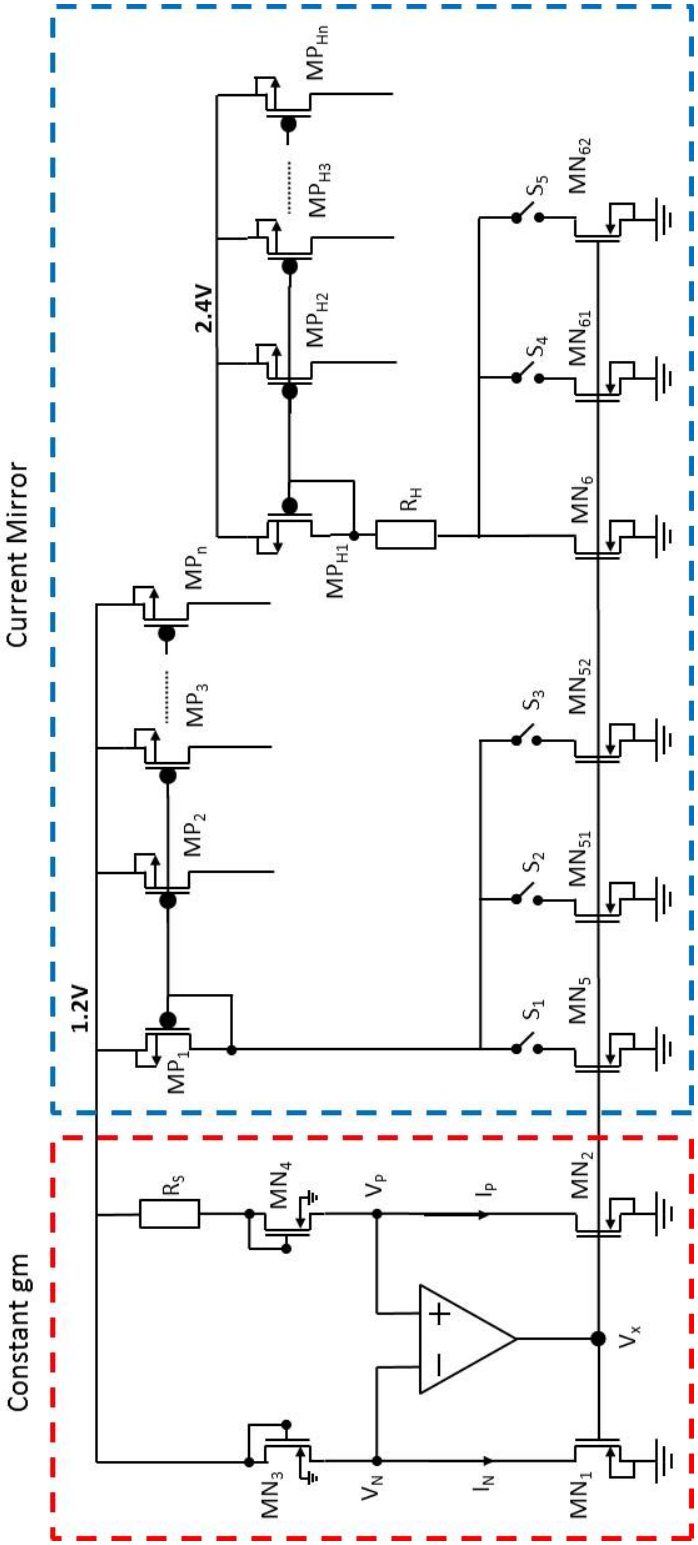


Figure 3.20: Biasing circuitry

ideal (no DC-offset, infinite gain), the drain voltage of MN_1 and MN_2 are the same ($V_N = V_P$). Let's call gate voltage of MN_1 and MN_2 V_X. As MN_1 and MN_2 are identical and all their terminals are at the same potentials, the drain current of MN_1 is the same as drain current of MN_2 ($I_N = I_P$). In addition, since there is no current flow into the inputs of the opamp, the drain current of MN_3 is equal to I_N and the drain current of MN_4 is equal to I_P. The drain current of MN_3 can be derived as following:

$$I_N = \frac{1}{2}\mu_N C_{OX}\frac{W_{MN_3}}{L}(V_{DD} - V_N - V_{TH(MN_3)})^2 \tag{3.13}$$

where V_{DD} is supply voltage and $V_{TH(MN_3)}$ is the threshold voltage of MN_3, and assuming the transistors obey the conventional square law model. μ_N is the drain mobility and C_{OX} is the gate oxide capacitance per square meter. The drain current of MN_4 can also be derived using same principle:

$$I_P = \frac{1}{2}\mu_N C_{OX}\frac{W_{MN_4}}{L}(V_{DD} - V_P - I_P R_S - V_{TH(MN_4)})^2 \tag{3.14}$$

where $V_{TH(MN_4)}$ is the threshold voltage of MN_4. From (3.13) and (3.14), the following equations are derived as (3.15) and (3.16):

$$V_{DD} = V_N + V_{TH(MN_3)} + \sqrt{\frac{2I_N}{\mu_N C_{OX}\frac{W_{MN_3}}{L}}} \tag{3.15}$$

$$V_{DD} = V_P + I_P R_S + V_{TH(MN_4)} + \sqrt{\frac{2I_P}{\mu_N C_{OX}\frac{W_{MN_4}}{L}}} \tag{3.16}$$

Since $V_N = V_P$, $I_N = I_P$, and threshold voltage of MN_3 and MN_4 are the same, the following equations are also true:

$$\sqrt{\frac{2I_N}{\mu_N C_{OX}\frac{W_{MN_3}}{L}}} = I_P R_S + \sqrt{\frac{2I_P}{\mu_N C_{OX}\frac{W_{MN_4}}{L}}} \tag{3.17}$$

$$I_P R_S = \sqrt{\frac{2I_P}{\mu_N C_{OX}\frac{W_{MN_3}}{L}}} - \sqrt{\frac{2I_P}{\mu_N C_{OX}\frac{W_{MN_4}}{L}}} \tag{3.18}$$

$$\sqrt{I_P} = \frac{1}{R_S}\sqrt{\frac{2}{\mu_N C_{OX}\frac{W_{MN_3}}{L}}}\left(1 - \sqrt{\frac{1}{\frac{W_{MN_4}}{W_{MN_3}}}}\right) \tag{3.19}$$

$$I_P = \frac{2}{\mu_N C_{OX}\frac{W_{MN_3}}{L}}\left(1 - \sqrt{\frac{1}{\frac{W_{MN_4}}{W_{MN_3}}}}\right)^2 \frac{1}{R_S^2} \tag{3.20}$$

The transconductance gm_{MN2} of MN_2 equals:

$$gm_{MN_2} = \sqrt{2\mu_N C_{OX}\frac{W_{MN_2}}{L_{MN_2}} I_P} \tag{3.21}$$

By plugging (3.20) into (3.21), the transconductance of MN_2 can be derived as following:

$$gm_{MN_2} = \sqrt{2\mu_N C_{OX}\frac{W_{MN_2}}{L_{MN_2}} \cdot \frac{2}{\mu_N C_{OX}\frac{W_{MN_3}}{L}}\left(1 - \sqrt{\frac{1}{\frac{W_{MN_4}}{W_{MN_3}}}}\right)^2 \frac{1}{R_S^2}} \tag{3.22}$$

$$gm_{MN_2} = \sqrt{\frac{W_{MN_2}}{L_{MN_2}} \cdot \frac{L}{W_{MN_3}}}\left(1 - \sqrt{\frac{1}{\frac{W_{MN_4}}{W_{MN_3}}}}\right)\frac{2}{R_S} \tag{3.23}$$

Since the width of MN_4 is four times of the width of MN_3, the equation (3.23) can be simplified as following:

$$gm_{MN_2} = \frac{1}{R_S} \cdot \sqrt{\frac{L}{L_{MN_2}} \cdot \frac{W_{MN_2}}{W_{MN_3}}} \tag{3.24}$$

Hence from equation (3.24), the transconductance of MN_2 is only dependent on two parameters, one of which is the width ratio of MN_2 to MN_3 and the other is the precision resistor R_S. Therefore, the transconductance of MN_2 can be made independent of the process corner and temperature, as long as the external precision resistor is constant with temperature. In this design, the precision resistor is placed outside the PAM4 driver IC (on PCB), therefore the temperature interference from the driver IC is minimized.

Transistors MN_5, MN_6, and MN_2 are identical and have the same biasing condition. So, the drain currents of MN_5 and MN_6 are equal to drain current of MN_2, and the gm of MN_5 and MN_6 are constant as well. By using the current

mirror circuitry, the constant gm bias currents have been copied by MP_1 and MP_{H1} and distributed to CML gray coding logic gates, high speed D flipflops, and level shifter circuits through $MP_2 \sim MP_n$ and $MP_{H2} \sim MP_{Hn}$. The current mirror circuitry is shown in Fig. 3.20.

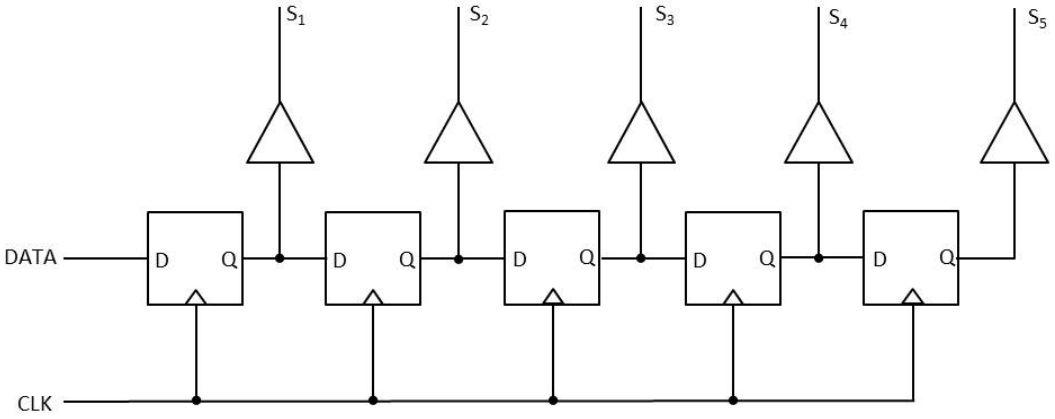


Figure 3.21: SPI control circuitry

To increase the controllability of the bias currents of CML gray coding logic gates, high speed D flipflops, and level shifter circuits, additional switches and current tail transistors have been introduced in current mirror. In Fig. 3.20, the channel width of MN_{51} is twice of the MN_5's width, and the channel width of MN_{52} is four times of the MN_5's width; MN_6, MN_{61}, and MN_{62} have the same width ratio as MN_5, MN_{51}, and MN_{52}. By adding switches $S_1 \sim S_5$, a binary weighted control of the bias current has been realized. The switches $S_1 \sim S_5$ are realized by NMOS transistors and are controlled via the serial interface (shift register) circuit shown in Fig. 3.21, consisting of standard low speed D flipflops. The on-off signal of $S_1 \sim S_5$ are coded into a series binary code by using external micro-controller board. After five clock cycles, the binary code is loaded into the D flipflops completely. The clock frequency is 4MHz generated by external micro-controller board.

3.11 Summary

The full chip schematic is shown in Fig. 3.22. It includes the encoder circuitry (Gray coding CML gates), driver stage circuitry (three level shifter circuits, six voltage combiner circuits and two switched capacitor banks), input matching network, biasing circuitry (constant gm circuit and current mirrors), and SPI

register control circuitry. The input matching network is discussed in chapter 4. The full chip layout is shown in Fig. 3.23. Since the CMOS driver chip will be flip-chipped on top of the silicon photonic Lumped-MZM, the output pads of the CMOS driver chip are located in the middle of the driver. The high speed I/O pads (two differential 20Gb/s NRZ signals and one 20GHz differential clock signal) are located on the top. The power supply pads are placed on the right and left sides . The pads for SPI control are located at the bottom. The full chip size is $1.9mm$ by $0.9mm$ and the core circuitry occupies $0.25mm$ by $0.44mm$.

The post layout simulation results of the PAM4 driver IC are shown in Fig. 3.24. The 40Gb/s PAM4 differential signals have been successfully generated with $\sim$0.9V peak-to-peak voltage swing cross all corners (process variation). The eye diagrams are plotted on the right side of Fig. 3.24. In order to overcome the nonlinearity of the electro-optical transfer function of Lumped-MZM shown in Fig 2.1, the capacitance of the capacitors' bank has been adjusted. Therefore, the middle of the eye is somewhat closed. The total power consumption of the driver chip is around 236mW (5.9pJ/bit at 40Gb/s). The driving stage consumes around 192.36mW. The rest part of the circuits (encoder circuit, biasing circuit, and SPI register control circuit) consumes around 43.64mW. If we only consider the driving stage, the efficiency is around 4.8pJ/bit.

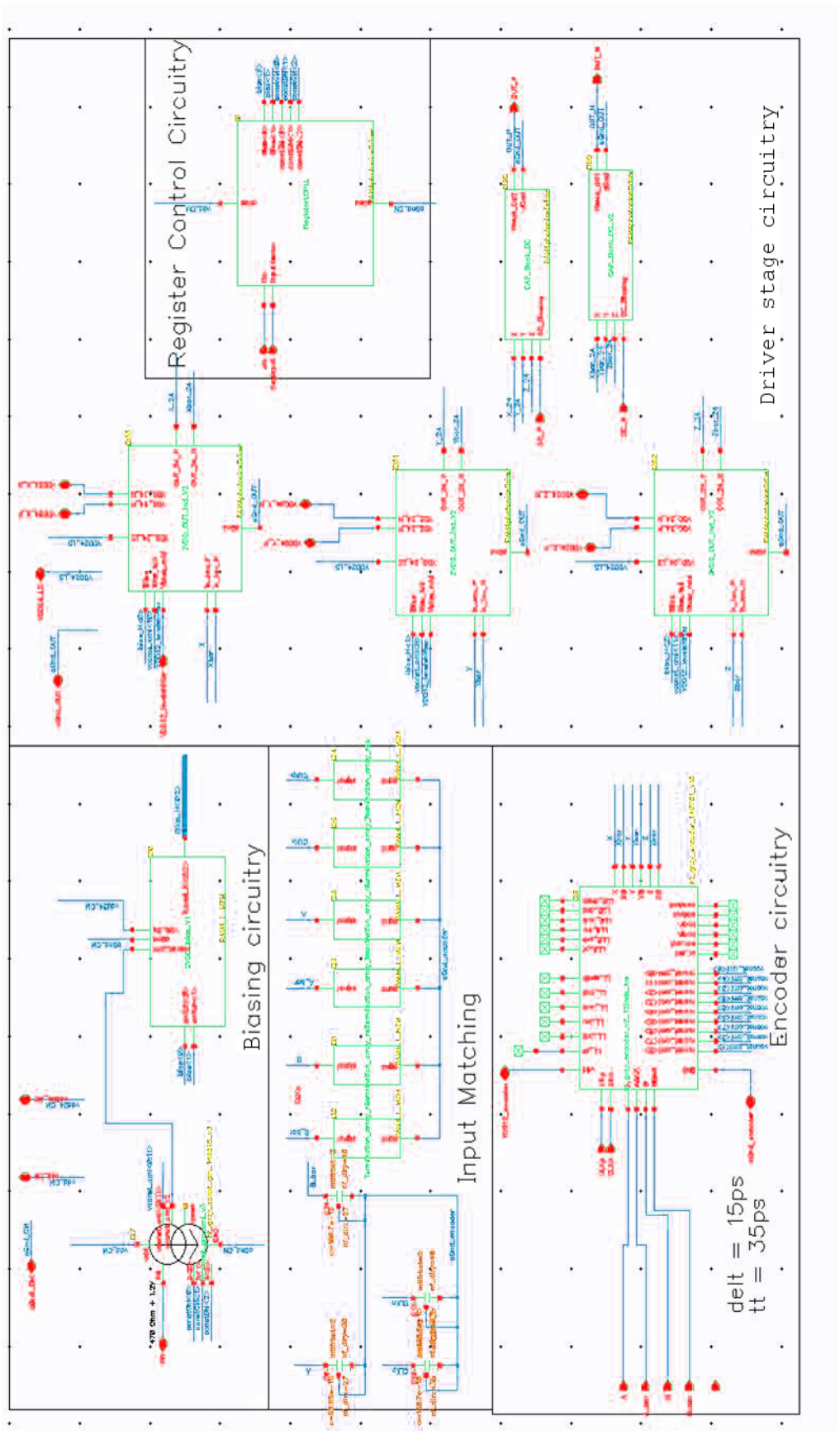


Figure 3.22: Schematic of PAM4 CMOS driver for Lumped MZM

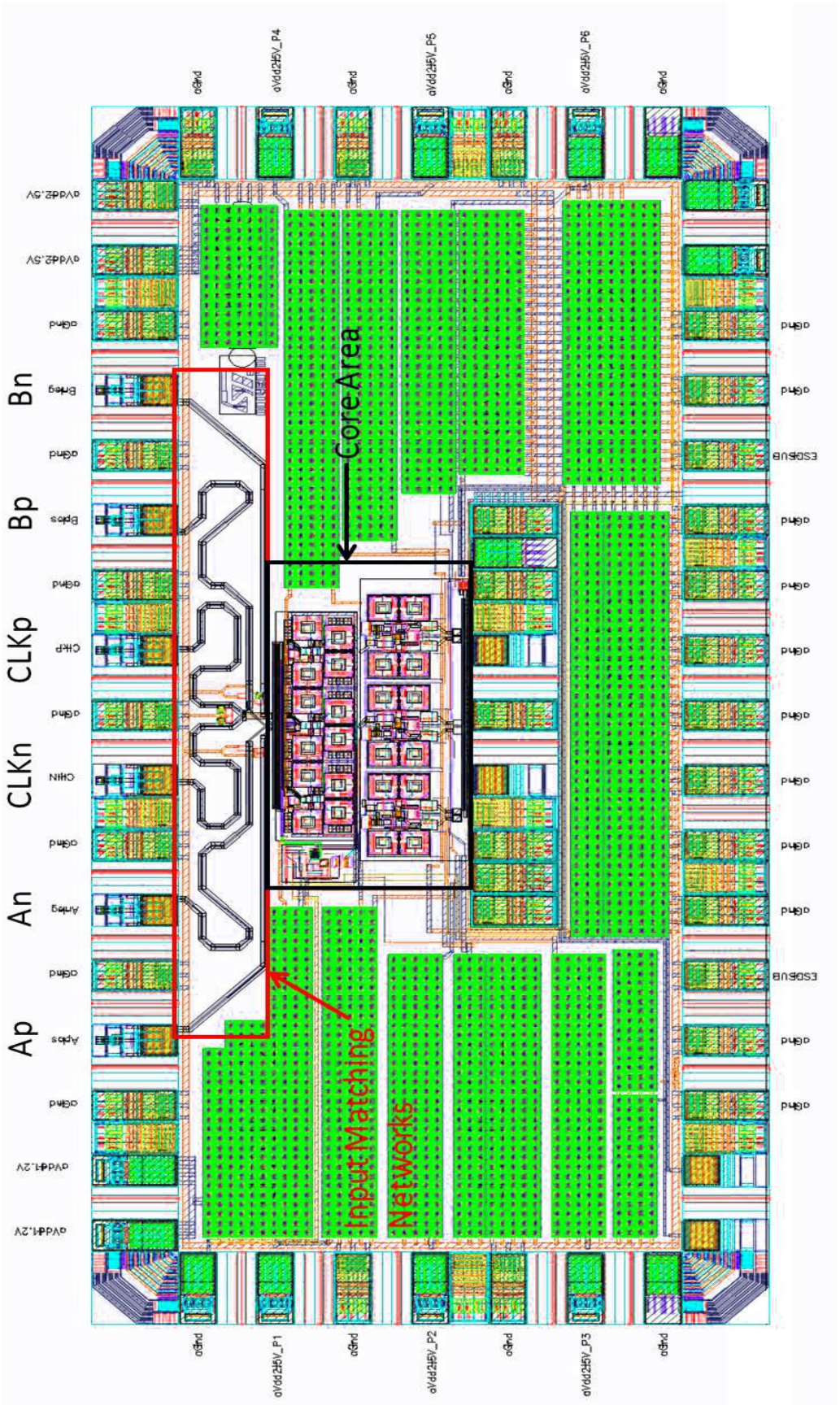


Figure 3.23: Layout of PAM4 CMOS driver for Lumped MZM

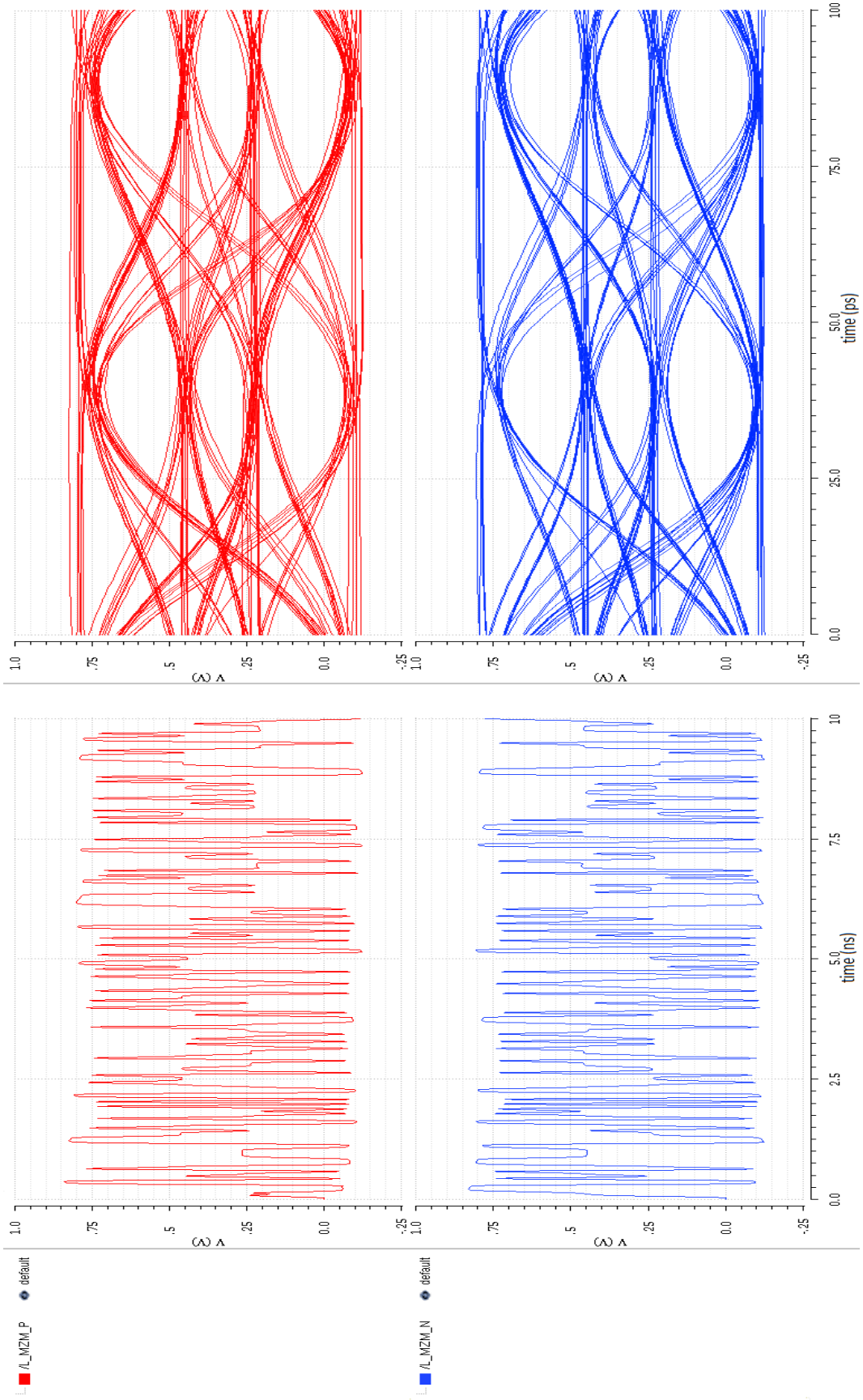


Figure 3.24: Post layout simulation results of PAM4 CMOS driver

Chapter 4

Broadband I/O and packaging design

The integrated circuits targeted in this thesis have a significant amount of IOs operating at bitrates up to 25Gb/s. For example the PAM-4 driver chip introduced in the previous chapter includes a total of 8 high-speed IOs. There are the two differential data inputs (accounting for 4 IOs), the differential clock input (accounting for another 2 IOs) and the output IOs. The first six IOs need to receive signals over long traces and coaxial cables and hence need to operate in a 50Ω matched environment. An important challenge is how to transfer these high-speed signals to and from the ICs. Indeed stringent requirements are placed upon the high-speed IOs: return loss less than 10dB and high bandwidth (>20GHz) are required for signal integrity despite the presence of the capacitance of the bondpad (which includes the capacitance of the ESD protection diodes) and the parasitic capacitance and inductance of the interconnect structure. In principle equalizers could be used to mitigate bandwidth limitations however this increases power consumption and chip area.

As a specific example, here we consider how to transfer the two data signals and the clock signal from the connectors on the PAM-4 transmitter all the way to the logic gates of the Gray encoder on the driver chip. The signals travel first across a printed circuit board, next a ceramic board to match the physical pitch of the Silicon Photonic IC, next across the Silicon Photonic IC itself before finally arriving on the chip itself. The connection is shown as Fig. 4.1. One thing needs to notice is that the ceramic interposer is required because the minimum pitch of PCB technology is much larger that the pitch on the silicon

photonic IC and the pitch of ceramic technology is perfect to create the link. On the chip itself the signals need to be distributed to three different logic gates (for the data signals) and three D-flipflops (for the clock signals). Options for broadband matching such as T-coil matching are discussed extensively. A design methodology for absorbing the interconnect inductance and capacitance into a microwave filter network with flat response is introduced.

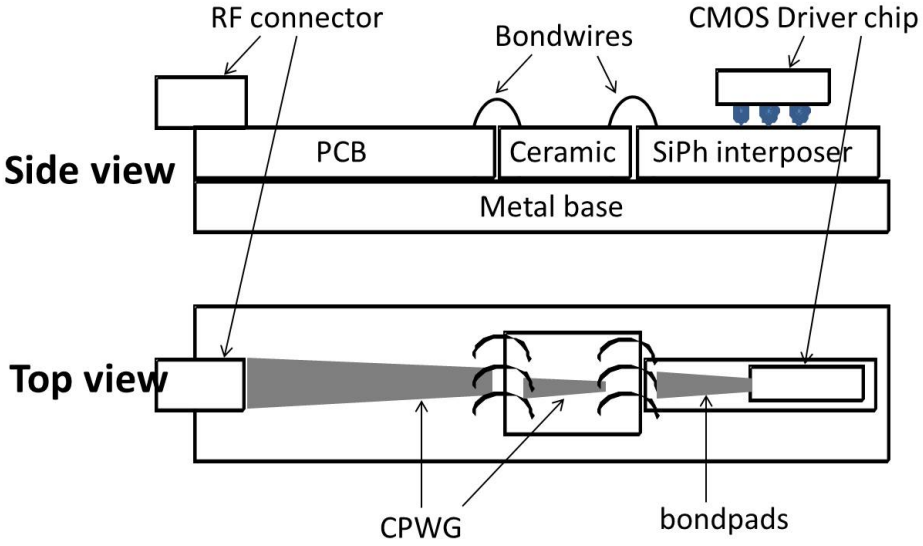


Figure 4.1: Connection to driver chip over printed circuit board (PCB), ceramic and Silicon Photonic (SiPh) interposer

4.1 Inductive properties of the metal traces

At high frequencies (tens of GHz) the inductance of the metal traces used to carry signals around a chip are no longer negligible. Therefore, it is important to develop a rule of thumb regarding the amount of inductance per unit length of the metal trace on a Silicon chip. While the inductance values can be derived using an EM simulator, a rule of thumb is important to avoid the need to run many time consuming EM simulations. Such a rule of thumb significantly increases the design speed.

The problem has been simplified as shown in Fig. 4.2. A metal trace is placed on top of the conductive semiconductor substrate. The thickness of the dielectric layers between the metal trace and conductive substrate is d; the width of the metal trace is w. The surface of magnetic flux has been selected as red rectangle

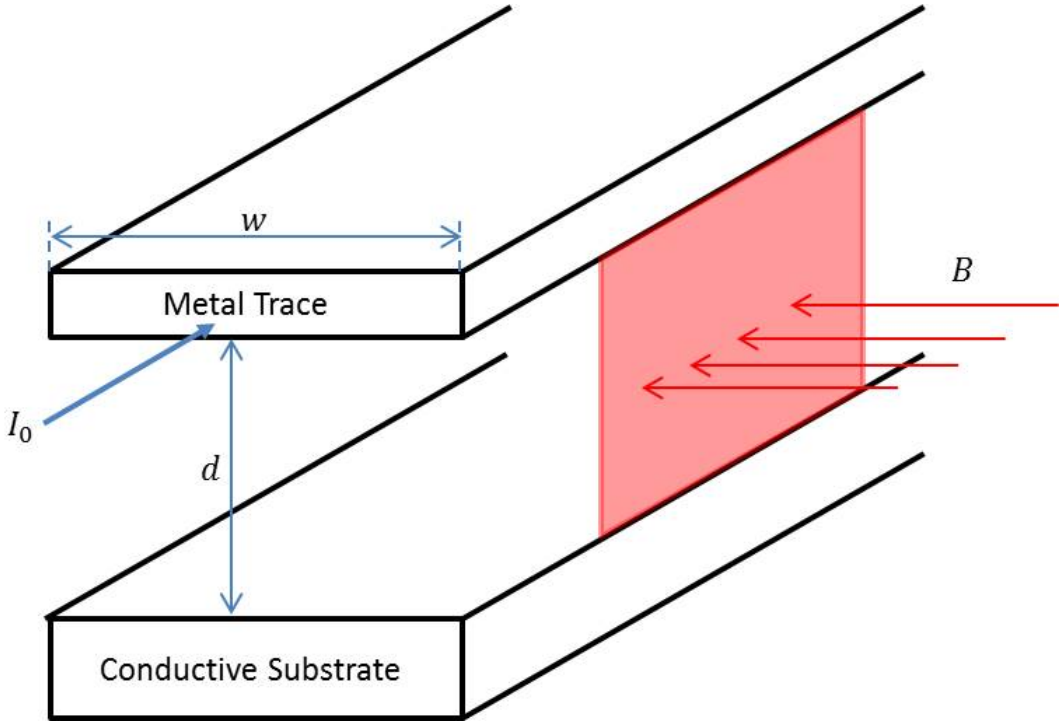


Figure 4.2: Inductance per unit length of metal trace

with the assumption that the magnetic field strength B is uniform. The length of the metal trace is l and the current is I. From the definition of the inductance, the following equation can be derived [37]:

$$L = \frac{1}{I} \oint_S Bds = \frac{1}{I} \cdot B \cdot d \cdot l \tag{4.1}$$

Where L is the inductance of the metal trace with length l. From Ampere's Law in Maxwell equation, the following formula can be derived [37]:

$$\oint_{\partial S} Bdl = \mu_0 \oint_S Jdl \tag{4.2}$$

where the left side of the equation is the integration of the B field circular around the metal trace and the right side of the equation is the integration of the current density (J) over the cross-section S of the metal trace. In order to simplify the calculation, it is assumed that the majority of the B field is concentrated within the area between the metal trace and conductive substrate. Therefore, equation (4.2) can be transformed into following equations [37]:

$$\oint_{\partial S} Bdl \approx B \cdot w \approx \mu_0 I \tag{4.3}$$

$$B \approx \frac{\mu_0 I}{w} \tag{4.4}$$

Plugging (4.4) into expression (4.1), the equations can be derived as following:

$$L \approx \frac{1}{I} \cdot \frac{\mu_0 I}{w} \cdot d \cdot l \tag{4.5}$$

$$\frac{L}{l} \approx \mu_0 \cdot \frac{d}{w} \tag{4.6}$$

The expression of inductance per unit length is derived as (4.6), where μ_0 is the permeability of the material between the metal trace and conductive substrate. Since the dielectric under the metal trace is not ferromagnetic material, the permeability is the same as the vacuum permeability. Equation (4.6) indicates that the inductance per unit length increases if the width of the metal trace is reduced, and increases if the distance between the trace and the conductive substrate is increased. This is the reason why most designs use the top metal layer for inductor. It not only has the lowest parasitic capacitance but also a higher inductance. Reducing the width is also possible to increase inductance, however this goes at the cost of increasing the parasitic resistance. If the width of the metal trace (w) is close to the value of the distance (d) between the metal trace and substrate, then equation (4.6) can be simplified further to:

$$\frac{L}{l} \approx \mu_0 \cdot \frac{d}{w} \approx \mu_0 = 4\pi \times 10^{-7} H/m \approx 1.26 pH/\mu m \tag{4.7}$$

Hence, as a rule of thumb, the inductance per unit length of the metal trace is around $1.26 pH/\mu m$. During the design process, a first iteration of a matching network that requires inductors can be designed using the $1.26 pH/\mu m$ rule of thumb. Then, an EM simulator can be used to get more precise estimations for the inductance.

4.2 Design methodology for broadband matching networks

The large capacitance (easily a few hundred femtofarrad) of ESD protection diodes and bondpads severely limits bandwidth. One option is to use inductive peaking to overcome these limitations. However it is known that it is difficult to simultaneously achieve good return loss over a large bandwidth using this technique [38]. In [39], the ESD capacitance is split into smaller, parallel capacitors (diodes) which are interconnected using inductive traces thus effectively creating a transmission line. Unfortunately the relatively long traces require large chip area and introduce RF losses, and also reduce the protection against ESD events. Here we use two other solutions. The first solution uses the well-known T-coil, the second solution absorbs the inductance and capacitance into a filter network with flat response. Two matching networks are design based on these two solutions and finally compared against each other. Of particular importance is how to achieve good return loss and minimum insertion loss even for the complicated interconnect involving for example signals carried over a ceramic substrate, over the Silicon Photonic chip onto the actual driver chip. (see Fig. 4.10 and Chapter 5 for the physical implementation of the PAM-4 transmitter).

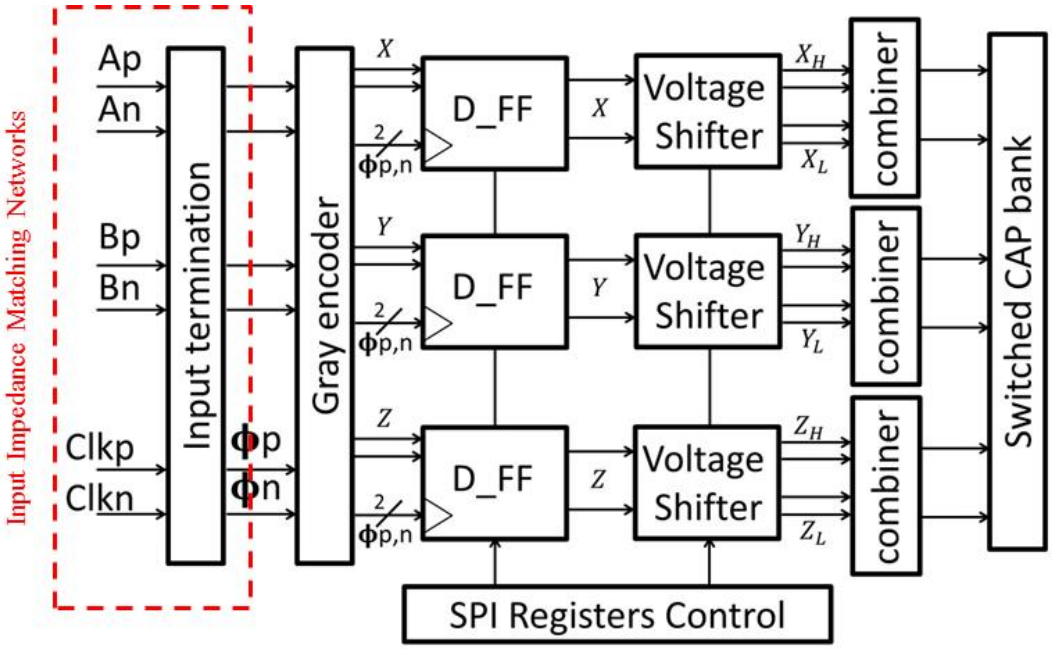


Figure 4.3: Top level of CMOS driver chip

The broadband matching network is the first stage of the electronic chip shown

in Fig. 4.3. In order to make sure the maximum energy can flow into the electronic chip through the silicon photonic chips with minimum reflection and maximum transmission, conjugate impedance matching is necessary from the PRBS data generator to the gates of the CMOS transistors in the electronic chip shown as Fig. 4.1. The spectral content of a 20Gb/s NRZ signals is mainly contained between 0Hz and 20GHz. Hence the matching network should have a 3dB bandwidth of at least 20GHz and the return loss should be better than -10dB over the same bandwidth.

Here we introduce a new approach based on microwave filter theory to design the broadband matching networks with much smaller chip area for the PAM4 driver chip. Before explaining the method itself it is usefull to consider two topologies of low pass microwave filters: constant k filters and modified butterworth filters.

4.2.1 Constant k filter

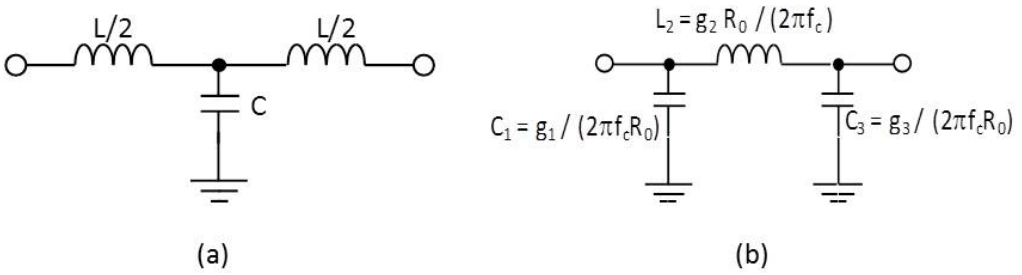


Figure 4.4: (a) Constant-k filter section (b) 3rd order low-pass filter (R_0: termination resistance, f_C: cut-off frequency)

Fig. 4.4 (a) shows a constant k filter section. If we define a cut-off frequency f_c and nominal characteristic impedance R_0 as:

$$f_C = \frac{1}{\pi\sqrt{LC}} \tag{4.8}$$

$$R_0 = \sqrt{\frac{L}{C}} \tag{4.9}$$

Then we can calculate the so-called image impedance Z_{iT} as:

$$Z_{iT} = R_0\sqrt{1 - \frac{f^2}{f_C^2}} \tag{4.10}$$

If we terminate this constant k filter section at both ports with its image impedances Z_{iT}, then it can be shown that up to the cutoff frequency f_C, its insertion loss is 0dB ([28], page 391). In practice it costs extra chip area to terminate a constant k filter section with its image impedances Z_{iT} since the m-derived sharp-cutoff sections have to be introduced ([28], page 396); rather the constant k filter section is terminated with a load resistance R_L which causes the actual filter transfer to be different from its ideal shape. However if the cut-off frequency f_C is sufficiently large compared to the frequency of interest, then good return loss and minimum insertion loss can be obtained if R_0 is chosen equal to the termination resistance R_L.

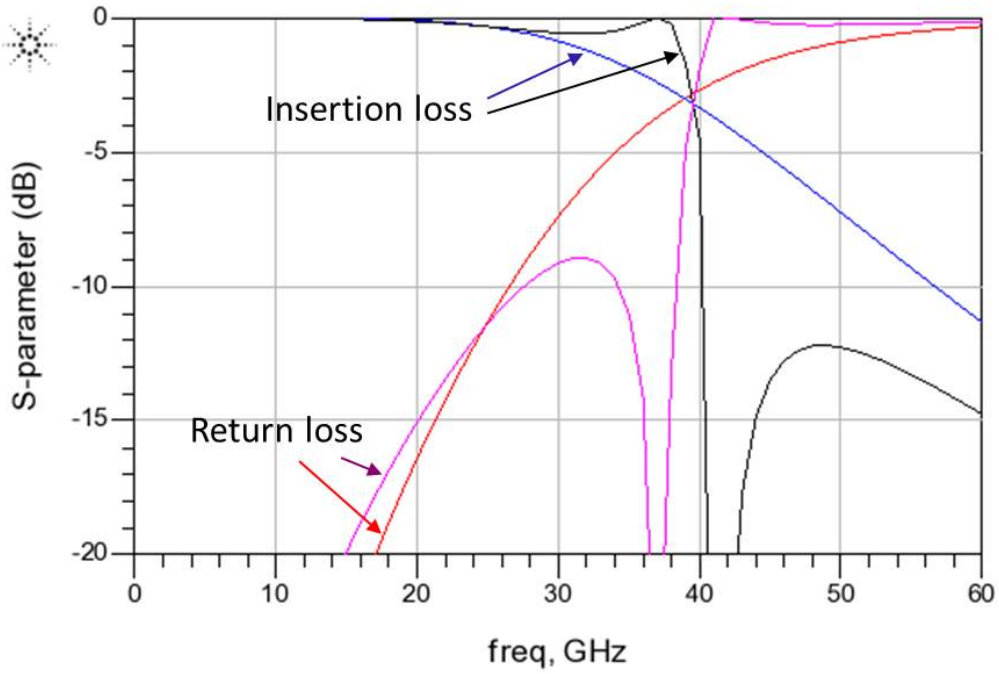


Figure 4.5: Insertion loss and return loss of constant-k filter ($f_C = 40GHz$, $R_0 = 50\Omega$) when terminated with image impedance (black line and pink line) and 50Ω termination impedance (blue line and red line).

This is shown in Fig. 4.5 for $f_C = 40GHz$ and $R_0 = R_L = 50\Omega$: observe how up to 20GHz (the frequency band of interest) the insertion loss is less than 0.1dB and the return loss is better than -18.2dB; the -10dB bandwidth is above 25GHz for a 50Ω termination, which is also close to the performance with perfect image impedance termination. In this case, the inductance (L) of the constant k filter

is 398pH and the capacitance (C) is around 160fF for the 50Ω system.

4.2.2 Modified Butterworth filter

Fig. 4.4(b) shows an implementation of an ideal 3rd order Butterworth low-pass filter: to obtain the Butterworth response, $g_1 = g_3 = 1$ and $g_2 = 2$. The insertion and return loss of the filter for 3dB cut-off frequency the $f_C = 30GHz$ are shown in Fig. 4.6 as the black and pink curve.

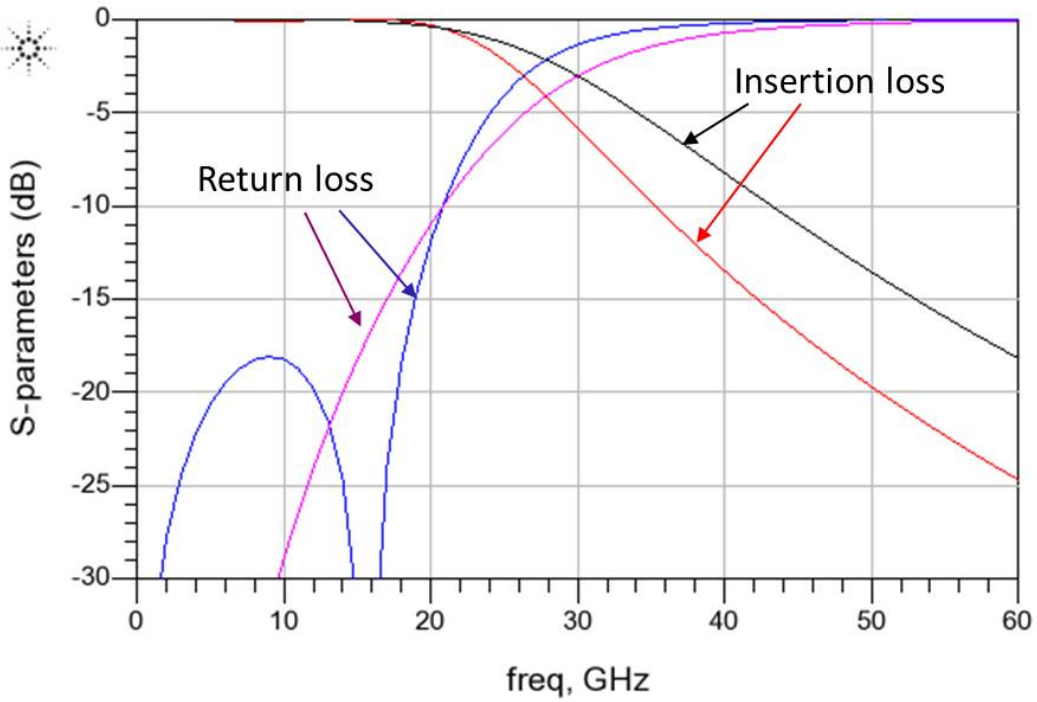


Figure 4.6: Insertion loss and return loss of (black and pink lines) Butterworth filter and the modified (red and blue lines) filter with reduced inductance for data signals

For a 50Ω termination, the inductor would be around $530pH$ and capacitor would be $106fF$ in Fig. 4.4(b) theoretically. In reality, the distance from bond-pads to the transistors' gates is limited and the length of each data signals' paths and clock signals' paths is not identical. In previous chapter Fig. 3.23, the layout of entire driver chip shows that the bondpads of two differential data signals (A_n, A_p and B_n, B_p) are located on both sides of the paths of differential clock signal (CLK_n, CLK_p). This indicates that the distance for data paths is larger than the clock paths. In addition, the capacitance of the high-speed bondpads is $160fF$ [16]. Therefore, the Butterworth filter structure has to be

modified and adapted for different situations. One modification for two differential data paths are shown in Fig. 4.6 as red and blue curves with coefficients $g_1 = g_3 = 1.5$ and $g_2 = 1.88$ in Fig. 4.4(b). The ripple in the passband of the filter (up to 20GHz) remains less than 0.2dB while the return loss improved to -12dB at 20GHz. In this case, the inductance (L) is $498pH$ and capacitance (C) is around $160fF$ for the 50Ω system.

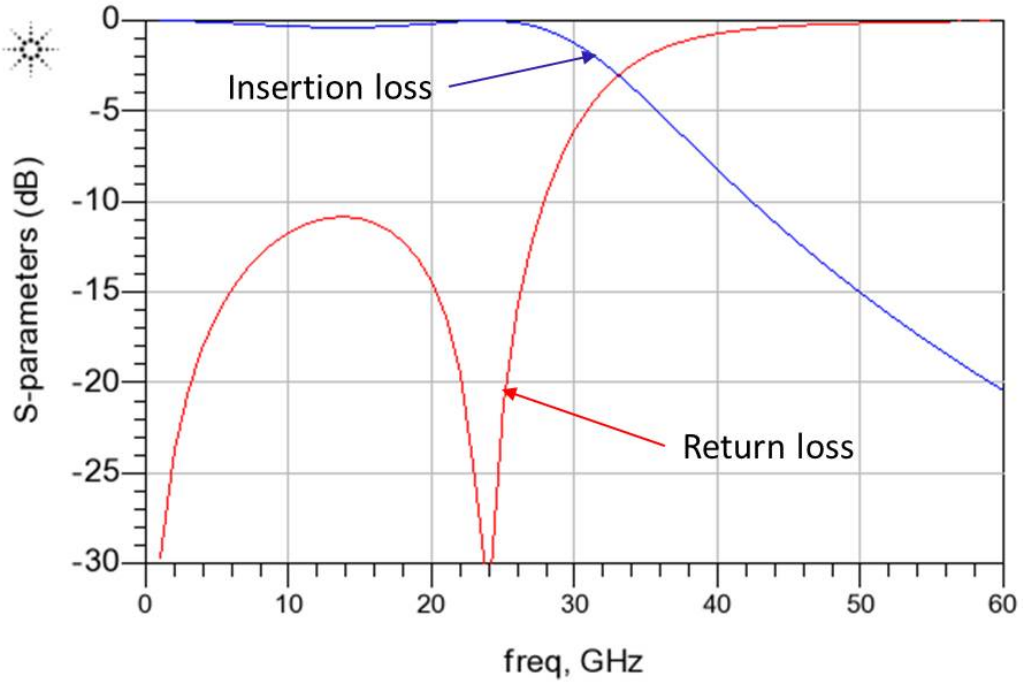


Figure 4.7: Insertion loss and return loss of modified Butterworth filter with reduced inductance for clock signals

The other modification for the differential clock signal is shown in Fig. 4.7 with coefficients $g_1 = 1.5$, $g_3 = 1.6$ and $g_2 = 1.23$ in Fig. 4.4(b). The ripple in the passband of the filter (up to 25GHz) remains less than 0.3dB while the -10dB bandwidth of return loss improved to 28GHz. In this case, the inductance (L) is $325pH$ and capacitance (C) is around $160fF$ and $176fF$.

4.2.3 Overview of broadband I/O design for PAM4 Tx

For the next step, the previously introduced two types of filter structures are cascaded to realize the matching network of the entire PAM4 transmitter. Fig. 4.1 shows a schematic diagram of the realized PAM-4 transmitter and in particular shows how the high-speed signals are transported from the RF connectors over a printed circuit board (PCB) and a ceramic substrate onto a Silicon Photonic

interposer chip (with Mach-Zehnder modulators). The driver IC is flip-chipped on top of Silicon Photonic interposer [23]. The high-speed signals are carried using grounded coplanar waveguides (CPWG) over the PCB, and using a cascade of a CPWG and a microstrip line over the ceramic to the Silicon Photonic interposer.

The layout of the ceramic interposer is shown in Fig. 4.8. The flip-chipped silicon photonic IC is placed within the white rectangle area. Six CPWGs are designed to conduct the differential data and clock signals to the other side of the board. The characteristic impedance of the six signal lines was designed to be 50Ohm. The width of the signal lines is increased in the middle of the board, and the gap between signal line and side ground is increased as well to maintain the same characteristic impedance. At the end of the CPWG, the short microstrip line is designed to facilitate a ribbon bondwire connection with the PCB. Ribbon bondwires are used to minimize inductance. The through hole vias connect the top ground planes to the grounded back plane. The dielectric constant of the ceramic board is 9.7 with $127\mu m$ thickness and the surface conductor is gold. The size of the ceramic is $5.14mm$ by $2.22mm$.

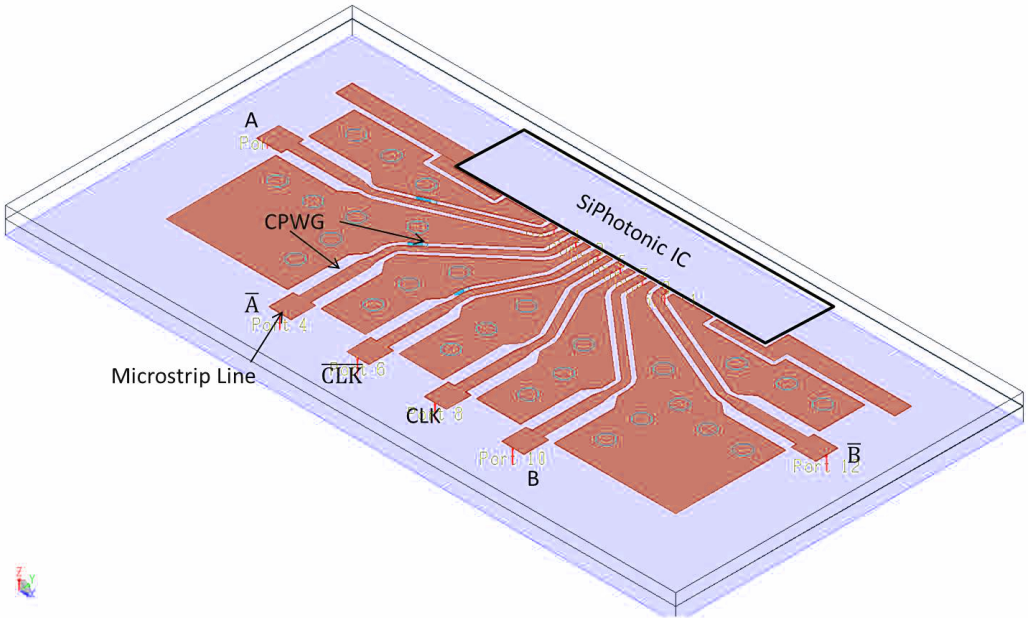


Figure 4.8: Layout of ceramic interposer

The layout of the PCB is shown in Fig. 4.9. The ceramic board is placed within the white rectangle area. The semi-circle shape is applied in order to equalize the group delay of the data signals and clock signals from the MSMP (Micro Sub-Miniature version P) connectors to the ceramic board in the center. Six

CPWGs are designed to conduct the differential data and clock signals from the Mini SMP connectors to the ceramic interposer. At the end of the CPWGs, additional routing traces are added to realize $\sim 200pH$ inductance and $\sim 160fF$ capacitance as per the constant k model in Fig. 4.4(a). The routing trace also acts as the bondpads to facilitate wirebonding between ceramic and PCB.

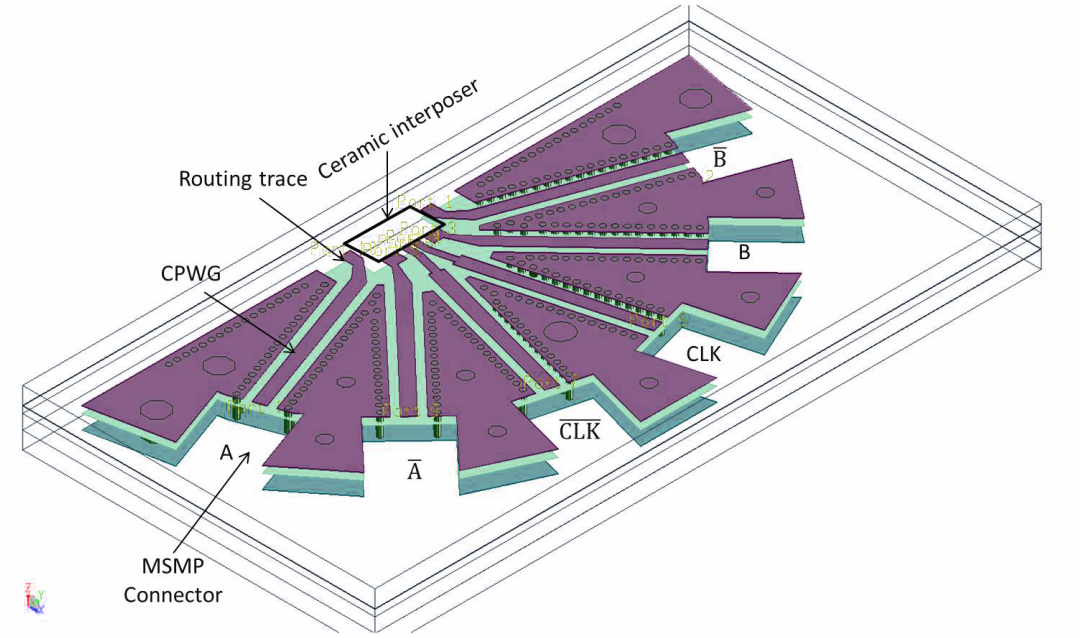


Figure 4.9: Layout of high speed PCB

All circles in Fig. 4.9 are through-hole vias which connect the top and middle group plane to the bottom ground. The dielectric between top and middle ground is Roger material with 3.66 dielectric constant and $508\mu m$ thickness. The material between middle ground and bottom ground is FR4 with 4.6 dielectric constant and $1.022mm$ thickness. The diameter of the semi-circle is $45mm$.

Fig. 4.10 shows how this complex interconnect can be mapped to a cascade of two constant k filter sections and a modified Butterworth low-pass filter on the driver chip itself. For the part on the electronic driver chip itself, the loading capacitance of the Gray coding CML gate, the capacitance of the bondpads (including ESD protection diodes) of the chip, and the inductance of the metal routing trace connecting the bondpads and the input gates form the modified Butterworth low-pass filter as explained before. The CMOS driver chip is flip-chipped on top of the silicon photonic IC. The inductance of the flip-chip bump and routing trace, the capacitance of the bondpad on the silicon photonic IC, and the inductance of the bondwire between the silicon photonic IC and ceramic interposer can be absorbed into a constant k filter. The inductance of the

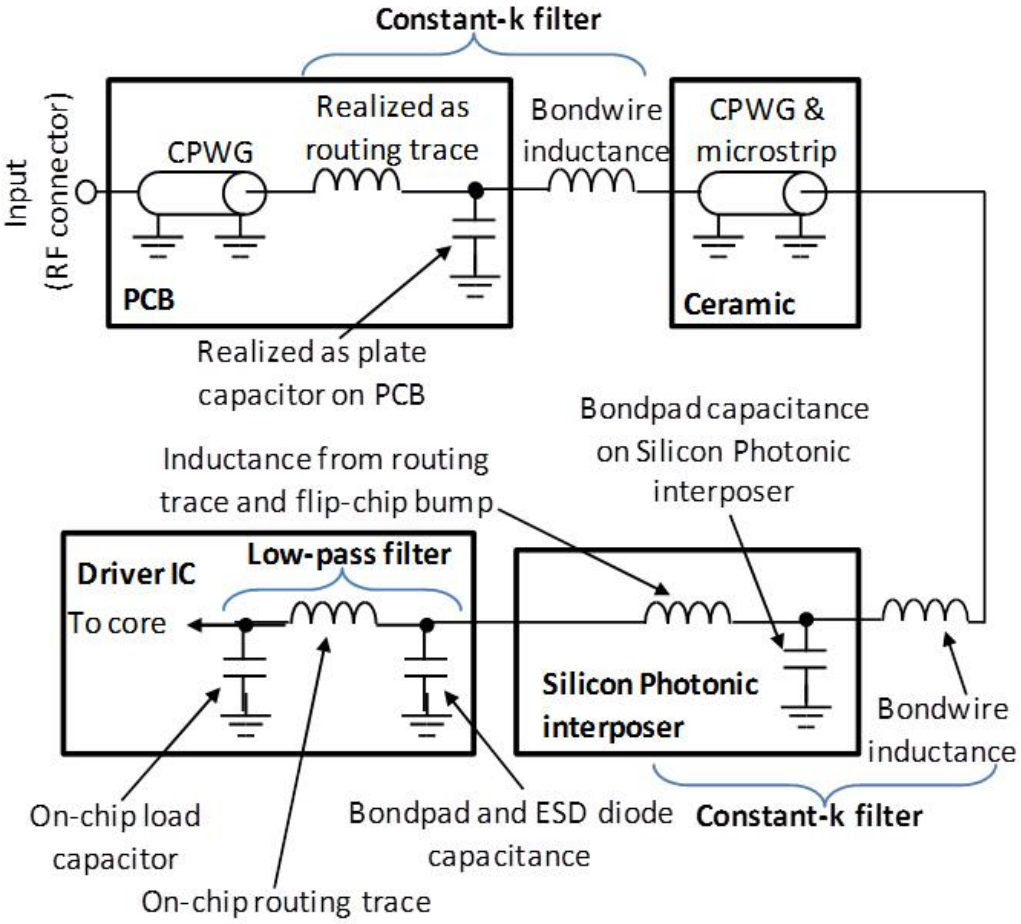


Figure 4.10: Overview of broadband I/O design for PAM4 transmitter

bondwire between the ceramic interposer and the high speed PCB, the capacitance of the bondpad on the PCB, and the inductance of the routing trace on PCB can be absorbed into a second final constant k section. The design of the constant k filter sections is done by first estimating the bondwire inductances (using electromagnetic design software), and then designing routing traces and contact pads on the PCB and ceramic that have a matched inductance and capacitance. The required capacitance can then be determined by the formula of constant k filter.

On the PCB and ceramic, the required capacitors are simply realized as plate capacitors between the top metal layer and the underlying ground plane; on the Silicon Photonic interposer this capacitance is the suitably sized bondpad capacitance. Note how the various parts are connected using CPWGs and microstrip lines: if care is taken to design these lines with constant 50Ω characteristic impedance then these do not affect the overall return loss and frequency response of the filter sections. For the constant k filter sections, the bondwire

inductance was estimated to be $\sim 200pH$ (realized using a ribbon bondwire from PCB to ceramic and a $18\mu m$ diameter bondwire from ceramic to Silicon Photonic interposer), thus requiring a capacitance of $160fF$ to fulfill the formula of constant k filter at a characteristic impedance of 50Ω and with a cut-off frequency $f_c = 40GHz$. The interconnections between the filters are coplanar waveguides; microstrip transmission lines were used on the ceramic interposer and high speed PCB.

The simulation results are shown in Fig. 4.11. The return loss is simulated with the ports located at the input of the MSMP connectors (Fig. 4.10). The -10dB bandwidth for the return loss is from DC to 27GHz for the two data paths. For clock signal path, the return loss bandwidth is from DC to 23GHz. The -3dB bandwidth of the insertion loss is above 25GHz for both data paths and clock path. The performance is good enough for the PAM4 driver in this case.

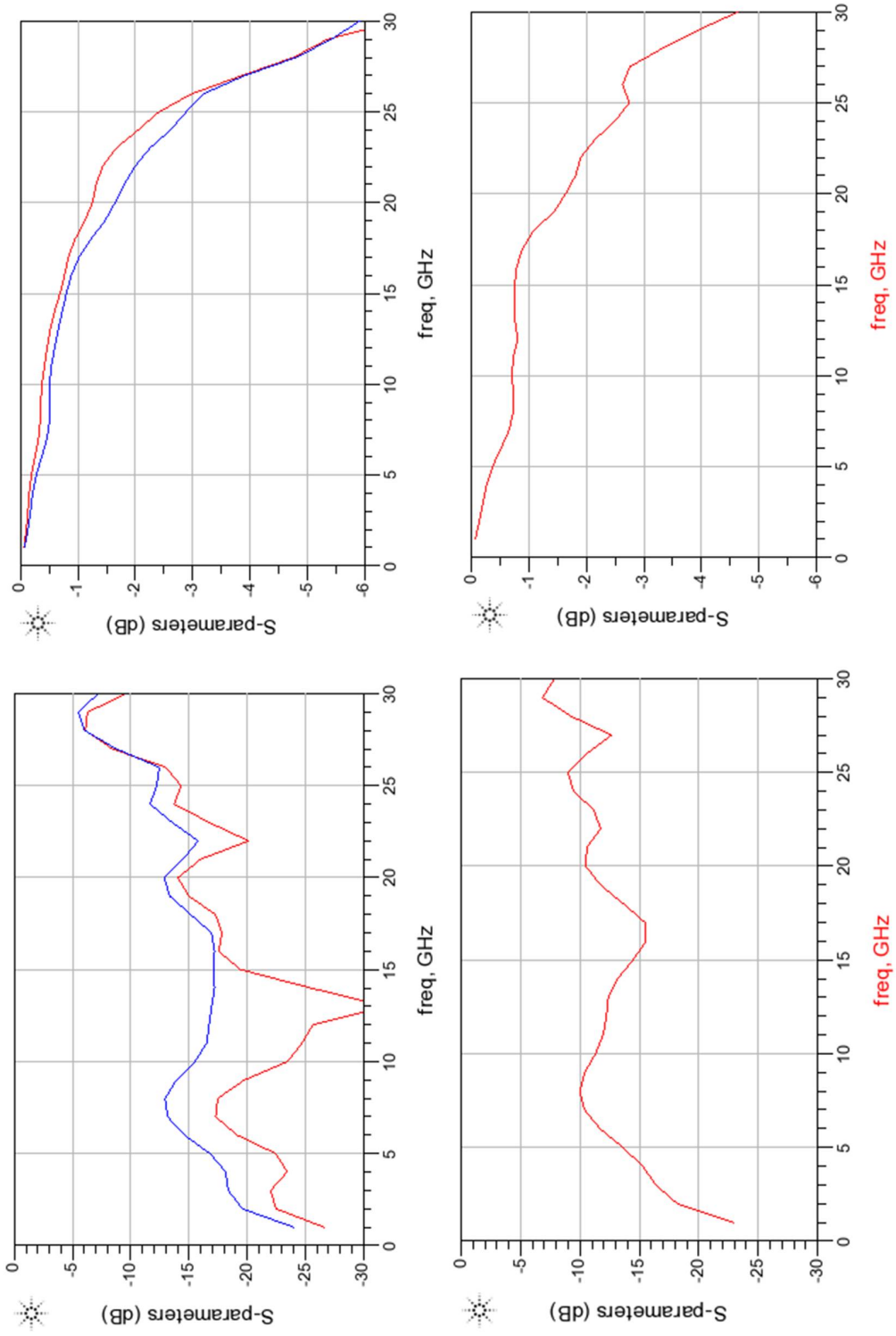


Figure 4.11: Simulation results of Ceramic and PCB, return loss (top left) and insertion loss (top right) of two data paths (blue and red), and return loss (bottom left) and insertion loss (bottom right) of clock path

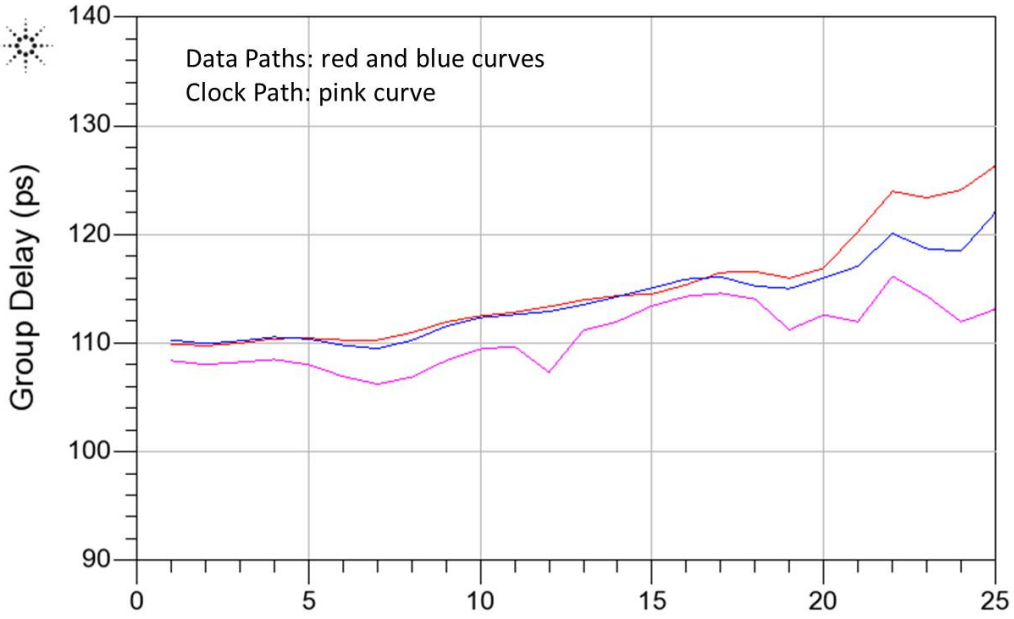


Figure 4.12: Group delay of Ceramic and PCB

According to the group delay, the delay difference between two data paths is less than 0.5ps from DC to 20GHz in Fig. 4.12. From 20GHz to 25GHz, the maximum delay difference is around 4ps, sufficiently low for 25Gb/s signaling. The group delay of clock path is also plotted in Fig. 4.12. Since the phase of the clock signal can be adjusted externally, the delay between clock signal and data paths shown in the co-simulation results does not impact the overall performance of the PAM-4 transmitter.

4.2.4 On-chip matching network

The design procedure for on-chip modified Butterworth low-pass filter is as follows. Firstly, the largest capacitance is identified on the chip which is the ESD and bondpad capacitance in this case, which act as one of the capacitors in the Butterworth filter, see Fig. 4.4(b). Secondly, a routing trace with the required amount of inductance to realize the equations shown in Fig. 4.4(b) is added. Of course this trace also routes the signal from the bondpads to the core circuitry. Thirdly, the routing trace is split into 3 paths and conducts the signal to each CML logic gate of the Gray coding circuits through this distribution network. The capacitance of each CML logic gate and the distribution network form the second capacitor in the Butterworth filter, see Fig. 4.4(b). Finally a 50Ω termination resistor and an extra capacitor are added to the distribution

Table 4.1: Input capacitance of gray coding CML gates

OR				AND				BUFF	
A	B	$\overline{A}$	$\overline{B}$	A	B	$\overline{A}$	$\overline{B}$	A	$\overline{A}$
$30fF$	$20fF$	$60fF$	$20fF$	$60fF$	$20fF$	$30fF$	$20fF$	$15fF$	$15fF$
D-ff									
CLK_P	$14fF$			$14fF$				$14fF$	
CLK_N	$14fF$			$14fF$				$14fF$	

network in order to match the modified Butterworth filter. The input signals (two differential data signals and one differential clock signal) are centralized by the impedance matching network and then split into three paths for CML OR gate, Buffer, and AND gate with following D flipflops respectively. By doing so, the layout for each data path is symmetrical and the delay can be well controlled.

In Fig. 4.13, the distribution network is shown as the part within the red dashed line, the other parts of the matching network are shown within the red solid line. In addition, the termination part (resistors and capacitor) is located within the blue line. As the distribution network and input capacitance of the gray coding CML gates form one of the capacitors of the modified Butterworth filter in Fig. 4.4(b), the capacitance of each CML gate and the distribution network needs to be characterized carefully. The input capacitance of each gray coding CML gate and the D flipflops are listed in Table 4.1 based on the design in previous chapter. Table 4.1 shows that the loading capacitance for each path is different. Data signals A and $\overline{A}$ have the highest load ($105fF$ each), the data signals B and $\overline{B}$ have $40fF$ each, and the clock signals' load is $42fF$ each.

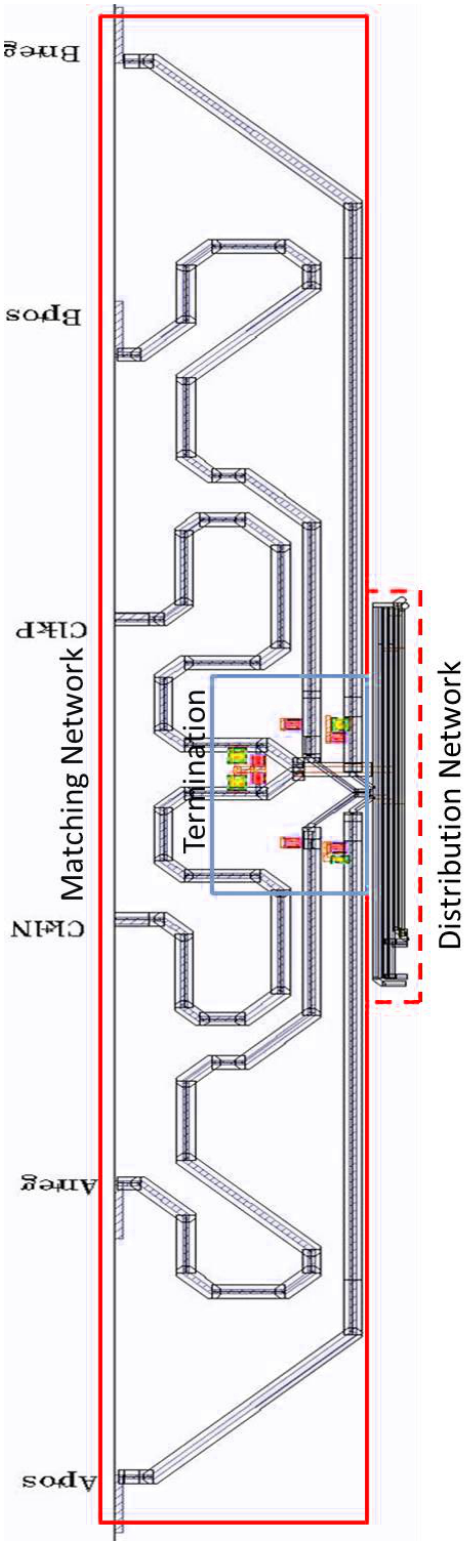


Figure 4.13: Layout of entire input matching network

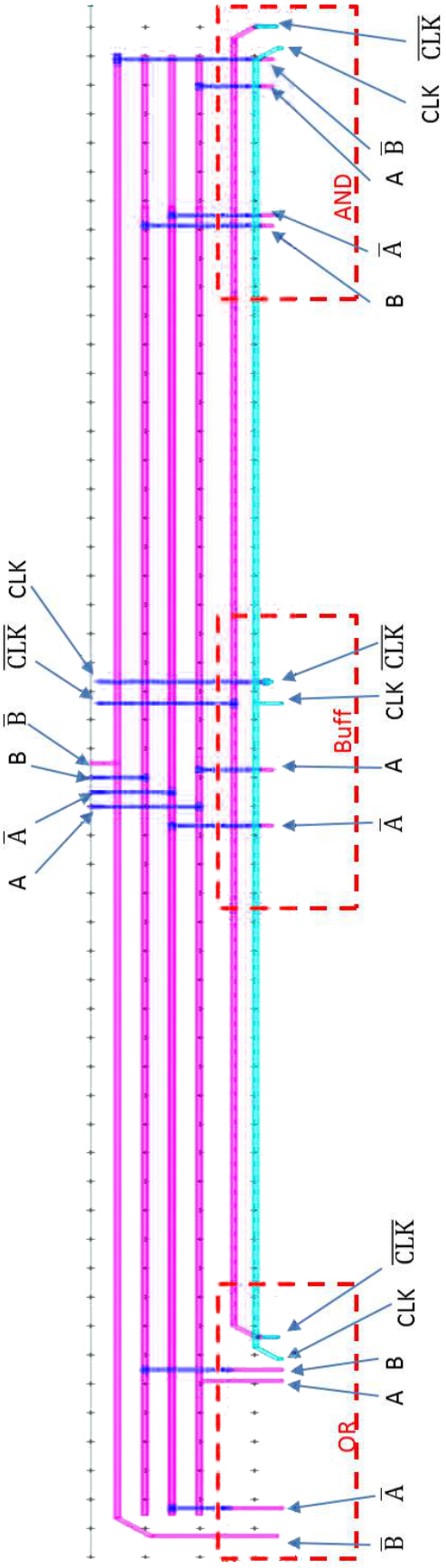


Figure 4.14: Connection of distribution network

The connections for each CML gate are demonstrated in Fig. 4.14. It also shows the layout of the distribution network, where the pink traces are realized using the 7^{th} metal layer; the dark blue traces are located at the 6^{th} metal layer; and the light blue traces are using the 5^{th} metal layer. The width of the routing traces is $0.5\mu m$ and the gap between two adjacent traces is around $2\mu m$; the total area is $260\mu m$ by $16\mu m$.

Since the capacitive load on each signal trace is different, the compensation capacitance with the 50Ω termination resistor for each path has to be trimmed individually. The metal-oxide-metal (MOM) capacitor has been chosen from the 65nm CMOS process design kits (PDK) to create the compensation capacitors, since the process variation of MOM capacitor is very small ($< 5\%$) [16]. For the clock signal paths in Fig. 4.15, the compensation capacitor is $130fF$ each bringing the total loading capacitance to $172fF$, which is close to the case plotted in Fig. 4.7.

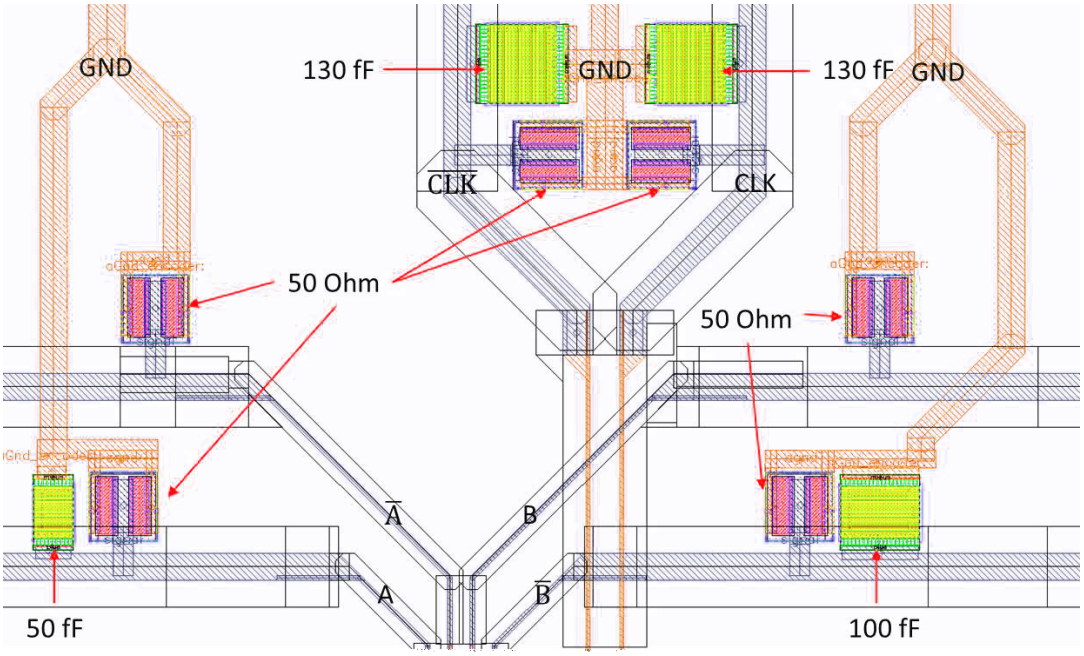


Figure 4.15: Termination of matching network

For data path A, the compensation capacitor is $50fF$. So, the total loading capacitance is $154fF$, which is also close to the case plotted as red and blue curves in Fig. 4.6. For the path $\overline{B}$, the compensation capacitor is $100fF$ and the total loading capacitance is $140fF$, close to the case plotted as red and blue curves in Fig. 4.6. For the network involving data paths $\overline{A}$ and B, the compensation capacitor is actually realized as the capacitance of the routing trace itself. Care has been taken to ensure that the length of each routing trace

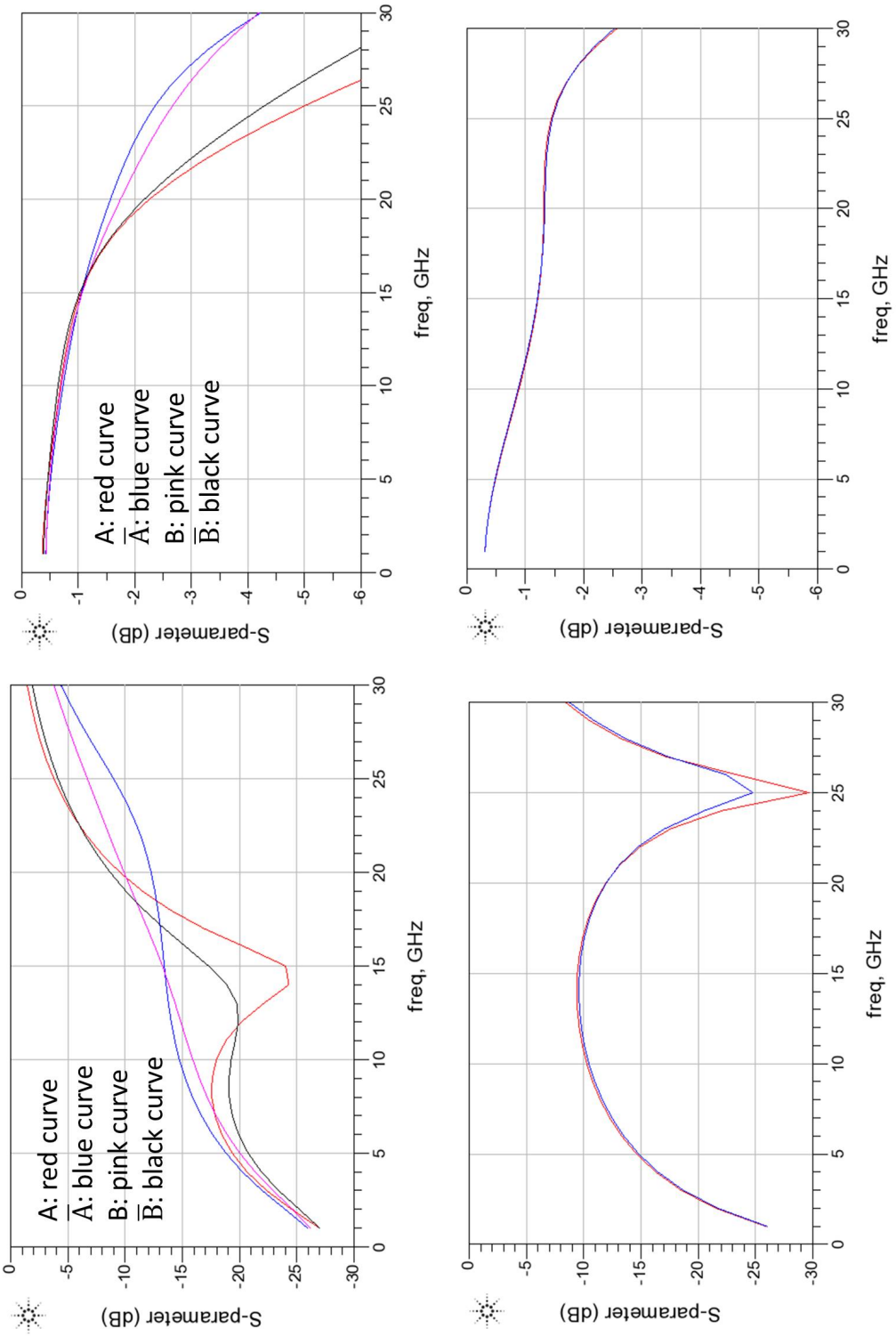


Figure 4.16: EM simulation results of modified Butterworth input matching network, return loss (top left) and insertion loss (top right) of data paths, and return loss (bottom left) and insertion loss (bottom right) of clock paths

is $\sim 500\mu m \pm 5\%$ variations, minimizing the group delay differences between each data path (from bondpads to termination area).

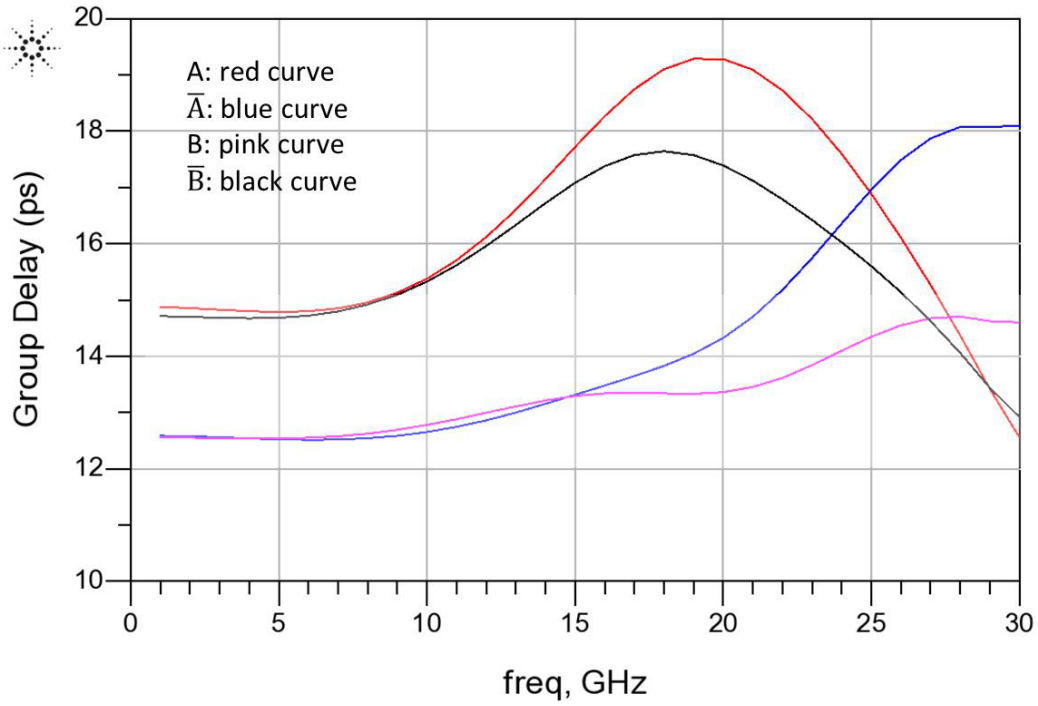


Figure 4.17: EM simulation results of group delay for data paths

The EM simulation results of the input matching network (Fig. 4.13) are plotted in Fig. 4.16. Better than -10dB return loss has been achieved from DC to 20GHz for both signal paths and clock paths. Regarding insertion loss, the -3 dB bandwidth is above 20 GHz for the data path. For the differential clock paths, the -3dB bandwidth is above 30GHz.

The group delays of the signal paths are plotted in Fig. 4.17. The maximum delay of all data paths across the entire bandwidth from DC to 20 GHz is around 6ps (at $\sim$20GHz) and the minimum delay is around 2.5ps (at low frequency range from DC to $\sim$12GHz) sufficiently small compared to the pulse width (40ps) at 25Gb/s.

The reference planes (50Ω ports) for the EM simulations cannot be located directly at the input of the logic gates and D flipflops due to the threeway split of the signal traces. For a final evaluation of the matching and distribution network, the S-parameters of entire structure (Fig. 4.13) simulated using the EM simulator are exported into Cadence to run a co-simulation with the gray coding CML logic gates and D flipflops (which contained postlayout extracted interconnect resistance and capacitance). The transient simulation results are

shown in Fig. 4.18:

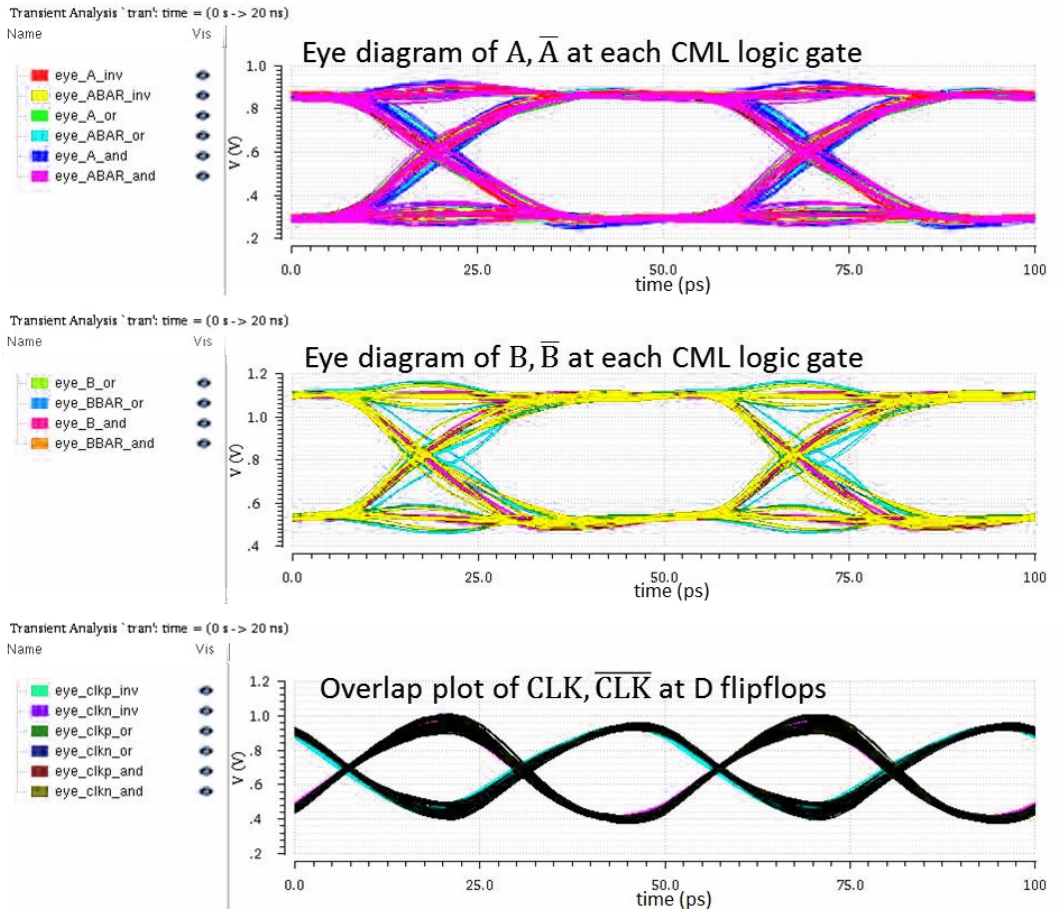


Figure 4.18: Transient simulation results of modified Butterworth matching network

Two differential 20Gb/s PRBS data and 20GHz differential signals are connected to the ports of Apos, Aneg, Bpos, Bneg, CLKN and CLKP (Fig. 4.13).And the outputs are connected to AND gate, OR gate, Buff gate, and D flipflops. The eye diagrams of Apos, Aneg and Bpos, Bneg at each logic gate are plotted as top and middle in Fig. 4.18 respectively. The maximum delay for Apos and Aneg at each logic gate is 6ps and the maximum delay for Bpos and Bneg is 8ps. The eye opening time is 28ps for both differential data paths, which is around 56% of the period and is sufficient for the D flipflop to retime without error. The delay difference between the differential data signals A and B to each gray coding logic gate can be measured by overlapping the eye diagrams for both signals with the same starting time and ending time.

In Fig. 4.19, the delay difference is 2.5ps, measured according to the data transition area of the eye diagrams. This corresponds well with the group delay plotted in Fig. 4.17. The plot in the bottom of Fig. 4.18 is the differential

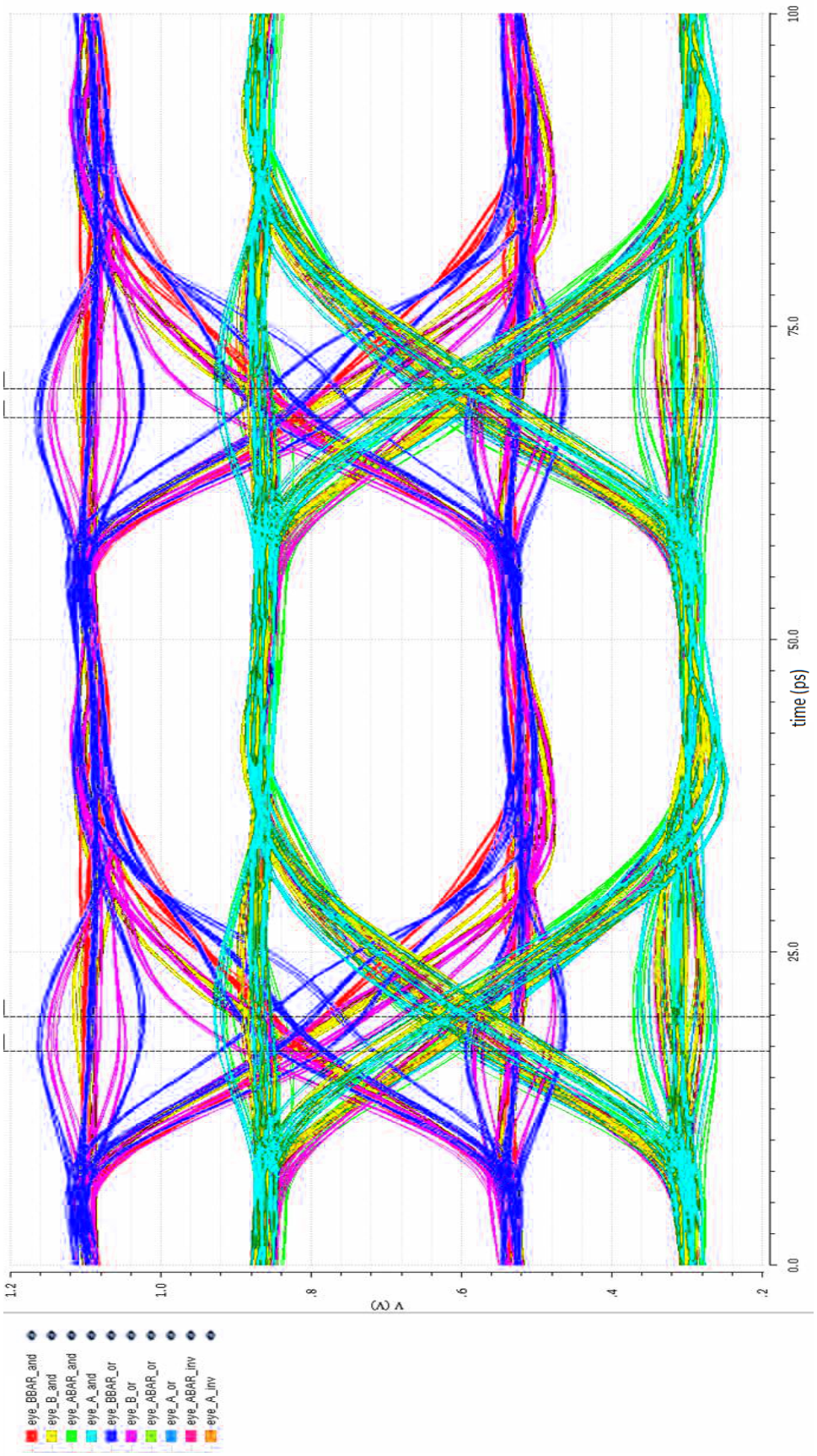


Figure 4.19: Transient simulation results of delay different between two differential datas

clock signals. The maximum delay difference of the clock signals between the D flipflops after the three logic gates is 3.5ps. Since there is an intrinsic 3.5ps delay of the clock signals among each D flipflop gates introduced by the matching network, the theoretical maximum time delay after the synchronization cannot be smaller than 3.5ps. From the previous chapter, it was indeed shown how the maximum jitter after the synchronization of D flipflops is 5ps.

4.3 Alternative approach: T-coil matching network

Another well-known solution to properly terminate high-speed signals is the T-coil impedance matching network, reported by Razavi's paper and shown in Fig.15 [38]. The T-coil is used to absorb the ESD capacitance: this structure has been shown to exhibit very good return loss characteristics over a large bandwidth. However the coupled inductors require a large chip area. In addition, they can only provide good return loss in the presence of the capacitance of the ESD diode: any residual capacitance from the bondpad and inductance from bondwires, flip-chip bumps and interconnect traces rapidly degrade the return loss of the T-coil structure.

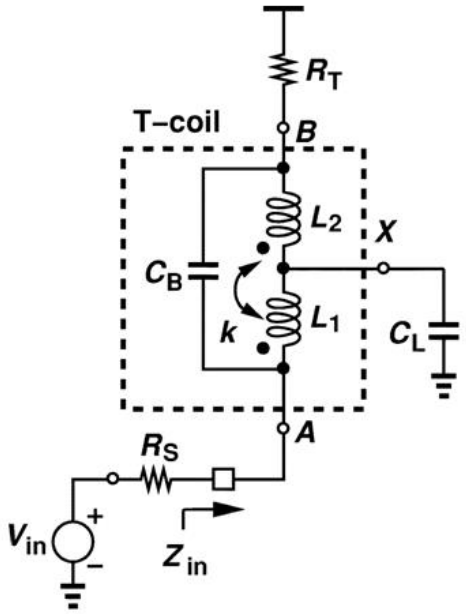


Figure 4.20: T-coil Network

T-coil networks consist of two coupled inductors L_1 and L_2 with coupling coefficient k and a shunt capacitor C_B. The input signal is applied to terminal A,

the termination resistor R_T is attached to the terminal B, and the load capacitor C_L (eg the capacitance of ESD protection diodes and the IO bondpad) is connected to terminal X. Intuitively, we recognize that L_1 and L_2 form a short between the input and R_T at low frequency. At high frequency when L_1 and L_2 have a high impedance, C_B shorts the input to R_T. Hence through proper design, the network will be a pure resistor across a large bandwidth and the input resistance is equal to R_T. It can be proven that the input impedance is purely resistive for all frequencies if the following conditions are true:

$$L_1 = L_2 = L = \frac{C_L R_T^2}{3} \tag{4.11}$$

$$C_B = \frac{C_L}{12} \tag{4.12}$$

$$M = \frac{L}{2} \tag{4.13}$$

One great advantage of this network is its symmetrical topology. The input signal can be applied to any of the nodes (A, B, or X) with minimum reflection and maximum output power. For example, the input is attached to node A in Fig. 4.20, and the broadband output can be obtained at either X or B. The input could also be connected to node X with the broadband output being either A or B. In addition, we could setup the input and output as A and B respectively and still maintain the broadband matching.

This concept has been applied to a real design. A 20Gb/s burst-mode transimpedance amplifier (TIA) designed by my colleagues for optical receiver is shown in Fig. 4.21, where two T-coils are design for the differential outputs. Although the design has been done in a 130nm SiGe BiCMOS technology, it can be readily re-used in 65nm CMOS technology since the metal stacks are quite similar (and better in 65nm CMOS due to more thick metal layers being available). An optical receiver was assembled by assembling the burst-mode TIA chip together with a photodectector into a butterfly module. The TIA chip is flip-chipped on an alumina ceramic carrier (see Fig. 5.4 in chapter 5). The interconnect between the differential output of the TIA and the module interface again needs to have minimum insertion loss and good return loss from DC up to 20GHz. T-coils were used here shown in Fig. 4.21: the two (one for positive phase output and one for negative phase output) T-coil broadband matching

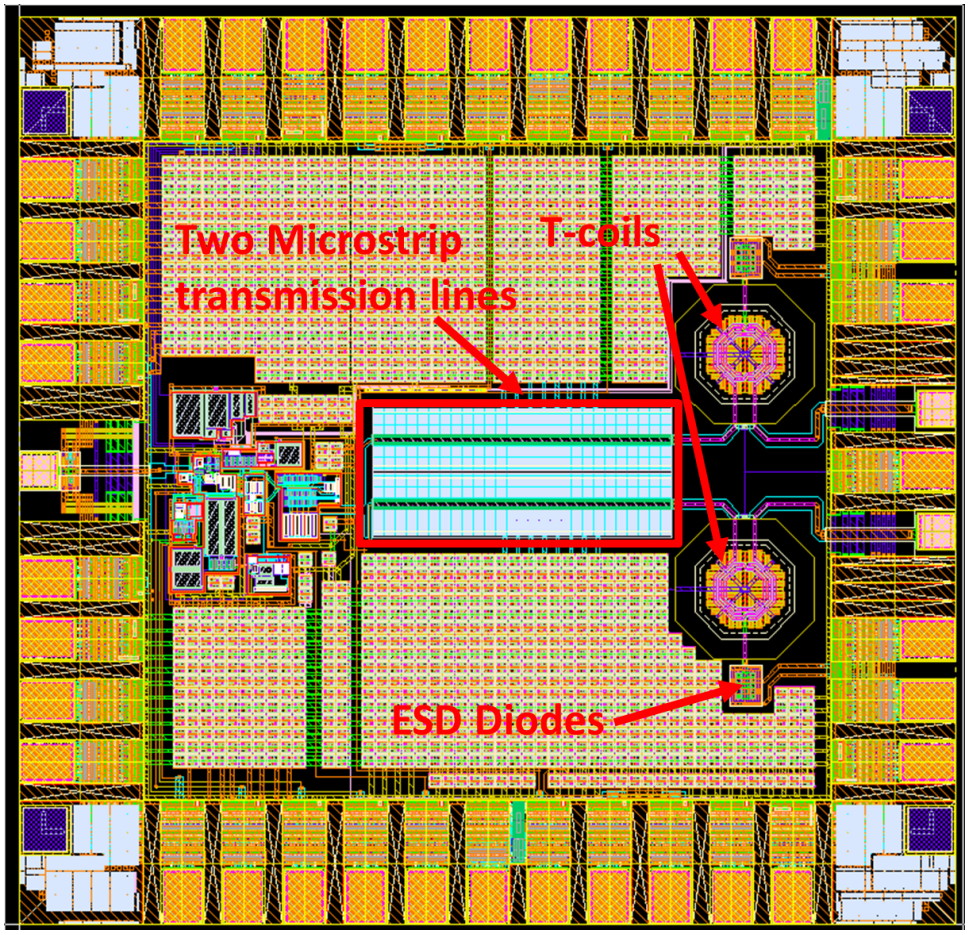


Figure 4.21: Layout of 25Gb/s Burst-mode TIA

networks can be seen in the middle right-hand side of the chip. Two microstrip transmission lines connect the TIA output (in the left middle of the chip) to the T-coils. The middle pins of the inductors are attached to the ESD diodes and their outputs are tied to the right hand side middle pins of the IO ring. The shunt capacitors are placed between the input and output of differential inductors. For this design, the ESD protection diodes had a capacitance of $310fF$; the parasitic capacitance of the flip chip bump was $60fF$.

The theoretical model of the interconnection circuitry is shown in Fig. 4.22. The output and input ports represent the input from the alumina test structure and the trans-impedance amplifier (TIA) output respectively. A $470pF$ decoupling cap is inserted in front of output port.

The simulation result of theoretical model is shown in Fig. 4.23. Although better than 10dB return loss up to 30GHz can be seen, note that the performance is significantly degraded comparing to the ideal T-coil matching behavior. The reason is the $60fF$ parasitic capacitance of the flip-chip bump.

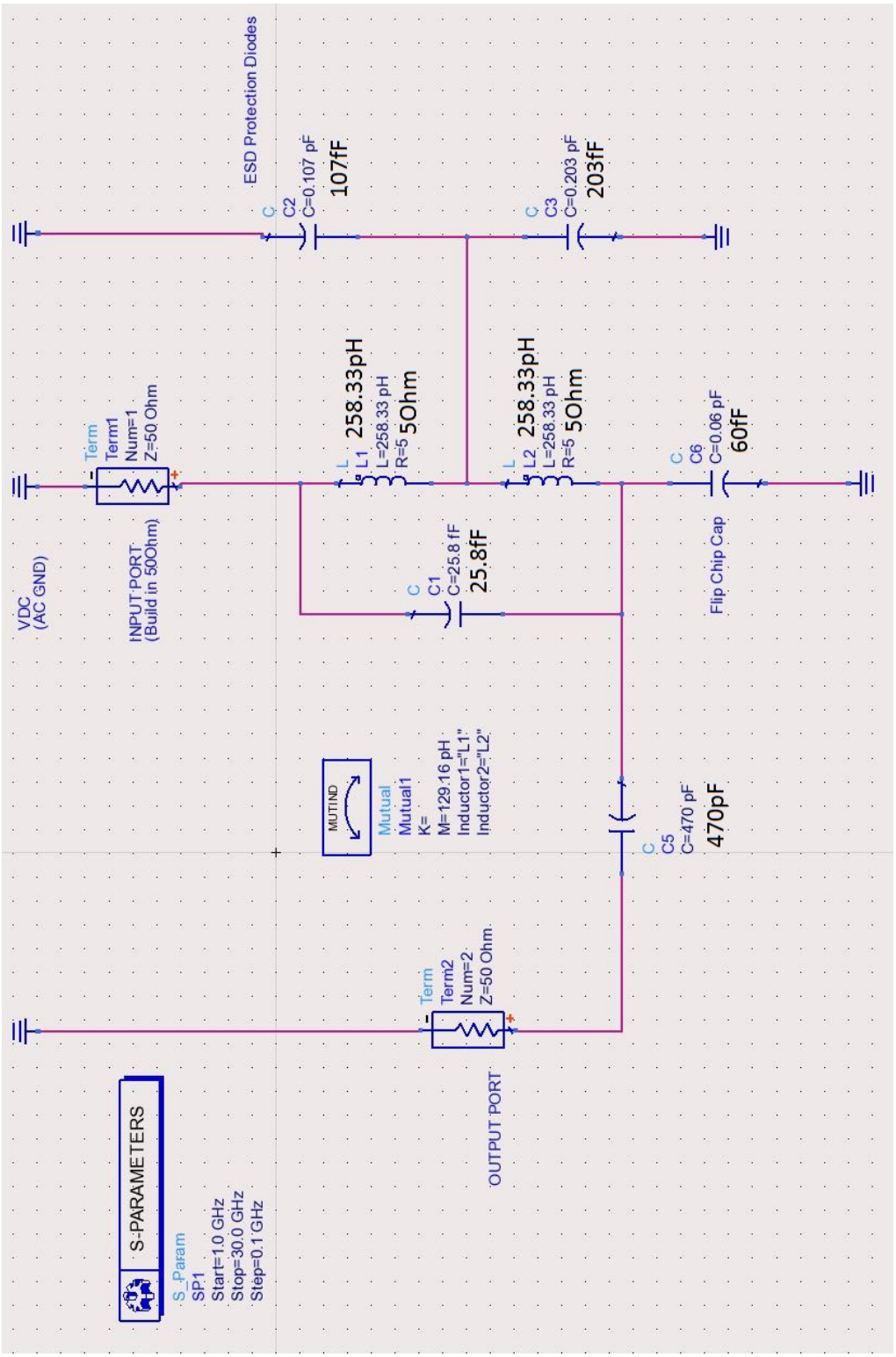


Figure 4.22: Theoretical model of broadband impedance matching network for 20Gb/s Burst-mode TIA

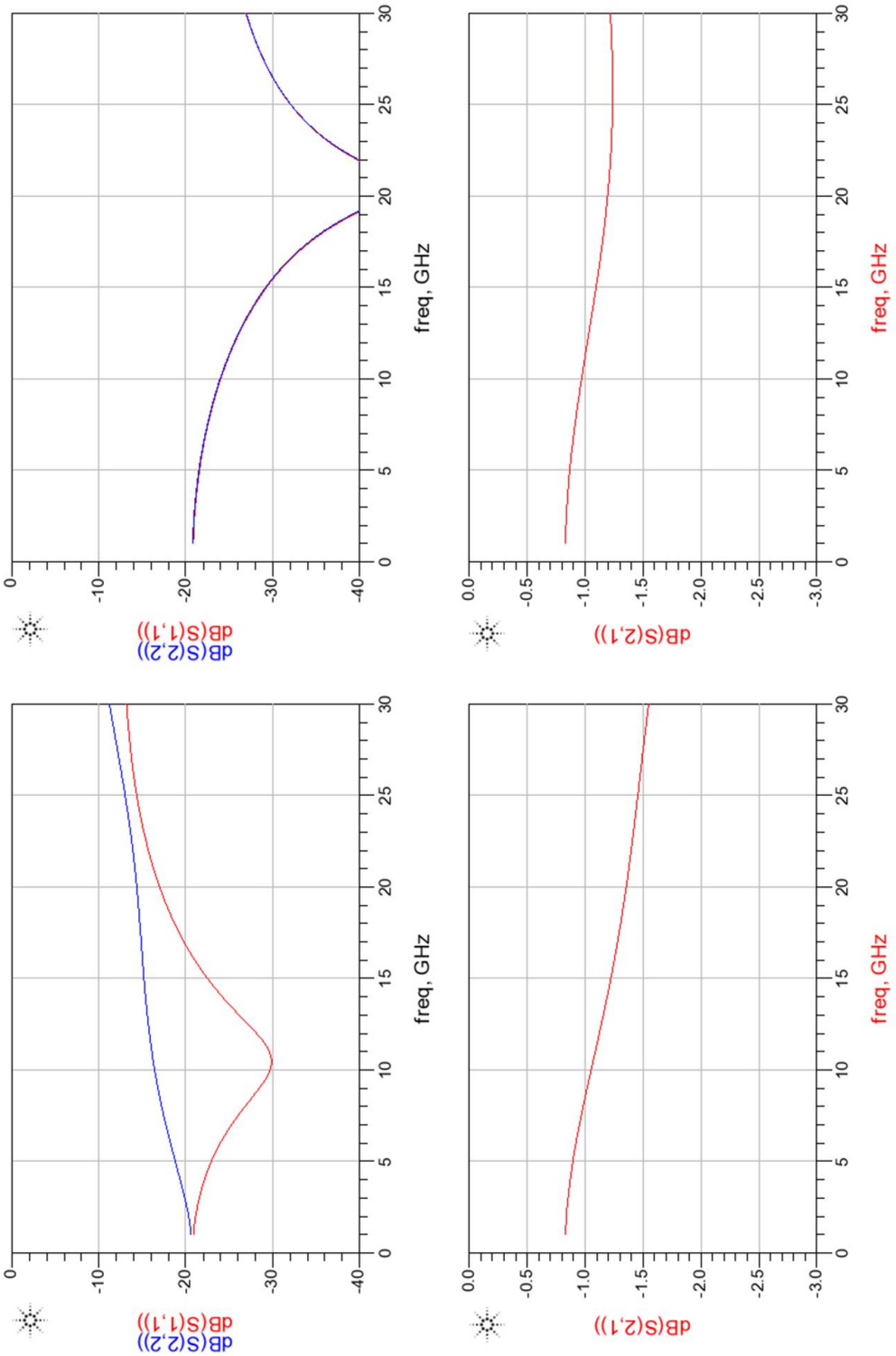


Figure 4.23: Simulation Results of theoretical model of T-coil Matching Network with flip chip cap (top left and bottom left) and without flip chip cap (top right and bottom right)

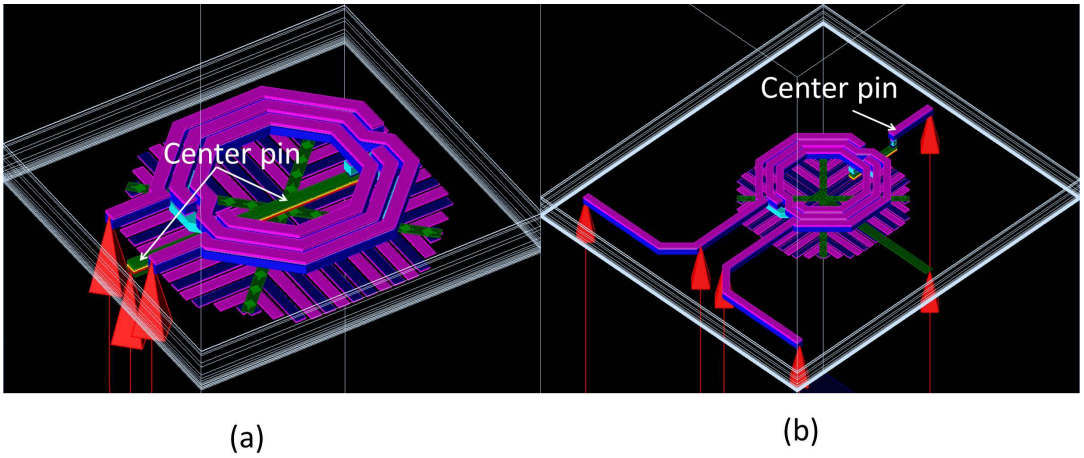


Figure 4.24: 3D Layout View of Differential Inductor AKA T-coil (a) original (b) modified

The T-coil has been realized as an inductor with 3 turns, $55\mu m$ diameter, $5\mu m$ metal trace width and a $10\mu m$ wide metal trace for the centre tap. The 3D view of the differential inductor is shown in Fig. 4.24 (a). Note how the center pin travels across the center of the differential inductor, which means the electromagnetic (EM) field projects into the surface of the center tap and generates eddy currents which increase the impedance for higher frequencies. This is fine for the applications such as a VCO, because the middle pin is always attached to an AC ground, usually the DC supply voltage. Hence the impedance variation of the middle connection is not important for the signal. However, in the T-coil structure the center pin is part of the signal path. Therefore, the center pin was routed to the other side of the inductor to avoid the interference with the center EM field as shown in Fig. 4.24(b). The EM coupling between the signal pins and the ground shield becomes important if we extend the signal pin's length to reach the output node of TIA and pad rings. In traditional applications of differential inductors there is negligible coupling between the signal pins and the ground shield, however for the T-coil matching network it may be more common. To reduce such coupling, the ground connection is turned 90 degrees away from the signal pins as shown in Fig. 4.24(b).

The differential inductor (T-coil) shown in Fig. 4.24(b) has been characterized using an EM simulator. An S-parameter model was generated and replaced the $L1$, $L2$ and $C1$ in the theoretical model in Fig. 4.22. The new setup is shown in Fig. 4.25. The shunt capacitor C_B in Fig. 4.25 is now $40fF$, larger than the capacitor in Fig. 4.22, $25.8fF$. The main reason is the extension of the signal pins. From the derivation of the inductance per unit length at the beginning of

this chapter, $\sim 1pH/\mu m$: there is approximately $300\mu m$ extra length of metal trace involved into the matching network. Therefore, we need to increase the bridge capacitance to compensate for the additional inductance.

The simulation results in Fig.4.26 indicate that the parasitic capacitor of the flip chip technology degrades the return loss by more than 10dB, while it has less impact on the insertion loss (bandwidth). With the parasitic capacitance, -20dB and -13dB return loss are achieved at 12.5GHz and 25GHz respectively in Fig. 4.26(a), well within the requirements for a 20Gb/s signal.

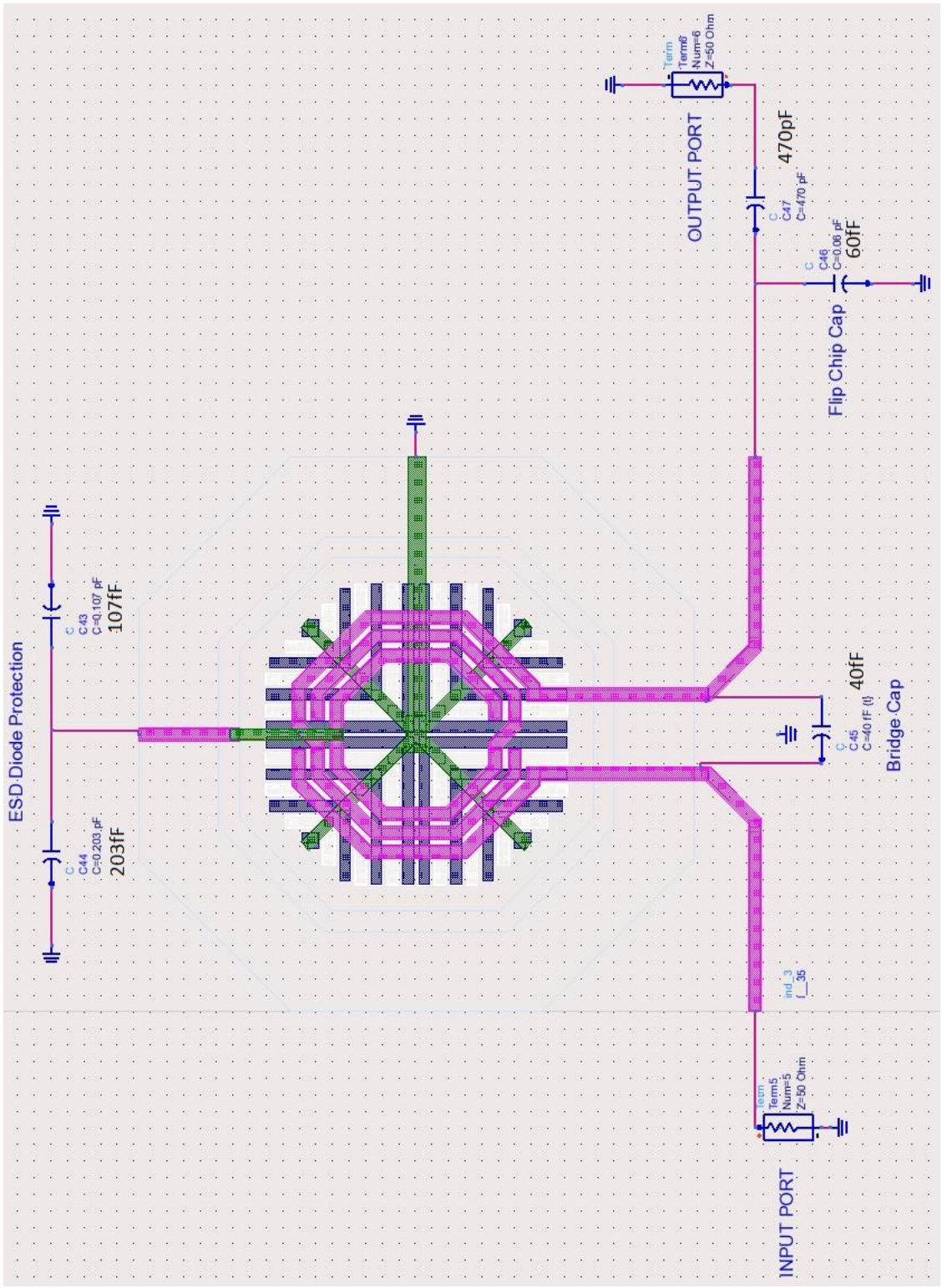


Figure 4.25: Simulation setup of matching network with EM model of differential inductor

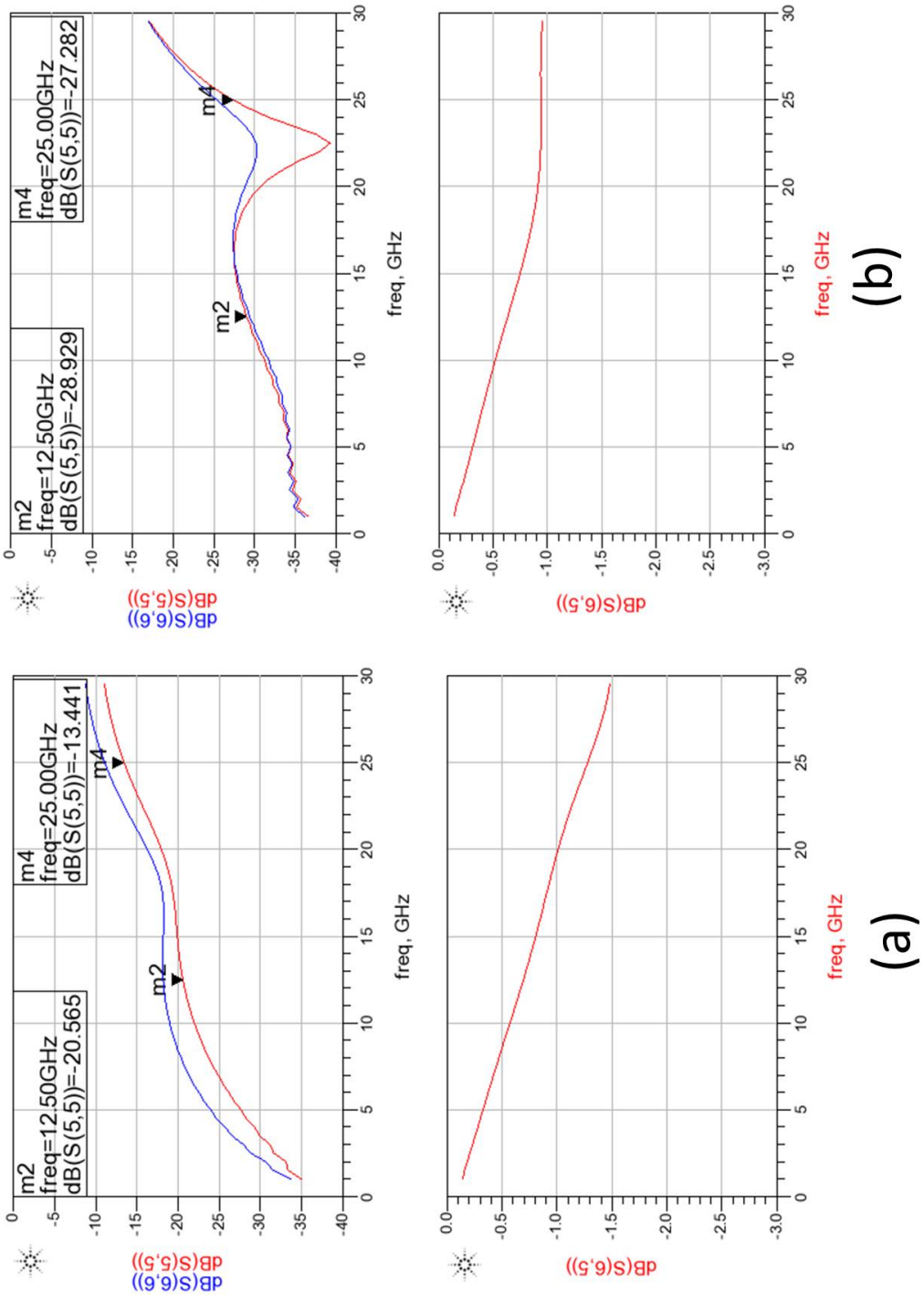


Figure 4.26: Simulation results of theoretical model of T-coil matching network (a) with flip chip cap (b) without flip chip cap

4.4 Comparison

The total chip area of the modified Butterworth matching network is $1040\mu m$ by $135\mu m$ for the PAM4 driver IC including the distribution network. The T-coils' area is $700\mu m$ by $240\mu m$ with two microstrip lines which accounts for $200\mu m$ by $470\mu m$. The area per IO for the modified Butterworth matching network is $2.34 \times 10^4 \mu m^2$. For the T-coils matching network, the area per IO is $8.4 \times 10^4 \mu m^2$ (with $4.7 \times 10^4 \mu m^2$ for the microstrip line, which is excluded however from the comparison, to make it a fair comparison). Therefore, the modified Butterworth matching network saves 72% chip area compared to the T-coil in terms of area per signal trace.

However, T-coils matching have better performance than the modified Butterworth matching as can be seen in Fig. 4.16 and Fig. 4.26. The bandwidth for which better than -10dB return loss is achieved ranges from DC to 25GHz for the T-coils, but only from DC to 20GHz for the modified Butterworth approach. According to the insertion loss, the T-coils bandwidth is beyond 30GHz, while only 22GHz is achieved for the modified Butterworth approach. Hence, there is a trade-off between chip area per IO and performance. The T-coils has better performance than the modified Butterworth one, but it consumes too much area to be of practical use if more than a few high-speed IOs are required.

4.5 Summary

In this chapter, the microwave filter theory based broadband matching network is proposed and applied for PAM4 modulator. The traditional T-coil matching network is also designed and applied to the burst mode optical receiver as the comparsion. The T-coils and the microwave filter have similar performance from DC upto 20GHz. And the T-coils is superior than the microwave filter from 20GHz to 30GHz. However, the microwave filter scheme uses less chip area comparing to the T-coils.

Chapter 5

Measurement Result and analysis

In this Chapter, the measurement results and analysis of the realized PAM-4 transmitter consisting of a Lumped Silicon Photonic Mach-Zehnder Modulator (L-MZM) and PAM4 driver chip are presented. First the assembly of the PAM-4 transmitter is discussed in detail, as it plays such a critical role in the performance of the device. Next, the measurement results themselves are presented and analyzed in detail.

5.1 Packaging and assembly of PAM4 modulator

The PAM-4 transmitter consists mainly of the Silicon Photonic modulator integrated into an SOI chip on one hand, and the CMOS driver circuit on the other hand. The overall assembly of the PAM-4 transmitter is driven by three main criteria. Firstly, any interconnect parasitics (whether capacitive, resistive or inductive) on the output of the driver will directly impact its performance (in particular reduce the eye diagram due to bandwidth limitations combined with ringing): hence any assembly needs to minimize the parasitics. Secondly, the high-speed inputs of the PAM-4 transmitter need to have a matched impedance environment with low reflections (good return loss) and sufficient bandwidth (negligible insertion loss all the way from the RF connectors used to connect the device to the test equipment down to the input of the logic gates, see Chapter 3 for a detailed description of the CMOS driver chip). It requires careful consideration of this interconnect, for example it has to keep the length of any bondwires as short as possible or using ribbon wires. A more fundamental treatment of how to design this interconnect has been already presented in Chapter

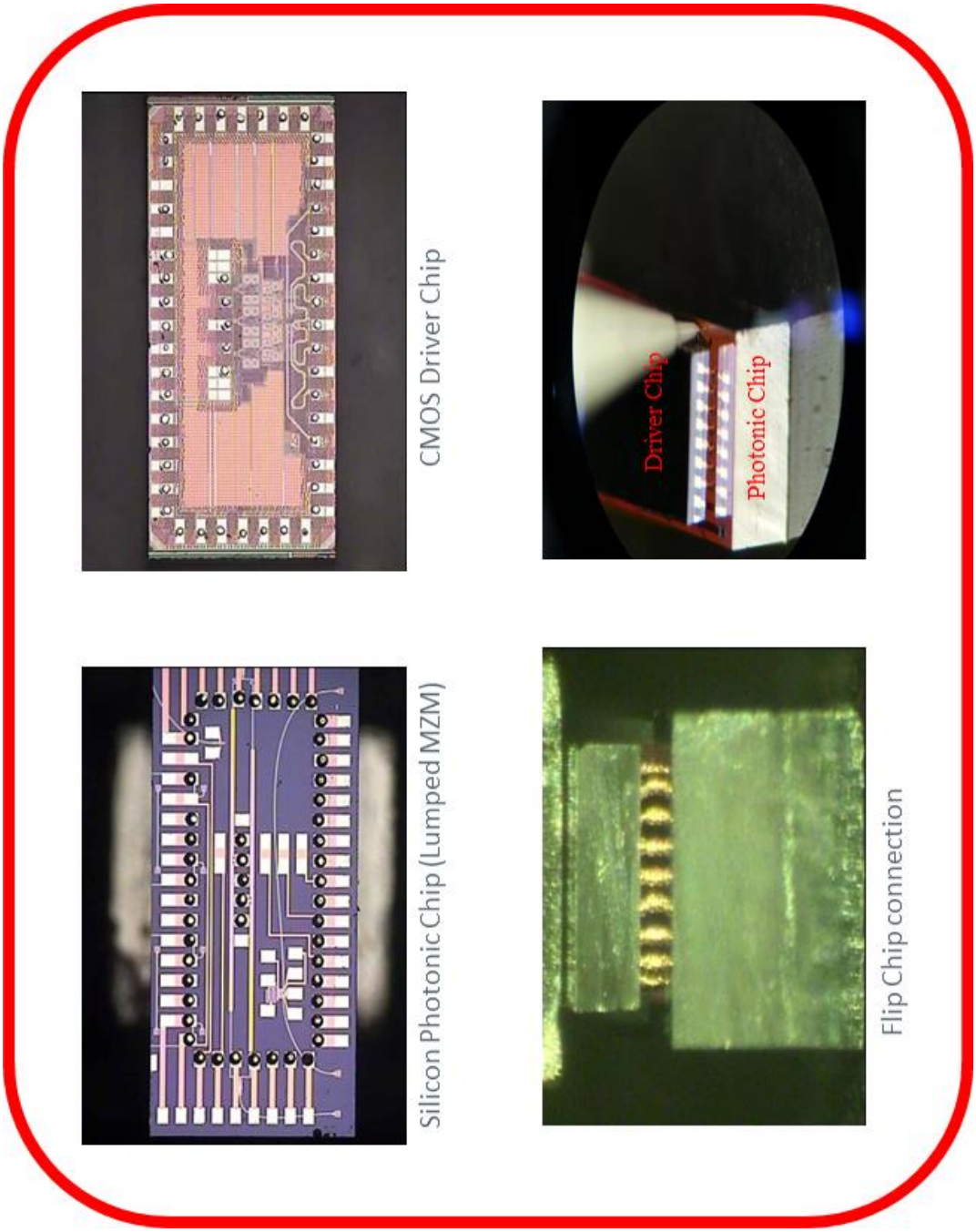


Figure 5.1: Connection between Lumped MZM and CMOS driver

4. Finally, the alignment of the optical fiber with the grating couplers needs to be considered. The optical fiber alignment is outside the scope of this thesis. However, the interested reader is referred to [23].

To minimize the parasitic between the Silicon Photonic modulator and the CMOS driver chip, it was decided to use a 3D stacked approach whereby the CMOS driver is flip-chipped on top of the Silicon Photonic chip with the modulator. The assembly of the module itself was done by the Photonic Packaging Group in Tyndall. Fig. 5.1 shows a number of details. The Silicon Photonic chip is shown in top-left of Fig. 5.1, and the CMOS driver in top-right of Fig. 5.1. The Lumped MZM modulator is located in the middle of the Silicon Photonic chip. Micro-bump (diameter $50\mu m$) solder balls have been placed on all contact pads. The flip-chip process is using laser assisted solder jetting. The same type of solder balls have been applied on the contact pads of the CMOS driver chip as well, see top-right of Fig. 5.1. This was mainly done to be able to properly contact the aluminum pads on the CMOS driver chip. The CMOS chip is then compressed onto the Silicon Photonic IC shown in the bottom of Fig. 5.1. All the high speed signals and DC power supplies are transferred through the IO ring of the Silicon Photonic IC.

After the flip-chip process, the stacked driver chip and modulator chip are placed on a metal (CoVar for thermal and mechanical stability) sub-mount and connected to the PCB and ceramic interposer as shown in Fig. 5.2. The reason to use such combination of a PCB and ceramic interposer (rather than a single PCB) is that very small (value: $100\mu m$) pitch is required for the connections at the edge of the Silicon Photonic chip. The spacing and edges need to be controlled to a few micro-meters to ensure the target characteristic impedance is met. Such pitches and accuracy are not readily achievable using even advanced PCB technology, but are however readily achievable using thin film ceramic carriers. A single ceramic interposer (replacing the PCB) would of course also be possible however this would be extremely expensive. Gold bondwires with 18um diameter are used to bond the contact pads of the silicon photonic chip to the pads of the ceramic interposer for the high speed inputs, and bond the contact pads of the silicon photonic chip to relevant pads on the PCB for the DC supplies. The PCB itself is a 4-layer PCB, combining FR4 as main carrier and Rogers RO4035 for the high-speed transmission lines. The impact of the bondwires on signal integrity and how to absorb these into matched connections have been covered in Chapter 4. The 50Ω co-planar wave guides (CPWG) were used for both the ceramic interposer and the Rogers PCB. The ribbon bondwires

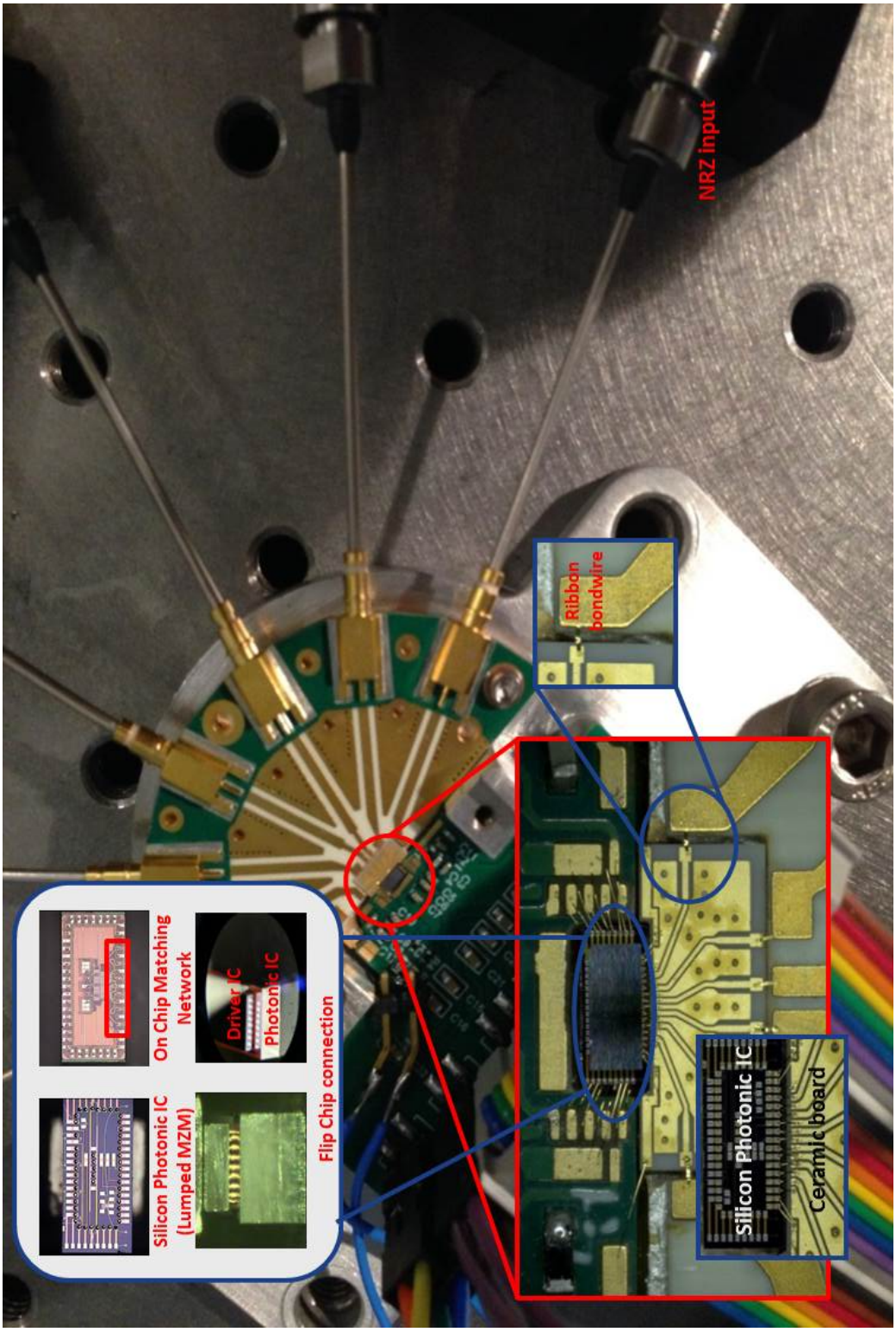


Figure 5.2: wirebonding of PAM4 modulator

have been applied to connect between roger PCB and ceramic interposer.

After the assembly and flip-chip operation described above, the next step in the creation of the PAM-4 module is the alignment of the input and output optical fibers, which will couple the light of a continuous-wave (CW) laser into the Lumped MZM on the Silicon Photonic IC, and the PAM-4 modulated signal back out again. In Fig. 5.3, two optical fibers (white wires) are attached to two holders, machined from a silicon wafer. The holders have been glued and UV cured on the metal arms such that the angle between the length axis of the optical fibers and grating couplers on the Silicon Photonic IC are optimized for maximum optical power transfer. The resulting PAM4 transmitter has been fixed on a metal sub-mount as shown in Fig. 5.3.

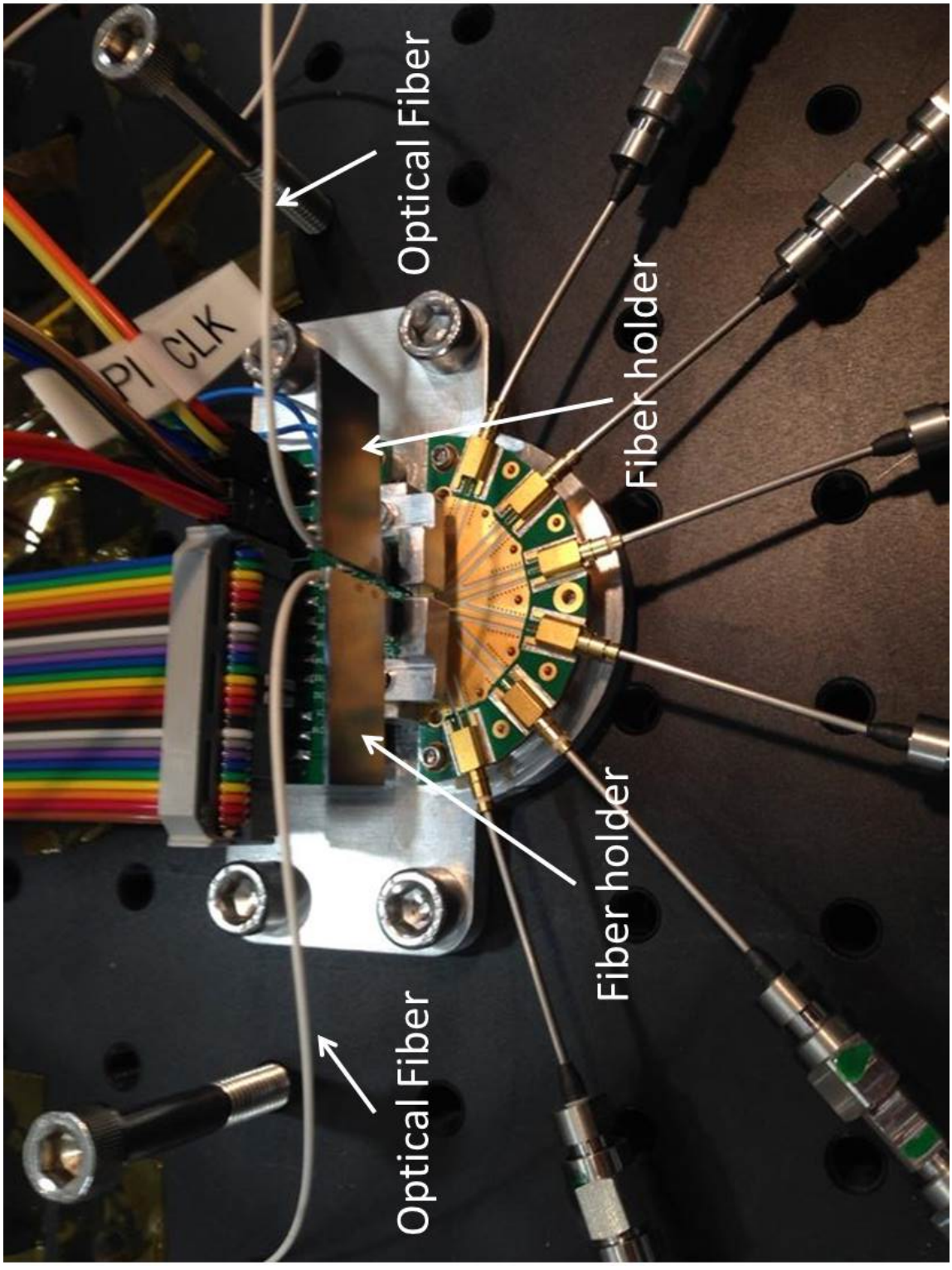


Figure 5.3: Full package of PAM4 modulator

5.2 Measurement of Broadband matching network

As explained in Chapter 4, two different kinds of broadband matching networks have been realized to facilitate high-speed IO: one approach is based on microwave filter theory and the other one is T-coil matching. The realized assemblies for both the PAM-4 transmitter (using microwave filter theory to design the broadband interconnect) and the linear burst mode trans-impedance amplifier (using T-coil matching for the broadband interconnect) are shown in Fig. 5.3 and Fig. 5.4 respectively.

For the PAM-4 modulator (shown in Fig. 5.2), it can be seen how the high-speed signals are transported from the RF connectors over a printed circuit board (PCB) and a ceramic onto the Silicon Photonic chip (with Mach-Zehnder modulator). As explained above, the driver IC is flip-chipped on top of the Silicon Photonic chip. The signal is carried using a grounded coplanar waveguides (CPWG) over the PCB, and uses a CPWG and a microstrip line over the ceramic to the Silicon Photonic chip. For the ceramic interposer shown in Fig. 5.2, at the top edge of the interposer, the pitch of the CPWG is matched with the pitch of the contact pads on the silicon photonic IC. Therefore, the length for the wire bonding connections has been minimized. On the ceramic interposer, the width of signal trace and signal-ground gap has been increased simultaneously to prepare the connection between ceramic interposer and PCB. However the characteristic impedance of the CPWG does not change. This is one advantage of CPWG structure. At the end of the CPWG (close to the bottom edge of the ceramic board), the microstrip line structure has been applied in order to provide enough space for the wire-bonding connection between the ceramic and PCB. The ribbon bond-wires have been applied to minimize the inductance and fit into the model shown in Fig. 4.10 in Chapter 4.

The burst-mode TIA (shown in Fig. 5.4) was flip-chipped onto a ceramic substrate inside a butterfly package. The differential RF signals are transported from the burst-mode TIA outputs via CPWG's on the ceramic carrier to MSMP connectors on the butterfly package.

The Vector Network Analyzer (VNA) has been used to measure the return loss (S_{11}) for the matching network. The VNA has to be calibrated before the measurement. The main purpose of calibration is to de-embed the connection cables between the ports of VNA and the RF connectors of the package. This process has been done through the Electronic Calibration Module (Agilent N4694-

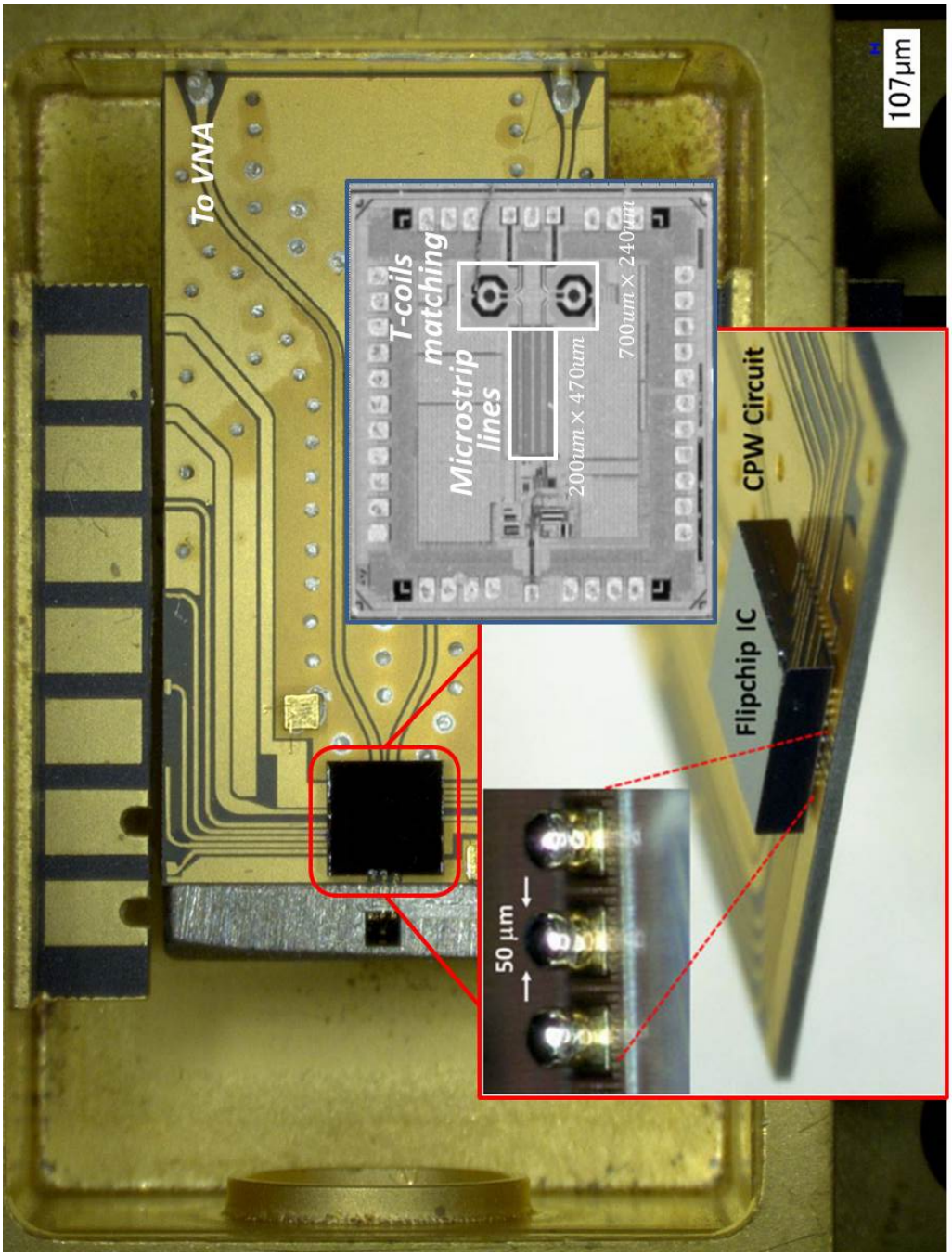


Figure 5.4: Package View of 25Gb/s Burst-mode TIA

60001). The measured return losses for the PAM-4 transmitter are shown in Fig. 5.5(a) and (b). The return loss is better than ∼10dB till 25GHz, rising up to 9dB at 18GHz, which is good enough for the PAM4 driver IC. For the clock input Fig. 5.5(b), an intentional (see Fig. 4.16) resonance can be observed at 25 GHz. Unfortunately, the location of this resonance is detuned from its design value, which was attributed to a difference between the actual bondwire inductance and its design value due to the variation of packaging process, as well as unavoidable process variations of the on-chip capacitors. Nevertheless, the return loss for clock inputs is better than ∼8dB till 20GHz, sufficient for our needs.

The return loss of the burst-mode TIA module was also measured; its return loss is shown in Fig. 5.5(a) (red traces). The 10dB return loss bandwidth is now as high as 30dB, underlining the superior performance of the T-coil matching structures compared to the microwave filter approach. However, the required chip-area per signal-path for the T-coil matching is $8.4 \times 10^{-4} \mu m^2$ compared to only $2.34 \times 10^{-4} \mu m^2$ for the proposed microwave filter approach, which means 70% expensive chip area has been saved.

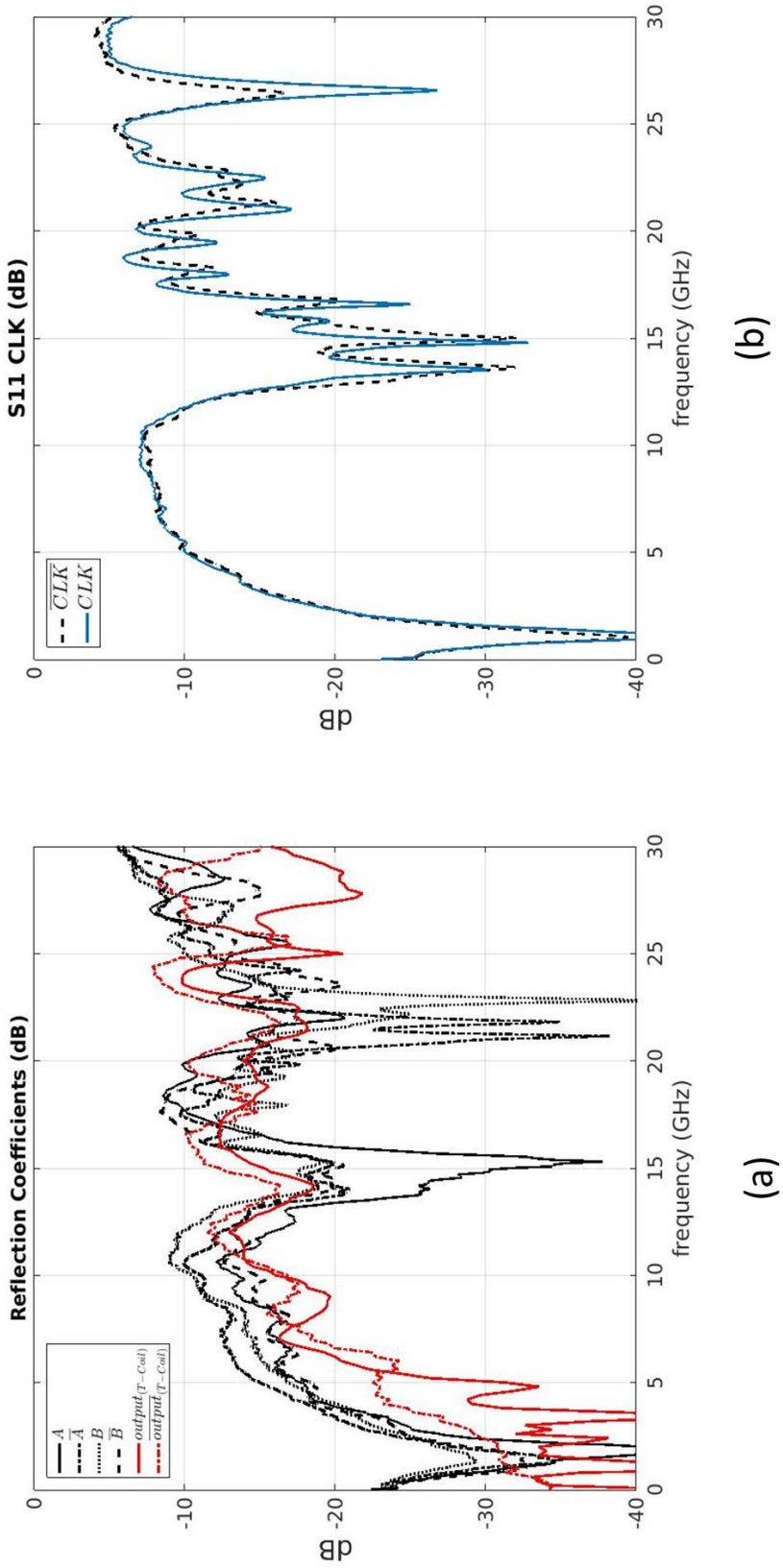


Figure 5.5: measurement results of broadband matching networks for (a) data signal paths and (b) clock signal path

5.3 Characterization of Lumped MZM

To better understand the performance of the complete PAM-4 transmitter, first the lumped MZM was characterized in terms of its DC transfer function as well as its high-frequency behavior. Two lumped MZMs have been characterized: firstly the DC-transfer curve on the lumped MZM assembled with the driver chip was measured. A second standalone device was also used to measure the electro-optical frequency transfer (bandwidth).

In the first step to evaluate the DC optical transfer function, the light from a CW laser (Agilent 8163B Lightwave Multimeter with built in Fabry Peroit Laser) is conducted into the lumped MZM using single-mode fibre coupled to the on-chip grating coupler. A polarization controller was used to align the polarization of the laser light with the preferred TE polarization of the grating coupler. For the initial measurement, no dc bias was applied to any of the MZM electrodes. The input optical power was set to 0dBm. For 0V bias voltage on both arms, the optical output power is -15dBm, measured using an optical power meter. Based on [20], the insertion loss of each grating coupler is 2.5dB and the optical loss of the MZM phase shifters is 3dB/mm. The Lumped MZM in top-left of Fig. 5.1 consists of two parallel phase shifters with a length of 1.5mm each. Hence, the total optical loss for the device is 12dB including the loss of the optical waveguide for the interconnection between the grating couplers and the lumped MZM. As the device is naturally (hence without any DC bias) operated in its quadrature point (based on Chapter 2), an additional 3 dB modulation loss should be added. Therefore, the total optical loss is 15dB which matches well with the measured result.

$$P_{optical} = |T_E(V_1, V_2)|^2 = \cos^2\left[\frac{\pi}{2} \times \left(\frac{V_1 - V_2 - V_{DCbias}}{8V}\right) - \frac{0.95 \times \pi}{4}\right] \quad (5.1)$$

Next, the DC bias voltages on both electrodes of the lumped MZM were swept and the optical output power was measured. The results are showing as the red curves in Fig. 5.6(a)(b). The output optical power has been measured by fixing the voltage of one arm and sweeping the DC bias voltage of the other arm. As the breakdown voltage of the on-chip capacitors on the driver chip is 4V, the maximum applied bias voltage was also limited to 4V. The normalized transfer function (5.1) of the Lumped-MZM has been fitted to the measured transfer

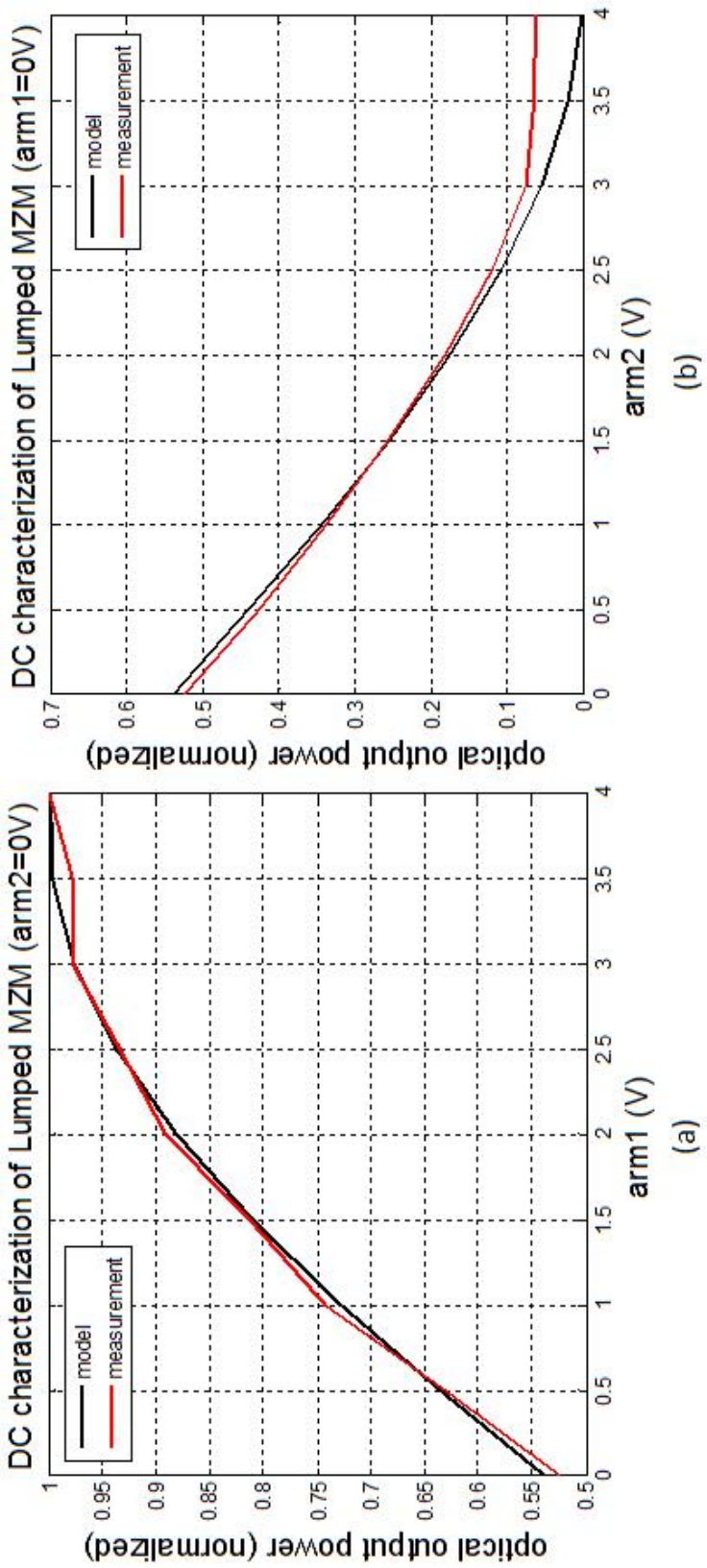


Figure 5.6: DC characterization of Lumped-MZM by sweeping voltage for (a) arm1 and (b) arm2

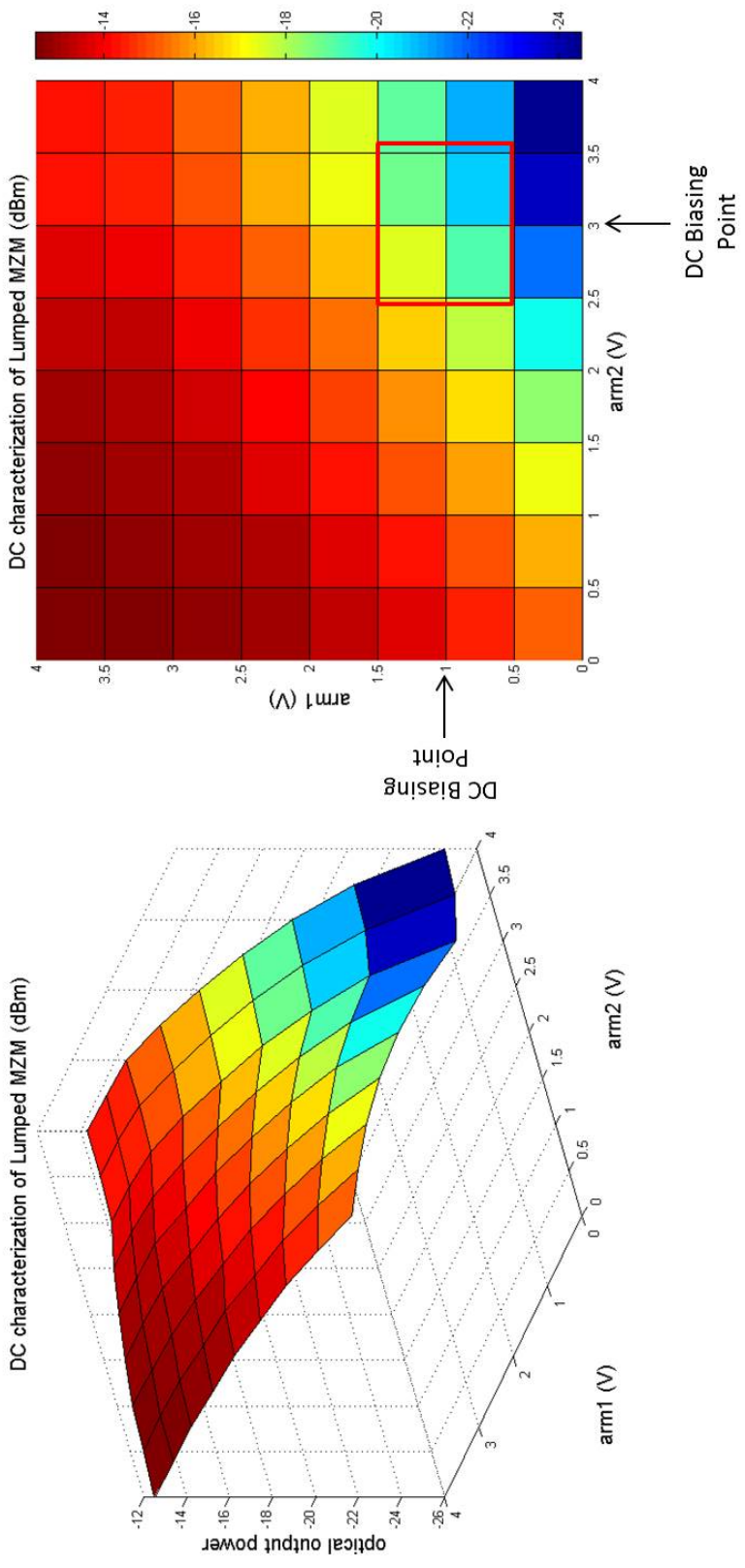


Figure 5.7: Operation point of lumped MZM

curve, and is plotted as the black curve in Fig. 5.6(a)(b). The 90 degree phase shift introduced in Chapter 2 has been achieved. The measurement result also shows that V_π of Lumped MZM is around 8V. By sweeping the DC bias voltage for both arms of the Lumped MZM, the 3D plot of the output optical power versus the biasing voltages has been plotted in the left part of Fig. 5.7.

As explained in Chapter 2, the asymmetrical Lumped-MZM needs to be biased below its quadrature point to achieve better extinction ratio. Here, and for the remaining experimental results, the DC bias voltages have been chosen as 1V and 3V for the two MZM arms respectively. Since the RF swing of the PAM4 signals generated by the driver is 1V for both arms, the "operating area" of the lumped MZM is within the red rectangle of the right part of Fig. 5.7. The achieved extinction ratio (ER) can be calculated based on (5.1) as following.

$$P_{optical} = \cos^2\left[\frac{\pi}{2} \times \left(\frac{(V_{RF1} + 1V) - (V_{RF2} + 3V) - V_{DCbias}}{8V}\right) - \frac{0.95 \times \pi}{4}\right] \tag{5.2}$$

$$P_{optical} = \cos^2\left[\frac{\pi}{2} \times \left(\frac{V_{RF1} - V_{RF2}}{8V}\right) - \frac{\pi}{8} - \frac{0.95 \times \pi}{4}\right] \tag{5.3}$$

$$P_{optical} = \cos^2\left[\frac{\pi}{2} \times \left(\frac{V_{RF1} - V_{RF2}}{8V}\right) - \frac{2.9 \times \pi}{4}\right] \tag{5.4}$$

$$P_{optical(max)} = \cos^2\left[\frac{\pi}{2} \times \left(\frac{1V}{8V}\right) - \frac{2.9 \times \pi}{4}\right] \approx 0.3455 \tag{5.5}$$

$$P_{optical(min)} = \cos^2\left[\frac{\pi}{2} \times \left(\frac{-1V}{8V}\right) - \frac{2.9 \times \pi}{4}\right] \approx 0.0545 \tag{5.6}$$

$$ER = 10 \times \log_{10} \frac{P_{optical(max)}}{P_{optical(min)}} \approx 8dB \tag{5.7}$$

One thing that needs to be noticed in Fig. 5.6(b) is that the fitting model (black curve) can reach 0 level of optical output power ($-\infty$dBm), which is completely off. However, it is impossible to reach $-\infty$dBm for the silicon photonic Lumped MZM used here. And the experiment data (red curve) has a minimum output power which normalized value is around 0.065. Therefore, the minimum optical power in (5.6) has to be adjusted and the value would be around

$0.116 = (1-0.065)\times 0.0545+0.065$. And the normalized maximum optical power in (5.5) would be adjusted to $0.388 = (1 - 0.065) \times 0.3455 + 0.065$ as well. So, the ER after adjustment is around 5.24dB which is matched the measurement value in Fig. 5.7. The likely cause for this behaviour (the limited DC extinction ratio) of the Silicon Photonic modulator is the non-linear phase versus voltage characteristic of the phase modulation introduced by the PN junction.

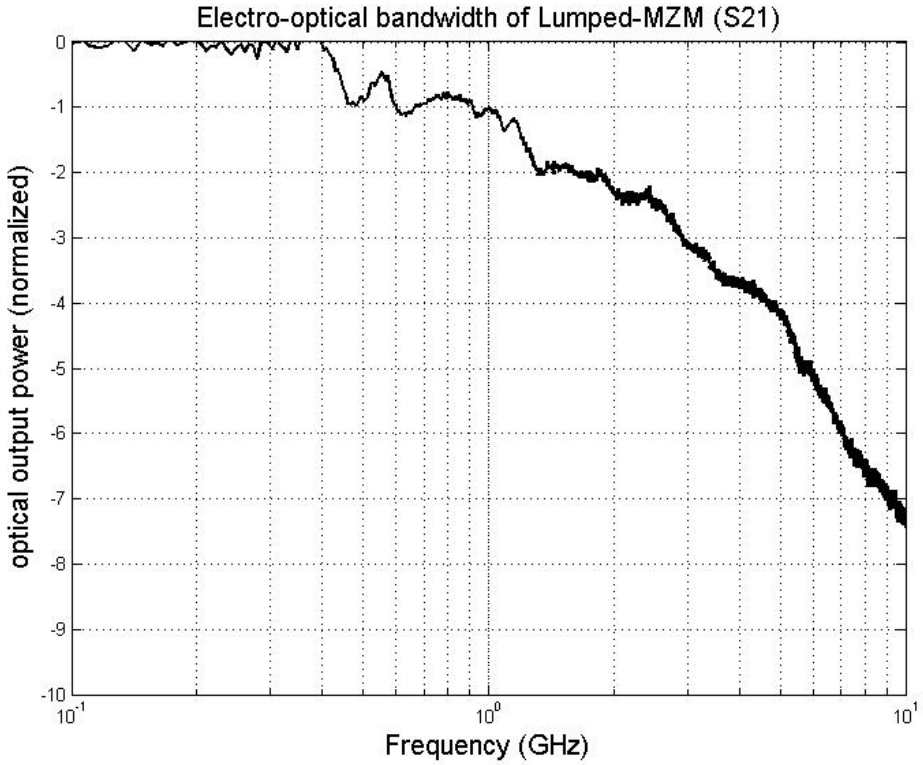


Figure 5.8: Electro-optical bandwidth (S_{21}) of the Lumped-MZM

For the measurement of electro-optical bandwidth, a standalone (hence it was not assembled with the driver chip, thus giving direct access to its pads) asymmetrical Lumped-MZM has been fibre-coupled. The electro-optical frequency response was measured using VNA. One port of the VNA is connected to the MZM with a GSG RF probe. The other port of the VNA is connected to a calibrated photon detector. For the calibrated photo-detector, the conversion ratio between optical signal and electrical signal has been normalized. The S_{21} of the Lumped MZM (normalized) is plotted as Fig. 5.8: the -3dB bandwidth is 3GHz. Using the equivalent circuit presented in Chapter 2 (Fig. 2.7) and using the fact that the source resistance of the VNA is 50Ω, the capacitance of the electrode can be calculated to be $884fF$, by assuming the parasitic resistance of electrode to be 10Ω. Originally, during the design process the parasitic capacitance of

the electrode was assumed to be $\sim 630fF$. However, the measurement result indicates the capacitance is around $884fF$, an increase of 40%. Therefore, the capacitance ratio within the switched capacitors' bank and the overall bandwidth needs to be re-evaluated. If the voltage swing after the voltage doubler (see Chapter 3, Fig. 3.5) was originally 2.3V, the maximum RF swing at each arm is now 0.78V instead of 1V, resulting in 1.55V maximum swing push-pull drive for the lumped MZM. The achievable extinction ratio has been reduced to 4.11dB due to this reduced voltage swing on the electrodes. In addition, the overall electro-optical bandwidth of the lumped MZM is reduced from 24GHz (Chapter 2 Fig. 2.7) to 18GHz assuming the parasitic resistance of electrode is 10Ω.

5.4 Measurement of the PAM4 modulator

Now that the DC characterization and electro-optical bandwidth of the lumped MZM have been measured, the next step is to evaluate the PAM-4 modulator consisting of the lumped MZM assembled with the driver chip. The experimental setup consists of two parts: one part generates the electronic input signals (both DC, high-speed and low-speed digital control signals), the other part consists of the optical setup, see Fig. 5.9.

Firstly, let's discuss the generation of the electronic input signals. As explained in Chapter 3, the CMOS driver chip needs two differential high speed inputs A (consisting of positive phase signal Ap and negative phase signal An) and B (consisting of positive phase signal Bp and negative phase signal Bn). The data rate should cover 5Gb/s up to 25Gb/s for A and B. Both of them are Pseudo-Random Binary Sequence (PRBS) data. Data stream A is PRBS11 with $(2^{11}-1)$ bits and data stream B is PRBS7 with (2^7-1) bits. By using two different PRBS setups, the correlation between data stream A and B is minimized to make sure that A and B are close to real-life data streams. In addition a full-rate clock signal is required for the retiming D-flipflops (see Chapter 3, Fig. 3.11), hence with a frequency ranging from 5GHz to 25GHz: the SHF 78120B clock generator was used as a clock frequency synthesizer. As this frequency synthesizer has only one RF output, a power splitter was used to create two copies of the original clock signal. One of these clock signals was used as the reference clock for the PRBS pattern generator (SHF1214A), which creates the two differential input signals for the PAM4 transmitter. The other copy of the

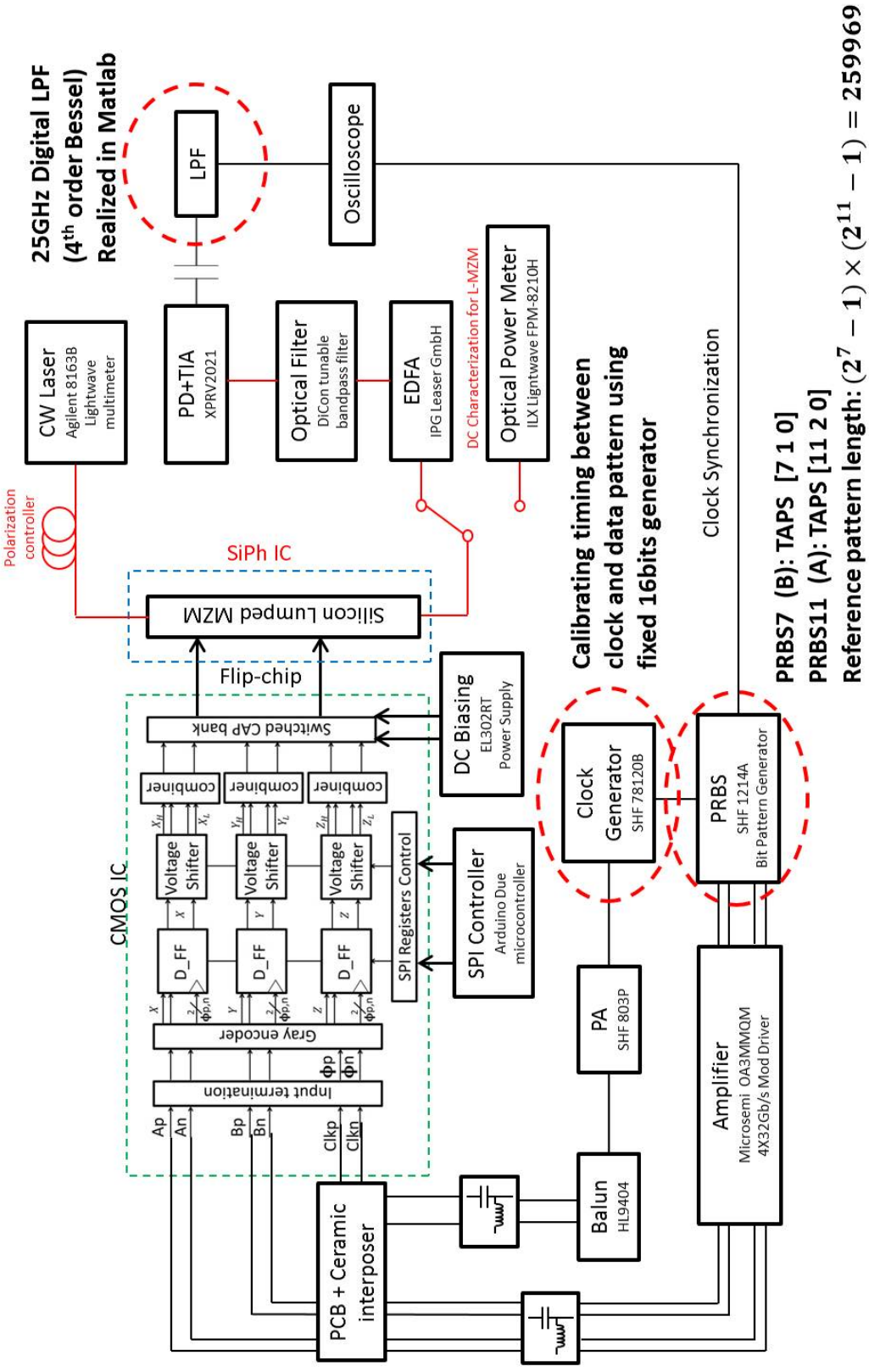


Figure 5.9: Schematic of experiment setup for PAM4 modulator

clock signal was first amplified by a power amplifier (SHF803P), and next a phase and anti-phase copy was generated using a Balun (HL9404) to create the differential clock signals for the PAM4 transmitter. A divided version of the clock signal which was generated by the PRBS pattern generator was used as a trigger signal for the oscilloscope (LeCroy) to capture the final PAM4 output data . The high speed data signals from the PRBS generator do not have enough swing to directly drive the CMOS driver chip and were therefore amplified by the 4×32Gb/s modulator driver quad amplifier (Microsemi OA3MMQM). Bias-tees were used to set the DC biasing point for the inputs to the driver chip. In this way, we have two differential data signals which have 5Gb/s-25Gb/s with 0.6V peak-to-peak swing and working at DC level 0.7V (Ap and An inputs) and 0.9V (Bp and Bn inputs), and two differential clock signals which have 5GHz-25GHz with 0.6V peak-to-peak swing and working at 0.7V DC level.

Finally, the CMOS driver chip contains a number of digital settings, see Chapter 3. These are controlled using the SPI interface of a microcontroller board (Arduino Due) connected to the PAM-4 transmitter in order to configure the internal registers of the CMOS driver chip.

The second part of the experimental setup is concerned with the optical signals. The DC bias voltages for the Lumped MZM are generated by a low-noise DC power supply (EL302RT). The CW laser (Agilent 8163B, wavelength: 1550nm) is connected to a polarization controller in order to keep the polarization in TE mode for maximum coupling efficiency with the grating coupler. The Lumped MZM was biased at the point for maximum extinction ratio. The output signal was coupled to an EDFA (IPG Leaser GmbH) to amplify the optical signal, to compensate for the >12dB optical insertion loss of the Lumped MZM. A tunable optical bandpass filter (bandwidth: 4nm) was used to remove the out-of-band amplified spontaneous emission (ASE) noise from the EDFA. After optical filtering, the signal was coupled into a photodetector equipped with a transimpedance amplifier (XPRV2021, gain is 150V/W and DC-40GHz bandwidth). The PD+TIA translates the optical signal into an electrical signal that can be captured by a high-speed real-time sampling oscilloscope (LeCroy, analog bandwidth = from DC to 50GHz, with 160GS/s sampling rate). A broadband coupling capacitor was used between the output of PD+TIA and the input of the low pass filter (LPF). Since the TIA+PD has 40GHz bandwidth, a 4th order Bessel Thomson low pass filter (LPF) with DC to 20GHz bandwidth is necessary to remove out-of-band thermal noise from the TIA, thus enabling the oscilloscope to capture clean eye diagrams. The laboratory setup also includes

the capability of measuring the bit-error rate by post processing the waveform stored by the real-time sampling scope. The software developed in the Photonic Systems Group allows estimating the bit-error rate either through direct counting, or fitting probability density functions to the measured signal levels at given sampling points. The picture of the laboratory setup is shown in Fig. 5.10. The outputs of the software can be seen in Fig. 5.11, Fig. 5.12 and Fig. 5.13 and are further discussed below.

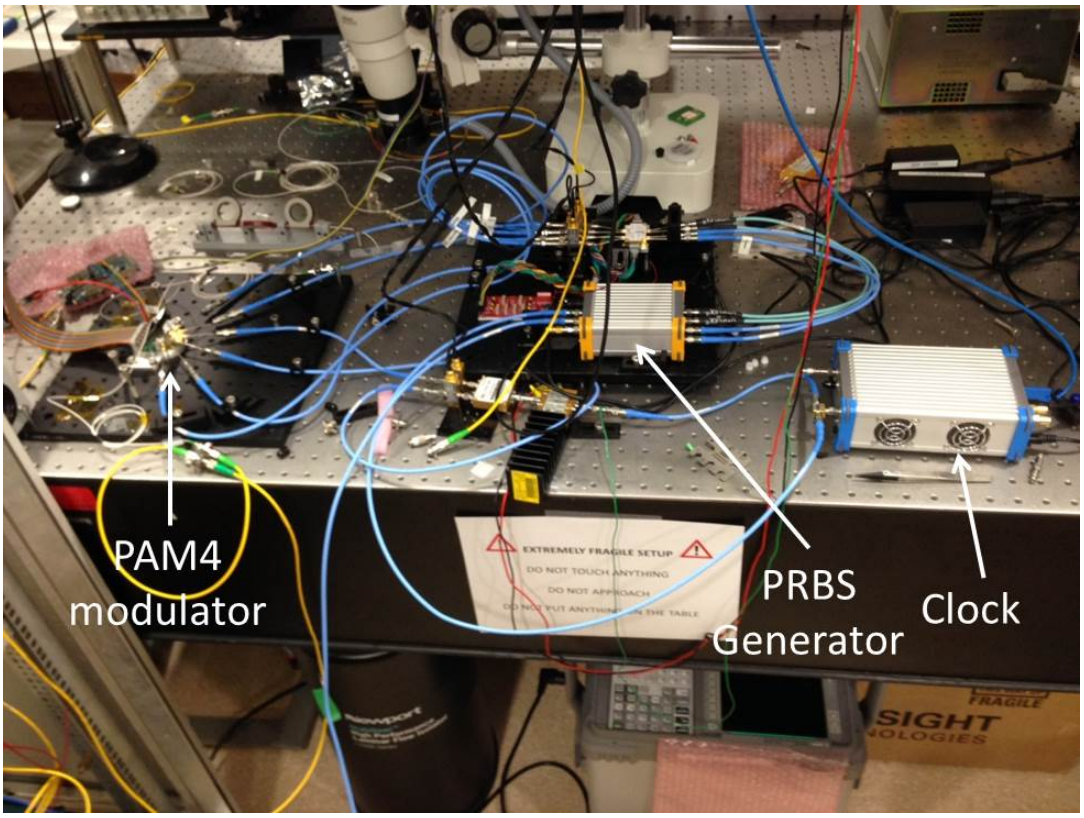


Figure 5.10: Laboratory setup for the measurement of PAM4 modulator

PAM-4 eye diagrams at different baudrates (30Gb/s, 36Gb/s and 40Gb/s) captured in this way are presented in Fig. 5.11, Fig. 5.12 and Fig. 5.13. A summary of the quality of the eye diagrams is shown in Table 5.1. As the Lumped MZM has been biased below its quadrature point, the device is operating in its non-linear region and hence the PAM-4 levels are not evenly spaced. Even though the capacitor bank inside the CMOS driver chip was sized to compensate for the MZM non-linearity here, it is only partially compensated. Indeed the capacitor values were calculated assuming the modulator was biased at its quadrature point.

Looking at the eye diagrams itself (and the accompanying probability density plots) in Fig. 5.11, Fig. 5.12 and Fig. 5.13, it can be seen how the standard

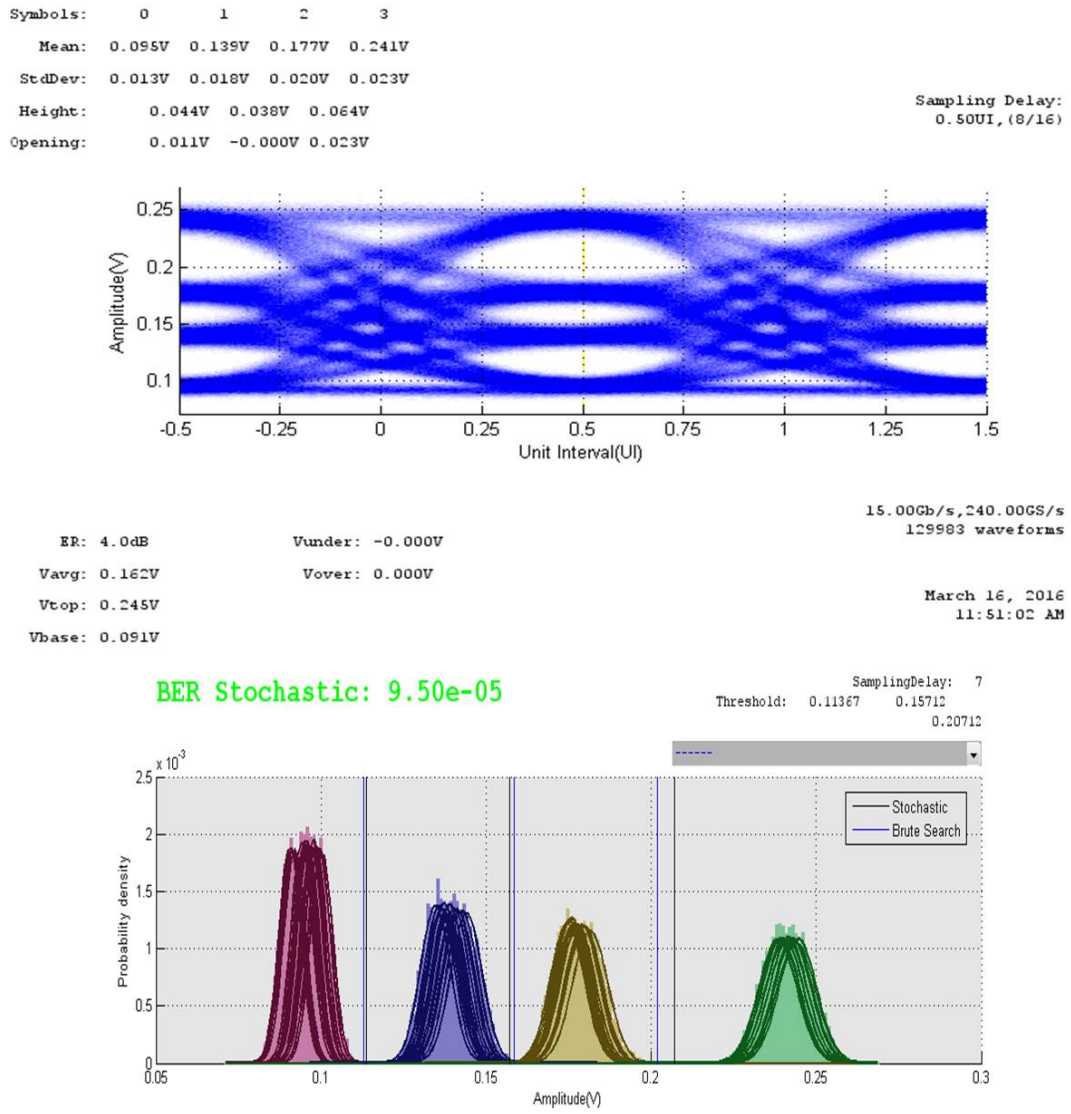


Figure 5.11: Measurement results for 30Gbits/s (15GBauds/s) PAM4 optical output

deviation of each level increases for increasing bitrates. A very rough (but quickly measured) quality of an eye diagram can be obtained by considering the spacing between two adjacent levels taking into account three times that measured standard deviation (σ). For the 30Gb/s eye diagram plotted in Fig. 5.11, the gaps after three times of the standard deviation (Opening) are 11mV between PAM1 and PAM2 levels, 23mV between PAM3 and PAM4 levels, and 0mV between PAM2 and PAM3 levels. This means the two levels in the middle are directly next to each other and will contribute heavily to the overall BER. When the bitrate is increased to 36 Gb/s (Fig. 5.12), the difference taking into account three times the standard deviation of the middle level is negative (-9mV). This is confirmed by the BER increases from 9.5×10^{-5} at 30Gb/s to $6.78\times$

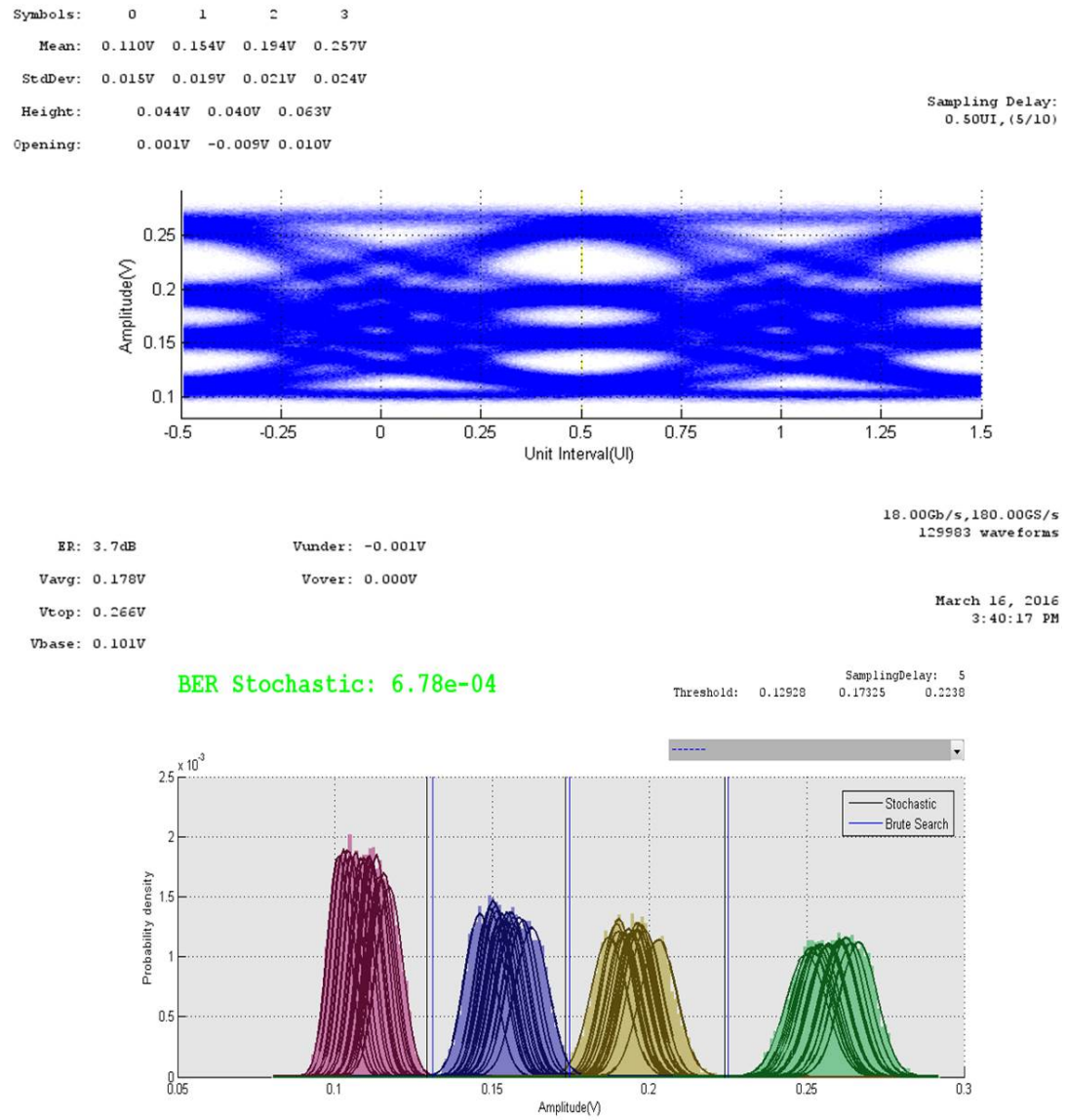


Figure 5.12: Measurement results 36Gbits/s (18GBauds/s) PAM4 optical output

10^{-4} at 36Gb/s. Note that this is actually sufficient to maintain an optical link, assuming for example the use of RS(255, 223) feedforward error correction. For the 40Gb/s eye diagram plotted in Fig. 5.13, all the separations between the different levels taking into account three times their standard deviation (Opening) are negative values. Indeed as can be seen in the probability density plots in Fig. 5.13, the PAM levels are spread out and heavily overlapped. Not surprisingly, the BER further worsens to 2.2×10^{-2}.

The main reason for this observed spread of the PAM levels has been traced back to small (but not negligible) differences in the moment where the retiming flipflops retime the data: these differences are important for some specific data

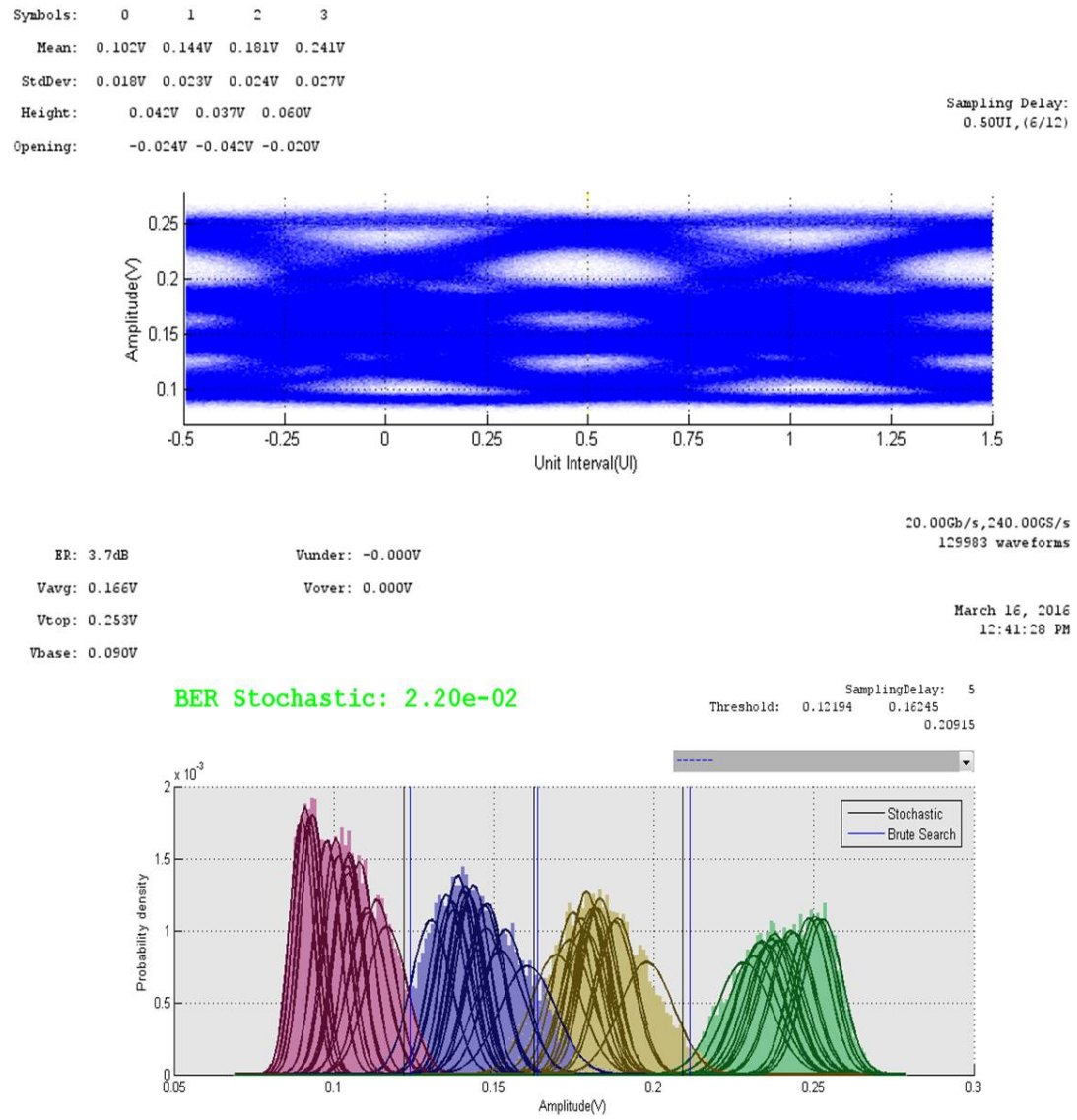


Figure 5.13: Measurement results for 40Gbits/s (20GBauds/s) PAM4 optical output

patterns. In Chapter 4, the clock signals as they appear after the matching network have been simulated: the overall maximum clock deterministic jitter was 5ps and is attributed to small path differences in the clock distribution network. In Chapter 3, it can already be seen that the delay differences of the signals after the synchronization by the D flipflop is around 5ps, which means the maximum delay difference between X, Y and Z is also around 5ps.

To further analyze this issue in detail, a simulation was performed at a full-rate clock of 20GHz. The A input signal of the driver chip was selected to be a 101010... sequence running at 5Gb/s (Clock/4) while the B (Clock/2) input signal of the driver chip was selected to be a 101010 sequence running

Table 5.1: Summary of eye diagrams

30Gb/s	PAM1	PAM2	PAM3	PAM4	BER	9.5×10^{-5}
Mean Value	95mV	139mV	177mV	241mV	ER	4dB
σ	13mV	18mV	20mV	23mV	V_{avg}	162mV
Eye height	44mV	38mV	64mV		V_{max}	245mV
Eye opening (3σ)	11mV	0mV	23mV		V_{min}	91mV
36Gb/s	PAM1	PAM2	PAM3	PAM4	BER	6.78×10^{-4}
Mean Value	110mV	154mV	194mV	257mV	ER	3.7dB
σ	15mV	19mV	21mV	24mV	V_{avg}	178mV
Eye height	44mV	40mV	63mV		V_{max}	266mV
Eye opening (3σ)	1mV	-9mV	10mV		V_{min}	101mV
40Gb/s	PAM1	PAM2	PAM3	PAM4	BER	2.2×10^{-2}
Mean Value	102mV	144mV	181mV	241mV	ER	3.7dB
σ	18mV	23mV	24mV	27mV	V_{avg}	166mV
Eye height	42mV	37mV	60mV		V_{max}	253mV
Eye opening (3σ)	-24mV	-42mV	-20mV		V_{min}	90mV

at 10Gb/s. To speed up the simulations (which can take days to complete for the full chip database including extracted parasitic and EM models for the 3D inductors and input matching network) arbitrary function generators were used to emulate the outputs of the D flipflops. Based on Table 3.2 in Chapter 3, the X signal is then a square wave with 75% duty cycle; the Y signal is a square wave with 50% duty cycle; and the Z signal is a square wave with 25% duty cycle. The voltage swing, rise time and fall time of the arbitrary function generators are set to be the same as outputs of the real D flipflops as introduced in Chapter 3. By assuming no delay different among the signals X, Y and X, the simulated output waveforms of the level shifter, the voltage combiner and the switched capacitor bank are shown in Fig. 5.14. The top plot in Fig. 5.14 is the input of the level shifters, which are also the outputs of the D flipflops from the previous stage. The outputs of the voltage combiners are plotted as the second waveforms in Fig. 5.14. Finally, the output of switched capacitors' bank is plotted as bottom two waveforms in Fig. 5.14. The four different PAM levels can be identified clearly.

Now, 5ps time delay difference is introduced between the X and Z signals, and the simulation results are shown in Fig. 5.15. In the top waveform of Fig. 5.15, there is 5ps shift of the Z (green curve), which can be identified by comparing with the top waveform in Fig. 5.14. The final PAM4 outputs of the switched capacitors' bank are plotted as bottom two waveforms in Fig. 5.15. As marked

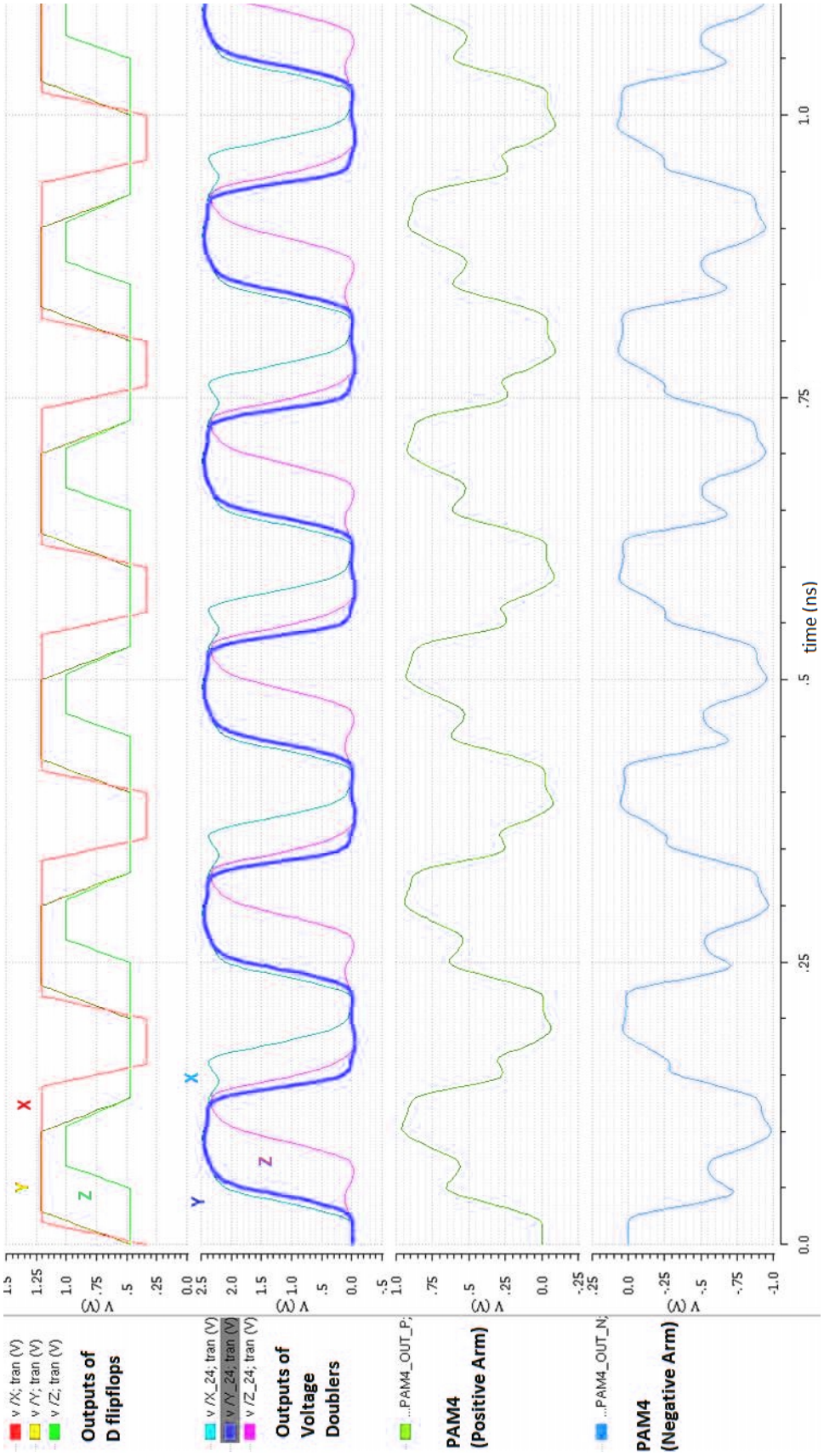


Figure 5.14: Simulation analysis of no delay case (A= Clock/4, B= Clock/2)

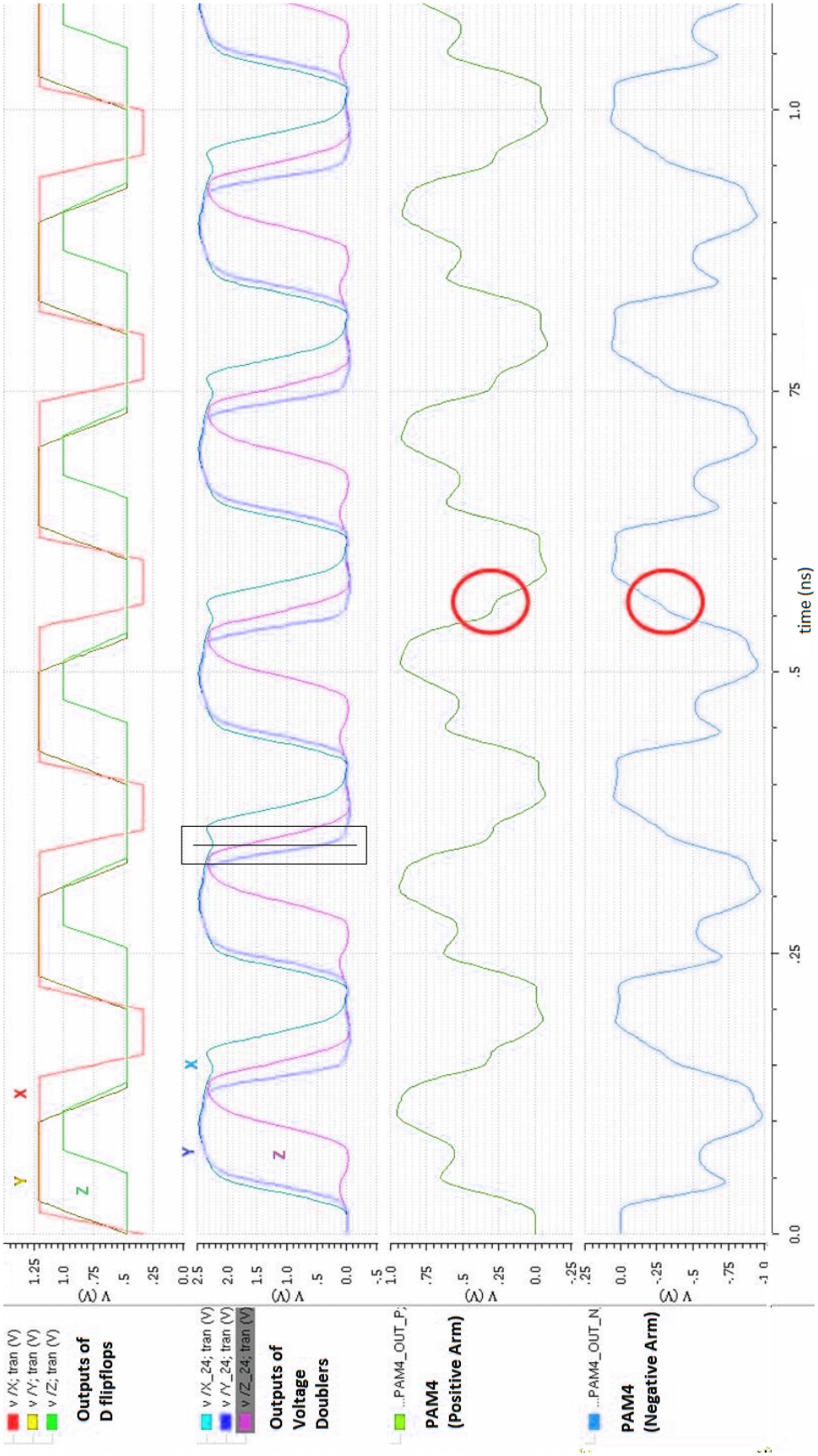


Figure 5.15: Simulation analysis of 5ps delay case (A= Clock/4, B= Clock/2)

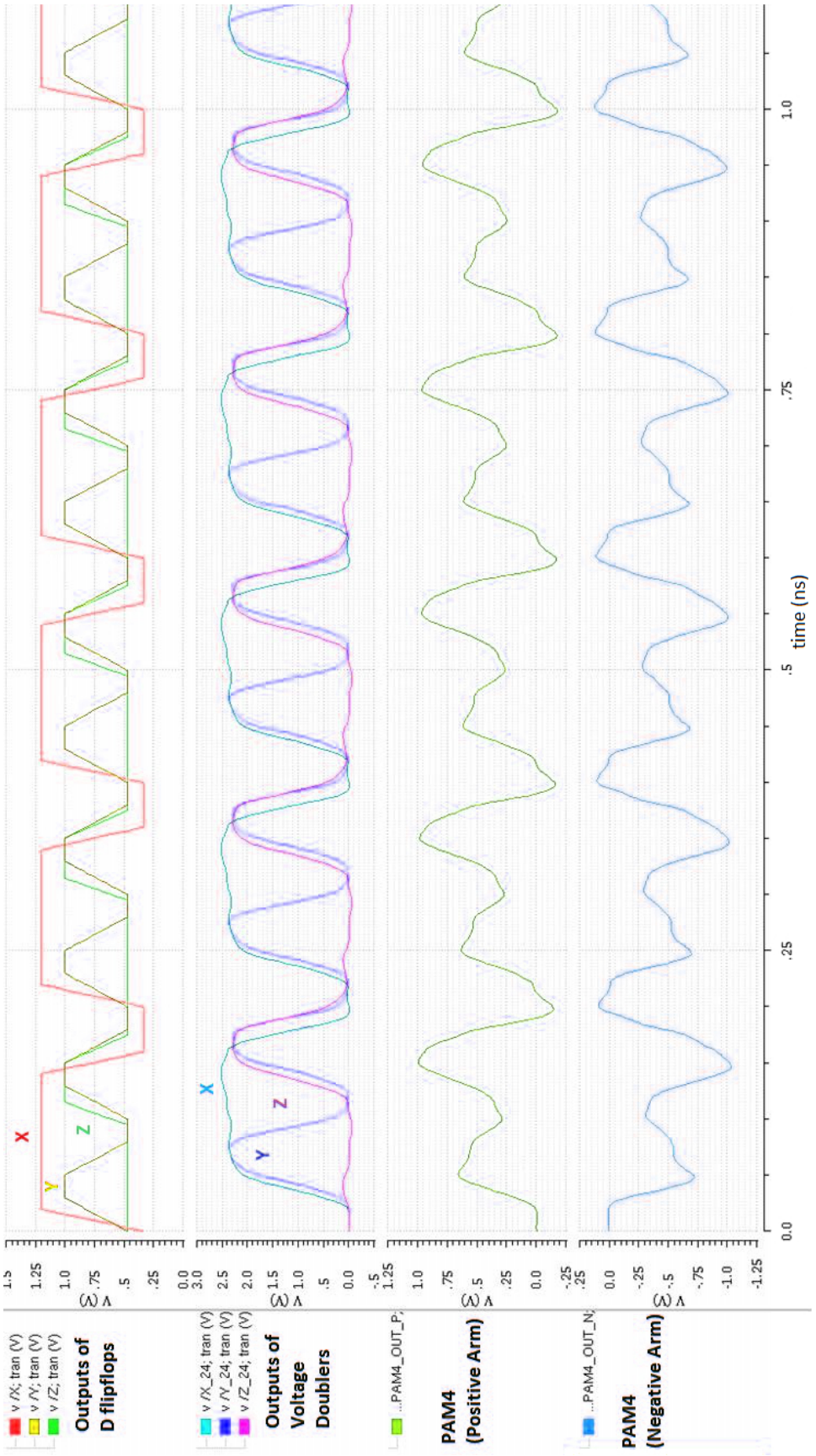


Figure 5.16: Simulation analysis of 5ps delay case (A= Clock/2, B= Clock/4)

by the red circles, no clear PAM2 and PAM3 are visible anymore. In the bottom waveform of Fig. 5.15, the PAM3 symbol is almost disappeared and drifted to the PAM2 level. By looking at the output signals of voltage doublers (marked with white rectangle), both X and Z are high voltage and Y is close to 0V. In another word, the gray coding within the white marker is X=1, Y=0, and Z=1 which could not be found in the truth Table 3.2. And this error data pattern is sharing the same time window for the correct data pattern (X=1, Y=0, and Z=0 shown in Fig. 5.14). Those are the two main reasons to cause the problem of PAM2 and PAM3 disappearing.

However, if the input data patterns are swapped to be A = with data rate of Clock/2 and B = with data rate of Clock/4, the symbols become visible once again even though the 5ps delay applied, as shown in Fig. 5.16, because the 5ps delay does not introduce any error pattern for PAM2 and PAM3 levels. In the bottom two waveforms in Fig. 5.16, the 4 PAM levels can once again be identified clearly. To further confirm the root cause, additional measurements have been done to observe the reaction of critical input patterns, and some transitions between the different PAM-4 levels is disappear. In Fig. 5.17, the input signals are Clock/4 for A and Clock/2 for B, which as explained is the critical pattern for the PAM-4 modulator. As expected, the 2 middle levels are hard to identify. However, when the input signals are swapped (clock/4 for input signal B and clock/2 for input signal A), the 4 levels are easily identified in Fig. 5.18.

To conclude the 40Gb/s case, small delay differences between the clocks distributed to the three retiming flipflops cause the PAM transitions to disappear for some critical data patterns, resulting in high BER. From another perspective, the gray coding scheme also has a weak point, which is the strict requirement for the alignment of the X, Y and Z signals, especially for some critical data patterns. This phenomenon was not been identified during the design process. The main reason is the limited computational power of the simulation server. In Chapter 3, the full chip post layout transient simulation time is around 20ns. So, for the 40Gb/s data rate, the simulation only captures 800bits (400 symbols). During the entire 800 bits, the critical pattern did not appear. However, in the measurement, the total pattern length is around 260,000 bits (130,000symbols) based on Fig. 5.9 and the total time period is around 6500ns, greatly increasing the occurrence frequency of the critical pattern.

Finally, the PAM4 modulator has been optimized to 36Gb/s case and the eye

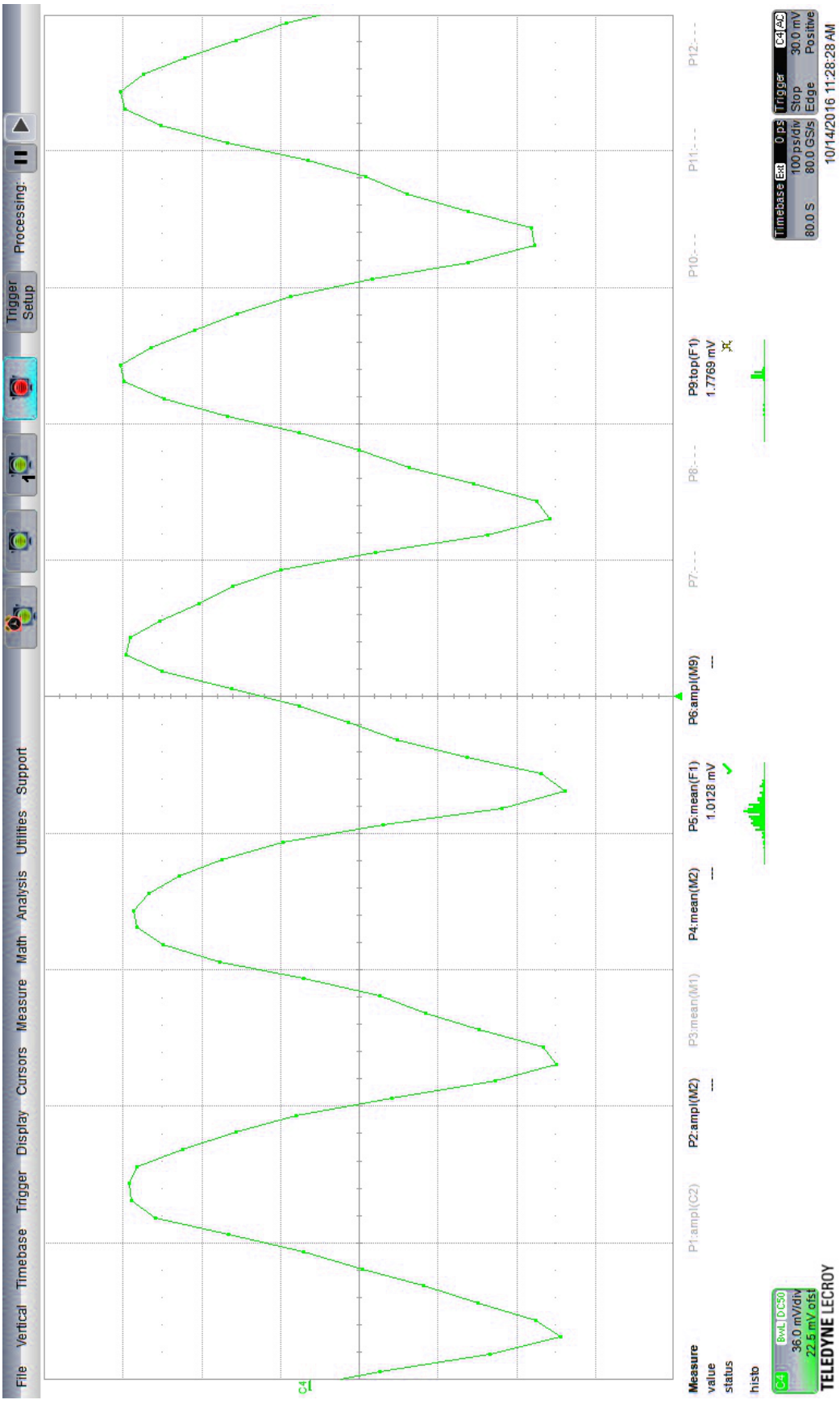


Figure 5.17: Measurement result of the case with A= Clock/4, B= Clock/2

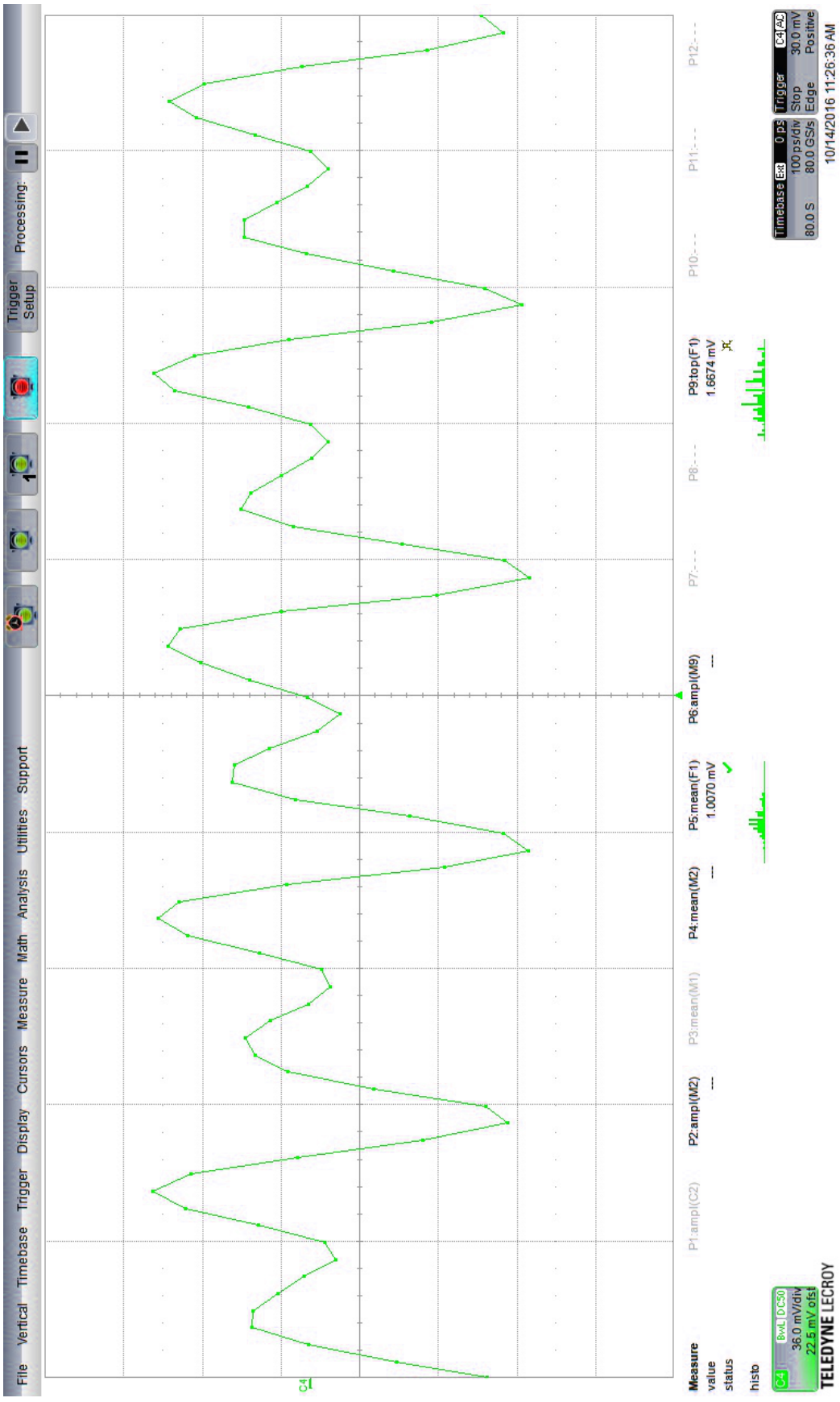


Figure 5.18: Measurement result of the case with A= Clock/2, B= Clock/4

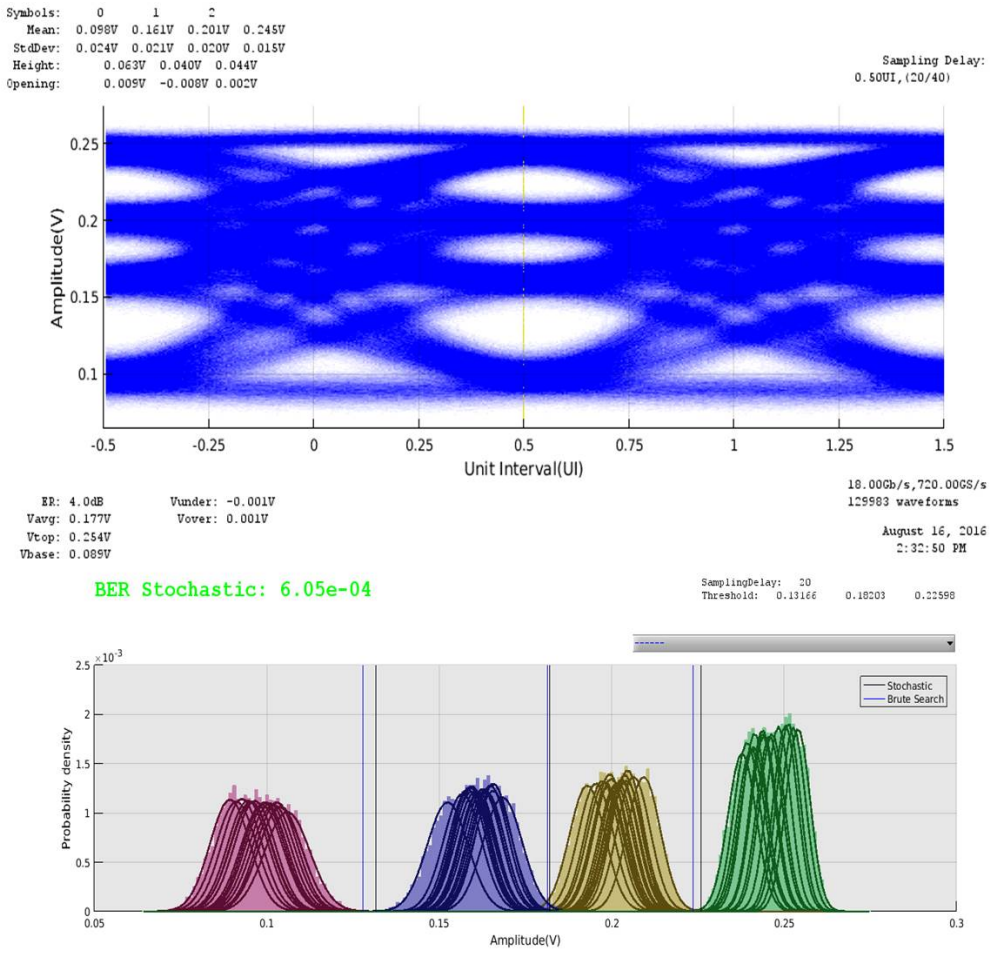


Figure 5.19: Measurement results for 36Gb/s (20GB/s) PAM4 optical output after optimization

diagram is plotted as Fig. 5.19: the extinction ratio between the top and bottom PAM-levels (ER) is 4dB. The bit-error rate was measured and found to be 6.05×10^{-4}. Note that the PAM-4 levels are not equidistant. The reason for this is that the capacitors C_X, C_Y and C_Z were sized in such a way that the generated PAM-4 voltage levels were precompensated for the cos^2 non-linear transfer of the MZM. The selected size of the capacitors C_X, C_Y and C_Z depends on the V_π and capacitance of the MZM, which turned out to be different on the actual device compared to the values assumed during the design process. In addition VDD can be tuned as well to match the actual V_π. This can be easily corrected by resizing the capacitor bank. The chip consumed a total of 236mW from 1.2V and 2.4V supply voltages (measured numbers). The total chip achieved an energy efficiency of 6.55pJ/bit including the retiming circuitry and Gray coding, or 5.37pJ/bit for the core circuit itself (excluding retiming and Gray coding). To understand better which blocks contribute most to this power consumption,

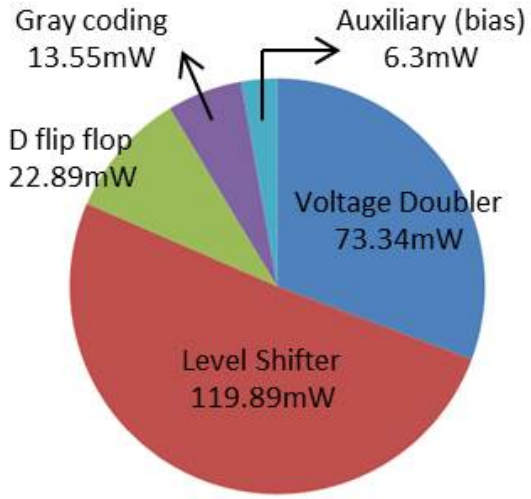


Figure 5.20: Distribution of power consumption over different blocks

Fig. 5.20 shows how this overall power consumption of the chip is distributed among the different blocks. One drawback of the switched capacitor approach is that its power consumption increases linearly with the bitrate, as indeed the power required to charge and discharge the capacitors increases linearly with bitrate. However, from Fig. 5.20 it is interesting to note that the power to drive the switched capacitor bank (73mW, dissipated through the voltage doubler circuit) is actually not the dominant part in the overall power consumption. Rather it is the level shifter circuit which consumes most power. As can be seen in Chapter 3, the level shifter is a differential circuit. Hence its power consumption is largely static and does not increase with bitrate. This indicates that additional power savings are possible by using an improved level shifter circuit. Finally it is also important to note that the dynamic power dissipated by the voltage doubler circuit consists of two parts: power dissipated purely to charge or discharge the capacitor bank, and short circuit power. This short circuit power is dissipated during bit transitions when a direct path can exist between VDD and GND due to transistors that have conducting channels at the same time. This short circuit power accounts for $> 50\%$ of the total voltage doubler power, and can be reduced by sharper transitions on the input signals (outputs of the level shifter). This can be achieved by changing the circuit topology (like driving stage shown in Fig. 1.11) or by using more advanced CMOS technology (higher f_t comparing with 65nm CMOS technology).

The overall performance summary and comparison with state-of-the-art hybrid (i.e. where the electronics and Silicon Photonics have been integrated on different chips) Silicon Photonic transmitters is provided in Table 5.2. Compared

to [15], the bitrate is increased by 80%, however, the energy efficiency is much worse, likely mainly as the authors in [15] used more complex structure of Silicon Photonic Lumped-MZM and a faster 40nm CMOS technology. References [10] and [14] use SiGe BiCMOS technology to achieve higher bitrates (but limited to non-return to zero modulation rather than the PAM-4 demonstrated in our work), at the expense of similar to worse energy efficiency. It is also noteworthy how the extinction ratio (here measured as the ratio of optical power of the highest to the lowest PAM-4 level) is 4dB, significantly better than[10] and [14]. Smallest circuit size has been achieved thanks to the use of 3D solenoids and small active area of the switched capacitor approach [21].

Finally, we compare the performance of our hybrid (i.e. the photonics and electronics have been integrated into two different technologies) approach to two different monolithic implementations. In [9], an NRZ transmitter is reported which uses a 90nm CMOStechnology equipped with photonic components, while in [13] a PAM-4 transmitter has been reported using the same technology. The modulator used in [13] is a travelling wave segmented (two segments used) MZM, terminated using sets of 50Ω resistors. The low $V_\pi \times L$ product of the used MZM results in low power consumption and excellent energy efficiency of 5.4pJ/bit at 25Gbaud (50Gb/s) PAM-4. We anticipate that by using our proposed PAM-4 driving scheme in such monolithic technology, an even lower power consumption can be achieved. Indeed in a monolithic technology the capacitance associated with the bondpads can be completely eliminated. On the other hand, note that in the hybrid approach, the overall chip area can be reduced as electronics can be stacked on top of the photonics.

5.5 Summary

In this Chapter, the switched capacitor technique, which enables the silicon photonic Lumped MZM for high speed optical data links, is proven through measurements. The failure of 40Gb/s is not caused by the switched capacitor technique but caused by the low tolerance of data miss alignments of the gray coding scheme. The chip performs well compared to the state-of-art designs. In addition, the broadband matching networks based on modified Butterworth and constant k filters have been evaluated in actual silicon.

Table 5.2: Performance summary

Items	Units	Our work	[15]	[10]	[14]	[9]	[13]
Wavelength	μm	1.55	N.A	1.3	1.3	1.3	1.3
Integration	-	Hybrid	Hybrid	Hybrid	Hybrid	Monolithic	Monolithic
$V_\pi \times L$	$V \cdot mm$	12	<2	N.A	N.A	14.7	14.7
Bitrates	$Gbit/s$	36	20	56	56	32	50
Modulation Format	-	PAM4	PAM4	NRZ	NRZ	NRZ	PAM4
Driver Technology	-	65nm CMOS	40nm CMOS	130nm SiGe BiCMOS	55nm SiGe BiCMOS	90nm CMOS	90nm CMOS
Driver Chip Size	mm^2	1.9×0.9	2.6×1.8	N.A	2.6×2.6	N.A	N.A
Driver Core Area	mm^2	0.11	N.A	N.A	0.386	N.A	N.A
Supply Voltage	V	1.2, 2.4	1	N.A	N.A	N.A	N.A
Power	mW	236	96	430	300	140	270
Efficiency (Driving Stage Only)	pJ/bit	5.37	1~2	7.68	5.36	4.4	5.4
ER	dB	4	9	2.7	2.5	3.5	6.4
BER	-	6.05×10^{-4}	N.A	10^{-5}	N.A	10^{-12}	10^{-12}

Chapter 6

Conclusion and future work

6.1 Conclusion

In this thesis, new design concepts to realize a high-speed PAM-4 transmitter have been proposed and experimentally verified. The PAM-4 transmitter consists of a Silicon Photonic lumped Mach-Zehnder modulator, integrated with a high-speed driver IC realized in a deep sub-micron (65nm) CMOS technology. A theoretical analysis has concluded that the lumped Mach-Zehnder modulator can be used for high speed (up to 25Gbaud) optical links, leveraging the miniaturization capability of silicon photonic technology. The driver IC is based upon switched capacitor class-G amplifier (aka. RF-DAC) [30]. This technique was originally applied in narrowband wireless communication systems, and has been introduced into optical communication systems for the first time in this thesis.

An asymmetric Lumped-MZM has been designed and fabricated based on IMEC ISIPP25G Silicon Photonic Technology. The PAM4 electronic driver chip has been designed based on 65nm CMOS technology, which includes Gray encoder circuitry (based on CML gates) and retiming flipflops, driver stage circuitry (three level shifter circuits, six voltage combiner circuits and two switched capacitor banks), an input matching network, biasing circuitry (constant gm circuit and current mirrors), and SPI register control circuitry. The CMOS driver chip has been flip-chipped on top of the Silicon Photonic chip containing the Lumped-MZM and grating couplers. The Lumped-MZM was biased below quadrature point for better ER, a detailed analysis investigated the MZM biasing point to maintain highest possible optical budget. Up to 36Gb/s PAM4 optical

signals have been successfully generated. Eye diagrams were captured using a high-speed photodetector and real-time sampling oscilloscope. At 36Gb/s, the ER is 4dB with a BER of 6.0×10^{-4}. The total power consumption of the driver chip was 236mW (6.6pJ/bit at 36Gb/s). The driving stage consumed 193mW. The other parts of the driver IC (encoder circuit and retiming flipflops, biasing circuits and SPI register control circuit) consumed around 43mW. If we only consider the driving stage, the efficiency is around 5.37pJ/bit. The full CMOS chip size is 1.9mm by 0.9mm with the core circuitry only occupying 0.25mm by 0.44mm. The full silicon photonic chip size is 2.5mm by 1.25mm and the lumped MZM occupies only 0.13mm by 2.16mm. To achieve bitrates beyond 36Gb/s, propagation delay differences in the encoding and retiming circuitry will need to be eliminated through improved layout of the clock distribution network. This will be done in a next version of the driver IC. However, the concept of using the switched capacitor technique combined with Lumped MZM for high speed optical data links has been proved through experiments and performs well when compared against state-of-the-art designs.

In addition, an approach to design broadband signal paths based on microwave filter theory (modified Butterworth and constant k) has been developed and proven experimentally. Worst case 8dB return loss across a bandwidth ranging from DC to 20GHz has been achieved, sufficient for our applications. In the best case, the performance is 10dB return loss across a bandwidth ranging from DC to 25GHz. The main advantage of the proposed technique is significantly reduced chip area. For example, compared to a conventional T-coil matching network, 70% less chip area is required. The trade-off is somewhat reduced return loss performance, for example compared against the T-coil method which has been shown to achieve better than 10dB return loss up to 30GHz.

6.2 Future works

6.2.1 System analysis of critical data pattern

In the previous chapter, problems with transmission at 40Gb/s have been investigated using simulations. Critical data patterns exist that require precise alignment among X, Y and Z. This issue could be potentially solved by line coding scheme. Currently in the experimental setup, the input data are PRBS7 and PRBS11 and transitions between each PAM level is randomly distributed. So

it is really hard to identify all critical data patterns. In a next step, the input signals could be generated by field-programmable gate array (FPGA) boards instead of a pattern generator (SHF 1214A). Arbitrary data patterns can be created by the FPGA and sent into the modulator. By sweeping the input data, all critical data pattern could be found experimentally. After this, we can apply a line coding scheme to avoid those critical pattern in order to reduce the BER of 40Gb/s transmission.

Another way to solve the critical pattern issue is using binary weighted coding scheme presented in Chapter 3 instead of gray coding. Based on Table 3.1, the binary weighted coding only requires the alignment of two data paths, which could be easily achieve in the chip layout by introducing symmetrical metal routing for clock distribution. However, from Fig. 3.2, the gray coding requires the precise alignment among three high speed data path, X, Y and Z, which is impossible to apply symmetrical metal routing technique. However, there is a trade-off. The BER is always larger than SER for the binary weighted coding scheme. The line coding scheme could also be a solution by reducing the probability of transitions between the two middle levels (PAM2 and PAM3).

6.2.2 Driver design for capacitive optical modulator

The switched capacitor scheme was developed specifically to drive a lumped MZM. However, this scheme is not limited to only lumped MZMs. In Fig. 3.3, the lumped MZM can be replaced by other optical modulators as long as the equivalent circuit model of the electrode is a capacitor. Therefore, the switched capacitor scheme is potentially suitable for micro-ring modulators and lumped Electro-Absorption Modulators (EAM).

From the circuit perspective, the ring modulator is just a reversed biased PN junction, the same as the lumped MZM in this thesis [40]. In [40], the total capacitance of the ring modulator is $144fF$ which is much smaller than $884fF$ in our case. Currently, people build the 50Ω inside the ring modulator in order to match the standard microwave system [40]. For the ring modulator alone, the electro-optical bandwidth is killed by the 50Ω RF system, which is only $\sim 20GHz$ [41]. If the bandwidth enhancement scheme shown in Fig. 2.7 is applied to drive the ring modulator, the overall -3dB bandwidth could be up to 48GHz (assuming $144fF$ for ring modulator and $298fF$ for contact pads and parasitic capacitance), which is sufficient for 56Gb/s NRZ or 100Gb/s PAM4

signals. Potentially, the power consumption will be halved compared to our lumped MZM driver and the data rate can be doubled. The efficiency of driver stage would be 1.34pJ/bit, very close to the 1pJ/bit goal. The disadvantage of ring modulators is that their sharp resonance is very sensitive to temperature and process variations [20].

The travelling-wave (TW) EAM is like the travelling wave MZM, which has been applied for high speed optical communication. However, when the dimension of EAM has been reduced dramatically by the silicon photonic technology, it is facing same problems discussed in Chapter 2. In [42], the length of the silicon photonic EAM is only $80\mu m$, which means the boundary frequency is beyond 100GHz. Therefore, the TW-EAM should be characterized as lumped model as well. Then the switched capacitor scheme can be applied here as well.

6.2.3 Advanced modulation formats

The switched capacitor approach introduced in Chapter 2 and 3 was inspired by the class G switched capacitor power amplifier (SCPA). The latter is also known as an RF-DAC (digital to analog converter) or digital power amplifier. Traditionally, the RF-DAC is used in wireless communication system. For example in [43], a 64 QAM LTE signal has been generated and amplified using an SCPA. The output power can reach up to 20.5dBm in a 2GHz RF frequency band (narrowband transmission). The SCPA can also have excellent performance for broadband operation. In [44], an 20dBm output power was achieved in a band ranging from 3GHz to 9.1GHz through magnetic coupling. From the linearity perspective, the SCPA has superior linearity comparing with other architectures [30], because the final RF output power is digitized by the capacitors and not limited by the supply voltage of the active switches. The differential nonlinearity is less than $\pm$0.4 LSB across the entire power range from -7dBm to 25dBm, and no pre-distortion is needed for non-constant envelop (e.g. QPSK, QAM, OFDM) modulated signals as used in the IEEE 802.11g standard [30].

The high linearity of the switched capacitor technique makes it ready applicable to more sophisticated and higher capacity transmitters. Three examples that should be achievable in my experience are listed hereafter. The presented concepts will be used in future versions of the transceiver technology, realized within the Irish Photonic Integration Centre (IPIC).

- 16 QAM optical transmitter for 400Gb/s link

Fig. 6.1 shows the proposed transmitter, it uses wavelength division multiplexing of four wavelengths located in the C-band (1550nm wavelength window). Since current silicon photonic technology can only work in one polarization [20], the TE mode has been chosen and modulated with a 16-QAM signal at 25Gbaud (100Gbits/s per polarization). Each wavelength uses a QPSK setup, which consists of two lumped MZMs and one 90 degree phase shifter. One lumped MZM is cascaded with a 90 degree phase shifter and then combined in parallel with a second optical power splitter. For each Lumped MZM, a binary weighted PAM4 coding scheme is used instead of the Gray coding scheme to overcome the over-sensitivity of the data alignment to critical data patterns. Indeed binary weighted modulation is fully symmetrical for all data transitions and with respect to the clock path. Since the PAM4 modulation is applied to both Lumped MZMs, the QPSK setup now generates a 16 QAM signal. For each lumped MZM, the optical output is a 50Gb/s PAM-4 signal. Therefore, the output of QPSK is a 100 Gb/s 16QAM signal. Based on [43], potentially, the 64 QAM has the possibility to realize in the future as well.

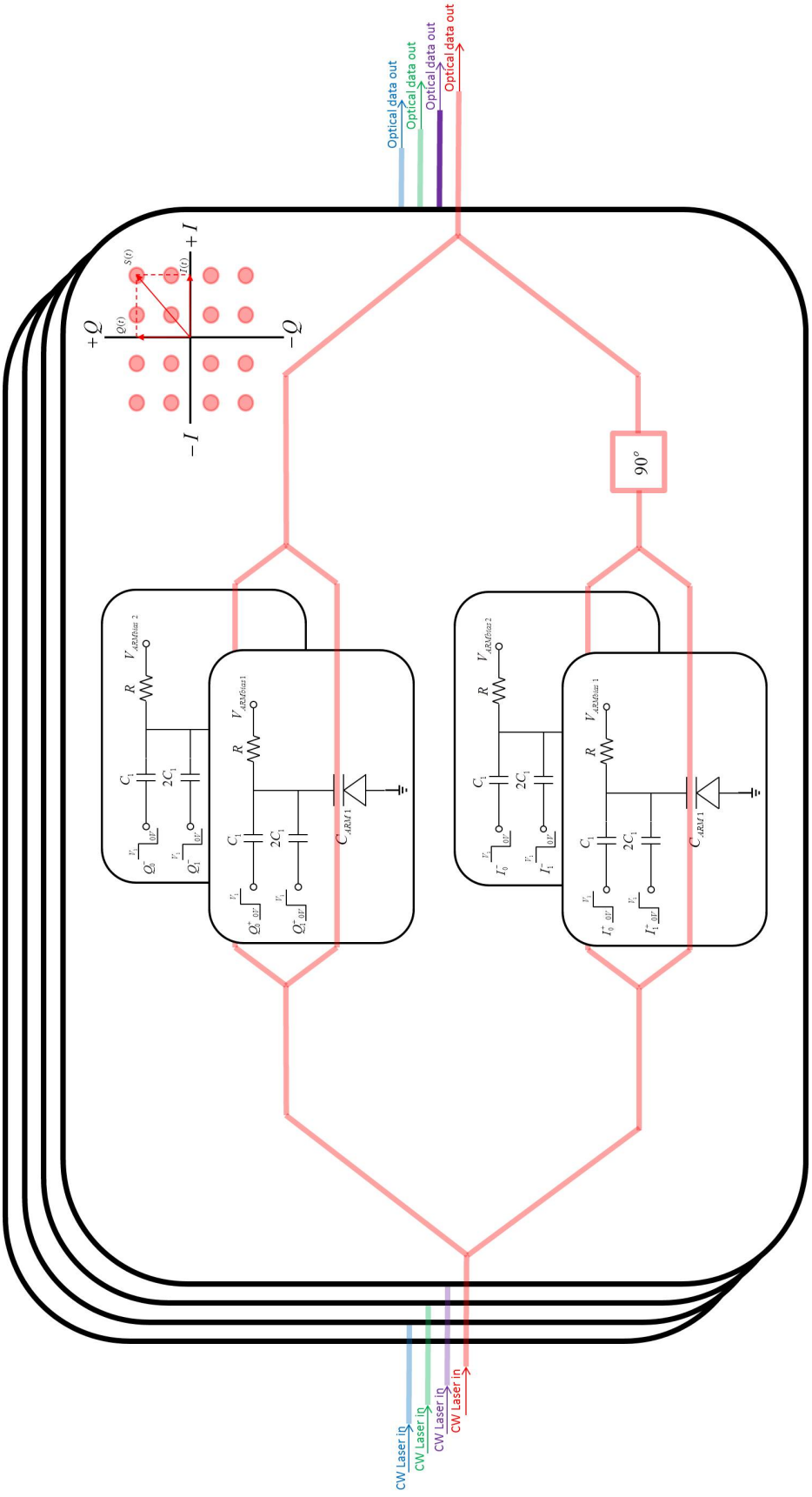


Figure 6.1: System view of 16 QAM 400G WDM transmitter

- Discrete multitone modulation

  In some applications, e.g. using plastic optical fibre or multimode fibre (which suffer from modal dispersion and have very limited reach x bandwidth products), single-mode fibre transmission over long distances (in scenarios with very high amounts of chromatic dispersion) or when using low-cost modulators with low bandwidth, transmission of a full-rate serial signal such as 25Gbaud PAM-4 can be challenging. Indeed the distortion introduced by either the fibre or the modulator can be so large that it can be difficult to recover the signal, even when using advanced dispersion compensation techniques. An alternative technique which stems from copper-based wireline applications and wireless applications is the use of discrete multitone modulation (DMT).

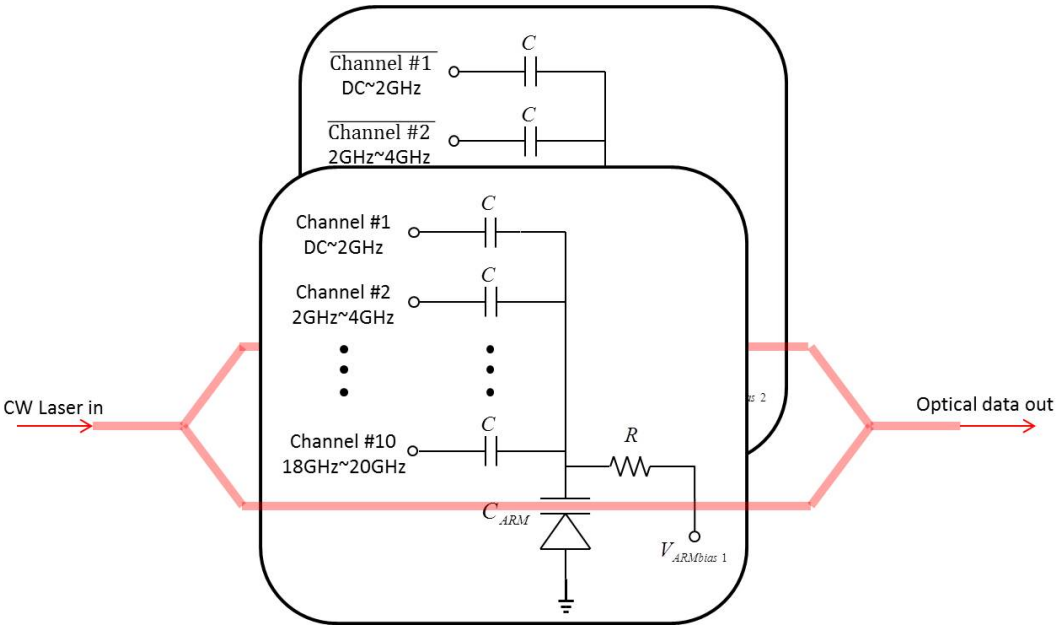


Figure 6.2: System view of discrete multitone modulation

  In DMT, a number of signal carriers (tones) are each modulated with a part of the total data bits. In this way the signal spectrum is divided in small bands. The amount of data on each band can be varied according to the signal to noise ratio (SNR) achieved in that particular band: for example 'low-frequency' tones can carry a higher order modulation format with high throughput (which is possible as the low frequency bands will typically have higher SNR) while high-frequency tones are modulated with lower-order constellations. In extreme cases (similar to fading in wireless applications) some sub-bands may not even carry any data. Such DMT signal can once again use the proposed switched capacitor approach. For

example, we can divide the entire required bandwidth (DC 20GHz as an example) into 10 channels shown as in Fig. 6.2. The different channels can then ben combined together using the SCPA scheme, the signal can be directly coupled to the Lumped MZM and thus transferred into the optical domain. The optical output would look like noise in the time domain. At the receiver side, the linear TIA will be required. After the TIA, the signal needs to be down converted into 10 channels with 2GHz bandwidth each.

- Transmiter-side feedforward equalization

  At high baudrates (≫10Gbaud), significant signal distortion and eye closure may occur due to bandwidth limitations of the electronics or the photonics, or due to chromatic dispersion. One option to overcome transmission limitations due to such signal distortion is to use equalization, in which a filter is used whose transfer function is the inverse of the channel response. In one particular implementation called feedforward equalization (FFE), this filter takes the shape of a tapped delay line, applied at the transmitter side. Fig. 6.3 shows how the switched capacitor approach can be used to implement such feedforward equalization. The input data has been copied into three channels with one clock cycle delay between each channel. By adjusting the ratio of the capacitors in the SCPA and the voltage swing on each channel (which can also be done by switching the capacitance in the capacitor bank), the FFE function can be realized to overcome the dispersion of optical channels.

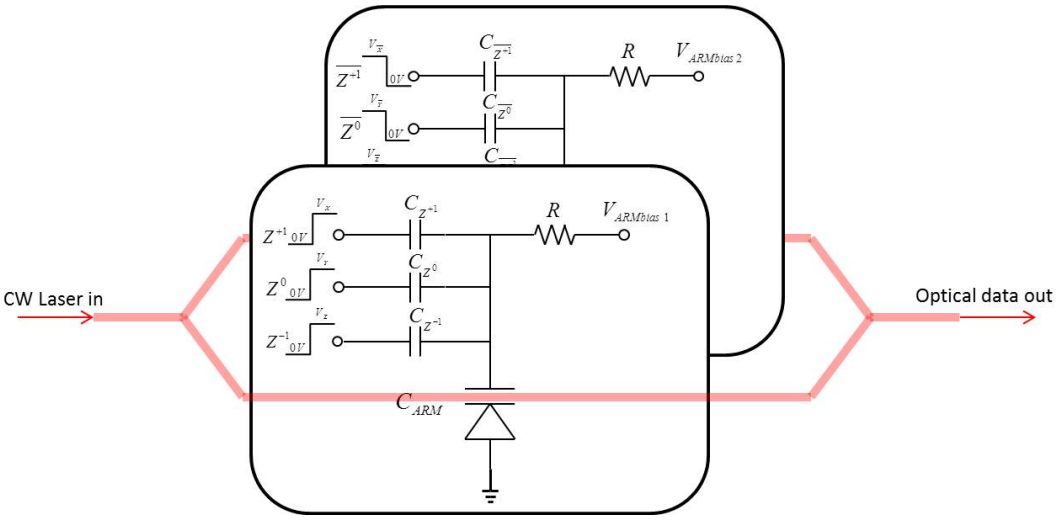


Figure 6.3: Modulator with FFE function

6.3 Summary of the thesis

In this thesis, I have briefly introduced the background of my PhD research, current state-of-the-art design of optical transmitters for short reach optical links, and my PhD research objectives. Then, I demonstrate how to optimize the performance of PAM-4 transmitters based on lumped Silicon Photonic Mach-Zehnder Modulators (MZMs) for short-reach optical links.

Firstly, we analyze the trade-off that occurs between extinction ratio and modulation loss when driving an MZM with a voltage swing less than the MZM's V_π. This is important when driver circuits are realized in deep submicron CMOS process nodes. Next, a driving scheme based upon a switched capacitor approach is proposed to maximize the achievable bandwidth of the combined lumped MZM and CMOS driver chip. This scheme allows the use of lumped MZM for high speed optical links with reduced RF driver power consumption compared to the conventional approach of driving MZMs (with transmission line based electrodes) with a power amplifier. This is critical for upcoming short-reach link standards such as 400Gb/s 802.3 Ethernet.

The driver chip was fabricated using a 65nm CMOS technology and flip-chipped on top of the Silicon Photonic chip (fabricated using IMEC's ISIPP25G technology) that contains the MZM. Open eyes with 4dB extinction ratio for a 36Gb/s (18Gbaud) PAM-4 signal are experimentally demonstrated. The electronic driver chip has a core area of only $0.11mm^2$ and consumes 236mW from 1.2V and 2.4V supply voltages. This corresponds to an energy efficiency of 6.55pJ/bit including Gray encoder and retiming, or 5.37pJ/bit for the driver circuit only.

For the future work, further system level analysis should be carried out to investigate the critical pattern issue of the PAM4 optical transmitter. The potential solutions toward 1pJ/bit are given (lumped EAM and micro-ring modulator). In addition, the advanced modulation formats (16 QAM, discrete multitone modulation, and FFE) are presented based on the switched capacitor approach.

Appendix A

Velocity Missmatch of TW-MZM

In a TW-MZM, the electrode is designed as a transmission line to distribute the capacitance over the entire device length. This allows a longer modulation length to enhance the modulation efficiency while maintaining a large bandwidth. To achieve optimum modulator performance, the microwave phase velocity should match the optical group velocity [25].

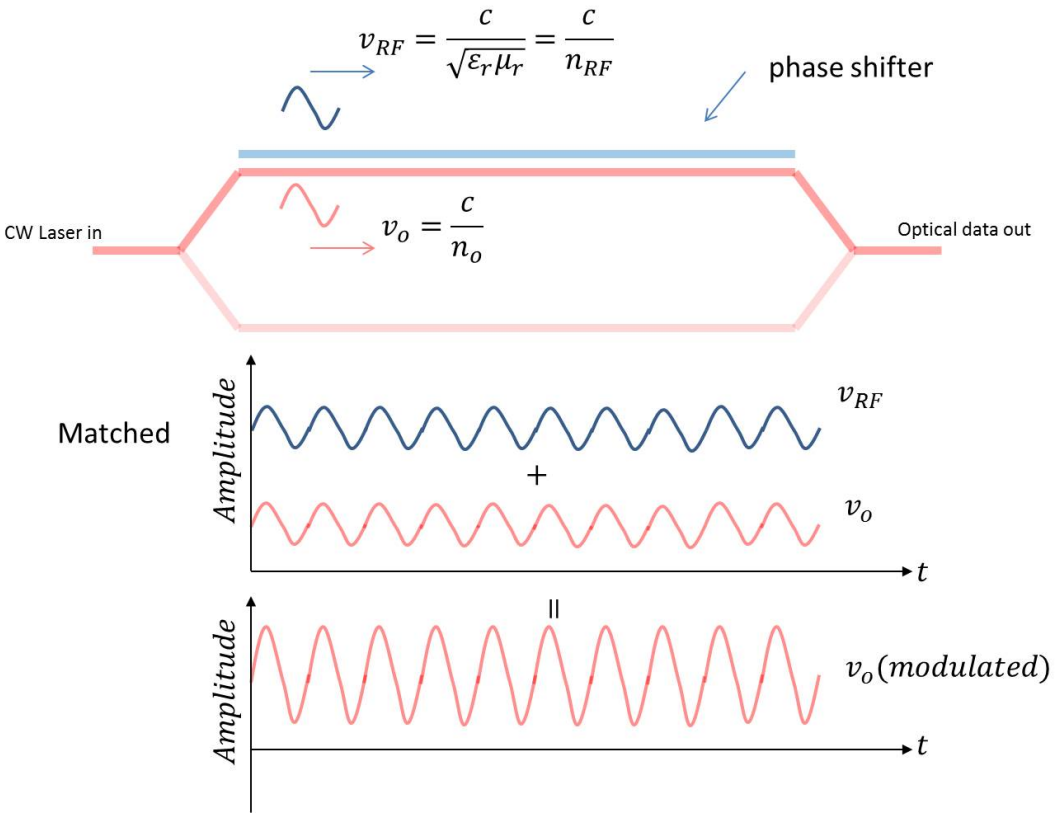


Figure A.1: Velocity Matching

The relationship between the group velocity of the microwave drive signal and

the optical signal is shown in Fig. A.1. Intuitively, if the phase of the microwave signal is matched with the optical signal, the amplitude of the optical output will be modulated and "amplified" by the electrical signal. However, if there is a velocity difference between optical signal and microwave signal, this is no longer the case. Consider, for example, the case where the electrical signal is travelling much faster than the optical signal: then the optical signal would just reach the output port when the electrical signal has already changed over a full cycle. In this case, the optical signal is not modulated. This is shown in Fig. A.2 clearly for any mismatch in velocities the amplitude of the final optical output is smaller compared to the matched case shown in Fig. A.1.

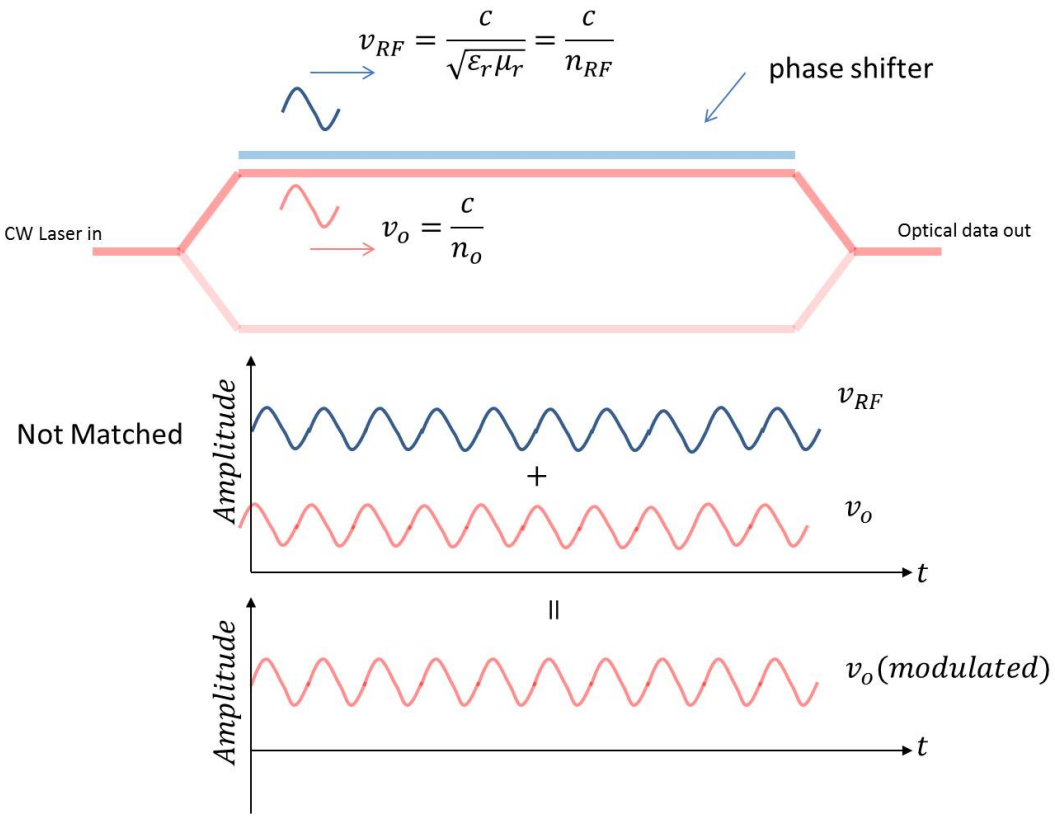


Figure A.2: Velocity Mismatching

The further analysis is based on the reference [19]. The normalized optical output power of a MZM can be written as follows: (A.1) as following :

$$P_{TWMZM(norm)} = \cos^2\left[\frac{\phi(V_{arm1}) - \phi(V_{arm2})}{2}\right] \tag{A.1}$$

where $\phi(V_{arm1})$ and $\phi(V_{arm2})$ are the phase shifts in both arms of the TW-MZM. To simplify the problem, we consider the TW-MZM as shown in Fig. A.3, where

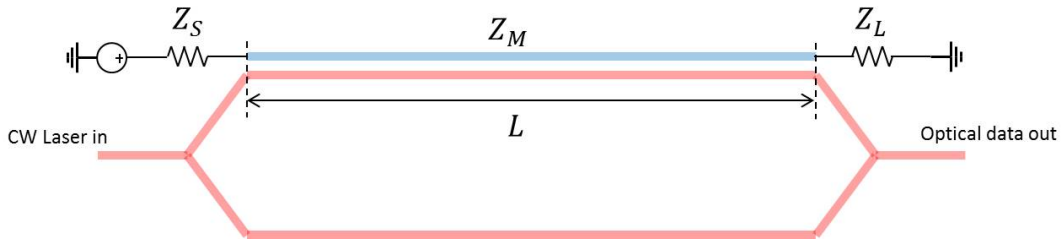


Figure A.3: TW-MZM

the second arm has no phase shift ($\phi(V_{arm2}) = 0$) and the impedance of the electrodes are perfectly matched with source and load ($Z_S = Z_M = Z_L$) without any attenuation. Therefore, the (A.1) can be simplified as following:

$$P_{TWMZM(norm)} = \cos^2\left[\frac{\phi(V_{arm1})}{2}\right] \tag{A.2}$$

Based on (A.2), the output optical power of the TW-MZM is a function of the phase shift introduced by one arms ($\phi(V_{arm1})$). To simplify the problem further, the phase shift can be derived based on Fig. A.4 which assume the direction of the microwave signal and optical signal are the same.

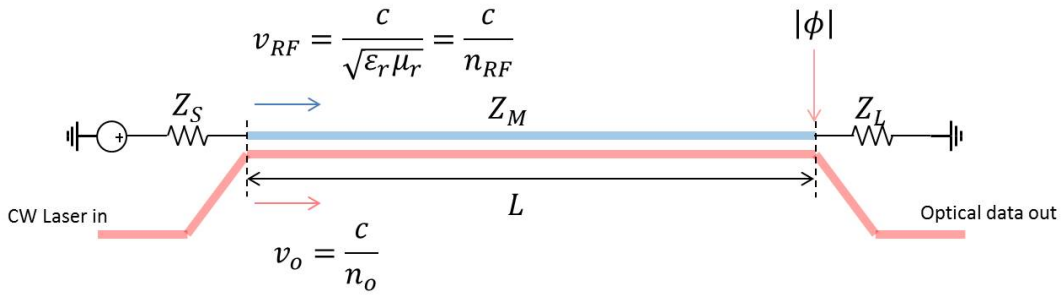


Figure A.4: One arm of the TW-MZM

Based on reference [27], we assume that a single frequency microwave signal along the electrode can be expressed as following:

$$V(z,t) = V_\pi \sin\left[2\pi f\left(\frac{z}{v_{RF}} - t\right)\right] \tag{A.3}$$

where V_π is the magnitude of the signal, v_{RF} is the group velocity of the RF signal, and $0 \leqslant z \leqslant L$. Hence, the total electro-optically induced phase shift at the end of the electrode for a certain time ($t = t_0$) can be derived as follows [27]:

$$\phi(t_0) = \int_0^L \Delta\beta(z)dz \tag{A.4}$$

$$\phi(t_0) = \Delta\beta \cdot \frac{\sin\left[f\pi L\left(\frac{1}{v_{RF}} - \frac{1}{v_0}\right)\right]}{f\pi L\left(\frac{1}{v_{RF}} - \frac{1}{v_0}\right)} \cdot \sin\left[2\pi f t_0 - f\pi L\left(\frac{1}{v_{RF}} - \frac{1}{v_0}\right)\right] \tag{A.5}$$

$$\Delta\beta = \pi \cdot k \cdot V_\pi \tag{A.6}$$

In (A.5), v_o and v_{RF} are the phase velocity of the optical signal and the electrical microwave signal respectively. Here, one assumption is added to further simplify (A.5). It is well known that a function of time with arbitrary wave shape can be described as a sum of sinusoidal waves by Fourier expansion [37]. Therefore, it is assumed that the phase velocity is constant for each frequency component in the Fourier expansion of the optical signal and electrical signal in TW-MZM, which means no chromatic dispersion for the optical signal and no electrical dispersion for the microwave signal. By taking this assumption, the phase velocity is equal to group velocity. Therefore, the following expressions can be established:

$$v_{RF} = \frac{c}{\sqrt{\varepsilon_r \mu_r}} = \frac{c}{n_{RF}} \tag{A.7}$$

$$v_0 = \frac{c}{n_0} \tag{A.8}$$

where c is the speed of light in vacuum, ε_r and μ_r are the relative permittivity and relative permeability of the TW-MZM's electrode respectively. By plugging (A.7) and (A.8) into (A.5), the expression of the overall phase shift can be simplified as following:

$$\phi(t_0) = \Delta\beta \cdot \frac{\sin\left[\frac{f\pi L}{c}\left(n_{RF} - n_0\right)\right]}{\frac{f\pi L}{c}\left(n_{RF} - n_0\right)} \cdot \sin\left[2\pi f t_0 - \frac{f\pi L}{c}\left(n_{RF} - n_0\right)\right] \tag{A.9}$$

In (A.6), k is the electro-optical parameter of the TW-MZM, which is dependent on the material and composition of the waveguide, for example, it is dependent on the doping concentration in case of a reversed biased PN junction. The

detailed physics are outside the scope of this thesis. The $\Delta\beta$ represents the amplitude of the phase shift, which is equal to π if the magnitude of microwave signal is V_π. Eventually, the total amplitude of induced phase retardation at the end of the electrode is the following [26] :

$$|\phi| = \pi \cdot \left| \frac{\sin\left[\frac{f\pi L}{c}\left(n_{RF} - n_0\right)\right]}{\frac{f\pi L}{c}\left(n_{RF} - n_0\right)} \right| \tag{A.10}$$

Substituting (A.10) into (A.2), the output power of the TW-MZM can be expressed as:

$$P_{TWMZM(norm)} = \cos^2\left\{ \frac{\pi}{2} \cdot \left| \frac{\sin\left[\frac{f\pi L}{c}\left(n_{RF} - n_0\right)\right]}{\frac{f\pi L}{c}\left(n_{RF} - n_0\right)} \right| \right\} \tag{A.11}$$

The transfer function of the TW-MZM is a $\cos^2(x)$ function which has been plotted in Fig. A.5 as blue curve. It could cause a problem if we just plotted the normalized optical power versus frequency based on (A.11), because this transfer function inverts the input signal, which means the full swing of the microwave signal would give 0 optical power and 0 swing would cause full optical power (from 0 to V_π in Fig. A.5).

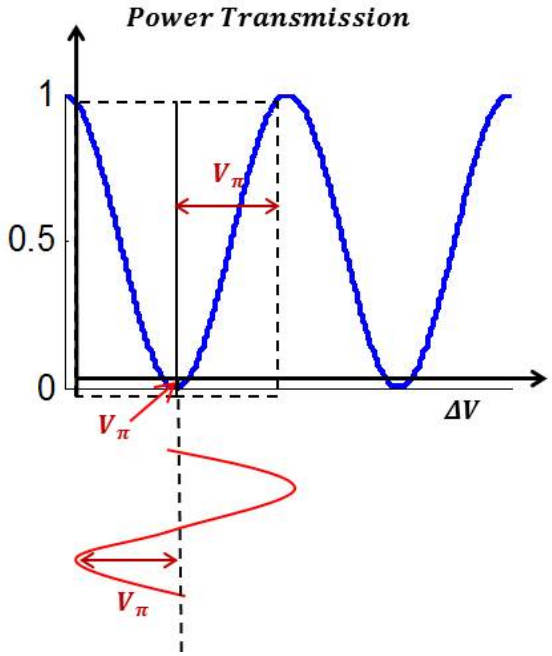


Figure A.5: DC biasing of the TW-MZM

Biasing the TW-MZM at the V_π point solves this problem. By doing so, the

optical output power and magnitude of the microwave signal would increase simultaneously (shown as red curve in Fig. A.5). The transfer function of the TW-MZM is then the following, without losing generality:

$$P_{TWMZM(norm)} = \cos^2\left\{\frac{\pi}{2}\cdot\left|\frac{\sin\left[\frac{f\pi L}{c}\left(n_{RF}-n_0\right)\right]}{\frac{f\pi L}{c}\left(n_{RF}-n_0\right)}\right| - \frac{\pi}{2}\right\} \tag{A.12}$$

Regarding the lumped MZM, note that in Fig. 2.6, there is an interesting problem for the lumped MZM connection in terms of velocity mismatch. Indeed, the microwave signal's propagation direction in the left half part of the electrode($L/2$) is opposite to the direction of the optical signal. To simplify the problem of the velocity mismatch in Lumped MZM, the right half of the electrode is removed, and perfect impedance matching for Z_L, Z_S and Z_M is assumed as shown in Fig. A.6. Indeed in the right half of the electrode, the directions of the microwave signal and the optical signal are the same. Based on Fig. 2.5, and (2.4), the $-1dB$ bandwidth of this right half part of the electrode with the same direction is beyond 60GHz. Therefore, no further analysis is required for this part of the electrode.

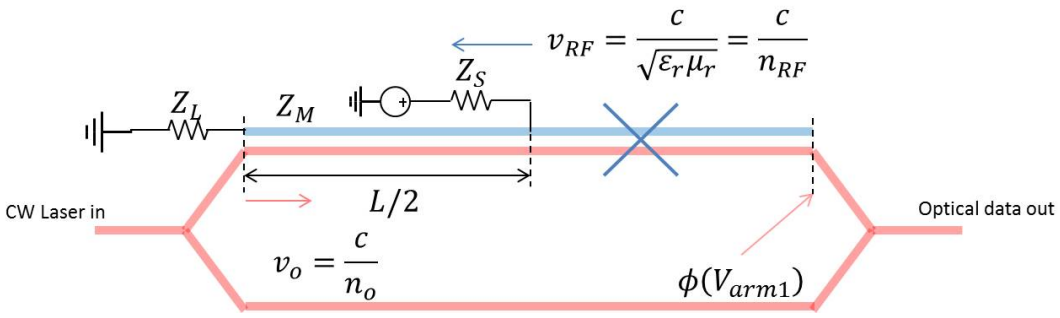


Figure A.6: Velocity mismatch for Lumped MZM

Based on the references [25] [26] [27], by assuming that the magnitude of the voltage swing across the half electrode is equal to V_π, the total amplitude of the induced phase retardation at the end of the electrode is the following:

$$|\phi(V_{arm1})| = \pi\cdot\left|\frac{\sin\left[\frac{f\pi L}{2c}\left(n_{RF}+n_0\right)\right]}{\frac{f\pi L}{2c}\left(n_{RF}+n_0\right)}\right| \tag{A.13}$$

Therefore, the new transfer function of the half electrode Lumped-MZM is the following [19]:

$$P_{TWMZM(norm)} = \cos^2\left\{\frac{\pi}{2}\cdot\left|\frac{\sin\left[\frac{f\pi L}{2c}\left(n_{RF}+n_0\right)\right]}{\frac{f\pi L}{2c}\left(n_{RF}+n_0\right)}\right| - \frac{\pi}{2}\right\} \tag{A.14}$$

Formula (A.14) has been plotted in Fig. A.7. The length $L/2$ is 0.75mm based on [20]. The normalized optical output power versus frequency has been plotted in three cases of mismatch $(n_0 + n_{RF})$. For the maximum mismatch $(n_0 + n_{RF} = 7.5)$, the -1dB bandwidth is more than 25GHz, more than sufficient for our application.

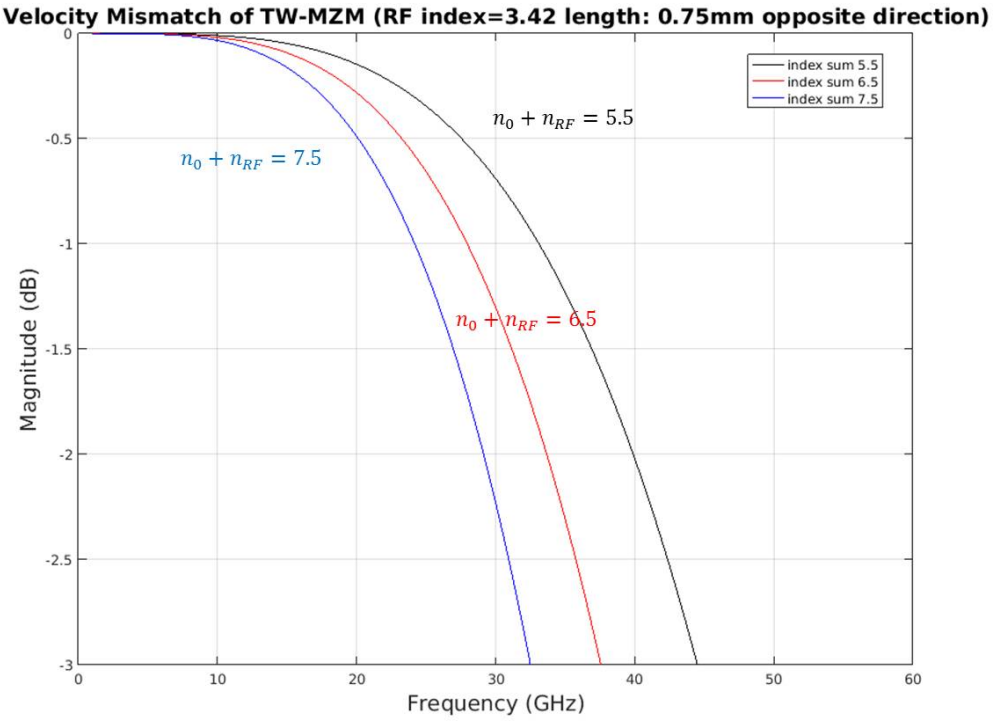


Figure A.7: Velocity mismatch for Lumped MZM with opposite propagation direction between microwave signal and optical signal

In summary, in terms of velocity mismatch, the Lumped-MZM can operate at DC-25GHz without any issue.

Appendix B

Boundary Frequency of the Transmission Line

An intuitive analysis of the boundary frequency (beyond which transmission line effects occur and hence the electrode can no longer be considered a lumped device) of the transmission line (TL) has been given in Chapter 2. Here is a mathematical analysis of an "open" (unloaded) transmission line. Based on the Lumped connection of MZM in Fig. 2.6, the equivalent circuit model can be simplified as Fig. B.1. In Fig. B.1, the transmission line is assumed to be ideal (no losses nor dispersion), and the length (L) and characteristic impedance (Z_M) of the TL have been given. The signal source is located on one side of the TL and the other side of TL is open, which means the load impedance Z_L is ∞. This corresponds to the lumped MZM electrode used in our PAM-4 transmitter. The input impedance (Z_{in}) can be calculated as following [28]:

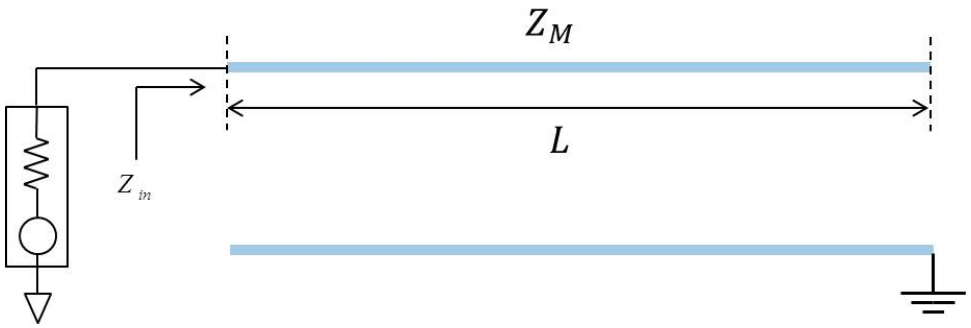


Figure B.1: Open loaded transmission line

$$Z_{in} = Z_M \cdot \frac{Z_L + jZ_M tan(\beta L)}{Z_M + jZ_L tan(\beta L)} \tag{B.1}$$

where β is the phase constant and shown as (B.2) and λ is the wavelength with:

$$\beta = \frac{2\pi}{\lambda} \tag{B.2}$$

Since the load impedance Z_L is ∞, equation (B.1) can be simplified as following:

$$Z_{in} = Z_M \cdot \frac{1 + j\frac{Z_M}{Z_L} tan(\beta L)}{\frac{Z_M}{Z_L} + jtan(\beta L)} \tag{B.3}$$

$$Z_{in} = Z_M \cdot \frac{1}{jtan(\beta L)} \tag{B.4}$$

$$Z_{in} = \frac{1}{j \cdot Z_M^{-1} \cdot tan(\beta L)} \tag{B.5}$$

In (B.5), the characteristic impedance (Z_M) is positive. Hence, as long as $tan(\beta L)$ is positive, the input impedance is always capacitive [28]. The following equation can be derived from $tan(\beta L) > 0$:

$$0 < \beta L < \frac{\pi}{2} \tag{B.6}$$

Plugging (B.2) into (B.6):

$$0 < \frac{2\pi}{\lambda} L < \frac{\pi}{2} \tag{B.7}$$

$$0 < \frac{2\pi}{v_{RF}/f} L < \frac{\pi}{2} \tag{B.8}$$

$$0 < 2\pi f \cdot \frac{L}{v_{RF}} < \frac{\pi}{2} \tag{B.9}$$

$$0 < f < \frac{1}{4} \cdot \frac{v_{RF}}{L} \tag{B.10}$$

where v_{RF} is the group velocity of microwave signal, which is equal to c/n_{RF} where c is speed of light in vacuum and n_{RF} is the microwave refractive index

of the TL. f is the frequency of the electrical signal. Then, equation (B.10) can be simplified as following:

$$0 < f < \frac{c}{4Ln_{RF}} \tag{B.11}$$

To conclude, as long as the frequency (f) is in the range (B.11), the Z_{in} in (B.5) acts as a capacitor. The expression for the boundary ($f_{\frac{\lambda}{4}}$) is then the following:

$$f_{\frac{\lambda}{4}} = \frac{c}{4Ln_{RF}} \tag{B.12}$$

For more informantion about the transformation between circuit impedance and TL, please check [28] : Richards' Transformation.

References

[1] Casimer DeCusatis. *Optical Interconnect Networks for Data Communications*. *IEEE Journal of Lightwave Technology*, Volume 32 Issue 4:pages 544–552, January 2014.

[2] D. M. Kuchta; A. V. Rylyakov ; C. L. Schow ; J. E. Proesel ; C. Baks ; P. Westbergh ; J. S. Gustavsson ; A. Larsson;. *64Gb/s Transmission over 57m MMF using an NRZ Modulated 850nm VCSEL*. In *Optical Fiber Communications Conference and Exhibition (OFC)*, pages 1–3, March 2014.

[3] Philip Moser; Philip Wolf; Gunter Larisch; Hui Li; James A. Lott; and Dieter Bimberg. *Energy-efficient Oxide-confined High-speed VCSELs for Optical Interconnects*. *Proc. SPIE 9001, Vertical-Cavity Surface-Emitting Lasers XVIII, 900103;*, (doi:10.1117/12.2044319):pages 1–8, February 2014.

[4] James Guenter; Bobby Hawkins; Robert Hawthorne; and Gary Landry. *Reliability of VCSEL>25Gb/s*. In *Optical Fiber Communications Conference and Exhibition (OFC)*, pages 1–3, March 2014.

[5] Fuad E. Doany. *High Density Optical Interconnects for High Performance Computing*. In *Optical Fiber Communications Conference and Exhibition (OFC)*, pages 1–3, March 2014.

[6] Daryl Inniss; and Roy Rubenstein. Silicon Photonics: Fuling he Next Information Revolution. Elsevier, ISBN-13: 978-0128029756, November 2016.

[7] Clint Schow; Fuad Doany; and Jeffrey Kash. *Get on the Optical Bus*. Technical report, IEEE Spectrum, August 2010.

[8] A. V. Krishnamoorthy; H. Schwetman ; X. Zheng ; R. Ho;. *Energy-Efficient Photonics in Future High-Connectivity Computing Systems*. *IEEE Journal of Lightwave Technology*, Volume 33 Issue 4:pages 889–900, February 2015.

[9] Douglas M. Gill; Chi Xiong ; Jonathan E. Proesel ; Jessie C. Rosenberg ; Jason Orcutt ; Marwan Khater ; John Ellis-Monaghan ; Andreas Stricker ; Edward Kiewra ; Yves Martin ; Yurii Vlasov ; Wilfried Haensch ; William M. J. Green. *Demonstration of Error-Free 32-Gb/s Operation From Monolithic CMOS Nanophotonic Transmitters*. *IEEE Photonics Technology Letters*, Volume 28 Issue 13:pages 1410–1413, July 2016.

[10] Gilles Denoyer; Chris Cole; Antonio Santipo; Riccardo Russo; Curtis Robinson; Lionel Li; Yuxin Zhou; Jianxiao Chen; Bryan Park; Frédéric Boeuf; Sébastien Crémer; Nathalie Vulliet. *Hybrid Silicon Photonic Circuits and Transceiver for 50Gb/s NRZ Transmission Over Single-Mode Fiber*. *IEEE Journal of Lightwave Technology*, Volume 33 Issue 6:page 1247–1254, March 2015.

[11] Xuezhe Zheng; Eric Chang; Philip Amberg; Ivan Shubin; Jon Lexau; Frankie Liu; Hiren Thacker; Stevan S. Djordjevic; Shiyun Lin; Ying Luo; Jin Yao; Jin-Hyoung Lee; Kannan Raj; Ron Ho; John E. Cunningham; and Ashok V. Krishnamoorthy. *A High-speed, Tunable Silicon Photonic Ring Modulator Integrated with Ultra-efficient Active Wavelength Control*. *Optics Express*, Volume 22 Issue 10:pages 12628–12633, May 2014.

[12] C.M. Tsai; and M.C. Chiu. *A 10Gb/s Laser-diode Driver with Active Back Termination in 0.18 μm CMOS*. In *IEEE International Solid-State Circuits Conference*, pages 222–223, February 2008.

[13] Chi Xiong; Douglas M. Gill; Jonathan E. Proesel; Jason S. Orcutt; Wilfried Haensch; and William M. J. Green. *Monolithic 56Gb/s silicon photonic pulse-amplitude modulation transmitter*. *OSA Optica*, Volume 3 Issue 10:pages 1060–1065, October 2016.

[14] Enrico Temporiti; Gabriele Minoia; Matteo Repossi; Daniele Baldi; Andrea Ghilioni; and Francesco Svelto. *A 56Gb/s 300mW Silicon-Photonics Transmitter in 3D-Integrated PIC25G and 55nm BiCMOS Technologies*. In *IEEE International Solid-State Circuits Conference*, pages 404–405, February 2016.

[15] M. Webster; C. Appel; P. Gothoskar; S. Sunder; B. Dama; K. Shastri. *Silicon Photonic Modulator based on a MOS-Capacitor and a CMOS Driver*. In *IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, pages 128–129, October 2014.

[16] CMOS065 Design Rule Manual 65nm Bulk CMOS Process Revision 1.2.5. STMicroelectronics, (Confidential).

[17] Govind P. Agrawal. Lightwave Technology. John Wiley and Sons, 1st edition, 2004.

[18] Hyundai Park; Matthew N. Sysak; Hui-Wen Chen; Alexander W. Fang; Di Liang; Ling Liao; Brian R. Koch; Jock Bovington; Yongbo Tang; Kristi Wong; Matt Jacob-Mitos; Richard Jones; and John E. Bowers. *Device and Integration Technology for Silicon Photonic Transmitters*. *IEEE Journal of Selected Topics in Quantum Electronics*, Volume 17 Issue 3:pages 671–688, March 2011.

[19] Peter J. Winzer; and Rene Jean Essiambre. *Advance Optical Modulation Format*. *Proceedings of IEEE*, volume 94 Issue 5:pages 952–985, May 2006.

[20] IMEC ISIPP25G Technology Handbook. Confidential Documents from Interuniversity Microelectronics Center, July 2014.

[21] S. Zhou; H. Wu; K. Sadeghipour; C. Scarcella; C. Eason; M. Rensing; M. Power; C. Antony; P. O'Brien; P. Townsend; P. Ossieur. *Driver Circuit for a PAM-4 Optical Transmitter using 65 nm CMOS and Silicon Photonic Technologies*. *IEEE Electronics Letters*, Volume 52 Issue 23:page 1939–1940, November 2016.

[22] Adithyaram Narasimha; Behnam Analui; Yi Liang; Thomas J. Sleboda; Sherif Abdalla; Erwin Balmater; Steffen Gloeckner; Drew Guckenberger; Mark Harrison; Roger G. M. P. Koumans; Daniel Kucharski; Attila Mekis; Sina Mirsaidi; Dan Song; Thierry Pinguet. *A Fully Integrated 4 $\times$ 10 Gb/s DWDM Optoelectronic Transceiver Implemented in a Standard 0.13 μm CMOS SOI Technology*. *IEEE Journal of Solid-State Circuits*, Volume 42 Issue 12:page 2736–2744, November 2007.

[23] Nicola Pavarelli; Jun Su Lee; Marc Rensing; Carmelo Scarcella; Shiyu Zhou; Peter Ossieur; and Peter A. O Brien. *Optical and Electronic Packaging Processes for Silicon Photonic Systems*. *IEEE Journal of Lightwave Technology*, Volume 33 Issue 5:pages 991–997, February 2015.

[24] Ming-Dou Ker; Chun-Yu Lin; and Yuan-Wen Hsiao. *Overview on ESD Protection Designs of Low-Parasitic Capacitance for RF ICs in CMOS Technologies*. *IEEE Transaction on device and materials reliability*, Volume 11 Issue 2:pages 207–218, June 2011.

[25] G. K. Gopalakrishnan; W. K. Burns; R. W. McElhanon; C. H. Bulmer; A. S. Greenblatt. *Performance and Modeling of Broadband LiNb03 Traveling Wave Optical Intensity Modulators*. *IEEE Journal of Lightwave Technology*, Volume 12 Issue 10:pages 1807–1819, August 1999.

[26] W. Leeb; A. Scholtz; E. Bonek. *Measurement of Velocity Mismatch in Traveling-Wave Electrooptic Modulators*. *IEEE Journal of Quantum Electronics*, Volume 18 Issue 1:pages 14–16, January 1982.

[27] R. Alferness; S. Korotky; E. Marcatili. *Velocity-matching techniques for integrated optic traveling wave switch/modulators*. *IEEE Journal of Quantum Electronics*, Volume 20 Issue3:pages 301–309, 1984.

[28] David M. Pozar. Microwave Engineering. John Wiley and Sons, 4th edition, 2012.

[29] K. Chang. Handbook of Optical Components and Engineering. Wiley, Hoboken, 2003.

[30] Sang-Min Yoo; Jeffrey S. Walling; Ofir Degani; Benjamin Jann; Ram Sadhwani; Jacques C. Rudell; and David J. Allstot. *A Class-G Switched-Capacitor RF Power Amplifier*. *IEEE Journal of Solid-State Circuits*, Volume 48 Issue 5, May 2013.

[31] Samuel Palermo; and Mark Horowitz. *High-Speed Transmitters in 90nm CMOS for High-Density Optical Interconnects*. *Proceedings of the 32nd European Solid-State Circuits Conference*, pages pages 508–511, September 2006.

[32] Chalvatzis T.; Yau K.H.K; Schvan P.; Yang M.T.; and Voinigescu S.P. *A 40-Gb/s Decision Circuit in 90-nm CMOS*. *Proceedings of the 32nd European Solid-State Circuits Conference*, pages 512–515, September 2006.

[33] Masayuki Mizuno; Masakazu Yamashina; Koichiro Furuta; Hiroyuki Igura; Hitoshi Abiko; Kazuhiro Okabe; Atsuki Ono; and Hachiro Yamada. *A GHz MOS Adaptive Pipeline Technique Using MOS Current-mode Logic*. *IEEE Journal of Solid-State Circuits*, Volume 31 Issue 6:pages 784–791, June 1996.

[34] Kaeriyama S.; Noguchi H.; Yamazaki Z.; Yamase T.; Hosoya K.; Okamoto M.; Tomari S.; Yamaguchi H.; Shoda H.; Ikeda H.; Tanaka S.; Takahashi T.; Ohhira R.; Noda A.; Hijioka K.; Tanabe A.; Fujita S.; and Kawahara N. *A 40Gb/s Multi-data-rate CMOS Transceiver Chipset with SFI-5 Interface*

for Optical Transmission Systems. In *IEEE International Solid-State Circuits Conference*, pages 358–359, February 2009.

[35] K. Hijioka; A. Tanabe; Y. Amamiya; and Y. Hayashi. *Crosstalk Analysis Method of 3-D Solenoid On-chip Inductors for High-speed CMOS SoCs*. In *International Interconnect Technology Conference*, pages 186–188, June 2008.

[36] Ali M. Niknejad. Electromagnetics for High-Speed Analog and Digital Communication Circuits. Cambridge University Press, 2007.

[37] Simon Ramo; John R. Whinnery; and Theodore Van Duzer. Field and Waves in Communication Electronics. John Wiley and Sons, 2nd edition, 1984.

[38] S. Galal; and B. Razavi. *Broadband ESD Protection Circuits in CMOS Technology*. *IEEE Journal of Solid State Circuits*, Volume 38 Issue 12:pages 2234–2340, December 2003.

[39] B. Kleveland; T. J. Maloney; I. Morgan; L. Madden; T. H. Lee; and S. S. Wong. *Distributed ESD Protection for High-speed Integrated Circuits*. *IEEE Electron Device Letters*, Volume 21 Issue 8:pages 390–392, August 2000.

[40] Adel Fatemi; Heinrich Klar; Friedel Gerfers; Dietmar Kissinger. *A 40 Gbps Micro-Ring Modulator Driver implemented in a SiGe BiCMOS Technology*. In *IEEE Compound Semiconductor Integrated Circuit Symposium*, pages 1–4, October 2016.

[41] Yung Hsu; Ta-Ching Tzu; Tien-Chien Lin; C. Y. Chuang; Xinru Wu; Jyehong Chen; Chien-Hung Yeh; Hon Ki Tsang; and Chi-Wai Chow. *64-Gbit/s PAM-4 20-km Transmission Using Silicon Microring Modulator for Optical Access Networks*. In *OSA Optical Fiber Communication Conference*, page M3H.2, March 2017.

[42] Jochem verbist; Michiel Verplaetse; Ashwyn Srinivasan; Peter De Heyn; Timothy De Keulenaer; Ramses Pierco; Renato Vaernewyck; Arno Vyncke; Philippe Absil; Guy Torfs; Xin Yin; Gunther Roelkens; Joris Van Campenhout; and Johan Bauwelinck. *First Real-Time 100-Gb/s NRZ-OOK Transmission over 2 km with a Silicon Photonic Electro-Absorption Modulator*. In *OSA Optical Fiber Communication Conference, Post deadline*, page TH5C.4, March 2017.

[43] Wen Yuan; Vladimir Aparin; Jeremy Dunworth; Lee Seward; and Jef-

frey S. Walling. *A Quadrature Switched Capacitor Power Amplifier*. *IEEE Journal of Solid State Circuits*, Volume 51 Issue 5:pages 1200–1209, May 2016.

[44] Huizhen Jenny Qian; Jian Orion Liang; and Xun Luo. *Wideband Digital Power Amplifiers With Efficiency Improvement Using 40-nm LP CMOS Technology*. *IEEE Transactions on Microwave Theory and Techniques*, Volume 64 Issue 3:pages 675–687, March 2016.