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GaN Nanowire Schottky Barrier Diodes

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***Abstract*—A new concept of vertical gallium nitride (GaN) Schottky barrier diode based on nanowire (NW) structures and the principle of dielectric REduced SURface Field (RESURF) is proposed in this paper. High threading dislocation density in GaN epitaxy grown on foreign substrates has hindered the development and commercialization of vertical GaN power devices. The proposed NW structure, previously explored for LEDs offers an opportunity to reduce defect density and fabricate low cost vertical GaN power devices on silicon (Si) substrates. In this work, we investigate the static characteristics of high voltage GaN NW Schottky diodes using 3D TCAD device simulation. The NW architecture theoretically achieves blocking voltages upwards of 700 V with very low specific on-resistance. Two different methods of device fabrication are discussed. Preliminary experimental results are reported on device samples fabricated using one of the proposed methods. The fabricated Schottky diodes exhibit a breakdown voltage of around 100 V and no signs of current collapse. Although more work is needed to further explore the nano-GaN concept, the preliminary results indicate that superior tradeoff between the breakdown voltage and specific on-resistance can be achieved, all on a vertical architecture and a foreign substrate. The proposed NW approach has the potential to deliver low cost reliable GaN power devices, circumventing the limitations of today's high electron mobility transistors (HEMTs) technology and vertical GaN on GaN devices.**

***Index Terms*—Gallium Nitride, Schottky diode, power semiconductor devices, wide bandgap, nanowire.**

I. Introduction

Gallium nitride (GaN) has emerged as a promising semiconductor material to replace Si for power applications owing to its wide bandgap, large critical electric field, high electron mobility, and high electron saturation velocity. However, unlike Si or Silicon Carbide (SiC), high quality bulk GaN substrates with reasonable fabrication costs are not currently available. Instead GaN epitaxy is heterogenically grown on Si, sapphire, or SiC foreign substrates. But the lattice mismatch between the substrate and epitaxy leads to very high threading dislocation densities (TDD) [1], [2]. Most of the GaN power devices are based on a lateral high electron mobility transistor (HEMT) architecture [3]–[5]. HEMT devices have several inherent drawbacks, including lack of avalanche capability and the current collapse phenomenon which are detrimental for reliable operation of these devices. Furthermore, the performance of state of the art GaN HEMTs, although superior to Si, is far below the theoretical limit of GaN as a material. Vertical GaN devices fabricated on freestanding GaN substrate with a reasonably low TDD (10^4-10^6 cm^{-2}) are recently reported with excellent voltage and on-resistance tradeoff [6], [7]. These devices exhibit good avalanche capability and no sign of current collapse. However, prohibitive cost of the bulk GaN wafers severely limits its prospect in commercial production. It would be highly desirable to realize vertical GaN device structures in the low TDD heteroexpitaxial GaN layer on a low cost Si substrate. In this paper, we explore a nano-structured GaN approach to tackle the TDD challenge caused by the lattice mismatch of heterogenic epitaxial material growth.

GaN nanowires (NW) grown on a foreign substrate have been extensively investigated as a scalable, low cost, and high performance approach for fabrication of LEDs and lasers [8]–[12]. GaN nanowires can elastically relax laterally, and accommodate lattice mismatch with Si substrate through pseudomorphic growth without dislocation formation as compared to thin-film heterostructures. Experimental studies have shown self-induced GaN NWs grown with a high surface to volume ratio on a Si substrate have a non-polar sideface and is virtually free of threading dislocations and other structural defects [13]–[15]. The TDs originating from the interface between the substrate and the nanowires bend out towards the outer walls of the nanowires within a short distance (< 50 nm) from the interface and finally end at the NW surface in order to minimize the dislocation line energy [11], [16]. This phenomenon limits the TD propagation into the active region of the NWs. Furthermore, recent investigations have alleviated the concerns regarding transformations of these TDs into other defects and near defect-free NWs are achieved for LEDs [16].

The unique properties of GaN nanostructures grown with bottom-up fabrication present a great potential for developing power device architectures offering high breakdown voltages, low leakage currents, and reliable device operation. This

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approach has been investigated for InAs wrap gated nanowire transistors [17] and more recently GaN enhancement mode power transistors having breakdown voltage of 100-140 V [18]. However, the NW power transistors have an unintentionally doped drift layer and exhibit significantly lower Figure of Merits (FoM) than the vertical GaN devices reported. Furthermore, there is a lack of discussion in these works on how to systematically achieve a higher breakdown voltage and a better FoM for power electronics applications. In general, this device concept is still in its infancy and its potential so far has remained largely unexplored. Important scientific issues and technological barriers must be addressed in the areas of novel device architectures, controlled nanowire synthesis, improved understanding of structural, electrical, and thermal properties of nano-GaN, and nano-GaN device fabrication before such a promise can be fully realized.

The objective of this paper is to investigate the realization of high voltage Schottky barrier diodes based on the proposed nano-GaN concept through extensive 3D TCAD modeling. Characteristics of the NW Schottky barrier diodes (NWSBD), in particular the method of achieving high blocking voltages based on the dielectric REduced SURface Field (RESURF) principle[19], [20] are studied, and device design considerations are discussed in detail. Two different fabrication techniques are proposed and preliminary experimental results on fabricated Schottky diodes are also reported. Both the theoretical and experimental results are compared with reported GaN HEMTs, bulk GaN diodes, GaN NW power transistor and theoretical limit of GaN at the end for a comparative understanding of the potential of the proposed NW architecture.

II. Device Concept And Fabrication Approach

The 3D schematic of the proposed NWSBD structure is shown in Fig 1. The n-type NWs are arranged as arrays of hexagonal pillars on a highly doped *n*+ Si (111) substrate. The pillars are free standing with or without a Silicon Nitride (Si_3N_4) layer depending on the fabrication approach used. Other substrates that may be used for this topography include sapphire, SiC or bulk GaN. The voids between NWs are refilled with SiO_2 or other dielectric materials. The sidewalls of the NWs may be deposited with ALD SiO_2 to reduce surface states. Ideally, a uniform Schottky metal layer such as nickel (Ni) forms the anode at the top, and an ohmic cathode is formed at the bottom. From practical considerations, the NW diameter and the gap between the NWs are in the range of several hundreds of nanometers while the NW height is in the range of a few micrometers. The base of the NWs is heavily doped (~$5x10^{18}$ cm^{-3}) while the rest of the NW is doped lightly (~10^{17} cm^{-3}) with Si as the dopant.

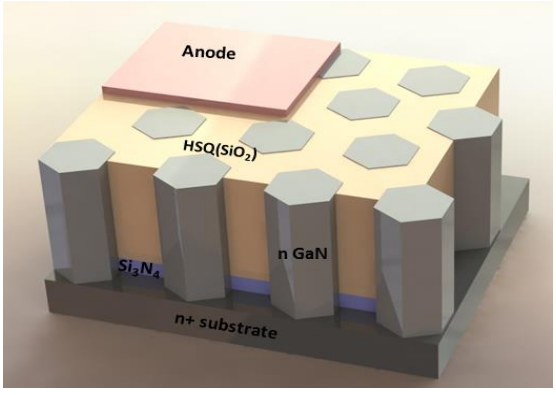


Fig. 1. Schematic of the GaN NW Schottky diode on a Si substrate (111) for the pure vertical case with a top anode and a back cathode. The nitride layer may or may not be present depending on the fabrication approach used. The top anode is uniform over the entire top wafer, but for clarity only a part of it is shown.

Two different approaches are proposed to fabricate the NWSBDs - the first being a top-down subtractive process while the second a bottom-up additive process. The top-down subtractive process starts with the growth of a thick GaN epitaxial layer (1-5 μm) on a (111) Si *n*+ substrate by metal oxide vapor phase epitaxy (MOVPE) in a controlled atmosphere of trimethylgallium (TMGa), disilane (Si_2H_6) and ammonia (NH_3) with hydrogen (H_2) as a carrier gas. The flow of disilane is controlled to grow a Si-doped *n*+ base epitaxial layer (~$5x10^{18}$ cm^{-3}) and then a *n*- epitaxy on top of it with doping concentrations of $2x10^{17}$ cm^{-3} to $5x10^{17}$ cm^{-3}. A 2D array of nanospheres (NSs) of desirable diameter (100-1100 nm, here 500 nm NSs were used) is formed by scooping them from the water surface as described elsewhere [21]. The array is then used as a hard mask for an ICP chlorine-based dry etch to form the GaN NCs beneath the NSs. The NSs are removed by treating the samples in an ultrasonic bath. The NCs are then annealed at ~900°C in a NH_3-N_2 atmosphere in order to force the dislocations to bend out towards the sidewalls similar to the work reported in [22]. The space between NCs is refilled with spin-on hydrogen silsesquioxanes (HSQ) which after bake/annealing transforms to conventional SiO_x. The excessive SiO_x then can be removed by chemo-mechanical polishing or back etched (using fluorine-based dry etch) to expose the top *c*-plane facet of the GaN NCs. A Schottky metal film/stack is then deposited and patterned to form the anode electrode. A passivation layer can then be used to protect the Schottky anode metal.

The second method is a bottom up additive approach. This method is the preferred method of fabricating NWSBDs as it has the theoretical potential to achieve even lower extended defect density. The hexagonal Wurtzite NWs (0001) are directly grown on a heavily doped *n*+ Si substrate (111) using a selective area MOVPE. The substrates are prepared with a silicon nitride (Si_3N_4) thin film on top which is then patterned through photo or electron beam lithography to produce an array of holes with diameters ranging from 100 nm to 500 nm and pitch of 100 nm to 500 nm between them. The selective area MOVPE growth uses these patterned holes to define the location of NWs, similar to the self-assisted growth method but without the need for a metal catalyst to a height of 1-5 μm on the exposed surface inside these holes. Similar to the first approach, the NWs are doped selectively during their growth by controlling the flow of disilane. Once the free standing NWs are grown, refilling the voids between the NWs are carried out similar to the first approach, first with ALD sidewall deposition and then HSQ refill and cure. For this approach, the TDs are expected to bend out during the growth of the NCs themselves

and additional post-growth annealing will not be necessary. For a pure vertical current flow, a uniform top anode and a back cathode is desired. Although successful growth of GaN NWs directly on a Si substrates have been reported using MBE [23] or catalyst-assisted MOVPE [24], the ideal vertical device structures with the back cathode do present a technical challenge for the catalyst-free MOVPE growth approach which previously required a highly resistive AlN buffer layer between the GaN NWs and the Si substrate. In this approach, we expect the GaN NWs to be grown without the AlN buffer layer and the cathode on the back of the *n*+ Si substrate.

III. TCAD Simulation and Design Optimization

The NW Schottky barrier diode concept introduced in the previous section is investigated with 3D TCAD device simulation (Sentaurus Synopsys workbench [25]). Physical models and corresponding calibrated model parameters for bulk GaN with a TDD of 10^4-10^6 cm^{-2} [26] are used to simulate the NW structure in this work. The 3D unit cell structure and the cross-sectional view of the simulated NWSBD are shown in Fig 2. For simulation purposes, the hexagonal NW is approximated as symmetrical cylindrical structure on the heavily doped *n*+ substrate interleaved in a matrix of SiO_2. The anode Schottky metal is assumed to have a work function of 5.01 eV, corresponding to that of Ni. The bottom cathode has an ohmic contact. The base of the NW is heavily doped at $5x10^{18}$ cm^{-3}. The reason for using a high base doping is to stop the expansion of the depletion region in the blocking mode, and prevent the electric field from reaching the high TDD region near the NW-substrate interface. From a real device point of view, this prevents the disruption of the electric field and premature breakdown of the microplasma. However, this lead to two height parameters- the height of the NW (T) and the effective height of the NW which actually supports the voltage (T_{eff}). The effect of different doping concentrations, NW heights, NW diameters and space between adjacent nanowires on the breakdown voltage and on-resistance are investigated in detail.

A. *Reverse Blocking*

The breakdown voltage of a conventional 1D p-n/Schottky junction is mainly determined by the doping concentration and dimension of the lightly doped drift region. For the proposed GaN NWSBDs, breakdown voltage depends on the NW doping concentration, height, and diameter as well as the oxide gap between adjacent NWs owing to a strong dielectric RESURF effect as discussed afterward.

Considering the practical limitation of the current fabrication technology, the maximum aspect ratio of a single NW (i.e. height to diameter ratio) is assumed to be no more than 10. The NW diameter is selected to be 500 nm with a SiO_2 spacing of 500 nm in between two adjacent NWs in simulation. The total height of the simulated NW is 5 µm and the base of the NW is a heavily doped *n*+ field-stop region with a height of 500 nm leaving the maximum effective height which support voltage in reverse bias at 4.5 µm. With this maximum effective height, the simulated breakdown voltage as a function of NW doping concentration is shown in Fig. 3(a). The doping concentration

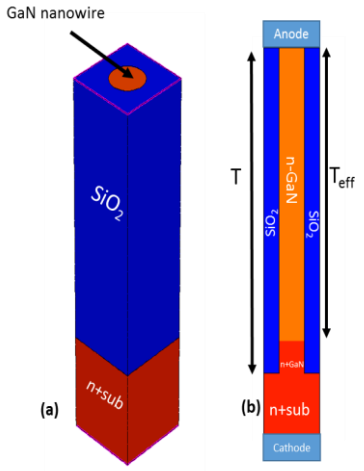


Fig. 2(a) 3D structure and (b) cross-section along the Z axis of a typical GaN NW Schottky barrier diode. The diameter of the NW is 500 nm with an inter-NW oxide gap of 500 nm and an effective height of 2.3 µm.

for the drift region is varied from $2x10^{16}$ cm^{-3} to $1x10^{18}$ cm^{-3}. Breakdown voltages are recorded when the ionization integral equals unity in TCAD simulation. The breakdown voltage of NWSBD generally decreases with increasing doping concentration to about 70 V for a doping concentration of $1x10^{18}$ cm^{-3}. For doping concentrations lower than $8x10^{16}$ cm^{-3} the reverse blocking voltage is limited by punch-through at around 1200V for the NW height limitation. Vertical bulk GaN diodes have been reported with epi doping concentrations as low as $2x10^{16}$ cm^{-3} [27], [28]. However, for our fabrication approach, the minimum controllable doping concentration is $2x10^{17}$ cm^{-3}. A theoretical breakdown voltage of 420 V can be achieved with this doping concentration as shown in Fig. 3(a). Since it is in the non-punch-through region, the effective height of the NW is varied from 0.8 µm to 3.8 µm to find the optimized height as shown in Fig. 3(b). Beyond 2.3 µm the breakdown is non-punch through and additional drift height does not result in breakdown voltage increase while the breakdown falls sharply for shorter NW heights. The maximum breakdown voltage of 420 V can be achieved with a controlled doping concentration of $2x10^{17}$ cm^{-3} at an effective NW height of 2.3 µm.

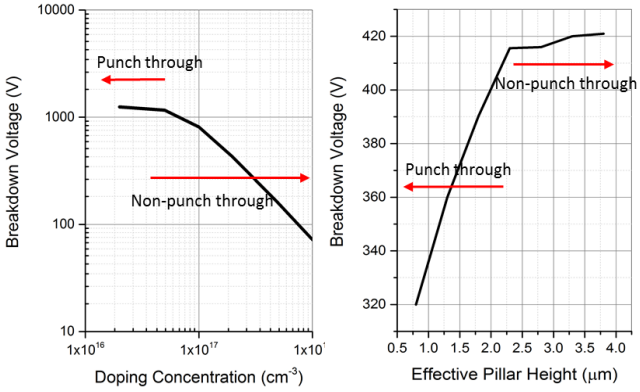


Fig 3(a) Simulated breakdown voltage dependence on the doping concentration for an effective NW height of 4.5 µm and (b) breakdown voltage dependence on the NW height for the controlled minimum drift doping concentration of $2x10^{17}$ cm^{-3}. The NW diameter is 500 nm with a 500 nm inter-NW oxide gap

Unlike one-dimensional p-n/Schottky junction, the breakdown voltage of the NWSBD is significantly influenced by the dielectric region surrounding it. A reverse biased p-n/Schottky junction with a very small cross-section can have a lower peak electric field and higher breakdown voltage due to the fringing effect of the surrounding dielectric capacitor which has a desirable uniform electric field distribution. This effect is referred to as the dielectric RESURF principle which is used to extend breakdown voltage of Si CMOS power devices [19]. The NWSBD structure, owing to its small diameter, takes full advantage of this voltage extension principle and offers a blocking voltage higher than its 1D bulk counterpart. The large band gap and the true 3D nature allow the GaN NWSBD to benefit greatly from the dielectric RESURF effect than Si power devices. The electric field and electrostatic potential distributions at the breakdown voltage for the optimized NWSBD are shown in Fig. 4(a) and 4(b), respectively. It can be observed that the e-field expands under the anode metal at the top into the adjacent oxides. The equipotential lines are distributed fairly uniformly along the drift region of the NWSBD, significantly different from that of an 1D diode. This is because the parallel plate oxide capacitor formed between the anode metal and the *n*+ base has a truly uniform equipotential distribution in the oxide, and when in contact with the NW, forces the otherwise non-uniform potential distribution in the GaN NW to conform to that in the surrounding oxide through the fringing effect. This is the basic principle for dielectric RESURF which is utilized in the NWSBD design. The electric field and the electrostatic potential through the center of the NW along the Z-axis is shown in Fig 4(c). The breakdown is borderline punch-through as the electric field drops to zero right before it reaches the highly doped *n*+ base with a peak electrical field of 3.8 MV/cm at the Schottky junction.

For dielectric RESURF based power devices, breakdown voltage depends on the permittivity and width of both the semiconductor and the dielectric layers [19], [29], [30]. The dependence of shown in Fig. 5 for an effective NW height of 2.3µm breakdown voltage on the NW diameter and the oxide gap between adjacent NWs is and constant doping concentration of $2x10^{17}$ cm^{-3} along with the 1D limit for the aforementioned doping. Breakdown voltage increases with decreasing NW diameter and increasing oxide gap. This is expected from the understanding of dielectric RESURF as a thinner NW is easily depleted with a thicker oxide, but the extent of the same is dramatic. This might be attributed to the wide bandgap of GaN which amplifies the otherwise underwhelming dielectric RESURF effect. With a 200 nm NW diameter and an oxide gap of 500 nm, breakdown voltage of nearly 700 V can be achieved which is 2.8 times higher than what is possible for a conventional 1-D breakdown without an oxide and 1.6 times higher than that of the optimized structure with 500 nm diameter and 500 nm oxide gap. For a thick NW and a thin oxide gap, the breakdown voltage nears the 1-D breakdown limit due to the weakening of the dielectric RESURF effect.

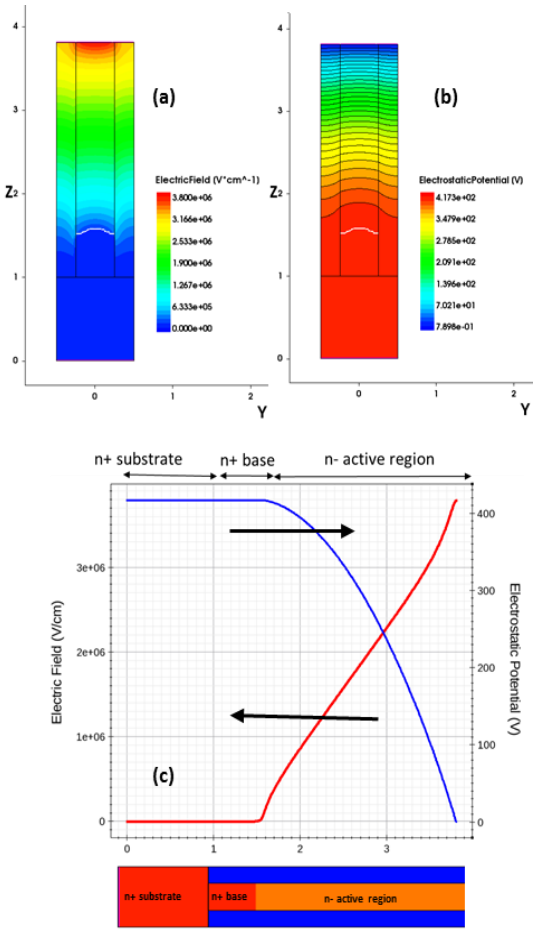


Fig 4. Simulated (a) electric field and (b) electrostatic potential contours through the optimized NWSBD cross-section and (c) electrostatic potential and electric field profile along the Z-axis at breakdown. The NW diameter is 500 nm with a 500 nm inter-NW oxide gap and effective NW height of 2.3 µm and a drift doping concentration of $2x10^{17}$ cm^{-3}.

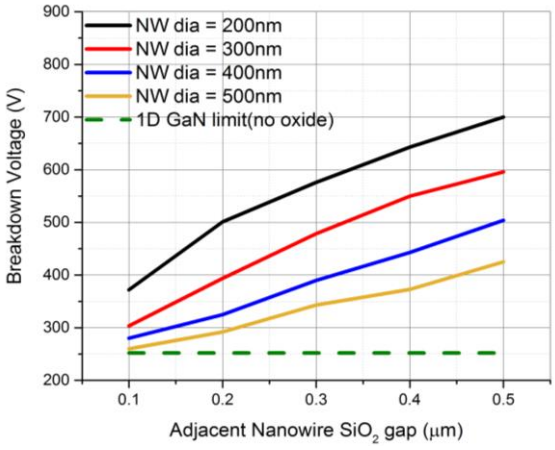


Fig. 5. Dependence of simulated breakdown voltage on NW diameter and the SiO_2 gap between adjacent NWs for a drift doping concentration of $2x10^{17}$ cm^{-3} and a height of 2.3 µm.

The simulated electric field profile at breakdown through the center of the NW along the Z-axis for different NW diameters and oxide gap combinations is shown in Fig 6. The effective NW height is 4.3 µm with a constant doping concentration of $2x10^{17}$ cm^{-3}. Varying the ratio of the NW diameter to the oxide gap modulates the electric field profile significantly even for a

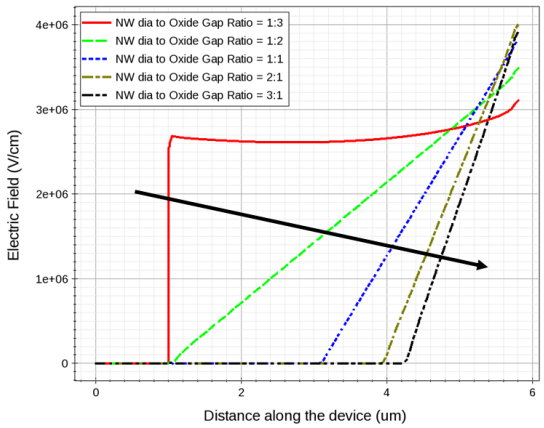


Fig. 6. Simulated electric field profiles along the Z-axis for different NW diameter and oxide gap ratios. The NW diameters are 500 nm with a 500 nm inter-NW oxide gap.

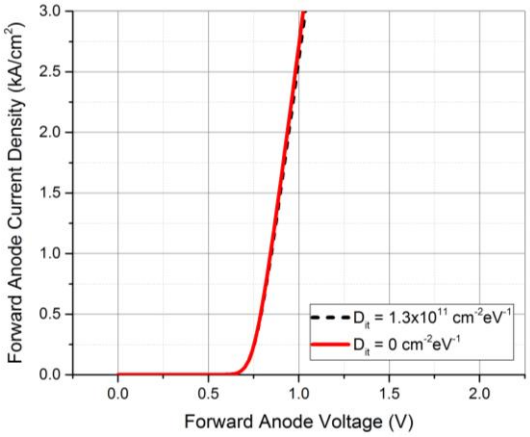


Fig. 7. Simulated forward bias characteristics of the NWSBD with a drift doping concentration of $2x10^{17}$ cm^{-3} and effective pillar height of 2.3 µm. The NW diameter is 500 nm with a 500 nm inter-NW oxide gap.

constant doping concentration. For a NW diameter to oxide gap ratio of 1:3, the electric field profile is almost rectangular, signifying strong depletion. With increasing ratio, the e-field is less modulated and for ratios upwards of 3:1, the dielectric RESURF effect is completely diluted. As seen from Fig. 6, the operation of the NWSBD can be changed from non-punch through to punch through and vice versa by simply changing the oxide gap. The dielectric RESURF effect provides two extra parameters to design the NW devices with an increased voltage rating which might have been otherwise difficult to achieve with the height and doping constraints. In addition, a strong dielectric RESURF reduces the electric field at the Schottky contact. This field reduction along with the small carrier lifetime and the large bandgap of GaN theoretically has the possibility to reduce the tunneling leakage current in the reverse bias. Also, pure avalanche breakdown can be achieved instead of leakage induced breakdown since the e-field is terminated by design using the high base doping before it reaches the high TDD region.

B. Forward Conduction

Forward conduction characteristics are simulated and knee voltage and on resistance is extracted for the NW architecture for different designs. The current flow for the simulated ideal vertical structure in the forward bias is from the top anode, through the NW bulk, into the Si substrate and then out through the back cathode. This vertical current path provides several challenges and a few assumptions are made during the simulations to accurately model the behaviors of the NWSBD.

Studies on GaN-Schottky interface has pointed out to the presence of a defect related tunneling phenomenon in association with the thermionic and field thermionic field emission. The defect related tunneling is attributed to a combination of interface states and deep level traps that are within a tunneling distance of the interface [31]. The deep level traps are attributed to the contamination layer on clean GaN and threading dislocations that reach the surface. Nevertheless, only the interface states at the Schottky contact are incorporated in our simulations and the effect of the deep level traps are ignored. Electrons are assumed not to encounter any threading dislocation induced deep level traps while moving through the bulk of the NWs. However, due to the high surface to volume ratio of the NWs, much of the current flow is along the sidewalls. The interface states at the GaN/SiO_2 boundary is expected to influence the current flow. Interface state density (D_{it}) for SiO_2/GaN interface has been reported around $1.3x10^{11}$ $cm^{-2}\cdot eV^{-1}$ [18] in the non-polar a-plane which is used in this work. The current path also includes the highly doped and high TD dense region near the base of the NWs. As this region is expected to be less than 50 nm in height, the effect of defects on the on-state resistance would be minimal when compared to the contribution of the drift layer which is almost 50 times greater. The effect of the defects in this region however needs to be analyzed in detail and is to be reported in a later work. Working under these assumptions, the forward bias characteristics for the optimized NW with 500 nm diameter, 500 nm oxide gap, 2.3 µm effective height and a doping concentration of $2x10^{17}$ cm^{-3} is simulated. The active area of the simulated NWs is 1965 μm^2. The forward bias I-V characteristics are shown in Fig. 7 with and without the interface states. The specific on-state shows a small decrease when interface states are incorporated in the simulations and has expectedly no effect on the knee voltage. For this case the simulated diodes show a knee voltage of around 0.75 V which is in the vicinity of reported data for GaN on GaN vertical devices [28] with low defect densities. The specific differential on resistance (R_{ON}) extracted is 0.091 $m\Omega\cdot cm^2$ leading to a figure of merit, FoM (V_{RB}^2/R_{ON}) of 1938 $MW\cdot cm^{-2}$.

The optimization of the NWSBD includes both the breakdown voltage and the specific R_{ON} working under constraints of a maximum NW height and a minimum controlled doping. A thin NW with a thick oxide gap offers a higher breakdown voltage but a lower effective cross-section for the current path and adds to extra on-resistance. This is shown in Fig. 8 where both the specific R_{ON} and the breakdown voltage is plotted for various NW diameters and oxide gaps. The specific on resistance increases with increased oxide gap and decreasing NW diameters expectedly.

Although with decreasing NW diameter the effective active area for current flow decreases, surprisingly the FoM (V_{RB}^2/R_{ON}) showed a gradual increase. FoM for different NW diameter and a constant oxide gap of 100 nm is shown in Table

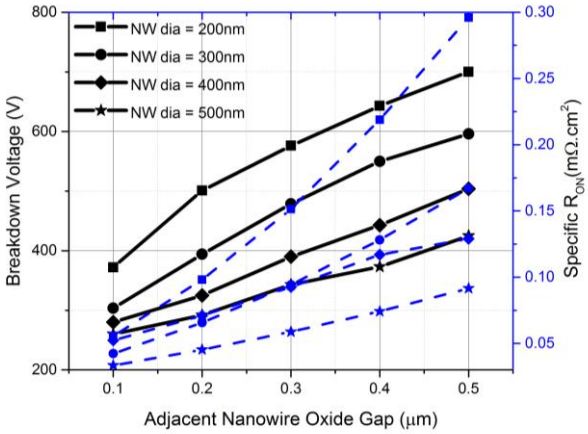


Fig. 8. Specific differential RON (dashed lines) and breakdown voltage (solid lines) for different NW diameters and oxide gap for the NWSBD. The NWSBDs have a drift doping concentration of $2x10^{17}$ cm^{-3} and effective pillar height of 2.3 μm.

I along with the breakdown voltage and specific on resistance for a doping concentration of $2x10^{17}$ cm^{-3} and an effective drift height of 2.3 μm. The same trend was observed for other constant oxide gaps. This is attributed to the dielectric RESURF effect which allows the loss of active area to be compensated giving a higher FoM. From Table I it can be seen that a thinner NW is preferred both in terms of the rated voltage as well as the overall FoM. The simulated FoM obtained for the thinner NWs (~2516·1 MW.cm^{-2}) is comparable to current state of the art GaN HEMTs (2.5 GW·cm^{-2}) [32].

TABLE I
FOM COMPARISON FOR DIFFERENT NW DIAMETER (CONSTANT OXIDE GAP)

NW diameter (nm)	Breakdown Voltage (V)	Specific R_{ON} (mΩ·cm^2)	FoM V_{RB}^2/R_{ON} (MW·cm^{-2})
200	372	0.055	2516.1
300	303	0.042	2185.9
400	280	0.037	2118.9
500	255	0.033	1970.5

IV. PRELIMINARY EXPERIMENTAL RESULTS AND DISCUSSION

Quasi vertical NWSBDs are fabricated by the top down subtractive fabrication approach discussed in Section II. The SEM images of the fabricated samples are shown in Fig. 9. The fabricated NWSBDs are densely packed, free standing perfectly hexagonal structures uniformly distributed in a matrix of SiO_2. A sapphire instead of Si substrate was initially used but our future work will extend into the study of Si substrate. The fabricated NWs are 500nm in diameter with an oxide gap of 50 nm and a pillar height of 1μm. The controlled doping concentration is $5x10^{17}$ cm^{-3} while the base is doped at $5x10^{18}$ cm^{-3} and annealed at 500°C for 60 s in N_2 atmosphere. Ni:Ti:Pt:Au (50 nm:10 nm:50 nm:200 nm) stack is used as the Schottky contact (anode)and is deposited as circular rings of 50 μm in diameter on the top surrounded by the bare cathode. Note that these quasi-vertical NWSBDs do not have direct backside cathode contact due to the use of nonconductive sapphire substrate. Instead the cathode contact is through a contact to the *n*+ base from the topside of the sample.

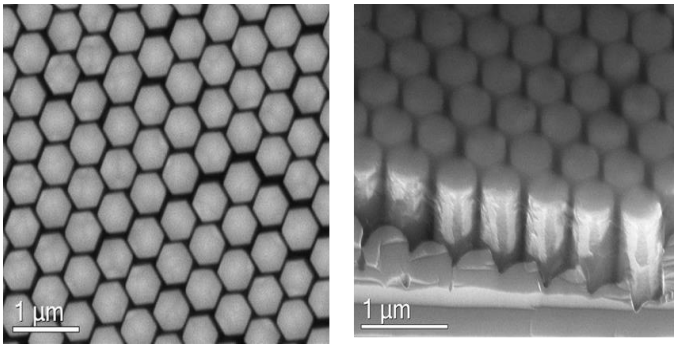


Fig. 9. (a) top down and (b) tilted SEM images of the fabricated NWs using the top down subtractive approach

Forward and reverse bias measurements are carried out for the fabricated diodes and shown in Fig. 10. The maximum breakdown voltage obtained is 100 V with a leakage current of 2.2 mA at 90 V. These preliminary NWSBD samples are fabricated to verify the NW concept for high power rectifying applications and are yet to be fully optimized. Due to the practical fabrication challenges, our initial Schottky device samples do not have the same optimal device structure as our modeling work suggested. The lower than expected breakdown voltage is attributed to a small NW height of roughly 1 μm and a high NW doping level estimated at $5x10^{17}$ cm^{-3}. Also with the circular top cathode layout and absence of an edge termination, the breakdown voltage is expected to be lower due to the weakening of the dielectric RESURF effect at the edge cells. TCAD simulations on the same fabricated device structure yield a breakdown voltage of 97 V, closely matching the measurement results. Simulation results also show that about 300 nm of the NW drift region is not depleted and the diode undergoes breakdown due to the field crowding at the edge cells due to a non-terminated top anode. The high leakage current may be attributed to a number of factors including surface states at the Schottky interface during fabrication and also to the relatively high doping level of the GaN NW drift region. With a passivated NW top surface before Schottky metal deposition and lower doping concentrations for the active region, leakage current is expected to decrease significantly. Also, with a back cathode, proper edge termination and an optimized NW diameter to oxide gap ratio, the dielectric RESURF effect is expected to be pronounced which will surely increase the breakdown voltage and also reduce the field at the Schottky anode, thereby further reducing the leakage current.

Repeated forward biasing was performed on the fabricated GaN NWSBDs to investigate presence of the current collapse phenomenon. In spite of repetitive biasing, the diodes did not show any sign of current collapse. The current density of the fabricated NWSBDs is as high as 2.54 kA·cm^{-2}. The static specific R_{ON} extracted was 0.59 mΩ·cm^{-2} with a knee voltage of 0.75 V. In contrast, the TCAD calculated specific R_{ON} is 0.0117 mΩ·cm^{-2} for the same structure, roughly 50 times lower than the measured value. This large difference might be attributed to a number of factors. The fabricated NWSBD samples have a quasi-vertical structure and hence the current flows downward through one NW from the anode to the thin *n*+ base layer, laterally in the *n*+ base, and up through another lightly doped NW to the cathode. This long current path along with the associated current spreading effect certainly increases

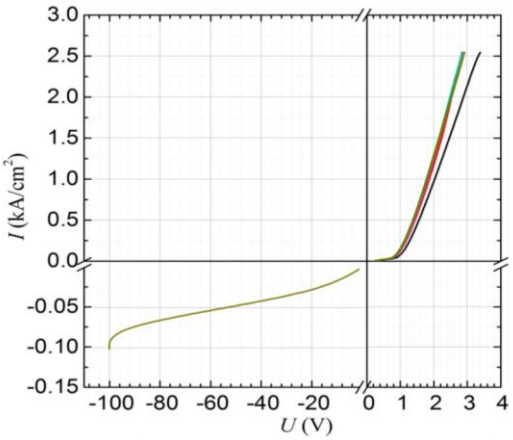


Fig. 10. Measured forward and reverse bias characteristics of the fabricated NW Schottky diodes.

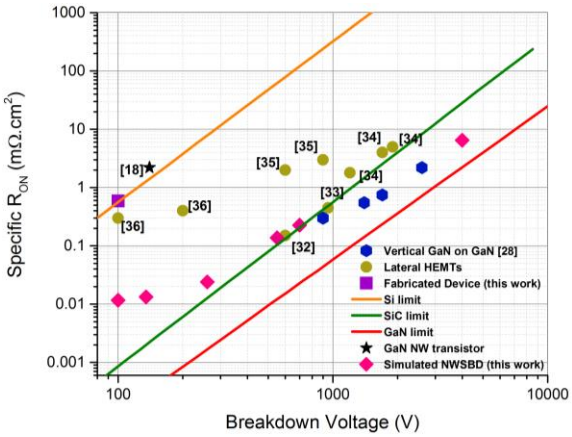


Fig. 11. FoM comparison of the simulated and fabricated NWSBD to the 1-D limits of GaN, SiC and Si and other state of the art GaN devices.

the on-state resistance. The deep level traps at the *n*+ base of the NW which is neglected for simulation purposes might degrade electron mobility which needs further work in order to be verified. Also, the surface states need to be evaluated in detail for the fabricated devices to account for the recombination along the surface of the NWs. In addition, contact resistances which add to a large chunk of the measured resistance was ignored for the simulation work.

The enhancement mode GaN nanowire power transistors with an unintentionally doped drift region have been reported in [18] with a breakdown voltage of 100 V-140 V and an specific on-resistance of 2.2 mΩ·cm^2, leading to a maximum (V_{RB}^2/R_{ON}) FoM of 8.9 MW·cm^2. In comparison, our fabricated NWSBD exhibits a (V_{RB}^2/R_{ON}) FoM of 16.9 MW·cm^{-2}, about 2x improvement. It should be pointed out that all the experimental results at this point are preliminary in nature and do not represent the full potential of the GaN nanowire device concept for this work as well as the reported GaN NW enhancement mode power transistors in [18]. The FoM for the fabricated and the simulated NWs is plotted in Fig. 11 along with other reported GaN HEMTs and vertical GaN devices from literature. The preliminary fabricated NWSBD FoM is higher than the Si limit but is lower than reported GaN HEMT performance. However, the simulated NWs show promise with performance almost at the SiC limit. Simulated FoMs with doping concentrations of 5x10^{17} cm^{-3} and 3x10^{17} cm^{-3} is shown for the fabricated structure with partial top anode coverage which yield a breakdown voltage of 97 V and 160 V respectively. The entire NW drift length is not fully depleted for these doping concentrations and so a lower doping concentration of 2x10^{17} cm^{-3} is used to deplete the entire NW and a breakdown voltage of 260 V is achieved. Devices with complete top coverage anode, edge termination and a back cathode is shown working under the doping and height constraints which yield voltages between 400 V and 700 V for the same doping but different NW diameter to oxide gap ratios. Interesting to note that with increasing breakdown voltages, the FoM improves for the GaN NWSBDs. For higher voltage applications, a longer NW is needed with the ability to dope below 2x10^{17} cm^{-3}. The NWs simulated without a height and doping constraint is also shown with a doping concentration of 4x10^{16} cm^{-3} and a pillar height of 20 µm. This device is designed with complete top anode coverage, back cathode and optimized NW diameter to oxide gap ratio to gain the best out of dielectric RESURF. With this design a breakdown voltage of nearly 4 kV with a specific on resistance of 8 mΩ·cm^{-2} can be achieved working close to the GaN performance limit.

V. Conclusion And Future Work

A new concept of vertical GaN Schottky barrier diode based on nanowire structures and the principle of dielectric RESURF is explored in this paper. The proposed NW structure offers an opportunity to reduce defect density and fabricate low cost vertical GaN power devices on Si and other foreign substrates. Quasi-vertical NWSBD samples were fabricated using the top down subtractive approach. These Schottky diodes exhibit a breakdown voltage around 100 V and no signs of current collapse. Although more work is needed to further explore the nano-GaN concept for higher voltages, the preliminary results indicate that superior tradeoff between breakdown voltage and specific on-resistance can be achieved. A pure vertical device with a back cathode and grown by the bottom up approach promises to deliver performance bordering on the GaN limit. However, several major challenges need to be addressed in order to make the nano-GaN concept a viable option for making high voltage power devices. First, fabrication techniques need to be developed for realizing GaN nanowires with a high aspect ratio (> 20). Secondly, the ability to control the silicon (n-type) doping concentration on the GaN nanowires is a key factor for achieving higher breakdown voltage and better performance FoM. Thirdly, it is important to achieve a certain level of uniformity among all NWs across the entire die area in terms of reliability. This is especially true for a large die area to support a high current rating. Furthermore, a full characterization and analysis on the reduction of threading dislocations in the NWs for different fabrication processes needs to be completed to produce electrically and structurally homogenous batches of NWs in the future.

References

[1] K. Nagata, K. Tamura, M. Suemitsu, Y. Narita, T. Ito, T. Endoh, H. Nakazawa, A. M. Hashim, and K. Yasui, "Growth of GaN on SiC/Si substrates using AlN buffer layer under low III/V source gas ratio by hot-mesh CVD," *2010 Int. Conf. Enabling Sci. Nanotechnology, ESciNano 2010 - Proc.*, pp. 0–1, 2010.

[2] C. Gupta, Y. Enatsu, G. Gupta, S. Keller, and U. K. Mishra, "High

breakdown voltage p-n diodes on GaN on sapphire by MOCVD," *Phys. Status Solidi Appl. Mater. Sci.*, vol. 882, no. 4, pp. 878–882, 2016.
[3] U. K. Mishra, P. Parikh, and Y. F. Wu, "AlGaN/GaN HEMTs - An overview of device operation and applications," *Proc. IEEE*, vol. 90, no. 6, pp. 1022–1031, 2002.
[4] C. Tang, G. Xie, and K. Sheng, "Enhancement-mode GaN-on-Silicon MOS-HEMT using pure wet etch technique," *Proc. Int. Symp. Power Semicond. Devices ICs*, vol. 2015–June, pp. 233–236, 2015.
[5] W. Saito, I. Omura, T. Domon, and K. Tsuda, "High voltage and high switching frequency power-supplies using a GaN-HEMT," *Tech. Dig. - IEEE Compd. Semicond. Integr. Circuit Symp. CSIC*, pp. 253–256, 2006.
[6] I. C. Kizilyalli, A. P. Edwards, H. Nie, P. Bui-Quang, D. Disney, and D. Bour, "400-A (pulsed) vertical GaN p-n diode with breakdown voltage of 700 V," *IEEE Electron Device Lett.*, vol. 35, no. 6, pp. 654–656, 2014.
[7] I. C. Kizilyalli, A. P. Edwards, H. Nie, S. Member, D. Disney, and D. Bour, "High Voltage Vertical GaN p-n Diodes With Avalanche Capability," vol. 60, no. 10, pp. 3067–3070, 2013.
[8] G. T. Wang and Q. Li, "Nanowires: lighting the future," *SPIE Newsroom*, pp. 2–4, Jul. 2011.
[9] I. H. Wildeson, R. Colby, D. A. Ewoldt, Z. Liang, D. N. Zakharov, N. J. Zaluzec, R. E. García, E. A. Stach, T. D. Sands, R. E. García, E. A. Stach, and T. D. Sands, "III-nitride nanopyramid light emitting diodes grown by organometallic vapor phase epitaxy," *J. Appl. Phys.*, vol. 108, no. 4, p. 44303, 2010.
[10] G. T. Wang, a A. Talin, D. J. Werder, J. R. Creighton, E. Lai, R. J. Anderson, and I. Arslan, "Highly aligned, template-free growth and characterization of vertical GaN nanowires on sapphire by metal–organic chemical vapour deposition," *Nanotechnology*, vol. 17, no. 23, pp. 5773–5780, 2006.
[11] C. H. Chiu, H. H. Yen, C. L. Chao, Z. Y. Li, P. Yu, H. C. Kuo, T. C. Lu, S. C. Wang, K. M. Lau, and S. J. Cheng, "Nanoscale epitaxial lateral overgrowth of GaN-based light-emitting diodes on a SiO2 nanorod-array patterned sapphire template," *Appl. Phys. Lett.*, vol. 93, no. 8, pp. 111–114, 2008.
[12] Y. B. Tang, Z. H. Chen, H. S. Song, C. S. Lee, H. T. Cong, H. M. Cheng, W. J. Zhang, I. Bello, and S. T. Lee, "Vertically aligned p-type single-crystalline GaN nanorod arrays on n-type Si for heterojunction photovoltaic cells.," *Nano Lett.*, vol. 8, no. 12, pp. 4191–5, Dec. 2008.
[13] L. Geelhaar, C. Ch, B. Jenichen, O. Brandt, C. Pf, M. Steffen, R. Rothemund, S. Reitzenstein, A. Forchel, T. Kehagias, P. Komninou, G. P. Dimitrakopulos, T. Karakostas, L. Lari, P. R. Chalker, M. H. Gass, and H. Riechert, "Properties of GaN Nanowires Grown by Molecular Beam Epitaxy," vol. 17, no. 4, pp. 878–888, 2011.
[14] Y. Inoue, T. Hoshino, S. Takeda, K. Ishino, A. Ishida, H. Fujiyasu, H. Kominami, H. Mimura, Y. Nakanishi, and S. Sakakibara, "Strong luminescence from dislocation-free GaN nanopillars," *Appl. Phys. Lett.*, vol. 85, no. 12, pp. 2340–2342, 2004.
[15] S. D. Hersee, X. Sun, and X. Wang, "The Controlled Growth of GaN Nanowires," vol. 221, 2006.
[16] S. D. Hersee, A. K. Rishinaramangalam, M. N. Fairchild, L. Zhang, and P. Varangis, "Threading defect elimination in GaN nanowires," *J. Mater. Res.*, vol. 26, no. 17, pp. 2293–2298, 2011.
[17] T. Bryllert, L.-E. Wernersson, T. Löwgren, and L. Samuelson, "Vertical wrap-gated nanowire transistors," *Nanotechnology*, vol. 17, no. 11, pp. S227–S230, 2006.
[18] F. Yu, D. Rümmler, J. Hartmann, L. Caccamo, T. Schimpke, M. Strassburg, A. E. Gad, A. Bakin, H. H. Wehmann, B. Witzigmann, H. S. Wasisto, and A. Waag, "Vertical architecture for enhancement mode power transistors based on GaN nanowires," *Appl. Phys. Lett.*, vol. 108, no. 21, pp. 1–6, 2016.
[19] J. Šonský, a Heringa, and J. Sonsky, "Dielectric Resurf: Breakdown voltage control by STI layout in standard CMOS," *IEDM Tech. Dig.*, vol. 2005, no. d, pp. 373–376, 2005.
[20] X. J. Chen, B. Gayral, D. Sam-Giao, C. Bougerol, C. Durand, and J. Eymery, "Catalyst-free growth of high-optical quality GaN nanowires by metal-organic vapor phase epitaxy," *Appl. Phys. Lett.*, vol. 99, no. 25, p. 251910, 2011.
[21] M. Conroy, V. Z. Zubialevich, H. Li, N. Petkov, S. O'Donoghue, J. D. Holmes, and P. J. Parbrook, "Ultra-High-Density Arrays of Defect-Free AlN Nanorods: A 'space-Filling' Approach," *ACS Nano*, vol. 10, no. 2, pp. 1988–1994, 2016.
[22] M. Conroy, H. Li, V. Z. Zubialevich, G. Kusch, M. Schmidt, T. Collins, C. Glynn, R. W. Martin, C. O'Dwyer, M. D. Morris, J. D. Holmes, and P. J. Parbrook, "Self-Healing Thermal Annealing: Surface Morphological Restructuring Control of GaN Nanorods," *Cryst. Growth Des.*, vol. 16, no. 12, pp. 6769–6775, 2016.
[23] S. Li and A. Waag, "GaN based nanorods for solid state lighting," *J. Appl. Phys.*, vol. 111, no. 7, p. 71101, 2012.
[24] M. F. Chisholm and S. J. Pennycook, "Direct imaging of dislocation core structures by Z-contrast STEM," *Philos. Mag.*, vol. 86, no. 29–31, pp. 4699–4725, Oct. 2006.
[25] *Sentaurus Device User*, no. DECEMBER. 2013.
[26] G. Sabui, P. J. Parbrook, M. Arredondo-Arechavala, and Z. J. Shen, "Modeling and simulation of bulk gallium nitride power semiconductor devices," *AIP Adv.*, vol. 6, no. 5, 2016.
[27] I. C. Kizilyalli, A. P. Edwards, H. Nie, D. Bour, T. Prunty, and D. Disney, "3.7 kV vertical GaN PN diodes," *IEEE Electron Device Lett.*, vol. 35, no. 2, pp. 247–249, 2014.
[28] D. Disney, H. Nie, A. Edwards, D. Bour, H. Shah, and I. C. Kizilyalli, "Vertical power diodes in bulk GaN," in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, 2013, pp. 59–62.
[29] X. Chen, L. S. Member, and M. Huang, "A Vertical Power MOSFET With an Interdigitated Drift Region Using High- k Insulator," *IEEE Trans. Electron Devices*, vol. 59, no. 9, pp. 2430–2437, 2012.
[30] M. Huang and X. Chen, "Study on layouts design of the voltage sustaining layer using high-k insulator," in *Proceedings - 2014 IEEE 12th International Conference on Solid-State and Integrated Circuit Technology, ICSICT 2014*, 2014, no. 1, pp. 6–8.
[31] J. C. Carrano, T. Li, P. a. Grudowski, C. J. Eiting, R. D. Dupuis, and J. C. Campbell, "Current transport mechanisms in GaN-based metal–semiconductor–metal photodetectors," *Appl. Phys. Lett.*, vol. 72, no. 5, p. 542, 1998.
[32] J. Hu, S. Stoffels, S. Lenci, B. Bakeroot, B. De Jaeger, M. Van Hove, N. Ronchi, R. Venegas, H. Liang, M. Zhao, G. Groeseneken, and S. Decoutere, "Performance Optimization of Au-Free Lateral AlGaN/GaN Schottky Barrier Diode With Gated Edge Termination on 200-mm Silicon Substrate," *IEEE Trans. Electron Devices*, vol. 63, no. 3, pp. 997–1004, 2016.
[33] E. Bahat-Treidel, O. Hilt, R. Zhytnytska, A. Wentzel, C. Meliani, J. Wurfl, and G. Trankle, "Fast-switching GaN-based lateral power schottky barrier diodes with low onset voltage and strong reverse blocking," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 357–359, 2012.
[34] M. Zhu, B. Song, M. Qi, Z. Hu, K. Nomoto, X. Yan, Y. Cao, W. Johnson, E. Kohn, D. Jena, and H. G. Xing, "1.9-kV AlGaN/GaN Lateral Schottky Barrier Diodes on Silicon," *IEEE Electron Device Letters*, vol. 36, no. 4. pp. 375–377, 2015.
[35] http://www.transphormusa.com/gan-technology/
[36] http://www.digikey.com/en/articles/techzone/2014/feb/dealing-with-enhancement-mode-gan-technology