CORA Cork Open Research Archive
Cartlann Taighde Oscailte Chorcaí

Title	A study of silicon and germanium junctionless transistors
Authors	Yu, Ran
Publication date	2013
Original Citation	Yu, R. 2013. A study of silicon and germanium junctionless transistors. PhD Thesis, University College Cork.
Type of publication	Doctoral thesis
Rights	© 2013, Ran Yu. - http://creativecommons.org/licenses/by-nc-nd/3.0/
Download date	2026-11-03 09:16:37
Item downloaded from	https://hdl.handle.net/10468/1283



UCC
University College Cork, Ireland
Coláiste na hOllscoile Corcaigh

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
NATIONAL UNIVERSITY OF IRELAND, CORK

A STUDY OF SILICON AND GERMANIUM JUNCTIONLESS TRANSISTORS

A thesis submitted in accordance with the requirements for the degree of

Doctor of Philosophy

Ran Yu

April 2013

Supervisors: Prof. Jean-Pierre Colinge
Dr. Ray Duffy
Department Head: Prof. Nabeel A. Riza

Silicon Research Group
Tyndall National Institute
Lee Maltings, Prospect Row, Cork, Ireland

Declaration

The thesis submitted is the candidate's own work and has not been submitted for another degree, either at University College of Cork or elsewhere.

Ran Yu

Acknowledgements

This dissertation would not have been possible without the help and contributions of many individuals, to whom my deep thanks and sincere gratitude should be given.

First of all, I want to express my sincere and deepest gratitude toward my supervisors, Professor Jean-Pierre Colinge, Professor Cindy Colinge and Dr. Ray Duffy, for giving me the opportunity to carry out the PhD, and their priceless support and guidance throughout the course of my PhD. The fun, stress-free and friend-kind relationship while continuing to encourage my academic progress makes it a real pleasure to work for them.

I would also like to give my special thanks to Dr. Yordan M. Georgiev, Dr. Nikolay Petkov, Richard Hobbs and Prof. Justin D. Holmes from Chemistry department of UCC and Dr. Samaresh Das from Ultimate Silicon Device group in Tyndall. We have spent so much time to discuss and work together. Without their support, I would not be possible to go through the difficult time and fabricated my device finally.

I am thankful to many former and current colleagues in Tyndall, Maryam Shayesteh, Dr. Ian Provey, Dr. Paul Hurley, Dr. Adi Negara, Olan Lotty, Colm O'Regan, Dan O'Connell, Vladimir Djara, Brendan McCarthy, Mary White, Dr. Anne-Marie Kellerher, Brendan O'Neil, Dr. Kiyeol Byun, Dr. Chi-Woo Lee, Dr. Ran Yan, Dr. Isabelle Ferain, Dr. Pedram Razavi, Dr. Nima Dehdashti Akhavan, Dr. Abhinav Kranti, Jean-Baptiste Milon, Dr. Aryan Afzalian.

I am very grateful to Professor Jean-Pierre Raskin and Dr. Karim Cherkaoui for serving on my dissertation committee, and especially for their great cooperation in reviewing to this dissertation timely.

Lastly, very special thanks to my parents, Wang Xiaoxing and Yu Jieyi, and to Jing for their wisdom, unflinching faith and strength.

Abstract

As the semiconductor industry approaches the limits of the traditional silicon CMOS scaling, the implementation windows of certain performance boosters, such as high mobility channel materials and novel structures, have been opened in the near future. In this dissertation, the properties and feasibility of the proposed Junctionless transistor (JNT) have been evaluated for both Silicon and Germanium channels.

In chapter 1, the conventional scaling of Silicon CMOS has been reviewed and the benefits of Moore's law, in terms of speed and power, have been discussed. The challenges of scaling beyond 22 nm technology nodes have been categorized into five groups, which are gate control, current output, capacitance, power/performance ratio, and variation/reliability. Solutions for beyond 22 nm devices, named as technology boosters, have been discussed and extended into the proposed Junctionless structure with novel Ge channel material.

In chapter 2, the simulations are carried out using the Synopsys Technology Computer-Aided Design (TCAD) software, in order to compare the Junctionless transistors (JNT) with the Inversion Mode (IM) devices, in terms of gate control, vertical electric field and capacitances. The unique conduction mechanism and electrical characteristics for JNT have been discussed. In order to scale the V_{DD}, lower *SS* value (sub-60 mV/dec at room temperature) in JNT has been obtained by simulation. The dependence of the effect on gate length is investigated and their influence on the I_D-V_G curves is discussed. For future current enhancement, simulation of JNTs with high mobility Ge channel was performed.

In chapter 3, the fabrication process of Si IM devices and JNTs down to 22 nm gate length has been discussed and characterizations have been carried out for these devices at elevated temperature and stressed conditions. Steep subthreshold slopes (*SS*) in JNT and IM devices are observed, and the influence of geometry, recombination mechanism and electric field on this effect for IM and JNTs are discussed according to the measurement and simulation results. It is observed that the floating body in JNT is relatively dynamic comparing with that in IM devices and proper design of the device structure may further reduce the V_D for a sub-60 mV/dec subthreshold slope. The diode

configuration of the JNT has also been evaluated, which demonstrates the first diode without junctions.

The high quality gate dielectric for surface passivation is one of the major challenges in realizing Ge CMOS. In chapter 4, thermally grown GeO_2 was used as interfacial passivation layer for high-*k*/Ge gate stack. The oxidation behaviour of Ge by Rapid Thermal Oxidation (RTO) has been investigated for various oxidation conditions in terms of temperatures, times, and gas flow. We have also examined effects of Forming Gas Annealing (FGA) on the physical and electrical properties of the interfacial GeO_2 passivation layer for high-*k*/Ge gate stack formed by RTO. The results show that oxidation temperatures higher than 600 °C lead to GeO_2 surface roughness of 14.5 nm, which can be related to serious GeO desorption. In contrast, the interfacial GeO_2 layers formed at higher temperatures exhibit systematically decreased D_{it} values in both upper and lower-half of the bandgap. Moreover, post-metallisation FGA of the MOS devices shows the potential to reduce the D_{it} values and hysteresis further, which indicates FGA can result in significant reduction of the interface states and compensate the charges inside the oxide.

In chapter 5, Germanium-on-Insulator (GeOI) wafers were fabricated using Smart-Cut with low temperature direct wafer bonding method. A Preferential etch solvent was developed and used to decorate the defects on Ge during the GeOI fabrication. For the lithography and pattern transfer, a top-down process of sub-50-nm width Ge nanowires is developed in this chapter and Ge nanowires with 35 nm width and 50 nm depth are obtained using this process. With the developed modules, JNT with p-type Ge channels have been fabricated by the CMOS-compatible top-down process. The transistors exhibit the lowest subthreshold slope to date for Ge junctionless devices. The devices with a gate length of 3 μm exhibit a *SS* of 216 mV/dec with an I_{ON}/I_{OFF} current ratio of 1.2×10^3 at V_D = -1 V and *DIBL* of 87 mV/V.

TABLE OF CONTENTS

Declaration ..... **I**

Acknowledgements ..... **II**

Abstract ..... **III**

Chapter 1 Introduction **1**

Abstract 1

1.1 The Scaling of CMOS Technology: Benefits of Moore's Law 1

1.1.1 The Transistor Gate Delay: Switching Speed 2

1.1.2 Power Dissipation: Active and Passive Power 3

1.1.3 From "Classic" Scaling to Selective Scaling: Cadence of Power Reduction and Speed Boosting 4

1.2 Scaling Challenges beyond 22 nm Technology Nodes 6

1.2.1 Gate Control for a Transistor 8

1.2.2 Current Output 8

1.2.3 Capacitance 9

1.2.4 Power/performance Ratio 10

1.2.5 Variation and Reliability 10

1.3 Advanced CMOS Technology for Sub-22 nm nodes 11

1.3.1 Progress of "non-classic" Scaling in the Industry 13

1.3.2 Silicon-on-Insulator (SOI): From Partially Depleted SOI to Multigate SOI and Fully Depleted Extremely-Thin-Body SOI (ETSOI) 15

1.3.3 FinFET on Bulk Silicon and on SOI 18

1.3.4 Junctionless Nanowire Transistor (JNT): Transistor without Junctions 19

1.3.5 Access Window for IIIV and Ge Logic Devices in Roadmap 20

1.4 Objectives and Organization of the Thesis 22

1.5 Reference 23

Chapter 2 TCAD Application on Semiconductor Devices and Process: Simulation of Silicon and Germanium JNT **29**

Abstract 29

2.1 TCAD Introduction 29

2.1.1 Process Simulation 30
2.1.2 Device Simulation 30
2.2 Device Physics of JNT 31
2.3 Simulation of Si JNT and its Comparison to Conventional Inversion Mode (IM) Transistors 33
2.3.1 Merits of JNT: Superior Gate Control without Abrupt Junctions 33
2.3.2 Merits of JNT: Relaxed Vertical Electric Field 35
2.3.3 Merits of JNT: Reduced Capacitance 36
2.3.4 Potential Drawbacks of JNTs: V_{th} Variability and Mobility Degradation 39
2.4 Simulation of Impact Ionization Effect in Short Channel JNT 40
2.4.1 Device Structure and Simulation 41
2.4.2 Results and Discussions 41
2.5 Device Design and Estimated Performance for P-type Junctionless Transistors on Bulk Germanium Substrates 46
2.5.1 Device Operation and Simulation Set-up 47
2.5.2 Results and Discussions 49
2.5.3 Summary and Conclusion 56
2.6 Conclusions 57
2.7 Reference 58

Chapter 3 Fabrication and Characterization of Silicon JNT 61

Abstract 61
3.1 Devices Fabricated and Used in the Work 61
3.1.1 Long Channel Si JNT 61
3.1.2 Short Channel Si JNT down to 22 nm 64
3.2 Devices Characterization 65
3.2.1 Characterization of Long Channel Si JNTs 65
3.2.2 Characterization of Short Channel JNTs down to 22 nm 67
3.3 Impact Ionization Induced Dynamic Floating Body Effect in JNTs 69
3.3.1 Introduction 70
3.3.2 Device Fabrication and Simulation set-up 70
3.3.3 Results and Discussion 71
3.3.4 Summary and Conclusion 75
3.4 Performance of 22 nm Tri-Gate JNTs at Elevated Temperatures 75

3.5 Characterization of a Junctionless Diode 81
3.5.1 Introduction 81
3.5.2 Results and Discussion 83
3.5.3 Summary 87
3.6 Conclusions 88
3.7 Reference 89

Chapter 4 High-*k* on Germanium and its Passivation Method 93

Abstract 93
4.1 Introduction 93
4.2 High-*k*/Ge Gate Stack with an Interfacial GeO_2 Passivation Layer formed by Rapid Thermal Oxidation 94
4.3 Experimental Details 95
4.4 Results and Discussion 96
4.4.1 Surface Morphology of Thermally Growth GeO_2 96
4.4.2 Oxidation Rate of Ge Substrate 98
4.4.3 Capacitance-Voltage Response of the MOS Structure with $Al_2O_3/GeO_2/Ge$ Gate Stacks at Room Temperature 101
4.4.4 D_{it} Extraction of the Gate Stacks 103
4.4.5 Hysteresis of the Gate Stack 107
4.5 Conclusions 108
4.6 Reference 109

Chapter 5 Germanium JNT: From Substrate to Device 112

Abstract 112
5.1 Fabrication of Germanium-on-Insulator by Low Temperature Direct Wafer Bonding 112
5.1.1 Introduction 112
5.1.2 Fabrication GeOI Wafer by Smart-Cut Technology 113
5.1.3 Experimental 114
5.1.4 Results and Discussion 114
5.1.5 Summary 118
5.2 Surface Defects on Germanium Wafer and the Decoration Method 119
5.2.1 Introduction 119

5.2.2 Wright Etch on Bulk Germanium Wafer 120
5.2.3 Defects Decoration during the GeOI Fabrication 121
5.2.4 Defects Decoration for as-implanted Ge Wafer.....121
5.2.5 Defects Decoration and Thinning of Transferred Ge Thin Film on GeOI123
5.2.6 Defects Decoration of the un-transferred Ge Donor Wafer.....125
5.2.7 Summary 126
5.3 Top-down Process of Ge Nanowires using EBL Exposure of Hydrogen Silsesquioxane (HSQ) Positive Resist 127
5.3.1 Introduction.....127
5.3.2 Top-down Process of Ge Nanowires.....128
5.3.3 Results and Discussions 129
5.3.4 Conclusions.....133
5.4 Ge Nanowire JNT 134
5.4.1 Device Fabrication Process 134
5.4.2 Device Characterization 136
5.4.3 Summary 139
5.5 Conclusions.....139
5.6 Reference.....140

Chapter 6 Conclusions and Future Perspectives 143

List of Publications..... 146

Chapter 1 Introduction

Abstract: In this chapter, the conventional scaling of Silicon CMOS has been reviewed and the benefits of Moore's law, in terms of speed and power, have been discussed. The challenges of scaling beyond 22 nm technology nodes have been categorized into five groups, which are gate control, current output, capacitance, power/performance ratio, and variation/reliability. Solutions for beyond 22 nm devices, named as technology boosters, have been discussed and extended into proposed Junctionless structure with novel Ge channel material.

1.1 The Scaling of CMOS Technology: Benefits of Moore's Law

The computing and communication technologies, supported by strong progress in nanoelectronics, have been proven as pervasive driving forces in the world economy over the past two decades. More than 10% of the world economy is built on electronic products and related services and this percentage is continuously growing.

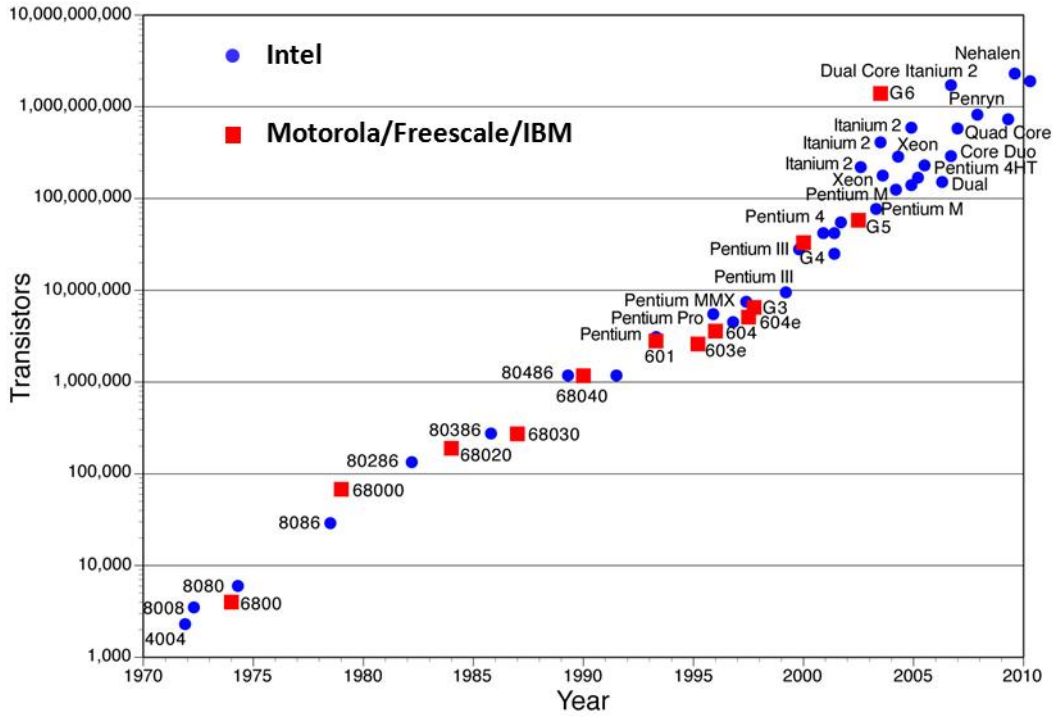


Figure 1.1: Illustration of Moore's law: transistor counts (number) against dates of introduction. The curve shows counts doubling every two years.

This revolutionary semiconductor industry started from the invention of the first solid-state device, a bipolar point-contact transistor on Germanium (Ge) substrate, invented by Bardeen, Brattain, and Shockley at Bell labs in 1947 [1-4]. Since its birth, it has experienced five decades of unprecedented explosive growth driven by several major enabling factors: Noyce and Kilby inventing the planar integrated circuit in 1958, the invention of the first metal-oxide-semiconductor field-effect transistor (MOSFET) was built by Kahng and Atalla in 1960, the invention of CMOS process by Wanlass, and the advantageous characteristics that result from scaling (shrinking) solid-state devices [5].

In 1965 Gordon Moore published a paper predicting that the number of transistor per chip would double every 18 months with improved characteristics [6]. After four decades, when we look back on the footprint of the CPU transistor counts as shown in the Figure 1.1, the number of transistors doubles approximately every two years, which actually follows Moore's law as a self-fulfilling prophecy.

The conventional scaling of the MOSFET not only increased functionality per unit chip-area, reduced cost per functionality, but also improved the fundamental device parameters for logic applications, namely: 1) intrinsic speed; 2) switching energy.

1.1.1 The Transistor Gate Delay: Switching Speed

As an important performance of the CMOS, the inverter delay, defined as the time required to propagate a transition through a single inverter driving a second, identical inverter, is commonly used as a method of marking the speed of CMOS transistors (the speed of switching being inversely proportional to the circuit delay). It has been found empirically that a delay, τ, calculated from

$$\tau = C_{GATE} \times V_{DD} / I_{DSAT} \quad (1)$$

correlates quite well with actual inverter delays. For 100 nm gate length n-type MOSFETs, τ typically ranges from 1.5 ps to 3 ps, and about twice as much for p-type, with corresponding inverter delays ranging from 10 ps to 20 ps [7].

1.1.2 Power Dissipation: Active and Passive Power

The power dissipation of an integrated circuit (IC) can be categorized into two types - active and passive. This can be accomplished empirically that the power of an IC, for a fixed operating voltage and temperature, increases linearly with the clock frequency f (the frequency of a master signal with which all operations must be synchronized). This component of power which is proportional to the frequency is referred to as the active power, P_{ACTIVE}. The active power is due primarily to the charging and discharging of capacitances on the IC, and can be represented by an effective switching capacitance, C_{EFF}. Extrapolation of the power vs. frequency response to a frequency of zero, which may be realized in a "sleep" mode, yields a nonzero power. This is referred to as the passive power, $P_{PASSIVE}$. The total power dissipation of an IC can be expressed by:

$$P_{TOTAL} = P_{ACTIVE} + P_{PASSIVE} = C_{EFF} \times V_{DD}^{2} f + I_{Leakage} \times V_{DD} \quad (2)$$

C_{EFF} is the effective device switching capacitance, which does not necessarily represent the actual total capacitance being switched by the chip, since many of the circuits may be switching at some fraction of f (or, for that matter, at some multiple of f).

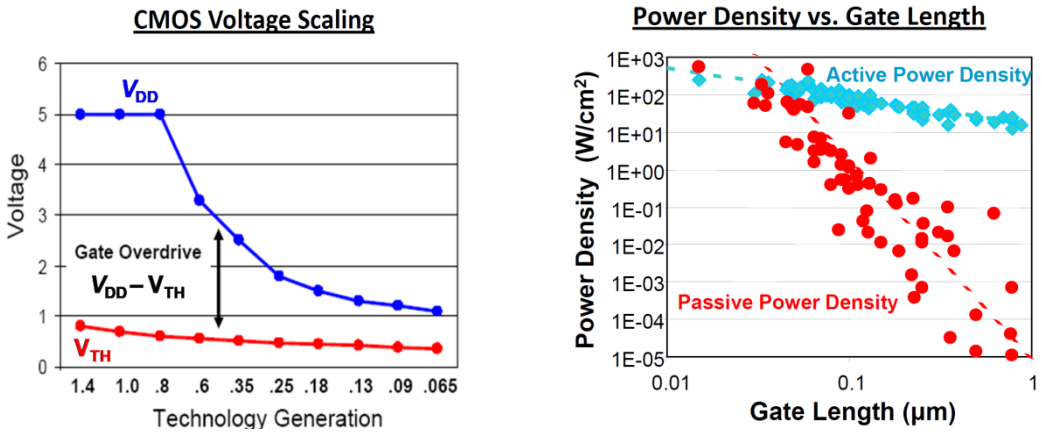


Figure 1.2: (a) Scaling trend of the supply (V_{DD}) and threshold voltage (V_{th}) with CMOS technology generation (adapted from [8]). (b) Scaling trend of the power density with gate length (L_{GATE}); leakage power density has exponentially increased with L_{GATE} scaling (adapted from [9]).

The passive power consumption is related to the leakage current, mainly consists of subthreshold leakage and junction leakage currents. Unfortunately, as the V_{DD} and V_{th} continuously are scaled down as shown in Figure 1.2(a), subthreshold leakage increases

simultaneously, and is not susceptible to be eliminated by means of new materials or process. Moreover, as the transistor goes into sub 100 nm nodes, the traditional planar MOSFET encounters short channel effects, which indicates a worse the gate control of the device. The degraded subthreshold slopes lead to increased subthreshold leakage currents, hence, increased passive power density starts to exceed the active power at short technology nodes as shown in Figure 1.2.

1.1.3 From "Classic" Scaling to Selective Scaling: Cadence of Power Reduction and Speed Boosting

For many years now, the shrinking of MOSFETs has been governed by the ideas of scaling [10, 11]. The basic idea is explained as: a large FET is scaled down by a factor to produce a smaller FET with similar behaviour. When all of the voltages and dimensions are reduced by the scaling factor and the doping and charge densities are increased by the same factor, the electric field configuration inside the FET remains the same as it was in the original device. This is called constant field scaling, which results in circuit speed increasing in proportion to the factor α and circuit density increasing as α^2. These scaling relations are shown in the second column of Table 1.1 along with the scaling behaviour of some of the other important physical parameters.

Physical Parameters	Constant-field scaling factor	Generalized scaling factor	Generalized selective scaling factor
Channel length, insulator thickness (L_{GATE}, T_{OX})	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Writing width, channel width (W_{GATE})	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Electric field in device	1	ε	ε
Voltage (V_{DS}, V_{GS})	$1/\alpha$	ε/α	ε/α_d
On-current per device (I_D)	$1/\alpha$	ε/α	ε/α_w
Doping, (N, X_J)	α	$\varepsilon\,\alpha$	$\varepsilon\,\alpha_d$
Area	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha_w^2$
Capacitance (C_{GATE})	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Gate delay (τ)	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Power dissipation	$1/\alpha^2$	ε^2/α^2	$\varepsilon^2/\alpha_w\alpha_d$
Power density	1	ε^2	$\varepsilon^2\alpha_w/\alpha_d$

Table 1.1: α is the dimensional scaling parameter; ε is the electric field scaling parameter; α_d and α_w are separate dimensional scaling parameters for the selective scaling case. α_d is applied to the device vertical dimensions and gate length, while α_w applies to the device width and the wiring width. [12]

For (deep) submicron devices, the voltage scaling slows down around 1 V (Figure 1.2(a)) and, thus, the electric field increases as the gate length decreases. As a result, the transistor characteristics are described in the third column of Table 1.1, which are related to the electric field scaling parameter, ε. Further deviation of "Classic" scaling parameters applies to the device vertical dimensions and gate length, named as α_d, and the device width and the wiring width, named as α_w. In this case, the device characteristics are summarized in the fourth column of Table 1.1.

Figure 1.3 illustrates the expected "classic" scaling consequences (dashed curves), along with data points calculated from the industry scaling trends for total gate capacitance (C_{GATE}), inverter delay, saturation current (I_{DSAT}), switching power density and calculated delay τ. While in "classic constant-field scaling" both I_{DSAT}, C_{GATE} and power density remain constant (normalized per MOSFET unit width) as shown in Table 1.1 second column.

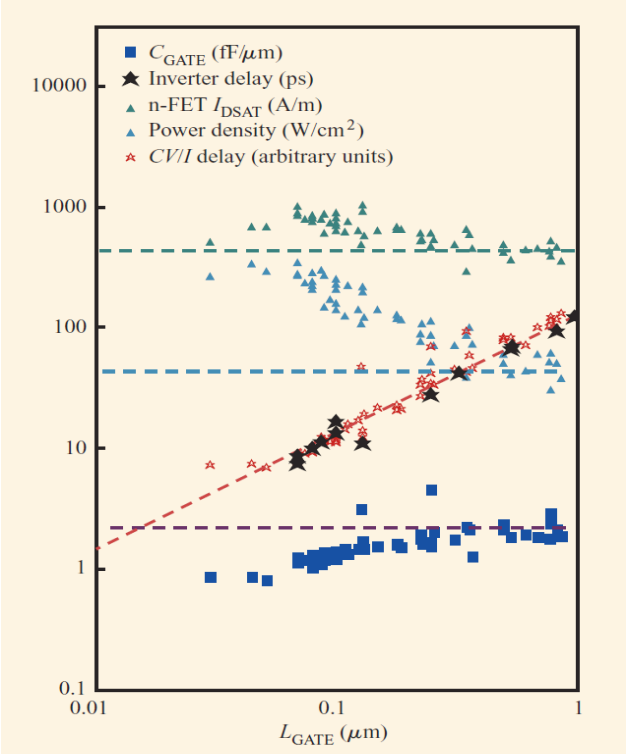


Figure 1.3: Published industry trends (points) are compared with "classic" scaling (dashed curves). I_{DSAT}, C_{GATE} and power density show clear signs of deviation from classic scaling with respect to L_{GATE}; delay τ scales nearly the same as the classic case (as L_{GATE}); [7]

From the industry-trend data shown in Figure 1.3, spanning an L_{GATE} reduction from 1 μm to 100 nm, indicate that I_{DSAT} has nearly doubled. The increase in I_{DSAT} is driven largely by subscaling of V_{DD} when it is close to 1 V. Similarly, C_{GATE} has decreased significantly in this period, since L_{GATE} drops more rapidly than T_{OX}. As a result, the inverter delay continues to decrease in proportion to (or perhaps slightly faster than) L_{GATE}, as in "Classic" scaling. The switching-power density should remain constant in "Classic" scaling. Unfortunately, in contrast to this, P, as calculated from the industry-trend data, has increased by nearly a decade. In this instance, the deviation of the V_{DD} trend from classic scaling has outweighed that of C_{GATE} (from T_{OX} subscaling), to yield this undesirable result. Thus, if die size is kept constant, to add more function with scaling the overall switching power must increase unless some other actions are taken [13].

1.2 Scaling Challenges beyond 22 nm Technology Nodes

As discussed in section 1.1.1 and 1.1.2, the fundamental transistor performance can be evaluated by the intrinsic speed and switching energy, which are expressed in the following equations in previous sections.

$$\tau = C_{GATE} \times V_{DD} / I_{DSAT} \tag{1}$$

$$P_{TOTAL} = P_{ACTIVE} + P_{PASSIVE} = C_{EFF} \times V_{DD}^{2} f + I_{LEAKAGE} \times V_{DD} \tag{2}$$

When we take a close look at the two formulas, three critical variables can be extracted. They are I_{DSAT}, $I_{LEAKAGE}$ and V_{DD}. Ideally, the I_{DSAT} should be as large as possible, while keeping the $I_{LEAKAGE}$ and V_{DD} as small as possible. However, it is not realistic as several conflicts exist inside the ideal case.

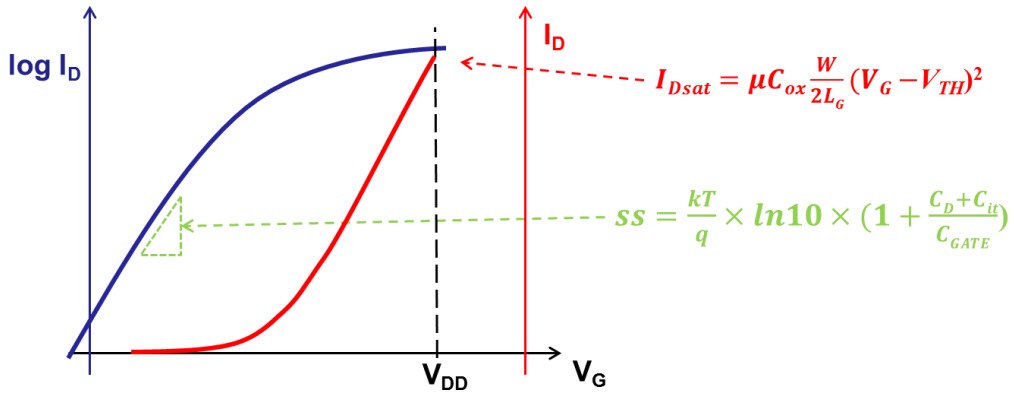


Figure 1.5: I_D-V_G characteristics in log (blue) and linear (red) scale for a MOSFET transistor. The equation of output current is expressed in red. The sub-threshold slope, *SS* is defined as the inverse of the slope of the log of the drain current versus gate voltage, has a theoretical equation (4), which is illustrated in green. C_D is the depletion capacitance, C_{GATE} is the gate capacitance and C_{it} is the capacitance from D_{it}.

$$I_{DSAT} = \mu C_{OX} \times (W/2L_{GATE}) \times (V_{GATE} - V_{th})^2 \quad (3)$$

$$SS = (kT/q) \times ln10 \times (1 + (C_D + C_{it})/C_{GATE}) \quad (4)$$

First, as shown in Figure 1.5, if a small V_{DD} is chosen, according to the current output expression in equation 3, the I_{DSAT} will be limited as well. Therefore the V_{DD} cannot be scaled aggressively while the speed of the transistor has to be considered. However, by making the gate length shorter and the mobility larger, the I_{DSAT} can be enhanced as well. This is one of the original driven forces for the transistor scaling and channel strain when pursuing more current output.

Second, as shown in the log scale I_D-V_G characteristic in Figure 1.5, when the *SS* value approaches to its theoretical limit of (kT/q)×ln10, which indicates the transistor has a perfect gate control that the C_D, C_{it} have been minimized and the C_{GATE} has been maximized. The shape of the I_D-V_G curve has been fixed for certain gate control, and the I_D-V_G curve can be shifted to left or right by tuning the gate work-function. However, it turns out as when a low $I_{LEAKAGE}$ is required, the I_{DSAT} has been lowered as well according to the shape fixed I_D-V_G curve mentioned above. Thus, the better gate control, in terms of *SS* and *DIBL* values, is always a focus of the semiconductor industry, especially as device scaled down into tens of nanometer. As the gate control of the technology node has been determined, a compromise has to be made for the performance and energy trade-off.

In a summary, in order to discuss the challenges of the ultra-short channel transistors, we categorized them into several groups: 1) gate control; 2) current output; 3) capacitances; 4) performance/energy ratio; 5) variation and reliability;

1.2.1 Gate Control for a Transistor

The gate control challenges consist of "short-channel effects" (*SCE*, which includes *SS* degradation, *DIBL*, *GIDL*), source to drain direct tunnelling and gate oxide tunnelling, etc., which lead to an unacceptable leakage and subthreshold characteristics. In devices with a very short channel length the drain potential can significantly influence the channel potential, creating these short-channel effects that worsen the off-state leakage current (I_{OFF}), the threshold voltage (V_{th}) roll-off and the drain-induced barrier lowering (*DIBL*). The increase of I_{OFF} may limit CMOS scaling because it raises static power consumption. Besides I_{OFF} increase owing to *SCE*, I_{OFF} grows with scaling also due to Band to Band Tunneling (*BBT*) at drain junction, with high channel pocket doping levels used to control *SCE*. On the other hand, to minimize *SCE* in bulk MOSFETs, the gate oxide thickness (T_{ox}) is decreased with gate length. A physical limitation is reached when scaling the SiO_2 gate oxide thickness below 2 nm due to the gate leakage current by quantum mechanical tunnelling. The use of higher permittivity gate dielectric material allows one to further reduce the equivalent oxide thickness (T_{ox}) while using a physically thicker dielectric in through which there is less electron tunnelling. Also, as the gate length shrunk down to decananometer regime (*i.e.* $L_{GATE}<$ 10 nm), large value of I_{OFF} due to source to drain tunnelling current limits the subthreshold slope and I_{OFF}, hence posing a serious challenge in further scaling of transistors.

1.2.2 Current Output

Ideally, the I_{DSAT} supposed to be as large as possible, since the connected devices can be charged quicker, resulting in a faster circuit. However, to minimize *SCE* in bulk MOSFETs, the channel depletion width (X_d), and the source/drain junction depth (X_j) have to be decreased with gate length as well. The channel doping concentration should be increased to reduce the depletion width. However, the use of high channel doping concentrations decreases carrier mobility. In order to boost device performance for

every technology generation, the current delivered through the channel has to be increased. Mobility enhancement through strained Si, different channel orientations or even alternate channel materials, such as IIIV and Ge, are all for the purpose of current improvement, which will be discussed in the later sections.

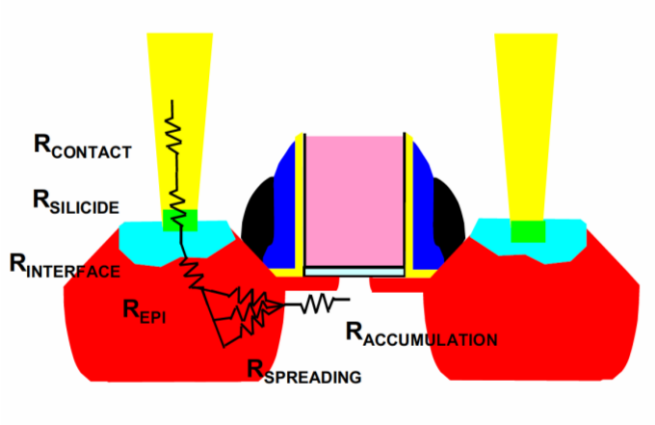


Figure 1.6: Resistive elements in planar architectures [14]

Moreover, traditional resistive elements previously neglected (interface and epi resistance) as well as new elements associated with the advanced transistor architectures will become critical (Figure 1.6) for the current output. New doping techniques (molecular doping, plasma doping), new annealing techniques (submelt, laser, flash anneal, etc.) new architectures (metal S/D, etc.) have been under development. Thus, the reduction of resistance (contact, silicide, epi and accumulation resistance) contributes to the total current output as well [14].

1.2.3 Capacitance

To switch the transistors faster, the capacitance elements except gate capacitance have to be minimized. While the transistor scales down, the traditional CMOS capacitive elements (Figure 1.7), such as under-lap capacitance (C_{xud}), channel capacitance, junction capacitances (both gated edge and area) and the inner and outer fringe capacitance, will become more challenging at reduced dimensions (Figure 1.7).

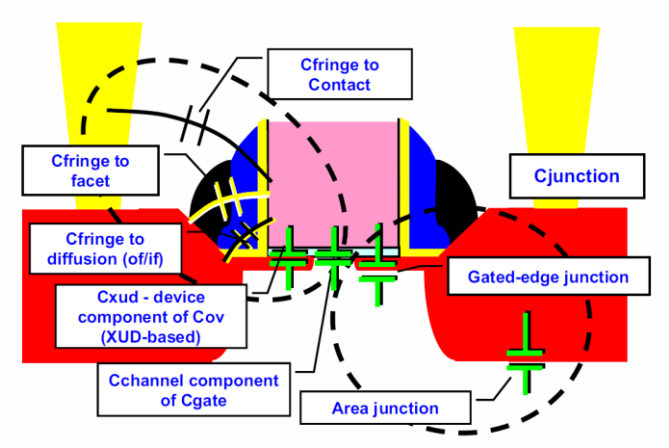


Figure 1.7: Capacitive elements in planar architectures [15]

Furthermore, in recent generations, gate and contact CD dimensions have been scaling slower than contacted gate pitch. This means that parasitic fringe capacitances (for example, contact-to-gate and epi-to-gate) are becoming significant issues. 3D geometries (such as MuGFET devices) have similar capacitive challenges as planar and also introduce additional "dead space" parasitic capacitance associated with the region between the fins [15]. These extra parasitic capacitances would raise the delay and thus, slow down the speed.

1.2.4 Power/performance Ratio

While scaling has enabled decades (both in time and scale) of improvement in CMOS VLSI, the rapid growth in subthreshold leakage has finally, fundamentally altered the direction of power/performance improvements to CMOS technology [16]. Figure 1.2(b) illustrates the growth of active and passive power density with scaling from 1 µm to sub-22 nm CMOS technology nodes. A significant transition occurs in the 130–65 nm regime, where passive power density moves from a minor part of the total to becoming dominant. This is attributed of the scaling of V_{th} and consistent or degraded *SS* values in every technology generations. It has become the main driving force of improving the gate control (*SS, DIBL*) or even leading to new device architecture such as TFETs.

1.2.5 Variation and Reliability

As technology scales further we will face new challenges, such as variability, single-event upsets (soft errors), and device (transistor performance) degradation - these effects

manifesting as inherent unreliability of the components. Moreover, as device size shrinks, the impact of these issues increases [17].

Variation sources in the CMOS front end can be categorized into two groups [18]. The first group consists of historical variation sources that will continue to offer challenges moving forward. This group includes patterning proximity effects [both classical and optical proximity correction (OPC) [19]], line-edge roughness (LER) and linewidth roughness (LWR) [20], polish variations [shallow trench isolation (STI) [21] and gate [22]], and variations in the gate dielectric (oxide thickness variations [23], fixed charge [24], and defects and traps [25]). Long-term variation management requires continuing to drive aggressive improvements for these historical sources [26, 27].

The second group includes variation sources that were historically of minor impact but have emerged as significant challenges in recent years. This group includes random dopant fluctuation [28-30], variation associated with implants and anneals [pocket implants [31] and rapid-thermal anneal (RTA) [32]], variation associated with strain [wafer-level biaxial [33], high-stress capping layers [34], and embedded silicon-germanium (SiGe) [35]], and variation associated with gate material granularity (poly gates [36] and metal gates [37]). Long-term variation management requires focused effort on understanding these sources so that new innovations and continual improvement strategies can be developed to address them.

Transistor reliability is very challenging both from the standpoint of introduction of new materials and requirement of higher field of operation for higher performance [27, 38, 39]. The reliability challenges include impact of scaling on transistor performance, gate-oxide, Negative (Positive) bias temperature instability (N(P)BTI), Hot carrier injection (HCl), silicided junctions, ESD, RC time delay, electron migration, stress migration, low-k dielectric, Joule heating and defectivity [38].

1.3 Advanced CMOS Technology for Sub-22 nm nodes

To defeat the challenges as scaling into ultra-short channel era, we categorized the developing and potential solutions into the same groups as well, which are : 1) gate control; 2) current output; 3) capacitances; 4) performance/energy ratio; 5) variation and reliability;

New technologies, which named as technology boosters, and alternative device structures are being investigated. Below is a summary of the potential solutions for the logic CMOS and the technologies shown in Figure 1.8 can mainly be categorized into the solution of improving gate control and enhancing the current output.

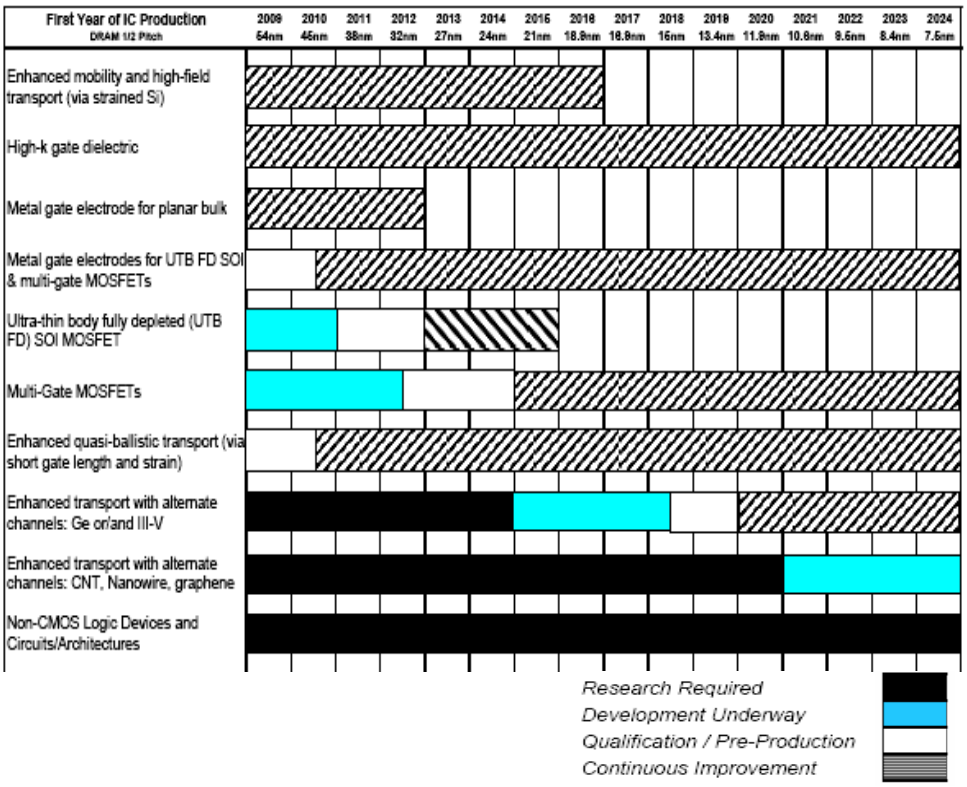


Figure 1.8: Evaluation of potential solutions for logic CMOS. [IRTS]

As shown in Figure 1.8, technologies of high-*k* gate dielectric, metal gate, UTB FD SOI and multigate structures are used to improve the gate control, while the strained Si, alternate channel materials and enhanced quasi-ballistic transport are designed to enhance the current output. Non-CMOS logic devices, such as tunnelling FET are dedicated to bypass the fundamental physical limit of subthreshold slopes, which are supposed to solve the challenges of the gate control and performance/energy ratio.

1.3.1 Progress of "non-classic" Scaling in the Industry

The golden era of traditional scaling (L_{GATE}, T_{OX}, *and* V_{DD}) in industry was in 1990's and ended by 90 nm technology node with first introduction of uniaxial strain as the mobility booster in year 2000 [40]. The second movement consists of the introduction of Hi-*k*/Metal gate at 45 nm node. And the latest approach involves with the first commercial non-planar transistor in the market at 22 nm node.

1.3.1.1 Strain and High-*k*/Metal Gate

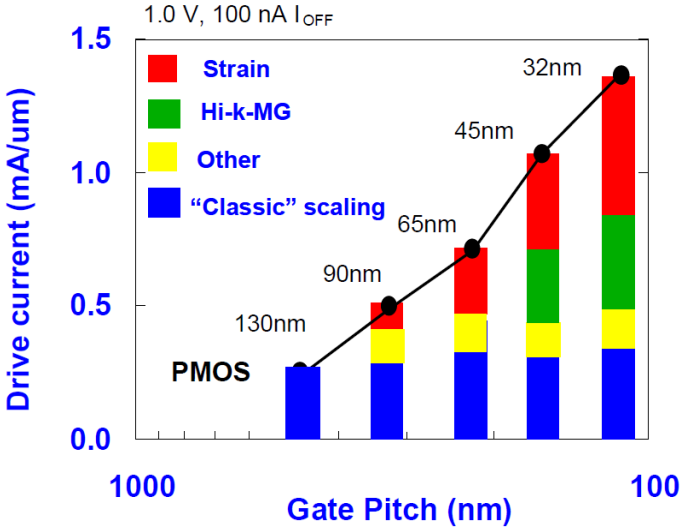


Figure 1.9: Technology boosters in modern transistor scaling by Intel [40]

From 130 nm to 90 nm technology node, the current output didn't increase as expected while L_{GATE} went shorter, which is due to the mobility degradations in highly doped channels coming from scaling of the channel doping. Thus, the strained Si was introduced to enhance the mobility of the channel, resulting in continuously increasing of the current from 130 nm to 90 nm node. Nowadays, as the gate length of the transistor goes into tens of nanometer scale, the "classic" (L_{GATE}) scaling contributes less the portion of increased drive current per technology generation as shown in Figure 1.9. Hi-*k*/Metal gate was first introduced at 45 nm technology node, in order to eliminate the gate leakage and enhance the gate control, which results in an increased current due to improvement of subthreshold slopes.

1.3.1.2 The State-of-the-art Devices: Tri-gate Transistor on Bulk Silicon

The term, Tri-gate Transistor, is used by Intel Corporation for the nonplanar transistor architecture while the other industrial and academic participants named the structure as multigate FET or FinFET. In April, 2012 Intel released a new line of CPUs, termed Ivy Bridge, which feature first commercialized tri-gate transistors.

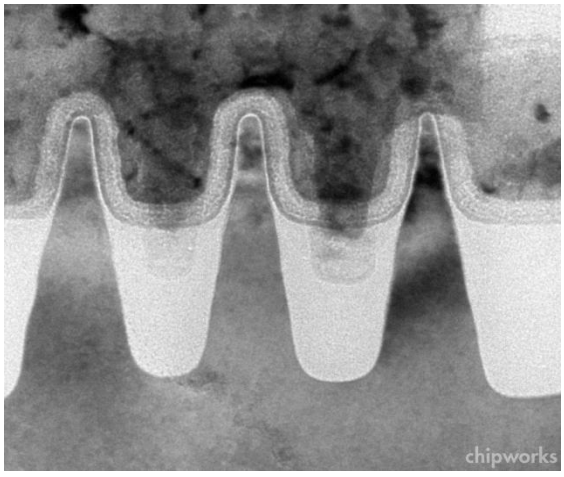


Figure 1.10: TEM images of three Intel Tri-gate fins [41].

In Figure 1.10, the first the tri-gate transistors from Intel employ a single gate stacked on top of trapezoidal Silicon substrates, allowing for essentially increased surface area than the planar devices and enhancing the gate control. The structure is likely fabricated by closing two Shallow Trench Isolation (STI), other than by defining rectangle fins directly. This allows up to 37% higher speed, or a power consumption at under 50% of the previous type of transistors used by Intel. Intel explains, "The additional control (gate control) enables as much transistor current flowing as possible when the transistor is in the 'on' state (for performance), and as close to zero as possible when it is in the 'off' state (to minimize power), and enables the transistor to switch very quickly between the two states (again, for performance)."

However, this first commercialized tri-gate transistor process is applied on the bulk substrates as Intel has eschewed SOI manufacturing for 30 years due to cost and limited vendor reasons. This technology node presents very promising gate control, however, the *SCE* immunity of tri-gate devices for sub-22 nm nodes is still susceptible. On the

other hand, the discrete channel width makes it challenging for the circuit designer and in order to achieve multi- V_{th}, the gate length has been redesigned, which is a drawback for pitch scaling. Moreover, analysis based on simulations of the released trapezoidal structure revealed that the difference in the on-current is within a 4 percent range, despite significant differences in the shape of the three fins in Figure 1.10 [41]. Compared with process variation across the chip or across the wafer 4 percent is small. But it is additional variation. Simulation revealed that the tri-gate process technology is complex and difficult to implement, partly because of the lack of a planarization process that can level-up shallow trench isolation oxides between transistors. One result of this is that bulk fin heights can vary. In contrast, moving from bulk tri-gate to tri-gate fabricated on SOI wafers could solve a number of problems and Intel may eventually need to turn to SOI wafers to scale its tri-gate beyond 22 nm.

1.3.2 Silicon-on-Insulator (SOI): From Partially Depleted SOI to Multigate SOI and Fully Depleted Extremely-Thin-Body SOI (ETSOI)

It is believed that Silicon-on-Insulator (SOI) technology, in which transistors are made in a thin silicon layer sitting on top of a silicon dioxide layer, can solve the fundamental physical limits of bulk CMOS devices [42-44]. During 1990s, SOI technology was considered as too "exotic" for real industrial applications. In the year 2000, however, SOI technology started to become mainstream and major semiconductor companies including IBM, AMD and Freescale, started to use SOI for product manufacturing. Now that SOI has established a solid reputation a reliable and trustworthy technology, an increasing number of companies consider SOI technology as the best approach to push CMOS scaling beyond the limits associated with classical silicon devices [45-47].

Advanced SOI MOSFETs with thin silicon thickness (T_{Si}) can suppress the leakage current by eliminating the part of the channel region that is not effectively modulated by the gate. However, a planar single SOI MOSFET needs ultra-thin silicon body ($T_{si}/2< L_{GATE}$) to avoid SCEs, which makes this approach challenging from a practical point of view. The body thickness can be relaxed by increasing the number of gates due to enhanced channel control ability of multigate devices, as shown in Fig 1.11. The International Technology Roadmap for Semiconductor (ITRS) recognizes the

importance of multiple-gate SOI MOSFET for the future of the microelectronics industry as shown in Figure 1.11.

Figure 1.11 shows the schematic view of the bulk, planar SOI MOSFET, and the multi-gate FET (MuGFET) category such as FinFET, tri-gate, pi-gate, omega-gate and gate-all-around SOI (GAA) devices as well as the corresponding "effective" number of gates for each device [48-53].

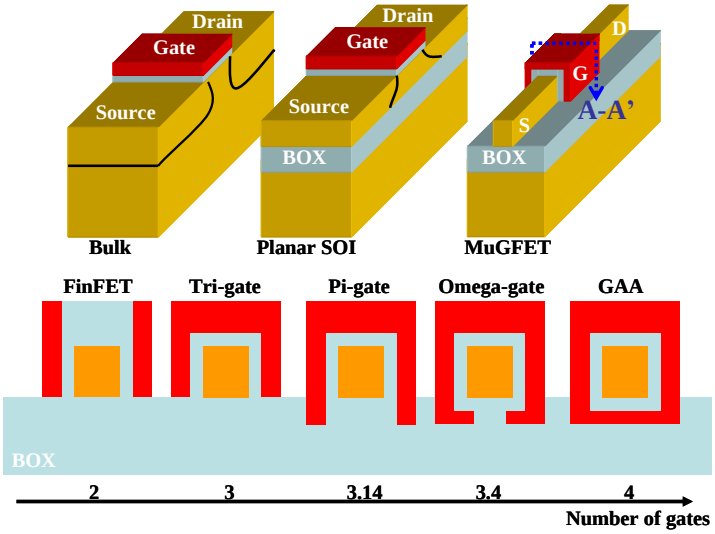


Figure 1.11: Schematic of bulk, SOI and MuGFET with cross-section of MuGFET and corresponding "effective" number of gates.

The first article on the double-gate MOS (DGMOS) transistor was published by T. Sekigawa and Y. Hayashi 1984 [54]. That paper shows that one can obtain significant reduction of short-channel effects by sandwiching a fully depleted SOI device between two gate electrodes connected together. The device was called XMOS because its cross section looks like the Greek letter Ξ (Xi). Using this configuration, a better control of the channel depletion region is obtained than in a "regular" SOI MOSFET, and, in particular, the influence of the drain electric field on the channel is reduced, which reduces short-channel effects [55]. The first fabricated double-gate SOI MOSFET was the "fully DEpleted Lean-channel TrAnsistor (DELTA, 1989)" [56], where the device is made in a tall and narrow silicon island called "finger", "leg" or "fin". The FinFET structure is similar to DELTA, except for the presence of a dielectric layer called the "hard mask" on top of the silicon fin [57, 58]. One year after the 2-gate DELTA device

was published, the first "Gate-All-Around device" (GAA) device was reported [59]. The GAA device is a planar MOSFET with the gate electrode wrapped around the channel region, the Silicon-On-Nothing (SON) MOSFET [60] is a more recent version of the GAA transistor. It is worth noting that the original GAA device was a double-gate device, even though the gate was wrapped around all sides of the channel region, because the silicon island was much wider than thick. Nowadays, most people use the GAA acronym for quadruple-gate or surrounding-gate devices having a width-to-height ratio much closer to unity [61].

1.3.2.1 Ultra-thin-body SOI and Ultra-thin-body BOX Fully Depleted SOI (UT2B FDSOI)

Although the transistor structure trends to evolve from planar to 3D for the SOI device, the other option is to fabricate the ultra-thin body BOX SOI (UT2B SOI) devices on the thinned-down silicon layer as shown in Figure 1.12.

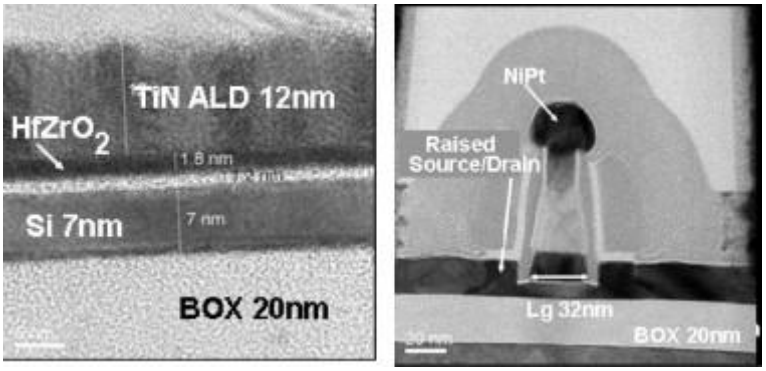


Figure 1.12: shows the transmission electron microscopy cross section of a 32 nm gate length transistor fabricated on a 20 nm thin buried oxide [62].

UT2B SOI technology has matured significantly during the last few [62-65]. Since it offers breakthroughs in terms of electrostatic control and variability, this technology is today a serious alternative to bulk for the coming technology generations. This technology is indeed likely to be scaled down to the 10 nm range with competitive gate control compared with FinFETs [63]. In addition, several performance booster options can be efficiently implemented to reach very high transistor performances. Furthermore, gate stacks allowing the design of low, medium and high threshold voltage transistors are identified and their integration is demonstrated. Finally, the use of UT2B SOI together with an implanted back-plane brings additional flexibility in terms of threshold

voltage adjustment, and ensures the efficiency of conventional power management techniques based on back-biasing, even in very aggressively scaled devices [66]. The UT2B has many advantages, in terms of multi-V_t via back-biasing and non-discrete device width, etc., however, the main drawback is the gate control compared with fully depleted FinFETs. Other concerns for the UT2B compared with FinFETs are the thermal dissipation of the high dense chip, as the oxide layer may isolate the thermal path depending on different oxide thicknesses, and the potential problems of floating body effects of SOI devices.

1.3.3 FinFET on Bulk Silicon and on SOI

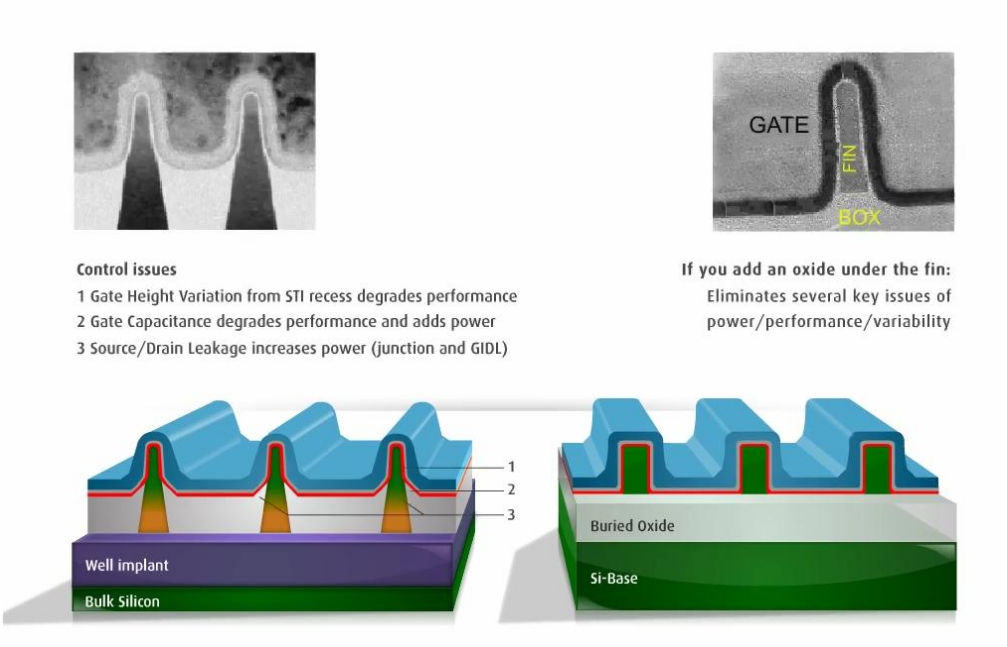


Figure 1.13: TEM and schematic of FinFET made on bulk Silicon and SOI substrates [67].

Figure 1.13 shows two proposed versions of FinFETs configurations, which on the left is the one adapted by Intel on the bulk Si and on the right one is mainly developed by IBM and STMicro. It is noticed that FinFETs for the high performance (HP) and system on chip (SOC) versions at 22 nm can be extendable to 10 nm, retaining fully depleted technology with high drive current per silicon area. However, it is facing several critical challenges. The gate height variation from STI recess degrades the performance. Gate capacitance degrades performance and adds power. Source/Drain leakage increases power (junction and *GIDL*). On the other hand, for fins on oxide configuration, it

eliminates several key issues of power/performance/variability, and are extendable to 10 nm and well beyond [68].

1.3.4 Junctionless Nanowire Transistor (JNT): Transistor without Junctions

An electrical junction refers to a thermoelectricity junction, a metal-semiconductor junction or a p-n junction (p-type semiconductor to n-type semiconductor junction). Typically, all Metal Oxide Semiconductor (MOS) transistors are made using two p-n junctions: the source junction and the drain junction. An n-channel transistor is an N-P-N structure. A p-channel transistor is a P-N-P structure. Trends in the electronic industry require smaller and smaller components resulting in transistor sizes down to the nano-scale. This is starting to pose significant manufacturing problems. In classical very small transistors one has to form two junctions, since source and drain regions are separated by channel area with opposite doping polarity [69]. The diffusion of source and drain doping atoms is difficult to control in very short-channel transistors as shown in Figure 1.14. In all transistors, the scattering and diffusion of source and drain impurities into the channel region becomes a bottleneck to the fabrication of very short-channel devices, and very low thermal budget processing techniques must be used [70].

Very costly techniques are used to minimise this diffusion, but even in the absence of diffusion the statistical variation of the impurity concentration due to ion implantation or other doping techniques can cause device parameter variation problems. There arises, therefore, the need to provide a transistor device structure that overcomes the above-mentioned problems.

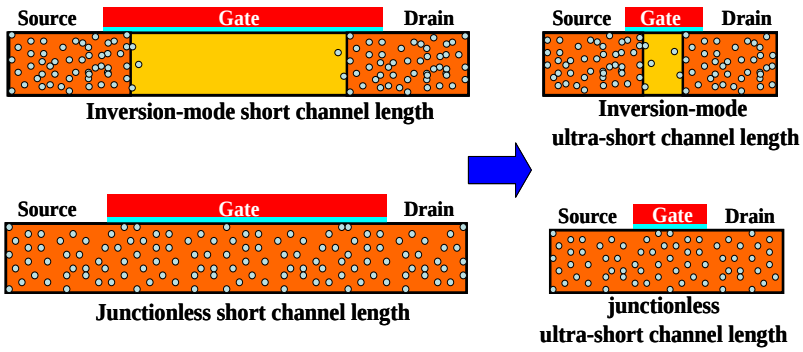


Figure 1.14: Source and drain doping of inversion-mode and junctionless transistor with short channel and ultra-short channel.

Ideally, it should be possible to completely deplete the semiconductor film of carriers, in which case the resistance of the device becomes quasi-infinite. In a multigate FET (MuGFET) the gate electrode is wrapped around a silicon wire, called “finger” or “fin”, forming a wrapping gate structure with excellent control of the channel electrostatics. The excellent gate-to channel coupling allows one to fully deplete the channel region even if it is heavily doped. The junctionless transistors (JNTs) proposed are fabricated without source and drain formation process, as the doping type and concentration in the channel region is essentially equal to that in the source and drain, or at least to that in the source and drain extensions [71-73]. These devices are essentially junction-free as shown in Figure 1.14. JNT is basically a fully depleted accumulation-mode (AM) device, consisting of a heavily-doped SOI nanowire resistor with an MOS gate to control current flow. Doping concentration is constant and uniform throughout the device and typically ranges from 10^{18} and 10^{20} cm^{-3}. The JNT device can be tuned to normal-off state when the gate workfunction is properly chosen and the highly doped channel can be fully depleted with no gate bias. As gate voltage is increased, the JNT enters into partially depletion state, and current conducts in the centre of the nanowire when V_D is supplied, and then at flatband voltage, the depletion region is completely gone. The accumulation starts at the nanowire surface when further raises the V_D, which additionally offers an accumulation current, in spite of the bulk current.

1.3.5 Access Window for IIIV and Ge Logic Devices in Roadmap

As the logic device scaling approaches 10-nanometer regime, a number of critical challenges need to be addressed. Among of them, the higher current deliverability is one of the main challenges. Strained Si has been introduced to enhance the current output, however, in order to increase the current further, the high mobility channels, such as IIIV and Ge, are demanded. Both IIIV and Ge face poor dielectric properties of their native oxides. This challenge can be relieved with the maturity of high-*k* dielectric process. Figure 1.15 shows a roadmap of the logic device scaling trend, and as seen in the figure, potential access window for IIIV and Ge can be beyond the 14 nm technology nodes. IIIV materials can deliver high electron mobility, nevertheless, Ge possesses the highest hole mobility amongst all. The ideal case is to fabricate both of

them onto the same chip; however, mixing two new materials to a manufacture process will be expensive, owing to challenges to integrate different process schemes for each material. It is preferable if both nMOS and pMOS can be made from the same material. Furthermore, hole exhibits generally much less mobility than electron for all IIIV and Ge materials, which represents a bottleneck for the CMOS. The highest hole mobility material is Ge, thus, Ge CMOS exhibits its potential of future performance enhancement, without having the penalty of involving hybrid substrates or beyond CMOS structures. Thus, there has been a strong motivation of developing both n-type and p-type Ge MOSFETs for the advanced technology nodes. When scaling down to 5 nm technology node, devices with new transport mechanisms are highly demanded [74].

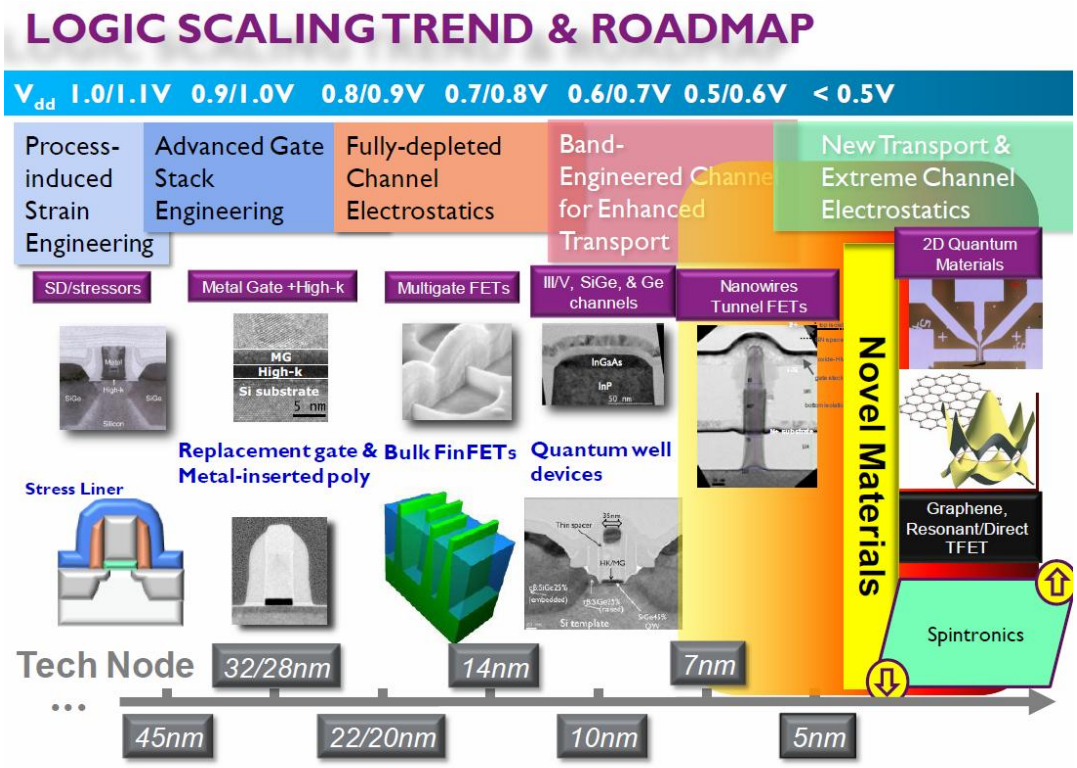


Figure 1.15: Logic scaling trend and roadmap. Potential access window opens for IIIV and Ge devices at 14 nm technology nodes, followed by devices with new transport mechanism after 5 nm technology nodes [74].

1.4 Objectives and Organization of the Thesis

The thesis is organized in the following chapters involving the simulation of the Si and Ge JNTs, characterizations of Si JNTs down to 22 nm gate length, high-*k* dielectric optimization for Ge substrate, and Ge nanowire JNTs from substrates fabrication, device processing to electrical characterizations.

Chapter 2 (Modeling) Si and Ge JNTs on different substrates are simulated by TCAD Sentaurus simulator. The characteristics of JNT are compared with conventional inversion mode transistors. Alternative JNT structure on bulk Ge substrates is discussed.

Chapter 3 (Si JNT Fabrication and Characterization) The state-of-the-art JNTs down to 22 nm gate length are fabricated and investigated. The performance of JNT is evaluated and discussed, in terms of the gate control and performance at elevated temperatures.

Chapter 4 (High-*k* Dielectric Optimization on Ge) High-*k* dielectric on Ge with a thermally formed passivation layer is investigated.

Chapter 5 (Ge Process Optimization and Ge JNT Fabrication) In this chapter, Ge JNTs down to 20 nm width are first fabricated. The performance is compared with that from literatures. Furthermore, the scopes discussed include GeOI substrates fabrication, top-down nanowire processing on Ge, processing of Ge JNT and characterizations of fabricated devices.

1.5 References

[1] Bardeen J. Surface States and Rectification at a Metal Semi-Conductor Contact. Phys Rev. 1947;71:717-27.

[2] Bardeen J, Brattain WH. The Transistor, a Semi-Conductor Triode. Phys Rev. 1948;74:230-1.

[3] Shockley W, Bardeen J, Brattain WH. The Electronic Theory of the Transistor. Science. 1948;108:678-9.

[4] Brattain WH, Bardeen J. Nature of the Forward Current in Germanium Point Contacts. Phys Rev. 1948;74:231-2.

[5] Thompson SE, Parthasarathy S. Moore's law: the future of Si microelectronics. Mater Today. 2006;9:20-5.

[6] Moore GE. Progress in digital integrated electronics. Electron Devices Meeting, 1975 International1975. p. 11-3.

[7] Nowak EJ. Maintaining the benefits of CMOS scaling when scaling bogs down. Ibm J Res Dev. 2002;46:169-80.

[8] Packan P. Performance Boosters for Advanced CMOS Devices. IEEE International Electron Device Meeting (IEDM '07) Short Course. 2007.

[9] Meyerson B. Semico Impact Conference, Taiwan. January 2004.

[10] Dennard RH, Gaenssle.Fh, Yu HN, Rideout VL, Bassous E, Leblanc AR. Design of Ion-Implanted Mosfets with Very Small Physical Dimensions. IEEE J Solid-St Circ. 1974;Sc 9:256-68.

[11] Critchlow DL. MOSFET scaling - The driver of VLSI technology. P IEEE. 1999;87:659-67.

[12] Frank DJ, Dennard RH, Nowak E, Solomon PM, Taur Y, Wong HSP. Device scaling limits of Si MOSFETs and their application dependencies. P IEEE. 2001;89:259-88.

[13] Electronic Device Architectures for the Nano-CMOS Era: From Ulitmate CMOS Scaling to Beyond CMOS Devices. Electronic Device Architectures for the Nano-Cmos Era: From Ulitmate Cmos Scaling to Beyond Cmos Devices. 2009:1-425.

[14] Kuhn KJ. CMOS scaling beyond 32nm: Challenges and opportunities. Design Automation Conference, 2009 DAC '09 46th ACM/IEEE2009. p. 310-3.

[15] Kuhn KJ. CMOS scaling for the 22nm node and beyond: Device physics and technology. VLSI Technology, Systems and Applications (VLSI-TSA), 2011 International Symposium on2011. p. 1-2.

[16] Haensch W, Nowak EJ, Dennard RH, Solomon PM, Bryant A, Dokumaci OH, et al. Silicon CMOS devices beyond scaling. Ibm J Res Dev. 2006;50:339-61.

[17] Borkar S. Designing reliable systems from unreliable components: The challenges of transistor variability and degradation. IEEE Micro. 2005;25:10-6.

[18] Kuhn K. Managing Process Variation in Intel's 45nm CMOS Process. Intel Technology Journal (ITJ), Volumn.12.

[19] Capodieci L. From optical proximity correction to lithography-driven physical design (1996-2006): 10 years of resolution enhancement technology and the roadmap enablers for the next decade. SPIE 31st International Symposium on Advanced Lithography: International Society for Optics and Photonics; 2006. p. 615401--12.

[20] Asenov A, Kaya S, Brown AR. Intrinsic parameter fluctuations in decananometer MOSFETs introduced by gate line edge roughness. Electron Devices, IEEE Transactions on. 2003;50:1254-60.

[21] Nag S, Chatterjee A, Taylor K, Ali I, O'Brien S, Aur S, et al. Comparative evaluation of gap-fill dielectrics in shallow trench isolation for sub-0.25/spl mu/m technologies. Electron Devices Meeting, 1996 IEDM'96, International: IEEE; 1996. p. 841-5.

[22] Steigerwald JM. Chemical mechanical polish: The enabling technology. Electron Devices Meeting, 2008 IEDM 2008 IEEE International: IEEE; 2008. p. 1-4.

[23] Koh M, Mizubayashi W, Iwamoto K, Murakami H, Ono T, Tsuno M, et al. Limit of gate oxide thickness scaling in MOSFETs due to apparent threshold voltage fluctuation induced by tunnel leakage current. Electron Devices, IEEE Transactions on. 2001;48:259-64.

[24] Kaushik VS, O'Sullivan BJ, Pourtois G, Van Hoornick N, Delabie A, Van Elshocht S, et al. Estimation of fixed charge densities in hafnium-silicate gate dielectrics. Electron Devices, IEEE Transactions on. 2006;53:2627-33.

[25] Wen H-C, Harris HR, Young CD, Luan H, Alshareef HN, Choi K, et al. On Oxygen Deficiency and Fast Transient Charge-Trapping Effects in High-< formula formulatype=. Electron Device Letters, IEEE. 2006;27:984-7.

[26] Kuhn K. Variation in 45nm and Implications for 32nm and Beyond. International Conference on CMOS Variability2009.

[27] Natarajan S, Armstrong M, Bost M, Brain R, Brazier M, Chang C-H, et al. A 32nm logic technology featuring 2 nd-generation high-*k*+ metal-gate transistors, enhanced channel strain and 0.171 μm 2 SRAM cell size in a 291Mb array. Electron Devices Meeting, 2008 IEDM 2008 IEEE International: IEEE; 2008. p. 1-3.

[28] Stolk PA, Widdershoven FP, Klaassen D. Modeling statistical dopant fluctuations in MOS transistors. Electron Devices, IEEE Transactions on. 1998;45:1960-71.

[29] Takeuchi K, Fukai T, Tsunomura T, Putra A, Nishida A, Kamohara S, et al. Understanding random threshold voltage fluctuation by comparing multiple fabs and technologies. Electron Devices Meeting, 2007 IEDM 2007 IEEE International: IEEE; 2007. p. 467-70.

[30] Asenov A. Random dopant induced threshold voltage lowering and fluctuations in sub-0.1 μm MOSFET's: A 3-D "atomistic" simulation study. Electron Devices, IEEE Transactions on. 1998;45:2505-13.

[31] Tanaka T, Usuki T, Futatsugi T, Momiyama Y, Sugii T. V_{th} fluctuation induced by statistical variation of pocket dopant profile. Electron Devices Meeting, 2000 IEDM'00 Technical Digest International: IEEE; 2000. p. 271-4.

[32] Ahsan I, Zamdmer N, Glushchenkov O, Logan R, Nowak E, Kimura H, et al. RTA-driven intra-die variations in stage delay, and parametric sensitivities for 65nm technology. VLSI Technology, 2006 Digest of Technical Papers 2006 Symposium on: IEEE; 2006. p. 170-1.

[33] Tsang Y, Chattopadhyay S, Uppal S, Escobedo-Cousin E, Ramakrishnan HK, Olsen SH, et al. Modeling of the Threshold Voltage in Strained Si/$Si_{1-x}Ge_x$/$Si_{1-y}Ge_y$ ($x \geq y$) CMOS Architectures. Electron Devices, IEEE Transactions on. 2007;54:3040-8.

[34] Weber O, Faynot O, Andrieu F, Buj-Dufournet C, Allain F, Scheiblin P, et al. High immunity to threshold voltage variability in undoped ultra-thin FDSOI MOSFETs and its physical understanding. Electron Devices Meeting, 2008 IEDM 2008 IEEE International: IEEE; 2008. p. 1-4.

[35] Pang L-T, Qian K, Spanos CJ, Nikolic B. Measurement and analysis of variability in 45 nm strained-Si CMOS technology. Solid-State Circuits, IEEE Journal of. 2009;44:2233-43.

[36] Brown AR, Roy G, Asenov A. Poly-Si-gate-related variability in decananometer MOSFETs with conventional architecture. Electron Devices, IEEE Transactions on. 2007;54:3056-63.

[37] Brown AR, Idris NM, Watling JR, Asenov A. Impact of metal gate granularity on threshold voltage variability: A full-scale three-dimensional statistical simulation study. Electron Device Letters, IEEE. 2010;31:1199-201.

[38] McPherson JW. Reliability challenges for 45nm and beyond. Proceedings of the 43rd annual Design Automation Conference: ACM; 2006. p. 176-81.

[39] Pae S, Ashok A, Choi J, Ghani T, He J, Lee S-h, et al. Reliability characterization of 32nm high-*k* and Metal-Gate logic transistor technology. Reliability Physics Symposium (IRPS), 2010 IEEE International: IEEE; 2010. p. 287-92.

[40] Kuhn KJ, Liu MY, Kennel H. Technology options for 22nm and beyond. Junction Technology (IWJT), 2010 International Workshop on2010. p. 1-6.

[41] http://www.goldstandardsimulations.com/.

[42] Wong HSP. Beyond the conventional transistor. Solid-State Electronics. 2005; 49: 755-62.

[43] Cristoloveanu S. Silicon on insulator technologies and devices: from present to future. Solid-State Electronics. 2001;45:1403-11.

[44] Cristoloveanu S. Future trends in SOI technologies. Journal of the Korean Physical Society. 2001;39:S52-S5.

[45] Yan RH, Ourmazd A, Lee KF. Scaling the Si MOSFET: from bulk to SOI to bulk. Electron Devices, IEEE Transactions on. 1992;39:1704-10.

[46] Yun SRN, Park WS, Lee BH, Park JT. Hot electron induced punchthrough voltage of p-channel SOI MOSFET's at room and elevated temperatures. Microelectronics Reliability. 2003;43:1477-82.

[47] Auth CP, Plummer JD. Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFET's. Electron Device Letters, IEEE. 1997;18:74-6.

[48] Doyle BS, Datta S, Doczy M, Hareland S, Jin B, Kavalieros J, et al. High performance fully-depleted tri-gate CMOS transistors. Electron Device Letters, IEEE. 2003;24:263-5.

[49] Jong-Tae P, Colinge JP. Multiple-gate SOI MOSFETs: device design guidelines. Electron Devices, IEEE Transactions on. 2002;49:2222-9.

[50] Jong-Tae P, Colinge JP, Diaz CH. Pi-Gate SOI MOSFET. Electron Device Letters, IEEE. 2001;22:405-6.

[51] Park JT, Colinge CA, Colinge JP. Comparison of gate structures for short-channel SOI MOSFETs. SOI Conference, 2001 IEEE International2001. p. 115-6.

[52] Fu-Liang Y, Hao-Yu C, Fang-Cheng C, Cheng-Chuan H, Chang-Yun C, Hsien-Kuang C, et al. 25 nm CMOS Omega FETs. Electron Devices Meeting, 2002 IEDM '02 Digest International2002. p. 255-8.

[53] Colinge JP, Gao MH, Romano-Rodriguez A, Maes H, Claeys C. Silicon-on-insulator `gate-all-around device'. Electron Devices Meeting, 1990 IEDM '90 Technical Digest, International1990. p. 595-8.

[54] Sekigawa T. Calculated threshold-voltage characteristics of an XMOS transistor having an additional bottom gate. Solid-State Electron. 1984;27:827.

[55] Agrawal B, De V, Pimbley J, Meindl J. Short channel models and scaling limits of SOI and bulk MOSFETs. Solid-State Circuits, IEEE Journal of. 1994;29:122-5.

[56] Hisamoto D, Kaga T, Kawamoto Y, Takeda E. A fully depleted lean-channel transistor (DELTA)-a novel vertical ultra thin SOI MOSFET. Electron Devices Meeting, 1989 IEDM'89 Technical Digest, International: IEEE; 1989. p. 833-6.

[57] Huang X, Lee W-C, Kuo C, Hisamoto D, Chang L, Kedzierski J, et al. Sub 50-nm FinFET: PMOS. Electron Devices Meeting, 1999 IEDM'99 Technical Digest International: IEEE; 1999. p. 67-70.

[58] Hisamoto D, Lee W-C, Kedzierski J, Takeuchi H, Asano K, Kuo C, et al. FinFET-a self-aligned double-gate MOSFET scalable to 20 nm. Electron Devices, IEEE Transactions on. 2000;47:2320-5.

[59] Colinge J-P, Gao M, Romano-Rodriguez A, Maes H, Claeys C. Silicon-on-insulatorgate-all-around device'. Electron Devices Meeting, 1990 IEDM'90 Technical Digest, International: IEEE; 1990. p. 595-8.

[60] Jurczak M, Skotnicki T, Paoli M, Tormen B, Martins J, Regolini JL, et al. Silicon-on-nothing (SON)-an innovative process for advanced CMOS. Electron Devices, IEEE Transactions on. 2000;47:2179-87.

[61] Singh N, Agarwal A, Bera L, Liow T, Yang R, Rustagi S, et al. High-performance fully depleted silicon nanowire (diameter≤ 5 nm) gate-all-around CMOS devices. Electron Device Letters, IEEE. 2006;27:383-6.

[62] Fenouillet-Beranger C, Denorme S, Perreau P, Buj C, Faynot O, Andrieu F, et al. FDSOI devices with thin BOX and ground plane integration for 32nm node and below. Solid State Electron. 2009;53:730-4.

[63] Khakifirooz A, Cheng K, Reznicek A, Adam T, Loubet N, He H, et al. Scalability of extremely thin SOI (ETSOI) MOSFETs to sub-20-nm gate length. Electron Device Letters, IEEE. 2012;33:149-51.

[64] Cheng K, Khakifirooz A, Kulkarni P, Ponoth S, Haran B, Kumar A, et al. ETSOI CMOS for system-on-chip applications featuring 22nm gate length, sub-100nm gate pitch, and 0.08 μm 2 SRAM cell. VLSI Technology (VLSIT), 2011 Symposium on: IEEE; 2011. p. 128-9.

[65] Choi Y-K, Asano K, Lindert N, Subramanian V, King T-J, Bokor J, et al. Ultra-thin body SOI MOSFET for deep-sub-tenth micron era. Electron Devices Meeting, 1999 IEDM'99 Technical Digest International: IEEE; 1999. p. 919-21.

[66] Nazarov A, Colinge J-P, Balestra F, Raskin J-P, Gamiz F, Lysenko V. Semiconductor-on-insulator materials for nanoelectronics applications: Springer; 2011.

[67] http://www.soiconsortium.org/.

[68] E.J.Nowak. 2nd-Generation FinFETs and Fins on Oxide. Fully Depleted Transistors Technology Symposium. San Francisco, California U.S.A.Dec. 10, 2012.

[69] Nieh CF, Ku KC, Chen CH, Chang H, Wang LT, Huang LP, et al. Millisecond Anneal and Short-Channel Effect Control in Si CMOS Transistor Performance. Electron Device Letters, IEEE. 2006;27:969-71.

[70] Jain SH, Griffin PB, Plummer JD, McCoy S, Gelpey J, Selinger T, et al. Low resistance, low-leakage ultrashallow p+ junction formation using millisecond flash anneals. Electron Devices, IEEE Transactions on. 2005;52:1610-5.

[71] Barraud S, Berthome M, Coquand R, Casse M, Ernst T, Samson MP, et al. Scaling of Trigate Junctionless Nanowire MOSFET With Gate Length Down to 13 nm. IEEE Electr Device L. 2012;33:1225-7.

[72] Colinge JP, Lee CW, Afzalian A, Akhavan ND, Yan R, Ferain I, et al. Nanowire transistors without junctions. Nat Nanotechnol. 2010;5:225-9.

[73] D.-Y. Jeon SJP, M. Mouis, M. Berthomé, S. Barraud, G.-T. Kim and G. Ghibaudo. Electrical characterization and Revisited Parameter Extraction Methodology in Junctionless Transistors. EuroSOI 2012, Montpellier - France. 2012:109-10.

[74] Thean A. Silicon & beyond CMOS: The Path of Advanced Electronic Structure Engineering for Low-Voltage Transistors. Solid State Phenomena. 2013;195:3.

Chapter 2 TCAD Application on Semiconductor Devices and Process: Simulation of Silicon and Germanium JNT

Abstract: In this chapter, the simulations are carried out using the Synopsys Technology Computer-Aided Design (TCAD) software, in order to compare the Junctionless transistors (JNT) with the Inversion Mode (IM) devices, in terms of gate control, vertical electric field and capacitances. The unique conduction mechanism and electrical characteristics for JNT have been discussed. In order to scale the V_{DD}, lower *SS* value (sub-60 mV/dec at room temperature) in JNT has been obtained by simulation. The dependence of the effect on gate length is investigated and their influence on the I_D-V_G curves is discussed. For future current enhancement, simulation of JNTs with high mobility Ge channel was performed.

2.1 TCAD Introduction

Technology Computer-Aided Design (TCAD) refers to using computer simulations to develop and optimize semiconductor processing technologies and devices. TCAD simulation tools solve fundamental, physical, partial differential equations, such as diffusion and transport equations for discretized geometries, representing the silicon wafer or the layer system in a semiconductor device. This deep physical approach allows TCAD simulation predictive accuracy. Therefore, it is possible to substitute TCAD computer simulations for costly and time-consuming test wafer runs when developing and characterizing a new semiconductor device or technology.

TCAD simulations are used widely in the semiconductor industry. As technologies become more complex, the semiconductor industry relies increasingly more on TCAD to cut costs and speed up the research and development process. The ITRS predicts 40% saving in development time and cost with TCAD. In addition, semiconductor manufacturers use TCAD for yield analysis, that is, monitoring, analysing, and optimizing their IC process flows, as well as analysing the impact of IC process variation. TCAD consists of two main branches: process simulation and device simulation. The main suppliers of the conventional TCAD tools include Synopsys [1],

which is mostly used in industry and Silvaco [2], which is prevailing in the academic world.

2.1.1 Process Simulation

In process simulation, processing steps such as etching, deposition, ion implantation, thermal annealing, and oxidation are simulated based on physical equations, which govern the respective processing steps. The simulated part of the silicon wafer is discretized (meshed) and represented as a finite-element structure (see Figure 2.1).

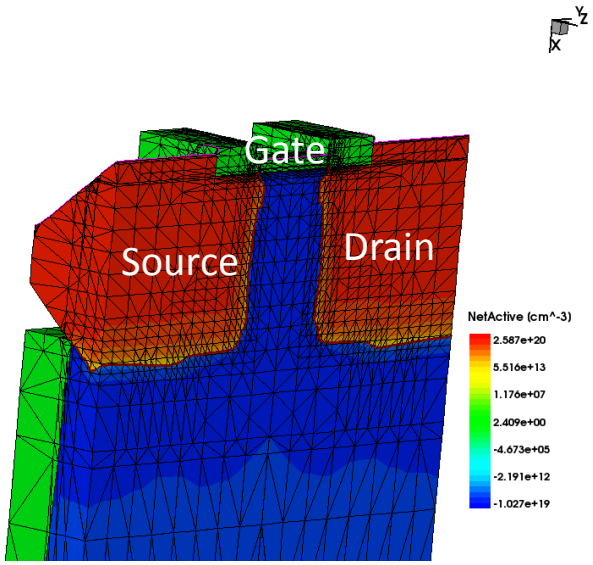


Figure 2.1: Illustration of n-FinFET with epi-grown source/drain regions and HfO_2 gate dielectric built by TCAD process simulation tool.

For example, in the simulation of thermal annealing, complex diffusion equations for each dopant species are solved on this mesh. For oxidation simulations, the growth of silicon oxide is simulated taking into account the oxygen diffusion, the mechanical stresses at corners, and so on.

2.1.2 Device Simulation

Device simulations can be thought of as virtual measurements of the electrical behaviour of a semiconductor device, such as a transistor or diode. The device is represented as a meshed finite-element structure. Each node of the device has properties associated with it, such as material type and doping concentration. For each node, the

carrier concentration, current densities, electric field, generation and recombination rates, and so on are computed (see Figure 2.2(a)).

Electrodes are represented as areas on which boundary conditions, such as applied voltages, are imposed. The device simulator solves the Poisson equation and the carrier continuity equation (and possibly other equations). After solving these equations, the resulting electrical currents at the contacts are extracted (see Figure 2.2(b)).

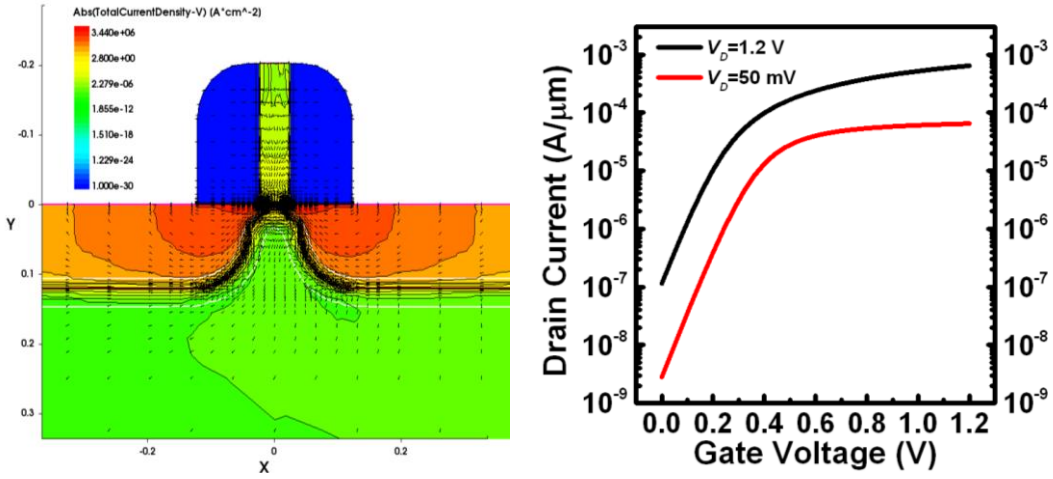


Figure 2.2: (a) Current flow arrows in a 45 nm NMOSFET at V_{gs} = 1.2 V and V_{ds} = 50 mV. (b) Drain current as function of gate voltage for the same 45 nm NMOSFET at V_{ds} = 50 mV and 1.2 V.

2.2 Device Physics of JNT

To avoid abrupt PN junctions for ultra-short channel, the novel JNT without doping concentration gradients in the device is introduced. JNT is basically a fully depleted accumulation-mode (AM) device, consisting of a heavily-doped SOI nanowire resistor with an MOS gate to control current flow. Doping concentration is constant and uniform throughout the device and typically ranges from 10^{18} and 10^{20} cm^{-3}. The JNT device can be tuned to normal-off state when the gate workfunction is properly chosen [3]. The highly doped channel can be fully depleted as shown in Figure 2.3(a). As gate voltage is increased, the JNT enters into partially depletion state, and current conducts in the centre of the nanowire when V_D is supplied (Figure 2.3(b,c)). At flatband voltage, the depletion region is completely gone (Figure 2.3(d)) and the accumulation starts at

the nanowire surface, which additionally offers an accumulation currents, in spite of the bulk current.

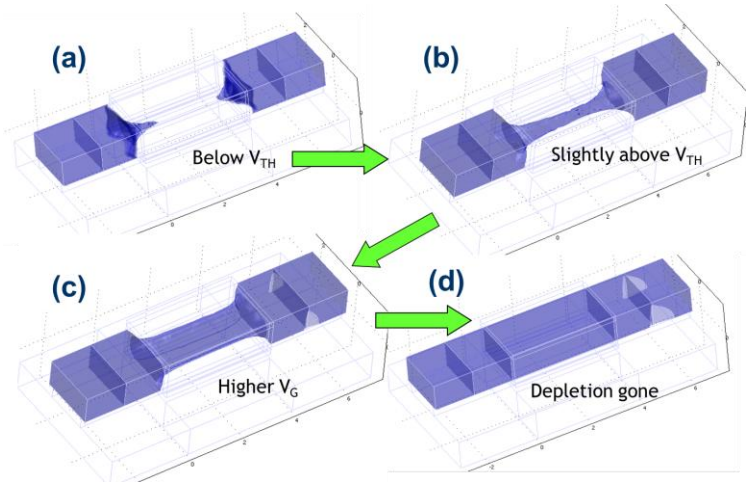


Figure 2.3: Electron concentration contour plots in an n-type junctionless transistor with V_D =50 mV. (a): V_G = 0 V; (b): V_G = 100 mV; (c): V_G = 300 mV; (d): V_G = 400 mV = Flatband voltage.

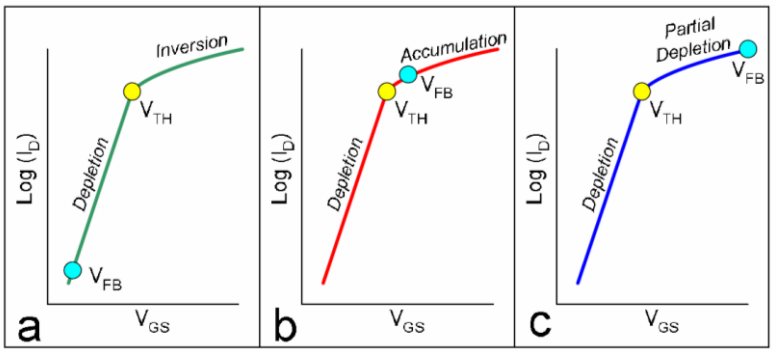


Figure 2.4: Current in different nanowire MuGFETs (a) Inversion-mode, (b) accumulation-mode and (c) junctionless. JNT operates in partial depletion region before reaches flatband voltage. Note the very different positions of the flatband voltage, V_{FB} [4].

The physics of the JNT is quite different from that of standard MuGFETs. Depletion of the heavily doped nanowire creates a large electric field perpendicular to current flow below threshold, but above threshold the field drops to zero. This is the opposite of inversion-mode (IM) or even accumulation-mode (AM) devices where the field is highest when the device is turned on. In Figure 2.4, conduction mechanism of nanowire MuGFETs in IM, AM and JNT are compared. It is noted that JNT operates in partial depletion region before reaches flatband voltage, while the other two modes exhibit very different positions of the flatband voltage, V_{FB} [4].

2.3 Simulation of Si JNT and its Comparison to Conventional Inversion Mode (IM) Transistors

In this section, the simulations were carried out, in order to compare the JNT with the IM devices, in terms of gate control, vertical electric field and capacitances. The results show that the JNT have unique characteristics and it is a very promising candidate for future decananometer MOSFET applications.

2.3.1 Merits of JNT: Superior Gate Control without Abrupt Junctions

Simulations of the IM and JNT MuGFETs have been carried out with the parameters shown in Table 2.1. The electrical characteristics of both conventional (N^+-P-N^+) and junctionless (N^+-N^+-N^+) devices were simulated using the Atlas 3-D device simulator. Abrupt source and drain junctions are used for the conventional transistors.

	Conventional	**Junctionless**
Channel doping	2×10^{15} cm^{-3} (P-type)	8×10^{19} cm^{-3} (N-type)
Gate oxide thickness	2 nm	2 nm
Gate work function	4.6 eV	5.5 eV
T_{si}	5 nm	5 nm
W_{fin}	5 nm	5 nm
L_{GATE}	5–30 nm	10–30 nm

Table 2.1: Device parameters of IM and JNT MuGFET.

Because of the *N*-type doping of the channel, a *N*-channel junctionless device requires a gate material with a high work function such as *P*+ polycrystalline silicon or platinum in order to achieve a suitable V_{th} value. It is, however, clear that the use of a metal as gate material is preferable for gate resistance reduction purposes. It is also to be noted that the junctionless device allows itself to the use of both gate-first and gate-last process, which facilitates the use of a metal gate. A midgap gate material is used for the classical IM device. If the cross section of the channel is small enough, the gate can deplete the heavily doped channel entirely, which turns the transistor off.

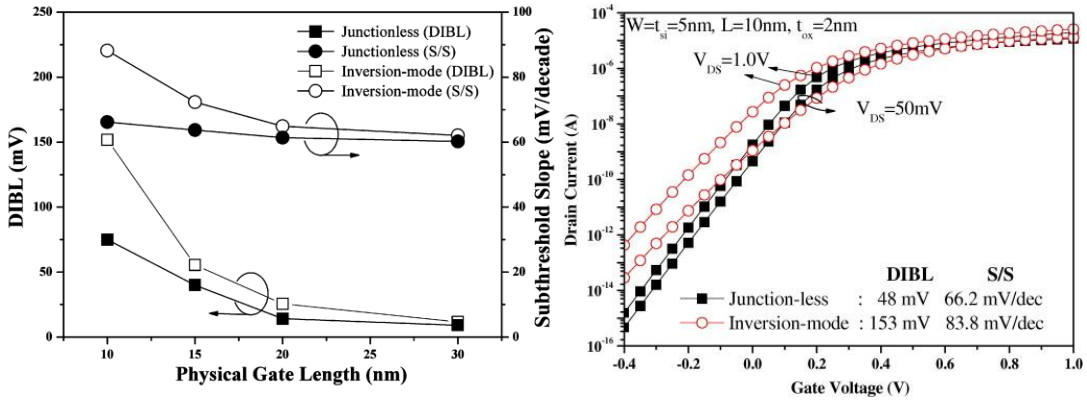


Figure 2.5: (a) *DIBL* and subthreshold slope at V_{DS} = 50 mV in JNT and IM devices for different gate length values from simulation [5]. (b) I_d–V_G characteristic of a JNT and an inversion-mode device with L_{GATE} = 10 nm [6].

The subthreshold characteristics of junctionless MuGFETs with different gate lengths (10–30 nm) at low drain voltage are shown in Figure 2.5(a). The subthreshold slope of shortest JNT (L_{GATE} = 10 nm) is below 70 mV/decade. This shows the potential of JNT for extremely short-channel applications. It is important to note that the off current is determined solely by the electrostatic control of the gate and not by the leakage current of a reverse-biased diode. This renders the device less sensitive to temperature and to contamination, which reduces carrier lifetime. It also enables one to minimize leakage current if a small bandgap semiconductor such as germanium is used. It is important for the cross section of the JNT to be sufficiently small in order to be able to fully deplete the channel of carriers and turn the device off. The higher the channel doping concentration, the smaller the cross section needs to be. In Figure 2.5(b), the electrical characteristics of junctionless and classical IM devices are compared. It can be seen that the JNT exhibits better subthreshold slope and *DIBL* characteristics than inversion-mode devices in this configuration.

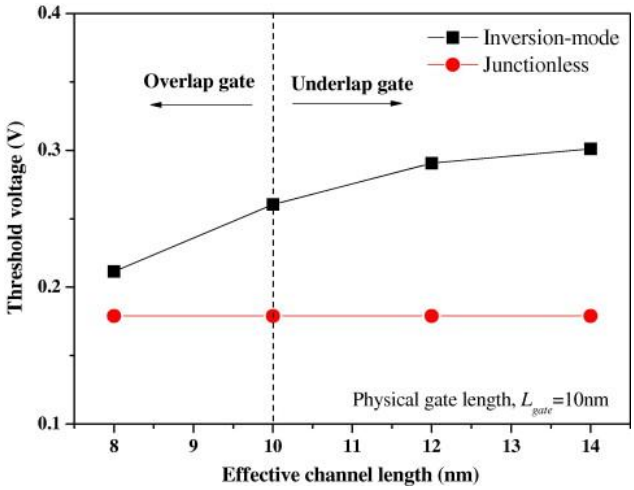


Figure 2.7: Threshold voltage of junctionless and inversion-mode devices as a function of effective channel length at V_{DS} = 50 mV.

Figure 2.7 shows simulated threshold voltage of IM devices and JNTs as a function of effective channel length at low drain voltage. The threshold voltage in IM devices drops corresponding to the shorter gate length, while the threshold voltage of the JNT present insensitive to effective channel length.

In summary, simulation results show that when proper configurations are set up, the JNT exhibits the potential to surpass the conventional IM devices in terms of *DIBL*, *SS* and V_{th} roll off, which represent a better gate control of JNT.

2.3.2 Merits of JNT: Relaxed Vertical Electric Field

Figure 2.8 shows the electron concentration in the form of concentration contour lines, superimposed to a grayscale representation of the norm of the electric field. The lower the field, the darker the gray shading, and the higher the field the lighter the gray shading. Some particular values of the field are given at locations marked by the symbol "⊗."

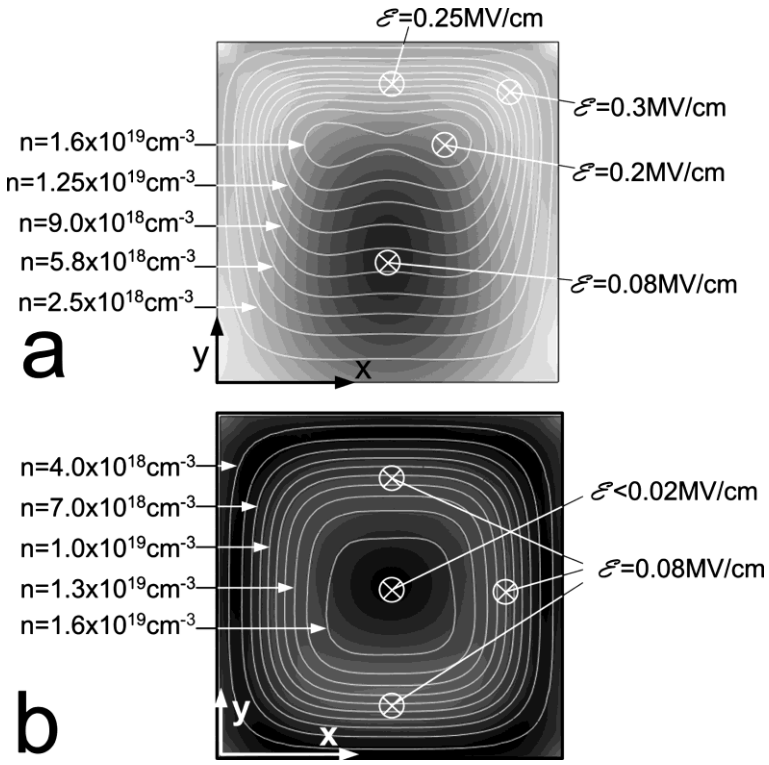


Figure 2.8: Electron concentration contour lines superimposed to a grayscale representation of the amplitude of the electric field. The lower the field, the darker the gray shading, and the higher the field the lighter the gray shading. Field values are given at locations marked by the symbol "⊗." (a) IM device and (b) JNT [7].

In the IM device, the majority of the inversion carriers, and in particular the points of peak electron concentration, are located in high electric field regions. This is quite normal, considering that inversion electrons are present because they are attracted by the electric field emanating from the gate. Accumulation-mode devices show results that are basically identical to those of inversion-mode devices. In the JNT, on the other hand, the peak electron concentration coincides with the region of lowest electric field. The field is not quite equal to zero but it is much lower ($E<0.02$ MV/cm) than in the inversion-mode device ($E \geq 0.2$ mV/cm). This may offer an advantage to JNT in terms of relaxed gate electric field, hence, easier high-*k* passivation scheme for the gate leakage current and better reliability.

2.3.3 Merits of JNT: Reduced Capacitance

The gate delay, that how fast the gate can be charged, is roughly proportional to the capacitance of gate. The reduction of gate capacitances is very important to boost the

performance of the MOSFETs. In this section, the simulation results of gate capacitances for both JNT and IM are compared. The JNT and IM devices simulated in this section have the same tri-gate structure and without S/D spacers. The physical gate length, L_{GATE}, for both JNT and IM devices is 25 nm. The theoretical maximum gate capacitance is calculated as 2.59×10^{17} F, with the corresponding configurations of the JNT and IM devices.

All I_{OFF} have been fixed to 100 nA/μm, corresponding to high performance MOSFETs, by applying the proper gate work functions. At the off-state, all the transistors show about identical gate capacitance C_{gg} (Figure 2.9), gate to source capacitance C_{gs} (Figure 2.10) and drain to gate capacitance C_{dg} (Figure 2.11). As the gate voltage increased, the IM transistor forms an inversion channel underneath the gate, while the JNT devices slowly reduce the depletion region and form a channel in the centre of the channel. Further increase of gate bias leads to the saturation of minority carrier at the Si/SiO_2 interface for IM, while majority carrier accumulates at the interface for JNT. The C_{gg} is slightly lower for JNT with $N_d = 4\times10^{19}$ cm^{-3} at $V_D = 1$ V, but the difference becomes larger when the V_D is scaled.

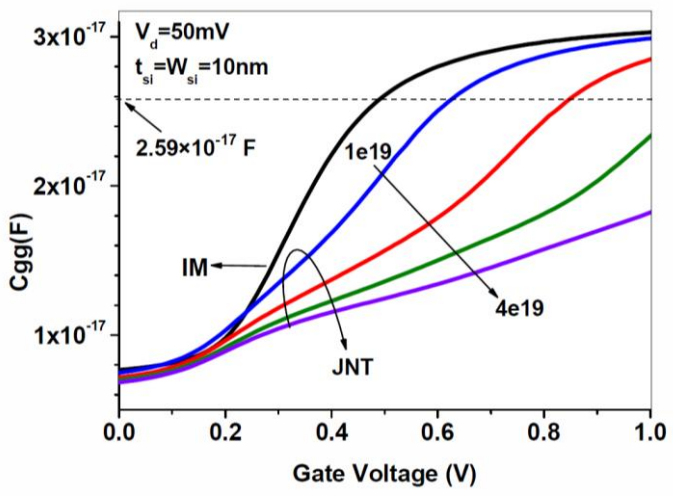


Figure 2.9: C_{gg} gate capacitance as a function of gate voltage for IM transistor and JNT.

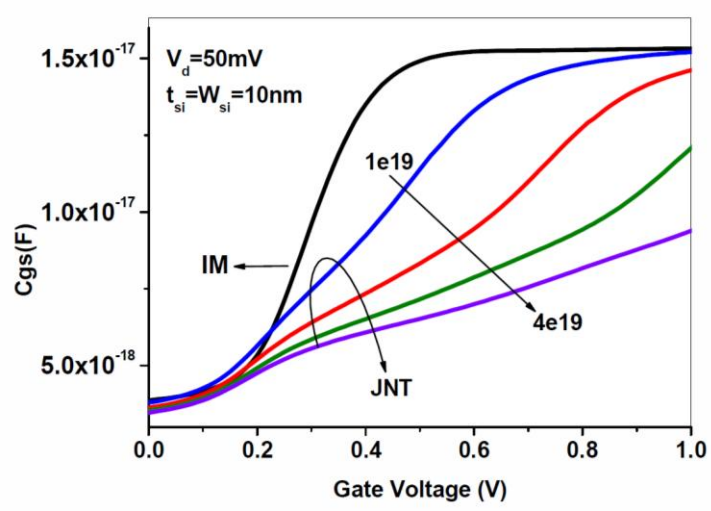


Figure 2.10: C_{gs} gate to source capacitance as a function of gate voltage for JNT and IM.

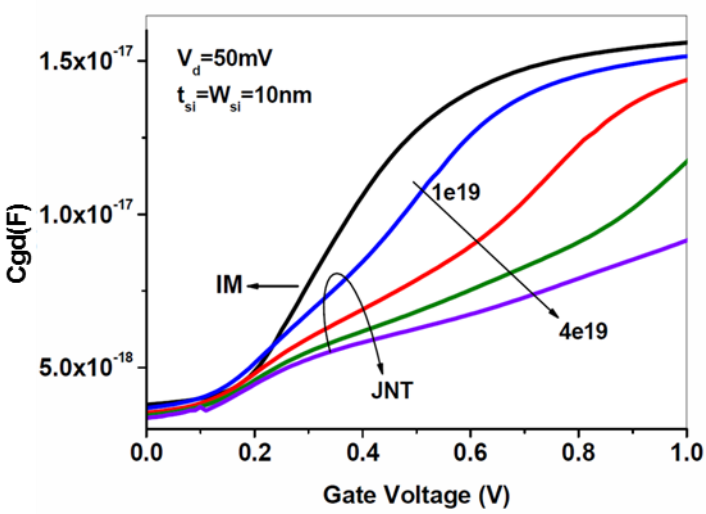


Figure 2.11: C_{gd} gate to drain capacitance as a function of gate voltage for JNT and IM.

For JNT with high doping concentration like N_d = 4×10^{19} cm^{-3}, as the leakage currents are fixed, the degraded subthreshold slopes result in a stretching out of the I_D-V_G curves. Thus, the capacitance is low because the gate bias has not even reached the flatband voltage and depletion layer still exists beneath the gate oxide. The capacitance can be further reduced by increasing the doping concentration in the channels, however, the device parameters have to be carefully designed, in order to minimize the penalty from subthreshold slope degradation.

In summary, the JNT devices have lower gate capacitance than IM transistor. By increasing the doping concentration in the channel of JNT, reduction of gate capacitance can be further modified. Additionally, the device parameters have to be carefully designed, in order to minimize the penalty from subthreshold slope degradation.

2.3.4 Potential Drawbacks of JNTs: V_{th} Variability and Mobility Degradation

The threshold voltage (V_{th}) of a JNT depends on the doping concentration N_D(N_A), on the effective gate oxide thickness *EOT*, on the nanowire thickness T_{Si} and its width W_{Si}.

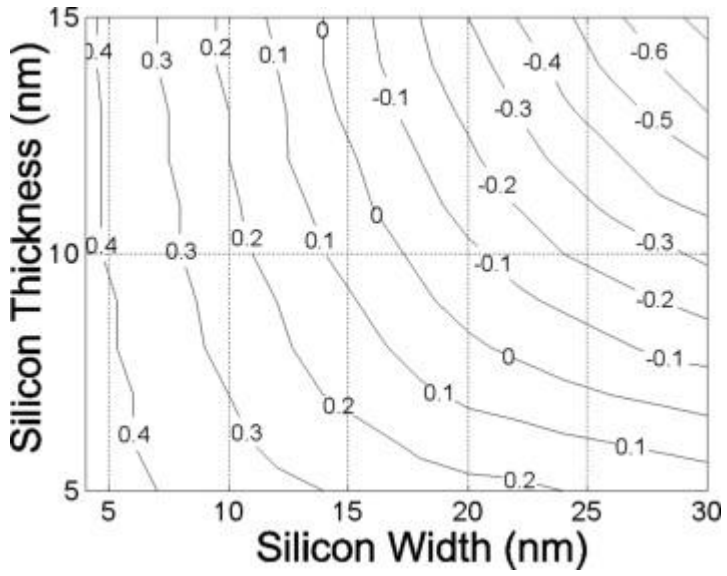


Figure 2.12: Long-channel JNT V_{th} vs. nanowire width and thickness for $N_D = 10^{19}$ cm^{-3} and *EOT* = 1 nm (midgap metal gate).

Figure 2.12 give examples of V_{th} variation with nanowire width and thickness, for selected values of N_D and *EOT*. The V_{th} variation with W_{Si} offers high flexibility for tuning threshold voltages. For instance, for a midgap metal gate, a channel doping concentration $N_D = 10^{19}$ cm^{-3}, T_{Si} = 10 nm and *EOT* = 1 nm, a device with V_{th} = 0.1 V is obtained if W_{Si} = 14 nm and a device with V_{th} = 0.2 V is obtained if W_{Si} = 11 nm (Figure 2.12). On the other side, this may result in unacceptable variation of electrical parameters on a wafer and from wafer to wafer. If a 15 nm-thick SOI layer is used, the threshold voltage variation with linewidth is very high (dV_{th}/dW_{Si} = 50 mV/nm). However, if T_{Si} is reduced to 5 nm, a much more acceptable variation is obtained: (dV_{th}/dW_{Si} = 13 mV/nm) [8]. The uniformity of the modern SOI wafers is

controlled less than 0.5 nm. It gives the opportunity to implement the JNT into the sub-22-nm technology nodes, however, with a tighter process window during the fabrication [9].

Another major concern is on the mobility degradation of the JNTs. Owing to the highly doped channel, the bulk mobility decreases dramatically. This limits the current deliverability of the JNTs, especially compared with the strained Si IM transistors. Effort has been made to apply the mobility enhancement techniques on JNTs and current enhancement has been observed [10]. Regardless the mobility degradation in highly doped channel, JNT exhibits two other strengths, which are attributed to the unique bulk current conduction and missing of the PN junctions. The bulk current conduction of JNTs relaxes the mobility degradation due to the surface scattering, which is related to a high vertical electric field, interface states, acoustic phonons, and surface roughness. Furthermore, owing to the missing PN junctions in JNTs, the mobility degradation associated to process induced defects located near the source and drain junctions can be improved [11].

2.4 Simulation of Impact Ionization Effect in Short Channel JNT

Supply voltage (V_{DD}) of a MOSFET transistor is continually reduced while gate length becomes shorter according the scaling rule. Both supply voltage and gate length scaling leads to a smaller gate delay (CV/I) and lower dynamic dissipation of the transistor. To have an acceptable on-current when V_{DD} is reduced, it requires further reduction of the threshold voltage. However, with a very fundamental limit of subthreshold slope (*SS*) of 60 mV/dec at room temperature, the off-current is increased simultaneously when threshold voltage is reduced. Thus, the static dissipation is increased and it cancels the reduction of dynamic dissipation of a short channel transistor. Theoretically, lower *SS* value (sub-60 mV/dec) can be expected to deliver higher on-current with a reduced supply voltage at the gate. To date, transistors with two different types of mechanisms show *SS* values below 60mV/dec at room temperature. One is the band to band tunneling FET and the other one is transistors with impact ionization effects [12, 13]. In this section, the dependence of impact ionization

effects on gate length is investigated and their influence on the I_D-V_G curves is discussed.

2.4.1 Device Structure and Simulation

Using Sentaurus Device Editor, 2-D double gate JNTs were built for the simulations. The thickness of the Silicon layer is 10 nm and the gate oxide is 2 nm. The entire nanowire is doped with 1×10^{19} cm^{-3} Arsenic. Various gate lengths from 100 nm to 32 nm are simulated. The mesh is carefully generated for the impact ionization region. The effective electric field obtained from the electron or hole carrier temperature is defined as the driving force in the calculation of generation rate of electron and hole pairs. The Van Overstraeten –de Man model is employed to calculate the ionization coefficient with following expression:

$$\alpha(F_{ava}) = \gamma a \exp\left(\frac{\gamma b}{F_{ava}}\right) \quad (1),$$

with:

$$\gamma = \frac{\tanh\left(\frac{\hbar\omega_{op}}{2kT_o}\right)}{\tanh\left(\frac{\hbar\omega_{op}}{2kT}\right)} \quad (2),$$

where α is the ionization coefficient, Fava is the effective electric field, $\hbar\omega_{op}$ is optical phonon energy expresses the temperature dependence of the phonon gas against which carriers are accelerated. The parameters, a and b, are related to material properties. Drain voltage arises from 1 V to 2 V with step of 0.2 V and the I_D-V_G curves of 32 nm and 65 nm are compared.

2.4.2 Results and Discussions

To further explain the steep subthreshold slope effect in JL devices, 2-D double gate simulations are carried out for a device with L_{GATE} = 100 nm, $N_d = 1 \times 10^{19}$ cm^{-3}, T_{Si} = 10 nm and 2 nm effective oxide thickness. Simulation results are extracted in the subthreshold region just as the impact ionization occurs. Figure 2.13 shows the 2-D double gate device simulation results of (a) electron current density, (b) impact ionization rate, (c) hole current density, (d) hole density, (e) electron density and (f)

SRH recombination rate for JL MOSFET. Figure 2.13(a) shows that the electron current starts to flow in the centre of the channel when the device is about to be turned on. Associated with a high electric field, impact ionization occurs around the channel-drain boundary (Figure 2.13(b)). Then electron-hole pairs are generated and holes flow along the SiO_2-Si interfaces away from the channel centre (Figure 2.13(c)). Figure 2.13(d) shows the holes accumulate near the SiO_2-Si interfaces and form a floating body. As holes are minority carriers in the JL device, it continuously recombines with the majority carrier. In contrast, the holes generated in IM devices flows towards the centre of the fin, where it is a p-type substrate and holes are majority carriers in this region. These holes would not recombine continuously when the bias conditions are not satisfied, and discharging of these holes may depend on many factors. It could result in worse adverse effects, such as history effect, which is difficult to be predicted. On the other hand, JL devices do not face this problem because the generated holes flow into an n-type substrate and recombine with electron continuously. Thus, this floating body in JL devices is relatively dynamic comparing with that in IM devices. Due to the electron distribution in the channel (Figure 2.13(e)) the holes gathering near the SiO_2-Si interfaces recombine with the electrons flowing in the channel (Figure 2.13(f)). The migrated holes can give a rise of the body potential, which decrease the threshold voltage. As the threshold voltage decreases, it results in an increase of drain current and impact ionization is further enhanced due to the increased drain current. Extra holes generated by the impact ionization again migrate towards the SiO_2-Si interfaces and enhance the floating body effects. It results in a positive feedback loop to turn on the device, hence steeper subthreshold slopes. In this loop, many factors can enhance the effect, such as the narrowed bandgap, increased impact ionization rate and area in JL device. The geometry of the device strongly affects the formation of the floating body. This explains why no low subthreshold slopes are observed in the measured narrow IM and JL devices. Another important factor to enhance the positive feedback is the electric field and it can be expected that increased electric field in short channel devices can trigger the effect at a lower V_{DD}.

In Figure 2.14 (a), it shows the electron temperature reaches a peak around 6000 K at the edge of the gate which corresponds to a high generation of electron and hole pairs, where the impact ionization occurs. Around the same region, the potential has a maximum change, hence a peak of electric field (Figure 2.14 (b)).

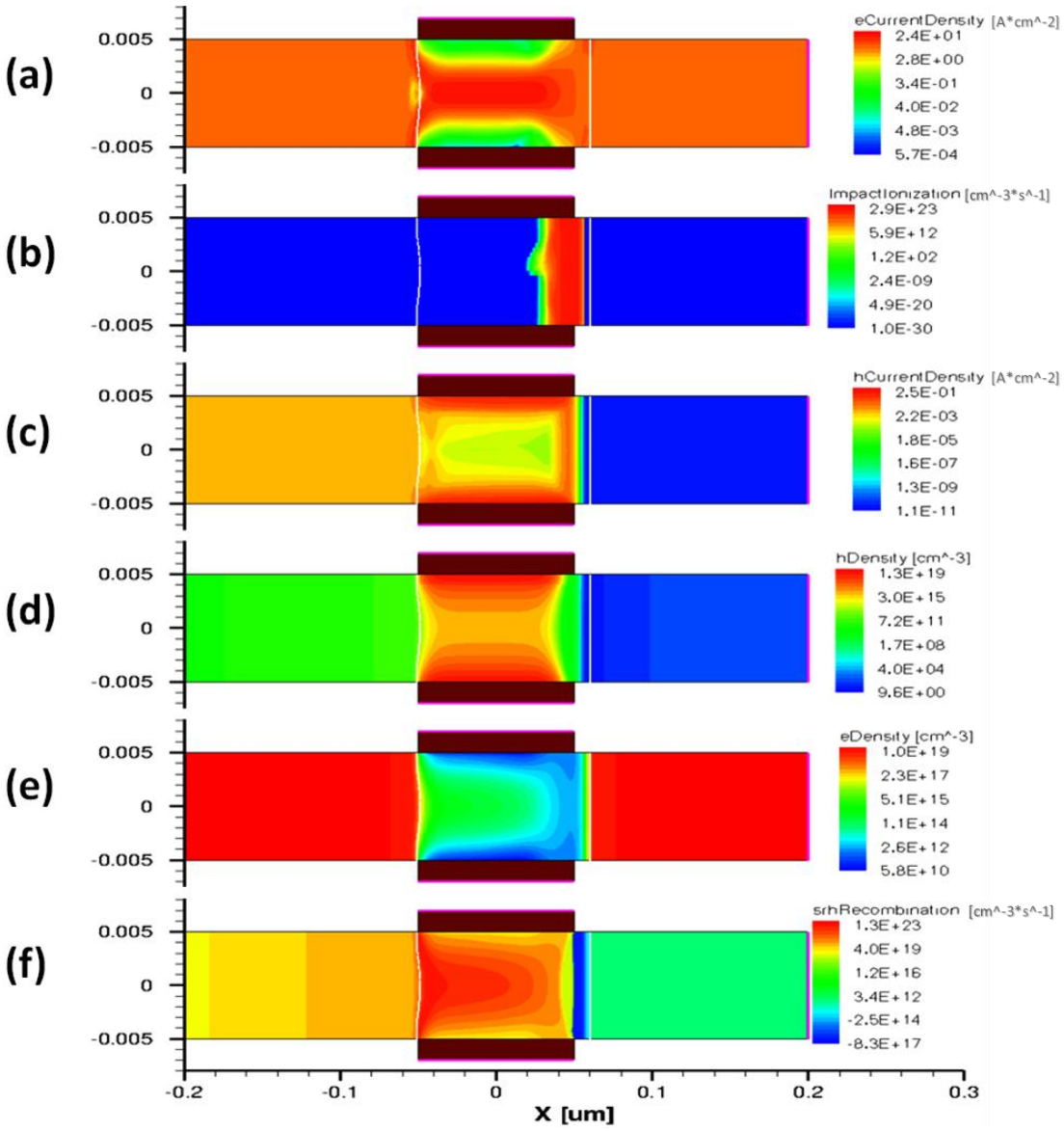


Figure 2.13: 2-D double gate junctionless device (T_{Si} = 10 nm, $N_d = 1\times10^{19}$ cm^{-3} , T_{ox} = 2 nm, L_{GATE} = 100 nm at V_G = 0.386 V, V_D = 2 V.) simulation of (a) electron current density, (b) impact ionization rate, (c) hole current density, (d) hole density, (e) electron density and (f) SRH recombination rate.

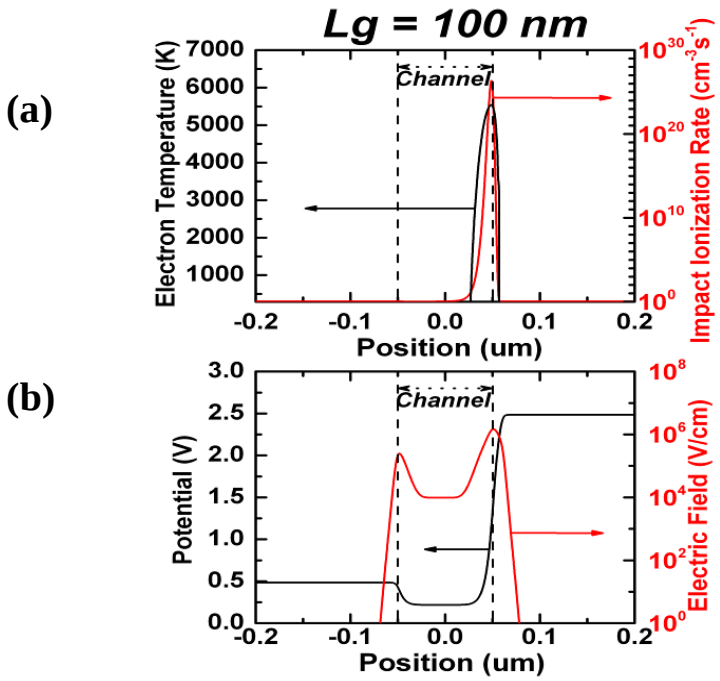


Figure 2.14: L_{GATE}= 100 nm, V_G = 0.386 V, V_D = 2 V. Along the channel: (a) Electron Temperature and Impact Ionization Generation. (b) Potential and Electric Field

Figure 2.15 presents the simulated I_D-V_G characteristics of the JNT with 32 nm and 65 nm gate length for various V_D. Above certain drain voltage, an increase of subthreshold current is observed for both gate length. It can be noticed that the increase of subthreshold current is more pronounced and occurs at lower voltage in JNT with gate length of 32 nm.

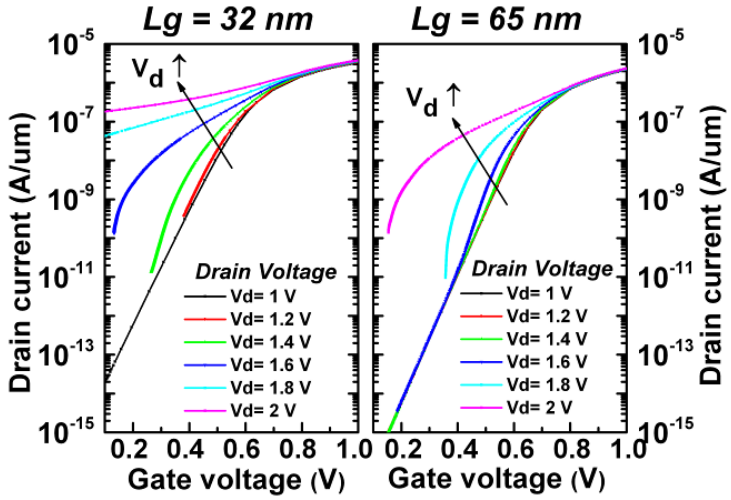


Figure 2.15: Drain current vs. gate voltage for a drain voltage from 1 V to 2 V with a step of 0.2 V. L_{GATE} = 32 nm and 65 nm.

For JNT with gate length of 65 nm, 2 V drain voltage is required for significant impact ionization effect while it can be reduced to 1.6 V for gate length of 32 nm. The subthreshold slope is extracted in Figure 2.16 and it shows for gate length of 65 nm, sub-60 mV/dec values are observed from 1.6 V and above. For gate length of 32 nm, similar curves are found from 1.4 V which confirms the previous observation.

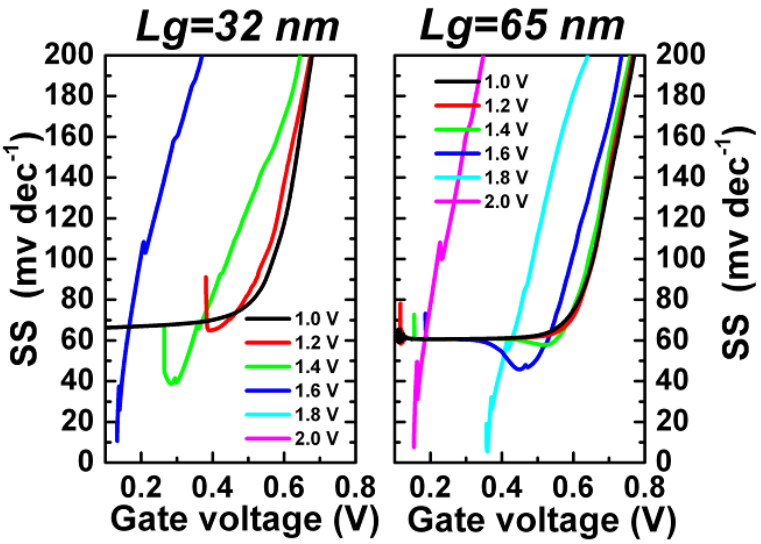


Figure 2.16: Subthreshold slope vs. gate voltage for a drain voltage from 1 V to 2 V with a step of 0.2 V. L_{GATE} = 32 nm and 65 nm

The origin of the more pronounced impact ionization effect in short channel JNT, than that in IM device, is still not clear. Possibly this effect can be related to higher subthreshold current and larger electric field according to formulae of impact ionization current. A higher subthreshold current offers more carriers which can scatter with the crystal structure and trigger more impact ionization. On the other side, a larger electric field can accelerate carriers into higher energy which increases the generation rate of impact ionization. Additionally, the bulk conduction mechanism could offer larger area to integrate the impact ionization currents. In order to completely switch off the device, the leakage current of short channel JNT has to be controlled under certain level without triggering the impact ionization effect. Further analysis has been discussed with measurement data in the next chapter.

2.5 Device Design and Estimated Performance for P-type Junctionless Transistors on Bulk Germanium Substrates

For the last 50 years, MOSFETs based on Si substrates have been improved through physical dimensions and as well as increased switching speed, according to Moore's law. As we approach 10-nanometer channel length, a number of critical challenges need to be addressed. These challenges include reducing short channel effects (SCEs), delivering higher on-current and reducing power consumption [14, 15]. A series of improvement techniques, called technology boosters, have been introduced by the industry. These include the use of high-*k* gate dielectrics and metal gate electrodes for suppressing direct tunneling current through gate oxides, mobility enhancement using strain, and the development of multi-gate gate structure for suppressing SCEs. Alternative channel materials, such as Ge and III-V compounds are being considered as well [16].

To date all the published non-silicon junctionless transistors were realized on semiconductor-on-insulator materials [17, 18]. The idea of a bulk version of the JNT needs to be further explored and compared to the semiconductor-on-insulator approach. In terms of channel material, it becomes important to look at novel higher-mobility channel materials such as Ge for pMOS. Belonging to the same group in the periodic table as Si, Ge offers attractive physical properties over Si. In Ge, the lower transport mass (m*) of electron and hole is responsible for higher electron and hole mobilities. The JNT architecture is particularly well suited to germanium because a large part of the current transport is in the bulk of the semiconductor, thereby reducing the impact of imperfect semiconductor-insulator interfaces on electric characteristics.

Concerning the fabrication of Ge MOSFETs, there are several significant challenges. The native GeO_2 is either water soluble or volatile which means that the formation of a high-quality gate dielectric is challenging [19]. Smaller direct band gap gives rise to high tunneling leakage [20, 21]. It is also difficult to make low-resistance contacts on n-type Ge substrates [22]. Inversion-mode (IM) MOSFETs exhibit high sensitivity to the quality of the gate dielectric. Moreover, both industry and academic data show rapid degradation in mobility with decreasing equivalent oxide thickness (EOT) in Ge MOSFETs and this issue exists even if a high-*k* dielectric is used [23]. The JNT, on the

other hand, is expected to be less sensitive to the interface imperfections due to its bulk conduction mechanism and reduced vertical electric field [7]. As the need for forming PN junctions is eliminated in a JNT, junction leakage current that related to the abrupt junction in scaled transistors possibly can be suppressed. Ideally MOSFETs fabricated on Germanium-on-insulator (GeOI) substrate have no leakage current flowing to the substrate. As a result, significant research efforts were made to fabricate GeOI wafers. Nakaharai *et. al.* reported 7-nm-thick strained GeOI made using a Ge-condensation technique [24]. Another approach applies the Smart-Cut method used for making silicon-on-insulator (SOI) substrates to fabricate GeOI wafers [25, 26]. However, fabrication of ultra-thin Ge layers is difficult, which motivates our study of the design of a JNT on bulk-like Ge wafer. In this section, the electrical performances of devices with various geometry and doping concentrations are investigated and proposed as a guideline to fabricate p-type Ge bulk JNTs.

2.5.1 Device Operation and Simulation Set-up

The Ge bulk JNT structure is depicted schematically in Figure 2.17. A narrow p-type "channel layer" is formed on top of n-type substrate. In terms of fabrication, the thickness of this layer can be precisely controlled by Ge epitaxial growth and the width of the fin can be controlled by advanced nanoscale lithography and etch processes.

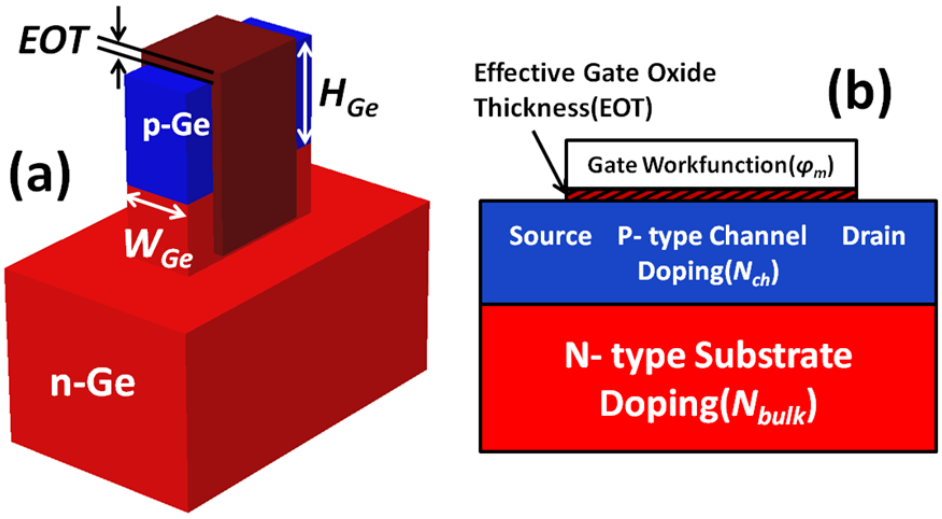


Figure 2.17: Schematic representation for (a) the multi-gate Ge JNT on a bulk substrate, and (b) a cross-section taken along the channel.

The gate dielectric wraps around the channel layer and extends down to the substrate for efficient coupling of electric field to control the bottom of channel. To approach comparable characteristics of JNT on GeOI, the leakage current from the substrate has to be eliminated. A PN junction between the heavily doped channel and the counter doped substrate is used to confine the current path in the channel. In this paper, three-dimensional simulations of the Ge JNT were carried out on the Sentaurus 3-D device simulator [1]. The detailed configurations of the bulk Ge JNT are listed in Table 2.2.

Symbol	PARAMETER	Value
W_{Ge}	fin width	8 nm to 70 nm
H_{Ge}	fin height	5 nm to 70 nm
N_{ch}	channel doping	5×10^{18} cm^{-3} to 5×10^{19} cm^{-3} (Boron)
N_{sub}	substrate doping	1×10^{15} cm^{-3} to 5×10^{19} cm^{-3} (Arsenic)
T_{ox}	effective oxide thickness	1 nm to 3 nm
L_{GATE}	gate length	5 nm to 70 nm
Φ_m	workfunction	3.5 eV to 5.1 eV

Table 2.2: Device parameters of JNT on bulk Ge substrate.

Based on available experimental data of Ge, Hellings *et. al.* have adapted the parameters of some important physical models for this commercial TCAD device simulator including model parameters for generation/recombination mechanisms (Shockley-Read-Hall (SRH), Trap-Assisted-Tunneling (TAT), and Band to Band Tunneling (BTBT)), mobility models, and Interface traps [27]. In this work, we implement a similar modeling methodology and parameter set as that reported. The SRH model used includes doping dependent and field enhancement models. The mobility model used includes doping dependence, transverse-field dependence and surface roughness dependence models. BTBT model and interface traps are not considered in the simulation.

2.5.2 Results and Discussions

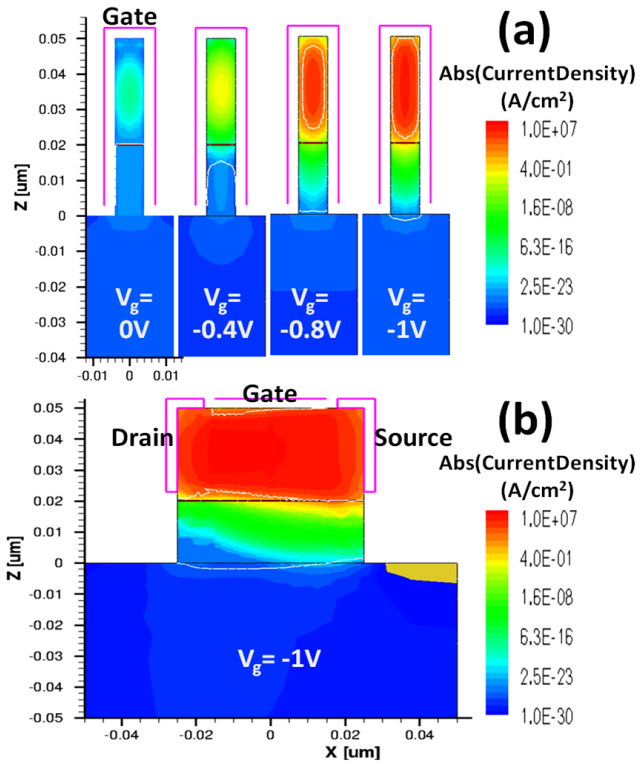


Figure 2.18: N_{ch}= 1×10^{19} cm^{-3}, N_{sub}= 1×10^{18} cm^{-3}, EOT = 2 nm, Φ_m = 4.1 eV (a) Current density in the vertical direction of the device taken in the middle of the channel for V_G= 0 V, V_G= -0.4 V, V_G= -0.8 V, V_G= -1 V, respectively, when V_D= -1V. (b) Current density along the channel for V_G= -1 V when V_D= -1V.

Figure 2.18(a) illustrates how the current density evolves in middle of the channel as gate voltage (V_G) equals to 0 V, -0.4 V, -0.8 V, and -1 V, respectively. The white solid lines indicate the edges of depletion regions. The result shows that as the gate becomes negative, the current starts to flow in the middle of the p-type Ge layer and the depletion layer is extended into the n-type Ge layer. Figure 2.18(b) shows the current density along the channel when the device is completely turned on. When the transistor is turned on, the holes are collected by the drain and an effective confinement of current can be observed. A potential barrier is formed in the substrate by the PN junction that isolates the channel to substrate. In the off-state, along the channel direction, another potential barrier is induced by the gate due to the difference of work-function which blocks the holes flowing to the drain. In the on-state, the potential barrier created by the gate is lowered and current is allowed to flow and to increase with the applied V_G.

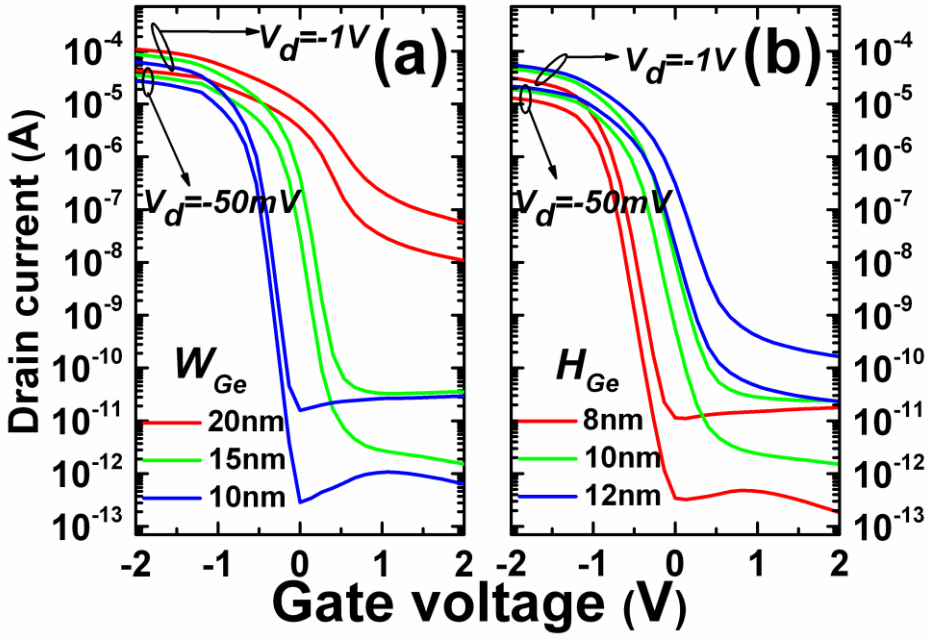


Figure 2.19: I_D-V_G characteristics of the linear (V_D= -50 mV) and saturation (V_D= -1V) region for devices with parameters of (a) W_{Ge}= 10, 15, 20 nm, H_{Ge}= 50 nm, L_{GATE} = 30 nm, EOT= 2 nm, N_{ch}= 1×10^{19} cm^{-3}, N_{sub}= 1×10^{18} cm^{-3} , Φ_m = 3.5eV (b) W_{Ge}= 50 nm, H_{Ge}= 8, 10, 12 nm, L_{GATE} = 30 nm, EOT= 2 nm, N_{ch}= 1×10^{19} cm^{-3}, N_{sub}= 1×10^{18} cm^{-3}, Φ_m = 3.5 eV

An important parameter in multi-gate FET design is the semiconductor height-to-width aspect ratio. Figure 2.19(a) shows the drain current vs. gate voltage (I_D-V_G) curves of 30 nm gate length JNTs with fin height of 50 nm and fin widths of 10 nm, 15 nm and 20 nm, respectively. One can see the electrical characteristics degrade rapidly as the fin width increases: both the subthreshold slope and the off current increase. The leakage current dramatically increases as the fin width reaches 20 nm. Figure 2.19 (b) shows the I_D-V_G curves of 30 nm gate length JNTs with a fin width of 50 nm and fin heights of 8 nm, 10 nm and 12 nm, respectively. It shows as the fin height increases, the electrical characteristics also degrade. Generally speaking the use of a thinner and narrower cross-section provides better device characteristics, although it can lead to process variability issues. As the value of the subthreshold slope directly reflects the efficiency of gate control on the channel.

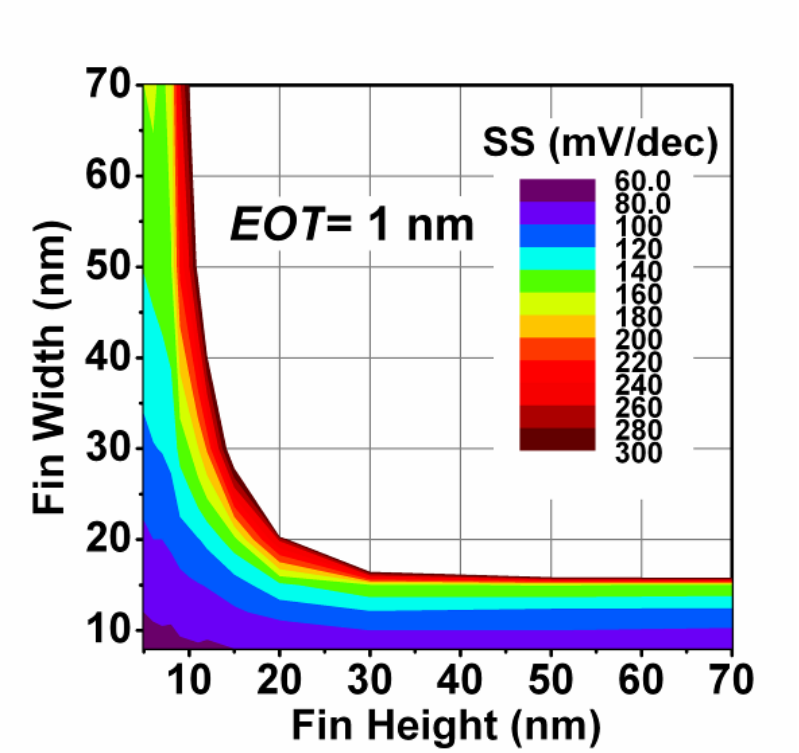


Figure 2.20: A contour map of *SS* values for various fin width and height for JNTs (L_{GATE} = 30 nm, *EOT* = 1 nm, N_{ch} = 1×10^{19} cm^{-3}, N_{sub}= 1×10^{18} cm^{-3}, Φ_m = 4.1 eV).

Unlike the threshold voltage the *SS* cannot be tuned by modifying the gate electrode work-function. It is thus very important to investigate the dependence of the *SS* value on different device geometry to optimize bulk Ge JNTs. Figure 2.20 shows a contour map of *SS* values plotted as a function of fin width and height for JNTs with L_{GATE} = 30 nm, T_{ox} = 1 nm, N_{ch} = 1×10^{19} cm^{-3}, N_{sub}= 1×10^{18} cm^{-3} and Φ_m = 4.1 eV. Contours are plotted for *SS* values up to 300 mV/dec with a step of 20 mV/dec. It can be observed that to achieve reasonable *SS* values either thin thickness or narrow fin width is required. *SS* value closes to the theoretical limit of 60 mV/dec can be obtained for the cross-section of 10 nm by 10 nm. Fin widths close to 10 nm can achieve *SS* values of 80 mV/dec to 100 mV/dec regardless of the fin heights. This indicates that the fin width and fin thickness have a different influence on the device characteristics. Like in silicon devices, double-gate gate control can be achieved from sidewalls for high-aspect-ratio structures, while only single-gate control is achieved when using a thinner but wider fin. Nevertheless, these results indicate that the electrical characteristics of JNT are sensitive to the minimum dimension of the fin (fin width or fin height).

Higher leakage currents are usually observed in Ge MOSFETs than that in silicon devices [28]. This higher leakage current is relating to the generation/recombination processes in the smaller bandgap of Ge (E_g = 0.66 eV). To accurately represent the leakage current, the doping dependent SRH and TAT (Hurkx) models are used [29].

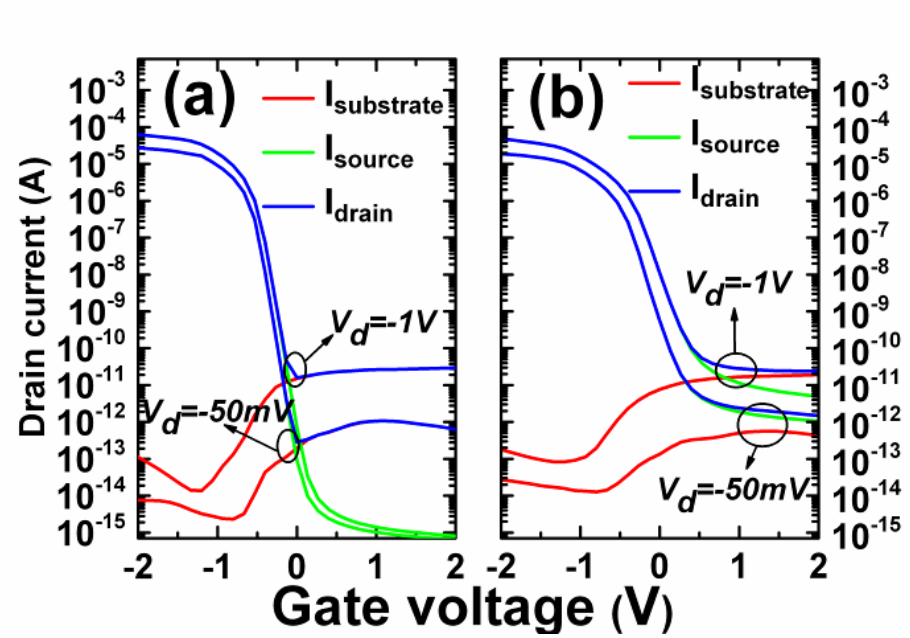


Figure 2.21: Source, drain and substrate current vs. gate voltage of the linear (V_D= -50 mV) and saturation (V_D= -1V) region for devices with parameters of (a) W_{Ge}= 10 nm, H_{Ge}= 50 nm, L_{GATE} = 30 nm, EOT= 2 nm, N_{ch}= 1×10^{19} cm^{-3}, N_{sub}= 1×10^{18} cm^{-3}, Φ_m = 3.5eV (b) W_{Ge}= 50 nm, H_{Ge}= 10 nm, L_{GATE} = 30 nm, EOT= 2 nm, N_{ch}= 1×10^{19} cm^{-3}, N_{sub}= 1×10^{18} cm^{-3}, Φ_m = 3.5 eV

The source, drain and substrate currents are shown for both high-aspect-ratio and low-aspect-ratio JNTs in Figure 2.21. It is noticed that for the high-aspect-ratio JNT (W_{Ge}= 10 nm, H_{Ge}= 50 nm, L_{GATE} = 30 nm, EOT= 2 nm, N_{ch}= 1×10^{19} cm^{-3}, N_{sub}= 1×10^{18} cm^{-3}) in Figure 2.21(a), the drain leakage current is identical to the substrate current in the off-state. The source leakage current is much less than the drain leakage current that indicates the leakage path is from the drain to the substrate and not from source to drain. For the low-aspect-ratio JNT (W_{Ge}= 50 nm, H_{Ge}= 10 nm, L_{GATE} = 30 nm, EOT= 2 nm, N_{ch}= 1×10^{19} cm^{-3}, N_{sub}= 1×10^{18} cm^{-3}) in Figure 2.21, the source current is much closer to the drain current. This larger source-to drain leakage is due to a worse gate control over the channel. In both cases, the substrate current becomes negligible when the transistor is turned on. This can be explained as follows: when current flows in the channel, the potential between the channel and the substrate decreases, which reduces the average amount of voltage applied to the reverse-biased channel-to-substrate junction and, therefore, reduces the substrate leakage current.

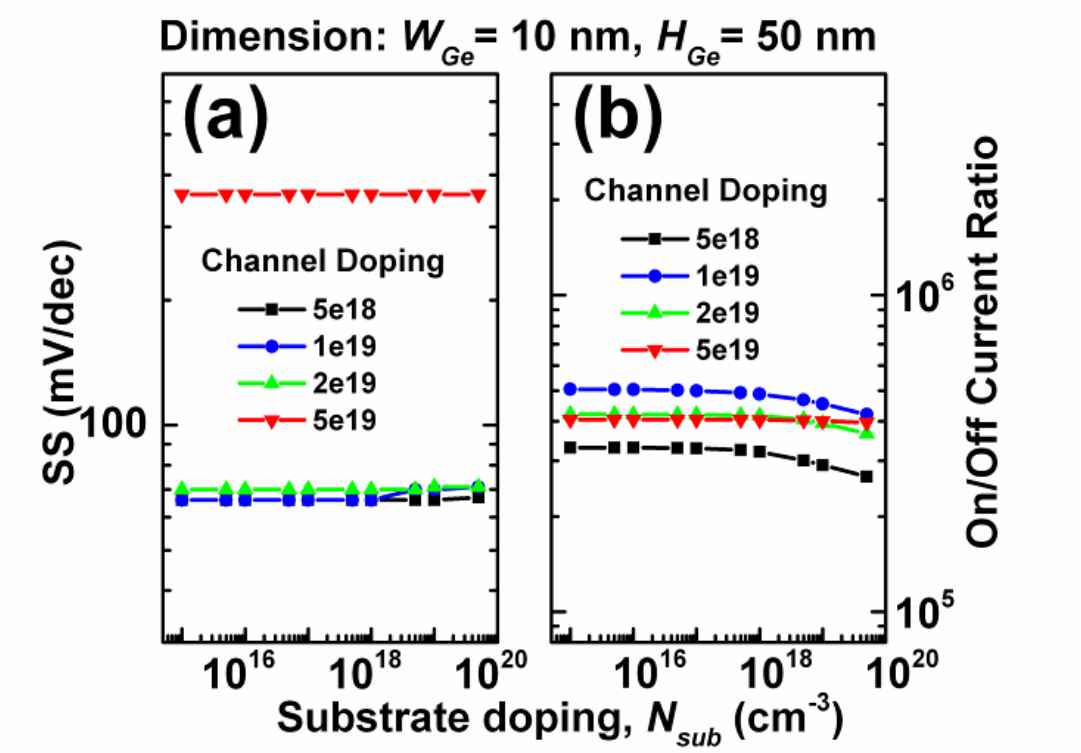


Figure 2.22: *SS* values and the I_{ON}/I_{OFF} current ratio for different substrate and channel doping concentrations for high-aspect-ratio device (W_{Ge}= 10 nm, H_{Ge}= 50 nm, L_{GATE} = 30 nm, T_{ox} = 2 nm).

The selection of appropriate mobility models is important for accurately evaluating the current. Here we considered mainly four mobility limiting factors: phonon scattering, impurity scatting, velocity saturation, and acoustic phonon/surface roughness scattering. The Masetti model is used to describe the doping-dependent mobility degradation effect [30]. Under high electric fields, the carrier drift velocity is no longer proportional to the electric field. Instead, the velocity saturates to a finite speed V_{sat}. Here the Canili model is utilized and the V_{sat} is set as 6×10^6 cm/s for both electron and holes [31]. In order to evaluate the influence of different channel and substrate doping concentrations on the device performance, both high-aspect-ratio (W_{Ge}= 10 nm, H_{Ge}= 50 nm, L_{GATE} = 30 nm, *EOT*= 2 nm) and low-aspect-ratio (W_{Ge}= 50 nm, H_{Ge}= 10 nm, L_{GATE} = 30 nm, *EOT*= 2 nm) devices were simulated. Figure 2.22 and Figure 2.23 show the *SS* values for different substrate and channel doping concentrations and for different aspect ratio values.

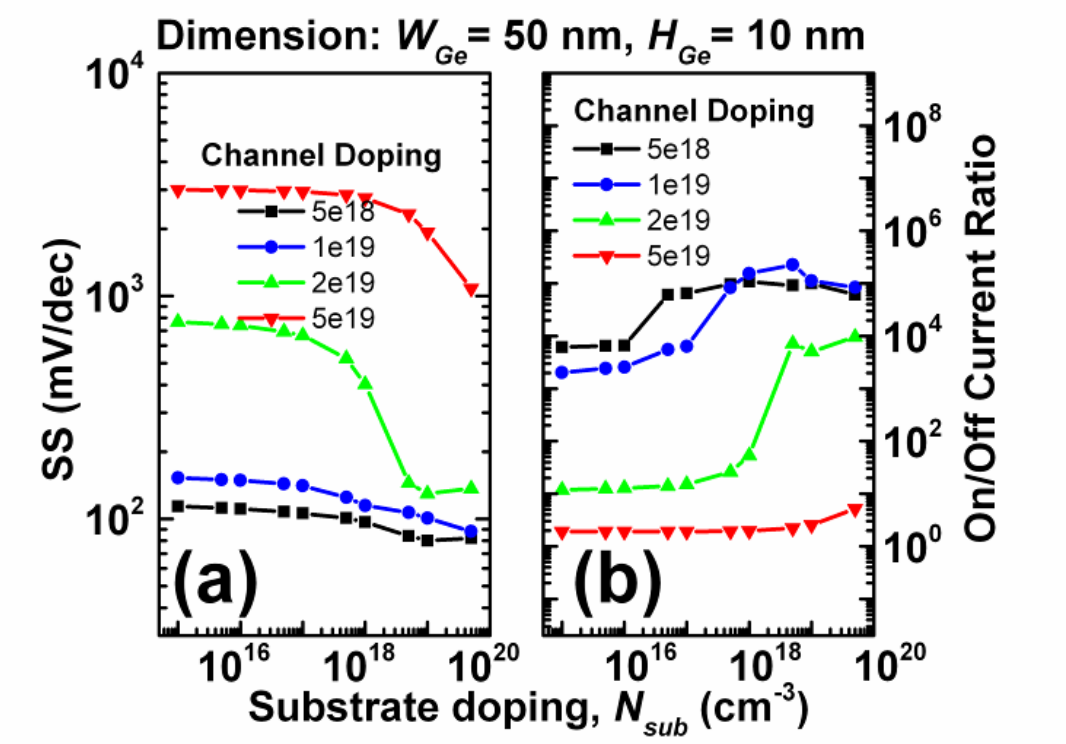


Figure 2.23: (a) *SS* values and (b) the I_{ON}/I_{OFF} current ratio for different substrate and channel doping concentrations for low-aspect-ratio device (W_{Ge}= 50 nm, H_{Ge}= 10 nm, L_{GATE} = 30 nm, T_{ox} = 2 nm).

SS values are extracted from the reciprocal of the steepest slope to the curve of the $log(I_D)$ vs. V_G. The I_{ON}/I_{OFF} current ratios are calculated after normalizing the I_{OFF} for V_G = 0 V and applying the same gate bias as -1 V. The results show that the lower-aspect-ratio devices exhibit more variability with substrate doping concentration in the terms of *SS* values and the I_{ON}/I_{OFF} current ratio. This can be explained as follows: In the JNT with low-aspect-ratio, the depletion layer in the channel formed by the counter-doped substrate constitutes a larger portion of the channel thickness than that in the high-aspect-ratio JNT. Figure 2.22 shows that the substrate doping does not affect the *SS* values and the I_{ON}/I_{OFF} current ratio much in the high-aspect-ratio JNT. In the low-aspect-ratio JNT, on the other hand, the *SS* and the I_{ON}/I_{OFF} current ratio are dramatically improved by using higher substrate doping concentrations. As far as the channel doping is concerned, Figure 2.22 and Figure 2.23 show that the use of lower channel doping concentrations results in a better gate control, improving *SS* value in both high- and low-aspect-ratio JNTs. Taking other factors into account (*i.e:* accounting for source and drain resistance, conductance of the channel and mobility dependence on doping concentration), the I_{ON}/I_{OFF} current ratio reaches a maximum value for channel

doping around 1×10^{19} cm^{-3} for the high-aspect-ratio case in this work. As the cross-section of the fin decreases, the optimum channel doping can be higher, and since high carrier density can be produced, higher I_{ON} is generated. However, it is a trade-off among the carrier density, gate control and mobility degradation for the highly doped channel. Generally, if channel doping concentration more than 5×10^{19} cm^{-3} is used, the I_{ON}/I_{OFF} current ratio decreases because higher doping degrades mobility. Furthermore switch characteristics and leakage current degrade due to loss of gate control. For the low-aspect-ratio JNT, as the electrostatic control from the sidewalls is limited, lower channel doping results in a better gate control. Higher substrate doping forms a thicker depletion layer in the channel which tends to suppress leakage currents.

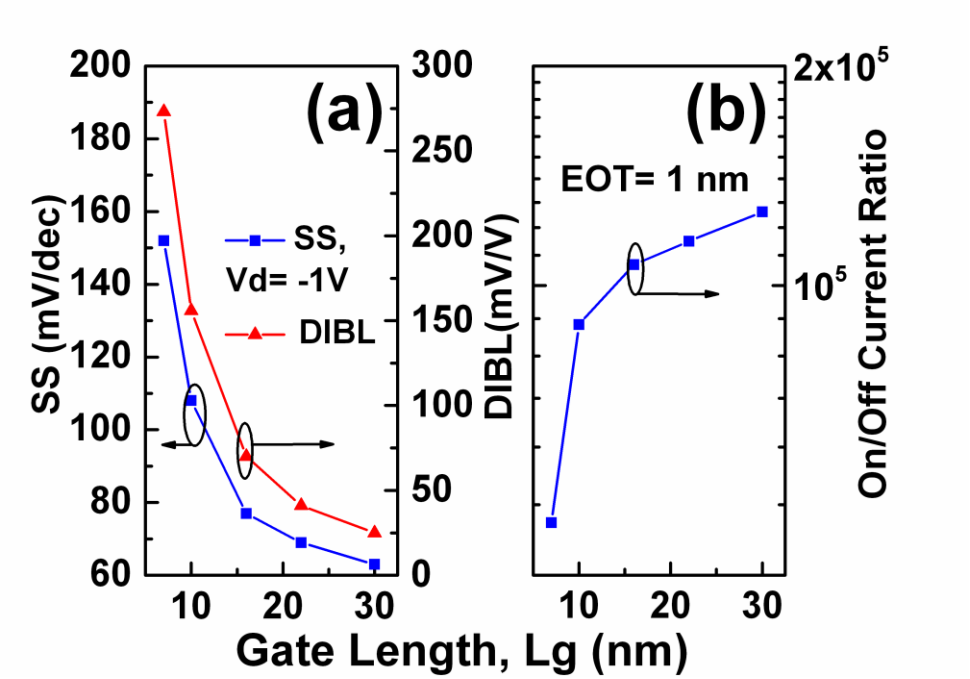


Figure 2.24: (a) *SS* values, *DIBL* and (b) the I_{ON}/I_{OFF} current ratio for devices with various gate length from 30 nm down to 7nm (W_{Ge}= 10 nm, H_{Ge}= 10 nm, *EOT*= 1 nm, N_{ch}= 1×10^{19} cm^{-3}, N_{sub}= 1×10^{18} cm^{-3}).

Figure 2.24 shows the scaling performance of the Ge bulk JNT for channel lengths ranging from 30 nm down to 7 nm. As the channel length is scaled below 16 nm, the gate electrostatics control degrades, resulting in a drastic increase of leakage current. For gate lengths below 16 nm, the *SS* and *DIBL* are larger than 80 mV/dec and 100mV/V, respectively, and the I_{ON}/I_{OFF} current ratio becomes smaller than 1×10^{5}. However, the gate electrostatics control can be further improved by adjusting the channel or the substrate doping.

Same as the Si JNT, the Ge bulk JNT exhibits inherent SCEs immunity and shows better gate control than the Ge IM transistor, in terms of *DIBL* and *SS* characteristics. Theoretically the mobility degradation due to the doping is more in the JNT than that in the IM transistor resulting in less I_{ON}. However, the Ge IM transistor shows serious degradation in mobility with decreasing electrical oxide thickness due to its imperfect interface condition [23]. The I_{ON} of Ge bulk JNT is less affected by the quality of the gate dielectric due to its bulk conduction mechanism and reduced vertical electric field. Thus, overall the Ge bulk JNT exhibits a better gate control, easier process and a competitive I_{ON} comparing with Ge IM transistor. For JNT when the Si channel is replaced by Ge, the gate control degrades slightly due to 35% larger dielectric constant of Ge than that of Si. Moreover, due to the small bandgap, the leakage current increases as well for Ge. However, inherently the larger mobility of Ge offers higher I_{ON} than that of Si which is critical for decreasing the gate delay. The drawbacks can significantly be reduced as supply voltage scaled close to the bandgap of Ge and carefully designed structure of transistor as well.

As technology boosters can be used and the pitch of nanowire transistor decreases continuously, the Ge bulk JNT transistor shows its potential for both high performance (HP) and low operating power (LOP) logic technology node for year 2016 with an I_{ON}/I_{OFF} current ratio around 1×10^5. As scaling of the supply voltage closer to 0.67 V, the I_{ON}/I_{OFF} current ratio further increases due to the reduction of the leakage current in Ge bulk JNT. Thus, with its inherent material properties and novel concept of transistor, Ge bulk JNT is very promising to outperform Si transistor in the future technology node.

2.5.3 Summary and Conclusion

Simulations of bulk Ge p-type JLTs demonstrate typical MOSFET characteristics. It shows that by adjusting the doping concentration in the channel and substrate, it is possible to suppress the subthreshold leakage current and confines saturation current to the channel fin. Device performance was evaluated for various geometry and doping conditions. Comparing high-aspect-ratio and low-aspect-ratio bulk Ge JNTs with same cross-sectional area, we found that high-aspect-ratio structures yield better device performance due to better electrostatic coupling between gate and channel. Moreover, in

the low aspect ratio case higher substrate doping concentrations is needed which may lead to a higher BTBT leakage. In general smaller cross-section of the bulk Ge JNT results in a better electrostatic gate control and an appropriate channel doping can be found between 5×10^{18} and 5×10^{19} cm^{-3} which gives a high I_{ON}/I_{OFF} current ratio.

2.6 Conclusions

In this chapter, the simulations are carried out using the Technology Computer-Aided Design (TCAD) software, in order to compare the Junctionless transistors (JNT) with the Inversion Mode (IM) devices, in terms of gate control, vertical electric field and capacitances. The unique conduction mechanism and electrical characteristics for JNT have been discussed. In order to scale the V_{DD}, lower *SS* value (sub-60 mV/dec at room temperature) in JNT has been obtained by simulation. The dependence of the effect on gate length is investigated and their influence on the I_D-V_G curves is discussed. For future current enhancement, simulation of JNTs with high mobility Ge channel was performed.

2.7 References

[1] http://www.synopsys.com/Tools/TCAD.

[2] http://www.silvaco.com/products/tcad.

[3] Colinge J-P, Lee C-W, Afzalian A, Akhavan ND, Yan R, Ferain I, et al. Nanowire transistors without junctions. Nat Nanotechnol. 2010;5:225-9.

[4] Kranti A, Yan R, Lee C-W, Ferain I, Yu R, Akhavan ND, et al. Junctionless nanowire transistor (JNT): Properties and design guidelines. Solid-State Device Research Conference (ESSDERC), 2010 Proceedings of the European: IEEE; 2010. p. 357-60.

[5] Lee C-W, Afzalian A, Akhavan ND, Yan R, Ferain I, Colinge J-P. Junctionless multigate field-effect transistor. Appl Phys Lett. 2009;94:053511--2.

[6] Lee C-W, Ferain I, Afzalian A, Yan R, Akhavan ND, Razavi P, et al. Performance estimation of junctionless multigate transistors. Solid State Electron. 2010;54:97-103.

[7] Colinge J-P, Lee C-W, Ferain I, Akhavan ND, Yan R, Razavi P, et al. Reduced electric field in junctionless transistors. Appl Phys Lett. 2010;96:073510--3.

[8] Colinge J, Kranti A, Yan R, Lee C, Ferain I, Yu R, et al. Junctionless nanowire transistor (JNT): Properties and design guidelines. Solid State Electron. 2011;65:33-7.

[9] Choi S-J, Moon D-I, Kim S, Duarte JP, Choi Y-K. Sensitivity of threshold voltage to nanowire width variation in junctionless transistors. Electron Device Letters, IEEE. 2011;32:125-7.

[10] Raskin J-P, Colinge J-P, Ferain I, Kranti A, Lee C-W, Akhavan ND, et al. Mobility improvement in nanowire junctionless transistors by uniaxial strain. Appl Phys Lett. 2010;97:042114--3.

[11] Cros A, Romanjek K, Fleury D, Harrison S, Cerutti R, Coronel P, et al. Unexpected mobility degradation for very short devices: A new challenge for CMOS scaling. Electron Devices Meeting, 2006 IEDM'06 International: IEEE; 2006. p. 1-4.

[12] Zhang Q, Zhao W, Seabaugh A. Low-subthreshold-swing tunnel transistors. Electron Device Letters, IEEE. 2006;27:297-300.

[13] Davis J, Glaccum A, Reeson K, Hemment P. Improved subthreshold characteristics of n-channel SOI transistors. Electron Device Letters, IEEE. 1986;7:570-2.

[14] Kuhn KJ. Moore's crystal ball: Device physics and technology past the 15nm generation. Microelectron Eng. 2011;88:1044-9.

[15] Hu C. Device challenges and opportunities. VLSI Technology, 2004 Digest of Technical Papers 2004 Symposium on: IEEE; 2004. p. 4-5.

[16] Takagi S, Tezuka T, Irisawa T, Nakaharai S, Numata T, Usuda K, et al. Device structures and carrier transport properties of advanced CMOS using high mobility channels. Solid State Electron. 2007;51:526-36.

[17] Yokoyama M, Iida R, Kim S, Taoka N, Urabe Y, Yasuda T, et al. Extremely-thin-body InGaAs-on-insulator MOSFETs on Si fabricated by direct wafer bonding. Electron Devices Meeting (IEDM), 2010 IEEE International: IEEE; 2010. p. 3.1. -3.1. 4.

[18] Zhao DD, Nishimura T, Lee CH, Nagashio K, Kita K, Toriumi A. Junctionless Ge p-channel metal–oxide–semiconductor field-effect transistors fabricated on ultrathin Ge-on-insulator substrate. Applied physics express. 2011;4:031302.

[19] Saraswat KC, Chui CO, Krishnamohan T, Nayfeh A, McIntyre P. Ge based high performance nanoscale MOSFETs. Microelectron Eng. 2005;80:15-21.

[20] Mitard J, De Jaeger B, Leys F, Hellings G, Martens K, Eneman G, et al. Record I_{ON}/I_{OFF} performance for 65nm Ge pMOSFET and novel Si passivation scheme for improved EOT scalability. Electron Devices Meeting, 2008 IEDM 2008 IEEE International: IEEE; 2008. p. 1-4.

[21] Hutin L, Le Royer C, Damlencourt J-F, Hartmann J-M, Grampeix H, Mazzocchi V, et al. GeOI pMOSFETs scaled down to 30-nm gate length with record off-state current. Electron Device Letters, IEEE. 2010;31:234-6.

[22] Shayesteh M, Daunt CLM, O'Connell D, Djara V, White M, Long B, et al. NiGe contacts and junction architectures for P and As doped germanium devices. Electron Devices, IEEE Transactions on. 2011;58:3801-7.

[23] Kuhn KJ, Murthy A, Kotlyar R, Kuhn M. (Invited) Past, Present and Future: SiGe and CMOS Transistor Scaling. ECS Transactions. 2010;33:3-17.

[24] Nakaharai S, Tezuka T, Sugiyama N, Moriyama Y, Takagi S-i. Characterization of 7-nm-thick strained Ge-on-insulator layer fabricated by Ge-condensation technique. Appl Phys Lett. 2003;83:3516-8.

[25] Nguyen Q, Damlencourt J, Vincent B, Clavelier L, Morand Y, Gentil P, et al. High quality Germanium-On-Insulator wafers with excellent hole mobility. Solid State Electron. 2007;51:1172-9.

[26] Yu R, Byun KY, Ferain I, Angot D, Morrison R, Colinge C. Fabrication of Germanium-on-Insulator by low temperature direct wafer bonding. Solid-State and

Integrated Circuit Technology (ICSICT), 2010 10th IEEE International Conference on: IEEE; 2010. p. 953-5.

[27] Hellings G, Eneman G, Krom R, De Jaeger B, Mitard J, De Keersgieter A, et al. Electrical TCAD simulations of a germanium pMOSFET technology. Electron Devices, IEEE Transactions on. 2010;57:2539-46.

[28] Brunco D, De Jaeger B, Eneman G, Mitard J, Hellings G, Satta A, et al. Germanium MOSFET devices: Advances in materials understanding, process development, and electrical performance. J Electrochem Soc. 2008;155:H552-H61.

[29] Hurkx G, Klaassen D, Knuvers M. A new recombination model for device simulation including tunneling. Electron Devices, IEEE Transactions on. 1992;39:331-8.

[30] Masetti G, Severi M, Solmi S. Modeling of carrier mobility against carrier concentration in arsenic-, phosphorus-, and boron-doped silicon. Electron Devices, IEEE Transactions on. 1983;30:764-9.

[31] Canali C, Majni G, Minder R, Ottaviani G. Electron and hole drift velocity measurements in silicon and their empirical relation to electric field and temperature. Electron Devices, IEEE Transactions on. 1975;22:1045-7.

Chapter 3 Fabrication and Characterization of Silicon JNT

Abstract: In this chapter, the fabrication process of IM devices and JNTs down to 22 nm gate length has been discussed and characterizations have been carried out for these devices at elevated temperature and stressed conditions. Steep subthreshold slopes (*SS*) in JNT and IM devices are observed, and the influence of geometry, recombination mechanism and electric field on this effect for IM and JNTs are discussed according to the measurement and simulation results. It is observed that the floating body in JNT is relatively dynamic compared with that in IM devices and proper design of the device structure may further reduce the V_D for a sub-60 mV/dec subthreshold slope. Diode configuration of the JNT has also been evaluated, which demonstrates the first diode without junctions.

3.1 Devices Fabricated and Used in the Work

pMOS and nMOS junctionless devices were fabricated on SOI wafers from SOITEC. The long channel Si JNTs with gate length around 1 μm were fabricated in Tyndall National Institute, Cork, Ireland and the short channel devices down to 22 nm, were processed in CEA-LETI, Grenoble, France within the SQWIRE project.

3.1.1 Long Channel Si JNT

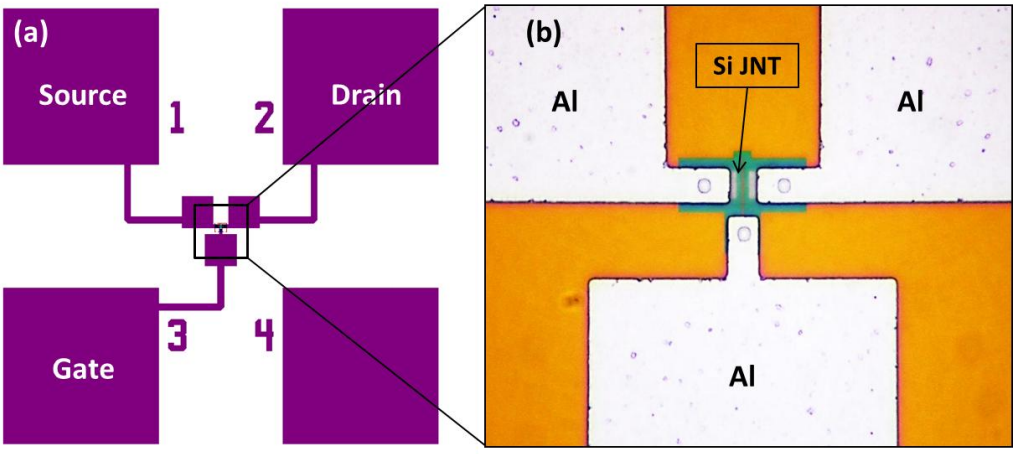


Figure 3.1: Layout and optical image of the Si JNTs. (a) S/D and gate metal electrodes. (b) Si JNT connecting to Al electrodes through contact windows.

In Figure 3.1, the schematic of the Si JNT layout has been presented. Figure 3.1(a) shows mainly the source, drain and gate metal electrode pads, which is deposited aluminium (Al). The optical image of a Si JNT has been demonstrated in Figure 3.1(b), which is connecting to the Al electrodes through contact windows.

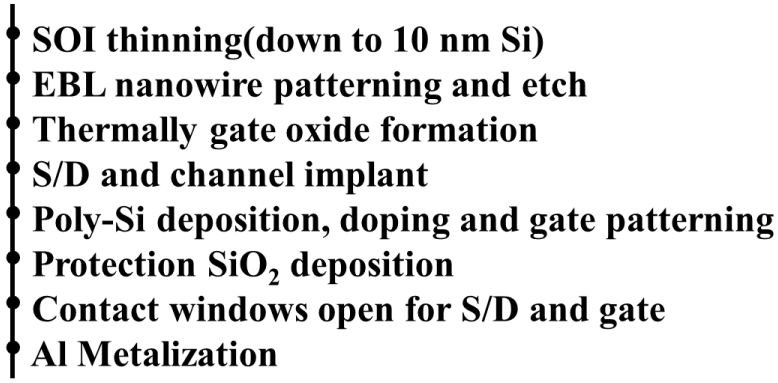


Figure 3.2: Process flow of the long channel Si JNT fabricated at Tyndall.

In Figure 3.2, the process flow of the long channel Si JNT has been presented. Starting with commercial SOI wafers (lightly p-doped, 70 nm top silicon layer and a buried oxide thickness of 145 nm), circle oxidation and wet etch have been performed to thin down the Si layer to about 10 nm. Electron-Beam Lithography(EBL) has been employed to define Si layer into nanowires (or nano-ribbons) of a few tens of nanometres wide. A 10-nm gate oxide has been grown by the dry oxidation afterwards. The nanowires were then uniformly doped by ion implantation, using arsenic to dope the n-type devices and BF_2 to dope the p-type devices. The implant energies and doses were chosen to yield uniform doping concentrations ranging from of 5×10^{18} to 5×10^{19} atoms cm^{-3} in different wafers, according to simulation results. Such high doping levels are traditionally reserved for source and drain extension formation in CMOS devices. The gate was formed by deposition of a 50-nm-thick layer of amorphous silicon at a temperature of 550 ºC in a low-pressure chemical vapour deposition (LPCVD) reactor. After heavy P or N gate doping using boron or arsenic ion implants at a dose of 2×10^{14} cm^{-2}, the samples were annealed in a nitrogen ambient at 900 ºC for 30 min to activate the doping impurities and transform the amorphous silicon gate material in polycrystalline silicon. The gate electrodes were then patterned and etched in a reactive-ion etch (RIE) reactor [1].

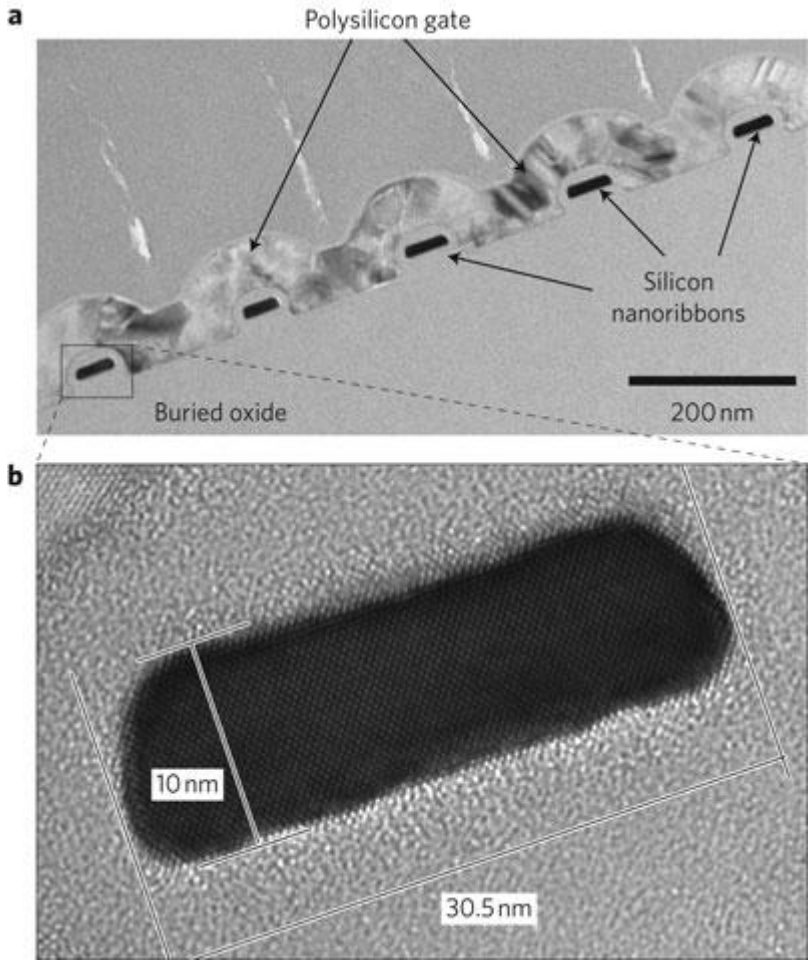


Figure 3.3: (a) Five parallel devices with a common polysilicon gate electrode. (b) Magnification of a single nanoribbon device. Individual atomic rows can be seen in the silicon [1].

Figure 3.3(a) shows a transmission electron micrograph of five parallel silicon gated resistor nanoribbons with a common polysilicon gate electrode. The magnified view of a single nanoribbon device is also shown (Figure 3.3(b)), in which individual silicon atomic rows can be observed. To obtain desirable values for the threshold voltage, a p polysilicon gate is used for the n-type device and an n polysilicon gate is used for the p-channel device. After gate patterning, a protective SiO_2 layer was deposited, contact holes were etched, and a classical TiW–aluminium metallization process was used to provide electrical contact to the devices. No doping step was performed after gate patterning, leaving the source and drain terminals with exactly the same doping type and concentration as the channel region. The device has a multigate (Tri-gate, to be more specific) configuration, which means that the gate electrode is wrapped along

three edges of the device (left, top and right sides of the nanoribbon). Classical Tri-gate FETs were fabricated on separate wafers for comparison purposes.

3.1.2 Short Channel Si JNT down to 22 nm

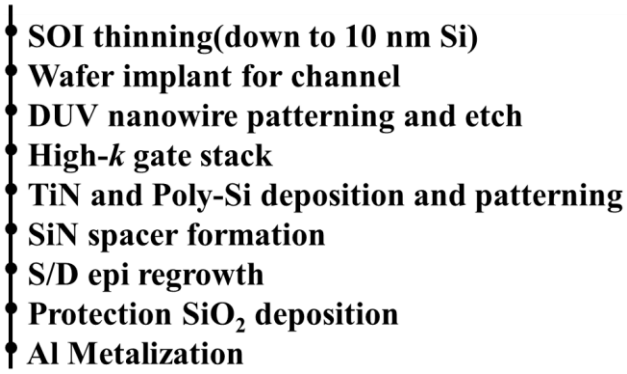


Figure 3.4: Process flow of the long channel Si JNT fabricated at CEA LETI.

Figure 3.4 shows the gate-first process flow of the short channel Si JNT down to 22 nm. Tri-gate nanowires with high-*k*/metal gate stack were fabricated on (100) SOI wafers with a 12 nm top silicon layer and a buried oxide thickness of 145 nm. The SOI layer was thinned down to 10 nm. Three doping concentrations were used for NMOS (resp., PMOS) with phospohorus (resp., boron) dose of 1.5×10^{13} cm^{-2} (resp., 3×10^{13} cm^{-2}), 1.5×10^{13} cm^{-2} (resp., 6×10^{13} cm^{-2}), and 7×10^{13} cm^{-2} (resp., 10^{14} cm^{-2}), respectively. The implant energies and doses were chosen to have uniform doping concentration ranging from 10^{19} cm^{-2}. The silicon layer is patterned to create NWs by using a Mesa isolation technique. NW patterns are defined by optical (DUV) lithography and followed by a resist trimming process. It is performed to achieve NW structure as small as 15 nm in width. The gate stack consists of 2.3 nm CVD HfSiON, 5 nm ALD TiN, and polysilicon (50 nm) layers (EOT ≈ 1.2 nm). As for the active patterning, the same photoresist trimming is used to address gate lengths down to 22 nm [2, 3].

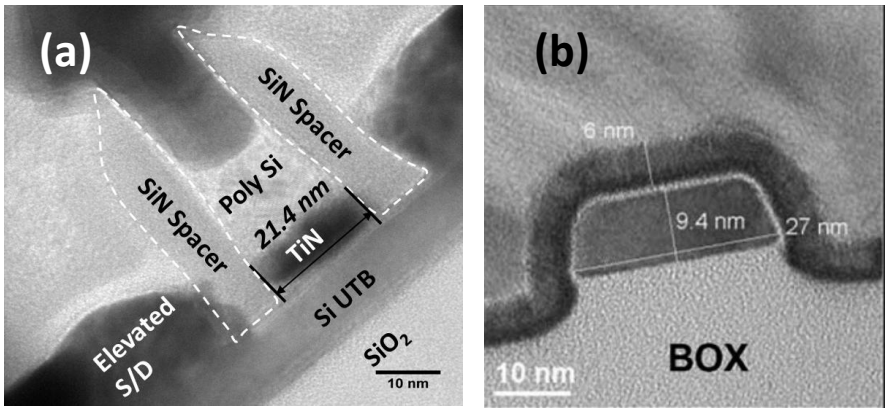


Figure 3.5: Cross-sectional TEM of trigate JNTs (a) along the fin direction and gate length as small as 22 nm are achieved (b) cross-section of the nanowire [2, 3].

HRTEM images of tri-gate NW cross section are shown in Figure 3.5. The SOI thickness, the gate lengths, and the NW widths estimated in this work result from ellopsometry measurements, SEM and TEM observations.

3.2 Devices Characterization

3.2.1 Characterization of Long Channel Si JNTs

The electrical characteristics of the JNT are proven remarkably identical to those of regular trigate MOSFETs with the first batch of devices fabricated in Tyndall. Figure 3.6 shows I_D-V_G characteristics. The device has an effective width of 25 nm and L_{GATE} = 1 um. Extrapolating using V_D = 1 V, V_{goff}= V_{th}- 0.3V and V_{gon}= V_{th}+ 0.7 V, L_{GATE} = 20 nm and a pitch of 50nm one finds that the device is capable of I_{OFF} and I_{ON} of 1 nA/μm and 1 mA/μm, respectively, without using any mobility-enhancing technique such as strain [4]. Figure 3.7 shows the experimental I_D-V_D characteristics of both p-type and n-type Si JNTs. These characteristics are strikingly similar to those of regular MOSFETs.

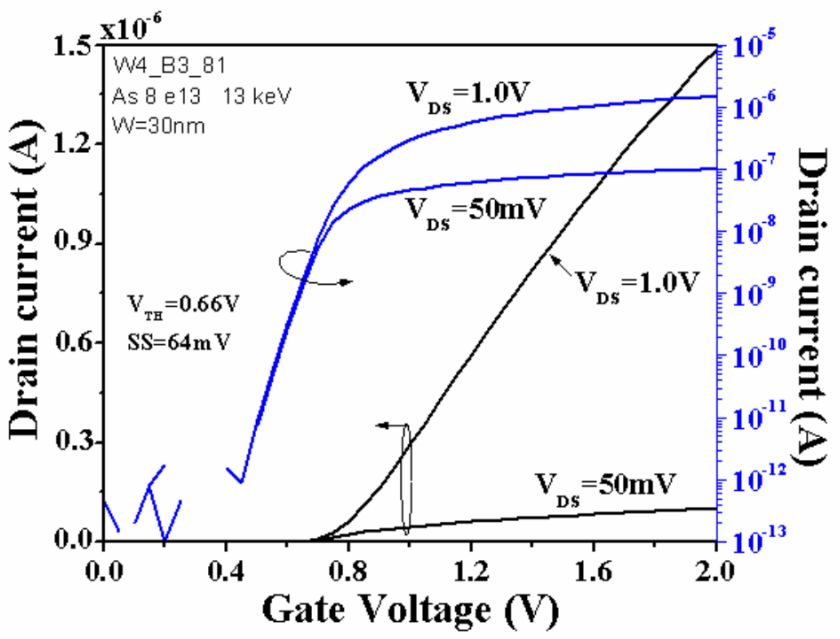


Figure 3.6: Measured I_D-V_G characteristics of an n-channel device with W_{eff} = 25nm and L_{GATE} = 1μm [4].

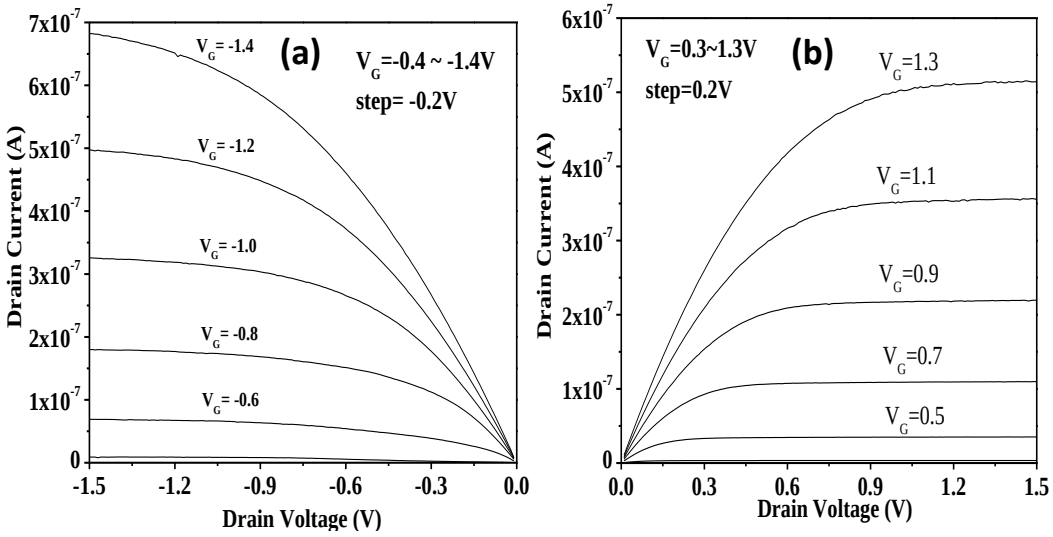


Figure 3.7: Measured I_D-V_D characteristics of Si JNTs. Drain current versus drain voltage for different values of gate voltage for Si JNTs with (a) a p-channel (b) a n-channel. Step of the V_G =0.2 V

As discussed in Section 2.3.4, the threshold voltage (V_{th}) of a JNT is related to the nanowire width W_{Si}. In Figure 3.8, the I_D-V_G curves shift systematically to the left, corresponding to small V_{th}, as the width of nanowire increases. This results confirms the conclusion from simulation in Section 2.3.4.

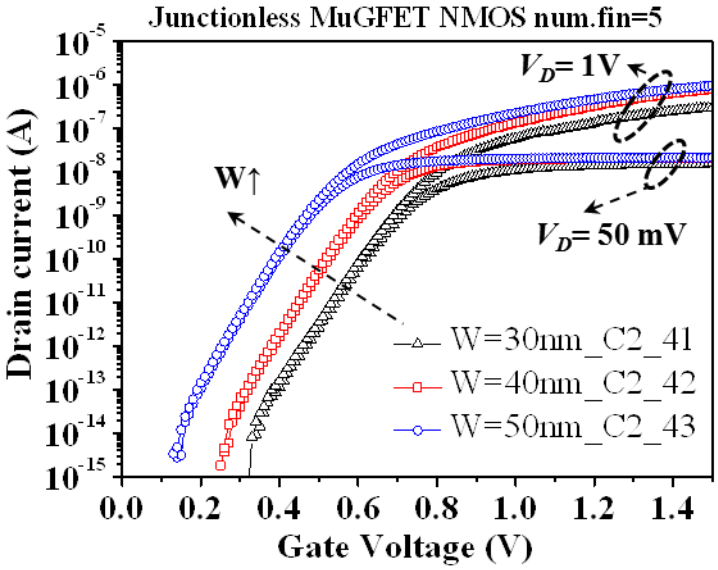


Figure 3.8: Experimental I_D-V_G characteristics of Si JNTs with various mask width values (30, 40, and 50 nm) at V_D of 0.05 and 1 V.

3.2.2 Characterization of Short Channel JNTs down to 22 nm

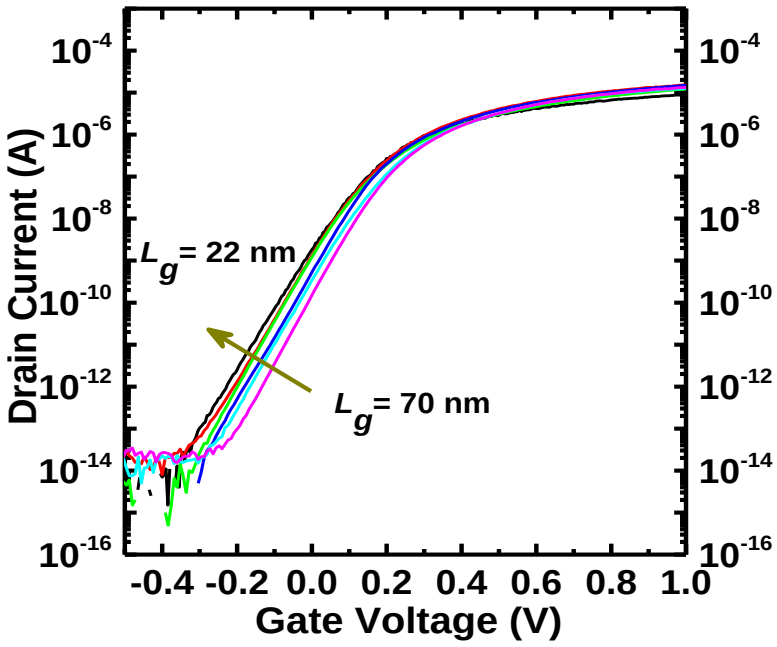


Figure 3.9: Measured I_D-V_G characteristics of n-channels JNT with L_{GATE} from 70 nm to 22 nm fabricate in CEA-LETI.

The I_D-V_G characteristics of the n-JNTs have been shown in Figure 3.9 with L_{GATE} from 70 nm down to 22 nm of devices from CEA-LETI. The results infer that due to short channel effects of the JNT, the subthreshold slopes of the JNT degrade as the gate

length goes shorter. However, the actual degradation of *SS* values is trivial and the leakage currents are well controlled.

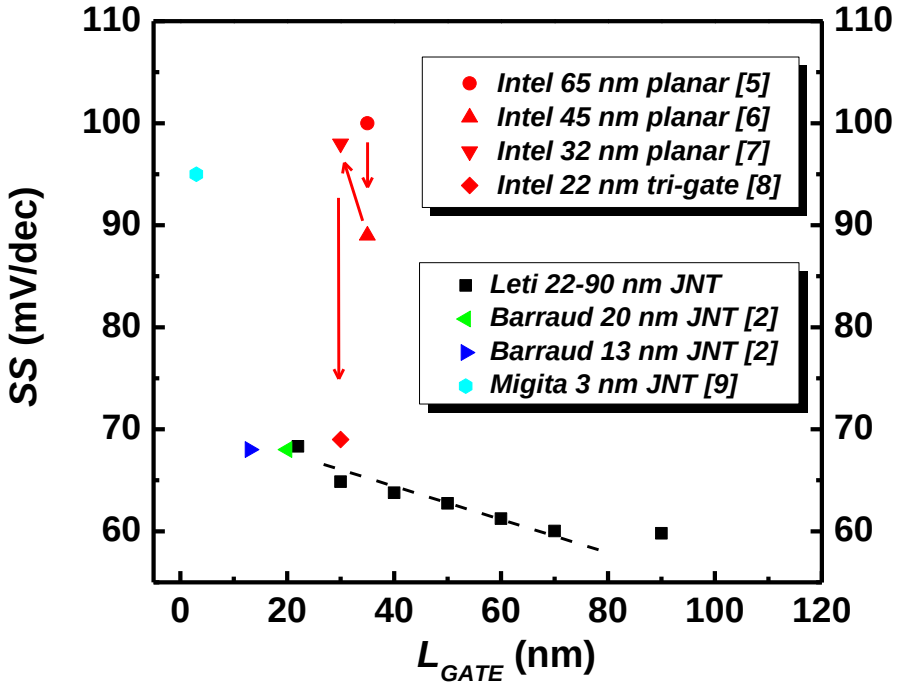


Figure 3.10: Summary of the *SS* values as a function of the gate lengths for both IM devices from Intel [5-8] and JNTs with gate lengths scaled down to 3 nm by Migita *et al.* [2, 9].

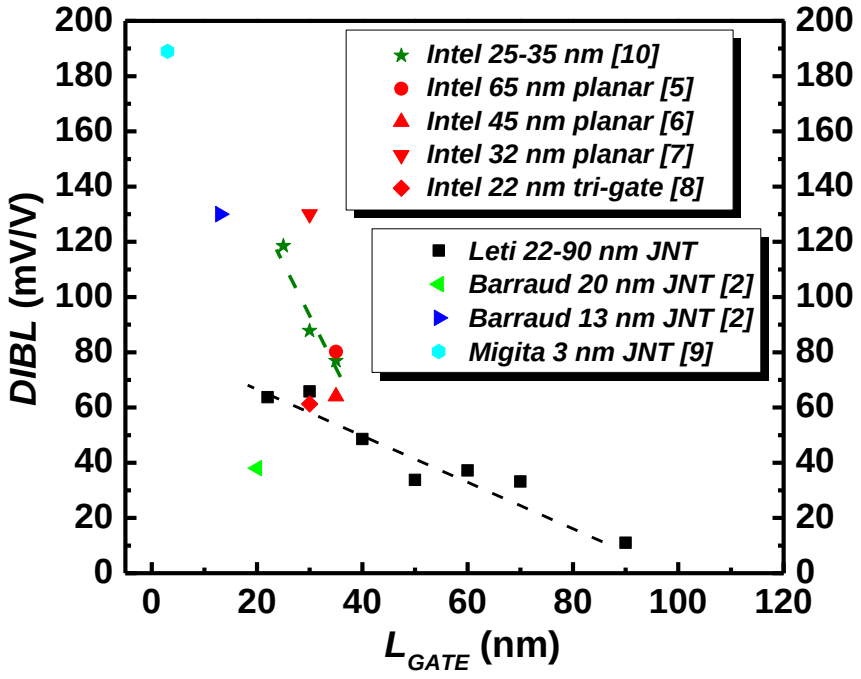


Figure 3.11: Summary of the *DIBL* values as a function of the gate lengths for IM test and commercial devices from Intel [5-8, 10], and as well as JNTs with gate lengths scaled down to 3 nm by Migita et al. [2, 9].

In order to quantitatively analyse the impact of short channel effects on JNTs, the measured *SS* values as a function of the gate lengths have been plotted in Figure 3.10 for both commercial IM devices from Intel [5-8], and the JNTs with gate lengths scaled down to 3 nm by Migita *et al.* [9]. The high performance devices of 65 nm and 45 nm technology nodes from Intel possess a gate length of 35 nm, while devices of 32 nm and 22 nm have the same gate length of 30 nm. As the High-*k*/Metal gate has been implemented when processing moved to 45 nm node, the *SS* value has been improved dramatically because of the enhanced gate control via the gate oxide scaling and metal gate. Devices of 32 nm node exhibit significant degradations in the gate control in terms of *SS*, and *DIBL* values shown in Figure 3.10 and Figure 3.11. Thus, in 32 nm node, improvements have been focused on the current boosting by further improved strain and High-*k*/Metal gate. The latest 22 nm tri-gate devices represent a tremendous improvement on the gate control as the electrostatics coupling has been elevated by 3-D structure and depletion capacitance has been eliminated. As a result, the *SS* and *DIBL* values drop to around 69 mV/dec and 61 mV/V, respectively, which are overwhelming comparing with previous generations.

Moreover, according to the measured results, the JNTs exhibit the inherent immunity to the short channel effects. Comparing with the latest 22 nm devices, the JNTs present better *SS* values as shown in the black dash trendline in Figure 3.10, which are closer to the theoretical limitations. Similarly, the *DIBL* of the fabricated devices forms a trendline below the traditional IM devices as shown with black dash line in Figure 3.11. With an optimization of the process [2], the *DIBL* becomes more competitive compared with Intel tri-gate [8, 10], which have even a longer physical gate length. In conclusion, JNTs exhibit the potential capability of scaling devices to the ultimate channel length, while acceptable functionality and gate control have been observed.

3.3 Impact Ionization Induced Dynamic Floating Body Effect in JNTs

3.3.1 Introduction

In the past 20 years, the on-chip supply voltage (V_{DD}) has been reduced from 5 V to 0.9 V while the gate length has been reduced from 1 μm to 22 nm. As a result, the active power consumption of the transistors dramatically decreases since it is proportional to V_{DD}^2. A further reduction of supply voltages as low as 0.6 V has been considered for low-operating-power applications in the semiconductor roadmap [11]. As a result, *SS* values smaller than the theoretical limitation of the classical transistors are desired. In previous chapter, steeper subthreshold slopes have been obtained from the simulation of short channel JNTs. In this section, the measured steeper slopes of JNT have been reported and compared to IM devices. The origin of this phenomenon, which is related to dynamic floating body effects, has been discussed.

IM mode SOI MOSFETs the impact ionization can trigger a sub-60 mV/dec *SS* value at room temperature, which is attributed to floating body effect [12]. Usually such phenomena appear in partially depleted SOI devices, but in some cases they can be observed in fully depleted devices [13]. As well as inversion mode SOI MOSFETs, Ref. [14] shows that even nanowire MuGFETs without junctions can demonstrate a decreased *SS* value, observed at V_D considerably smaller than in classical IM MOSFETs. It was explained that this phenomenon is associated with enhanced impact ionization in the highly doped channel of the JNT [15, 16]. In this section we report the dependence of this effect on channel geometry, which gives a hint about physical mechanisms.

3.3.2 Device Fabrication and Simulation set-up

The fabrication process of JNT is similar as mentioned section 1 in this chapter. The SOI layer was thinned down to T_{Si} = 10-20 nm and patterned into fins using e-beam lithography. Dry oxidation was performed to grow the gate oxide, and ion implantation was used to dope the devices uniformly n^+ with a concentration of $N_d = 1\times10^{19}$ cm^{-3} to realize N channel JNTs (Figure 3.12(b)). The n-type IM devices had the same dimensions as JNTs but a p-channel was ion implanted up to $N_a = 2 \times 10^{18}$ cm^{-3}, and source and drain N+ regions up to $N_d = 1\times10^{20}$ cm^{-3}. The source/drain region is self-aligned to the gate, and gate oxide thickness determined from HRTEM was 10 nm. The

length of the gate (L_{GATE}) is 1 μm. The width of the fin mask (W_{mask}) was from 50 to 30 nm, but in reality the channel width was 15-20 nm smaller than the mask width.

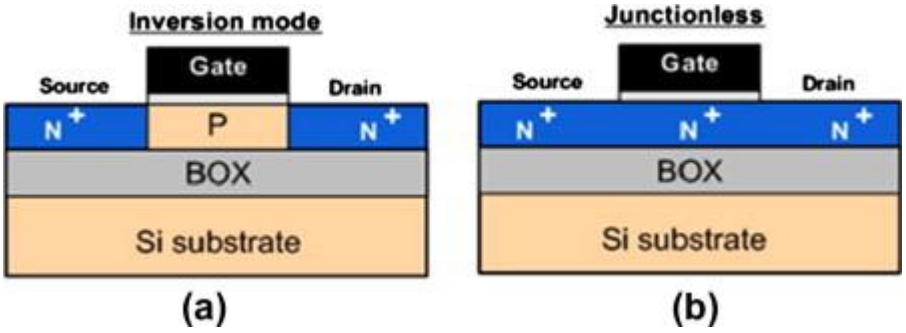


Figure 3.12: (a) Schematic view of a cross-section taken along the channel for IM MuGFET and (b) schematic view of a cross-section taken along the channel for JNT.

To investigate impact ionization and associated floating body effect for the JNT, simulations of 2-D double gate and 3-D tri-gate JNT are carried out using the Sentaurus device simulator. In the simulations the thickness of the silicon layer (T_{Si}) is 10 nm and the gate oxide (T_{ox}) is 2 nm. The entire nanowire is doped up to 1×10^{19} cm^{-3} with Arsenic. Various gate lengths (L_{GATE}) from 100 nm to 32 nm are simulated. The mesh is carefully generated for the impact ionization regions. The physical models used in the simulation are set up as described in chapter 2.

3.3.3 Results and Discussion

In analog devices, the floating body effect is known as the kink effect, which exhibits a rise in drain current at saturation region in I_D-V_D curves. For both IM devices and JNTs with W_{mask} = 40 nm, the kink-effect and steeper subthreshold slopes are observed experimentally in Figure 3.13 and 3.14. The similar effects are also observed for W_{mask} = 50 nm (not shown here). It should be noted that a considerable drain current increase in classical IM mode devices is observed at a drain voltage higher than 4 V (Figure 3.13(a)) while for the JNTs a sub-60 mV/dec subthreshold slope appears for a drain voltage as low as 2.5 V (Figure 3.14(b)) but the kink-effect is not very pronounced (Figure 3.14(a)).

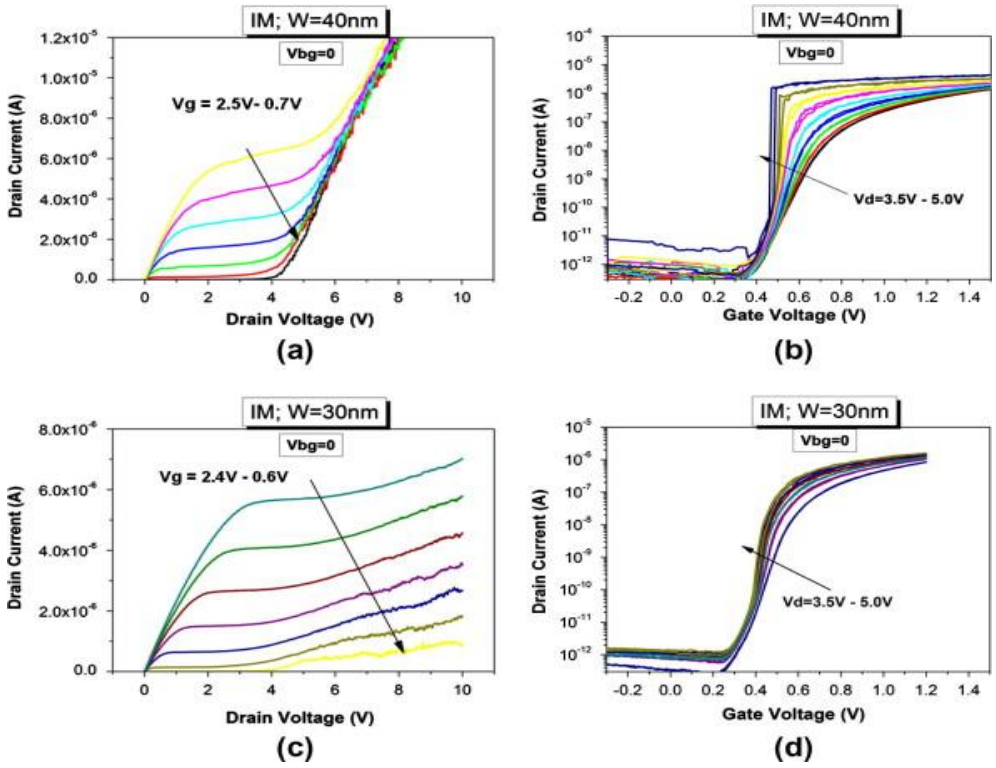


Figure 3.13: (a) Measured I_D-V_D characteristics as a function of V_G for n-type IM MuGFETs with W_{mask} = 40 nm, L_{GATE} = 1 µm, (b) I_D-V_G characteristics of IM MuGFETs with W_{mask} = 40 nm. (c) I_D-V_D characteristics as a function of V_G for n-type IM MuGFETs with W_{mask} = 30 nm, L_{GATE} = 1 µm and (d) I_D-V_G characteristics of IM MuGFETs with W_{mask} = 30 nm.

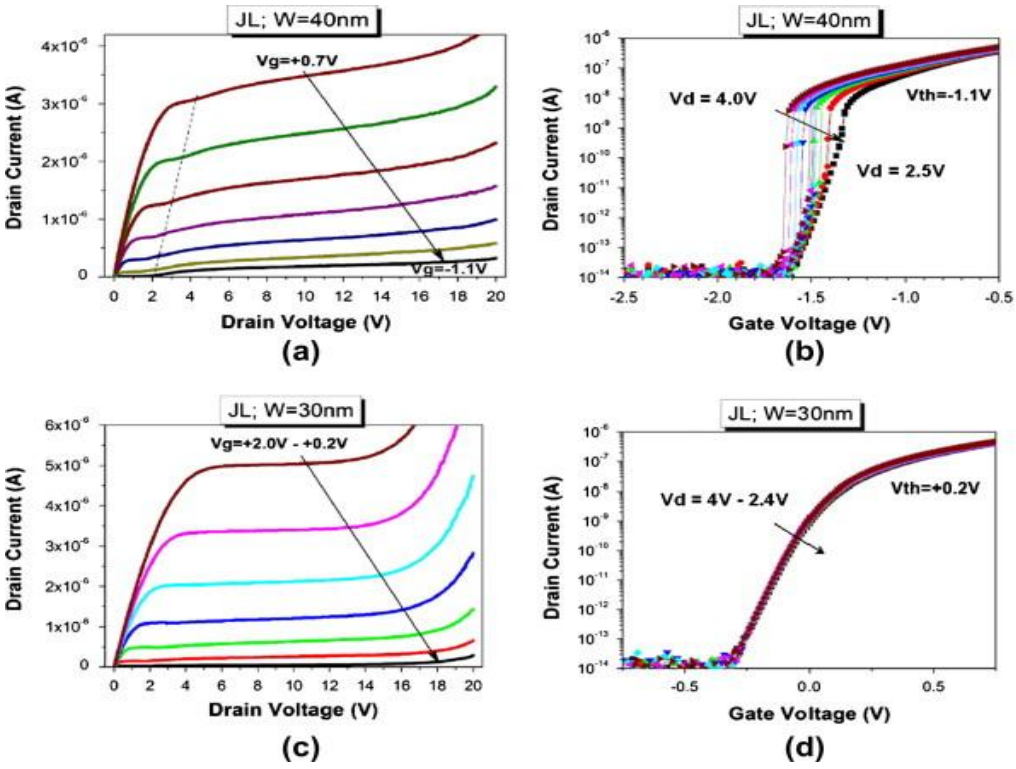


Figure 3.14: (a) Measured I_D-V_D characteristics as a function of V_G for n-type JNTs with W_{mask} = 40 nm, L_{GATE} = 1 µm, (b) I_D-V_G characteristics of JNTs with W_{mask} = 40 nm. (c) I_D-V_D characteristics as a function of V_G for n-type JNTs with W_{mask} = 30 nm, L_{GATE} = 1 µm and (d) I_D-V_G characteristics of JNTs with W_{mask} = 30 nm.

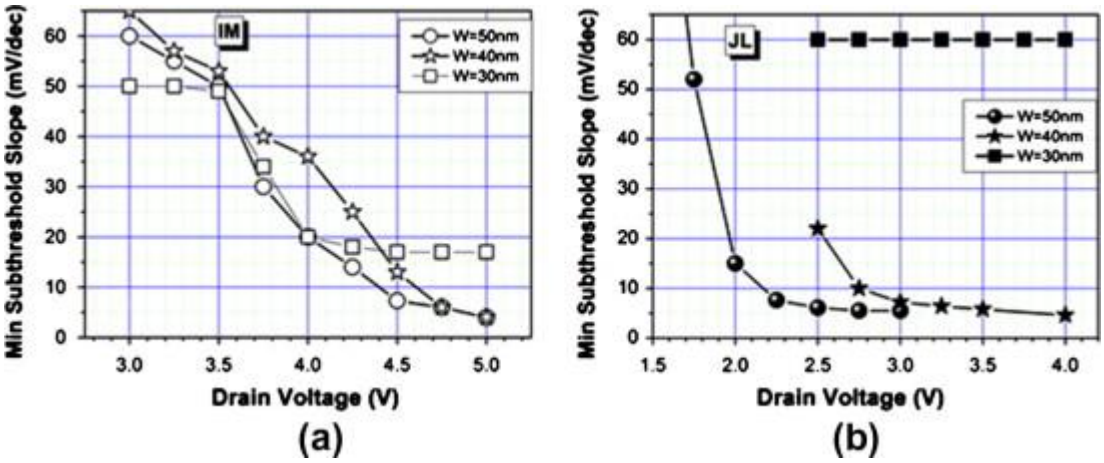


Figure 3.15: Measured minimum subthreshold slope vs. drain voltage as a function of channel width for (a) IM MuGFETs and (b) JNTs with, L_{GATE} = 1 μm.

The minimum *SS* value is plotted vs. applied V_D for both IM devices and JNTs in Figure 3.15. It shows that minimum *SS* value can reach 5 mV/dec for both devices. However, for 50 nm JNTs a drain voltage of 2.5 V is needed to obtain this slope, while for the IM MOSFET it is 5 V (a factor of two higher). This effect is partly attributed to bandgap narrowing in the highly doped channel of the JNT. Moreover, the larger V_D required for generating impact ionization in IM MOSFETs than in JNT can also be associated with increased scattering of electrons near SiO_2-Si interface and reduced energy relaxation length (λ_e) on the surface [17], which can be related to the electron temperature by the relationship:

$$\lambda_e E = \frac{5}{2}\frac{k}{q}(T_e - T_0) \tag{1}$$

where E is the electric field and T_0 is the lattice temperature. It has been shown [17] and [18] that the surface energy relaxation length can be in factor of two smaller than in bulk silicon. Thus, decreased surface energy relaxation length results in decreased electron temperature and decreased impact ionization generation rate and increased drain voltage, which initiates impact ionization for IM devices.

Besides the impact ionization rate, the total area of impact ionization is a considerable factor as well. 3-D simulation is carried out for impact ionization processes in the subthreshold region. Instead of surface current flowing in IM device, JNT exhibit bulk conduction, which means the current flow through entire fin. As a result, the

location and area of the impact ionization, which originated from the current, would be different in both cases. In Figure 3.16(a) simulation shows that the impact ionization rate is high close to the SiO_2-Si interfaces as it occurs at the thin inversion layer close to drain in IM MuGFET. Figure 3.16(b) shows that the impact ionization is more pronounced in the center of the fin for JNTs. Thus, due to its bulk conduction mechanism of JNTs, the impact ionization area is relatively larger than that in IM devices that has a surface conduction. Considering both impact ionization rate and area, it would more pronounce and efficient for JNT to initiate the impact ionization effect, and hence a lower activation voltage is required.

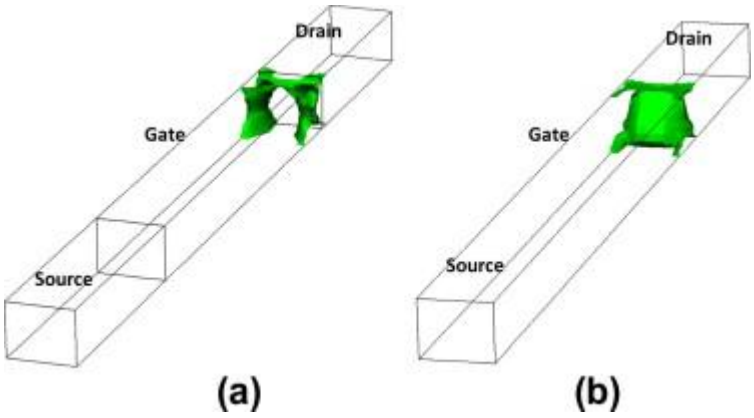


Figure 3.16: 3-D simulation of impact ionization rate of 100 nm gate length device (V_D = 3 V, V_G = 0.57 V) for (a) IM MuGFET with 1.836×10^{28} cm^{-3} s^{-1} surface and (b) JNT with 2.079×10^{28} cm^{-3} s^{-1} surface.

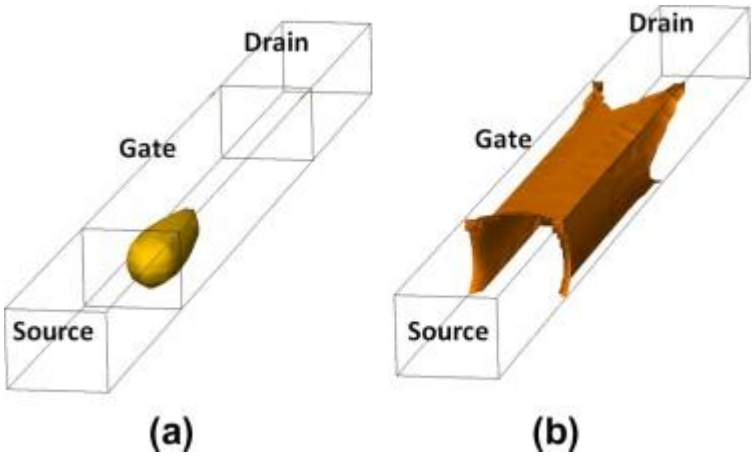


Figure 3.17: 3-D simulation of hole density of 100 nm gate length device (V_D = 3 V, V_G = 0.57 V) for (a) IM MuGFET with 1.663×10^{17} cm^{-3} surface and (b) JNT with 1.629×10^{18} cm^{-3} surface.

The generated holes from the impact ionization can form a floating body in the devices for both IM and JNTs. Figure 3.17 shows the simulated 3D hole density distribution in subthreshold region for (a) IM MuGFET and (b) JNT devices with 100 nm gate length (V_D = 3 V, V_G = 0.57 V). In Figure 3.17(a) it is seen that the generated holes are collected in the channel region near the source and accumulated as a floating body for IM device. On the other hand, the generated holes flow towards the SiO_2-Si interfaces near the source for JNTs and the hole density there is high (Figure 3.17(b)). Reduction of channel width increases surface scattering and recombination of charge carriers. Due to this enhanced charge recombination, holes accumulation is suppressed. A decrease of the channel width results in suppressing the floating body effects in IM and JNTs (see Figure 3.13(c) and (d) and Figure 3.14(c) and (d)). Thus, it can be noticed that the different geometry and location of the floating bodies in both IM and JNTs affect the subthreshold behavior dramatically.

3.3.4 Summary and Conclusion

Steep subthreshold slopes in JNT and IM devices are observed, which are explained in chapter 2 relating to a positive feedback loop which turns on the device at gate voltage lower than threshold. The influence of geometry, recombination mechanism and electric field in this loop for IM and JNTs are discussed according to the measurement and simulation results. It is observed that the impact ionization can be initiated by a decreased V_D and the kink-effect is less significant in JNTs comparing with classical IM device. Moreover, the impact ionization effect in short channel JNT is more pronounced, which gives the possibility of further reduction of the V_D. The floating body in JNT is relatively dynamic comparing with that in IM devices and proper design of the device structure may further reduce the V_D for a sub-60 mV/dec subthreshold slope.

3.4 Performance of 22 nm Tri-Gate JNTs at Elevated Temperatures

In this section, the high temperature performance of the short channel JNT has been studied. The performance evaluation at elevated temperature is critical for the advanced devices, owing to continually increasing density of the transistors, thus, higher power and heat dissipation on the chip nowadays.

The used short channel JNTs are Tri-gate High-k/Metal JNTs fabricated at CEA-LETI. They were fabricated on (100) silicon-on-insulator (SOI) wafers with a buried oxide (BOX) thickness of 145 nm and a starting SOI thickness of 12 nm. A detailed fabrication process is described elsewhere [25]. The gate stack consists of an HfSiON gate dielectric with an Equivalent Oxide Thickness (EOT) of 1.2 nm and a TiN/Poly-Si gate electrode. The 22 nm channel length p-MOS and n-MOS JNTs are available with different SOI doping concentrations (5×10^{18} cm^{-3} and 1×10^{19} cm^{-3}). A SiN spacer of 10 nm, between the end of the channel and the source/drain regions, has been used for the present devices. The measured devices are single NW transistors with height H = 10 nm and a 19 nm width (W). In previous Figure 3.5 shows the typical cross sectional TEM image of JNT. The measured physical gate length is 21.4 nm. The temperature dependent electrical characteristics of the JNTs were measured from 293 K to 473 K in a Cascade thermal probe station and an Agilent B1500 semiconductor parameter analyzer.

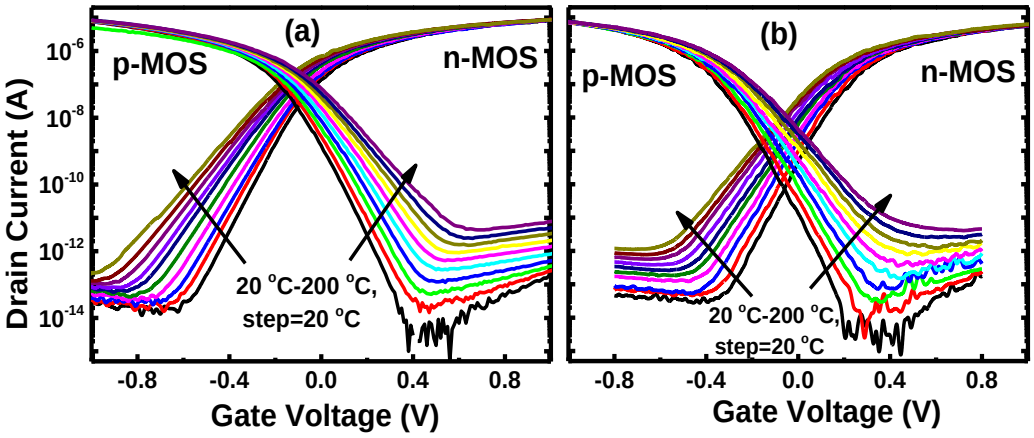


Figure 3.18: Transfer characteristics (I_D-V_G) of JNTs at different temperatures for for 22 nm gate length with nanowire doping (a) $N_D(N_A)=1\times10^{19}$ cm^{-3}, and (b) $N_D(N_A)=5\times10^{18}$ cm^{-3} at V_{DS} = ±0.9 V.

Figure 3.18 shows measured transfer characteristics (drain current as a function of gate voltage) of JNT at different temperatures, for a 22 nm gate length with nanowire doping (a) $N_D(N_A)=1\times10^{19}$ cm^{-3}, and (b) $N_D(N_A)=5\times10^{18}$ cm^{-3} at V_{DS} = ±0.9 V. The source terminal and the substrate are grounded during electrical measurements. These curves are used to extract the threshold voltage in saturation V_{thsat}, sub-threshold slope, and leakage current. The threshold voltage has been extracted by the second derivative

method. Figure 3.18 presents the expected trend: as the substrate temperature increases, the threshold voltage decreases and the subthreshold slope is degraded. The measured ON current at 473 K is 5.4 μA (4.9 μA) for n-MOS (p-MOS) JNT with a 1×10^{19} cm^{-3} doping. The ON current is extracted at fixed gate overdrive voltage, $G_{V0} = |V_{GS}-V_{th}|$=0.5 V. The off-state current is 2.4 pA (4.8 pA) at 473 K, which gives a high I_{ON}/I_{OFF} ratio (10^6). This leakage current is much lower than the recently reported values for ultra–thin-body (UTB) SOI MOSFETs having same gate stack [26], which indicates the electrostatic gate control of JNT is competitive to that of UTB SOI MOSFETs.

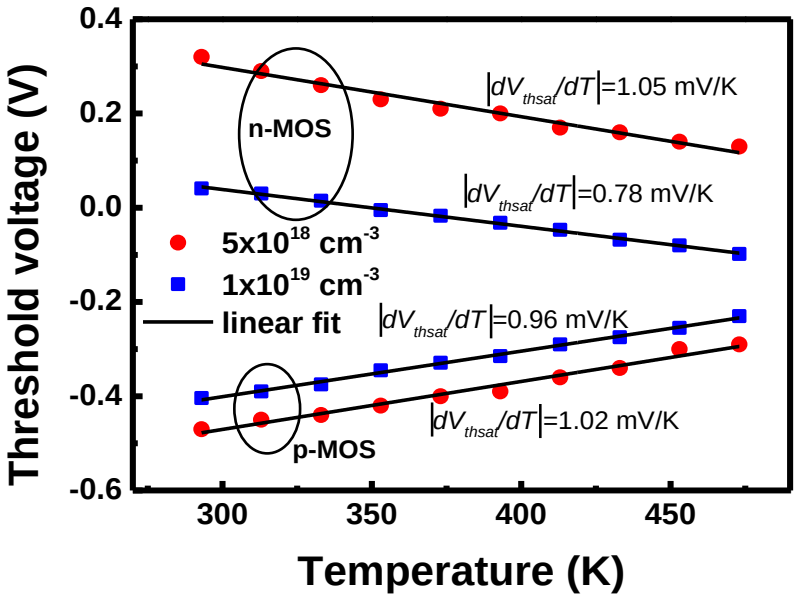


Figure 3.19: Measured threshold voltage V_{thsat} of an n-MOS and a p-MOS JNTs with 22 nm gate length, as a function of temperature for two different doping levels.

Figure 3.19 shows the variation of V_{thsat} with temperature for a p-MOS and an n-MOS JNTs for two different doping concentrations. The devices were measured in a temperature range varying from 293 K to 473 K. The threshold voltage was calculated from the maximum of the derivative of the transconductance. The V_{thsat} dependence on temperature is mainly due to the temperature dependence of the flatband voltage and of the doping concentration [21]. As the temperature increases, the position of the Fermi-level changes due to the increase of intrinsic carrier concentration. The absolute value of the temperature co-efficient for the temperature-dependent threshold voltage term ($|dV_{thsat}/dT|$) are 0.96 and 0.78 mV/K for 1×10^{19} cm^{-3} doping, and 1.02 and 1.05 mV/K for 5×10^{18} cm^{-3} doping for pMOS and nMOS JNTs, respectively. For the lower doping

levels, the value of $|dV_{thsat}/dT|$ is high, which may be related to higher rate of incomplete ionization [27]. Using the model given in ref. 26, the calculated ionization rate is about 92% for 5×10^{18} cm^{-3} doping and 98% for 1×10^{19} cm^{-3} doping at room temperature. Previously, values of $|dV_{th}/dT|$ = 1.3-1.7 mV/K [26] have been reported for long channel (1 µm) JNTs with a 1×10^{19} cm^{-3} nanowire doping (V_D= 0.05V). This value is significantly higher than in our results for short JNTs. This can be reasonably attributed to enhanced electrostatics gate control in the short devices, due to their much smaller EOT than those characterized in Ref. 22. For similar gate stack in UTB SOI MOSFETs the absolute threshold voltage shift of 0.63 mV/K has been reported [26].

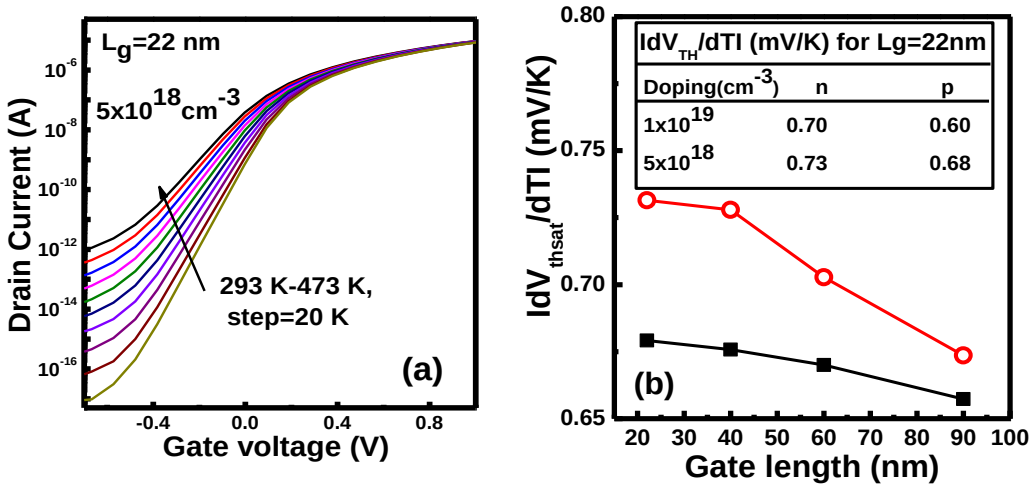


Figure 3.20: (a) Simulated I_D-V_G curve of N-MOS for different temperature, and (b) variation of $|dV_{thsat}/d_T|$ with gate length for n-MOS (○) and p-MOS (■)JNTs with 5×10^{18} cm^{-3} doping.

In order to understand the threshold voltage variation with temperature, the three-dimensional simulations of the Si JNTs were carried out on the Sentaurus 3-D device simulator. Figure 3.20 (a) shows the simulated I_D-V_G curve for 22 nm gate length n-MOS device at different temperatures. The value of $|dV_{thsat}/dT|$ for different gate lengths have been extracted using the simulation and are plotted in Figure 3.20(b). Also, from simulation we observe a higher $|dV_{thsat}/dT|$ value for lower doping concentration (inset table in Figure 3.20(b)), which is consistent with the experimental results. A small divergence between the experimental and simulated values can possibly be related to the temperature dependence of the interface charge density in the gate oxide.

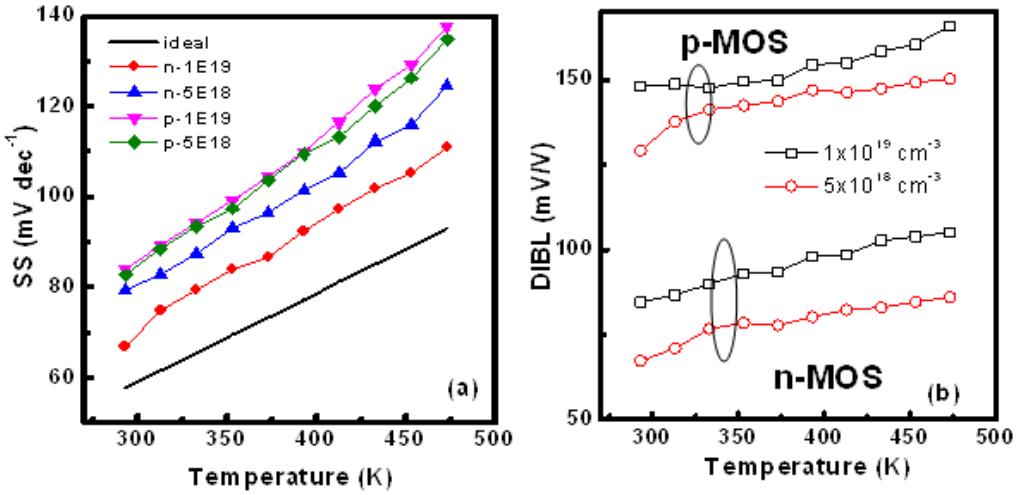


Figure 3.21: Variation of (a) sub-threshold slope (*SS*) and (b) *DIBL* with temperature of p-MOS and n-MOS JNTs. Solid black line in Figure 3.21(a) shows the evolution of the theoretical *SS* with temperature.

The sub-threshold slope, *SS* is defined as the inverse of the slope of the log of the drain current versus gate voltage, has a theoretical minimum value of *SS* = (kT/q) ln(10), which is illustrated in Figure 3.20(a) (solid black line) along with the temperature dependence of the *SS* for JNTs. The minor difference compared to the theoretical limit may be due to the presence of interface traps. According to the Fermi-level movement at the oxide/semiconductor interface, the interface trap distribution has an effect on *SS* value. The sub-threshold slope measured at room temperature is 68 and 84 mV/decade for n-MOS and p-MOS JNTs, respectively, for a 1×10^{19} cm^{-3} doping, which is comparable with the recently reported value of 79 mV/decade for 22 nm JNT by C.-H. Park *et al.* [28]. From Figure 3.20(a), it is clear that the *SS* value increases linearly with temperature and at the same rate as the theoretical limit, which confirms the good electrostatics gate control even at high temperature. Temperature dependent drain induced barrier lowering (*DIBL*) is shown in Figure 3.20(b). For n-MOS (1×10^{19} cm^{-3}) the *DIBL* is below 100 mV/V even at 473 K, which is lower than the room temperature reported value (200 mV/V) for 26 nm SOI FET [29].

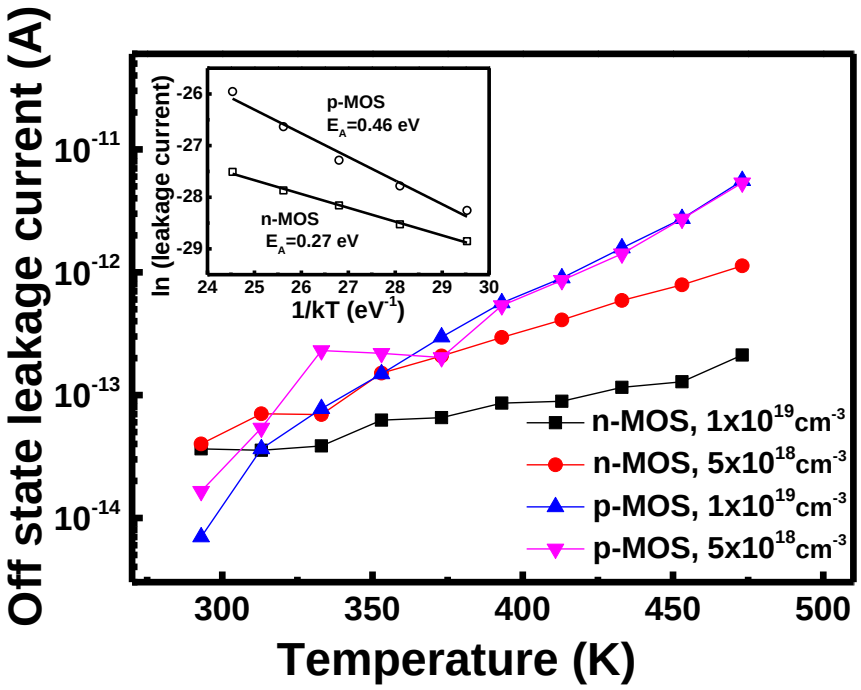


Figure 3.22: Temperature dependent off-state leakage current of 22 nm JNTs; Inset shows the Arrhenius plot of I_{OFF} from 393 K to 473 K for a n-MOS and a p-MOS, devices with 5×10^{18} cm^{-3} doping. V_D = 0.9 V.

Figure 3.22 shows the evolution of off-state leakage current with temperature for p-MOS and n-MOS JNTs devices for two different doping concentrations. The off-state leakage current is extracted at a fixed gate voltage, $V_G = V_{thsat} \pm 1.0$ V for p(n)-MOS. The off-state leakage current is close to 1 pA for the 19 nm NW width (53 pA/μm) n-MOS devices at 473 K, which is substantially lower than the values recently reported for JNTs measured at room temperature (10 pA for 15 nm NW width) [28]. For p-MOS devices the off-state leakage current is slightly higher than in n-MOS but below than 6.0 pA at 473 K. The inset of Figure 3.22 shows that the thermal activation energy (E_a) for the off-state leakage current is 0.48 and 0.27 eV for n-MOS and p-MOS, respectively (5×10^{18} cm^{-3} doping). This is calculated by approximating the Arrhenius plot for T ranging from 393 K to 473 K. The activation energies are smaller than half of band gap of silicon, which suggests that the off-state leakage current is caused by trap-assisted tunneling with Poole-Frenkel effect [30]. Note that for smaller gate lengths, further increase of the off-state leakage current caused by band-to-band tunnelling (BTBT) is foreseen.

In conclusion, 22 nm silicon JNT was presented with temperature studies on the electrical performance. The JNT showed excellent electrical characteristics at high temperature (473 K) with a high I_{ON}/I_{OFF} (~10^6), low leakage current (1-6 pA), and good subthreshold slope (110-138 mV/dec). Linear increases of *SS* value with temperature at the same rate as the theoretical limit confirms the good electrostatics gate control even at high temperature. The origin of off-state leakage is explained by calculating the thermal activation energy. The measured $|dV_{thsat}/dT|$ of 22-nm JNT is 0.78-1.05 mV/K, which depends on the doping concentration. Whilst having superior transistor properties at room temperature, the 22-nm JNT has managed to maintain these properties even as temperature is increased up to 473 K.

3.5 Characterization of a Junctionless Diode

3.5.1 Introduction

Diode connected transistor consists of two terminals, which are a shorted gate-drain and the source. This setup is commonly used in circuit design, such as the current mirror circuit. In this section, a diode has been realised using a silicon JNT. The device contains neither PN junction nor Schottky junction. The device is measured at different temperatures. The characteristics of the junctionless diode (JL diode) are essentially identical to those of a regular PN junction diode. The JL diode has an ON/OFF current ratio of 10^8, an ideality factor of 1.09, and a reverse leakage current of 1×10^{-14} Ampere at room temperature. The mechanism of the leakage current is discussed using the activation energy (E_A). The turn-on voltage of the device can be tuned by JL transistor threshold voltage.

The JNT has been recently introduced and is a promising candidate for end-of-roadmap complementary metal-oxide-semiconductor (CMOS) circuit fabrication [1, 19]. The electrical properties of JNThave been reported in several publications [22, 31]. However the operation of the device in the diode configuration has not been reported yet. The diode configuration setup is commonly used in circuit designs [32].

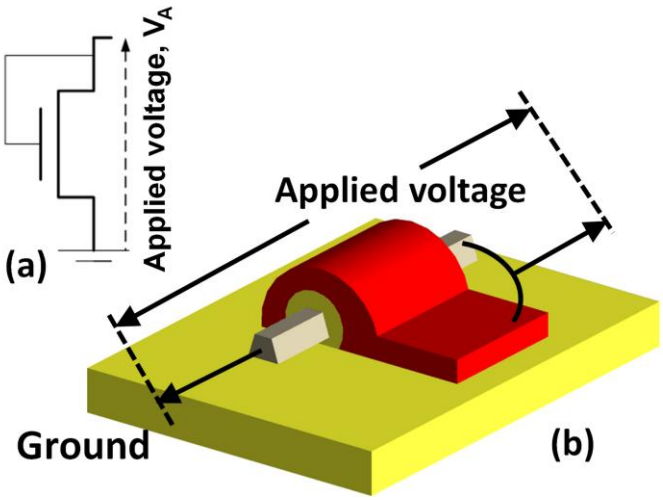


Figure 3.23: (a) Schematic representation for the JL transistor in diode configuration (circuit symbol) (b) Schematic diagram of the structure of a JL diode

The Junctionless diode (JL diode) is obtained by shorting the gate and drain electrodes of a JL transistor (Figure 3.23(a)). The JL transistor used here has a gate length of 1μm and a cross section of approximately 10 nm × 10 nm. The n-type JL transistor has a uniform doping concentration of 1×10^{19} cm^{-3} in the source, drain and channel regions (Figure 3.23(b)). The gate oxide thickness is 7 nm. The performance of the diode is measured by Cascade thermal probe station and Agilent B1500 semiconductor parameter analyzer.

3.5.2 Results and Discussion

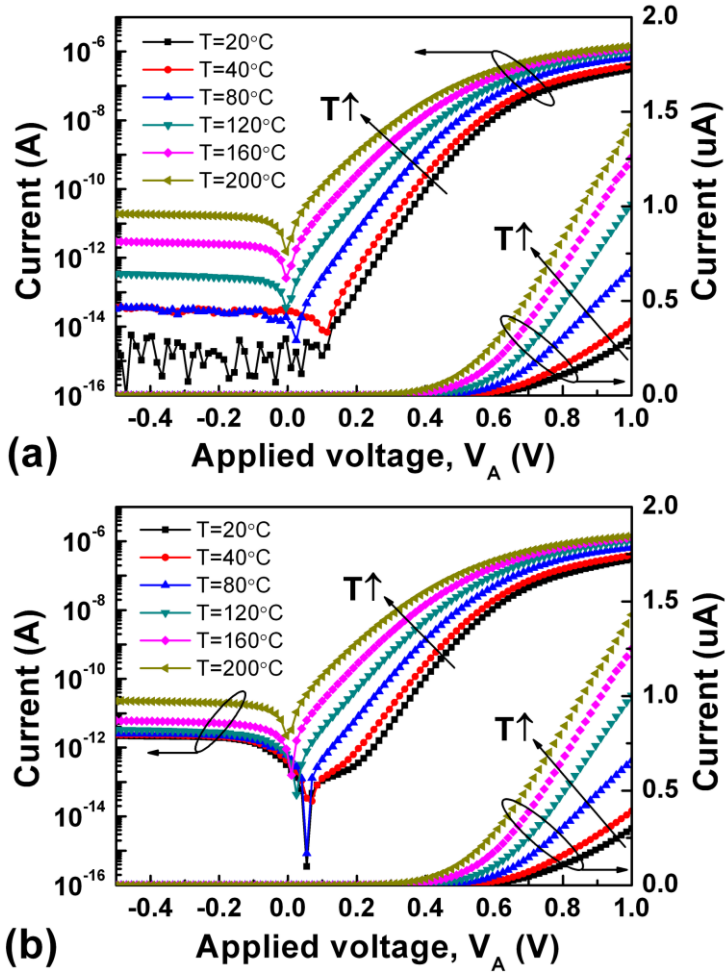


Figure 3.24: $I(V_A)$ characteristics of the JL diode in linear and log scale (a) in the dark and (b) under illumination at temperatures ranging from 20 ºC to 200 ºC.

Figure 3.24 shows the experimental $I(V_A)$ characteristics of the JL diode in the dark (Figure 3.24(a)) and under microscope light illumination (Figure 3.24(b)), where V_A is the applied voltage on the JL diode. In Figure 3.24(a), the dark current of the JL diode is lower than 10^{-14} Ampere and an on/off current ratio of 10^8 is observed at 20 ºC. When the temperature is increased, the dark current increases and is attributed to the increase of intrinsic carrier concentration, but remains low compared to the dark current of Silicon on insulator (SOI) diodes based on MOSFETs with junctions [33]. When under illumination, in Figure 3.24(b), the current under reverse bias increases due to the photogeneration of electron-hole pairs. Under forward bias, the slope of the $\log(I(V_A))$ curves decreases as temperature increased, which is commonly observed in regular PN

junction diodes [34]. In our device, this is caused by the increase of subthreshold slope of the JL transistor with temperature.

The electrical characteristics of the JL diode are substantially similar to those of a regular PN junction diode. However, the physics involved is quite different. In a PN junction the forward current results from of recombination of electrons injected in the P-type region and the recombination of holes injected in the N-type region. In the JL diode, the current is formed by the drift/diffusion of majority carriers (electrons) in the channel region, where the electron concentration varies exponentially with the gate bias. In a classical PN junction diode, generation/recombination mechanisms in the transition region are the main source of reverse current; they also degrade (decrease) the slope of the log($I(V_A)$) curve in forward bias operation [35]. The total current in the diode can be expressed by a single relationship that encompasses both diffusion current and generation/recombination:

$$I = I_S[\exp(\frac{qV_A}{nkT}) - 1] \tag{2}$$

where I_s is the reverse saturation current, n is the ideality factor, q is the charge of electron, k is Boltzmann's constant and T is the temperature in Kelvin (K). The value of the ideality factor varies between 1 and 2. It is equal to 1 in the case of a pure diffusion current and to 2 in the case where the current is entirely dominated by recombination/generation mechanisms in the transition region. In the JL diode these generation/recombination mechanisms take place in the fully depleted channel region instead. We extracted the ideality factor of JL diodes from their $I(V_A)$ curves, using the following expression derived from (1) under forward biasing conditions:

$$n = \frac{dV_A}{d(\ln(I))} \times \frac{q}{kT} \tag{3}$$

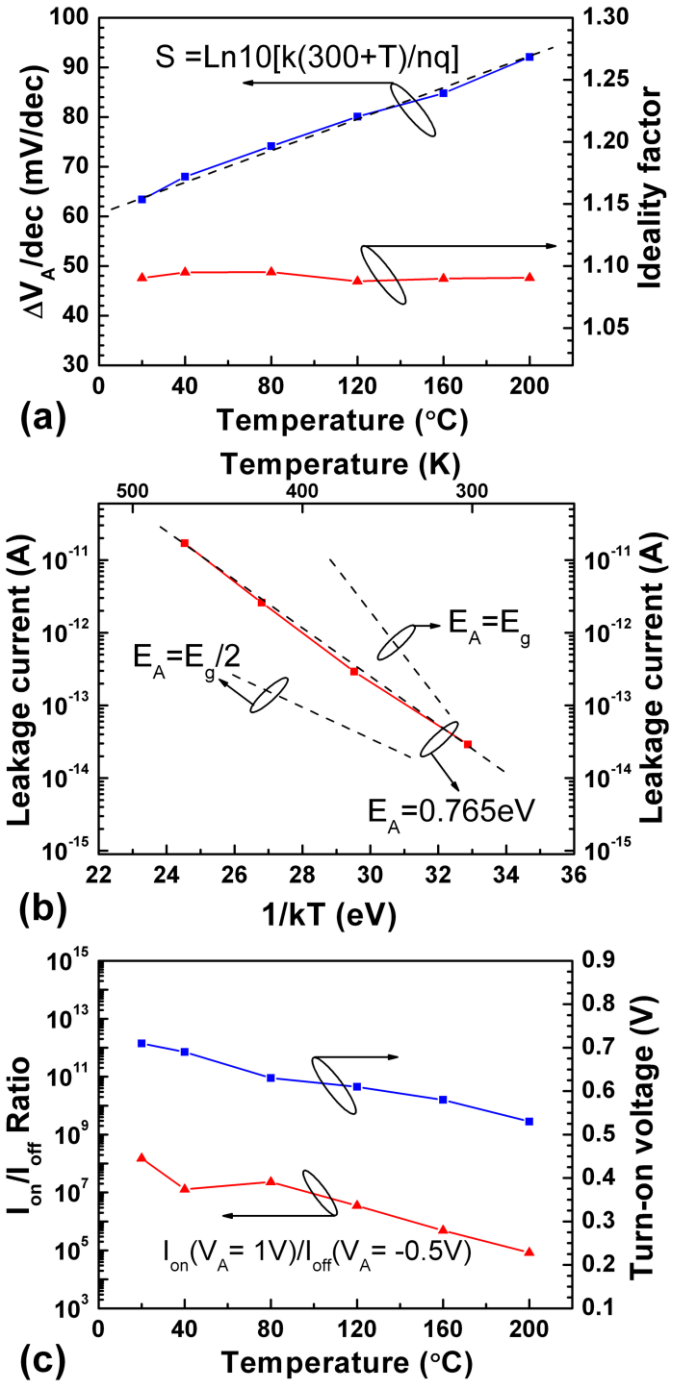


Figure 3.25: (a) V_A variation for a decade change in current and ideality factor at temperatures ranging from 20 ºC to 200 ºC (b) Arrhenius plot of reverse leakage current of the JL diode (c) On/off current ratio and turn-on voltage of the JL diode at temperatures ranging from 20 ºC to 200 ºC.

Figure 3.25(a) shows the values of n of the JL diode at temperature ranging from 20 ºC to 200 ºC. An ideality factor close to 1 (n=1.1) is observed for all temperatures. For a decade change in current, ideally the V_A varies by the factor $\Delta V_A = ln10kT/q$. ΔV_A is linearly increased as temperature arises. The measured $\Delta V_A/dec$ values match the theoretical calculation. $\Delta V_A/dec$ values derive from having a subthreshold slope close to $\frac{kT}{q}\ln(10)$ measured in JL transistors over the same range of temperatures and have neglectable degradation when using diode configuration [36].

In CMOS technology, the drain and gate connected transistors present, as a major drawback, high leakage current. However JL diodes show a significantly reduced leakage current. As leakage current due to band to band tunneling (BBT) and trap-assisted tunneling (TAT) has strong lateral voltage dependence and activation energy (E_A) close to 0 eV for BBT which has not been observed in our measurements [37]. We consider two components of the off-state leakage current of JL diodes: current due to thermal generation in the depleted body film ($I_{gen,dep}$) and current due to diffusion at the edge of neutral body just outside the channel-drain junction (I_{diff}) [38].

$$I_{Leakage} = I_{gen,dep} + I_{diff} \tag{4}$$

For the first component, electron-holes pairs are generated in the depleted nanowire and it is temperature-dependent. The generated electrons are swept to the drain and the generated holes are attracted to the source. The current is due to the thermal generation inside the depleted region and given by [38]

$$Igen,dep = \frac{qn_i}{\tau_g}V \tag{5}$$

where n_i is the intrinsic electron concentration, τ_g is the effective generation lifetime inside the depletion region and V is the volume of the depletion region. The temperature dependence behaviour of the leakage current is related to the temperature dependence of n_i which is proportional to $exp(-E_g/2kT)$, where E_g is the band gap of silicon. Thus $I_{gen,dep}$ is proportional to $exp(-E_g/2kT)$, and the E_A expected to be 0.56 eV. The second current component is due to diffusion at the edge of neutral body film just outside of the

depletion region in the channel-drain junction. This current is usually called diffusion current and expressed as [38]

$$I_{diff} = q\sqrt{\frac{D_n}{\tau_n}}\frac{n_i^2}{N_d}(\exp(\frac{q(\varphi_S - V_D)}{kT}) - 1)A \quad (6)$$

where D_n is the electron diffusion coefficient, τ_n is the electron lifetime inside the depletion region, V_D is the applied voltage at drain, φ_S is the surface potential in the depletion region close to drain and A is the area of the channel-drain junction. The diffusion current in JL diode is approximately proportional to n_i^2. Thus I_{diff} is proportional to $exp(-E_g/kT)$, and E_A expected to be 1.12 eV. Figure 3.25(b) shows the activation energy extracted from the average of reverse leakage current curves measured in the dark (V_A = -0.5 V to -0.1 V). E_A = 0.765 eV indicates the leakage currents are mainly dominated by thermal generation current in depletion region. The diffusion component of the leakage current makes $E_A > E_g/2$. It is also noted that I_{diff} is also increased by $|\varphi_S - V_D|$ exponentially. As the gate and drain is shorted in JL diode, drain voltage (V_D) and gate voltage (V_G) are identical. φ_S changes slower than V_G [34], thus $|\varphi_S - V_D|$ is increased slightly when $|V_A|$ arises. Thus I_{diff} increases slightly when larger reverse voltage applied. This is consistent with the results observed in Figure 3.25.

Figure 3.25(c) shows that the turn-on voltage of the JL diode decreases from 0.73 V to 0.51 V as temperature increased from 20 ºC to 200 ºC. This shift is related to the shift in threshold voltage of the JL nanowire transistor with temperature [22]. Indeed, unlike in regular PN junction diodes, the turn-on voltage of JL diodes is not determined by the band gap but by the threshold voltage of the JL transistor [39]. Lower turn-on voltage can readily be achieved by tuning the cross-sectional dimensions of the nanowire or the gate material. The on and off currents are extracted at V_A = 1 V and -0.5 V, respectively. The on/off current ratios degrade with temperature, due to the exponential increase of the leakage currents and smaller current change under forward bias.

3.5.3 Summary

In summary, we observe that a JL nanowire transistor connected in the diode configuration presents characteristics similar to those of a regular PN junction diode. An

ideality factor close to unity is observed in the temperature range 20 ºC to 200 ºC. Leakage currents due to thermal generation and diffusion is evident as E_A = 0.765 eV. The diode turn-on voltage can be tuned by varying the threshold voltage of the junctionless transistor.

3.6 Conclusions

In this chapter, the fabrication process of IM devices and JNTs down to 22 nm gate length has been discussed and characterizations have been carried out for these devices at elevated temperature and stressed conditions. Steep subthreshold slopes (*SS*) in JNT and IM devices are observed, and the influence of geometry, recombination mechanism and electric field on this effect for IM and JNTs are discussed according to the measurement and simulation results. It is observed that the floating body in JNT is relatively dynamic compared with that in IM devices and proper design of the device structure may further reduce the V_D for a sub-60 mV/dec subthreshold slope. Diode configuration of the JNT has also been evaluated, which demonstrates the first diode without junctions with outstanding characteristics.

3.7 References

[1] Colinge JP, Lee CW, Afzalian A, Akhavan ND, Yan R, Ferain I, et al. Nanowire transistors without junctions. Nat Nanotechnol. 2010;5:225-9.

[2] Barraud S, Berthomé M, Coquand R, Cassé M, Ernst T, Samson M-P, et al. Scaling of trigate junctionless nanowire MOSFET with gate length down to 13 nm. Electron Device Letters, IEEE. 2012;33:1225-7.

[3] Jeon D-Y, Park S, Mouis M, Berthomé M, Barraud S, Kim G-T, et al. Revisited parameter extraction methodology for electrical characterization of junctionless transistors. Solid State Electron. 2013.

[4] Kranti A, Yan R, Lee C-W, Ferain I, Yu R, Akhavan ND, et al. Junctionless nanowire transistor (JNT): Properties and design guidelines. Solid-State Device Research Conference (ESSDERC), 2010 Proceedings of the European: IEEE; 2010. p. 357-60.

[5] Bai P, Auth C, Balakrishnan S, Bost M, Brain R, Chikarmane V, et al. A 65nm logic technology featuring 35nm gate lengths, enhanced channel strain, 8 Cu interconnect layers, low-k ILD and 0.57 μm^2 SRAM cell. Electron Devices Meeting, 2004 IEDM Technical Digest IEEE International: IEEE; 2004. p. 657-60.

[6] Jan C-H, Bai P, Biswas S, Buehler M, Chen Z-P, Curello G, et al. A 45nm low power system-on-chip technology with dual gate (logic and I/O) high-k/metal gate strained silicon transistors. Electron Devices Meeting, 2008 IEDM 2008 IEEE International: IEEE; 2008. p. 1-4.

[7] Natarajan S, Armstrong M, Bost M, Brain R, Brazier M, Chang C-H, et al. A 32nm logic technology featuring 2 nd-generation high-k+ metal-gate transistors, enhanced channel strain and 0.171 μm^2 SRAM cell size in a 291Mb array. Electron Devices Meeting, 2008 IEDM 2008 IEEE International: IEEE; 2008. p. 1-3.

[8] Auth C, Allen C, Blattner A, Bergstrom D, Brazier M, Bost M, et al. A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors. VLSI Technology (VLSIT), 2012 Symposium on: IEEE; 2012. p. 131-2.

[9] Migita S, Morita Y, Masahara M, Ota H. Impact of atomic-scale structural design on ultra-short channel (3 nm) MOSFETs. Nanoelectronics Conference (INEC), 2013 IEEE 5th International: IEEE; 2013. p. 132-5.

[10] Rios R, Cappellani A, Armstrong M, Budrevich A, Gomez H, Pai R, et al. Comparison of Junctionless and Conventional Trigate Transistors With L_g down to 26 nm. Electron Device Letters, IEEE. 2011;32:1170-2.

[11] International Technology Roadmap for Semiconductors, http://www.itrs.net/.

[12] Colinge J-P. Silicon-on-insulator technology: materials to VLSI: Kluwer Academic Pub; 1997.

[13] Bawedin M, Cristoloveanu S, Flandre D. Innovating SOI memory devices based on floating-body effects. Solid State Electron. 2007;51:1252-62.

[14] Lee C-W, Nazarov AN, Ferain I, Akhavan ND, Yan R, Razavi P, et al. Low subthreshold slope in junctionless multigate transistors. Appl Phys Lett. 2010;96:102106--3.

[15] Lee C-W, Afzalian A, Yan R, Akhavan ND, Xiong W, Colinge J-P. Drain breakdown voltage in MuGFETs: Influence of physical parameters. Electron Devices, IEEE Transactions on. 2008;55:3503-6.

[16] Lee C-W, Yan R, Ferain I, Kranti A, Akhvan N, Razavi P, et al. Nanowire zero-capacitor DRAM transistors with and without junctions. Nanotechnology (IEEE-NANO), 2010 10th IEEE Conference on: IEEE; 2010. p. 242-5.

[17] Slotboom J, Streutker G, van Dort M, Woerlee P, Pruijmboom A, Gravesteijn D. Non-local impact ionization in silicon devices. Electron Devices Meeting, 1991 IEDM'91 Technical Digest, International: IEEE; 1991. p. 127-30.

[18] Slotboom J, Streutker G, Davids G, Hartog P. Surface impact ionization in silicon devices. Electron Devices Meeting, 1987 International: IEEE; 1987. p. 494-7.

[19] Lee CW, Afzalian A, Akhavan ND, Yan R, Ferain I, Colinge JP. Junctionless multigate field-effect transistor. Appl Phys Lett. 2009;94.

[20] Colinge JP, Kranti A, Yan R, Lee CW, Ferain I, Yu R, et al. Junctionless Nanowire Transistor (JNT): Properties and design guidelines. Solid State Electron. 2011;65-66:33-7.

[21] de Souza M, Pavanello MA, Trevisoli RD, Doria RT, Colinge JP. Cryogenic Operation of Junctionless Nanowire Transistors. IEEE Electr Device L. 2011;32:1322-4.

[22] Lee CW, Borne A, Ferain I, Afzalian A, Yan R, Akhavan ND, et al. High-Temperature Performance of Silicon Junctionless MOSFETs. IEEE T Electron Dev. 2010;57:620-5.

[23] Shan Y, Ashok S, Fonash SJ. Unipolar accumulation-type transistor configuration implemented using Si nanowires. Appl Phys Lett. 2007;91:093518--3.
[24] Iqbal M-H, Hong Y, Garg P, Udrea F, Migliorato P, Fonash SJ. The nanoscale silicon accumulation-mode MOSFET—a comprehensive numerical study. Electron Devices, IEEE Transactions on. 2008;55:2946-59.
[25] D.-Y. Jeon SJP, M. Mouis, M. Berthomé, S. Barraud, G.-T. Kim and G. Ghibaudo. Electrical characterization and revisited parameter extraction methodology in junctionless transistors. Proceedings of EuroSOI, Montpellier, France. 2011:109-10.
[26] V. Kilchytska FA, O. Faynot, D. Flandre. High-temperature perspectives of UTB SOI MOSFETs. Ultimate Integration of Silicon (ULIS) Conference. 2011.
[27] Altermatt PP, Schenk A, Schmithusen B, Heiser G. A simulation model for the density of states and for incomplete ionization in crystalline silicon. II. Investigation of Si : As and Si : B and usage in device simulation. J Appl Phys. 2006;100.
[28] Park CH, Ko MD, Kim KH, Baek RH, Sohn CW, Baek CK, et al. Electrical characteristics of 20-nm junctionless Si nanowire transistors. Solid State Electron. 2012;73:7-10.
[29] Majumdar A, Ren ZB, Sleight JW, Dobuzinsky D, Holt JR, Venigalla R, et al. High-performance undoped-body 8-nm-thin SOI field-effect transistors. IEEE Electr Device L. 2008;29:515-7.
[30] Nakashima A, Kimura M. Mechanism Analysis of Off-Leakage Current in an LDD Poly-Si TFT Using Activation Energy. IEEE Electr Device L. 2011;32:764-6.
[31] Nazarov A, Ferain I, Akhavan ND, Razavi P, Yu R, Colinge J. Random telegraph-signal noise in junctionless transistors. Appl Phys Lett. 2011;98:092111--3.
[32] Baker RJ. CMOS: circuit design, layout, and simulation: Wiley-IEEE Press; 2011.
[33] De Souza M, Rue B, Flandre D, Pavanello MA. Performance of Ultra-Low-Power SOI CMOS Diodes Operating at Low Temperatures. ECS Transactions. 2011;35:325-30.
[34] Sze SM, Ng KK. Physics of semiconductor devices: Wiley-interscience; 2006.
[35] Schroder DK. Semiconductor material and device characterization: Wiley-interscience; 2006.
[36] Nazarov A. Semiconductor-on-insulator materials for nanoelectronics applications: Springerverlag Berlin Heidelberg; 2011.

[37] Duffy R, Heringa A, Venezia V, Loo J, Verheijen M, Hopstaken M, et al. Quantitative prediction of junction leakage in bulk-technology CMOS devices. Solid State Electron. 2010;54:243-51.

[38] Jeon D-S, Burk DE. A temperature-dependent SOI MOSFET model for high-temperature application (27 C-300 C). Electron Devices, IEEE Transactions on. 1991;38:2101-11.

[39] Ueno S, Furuta H, Okumura Y, Eimori T, Inoue Y. Novel low offset voltage diode using asymmetric threshold voltage MONOS-FET for next generation devices demanding low voltage operation. Electron Devices Meeting, 2002 IEDM'02 International: IEEE; 2002. p. 449-52.

Chapter 4 High-*k* on Germanium and its Passivation Method

Abstract: The high quality gate dielectric is one of the major challenges in realizing Ge CMOS. In this chapter, the thermal grown GeO_2 was used as interfacial passivation layer for high-*k*/Ge gate stack. The oxidation behaviour of Ge by RTO has been investigated for various oxidation conditions in terms of temperatures, times, and gas flow. We have also examined effects of FGA on the physical and electrical properties of the interfacial GeO_2 passivation layer for high-*k*/Ge gate stack formed by RTO. The results show that oxidation temperatures higher than 600 °C lead to GeO_2 surface roughness of 14.5 nm, which can be related to serious GeO desorption. In contrast, the interfacial GeO_2 layers formed at higher temperatures exhibit systematically decreased D_{it} values in both upper and lower-half of the bandgap. Moreover, post-metallisation FGA of the MOS devices shows the potential to reduce the D_{it} values and hysteresis further, which indicates FGA can result in significant reduction of the interface states and compensate the charges inside the oxide.

4.1 Introduction

The traditional scaling of the metal-oxide-semiconductor field-effect transistors (MOSFETs) is experiencing serious difficulties in keeping increasing performance once the transistors are scaled down to sub-22 nm nodes. The physical limitation of the subthreshold slope to 60mV/dec at room temperature makes it difficult to fabricate a transistor with low leakage and high on-current when the supply voltage is reduced below 1V. Alternative channel materials with enhanced carrier transport properties are being considered by the industry. In general, Ge exhibits higher carrier bulk mobility than Si, especially for p-channel devices. Due to carrier velocity saturation at high electric fields, the advantage of Ge mobility is only valid below certain values of electric field at room temperature, which limits the performance of Ge short channel transistors. However, as the transistors enter sub-22nm nodes, Ge can be used in the ultra-short channel MOSFETs exhibiting (quasi-) ballistic transport and in this case the drive current is determined by the carrier injection probability. This probability is related to the mobility at low electric field [1]. Thus, Ge again becomes a very promising channel material and has attracted much attention recently.

4.2 High-*k*/Ge Gate Stack with an Interfacial GeO_2 Passivation Layer formed by Rapid Thermal Oxidation

One of the most challenging issues in establishing Ge CMOS technologies is to realize good Ge dielectric interfaces with a low interface state density (D_{it}), which is critical to achieve low value of the inverse subthreshold slope, high carrier mobility and associated high current drive. Different attempts have been made to form a dielectric layer with low interface states on Ge. They include approaches with various types of interfacial layers such as Si [2, 3], GeO_2 [4-7], oxynitrides [8-11], and different high-k dielectric materials [7, 12-14]. Novel processes have been investigated, i.e. sulphur passivation [13], high pressure thermal oxidation [15, 16], vacuum ultraviolet-assisted oxidation [17], plasma oxidation [18, 19], radical oxidation [20, 21], direct neutral beam oxidation [22] and plasma post-oxidation [14, 23].

Among the different types of proposed MOS systems, GeO_2/Ge interfaces have recently been reported to provide low density interface defects and have been used to create high-performance MOSFETs both experimentally and theoretically [15, 24, 25]. Although, GeO_2 is not a physically stable material as SiO_2, GeO_2/Ge shows the similar bonding constraint as its counterpart SiO_2/Si system in terms of a large spread in bond angle and a random distribution of dihedral angles [26]. Moreover, similar to the high-*k*/Si system which has an interfacial SiO_2 layer, a GeO_2 interfacial layer can be used to maintain a good interface condition for the high-*k*/Ge structure. Thus, GeO_2 has been recently reinvestigated as one of the promising candidates for Ge surface passivation.

High quality GeO_2/Ge interfaces fabricated by both thermal and plasma oxidation have been report recently [5-7, 16, 18, 20, 21, 23]. However, GeO_2 forming using conventional Rapid Thermal Oxidation (RTO) has not been extensively characterized yet. In this chapter, the influences of different oxidation conditions of RTO on both surface morphology and interface properties of thermally grown Metal/Al_2O_3/GeO_2/Ge structures are investigated quantitatively. The behaviour of GeO_2 formation and GeO desorption are discussed as well. The trends of surface morphology evolution of the GeO_2 layer with different oxidation conditions were studied and a baseline process for the growth of GeO_2 using RTO has been estabilished for future device fabrication.

4.3 Experimental Details

In this experiment, (100)-oriented n-type Ge wafers (Sb-doped, nominal ~4×10^{16} cm^{-3}) and (100)-oriented p-type Ge wafers (B-doped, nominal ~7×10^{16} cm^{-3}) were selected for the rapid thermal oxidation and capacitance measurements. Prior to immersion in aqueous HF solution, all Ge surfaces were initially degreased by sequentially rinsing for 1 min each in acetone, methanol, and isopropanol. HF concentration of 5 % in deionized H_2O was used, and the Ge surfaces were subjected to the dilute HF for 3 min, with the solution at room temperature (~ 295 K), to achieve a hydrogen terminated surface. The substrates were immediately delivered into the rapid thermal process tool (Jipelec) within 1 min after removal from the aqueous HF solution and blown dry with N_2. This air exposure was kept as short as possible in an effort to minimize both native oxide regrowth and ambient contamination prior to GeO_2 growth. The RTO of the Ge substrates was performed with various temperatures, oxygen gas flow and times. The surface morphology was characterized by the atomic force microscope (AFM) and scanning electron microscope (SEM) after the thermal process. A transmission electron microscope (TEM) calibrated GeO_2/Ge model is built in the ellipsometer to measure the thickness of the GeO_2 for various conditions of the thermal oxidation [27]. In order to evaluate the GeO_2/Ge interface quality, the Metal-Oxide-Semiconductor (MOS) structures of the metal/Al_2O_3/GeO_2/Ge stack were fabricated. An Al_2O_3 layer (nominal thickness 7.5 nm) was grown by Atomic layer deposition (ALD) on top of GeO_2 to prevent the water absorption or dissolution of GeO_2 in water. 150 nm thick gate contacts were formed by e-beam evaporation consisting of Ti (60 nm), Pt (50 nm) and Au (40 nm), through a lift-off process. For comparative purposes across all samples, the electrical tests were performed on capacitors with a nominal diameter of 50 μm, and in order to rule out variation due to any differences in the masks used for metal deposition, the actual dimensions of the test devices were measured using an optical microscope for all samples.

Multi-frequency capacitance-voltage (C-V) and conductance-voltage (G-V) measurements were recorded using an Agilent B1500 semiconductor analyzer with C-V module. The measurements were performed at room temperature on-wafer in a microchamber probe station (Cascade Microtech, model Summit 12971B) in a dry air, dark environment. The measurements were carried out before and after 30 minutes

FGA, which consists of 5% H_2 and 95% N_2 at 300 °C. Multiple sites were examined in all cases to ensure the results are representative of device behavior. It is also noted that larger and smaller device areas were measured on all samples and the capacitance scaled as expected with area.

4.4 Results and Discussion

Ge posseses a complex native oxide consisting of different types of GeO_x according to different oxidation conditions and methods. It can form 1+, 2+, 3+ and 4+ oxidation states which have been assigned to the surface atoms bonded to 1, 2, 3 and 4 oxygen atoms. Unlike Si, besides the completely oxidized GeO_2 (4+) and half oxidized GeO (2+) are chemical stable states, the other states (1+, 3+) that form in the transit region may generate dangling bonds causing large interface states densities. These incomplete bonding states are due to a lack of thermal energy or activated oxygen that prevents them to be transformed into more chemical stable GeO or GeO_2 . On ther other hand, the GeO formed in GeO_2 or GeO_2/Ge interface can desorb in gas form (Eq. 1). As a result, the GeO_2/Ge interface control is thermodynamically difficult and GeO desorption leads to a critical deterioration of the interface properties and, hence, an increase of D_{it} [29].

$$GeO_2(s) + Ge(s) = 2GeO(g) \tag{1}$$

4.4.1 Surface Morphology of Thermally Growth GeO_2

In order to observe the oxidation behaviour of RTO, the surface morphology of GeO_2 layers was investigated using an AFM for various oxidation conditions. It can be expected that the roughness of the GeO_2 layer formed by RTO may increase when GeO desorbs from either the GeO_2 layer or the GeO_2/Ge interface [30]. Thus, the surface roughness can be an indication of desorption issues.

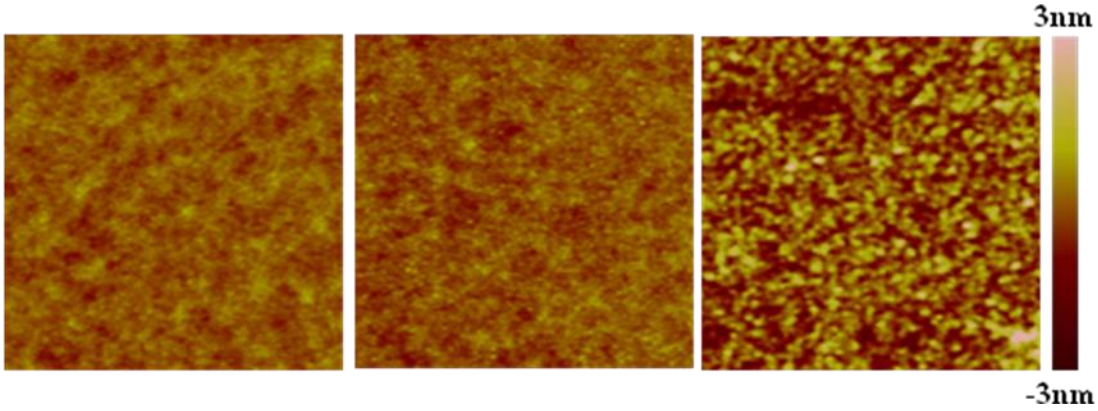


Figure 4.1 Atomic Force Microscopy images of the GeO_2 passivation layers grown by RTO after wet chemical cleaning at (a) 450 ºC, (b) 500 ºC and (c) 550 ºC, respectively.

Figure 4.1 shows the AFM images of GeO_2 layers formed by RTO with the temperatures ranging from 450 °C to 550 °C. The Root Mean Square Roughness (RMS or Rq) of GeO_2 surface is 0.27 nm, 0.35 nm and 0.81 nm for the oxidation temperatures of 450 °C, 500 °C and 550 °C, respectively. It can be noted that although all the RMS roughness is below 1 nm for these three temperatures, the RMS roughness more than doubled when temperature changes from 500 °C to 550 °C which may indicate that strong desorption occurs around this temperature range.

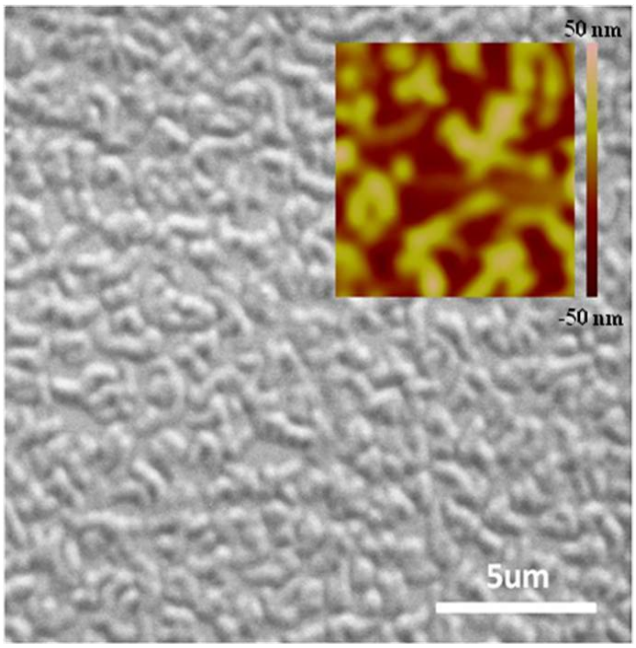


Figure 4.2 Scanning Microscopy image of the GeO_2 passivation layer grown by RTO at 600 ºC. Inset: AFM image of the GeO_2 layer.

Figure 4.2 shows the SEM and AFM images of GeO_2 layer formed by RTO at 600°C. Worm-like morphology can be observed on the surface and the RMS roughness is drastically increased up to 14.5 nm. This suggests that GeO was volatilized intensively during thermal oxidation around 600°C. This GeO_2 layer has a large variation in thickness and is thus not suitable for device fabrication anymore. In order to summarize the surface conditions of the GeO_2 layers grown under various oxygen flow rates, oxidation times and temperatures, the RMS roughness of GeO_2 layer is plotted in Figure 4.3.

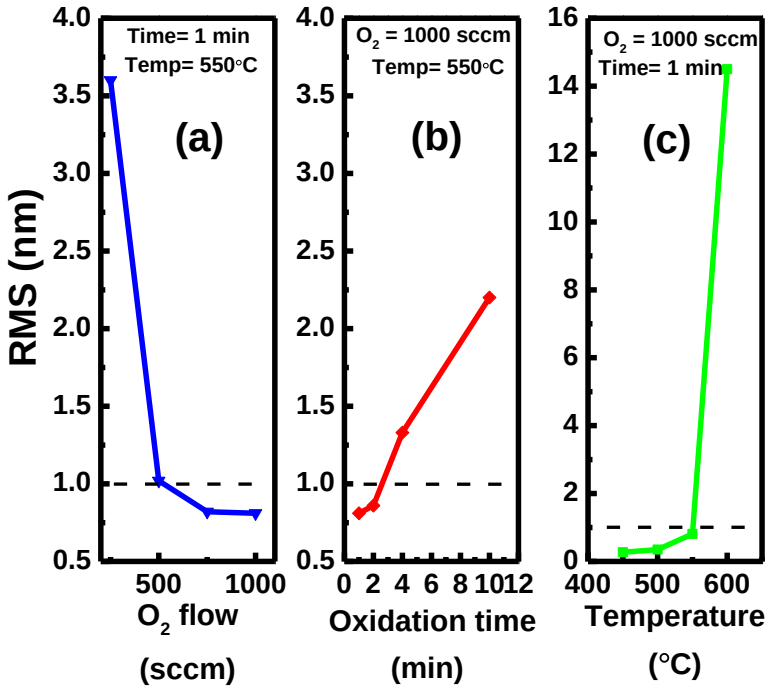


Figure 4.3 (a) Surface roughness of GeO_2 layers for various O_2 gas flow associated with oxidation temperature of 550 °C and oxidation time of 1 minute. (b) Surface roughness of GeO_2 layers for various oxidation times associated with oxidation temperature of 550 °C and O_2 gas flow of 1000 sccm. (c) Surface roughness of GeO_2 layers for various oxidation temperatures associated with oxidation time of 1minute and O_2 gas flow of 1000 sccm.

4.4.2 Oxidation Rate of Ge Substrate

In Figure 4.3(a), the temperature was set to 550 °C and oxidation time is 1 minute. The RMS roughness larger than 1 nm can be observed when the oxygen flow rates are smaller 750 sccm. This can be explained as insufficient and incomplete oxidation rather than a GeO desorption across the surface as not enough oxygen is supplied. In Figure

4.3(b), the temperature was set to 550 °C and oxygen flow rate was 1000 sccm. The RMS roughness larger than 1 nm can be observed when the oxidation time is more than around 3 minutes. Similar results of desorption dependence on time was observed by Wang *et. al*. [30]. Their results show a peak of GeO desorption appears after several minutes of annealing which can represent here as the RMS roughness dramatically increases. It is also noted that even at a temperature which supposes not enough to trigger GeO desorption at the very beginning, the RMS roughness of GeO_2 could increase after certain time range. In Figure 4.3(c), the oxygen flow rate was set to 1000 sccm and oxidation time for 1 minute. The RMS roughness is below 1 nm when the temperature ranges from 450 °C to 550 °C and there is an abrupt increase when temperature reaches up to 600 °C, which corresponding to the AFM and SEM images in Figure 4.1 and Figure 4.2, respectively.

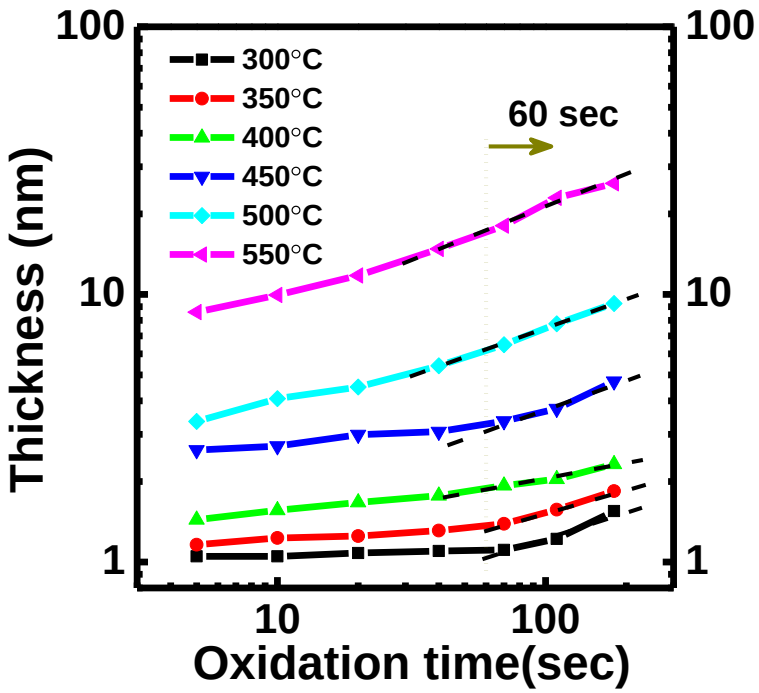


Figure 4.4 Thickness of GeO_2 grown by RTO as a function of oxidation time in logarithm scale at oxidation temperatures ranging from 300 °C up to 550 °C.

To obtain an insight into the behaviour of GeO_2 growth by RTO, GeO_2 thickness as a function of oxidation time in logarithmic scale for temperatures ranging from 300 °C up to 550 °C is shown in Figure 4.4. At low oxidation temperatures up to 400 °C, it exhibits a linear relationship in logarithmic scale after 60 seconds oxidation. On the other hand, for higher oxidation temperatures, this linear relationship in logarithmic

scale occurs earlier. This can be explained as higher temperatures offer sufficient energy for oxygen to diffuse through the native oxide layer which is blocking the oxygen diffusion and thus the linear relationship occurs earlier.

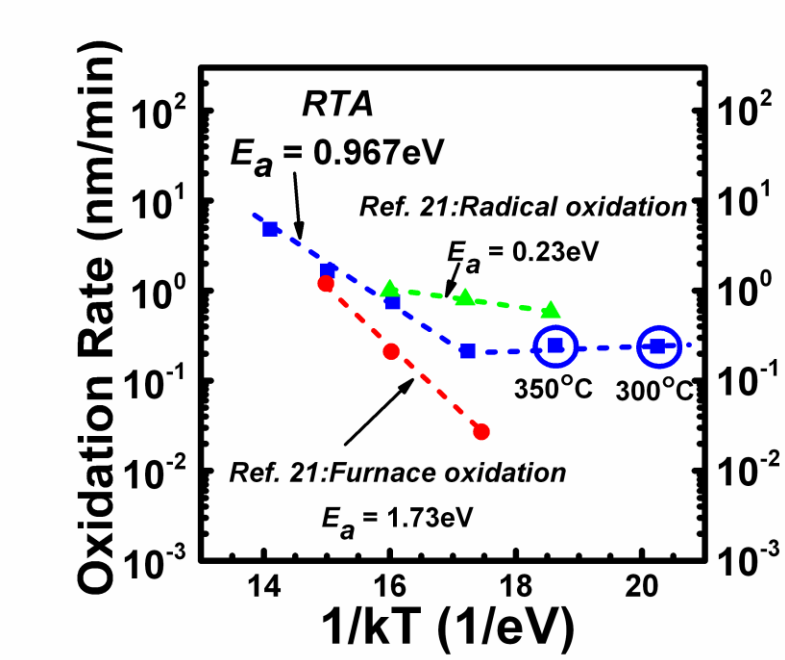


Figure 4.5 The oxidation rate as a function of the inverse of oxidation temperature.

To analyze the oxidation mechanism, the measured oxidation rates were plotted as a function of $1/kT$ in Figure 4.5. The oxidation activation energy can be extracted from the Arrhenius curves. The activation energy for RTO is approximately 0.976 eV at temperature higher than 400 °C, which is smaller than that of furnace oxidation (1.73 eV), but larger than that of the radical oxidation (0.23 eV) reported by Kobayashi *et al.* [21]. It indicates that the oxidation rate of RTO is less temperature dependent than that of furnace oxidation. However, it shows higher temperature dependence than the radical oxidation. The activation energy of RTO infers that either higher reactivity of oxygen molecules or the more efficient transformation of thermal energy to the Ge surface is achieved by RTO than by furnace oxidations. It is also noted in Figure 4.3 that the Arrhenius curve of RTO can be split into two parts. For oxidation temperatures less than 400 °C, the oxidation rates exhibit almost a consistent value of 0.24 nm/min and show almost no temperature dependence. The reason for this behaviour is still not clear and further investigation is needed.

4.4.3 Capacitance-Voltage Response of the MOS Structure with $Al_2O_3/GeO_2/Ge$ Gate Stacks at Room Temperature

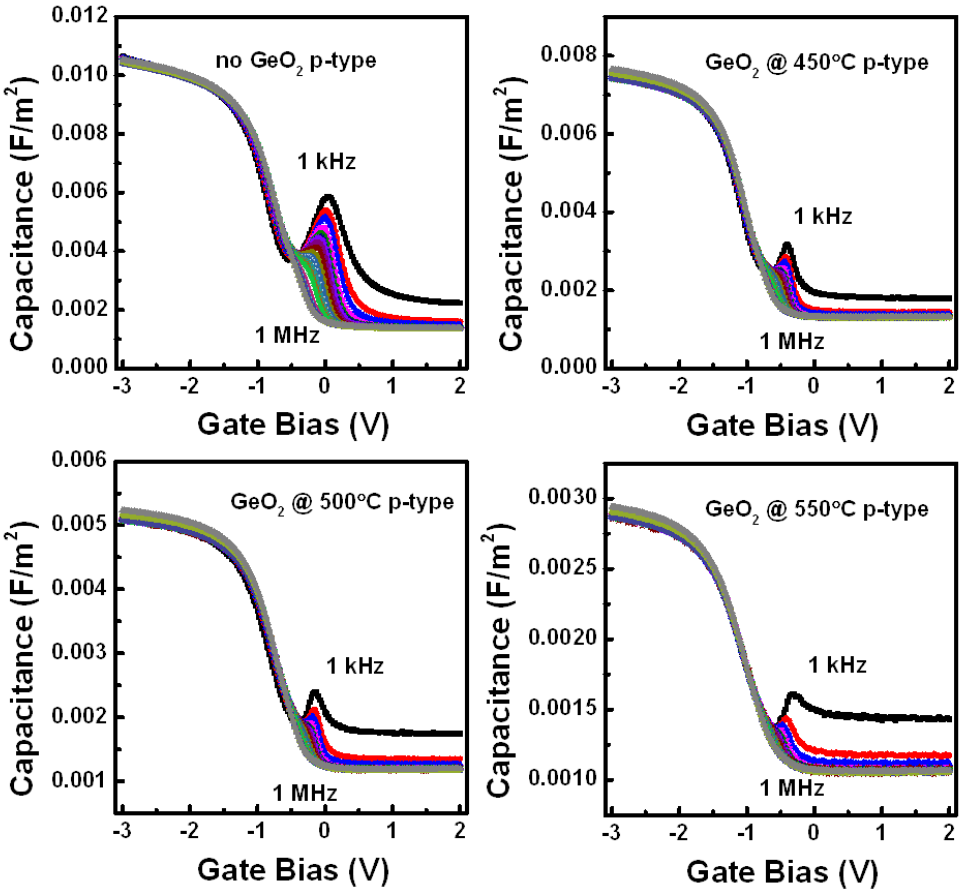


Figure 4.6 Room temperature multi-frequency C-V (1kHz to 1MHz) of Metal/Al_2O_3/GeO_2/p-Ge gate stacks (a) without GeO_2 passivation layer, (b) with GeO_2 grown at oxidation temperature of 450 °C, (c) with GeO_2 grown at oxidation temperature of 500 °C and (d) with GeO_2 grown at oxidation temperature of 550 °C

In the second part of the experiments, capacitance-voltage (C-V) and conductance-voltage (G-V) characterization of MOS device structures was performed. Multi-frequency dispersion over the bias range examined occurs for both n-type and p-type Ge samples before and after FGA. The C-V response at room temperature (295 K) with ac signal frequencies from 1 kHz to 1 MHz for the p-type samples without GeO_2, and with the 450 °C, 500°C, and 550°C oxidized surfaces associated with FGA are shown in Figure 4.6(a)-(d), respectively. For all p-type samples frequency dispersion is observed, with a peak response in the depletion and weak inversion region. A significant difference in the C-V responses has been observed between the sample without the

GeO_2 passivation layer (Figure 4.6(a)) and the thermally oxidized samples (Figure 4.6(b)-(d)). The C-V response is noticeably improved for the latter samples and reduced responses are observed for the interface state related capacitance in terms of the peak magnitude and width in Figure 4.6(b)-(d).

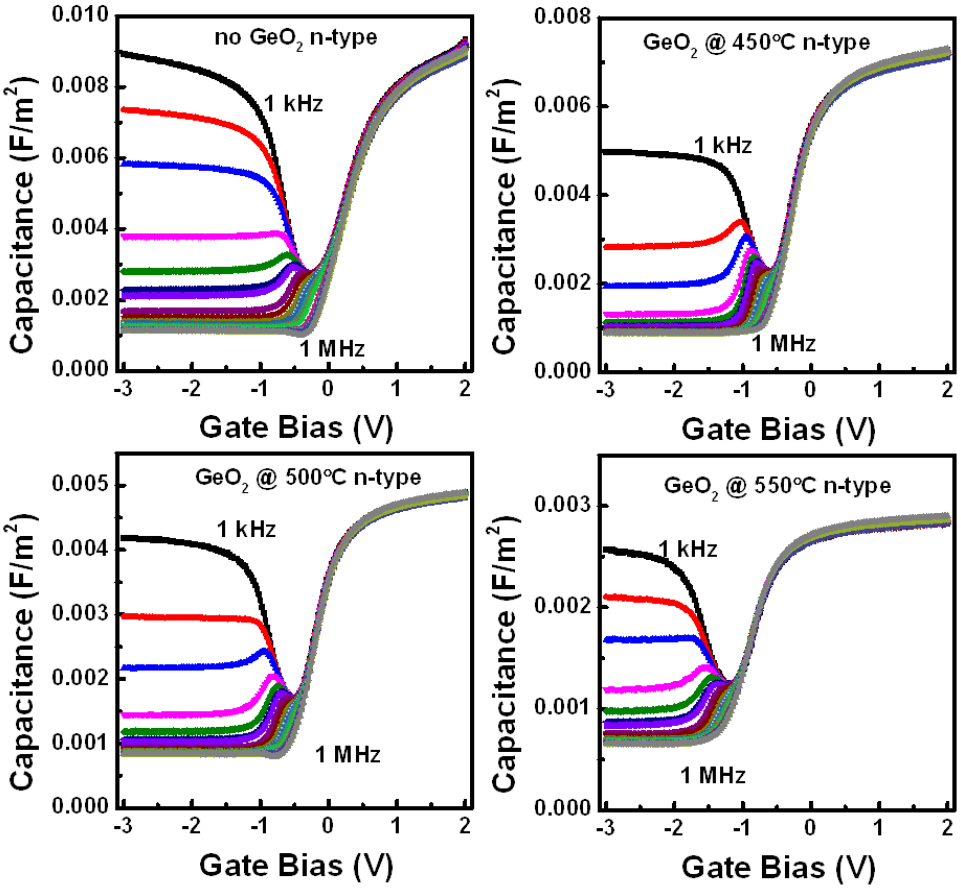


Figure 4.7 Room temperature multi-frequency C-V (1kHz to 1MHz) of Metal/Al_2O_3/GeO_2/n-Ge gate stacks (a) without GeO_2 passivation layer, (b) with GeO_2 grown at oxidation temperature of 450 °C, (c) with GeO_2 grown at oxidation temperature of 500 °C and (d) with GeO_2 grown at oxidation temperature of 550 °C

The C-V response at room temperature (295 K) with ac signal frequencies from 1 kHz to 1 MHz for the n-type samples without GeO_2, and with the 450 °C, 500°C, and 550°C oxidized surfaces associated with FGA are shown in Figure 4.7(a)-(d), respectively. The C-V response related to a minority carrier contribution is clearly observed in all cases (see Figure 4.7(a)-(d)). This is characteristic of true inversion at the GeO_2/Ge interface, which results in a constant capacitance as a function of V_{GATE}, where the magnitude of this constant capacitance region increases with increasing temperature or decreasing frequency up to a maximum value defined by the oxide

capacitance (C_{ox}) [31]. Unlike the case for the p-type samples, the clear minority carrier C-V response makes it more difficult to distinguish between interface defects and a minority carrier contribution using only C-V responses. Therefore the high-low frequency method is not suitable to extract D_{it} in this case. The total capacitances per area of the bilayer GeO2 and Al2O3 are calculated by the bilayer thicknesses calibrated by TEM data and fitting value of ε_{GeO2} , ε_{Al2O3} as listed in Table 4.1.

Oxidation Temp	ε_0 (Fm^{-1})	ε_{GeO2} (1)	ε_{Al2O3} (1)	T_{GeO2} (nm)	T_{Al2O3} (nm)	C_{GeO2} (F)	C_{Al2O3} (F)	C_{Total}/m^2 (F/m^2)
0 °C	8.85×10^{-12}	5.5	9	0	7.5	0	1.06×10^{-11}	1.06×10^{-2}
450 °C	8.85×10^{-12}	5.5	9	1.316	7.5	3.70×10^{-11}	1.06×10^{-11}	8.25×10^{-3}
500 °C	8.85×10^{-12}	5.5	9	4.66	7.5	1.05×10^{-11}	1.06×10^{-11}	5.27×10^{-3}
550 °C	8.85×10^{-12}	5.5	9	9.954	7.5	4.89×10^{-12}	1.06×10^{-11}	3.35×10^{-3}

Table 4.1 Fitted capacitance and oxide thicknesses for bilayer GeO_2 and Al_2O_3 gate stack grown at different Ge oxidation temperatures. ε_0 is the electric constant; ε_{GeO2} , ε_{Al2O3} are the relative static permittivity (sometimes called the dielectric constant) of GeO_2 and Al_2O_3, respectively; T_{GeO2}, T_{Al2O3} are the thicknesses of the GeO_2 and Al_2O_3 layers, respectively.

4.4.4 D_{it} Extraction of the Gate Stacks

In order to estimate D_{it} for both p-type and n-type Ge and evaluate the influence of oxidation temperatures on the interface, the conductance method as discussed in Nicollian and Brews' work was used [32]. The conductance method at low temperature was used in many papers because the lower measurement temperature allows one to evaluate D_{it} at energies closer to the conduction and valence band edges [5]. However, the reduced temperature has a possibility to suppress the D_{it} contribution to the measured CV and GV responses also. The low temperature measurements do not account for the entire D_{it} that can respond at room temperature and hence the D_{it} can possibly be underestimated [33]. Thus, the method used here to extract the D_{it} is the standard approach of the conductance method, although it may include a conductance contribution by the minority carrier generation-recombination even in weak inversion. The equivalent parallel conductance (G_p/ω) is estimated from the measured conductance

(G_m), and measured capacitance (C_m) against voltage sweep, using Eq. (2) below, where ω is the fixed angular frequency, and C_{ox} is the oxide capacitance [32]. Most of the C-V responses show the accumulation capacitance is very close to the expected C_{ox}, except for the n-type sample without RTO. The C_{ox} values were calculated using the Al_2O_3 (dielectric constant, k=9) and GeO_2 (k=5.5) thickness determined by TEM and checked by the accumulation capacitance in actual measurements. The equivalent parallel conductance, G_p, was converted to peak interface state density using the approximation in Eq. (3), which assumes zero deviation in surface potential band bending, and where q is the electron charge

$$(\frac{G_p}{\omega}) = \frac{\omega C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2}, \tag{2}$$

$$D_{it} = (\frac{G_p}{\omega})_{fp} \times (\frac{1}{0.4 \times q}). \tag{3}$$

p and n-type substrates were used for the D_{it} calculation in the lower half and upper half of the bandgap, respectively. The surface potential at each gate voltage was determined from capacitance values at 1 MHz by fitting them with theoretical C-V curves.

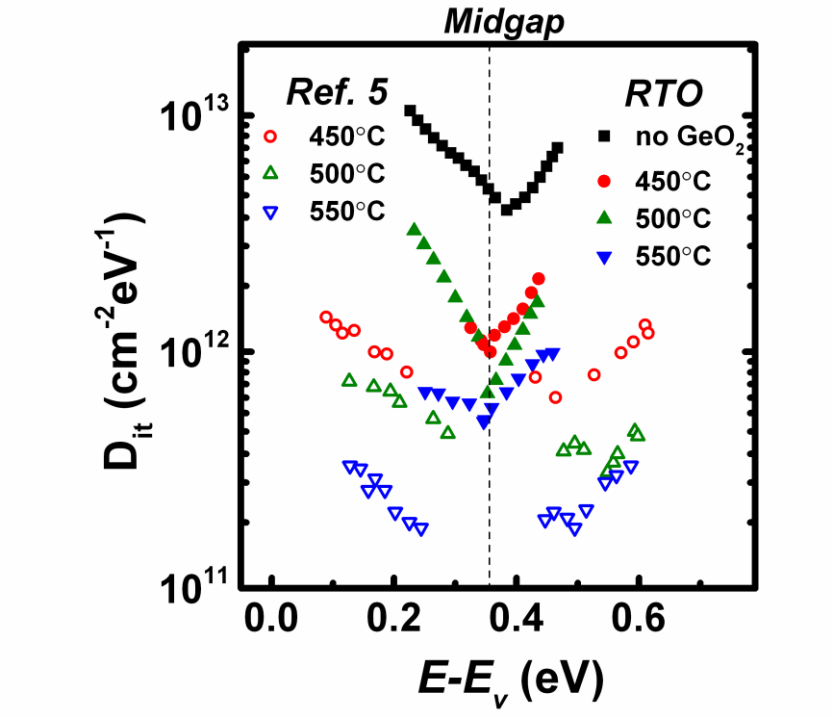


Figure 4.8 Energy distribution of the interface state density (D_{it}) for GeO_2/Ge interfaces before FGA, measured by the room temperature conductance method. N-type and P-type substrates

were used for D_{it} measurement in the upper-half and the lower-half of the bandgap, respectively. Results from Ref. 5 were plotted for comparison.

Figure 4.8 shows the oxidation temperature dependence of the D_{it} distribution extracted by room temperature conductance method of the Metal/Al_2O_3/(GeO_2)/Ge structures before FGA. The D_{it} distribution extracted by low temperature conductance method as reported in ref. 5 was plotted as well for comparison. It is found that the GeO_2 passivation layer formed by RTO dramatically reduces the interface state density compared to the Metal/Al_2O_3/Ge structures without GeO_2 layer. Closer to the valence band edges D_{it} appears to decrease by more than an order of magnitude for RTO at 550 °C, from $1.0\times10^{13}/cm^2$ to $6.8\times10^{11}/cm^2$ at 0.23 eV and 0.251 eV from the valence band edge, respectively. A similar reduction was observed in the upper-half of the bandgap. As for the GeO_2 layer formed at 550 °C, it shows a minimum D_{it} value of $5.1\times10^{11}/cm^2$ measured in the range from the valence band edge to midgap and $5.8\times10^{11}/cm^2$ measured in the range from the conduction band edge to midgap.

The D_{it} decreases as the oxidation temperature increases which shows the same trend as in ref. 5. It can be noted that the D_{it} level in ref. 5 is marginally lower than the D_{it} extracted in our experiments, possibly due to D_{it} extraction being performed in that case at lower temperature, which may result in the D_{it} response being partially frozen out at low temperature. In our experiment, it is also noted that due to the observation of a minority carrier response for n type samples, the conductance may have partial contributions from the minority carrier response, resulting in the D_{it} values being overestimated. However, for the purpose of examining the effect of oxidation temperatures and FGA on the high-*k*/Ge system in the current study, it is noted that the D_{it} values extracted in this work provide a valuable qualitative comparison between the samples rather than providing an absolute quantitative estimate of the D_{it} levels in these Ge devices.

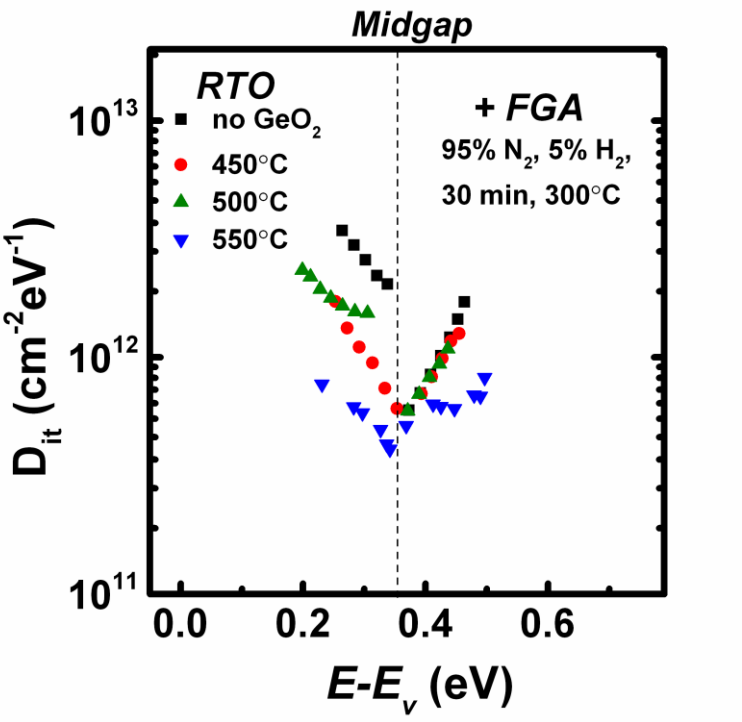


Figure 4.9 Energy distribution of the interface state density (D_{it}) for GeO_2/Ge interfaces after FGA, measured by the room temperature conductance method.

A significant reduction in D_{it} is observed after FGA especially for the Metal/Al_2O_3/Ge structures without a GeO_2 passivation layer. Figure 4.9 shows the D_{it} distribution in the bandgap after FGA. D_{it} values of both p and n-type Ge substrates decrease after FGA for all oxidation temperatures and it is also noted that the D_{it} distribution almost overlaps for n-type Ge, which indicates FGA has a strong effect on reducing the D_{it} in the upper-half of the bandgap from conduction band edge towards midgap. The minimum D_{it} values detected after FGA have reduced to $4.1\times10^{11}/cm^2$ and $5.2\times10^{11}/cm^2$ in the lower-half and upper-half of the bandgap near the midgap, respectively.

4.4.5 Hysteresis of the Gate Stack

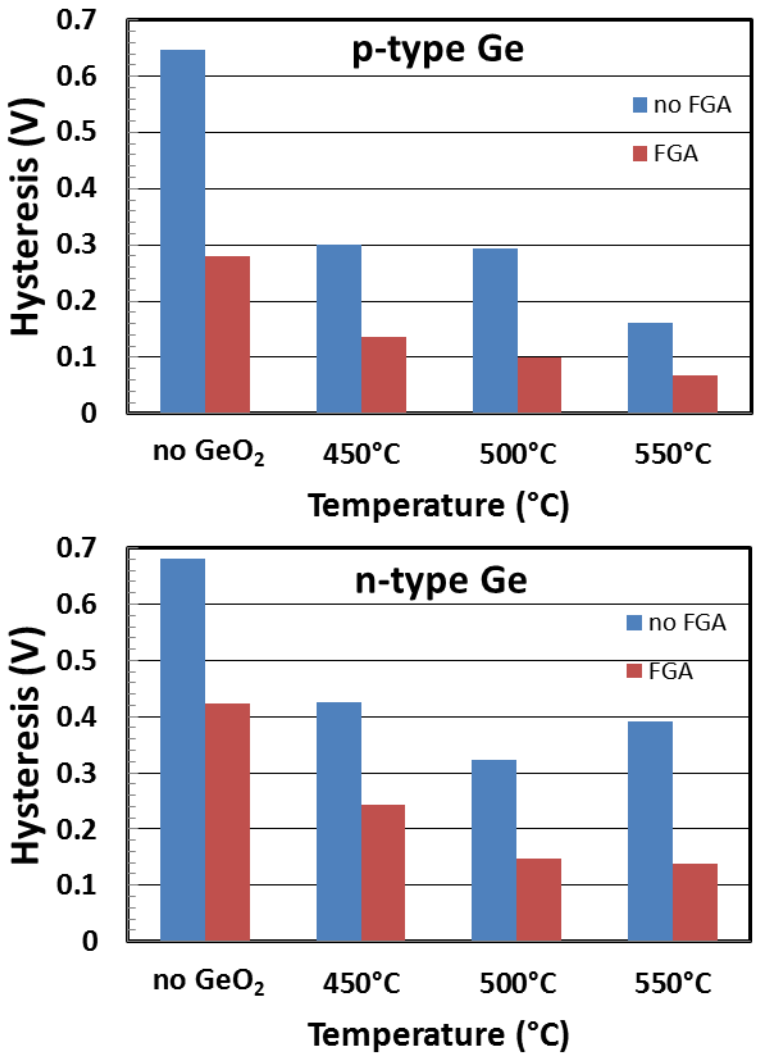


Figure 4.10 Hysteresis measured at mid-capacitance at 100 kHz before and after FGA for all the temperatures oxidized (a) p-type and (b) n-type samples. The hysteresis measurements were performed by sweeping from negative to positive gate bias for n-type devices (-3.0 to 3.0 V), and from positive to negative gate bias for p-type devices (3.0 to -3.0 V). There was no hold time in accumulation, and two consecutive sweeps were performed.

It is observed that a hysteresis loop in the C-V response occurs for both p and n-type Ge samples before and after FGA for both high and low frequencies. This effect has been systematically studied by Oniki *et al.* and they related this effect to the anomalous positive charge in the GeO_2 film generated by electron emission from water-related donor-like traps above the Ge Fermi-level [34]. In order to quantitatively estimate the effect of FGA on the hysteresis, the voltage shifts at the mid-capacitance, which is determined as halfway between the maximum and minimum capacitance measured at 100 kHz, were plotted before and after FGA for both p and n-type samples

in Figure 4.10. It is noted that FGA can noticeably reduce the hysteresis of both p and n-type samples. Moreover, the higher oxidation temperature associated with FGA results in a trend of lower hysteresis. The hysteresis has been explained in relation to the process conditions, such as exposure time after oxidation, and the amount of positive charge can be controlled by the amount of water molecules in the GeO_2 film [34]. Thus, the FGA can possibly evaporate off the water molecules and eliminate the charges in the GeO_2 film, which leads to a reduction of hysteresis for both p and n-type samples.

4.5 Conclusions

In summary, we have examined effects of FGA on the physical and electrical properties of the interfacial GeO_2 passivation layer for high-*k*/Ge gate stack formed by RTO. The oxidation behaviour of Ge by RTO has been investigated for various oxidation conditions in terms of temperatures, times, and gas flow. The results show that oxidation temperatures higher than 600 °C lead to GeO_2 surface roughness of 14.5 nm, which can be related to serious GeO desorption. In contrast, the interfacial GeO_2 layers formed at higher temperatures exhibit systematically decreased D_{it} values in both upper and lower-half of the bandgap. Moreover, post-metallisation FGA of the MOS devices shows the potential to reduce the D_{it} values and hysteresis further, which indicates FGA can result in significant reduction of the interface states and compensate the charges inside the oxide.

4.6 References

[1] Lundstrom M. Elementary scattering theory of the Si MOSFET. IEEE Electr Device L. 1997;18:361-3.

[2] Wu N, Zhang QC, Zhu CX, Chan DSH, Li MF, Balasubramanian N, et al. Alternative surface passivation on germanium for metal-oxide-semiconductor applications with high-*k* gate dielectric. Appl Phys Lett. 2004;85:4127-9.

[3] De Jaeger B, Bonzom R, Leys F, Richard O, Van Steenbergen J, Winderickx G, et al. Optimisation of a thin epitaxial Si layer as Ge passivation layer to demonstrate deep sub-micron n- and p-FETs on Ge-On-insulator substrates. Microelectron Eng. 2005;80:26-9.

[4] Jack MD, Lee JYM, Lefevre H. Dlts Measurements of a Germanium M-I-S Interface. J Electron Mater. 1981;10:571-89.

[5] Matsubara H, Sasada T, Takenaka M, Takagi S. Evidence of low interface trap density in GeO_2/Ge metal-oxide-semiconductor structures fabricated by thermal oxidation. Appl Phys Lett. 2008;93.

[6] Sasada T, Nakakita Y, Takenaka M, Takagi S. Surface orientation dependence of interface properties of GeO_2/Ge metal-oxide-semiconductor structures fabricated by thermal oxidation. J Appl Phys. 2009;106.

[7] Delabie A, Bellenger F, Houssa M, Conard T, Van Elshocht S, Caymax M, et al. Effective electrical passivation of Ge(100) for high-k gate dielectric layers using germanium oxide. Appl Phys Lett. 2007;91.

[8] Chui CO, Ito F, Saraswat KC. Nanoscale germanium MOS dielectrics - Part I: Germanium oxynitrides. IEEE T Electron Dev. 2006;53:1501-8.

[9] Chui CO, Ito F, Saraswat KC. Scalability and electrical properties of germanium oxynitride MOS dielectrics. IEEE Electr Device L. 2004;25:613-5.

[10] Shang HL, Lee KL, Kozlowski P, D'Emic C, Babich I, Sikorski E, et al. Self-aligned n-channel germanium MOSFETs with a thin Ge oxynitride gate dielectric and tungsten gate. IEEE Electr Device L. 2004;25:135-7.

[11] Xu JP, Lai PT, Li CX, Zou X, Chan CL. Improved electrical properties of germanium MOS capacitors with gate dielectric grown in Wet-NO ambient. IEEE Electr Device L. 2006;27:439-41.

[12] Chui CO, Kim H, Chi D, McIntyre PC, Saraswat KC. Nanoscale germanium MOS dielectrics - Part II: High-kappa gate dielectrics. IEEE T Electron Dev. 2006;53:1509-16.

[13] Frank MM, Koester SJ, Copel M, Ott JA, Paruchuri VK, Shang HL, et al. Hafnium oxide gate dielectrics on sulfur-passivated germanium. Appl Phys Lett. 2006;89.

[14] Zhang R, Iwasaki T, Taoka N, Takenaka M, Takagi S. Al_2O_3/GeO_x/Ge gate stacks with low interface trap density fabricated by electron cyclotron resonance plasma postoxidation. Appl Phys Lett. 2011;98.

[15] Toriumi A, Tabata T, Lee CH, Nishimura T, Kita K, Nagashio K. Opportunities and challenges for Ge CMOS - Control of interfacing field on Ge is a key. Microelectron Eng. 2009;86:1571-6.

[16] Lee CH, Nishimura T, Nagashio K, Kita K, Toriumi A. High-Electron-Mobility Ge/GeO_2 n-MOSFETs With Two-Step Oxidation. IEEE T Electron Dev. 2011;58:1295-301.

[17] Craciun V, Boyd IW, Hutton B, Williams D. Characteristics of dielectric layers grown on Ge by low temperature vacuum ultraviolet-assisted oxidation. Appl Phys Lett. 1999;75:1261-3.

[18] Fukuda Y, Ueno T, Hirono S, Hashimoto S. Electrical characterization of germanium oxide/germanium interface prepared by electron-cyclotron-resonance plasma irradiation. Jpn J Appl Phys 1. 2005;44:6981-4.

[19] Xie Q, Deduytsche D, Schaekers M, Caymax M, Delabie A, Qu XP, et al. Effective Electrical Passivation of Ge(100) for HfO_2 Gate Dielectric Layers Using O^{-2} Plasma. Electrochem Solid St. 2011;14:G20-G2.

[20] Johnson RS, Niimi H, Lucovsky G. New approach for the fabrication of device-quality $Ge/GeO_2/SiO_2$ interfaces using low temperature remote plasma processing. J Vac Sci Technol A. 2000;18:1230-3.

[21] Kobayashi M, Thareja G, Ishibashi M, Sun Y, Griffin P, McVittie J, et al. Radical oxidation of germanium for interface gate dielectric GeO_2 formation in metal-insulator-semiconductor gate stack. J Appl Phys. 2009;106.

[22] Wada A, Zhang R, Takagi S, Samukawa S. High-quality germanium dioxide thin films with low interface state density using a direct neutral beam oxidation process. Appl Phys Lett. 2012;100.

[23] Zhang R, Iwasaki T, Taoka N, Takenaka M, Takagi S. High-Mobility Ge pMOSFET With 1-nm EOT Al_2O_3/GeO_x/Ge Gate Stack Fabricated by Plasma Post Oxidation. IEEE T Electron Dev. 2012;59:335-41.

[24] Nishimura T, Lee CH, Tabata T, Wang SK, Nagashio K, Kita K, et al. High-Electron-Mobility Ge n-Channel Metal-Oxide-Semiconductor Field-Effect Transistors with High-Pressure Oxidized Y_2O_3. Appl Phys Express. 2011;4.

[25] Houssa M, Pourtois G, Caymax M, Meuris M, Heyns MM, Afanas'ev VV, et al. Ge dangling bonds at the (100) Ge/GeO_2 interface and the viscoelastic properties of GeO_2. Appl Phys Lett. 2008;93.

[26] Lucovsky G, Wu Y, Niimi H, Misra V, Phillips JC. Bonding constraints and defect formation at interfaces between crystalline silicon and advanced single layer and composite gate dielectrics. Appl Phys Lett. 1999;74:2005-7.

[27] Hu YZ, Zettler JT, Chongsawangvirod S, Wang YQ, Irene EA. Spectroscopic Ellipsometric Measurements of the Dielectric Function of Germanium Dioxide Films on Crystal Germanium. Appl Phys Lett. 1992;61:1098-100.

[28] Schmeisser D, Schnell RD, Bogen A, Himpsel FJ, Rieger D, Landgren G, et al. Surface Oxidation-States of Germanium. Surf Sci. 1986;172:455-65.

[29] Kita K, Suzuki S, Nomura H, Takahashi T, Nishimura T, Toriumi A. Direct evidence of GeO volatilization from GeO_2/Ge and impact of its suppression on GeO_2/Ge metal-insulator-semiconductor characteristics. Jpn J Appl Phys. 2008;47:2349-53.

[30] Wang SK, Kita K, Lee CH, Tabata T, Nishimura T, Nagashio K, et al. Desorption kinetics of GeO from GeO_2/Ge structure. J Appl Phys. 2010;108.

[31] Wadsworth HJ, Bhattacharya S, McNeill DW, Ruddell FH, Armstrong BM, Gamble HS, et al. Germanium MOS capacitors with hafnium dioxide and silicon dioxide dielectrics. Mat Sci Semicon Proc. 2006;9:685-9.

[32] Streetman BG. Mos (Metal-Oxide Semiconductor) Physics and Technology - Nicollian,Eh, Brews,Jr. Am Sci. 1983;71:549-.

[33] Engel-Herbert R, Hwang Y, Stemmer S. Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces. J Appl Phys. 2010;108.

[34] Oniki Y, Ueno T. Water-Related Hole Traps at Thermally Grown GeO_2-Ge Interface. Jpn J Appl Phys. 2012;51.

Chapter 5 Germanium JNT: From Substrate to Device

Abstract: In this chapter, Germanium-on-Insulator (GeOI) wafers were fabricated using Smart-Cut with low temperature direct wafer bonding method. A Preferential etch solvent was developed and used to decorate the defects on Ge during the GeOI fabrication. For the lithography and pattern transfer, a top-down process of sub-50-nm width Ge nanowires is developed in this chapter and Ge nanowires with 35 nm width and 50 nm depth are obtained using this process. With the developed modules, JNT with Ge channels have been fabricated by the CMOS-compatible top-down process. The transistors exhibit the lowest subthreshold slope to date for Ge junctionless devices. The devices with a gate length of 3 μm exhibit a *SS* of 216 mV/dec with an I_{ON}/I_{OFF} current ratio of 1.2×10^3 at V_D = -1 V and *DIBL* of 87 mV/V.

5.1 Fabrication of Germanium-on-Insulator by Low Temperature Direct Wafer Bonding

5.1.1 Introduction

Ge is a semiconductor element from Group IV of the periodic table like Si which also has a diamond-like crystal structure. The first transistor was a germanium device fabricated by Bell Telephone Laboratories (BTL) in 1947 [1]. M. M. Atalla and his group at BTL stabilized a Si surface by thermally growing a SiO_2 film on it in 1957. They had been systematically investigating the Si/SiO_2 interface and reduced the density of surface states by several orders of magnitude [2]. This method made silicon dominant semiconductor material since the middle 1960s [3]. However, as the dimensions of the MOS transistors were reduced, the SiO_2 layer performing as a gate dielectric needs to be scaled down below 2 nm. As gate tunneling current became unacceptable for SiO_2, the introduction of new materials with higher permittivity (high-*k*) was necessary. The relationship between Si and SiO_2 was broken by depositing high-k materials as gate dielectric and this brought Ge back into focus. Furthermore the degradation in performance of Si MOS devices by fundamental material limitations is also forcing the semiconductor industry to consider extraordinary materials and Ge is a promising candidate. Bulk Ge wafer driven by the solar cell industry for space applications was already available as large as 300 mm with good quality [4]. However,

the MOS devices in a bulk Ge suffer a fatal leakage current due to the lower bandgap which could be overcome by using a Germanium-on-Insulator (GeOI) substrate. Although several methods to fabricate GeOI substrate are available including heteroeptaxial growth [5], condensation technique [6] and Smart-Cut^{TM} technology, commercial GeOI substrates are not commonly available in the market. Here we demonstrate a Smart-Cut^{TM} method to fabricate GeOI wafer which has been intensively used for Silicon-on-Insulator (SOI) fabrication. Low thermal budget was used in order to reduce the stress in the interface of two materials with dissimilar thermal expansion coefficients.

5.1.2 Fabrication GeOI Wafer by Smart-Cut Technology

GeOI wafers are fabricated using low temperature direct wafer bonding method with the process flow as shown in Figure 5.1. A hydrogen implanted Ge donor wafer is bonded to a thermally oxided Si handle wafer with in-situ oxygen radical activation before bonding in a vacuum chamber. Ex-situ anneals were used to enhance the bond strength or exfoliate the implanted Ge wafer. The insight into the exfoliation mechanism of the hydrogen implanted Ge wafer was observed by the high resolution transmission electron microscopy (HRTEM). The Ge surface after radical activation was analyzed by Angle-Resolved X-ray Photoelectron spectroscopy (APXPS). Scanning electron microscopy (SEM) was used to characterize the exfoliated Ge surface on handle SiO_2 film.

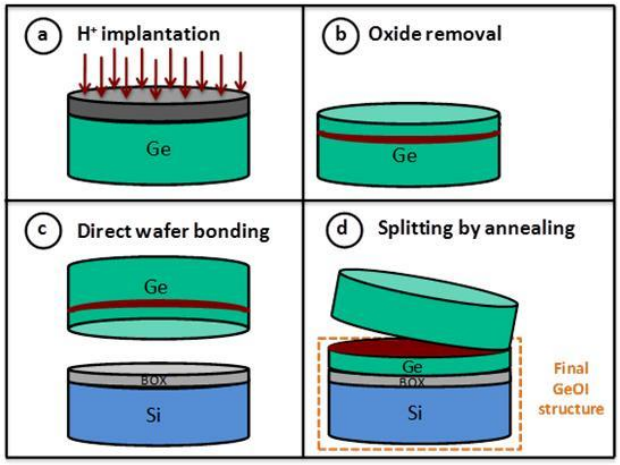


Figure 5.1: Process flow of GeOI wafer fabrication by Smart-Cut^{TM} technology. (a) H^+ implantation into the Ge wafer with protection SiO_2 on top (b) protection oxide removed (c) low temperature direct wafer bonding to the handle wafer (d) Ge wafer exfoliation by annealing.

5.1.3 Experimental

In the experiment, 4 inch 100-orientated n-type Ge wafer (Sb doped, 0.03Ω/cm) was used. Prior to the hydrogen-implant, a 100 nm thick SiO_2 layer was deposited to protect the Ge surface by Plasma-Enhanced Chemical Vapor Deposition (PECVD) and densified at 600 °C. Then the Ge wafer was implanted at room temperature with H_2^+ at a dose of 5×10^{16} cm^{-2} at 180 keV. The projected ion and the Ge vacancy planes were expected to be located at 650 nm and 590 nm beneath the Ge surface, respectively. Following the implant, dilute HF solution was used to remove the 100 nm SiO_2 damaged layer. The strain profile of the implanted Ge wafer has been assessed by high resolution x-ray diffraction (XRD) measurements [7]. Variation of the strain profile observed on the wafer was negligible, which indicates excellent implant uniformity among the sample. Then both the Si handle wafer with 100 nm oxide on the surface and Ge donor wafer were cleaned in SC1-equivalent solutions [deionized (DI) H_2O:NH_4OH:H_2O_2 =5:1:1] (without H_2O_2 in the Ge case) at 75 °C, rinsed in DI water, and dried in a spin dryer prior to the bonding. The wafer surfaces were hydrophilic after cleaning and the Si and Ge wafers were loaded into an AML wafer bonder immediately. In-situ remote plasma activation using oxygen was performed before the bonding. The Ge surface after radical activation was analyzed with another wafer by the XPS. After surface activation, a force of 1 kN was applied for 5 minutes to bond the wafer pairs in a vacuum chamber at a pressure of 10^{-5} mbar. Bonded pairs were annealed at 100 °C in-situ in order to improve the bond strength with a force of 500 N applied on the wafer pairs. This temperature step was performed with a low ramp up rate of 1°C/min to avoid high stress formation between Ge and Si (owing to a large difference of thermal expansion coefficients). Additional higher temperature anneals with a very low ramp rate, i.e. 0.5 °C/ minute, were performed to increase the bond strength again (T=130 °C, 24 hrs. and T=300 °C, 5 minutes). In order to remove the damaged layer on the transferred Ge thin film, a 5 minutes etching in dilute hydrogen peroxide (3% H_2O_2) solution was performed and the transferred Ge thin film was characterized by SEM.

5.1.4 Results and Discussion

Remote plasma (radical) activation prior to the bonding has a positive improvement on bond strength of the Ge bonded to Si wafer [8]. In previous experiments, in-situ

radical activation using oxygen was performed on Ge wafer before the bonding. In Table 5.1., Angle-Resolved X-ray Photoelectron Spectroscopy (ARXPS) has been used to characterize the surface properties at four take-off angles, which infers signals from different depths from the surface. The results indicate that the Ge oxide thickness was increased by remote plasma activation. The quantifiable APXPS data were used to estimate the film thickness as 0.39 and 0.72 nm for the reference and oxygen radical activated samples, respectively [8]. It was also observed that Hydroxyl (-OH) group concentration was modified after radical activation. The thicker Ge oxide layer and modified concentration of –OH group were likely the reason that high bond strength of the GeOI was achieved in our experiment.

Take-off angles (º)	**0**	**25**	**50**	**75**
Reference (O/Ge)	0.04	0.04	0.08	0.25
Reference (O^-/O^{2-})	0.34	0.24	0.09	0
Oxygen radical (O/Ge)	0.06	0.07	0.12	0.40
Oxygen radical (O^-/O^{2-})	0.11	0.11	0.02	0

Table 5.1: ARXPS peak area ratio. O/Ge is the total O 1s peak area divided by total Ge 2p3/2 peak area.O^-/O^{2-} is the O^- signal area divided by O^{2-} signal area in O 1s spectra. Take-off angles: angle between the X-ray as it targets or average surface plane.

In the experiment, an in-situ anneal at 100 °C for 1 hr, additionally an ex-situ anneal at 130 °C for 24 hrs and another ex-situ anneal at 300 °C for 5 minutes were performed. The first in-situ anneal was carried out to increase the bond strength of Ge/SiO_2 interface. In the second anneal at 130 °C for 24 hrs, it enhanced the nucleation of hydrogen platelets significantly and also had the function of increasing the bond strength. The third anneal was shown to complete the exfoliation process by triggering the formation of extended platelets [7, 9]. Figure 5.2(a) shows TEM image of the implanted Ge wafer. A 600 nm thick damaged layer was formed by the implant in the Ge wafer. In Figure 5.2(b), some nanocracks with the length no more than 50 nm were observed after anneal at 150 °C for 22 hrs. Figure 5.2(c) shows previous nanocracks transformed into microcracks parallel to the Ge surface which completes the exfoliation of the implanted Ge wafer. The microcracks were located around 600 nm beneath the surface.

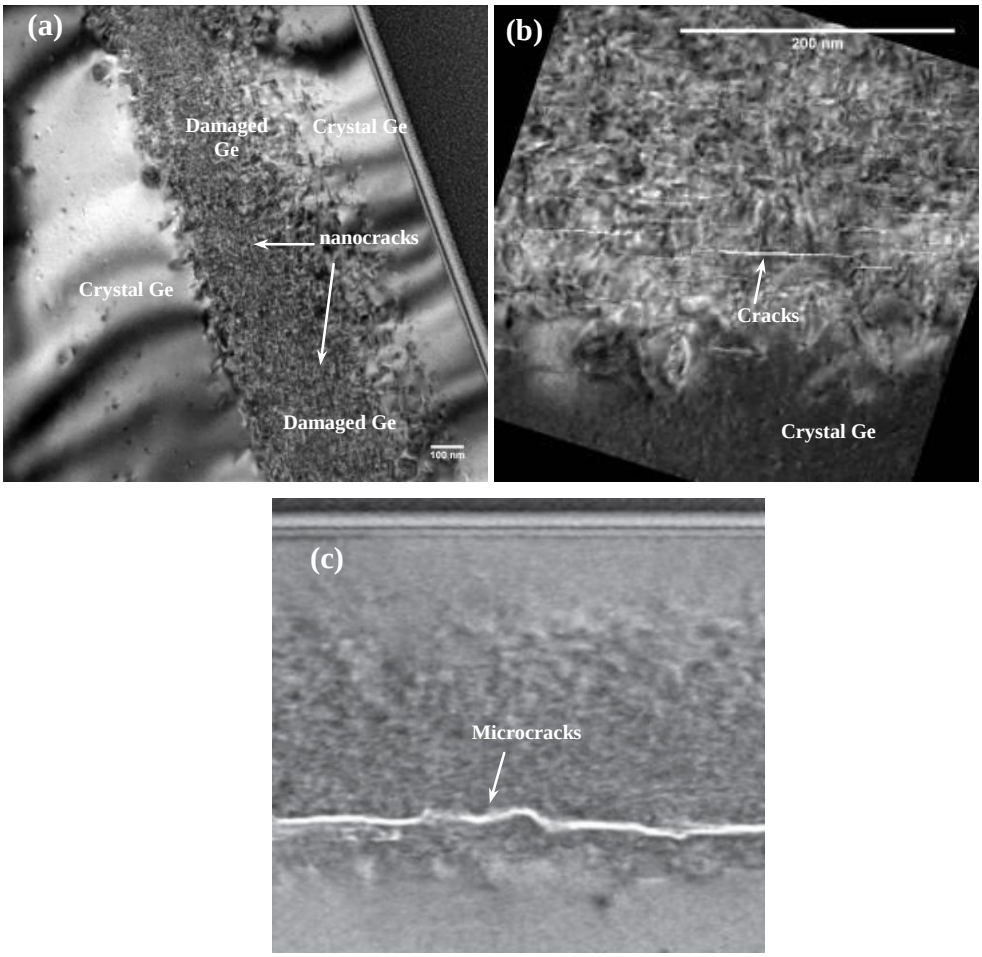


Figure 5.2: TEM images (a) Damage layer in the implanted Ge wafer; (b) nanocracks formation after anneal at 150 °C for 22 hrs in the Ge wafer; (c) macrocracks formation after additionl anneal at 300 °C for 5 minutes in the Ge wafer;

After one in-situ and two ex-situ steps of anneals, a thin Ge layer was successfully transferred onto a Si handle wafer with 100 nm SiO_2 on the top. A GeOI wafer was fabricated after the exfoliation of the Ge layer. Figure 5.3 shows the image of transferred 4 inch thin Ge layer with some voids in the layer. The formation of the voids was likely due to the particles in the SiO_2/Ge interface which can entrap the by-products (water, gas) from the interface reaction during the annealing process. The voids can be eliminated by better control of particles during the process.

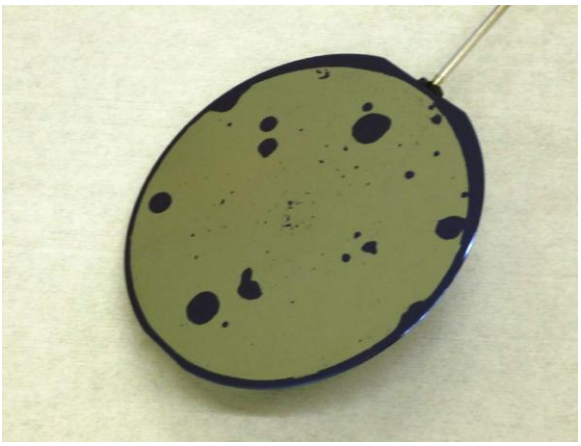


Figure 5.3: Transferred thin Ge layer onto Si handle wafer with 100 nm thermal grown SiO_2 (GeOI wafer). Dark spots on the substrates represent voids due to particle control.

In Figure 5.4(a), the SEM image shows plenty of cavities all over the surface formed by the hydrogen coalescence. Before the H_2O_2 wet etching and the Ge surface is in the 600 nm damaged range which should be removed by Chemical Mechanical Polishing (CMP) or wet etching to achieve a smooth surface, which is suitable for further device fabrication process. Figure 5.4(b) confirmed the thickness of the exfoliation Ge layer is around 600 nm, which is consistent with TEM images. Chemical Mechanical Polishing (CMP) is required to remove the damaged layer and thin down the Ge further, however, the nano-scale CMP is current not available at Tyndall.

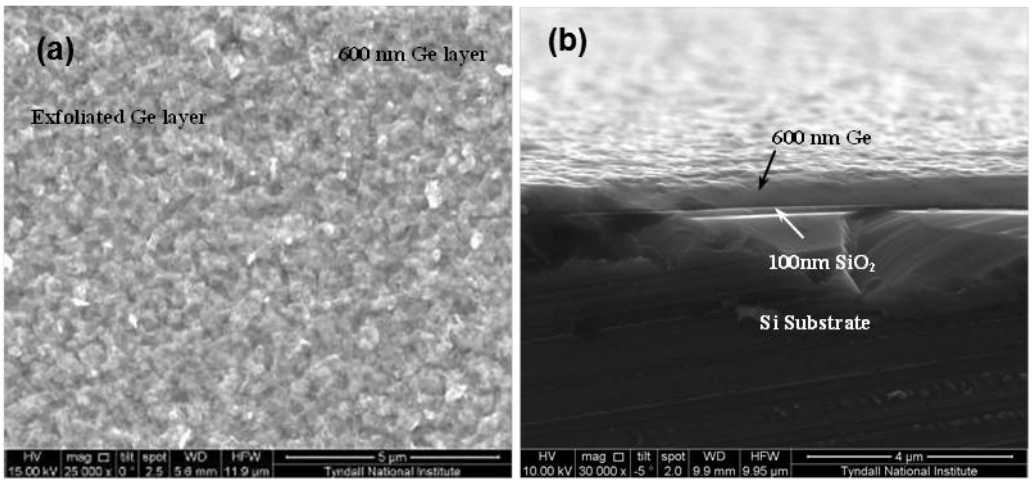


Figure 5.4: SEM image of (a) transferred Ge layer after exfoliation; (b) cross-section of the transferred Ge layer

Rather than starting with CMP process, here we simply utilized H_2O_2 wet etching to remove the damaged Ge layer. In dilute H_2O_2 (3 %), Ge bulk performs an aggressive etch rate, 22 nm/min according to literature [9]. The implant damaged Ge layer is expected to have a higher etch rate than bulk. Variable Angle Spectral ellipsometry (VASE) was used to measure the thickness of the Ge layer after immersing GeOI in H_2O_2 for 5 minutes. Around 100 nm thick Ge layer was measured by VASE on SiO_2 box. In Figure 5.5, different sizes of rectangle cavities with the same orientation were observed all over the etched layer. It can be explained by phenomenon of the orientation-dependent etching which appears in a crystalline structure [10]. Refined CMP is required to polish the surface down to certain roughness and thin film uniformity.

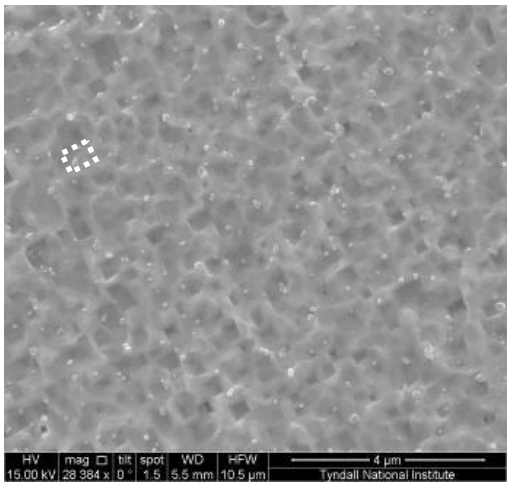


Figure 5.5: SEM image of transferred Ge layer after 5 minutes H_2O_2 wet etching.

5.1.5 Summary

Single crystal Ge on insulator (GeOI) was fabricated by low temperature direct wafer bonding method. The Ge layer was transferred onto a 100 nm thick SiO_2 film successfully. Three steps of anneal were performed to enhance the bond strength or trigger the exfoliation. After removing the damaged Ge layer using H_2O_2 solution, the surface was characterized by SEM, which shows rectangle cavities all over the surface. This orientation-dependent etching indicates a crystalline structure was achieved at the 100 nm thick of the transferred Ge layer. Refined CMP is required to polish the Ge thin film further.

5.2 Surface Defects on Germanium Wafer and the Decoration Method

5.2.1 Introduction

In order to evaluate the quality of GeOI wafer and optimize the Ge processing, defects in Ge substrates have to be studied. The preferential etching is used to reveal the defects in the substrates, by marking defects intersecting the surface by a small pit or groove, so they become visible in a microscope. Defects etching, or defect decoration, on silicon including Secco [11], Sirtl [12], Wright [13], Seiter [14], was extensively discussed for the past decades but in case of germanium only a few references have been reported [15, 16]. An efficient defect decoration method is thus demanded for germanium. Generally, the wet chemistry used for defect etching should include an oxidizer, an etchant and dilute solvent. The reaction must be sensitive to the presence of defects, the difference in stress level so that the surface has been etched faster or slower at the defects than in the perfect crystal. For germanium, the requirements of the solvent can be much different than silicon due to the complex germanium oxide. Generally a germanium surface oxidizes to GeO_2 by transitioning through a suboxide regime [17]. GeO_2 is not as stable, however, as SiO_2 and the removal of GeO_2 occurs in water described in following equation:

$$GeO_2 + H_2O = H_2GeO_3 \quad (1)$$

Therefore, water serves as the etchant when the oxidation state of germanium reaches Ge^{+4}, i.e. GeO_2. Solutions with an overall slow etch rate but dramatic etch rate difference between single crystal structures and distorted defect regions can be used for defect decoration for a thin film germanium layer. In the experiment, we found an H_2O_2:H_2O (1:10) solution is a good mixture for defects etching on germanium due to the large difference of etch rate on single crystalline structures and defect regions. In the mixture, H_2O_2 oxidizes the germanium bulk and germanium suboxide into GeO_2 and DI water acts as an agent to dissolve the GeO_2. Because of the aggressive etch rate at the imperfect crystal structure, the special orientated morphologies turn up after a certain time of wet etching.

In the first experiment, one 4 inch 100-orientated bulk, single crystal p-type Ge wafer (Ga doped, 0.018 Ω/cm) was etched with Wright etch, in order to characterize the initial defect density from the bulk wafer. In the second experiment, two 4 inch 100-orientated p-type Ge wafer (Ga doped, 0.018 Ω/cm) were covered with 100 nm thick SiO_2 layer by PECVD and densified at 600°C in preparation for hydrogen implantation. Then the germanium wafer was implanted at room temperature with H^+ at a dose of 2.5×10^{16} cm^{-2} at 90 keV. Following the implant, BOE (Buffer Oxide Etchant) solution was used to remove the 100 nm SiO_2 layer. One as implanted Ge wafer was diced into pieces and dipped into the decoration solution (H_2O_2:H_2O (1:10)) for different periods of time. The morphologies of the etched as implanted Ge wafers were characterized by SEM. The other implanted Ge wafer has been bonded to a Si handle wafer with 100 nm oxide on the top. Using the same process developed in the first section of this chapter, Ge thin film has been successfully transferred on the SiO_2 substrate. 2 minutes etching in an H_2O_2:H_2O (1:10) solution has been performed and SEM images indicate the damaged porous layer due to hydrogen implantation on the transferred germanium thin film was removed after the etching. Special morphologies were observed on the transferred germanium after the wet etching. In additional remaining part of the germanium donor wafer, which also has a damaged porous surface, was dipped into the same decoration solution to characterize the defects properties.

5.2.2 Wright Etch on Bulk Germanium Wafer

The Wright etch is conventionally used as a preferential etch solvent to reveal defects on (100) and (111) orientated silicon surface. The solution used in this experiment consists of HF, CrO_3 and DI water with the ratio of 1:0.5:1. For silicon the etch rate of Wright etch is proximately 1 um/min [13]. It is expected that the etch rate should be faster on germanium surface since two etchants (HF and DI water) were etching the germanium dioxide. For bulk germanium wafer with a relatively low defect density expected, a high etch rate of several micron per minute is demanded. The etch rate for p type bulk germanium in an H_2O_2:H_2O (1:10) solution is 17 nm/min, measured by Brunco, *et al.* [9]. This etch rate is not enough for defect decoration on bulk germanium. Therefore a Wright etch was performed here. Figure 5.6 shows a defect with square morphology on a germanium surface after 8 minutes Wright etch. The size of the defect is approximately 903.5 nm by 866.7 nm. The preferential etched planes, which end up

in the centre of the defect, can be observed in the square. This can be explained by the preferential etch mechanism in crystal structure. As a suspect threading dislocation extended on to the germanium surface, the crystal can be etched faster than the other parts due to distorted crystal structure by the threading dislocation. The etching will start at the defect point and etch in certain direction which makes four planes ending up on the germanium surface with the flipped pyramidal morphology.

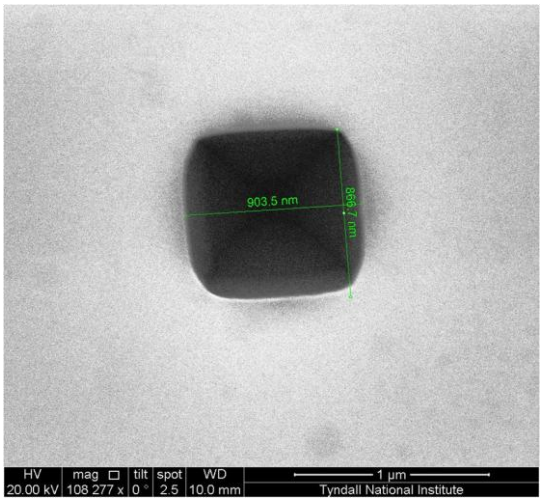


Figure 5.6: A Wright etch on (100) p-type germanium wafer.

Although the flipped pyramids, which represent the defects after Wright etch, have been observed, the density of these defects is lower than that can be statistically analysed as only 3 defects have been found at random locations on one Ge wafer. Throughout the surface, a couple of flipped pyramids have been discovery at very random locations, which adversely affects the calculation of a reliable defects density. The actual defect density in the bulk Ge wafer can be much larger than surface defects density as many defects have not extended onto or near the surface.

5.2.3 Defects Decoration during the GeOI Fabrication

5.2.4 Defects Decoration for as-implanted Ge Wafer

The Wright etch has a fast etch rate for Ge, which is suitable for observation of very low defect density. Thus, for defects decoration during the GeOI fabrication a mild preferential etchant has been required. In order to slow down the etch rate, the

H_2O_2:H_2O (1:10) solution has been proposed in this experiment. As many process steps have been involved during the GeOI fabrication, the decoration has been performed during each individual processing step.

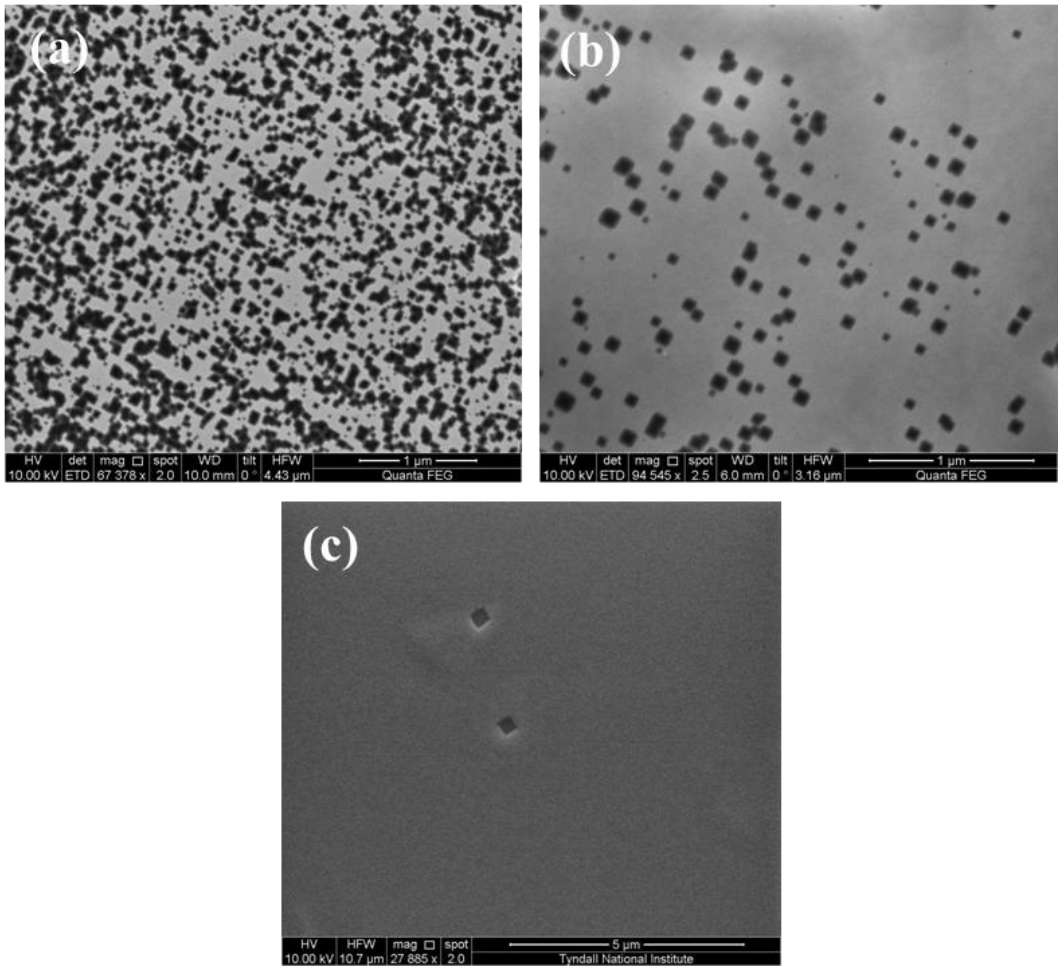


Figure 5.7: H_2O_2 wet etching at different locations on as implanted germanium wafer. (a) 3 minutes; (b) 2 minutes; (c) 2 minutes

First, the hydrogen implanted germanium wafer was etched by an H_2O_2:H_2O (1:10) solution. The mechanism that H implantation creates microcracks parallel to the surface has been extensively discussed in silicon, germanium [18] and III-V compounds[19]. In these discussions, mostly it's about H-related extended defects, the so called platelets that are at the origin of the ion cutting process. The hydrogen implant induced surface damage was discussed only in a few papers [20]. Figure 5.7 shows square morphology on as implanted germanium surface after the decoration, which indicates that possibly defects have been introduced during hydrogen implantation. All the square morphologies are in the same orientation and the highest defect density on some region

is up to ~$1\times10^{10}/cm^2$. These defects may be attributed to agglomeration of point defects induced by hydrogen implantation. The parameters of hydrogen implantation, such as dose, energy, current, temperature, thickness of protection layer, etc., need to be optimized to get a less defective ion-implanted germanium wafer. Another possible origin for these defects may be related to the deposition process of protection oxide. The temperature of PECVD oxide is approximately 300 °C, however, followed by densification at 600 C. This 600 °C process may induce desorption of Ge substrate, even through the 100 nm SiO_2.

5.2.5 Defects Decoration and Thinning of Transferred Ge Thin Film on GeOI

The hydrogen peroxide solution can decorate the defects because of the contrast etch rates in different crystal orientations, which exhibit generally a faster etch rate in the highly defected region than that in the crystal perfect region. In order to quantitatively analyze the effect, Variable Angle Spectroscopic Ellipsometry (VASE) was used to estimate the thickness of transferred Ge thin film at various etch times.

Before the etching, the GeOI surface was full of pores due to exfoliation process and a large RMS of 39 nm was measured by AFM in a 2 um × 2 um region. The roughness of the transferred Ge thin film causes an poor match of the ellipsometry models, however, it still may be used as an indication of the average etch rates. As shown in Figure 5.8, the measured initial Ge thickness is 670 nm, which agrees with the projected ion and Ge vacancy ranges from the simulation software. The average etch rate for the damaged region is approximately 145 nm/min and decreases to 70 nm/min after around 100 seconds in an H_2O_2:H_2O (1:10) solution as shown in Figure 5.8. This result confirms the inference that the etch rate is higher in highly defected region than that in the crystal perfect region. Moreover, it indicates that at least 400 nm of the transferred Ge thin film possesses much low defects density, comparing with the damage region.

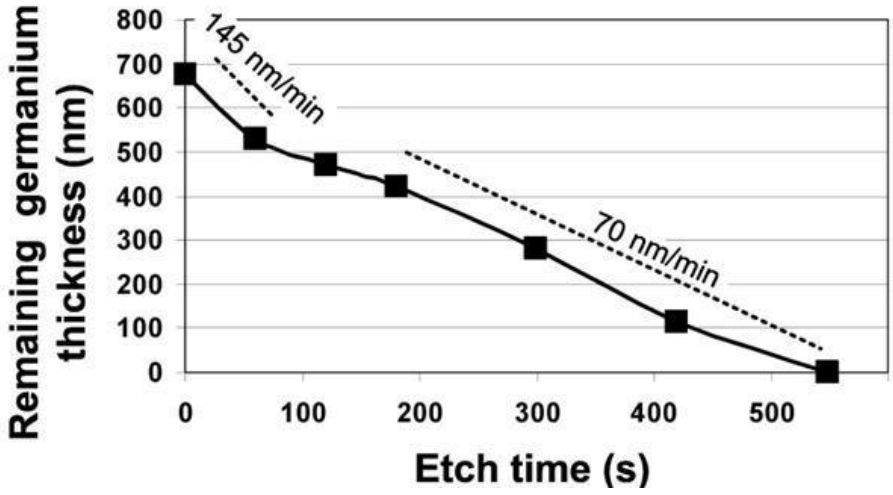


Figure 5.8: Remaining Ge thickness as a function of etch time. In the damage region, the etch rate (145 nm/min) is higher than that closing to the bonding interface region (70 nm/min).

In Figure 5.9, square morphologies (red dash) have been observed again after the wet etch and all the square morphologies are in the same orientation. The angle between the primary flat of the germanium wafer and the orientated square was measured. The primary flat orientation of the transferred p-type germanium wafer is <100>. The square orientation is <110>, which is 45º from the <100> direction. The preferentially etched planes, which are in {111} orientation, end up in the centre. The result is similar to the square showed in Figure 5.6, which can be explained as the etch start at the defect points and developed into a flipped pyramid with four same orientated planes. As the original exfoliated Ge thin film exhibits a large roughness before the thinning process, the Ge surface after etching inherently shows non flat surface. In most case, no preferentially etched planes end up in the centre, which indicates that no defects have been extended onto the surface in this region.

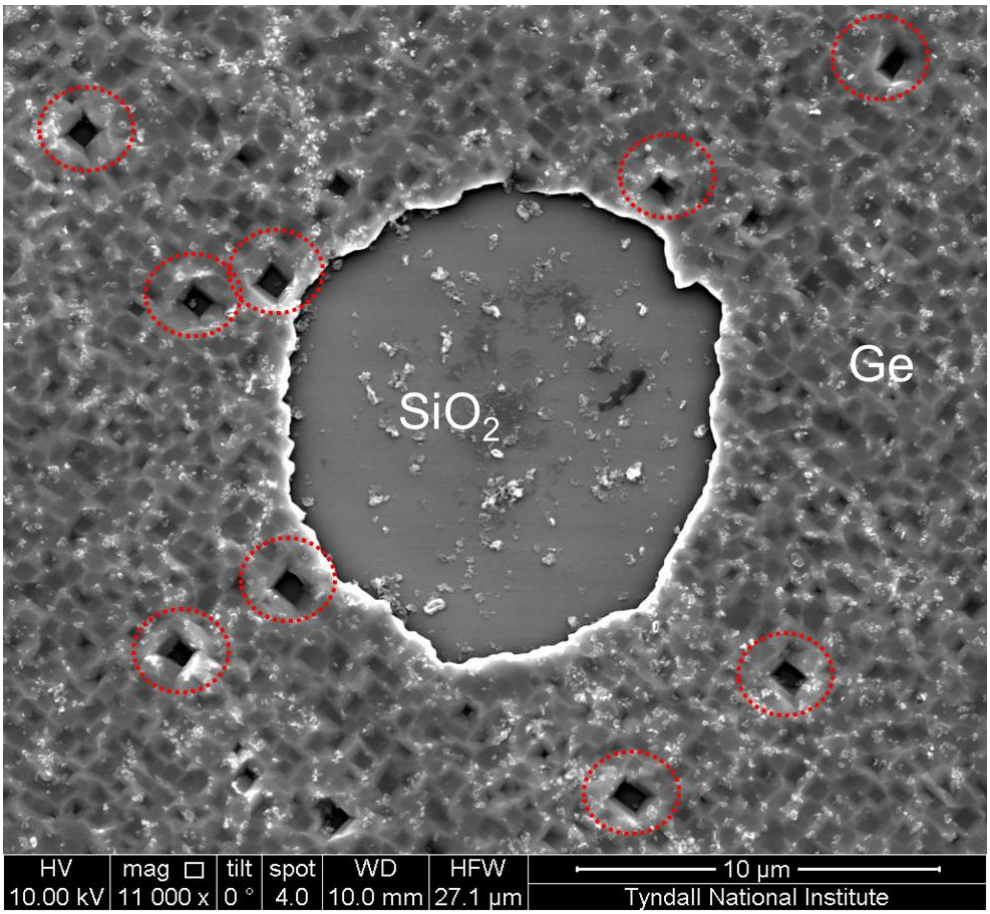


Figure 5.9: GeOI wafer with one void in centre and defects (red dash) in the Ge thin film after H_2O_2 solution etch

5.2.6 Defects Decoration of the un-transferred Ge Donor Wafer

In order to further understand the etch mechanism on the GeOI process, the remaining part of the donor germanium wafer was etched in the same H_2O_2 solution for 15 minutes. This wet etch results in a consumption of 1 µm Ge into the donor wafer, where is far away from the region influenced by H^+ implantation. Figure 5.10 shows two types of square morphologies after a long time wet etch. The type A square in Figure 5.10 shows four planes end up in the centre of the square, which indicates it is a defect extended to the germanium surface. The type B square also has four planes on the edge, but the planes are not ending up in the centre. The B type square possibly exhibit a preferential etching due to an un-flat exfoliated initial surface. In T. Kawase's paper [21], a pyramidal-shaped etch pits was discovered on a p type (100) Ge wafer, which likely has the same mechanism of a preferential etch on Ge surface. The etched plane has a 54º angle with the <100> Ge surface. That means the etched planes are {111} planes. This result agrees with our observations. Since the all the squares discovered on

our GeOI are in <110> orientation, {111} preferential etched planes are the most possible planes expected. As the wet etch consumes around 1 μm Ge, the region scanned is far away from the H^+ implantation affected area. As a result, the density of type A square is similar to the case on bulk Ge wafer, which indicates the high defects density in transferred Ge thin film is related to the fabrication processing.

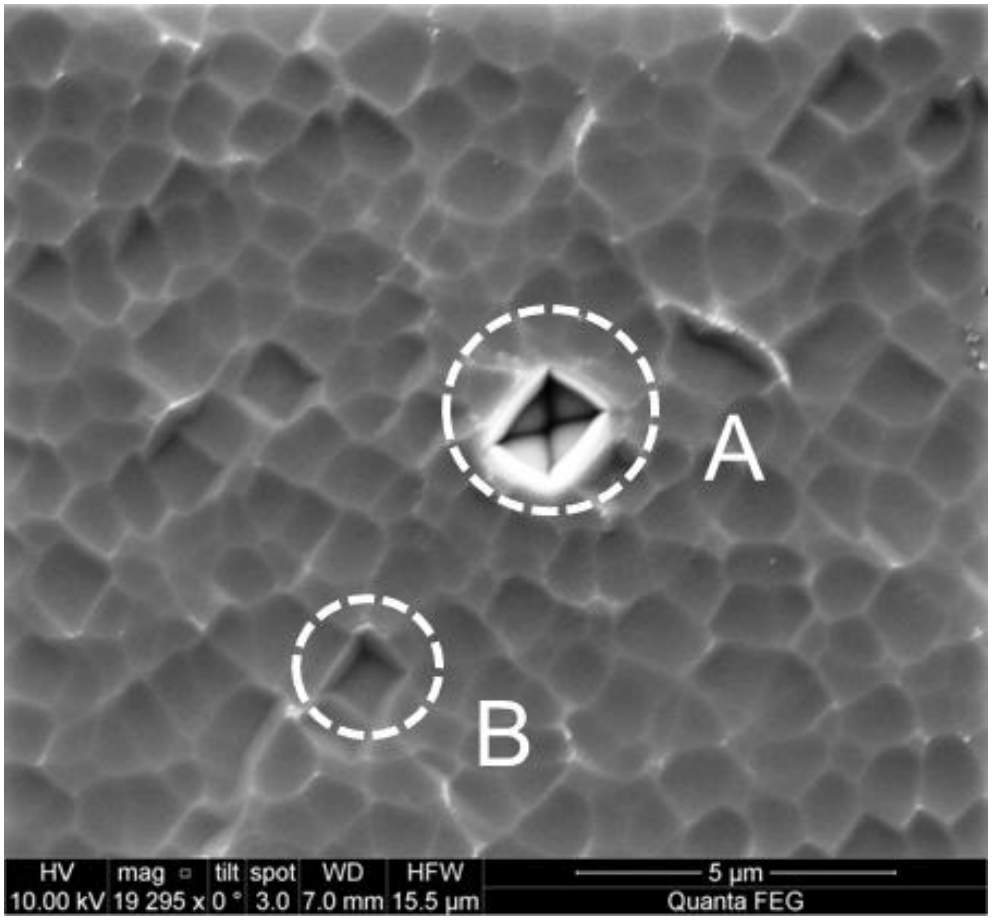


Figure 5.10: 15 mins H_2O_2 wet etching on remaining part of Ge donor wafer

5.2.7 Summary

In summary, a simple decoration method to highlight the surface defects on Ge has been proposed in this section and the possible defects etch mechanism was explained. The results show that the high defects density in the transferred Ge thin film is related to the GeOI fabrication processing, especially to the implant or PECVD oxide process. The parameters of H^+ implantation, such as, dose, energy, current, temperature, process of protection layer, etc., need to be optimized to get fewer defects into the Ge wafer.

5.3 Top-down Process of Ge Nanowires using EBL Exposure of Hydrogen Silsesquioxane (HSQ) Positive Resist

5.3.1 Introduction

Three-dimensional (3D) transistors with a multi-gate structure (double-, triple- or quadruple- gate devices) intrinsically provide a better electrostatic gate control of the channel than regular, planar transistors. As a result, 3D transistor such as nanowire transistor, with the special properties of higher current drive, lower power consumption and immunity to short channel effects, becomes a promising candidate for future CMOS scaling [22]. Germanium (Ge), due to its high electron/hole mobility and low effective mass, has the potential to replace Si beyond 22 nm node [23]. The fabrications of nanowire transistors using bulk silicon or Silicon-on-Insulator (SOI) substrates were intensively studied by many groups [24-26]. However, top-down fabrication process of sub-50-nm Ge nanowire has not yet been well investigated due to the challenges of lithography related to Ge surface chemistry and different wafer quality. In this work, we demonstrate an initial fabrication process of Ge nanowires using a nitride hardmask and the HSQ resist which is a very suitable e-beam resist when aiming for sub-20-nm resolution.

In the past decade, the feature size in ultra-large-scale integration (ULSI) has been continuously decreasing, leading to nanostructure fabrication. Nowadays, various lithographic techniques ranging from conventional methods (e.g. photolithography, x-rays) to unconventional ones (e.g. nanoimprint lithography, self-assembled monolayers) are used to create small features. Among all these, resist-based electron beam lithography (EBL) seems to be the most suitable technique when nanostructures are desired. The achievement of sub-20-nm structures using EBL is a very sensitive process determined by various factors, starting with the choice of resist material and ending with the development process. After a short introduction to nanolithography, a framework for the nanofabrication process is presented. To obtain finer patterns, improvements of the material properties of the resist are very important. The present review gives an overview of the best resolution obtained with several types of both

organic and inorganic resists. For each resist, the advantages and disadvantages are presented. Although very small features (2-5 nm) have been obtained with PMMA and inorganic metal halides, for the former resist the low etch resistance and instability of the pattern, and for the latter the delicate handling of the samples and the difficulties encountered in the spinning session, prevent the wider use of these e-beam resists in nanostructure fabrication. A relatively new e-beam resist, hydrogen silsesquioxane (HSQ), is very suitable when aiming for sub-20-nm resolution.

The changes that this resist undergoes before, during and after electron beam exposure are discussed and the influence of various parameters (e.g. pre-baking, exposure dose, writing strategy, development process) on the resolution is presented. In general, high resolution can be obtained using ultrathin resist layers and when the exposure is performed at high acceleration voltages. Usually, one of the properties of the resist material is improved to the detriment of another. It has been demonstrated that aging, baking at low temperature, immediate exposure after spin coating, the use of a weak developer and development at a low temperature increase the sensitivity but decrease the contrast. The surface roughness is more pronounced at low exposure doses (high sensitivity) and high baking temperatures. A delay between exposure and development seems to increase both contrast and the sensitivity of samples which are stored in a vacuum after exposure, compared to those stored in air. Due to its relative immaturity, the capabilities of HSQ have not been completely explored, hence there is still room for improvement.

Applications of this electron beam resist in lithographic techniques other than EBL are also discussed. Finally, conclusions and an outlook are presented.

5.3.2 Top-down Process of Ge Nanowires

The experiments are carried out on samples from 4 inch (100)-oriented p-type Ge (resistivity=0.016 Ωcm) wafer (Umicore, Belgium). Samples are first degreased by sonication in acetone and Isopropyl alcohol (IPA), cleaned in 5:1 H_2SO_4:H_2O for 2 minutes, rinsed with DI water, etched in Buffered Oxide Etcher (BOE) for 5 minutes, and then followed by a N_2 blow dry. Figure 5.11 illustrates the four major steps of Ge nanowire formation. Figure 5.11(a) shows a 20 nm Si_3N_4 layer (red) is deposited on Ge

surface (blue) by PECVD and 50 nm HSQ (white) (XR-1541 Dow Corning Corp.) is spin coated on the top of nitride layer. EBL is performed using a Zeiss Supra 40 FESEM equipped with a Raith Elphy digital pattern generator with a dose of 2100 $\mu C/cm^2$. The sample is then developed in aqueous 0.125 M NaOH, followed by DI rinse and a N_2 blow dry (Figure 5.11(b)). The hardmask etch and Ge etch are performed on a STS and an Oxford ICP etcher, respectively (Figure 5.11(c-d)). Three different etch recipes are tested as hardmask etch (Table 5.2). As a result, the pattern is successfully transferred to the nitride using a RIE mode recipe with CH_4:CHF_3 gas.

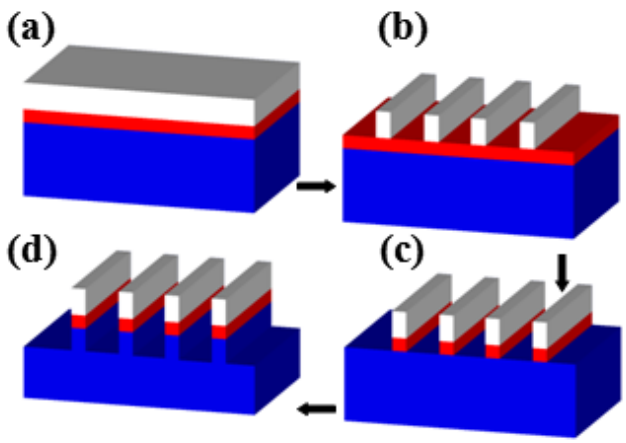


Figure 5.11: White: HSQ; Red: Si_3N_4; Blue: Ge; Schematic of the fabrication process of Ge nanowires. (a) 20nm S_3N_4 layer is deposited on Ge by PECVD and 50 nm HSQ is spin coated on the top of nitride layer (b) EBL exposure and development (c) Hardmask etch (d) Ge etch

It gives the most anisotropic etch of the hardmask and least impacts on the HSQ resist (Figure 5.11(c)). Figure 5.11(d) illustrates the last step of the nanowire formation corresponding to a proper Ge etch. It shows the etch recipe using pure Cl_2 gas gives a reasonable etch results of 1 nm/sec. Finally the nitride hardmask and HSQ are removed by 5 min BOE and the sample is characterized by SEM.

5.3.3 Results and Discussions

The native Ge oxides have different forms such as oxide rich GeO_2 and Ge suboxide (GeO_x, $x<2$). The GeO_2 is water soluble and has negative impacts on nanoscale lithography. Although the Ge native oxides are etched in BOE at the last step of sample preparation, the oxide regrows in minutes. When the width of nanowires is smaller than 50 nm, a poor adhesion or a lift-off of the photoresist during development can easily be

observed if the photoresist is directly spin coated on the bare Ge surface. Therefore, a deposited Si_3N_4 layer on Ge can offer more suitable surface properties for lithography. A nitride hardmask etch is followed after EBL exposure and development.

Etchant	Nitride Hardmask Etch		
	parameters	Etch Rate	Results
(i) SF_6	50 sccm; ICP:500 W; RF:10 W; 30 mTorr	80 nm/min	Isotropic; rough sidewall and hardmask
(ii) CH_4:CHF_3	12 sccm:18 sccm; ICP:800 W; RF:75 W; 2.5 mTorr	N/A	Isotropic; pattern gone
(iii) CH_4:CHF_3	12 sccm:18 sccm; ICP:0 W; RF:75 W; 2.5 mTorr	18 nm/min	Anisotropic pattern transferred

Table 5.2: Summary of conditions and results of nitride hardmask etch with three exiting recipes on the STS ICP etcher in Tyndall IIIV cleanroom.

The assessment of the existing recipes has been performed for the nitride etch on STS ICP etcher in Tyndall IIIV cleanroom. A summary of the tested etch recipes of nitride hardmask are described in Table 5.2. It is worth noting that fluorine based etchants without carbon portion or too high density of fluorine plasma give an isotropic etch on both HSQ and nitride and the nano-scale patterns cannot be successfully transferred into the nitride layer due to the damage of the HSQ or large etch undercut in nitride. According to the results, the option iii shows its potential to be used in nano-scale nitride etch with HSQ photoresist.

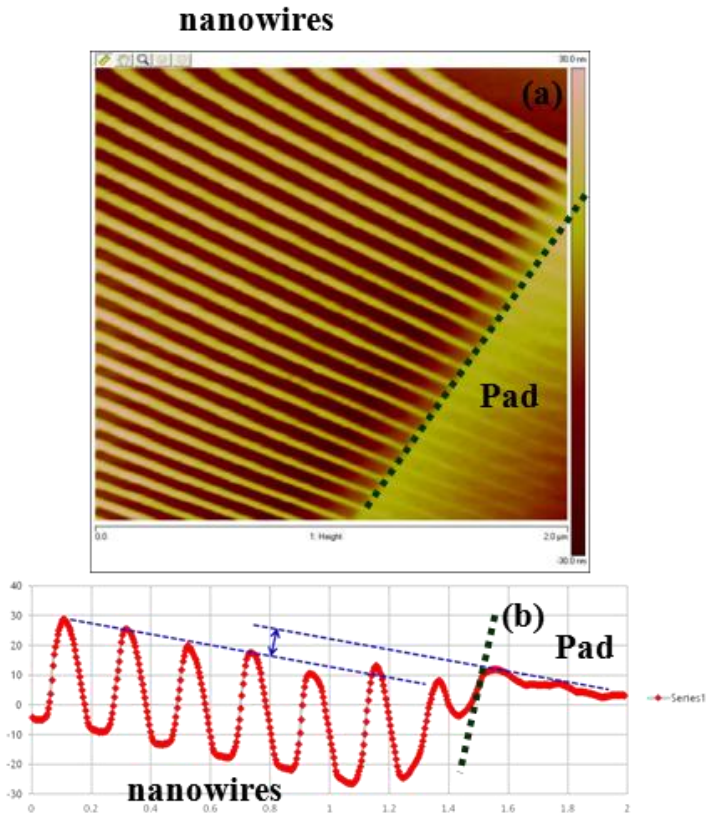


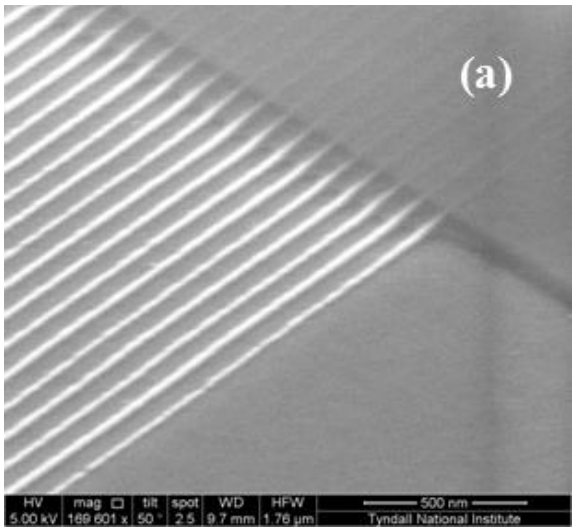
Figure 5.12: AFM images of patterns transferred into nitride using (iii) hardmask etch recipe (a) topview (b) cross-section

In Figure 5.12 after nitride etch using the (iii) hardmask recipe, the surface is characterized by AFM. In Figure 5.12(a), it can be observed that the consumptions of HSQ during the process are different in the nanowire region and the large pad region. In Figure 5.12(b) it is noted HSQ is etched 10 nm more in the nanowire region than the pad region. It can be explained as the density of HSQ in the nanowire region is smaller than that in the pad region which leads to a higher etch rate. Also the nanowire structure provides two sidewalls which can be partially etched even a very anisotropic etch recipe is used.

Etchant	Ge Etch		
	parameters	Etch Rate	Results
(i) Cl_2	30 sccm; RF:50 W; 10 mTorr	50 nm/min	Anisotropic; pattern transferred
(ii) Cl_2	30 sccm; ICP:0 W; RF:80 W; 10 mTorr	58 nm/min	Anisotropic; pattern transferred
(iii) SF_6:C_4F_8	45 sccm:85 sccm; ICP:600 W; RF:15 W; 15 mTorr	125 nm/min	Isotropic; rough sidewall; large undercut

Table 5.3: Summary of conditions and results of Ge etch with two exiting (i,iii) and one modified (ii) recipes on the Oxford ICP etcher in Tyndall IIIV cleanroom.

The assessment of two existing recipes (i,iii) has been performed for the Ge etch on Oxford ICP etcher in Tyndall IIIV cleanroom. According to the results of the existing recipes, a modified recipe has been given. The Ge etch recipes tested are summarized in Table 5.3. It is observed that the nanowire patterns can be successfully transferred using pure chlorine etchant. It gives a relative anisotropic etch and good sidewalls. Even Pseudo Bosch etch which is commonly used for nanoscale high aspect-ratio Si etch, is still too aggressive for Ge and leads to very rough sidewalls and large undercut. However it is noted that pure chlorine etchant gives a maximum etch depth of 100 nm for 50 nm width of nitride hardmask. According to the results, the option ii shows its potential to be used in nano-scale Ge etch with HSQ photoresist and nitride hardmask.



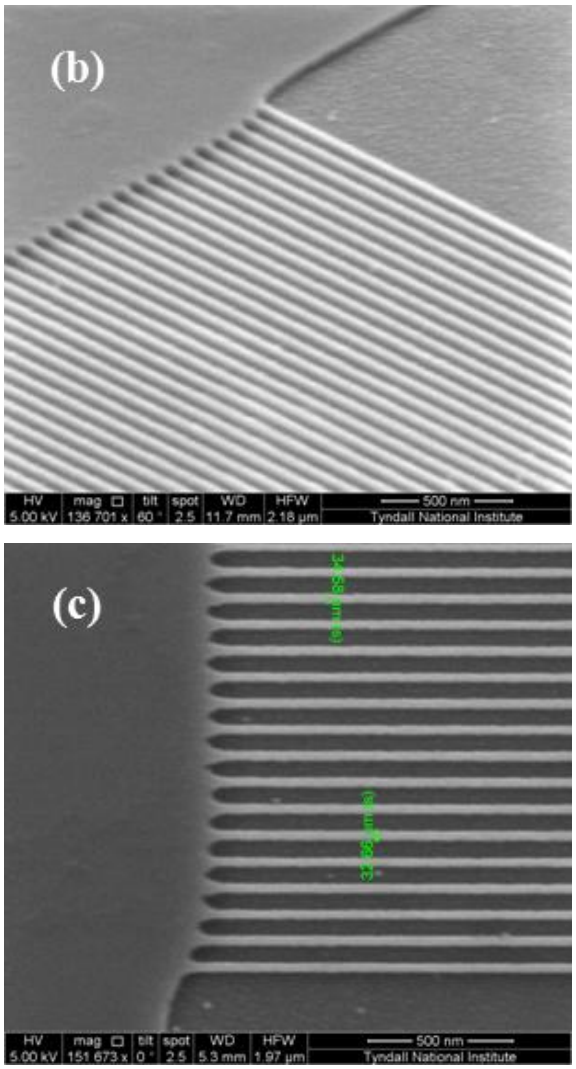


Figure 5.13: SEM images of (a) patterns transferred into nitride using (iii) hardmask etch recipe. (b) tilted Ge nanowires after Ge etch using Cl_2 gas. (c) topview of Ge nanowires after Ge etch using Cl_2 gas.

The undercut cannot be negligible when the etch depth beyond 100 nm for pure chlorine etchant. Therefore it is worth to introduce some passivation gas into the chlorine gas when high aspect-ratio etch is required. Finally using the hardmask etch recipe (iii) and Ge etch recipe (ii), Ge nanowires with around 35 nm width and 50 nm depth are obtained in this work (Figure 5.13(b),(c)).

5.3.4 Conclusions

A top-down process of sub-50-nm width Ge nanowires is developed in this work. A Si_3N_4 layer (PECVD) is deposited on top of Ge to prevent the challenges of lithography related to Ge native oxide (GeO_2). A hardmask etch and a Ge etch recipe are selected.

As a result, Ge nanowires with 35 nm width and 50 nm depth are obtained using this process. Future work can be done to obtain narrower and high aspect-ratio Ge nanowires by oxidation and introducing some passivation gases during the Ge etch, respectively.

5.4 Ge Nanowire JNT

JNT with Ge channels have been fabricated by a CMOS-compatible top-down process in this section. The transistors exhibit the lowest subthreshold slope to date for Ge junctionless devices. The devices with a gate length of 3 μm exhibit a subthreshold slope (*SS*) of 216 mV/dec with an I_{ON}/I_{OFF} current ratio of 1.2×10^3 at V_D = -1 V and *DIBL* of 87 mV/V.

5.4.1 Device Fabrication Process

Figure 5.14 shows the designed mask of the Ge JNT, including EBL mask, contact windows mask and metal gate+S/D mask. In Figure 5.14(b), the green region is used to define Ge pads and nanowire by EBL. The black region is used to open contact windows via high-*k* dielectric. The dash region is used for Ni metal gate and S/D electrodes.

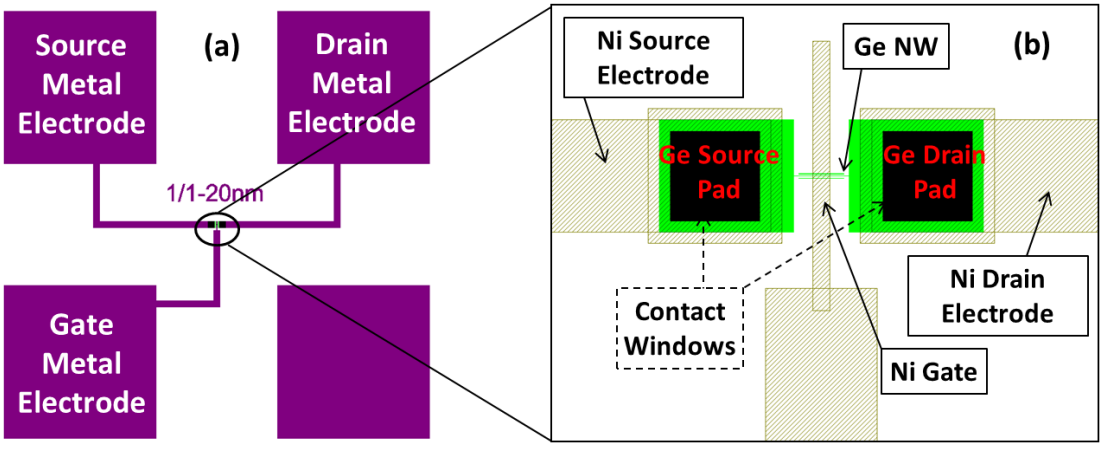


Figure 5.14: Designed mask of the Ge JNT, including EBL mask, contact windows mask and metal gate+S/D mask.

Figure 5.15 shows the process flow of the Ge JNT fabrication. Germanium-on-Insulator wafer (GeOI) with highly p-doped (~1 × 10^{19}) top Ge layer of 39 nm and buried oxide (BOX) SiO_2 layer of 145 nm is used in this work. The nanowire structures of width down to 20 nm were defined by JEOL electron-beam lithography system with a negative hydrogen silsesquioxane (HSQ) resist process developed in previous section.

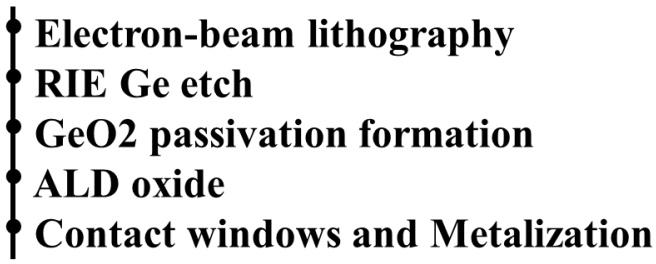


Figure 5.15: Process flow of the Ge JNT with high-k dielectric and Ni metal gate.

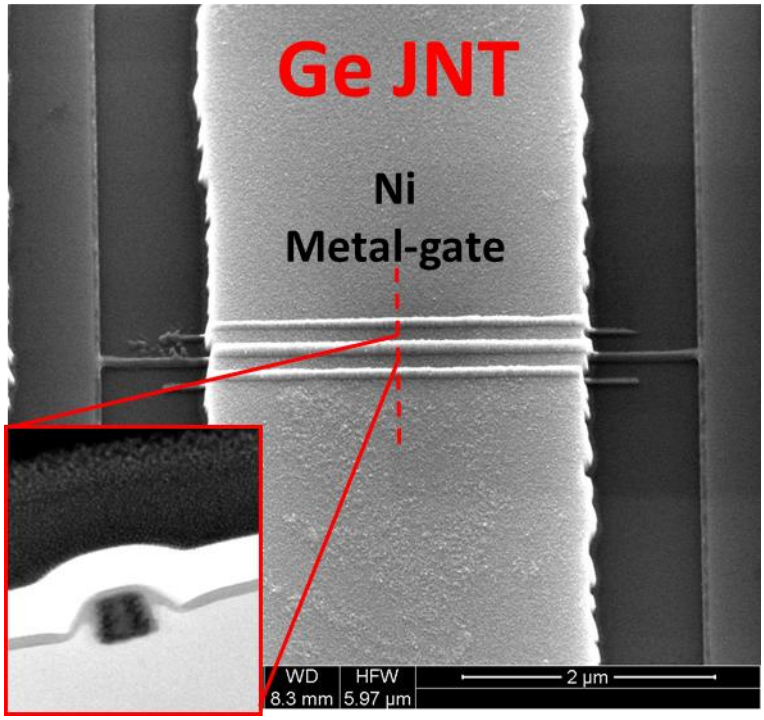


Figure 5.16: SEM and TEM cross-section image of Ge JNT with T_{Ge} = 39 nm, W_{Ge} = 20 nm and a gate length of 3 µm. The Ge nanowires are passivated by GeO_2 and then 8 nm Al_2O_3 layer is deposited.

The pattern was then transferred into Ge by a Cl_2 based RIE process. GeO_2 passivation layer was formed by rapid thermal oxidation at 500 °C for 1 min. An Al_2O_3 layer (~8 nm) was deposited by ALD. Contact windows for the source and drain region

were opened by a wet etch in 5:1 BOE. The source/drain electrodes and metal gate were defined by the same lithography mask. Thus, both the source/drain electrodes and the gate were formed using one-step 100 nm Nickel metallization by the electron-beam evaporator. Figure 5.16 shows the fabricated Ge JNT with a Ni metal gate on the top of the Ge nanowire. Electrical measurements of devices were carried out by cascade probe station and Agilent B1500.

5.4.2 Device Characterization

Figure 5.17 shows the drain current vs. gate voltage (I_D-V_G) curves of 3 μm gate length Ge JNT with fin height of 39 nm and fin widths of 20 nm. It can be observed that when the V_D increases from -0.7 V to -0.4 V, the leakage current is dramatically reduced. This can be explained as when the V_D is larger than the Ge bandgap, band to band tunnelling current occurs even in junctionless structures, which have theoretically non PN junction defects. In addition, the leakage currents exhibit at approximate levels for V_D = - 0.7 V and -1 V.

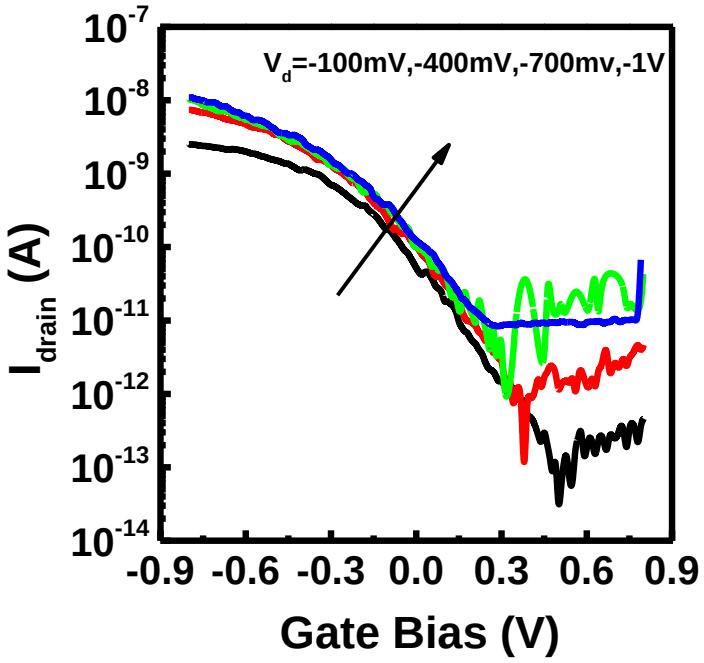


Figure 5.17: I_D-V_G curves at V_D = -0.1~-1 V, V_{bg} = 0 V. Ge JNT with 1 Ge NW of 5 μm length. T_{Ge} = 39 nm, W_{Ge} = 20 nm and a gate length of 2.5 μm.

This Ge JNT exhibit a subthreshold slope (*SS*) of 216 mV/dec with an I_{ON}/I_{OFF} current ratio of 1.2×10^3 at V_D = -1 V and 189 mV/dec with an I_{ON}/I_{OFF} current ratio of

2.0×10^5 at V_D = -0.1 V. The *DIBL* is calculated as 87 mV/V from V_D = -0.1 V and -1 V. It is also noted that the curves are not very smooth at the subthreshold regions. This effect might be due to the sidewall roughness of the long and narrow Ge nanowire, which is introduced by the lithography and etch process.

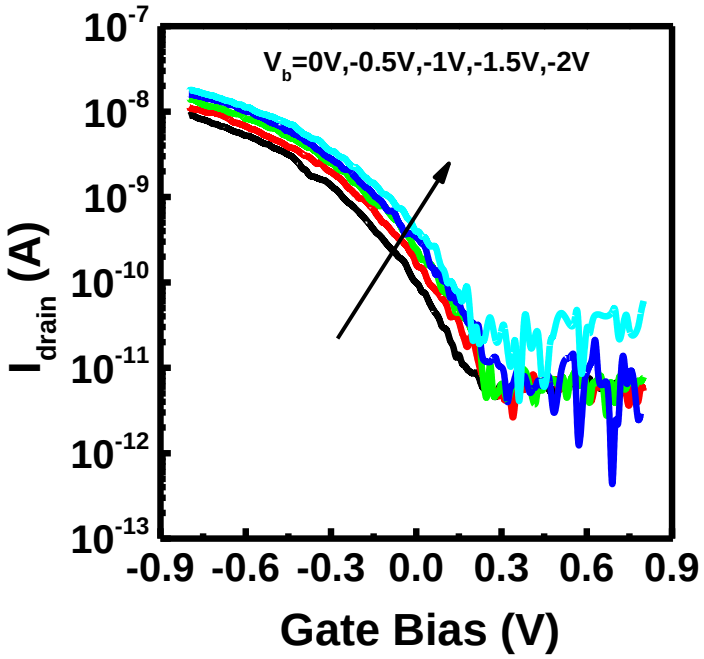


Figure 5.18: I_D-V_G curves at V_b = 0 ~ -2 V, V_D = -1 V. Ge JNT with 1 Ge NW of 5 μm length. T_{Ge} = 39 nm, W_{Ge} = 20 nm and a gate length of 2.5 μm.

In Figure 5.18, the I_D-V_G curves were measured for different back-gate voltage from 0 V to -2 V. It can be observed that the on-currents increase as V_G changes from 0 V to – 2 V simultaneously. In contrast, the leakage currents show similar level at V_b > -1.5 V, and abruptly increased at V_b = -2 V.

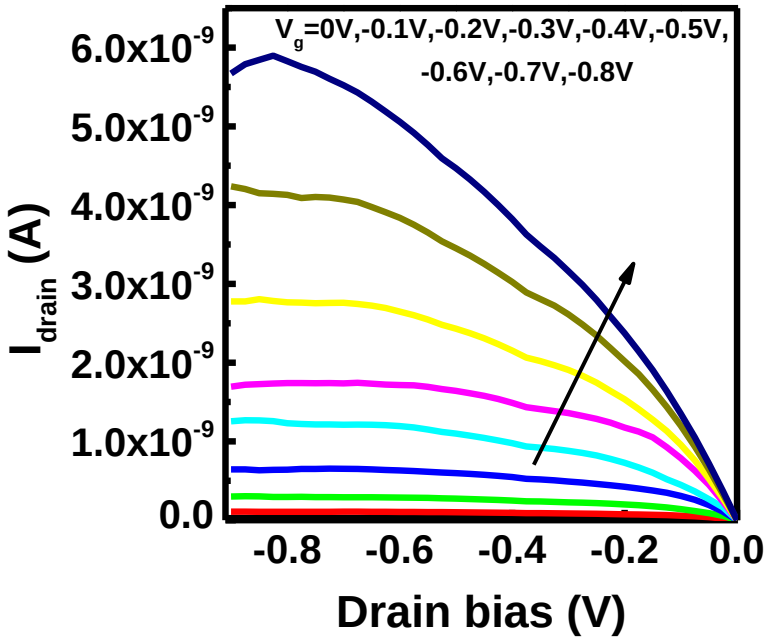


Figure 5.19: I_D-V_D curves at V_G = 0~ -0.8 V. Ge JNT with 1 GeNW of 5 μm length. T_{Ge} = 39 nm, W_{Ge} = 20 nm and a gate length of 2.5 μm.

I_D-V_D output characteristics of the Ge JNT are shown in Figure 5.19. The curves exhibit the linear and saturation regions. It can be observed that the increase of current is relatively proportional to $(V_G - V_{th})^2$, which indicates the carriers in the channel have not reached the velocity saturation.

In order to compare the Ge Junctionless transistors [27-29] with our device, a summary of the device characteristics have been listed in Table 5.4. As shown in the table, our Ge JNT has much smaller dimensions in both channel length and width, than those from Ref. [27-29]. I_{ON}/I_{OFF} current ratio of our device is close to the value in Ref. [28] at high and low V_D, respectively. The *DIBL* of our device exhibits much better value of 87 mV/V, than that from the reference devices. The subthreshold slopes of our devices is c.a. 4 times better than best data from Ref. [29] for both high and low V_D, which indicates excellent gate control of our devices. The superb gate control can be attributed to the small dimension of our devices and the proper passivation scheme applied before the high-*k* dielectric.

Parameters	Ref.27	Ref.28	Ref.29	Our device
W(μm)		0.16	130	0.02
L_{GATE}(μm)	100	5.2	160	3
W/ L_{GATE}		0.033	0.812	0.013
I_{ON}/I_{OFF}(high V_D= -1V)		1.3×10^{4}	114	1.2×10^{4}
I_{ON}/I_{OFF}(low V_D=10,100mV)	10^4	3×10^{4}	3×10^{3}	2×10^{5}
SS(high V_D)(mV/dec)		5087	1000	216
SS(low V_D)(mV/dec)	3600	7368	833	189
I_{OFF}(V_D= -1V) (μA)		3×10^{-10}	8.5×10^{-8}	1.0×10^{-11}
I_{ON}(V_D= -1V) (μA)		4×10^{-6}	2.5×10^{-5}	1.2×10^{-8}
*Normalized I_{OFF}(μA)		9.0×10^{-9}	1.05×10^{-7}	1.40×10^{-9}
*Normalized I_{ON}(μA)		1.2×10^{-4}	3.07×10^{-5}	1.82×10^{-6}
DIBL(mV/V)		15000	421	87

Table 5.4: Comparisons of the existing Ge junctionless transistors [27-29]
* The I_{ON} and I_{OFF} (high V_D) were normalized by the W/L_{GATE}

5.4.3 Summary

In summary, JNT with Ge channels have been fabricated by a CMOS-compatible top-down process in this work. The transistors exhibit the lowest subthreshold slope to date for Ge junctionless devices. The devices with a gate length of 3 μm exhibit a *SS* of 216 mV/dec with an I_{ON}/I_{OFF} current ratio of 1.2×10^3 at V_D = -1 V and *DIBL* of 87 mV/V.

5.5 Conclusions

In this chapter, GeOI wafers were fabricated using Smart-Cut with low temperature direct wafer bonding method. A Preferential etch solvent was developed and used to decorate the defects on Ge during the GeOI fabrication. For the lithography and pattern transfer, a top-down process of sub-50-nm width Ge nanowires is developed in this chapter and Ge nanowires with 35 nm width and 50 nm depth are obtained using this process. With the developed modules, JNT with Ge channels have been fabricated by the CMOS-compatible top-down process. The transistors exhibit the lowest subthreshold slope to date for Ge junctionless devices, compared with the devices from literatures. The devices with a gate length of 3 μm exhibit a *SS* of 216 mV/dec with an I_{ON}/I_{OFF} current ratio of 1.2×10^3 at V_D = -1 V and *DIBL* of 87 mV/V.

5.6 References

[1] Ross IM. The invention of the transistor. P IEEE. 1998;86:7-28.

[2] Atalla MM, Tannenbaum E, Scheibner EJ. Stabilization of Silicon Surfaces by Thermally Grown Oxides. At&T Tech J. 1959;38:749-83.

[3] Goldstein A, Aspray W. Facets: New Perspectives on the History of Semiconductors: IEEE Center for the History of Electrical Engineering; 1997.

[4] http://eom.umicore.com/en/home/.

[5] Cheng Z, Taraschi G, Currie MT, Leitz CW, Lee ML, Pitera A, et al. Relaxed silicon-germanium on insulator substrate by layer transfer. J Electron Mater. 2001;30:L37-L9.

[6] Tezuka T, Moriyama Y, Nakaharai S, Sugiyama N, Hirashita N, Toyoda E, et al. Lattice relaxation and dislocation generation/annihilation in SiGe-on-insulator layers during Ge condensation process. Thin Solid Films. 2006;508:251-5.

[7] Ferain I, Byun K, Colinge C, Brightup S, Goorsky M. Low temperature exfoliation process in hydrogen-implanted germanium layers. J Appl Phys. 2010;107:054315--5.

[8] Byun KY, Ferain I, Fleming P, Morris M, Goorsky M, Colinge C. Low temperature germanium to silicon direct wafer bonding using free radical exposure. Appl Phys Lett. 2010;96:102110--3.

[9] Brunco D, De Jaeger B, Eneman G, Mitard J, Hellings G, Satta A, et al. Germanium MOSFET devices: Advances in materials understanding, process development, and electrical performance. J Electrochem Soc. 2008;155:H552-H61.

[10] Bean KE. Anisotropic etching of silicon. Electron Devices, IEEE Transactions on. 1978;25:1185-93.

[11] d'Aragona FS. Dislocation etch for (100) planes in silicon. J Electrochem Soc. 1972;119:948-51.

[12] Sirtl E, Adler A. Chromic Acid-Hydrofluoric Acid as Specific Reagents for the Development of Etching Pits in Silicon. Z Metallkd. 1961;52:529-34.

[13] Jenkins MW. A new preferential etch for defects in silicon crystals. J Electrochem Soc. 1977;124:757-62.

[14] Seiter H. Integrational Etching Methods. Semiconductor Silicon. 1977;3:187.

[15] Vogel F, Pfann W, Corey H, Thomas E. Observations of dislocations in lineage boundaries in germanium. Phys Rev. 1953;90:489.

[16] Souriau L, Atanasova T, Terzieva V, Moussa A, Caymax M, Loo R, et al. Characterization of threading dislocations in thin germanium layers by defect etching: Toward chromium and HF-Free solution. J Electrochem Soc. 2008;155:H677-H81.
[17] Schmeisser D, Schnell R, Bogen A, Himpsel F, Rieger D, Landgren G, et al. Surface oxidation states of germanium. Surface science. 1986;172:455-65.
[18] Zahler J, i Morral AF, Griggs M, Atwater HA, Chabal Y. Role of hydrogen in hydrogen-induced layer exfoliation of germanium. Phys Rev B. 2007;75:035309.
[19] Hayashi S, Goorsky M, Noori A, Bruno D. Materials Issues for the Heterogeneous Integration of III-V Compounds Exfoliation and Layer Transfer. J Electrochem Soc. 2006;153:G1011-G4.
[20] Desrosiers N, Giguère A, Terreault B, Chicoine M, Schiettekatte F. Implantation effects of low energy H and D ions in germanium at - 120° C and room temperature. Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms. 2008;266:1971-8.
[21] Kawase T, Nishitani K, Dei K, Uchikoshi J, Morita M, Arima K. Formation of Pyramidal-shaped Etch Pits on Germanium Surfaces Using Catalytic Reactions with Metallic Nanoparticles in Water.
[22] Colinge J-P. Multiple-gate soi mosfets. Solid State Electron. 2004;48:897-905.
[23] Toriumi A, Lee C-h, Nishimura T, Wang S, Kita K, Nagashio K. Recent progress of Ge technology for a post-Si CMOS. ECS Transactions. 2011;35:443-56.
[24] Ferain I, Colinge CA, Colinge J-P. Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors. Nature. 2011;479:310-6.
[25] Chau R, Boyanov B, Doyle B, Doczy M, Datta S, Hareland S, et al. Silicon nano-transistors for logic applications. Physica E: Low-dimensional systems and nanostructures. 2003;19:1-5.
[26] Huang X, Lee W-C, Kuo C, Hisamoto D, Chang L, Kedzierski J, et al. Sub 50-nm FinFET: PMOS. Electron Devices Meeting, 1999 IEDM'99 Technical Digest International: IEEE; 1999. p. 67-70.
[27] Zhao DD, Nishimura T, Lee CH, Nagashio K, Kita K, Toriumi A. Junctionless Ge p-channel metal–oxide–semiconductor field-effect transistors fabricated on ultrathin Ge-on-insulator substrate. Applied physics express. 2011;4:031302.
[28] Zhao DD, Nishimura T, Lee C-h, Ifuku R, Nagashio K, Kita K, et al. Junctionless Ge MOSFETs Fabricated on 10 nm-Thick GeOI Substrate. ECS Transactions. 2011;35:457-64.

[29] Zhao DD, Lee CH, Nishimura T, Nagashio K, Cheng GA, Toriumi A. Experimental and Analytical Characterization of Dual-Gated Germanium Junctionless p-Channel Metal-Oxide-Semiconductor Field-Effect Transistors. Jpn J Appl Phys. 2012;51:04DA3.

Chapter 6 Conclusions and Future Perspectives

The aim of the work was to evaluate the Si JNTs concept and advance it by using alternative channel material, such as Ge. TCAD simulation has been employed to compare JNTs with the IM devices. The results show that JNTs present many advantages such as superior gate control without abrupt junctions, relaxed vertical electric field, reduced capacitance, and simplified processing. On the other hand, some potential drawbacks of JNTs have been discussed and solutions have been suggested. Si JNTs down to 22 nm have been characterized under different conditions and configurations. Benchmarking of JNTs has been carried out with the most advanced IM devices. Furthermore, steeper subthreshold slopes can be achieved in JNTs at lower supply voltage, owing to the dynamic floating body effects, which exhibit potential to scale down the supply voltage further. An alternative channel material, Ge, has been explored as the extension of Si JNTs. In order to make Ge JNTs, GeOI fabrication, defects on Ge, nano-scale lithography and high-*k* passivation scheme for Ge have been studied. Eventually, with the developed modules Ge JNTs, which exhibit excellent gate control, have been fabricated and characterized. Comparison with the other Ge junctionless devices from literature has been carried out and it shows a promising result of our devices, which exhibit best *SS* and *DIBL* values to date. This can be attributed to small dimension of our nanowire like devices, hence, better gate control.

To implement Ge JNTs or even Ge IM devices into the semiconductor industry, the full range of Ge process technologies have to be developed, evaluated and then optimized.

(i) Wafer platforms

High quality ≥ 300 mm diameter GeOI wafers with a top Ge layer thicknesses of < 30 nm and a thickness variation of less than 3% are demanded. Alternative process approaches other than Smart-Cut need to be developed, which can potentially cost down the GeOI wafers to the level of SOI. Epi grown low-defect-density Ge layer from the SiO_2 trenches is promising to fabricate low cost Ge substrates from Si platform. It can be another option to implement Ge material into the semiconductor industry with a more economical process.

(ii) Gate stack

The high quality gate dielectric is one of the major challenges in realizing Ge CMOS. Good Ge dielectric interfaces with a low interface state density (D_{it}) is critical to achieve low values of the inverse subthreshold slope, high carrier mobility and associated high current drive. In this dissertation, thermally grown GeO_2 has been employed as the interfacial layer to reduce the D_{it}. Nevertheless, other different approaches have been made to form a dielectric layer with low interface states on Ge. They include various types of interfacial layers such as Si, oxynitrides, and different high-*k* dielectric materials. Novel processes have been investigated, i.e. sulphur passivation, high pressure thermal oxidation, vacuum ultraviolet-assisted oxidation, plasma oxidation, radical oxidation, direct neutral beam oxidation and plasma post-oxidation. Systematic evaluation has to be carried out and the qualified Ge gate stack should deliver competitive properties comparing with that in Si platform, especially for n-type Ge channel, in terms of *EOT*, D_{it}, gate leakage, etc.

(iii) Doping and Contract resistance

For the further downscaling of MOSFET devices, formation of ultra-shallow layers with high doping levels is mandatory. This in turn requires the use of dopants with a low diffusivity, a high solubility and a high activation and/or the application of advanced process techniques, which operate far away from thermal equilibrium and can exceed the solubility limitations. For potential p-type dopants in Ge it is known that boron has a low diffusivity (although its solubility is limited) and that Ga feature a very high solubility in the order of 5×10^{20} cm^{-3}. However, typical n-type dopants (P, As, Sb) have a significantly lower solubility in Ge than in Si and their diffusivity in Ge is higher than that of B or Ga. Thus, n^+ doping in Ge is much more challenging than p^+ doping, which needs attention for both channel and S/D doping. Beside the high level of doping, the formation of low resistivity contacts for p- and especially n-type Ge is very important for the fabrication of high-performance Ge JNTs. The focus will be put on formation of such contacts with n-type Ge since it is significantly more challenging. High contact resistance on n-type Ge is usually observed and it is mainly attributed to Fermi-level pinning (FLP), and subsequently to a large electron Schottky barrier height (eSBH). Contact scheme has to be selected among the potential solutions including: (i) ultra-thin amorphous insulating layers to terminate the free dangling bonds and

eliminate FLP, (ii) surface passivation to bond other impurity species to the dangling Ge bonds at the surface, and (iii) optimisation of a metal-semiconductor alloy, such as NiGe, in combination with high active doping concentrations underneath to create stable low-resistive contacts.

List of Publications

2013

1. S. Das, **R. Yu**, K. Cherkaoui, P. Razavi, and S. Barraudc, "Performance of 22 nm Tri-Gate Junctionless Nanowire Transistors at Elevated Temperatures", ECS Solid State Letters, 2 (8) Q1-Q4, 2013

2. M. Shayesteh, K. Huet, I. Toqué-Tresonne, R. Negru, C. L. M. Daunt, N. Kelly, D. O'Connell, **R. Yu**, V. Djara, P. B. Carolan, N. Petkov, and R. Duffy, "Atomically-Flat Low-Resistive Germanide Contacts Formed By Laser Thermal Anneal", IEEE Transactions on electron devices, accepted ,2013

3. R. Duffy, M. Shayesteh, I. Kazadojev, **R. Yu**," Germanium doping challenges", invited paper, IWJT, Kyoto, 2013

4. **R. Yu**, A.N. Nazarov, V.S. Lysenko, S. Das, I. Feraina, P. Razavi, M. Shayesteh, A. Krantic, R. Duffy, J.-P. Colinge, "Impact ionization induced dynamic floating body effect in junctionless transistors", Solid-State Electronics, 2013

5. **R. Yu**, Y. M. Georgiev, I. M. Povey, S. Das, N. Petkov, M. Shayesteh, D. O'Connell, J. D. Holmes, R. Duffy, "Ge Nanowire Junctionless Transistor", EuroSOI, France, 2013

6. **R. Yu**, Y. M. Georgiev, O. Lotty, B. McCarthy, N. Petkov, D. O'Connell, A. Nightingale, S. Das, J. D. Holmes, "Si Junctionless Transistor for Sensing Application: Subthreshold Region Sensor", EuroSOI France, 2013

2012

7. **R. Yu**, S. Das, I. Ferain, P. Razavi, M. Shayesteh, A. Kranti, R. Duffy, and J.-P. Colinge, "Device Design and Estimated Performance for p-TypeJunctionless Transistors on Bulk Germanium Substrates", IEEE Transactions on electron devices, Vol. 59, No. 9 ,2012

8. R. Hobbs, M. Schmidt, C. Bolger, Y. Georgiev, P. Fleming, M. Morris, N. Petkov, J. Holmes, F. Xiu, K. Wang, V. Djara, **R. Yu**, J.-P. Colinge, "Resist–substrate interface tailoring for generating high-density arrays of Ge and Bi_2Se_3 nanowires by electron beam lithography", Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures,Vol. 30, Issue 4, pp. 041602, 2012

9. P. Razavi, G. Fagas, I. Ferain , **R. Yu** , S. Das , J.-P. Colinge, "Influence of Channel Material Properties on Performance of Nanowire Transistors", Journal of Applied Physics, Vol. 111, Issue 12, 124509, 2012

10. N. D. Akhavan, I. Ferain, **R. Yu**, P. Razavi, J.-P. Colinge "Influence of discrete dopant on quantum transport in silicon nanowire transistors", Solid-State Electronics, Vol. 70, pp. 92-100, 2012

11. **R. Yu**, S. Das, Ri. Hobbs, Y. Georgiev, I. Ferain, P. Razavi, N. D. Akhavan, C. A. Colinge and J.-P. Colinge "Top-down Process of Germanium Nanowires using EBL Exposure of Hydrogen Silsesquioxane Resist", Proceedings Ultimate Integration on Silicon (ULIS), Grenoble, France, pp. 145-147, 2012.

12. P. Razavi, I. Ferain, S. Das, **R. Yu**, N. D. Akhavan, and J.-P. Colinge "Intrinsic Gate Delay and Energy-Delay Product in Junctionless Nanowire Transistors", Proceedings Ultimate Integration on Silicon (ULIS), Grenoble, France, pp. 125-128, 2012.

13. **R. Yu**, S. Das, I. Ferain, P. Razavi, N. D. Akhavan, C. A. Colinge and J.-P. Colinge "Simulation of Impact Ionization Effect in Short Channel Junctionless Transistors", Proceedings EUROSOI, pp. 37-38, 2012.

14. A.N. Nazarov, V.S. Lysenko, I. Ferain, S. Das, **R. Yu**, A. Kranti, N. Dehdashti Akhavan, P. Razavi, JP Colinge, "Floating body effects in junctionless MuGFETs", Proceedings EUROSOI, pp. 93-94, 2012.

2011

15. **R. Yu**, I. Ferain, N. D. Akhavan, P. Razavi, R. Duffy, and J.-P. Colinge, "Characterization of a junctionless diode", Applied Physics Letters, 99, 13502, 2011

16. R. Duffy, M. Shayesteh, B. McCarthy, A. Blake, M. White, J. Scully, **R. Yu**, A.-M. Kelleher, M. Schmidt, N. Petkov, L. Pelaz, LA Marqués, "The curious case of thin-body Ge crystallization", Applied Physics Letters, 99, 131910, 2011

17. K. Y. Byun, I. Ferain, **R. Yu**, C. Colinge, J. Ihm, H. Cheong, "Chemical Reactions and Mechanical Properties of the Directly Bonded Ge-Si Interface", 30th International Conference on the Physics of Semiconductors., Volume 1399, pp. 201-202 (2011)

18. K. Y. Byun, I. Ferain, J. Hayes, **R. Yu**, F. Gity, C. Colinge, "Surface activation using oxygen and nitrogen radical for Ge–Si Avalanche photodiode integration", Microelectronic Engineering, Vol. 88, Issue 4, pp. 522-525, 2011

19. N. Nazarov, I. Ferain, N. D. Akhavan, P. Razavi, **R. Yu**, J.-P. Colinge, "Field-effect mobility extraction in nanowire field-effect transistors by combination of transfer characteristics and random telegraph noise measurements", Applied Physics Letters, 99, 73502, 2011

20. R. Yan, A. Kranti, I. Ferain, C.-W. Lee, **R. Yu**, N. Dehdashti, P. Razavi, J.-P. Colinge, "Investigation of high-performance sub-50 nm junctionless nanowire transistors", Microelectronics Reliability, Vol. 51, Issue 7, 1166-1171, 2011

21. N. D. Akhavan, I. Ferain, P. Razavi, **R. Yu**, J.-P. Colinge, "Improvement of carrier ballisticity in junctionless nanowire transistors", Applied Physics Letters, 98, 103510, 2011

22. R. T. Doria, M. A. Pavanello, R. D. Trevisoli, M. de Souza, C.-W. Lee, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, **R. Yu**, A. Kranti, J.-P. Colinge, "Junctionless Multiple-Gate Transistors for Analog Applications", IEEE Transactions on electron devices,99, pp.1-9, 2011

23. J.-P. Colinge, A. Kranti, R. Yan, C.-W. Lee, I. Ferain, **R. Yu**, N. D. Akhavan, P. Razavi, "Junctionless Nanowire Transistor (JNT): Properties and design guidelines", Solid-State Electronics, Vol. 55-56, pp. 33-37, 2011

24. J.-P. Colinge, I. Ferain, A. Kranti, C.-W. Lee, N. D. Akhavan, P. Razavi, R. Yan, **R. Yu**, "Junctionless Nanowire Transistor: Complementary Metal-Oxide-Semiconductor Without Junctions", Science of Advanced Materials, Vol. 3, 3, pp. 477-482, 2011

25. N. D. Akhavan, A. Afzalian, A. Kranti, I. Ferain, C.-W. Lee, R. Yan, P. Razavi, **R. Yu**, J.-P. Colinge, "Influence of Elastic and Inelastic Electron–Phonon Interaction on Quantum Transport in Multigate Silicon Nanowire MOSFETs", IEEE Transactions on electron devices,Vol. 58, 4, pp.1029-1037, 2011

26. N. Nazarov, I. Ferain, N. D. Akhavan, P. Razavi, **R. Yu**, J.-P. Colinge, "Random telegraph-signal noise in junctionless transistors", Applied Physics Letters, 98, 092111, 2011

27. N. D. Akhavan, A. Afzalian, C.-W. Lee, R. Yan, I. Ferain, P. Razavi, **R. Yu**, G. Fagas, J.-P. Colinge, "Nanowire to Single-Electron Transistor Transition in Trigate SOI MOSFETs", IEEE Transactions on electron devices, Vol. 58, No. 1, 2011

28. R. T. Doria, M. A. Pavanello, R. D. Trevisoli, M. de Souza, C.-W. Lee, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, **R. Yu**, A. Kranti, J.-P. Colinge, "Analog Operation Temperature Dependence of nMOS Junctionless Transistors Focusing on Harmonic Distortion", Journal of Integrated Circuits and Systems, vol.6, No.1, pp. 114-121,2011

29. Kranti, C.-W. Lee, I. Ferain, R. Yan, N. Akhavan, P. Razavi, **R. Yu**, G.A. Armstrong, J.-P. Colinge, "Junctionless 6T SRAM cell", Electronics Letters, Vol.46 , Issue: 22, pp. 1491 – 1493, 2011

30. N. D. Akhavan, I. Ferain, P. Razavi, **R. Yu**, J.-P. Colinge, "Random dopant variation in junctionless nanowire transistors", 2011 IEEE International SOI Conference (SOI), pp. 55-56,2011

31. M. Shayesteh, R. Duffy, B. McCarthy, A. Blake, M. White, J. Scully, **R. Yu**, V. Djara, M. Schmidt, N. Petkov, A.-M. Kelleher, "Germanium Fin Structure Optimization for Future MugFET and FinFET Applications", ECS Transactions, Vol. 35, Issue 2, pp. 27-34, 2011

32. Nazarov, C.-W. Lee, A. Kranti, I. Ferain, R. Yan, N. D. Akhavan, P. Razavi, **R. Yu**, J.-P. Colinge, "Comparative Study of Random Telegraph Noise in Junctionless and Inversion-Mode MuGFETs", ECS Transactions, Vol. 33, Issue 5, pp. 73-78, 2011

33. J.-P. Colinge, A. Kranti, R. Yan, I. Ferain, N. D. Akhavan, P. Razavi, C.-W. Lee, **R. Yu**, C. Colinge, "A Simulation Comparison between Junctionless and Inversion-Mode MuGFETs", ECS Transactions, Vol. 35, Issue 5, pp. 63-72, 2011

34. R. T. Doria, M. A. Pavanello, R. D. Trevisoli, M. D. Souza, C.-W. Lee, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, **R. Yu**, A. Kranti, J.-P. Colinge, "The Roles of the Electric Field and the Density of Carriers in the Improved Output Conductance of Junctionless Nanowire Transistors", ECS Transactions, Vol. 35, Issue 5, pp. 283-288, 2011

35. P. Razavi, G. Fagas, I. Ferain, N. D. Akhavan, **R. Yu**, J.-P. Colinge, "Performance investigation of short-channel junctionless multigate transistors", Proceedings Ultimate Integration on Silicon (ULIS), Cork, Ireland, pp. 122-124, 2011.

36. A.N. Nazarov, C.W. Lee, A. Kranti, I. Ferain, R. Yan, N. D. Akhavan, P. Razavi, **R. Yu**, J.-P. Colinge, "Extraction of channel mobility in nanowire MOSFETs using Id (Vg) characteristics and random telegraph noise amplitude", Proceedings Ultimate Integration on Silicon (ULIS), Cork, Ireland, pp. 107-109, 2011.

2010

37. **R. Yu**, K. Y. Byun, I. Ferain, D. Angot, R. Morrison, C. Colinge, "Fabrication of Germanium-on-Insulator by low temperature direct wafer bonding", 2010 10th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), pp. 953-955, 2010

38. **R. Yu**, K. Y. Byun, F. Gity, J. Hayes, I. Ferain, C. Colinge and B. Corbett "Structural and Electrical Properties of Low Temperature Direct Bonded Germanium to Silicon Wafer for Photodetector Applications", ECS Transactions, Vol. 33, Issue 4, pp. 161-168, 2010

39. Kranti, R. Yan, C.-W. Lee, I. Ferain, **R. Yu**, N. D. Akhavan, P. Razavi, J.-P. Colinge, "Junctionless nanowire transistor (JNT): Properties and design guidelines", 2010 Proceedings of the European Solid-State Device Research Conference (ESSDERC), pp. 357-360, 2010

40. N. D. Akhavan, A. Afzalian, C.-W. Lee, R. Yan, I. Ferain, P. Razavi, **R. Yu**, G. Fagas, J.-P. Colinge, "Effect of intravalley acoustic phonon scattering on quantum transport in multigate silicon nanowire metal-oxide-semiconductor field-effect transistors", Journal of Applied Physics, Vol. 108 , Issue 3, pp. 034510-8, 2010

41. J.-P. Raskin, J.-P. Colinge, I. Ferain, A. Kranti, C.-W. Lee, N. D. Akhavan, R. Yan, P. Razavi, **R. Yu**, "Mobility improvement in nanowire junctionless transistors by uniaxial strain", Applied Physics Letters, 97, 042114, 2010

42. C.-W. Lee, A. N. Nazarov, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, **R. Yu**, R. T Doria, J.-P. Colinge, "Low subthreshold slope in junctionless multigate transistors", Applied Physics Letters, 96, 102106, 2010

43. J.-P. Colinge, C.-W. Lee, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, **R. Yu**, A. N. Nazarov, R. T. Doria, "Reduced electric field in junctionless transistors", Applied Physics Letters, 96, 073510,2010

44. N. Dehdashti, A. Kranti, I. Ferain, C.W. Lee, R. Yan, P. Razavi, **R. Yu**, J.-P. Colinge, "Emission and absorption of optical phonons in multigate silicon nanowire MOSFETs", Proceedings 14th International Workshop on Computational Electronics (IWCE), pp. 351-354, 2010

45. R. T. Doria, M. A. Pavanello, R. D. Trevisoli, M. de Souza, C.W. Lee, I. Ferain, N. D Akhavan, R. Yan, P. Razavi, **R. Yu**, A. Kranti, J.-P. Colinge, "Analog operation of junctionless transistors at cryogenic temperatures", IEEE International SOI Conference, pp. 72-73, 2010

46. K. Y. Byun, **R. Yu**, N. Saeidia, M. Flynna, I. Feraina, and C. Colinge, "Pattern Stamping Using Exfoliation for Heterogeneous Integration", ECS Transactions, Vol. 33, Issue 4, pp. 187-194, 2010

47. N. Saeidi, M. Flynn, K. Y. Byun, **R. Yu**, I. Ferain, C. Colinge, A. Demosthenous, N. Donaldson, "Developing a Wafer Level Gold-Polysilicon Eutectic Bond Process to Protect Sensitive Electronic Devices", ECS Transactions, Vol. 33, Issue 4, pp. 83-92, 2010

48. M. Flynn, N. Saeidi, K. Y. Byun, **R. Yu**, I. Ferain, C. Colinge, A. Demosthenous, N. Donaldson, "Characterization and Mechanical Reliability Evaluation

of Gold Polysilicon Eutectic Bonded Wafers", ECS Transactions, Vol. 33, Issue 4, pp. 103-112, 2010

49. R. T. Doria, M. A. Pavanello, C.-W. Lee, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, **R. Yu**, A. Kranti, J.-P. Colinge, "Analog Operation and Harmonic Distortion Temperature Dependence of nMOS Junctionless Transistors", ECS Transactions, Vol. 31, Issue 1, pp. 13-20, 2010

50. N. Dehdashti, A. Kranti, I. Ferain, C.-W. Lee, R. Yan, P. Razavi, **R. Yu**, J.-P. Colinge, "Dissipative transport in Multigate silicon nanowire transistors", 2010 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), pp. 97-100, 2010

51. C.-W. Lee, R. Yan, I. Ferain, A. Kranti, N. D. Akhvan, P. Razavi, **R. Yu**, J.-P. Colinge, "Nanowire zero-capacitor DRAM transistors with and without junctions", 2010 10th IEEE Conference on Nanotechnology (IEEE-NANO), pp.242-245, 2010

52. C.W. Lee, I. Ferain, A. Kranti, N. D. Akhavan, P. Razavi, R. Yan, **R. Yu**, B. O'Neill, A. Blake, M. White, A.M. Kelleher, B. McCarthy, S. Gheorghe, R. Murphy, J.-P. Colinge, "Short-channel junctionless nanowire transistors", Proc. SSDM, pp. 1044-1045, 2010

Book Chapter:

C. A. Colinge, K. Y. Byun, I. P. Ferain, **R. Yu** and M. Goorsky, (2008) "Low-Temperature Fabrication of Germanium-on-Insulator Using Remote Plasma Activation Bonding and HydrogenExfoliation", in an Edited book "Semiconductor-On-Insulator Materials for Nanoelectronics Applications" eds. Nazarov, A.; Colinge, J.-P.; Balestra, F.; Raskin, J.-P.; Gamiz, F.; Lysenko, V.S. (Eds.), Springer-Verlag Berlin Heidelberg (2011), ISBN 978-3-642-15867-4.

J. P. Colinge, C. W. Lee, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, A. Kranti and **R. Yu**, "Junctionless Transistors: Physics and Properties", in an Edited book "Semiconductor-On-Insulator Materials for Nanoelectronics Applications" eds. Nazarov, A.; Colinge, J.-P.; Balestra, F.; Raskin, J.-P.; Gamiz, F.; Lysenko, V.S. (Eds.), Springer-Verlag Berlin Heidelberg (2011), ISBN 978-3-642-15867-4.