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"Switching at the Contacts in $Ge_9Sb_1Te_5$ Phase-Change Nanowire Devices"

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Abstract

Phase-change random access memory is a promising approach to non-volatile memory. However, the inability to secure consistent, reliable switching on a nanometre scale may limit its practical use for high density applications. Here, we report on the switching behaviour of PCRAM cells comprised of single crystalline $Ge_9Sb_1Te_5$ (GST) nanowires. We show that device switching is dominated by the contacts and does not result in a resistance change within the bulk of the wire. For the devices studied, the typical contact resistance was ~30 kΩ, whereas the resistance of the GST channel was 1.8 kΩ. The applied voltage was predominately dropped across the passivating oxide on the surface of the GST nanowires, resulting in local resistive switching at the contacts and local power dissipation, which limited the endurance of the devices produced. The optimal device must balance low resistance contacts with a more resistive channel, to facilitate phase change switching within the nanowires. These results highlight the importance of contact formation on the switching properties in phase change devices and help guide the future design of more reliable neuromorphic devices.

Keywords: Neuromorphic, Switching, Contact resistance, Phase change, Nanowire

Introduction

The recent interest in neuromorphic computing has been facilitated by the emergence of devices that exhibit memristance and resistive switching behaviours. Many candidate materials systems have been investigated [1,2] and the chalcogenide-based phase-change memory (PCM) materials has emerged as a leading candidate for both optical data storage and next generation non-volatile memory [2,3] where differences in optical reflectivity or electrical resistance between amorphous and crystalline phases is used to store and manipulate information. Specifically, the application of electrical or optical pulses provide the means of switching in non-volatile PCM devices. In each case long duration low amplitude pulses are used to crystallize the material while short duration large amplitude pulses induce amorphization [4,5]. Improved scaling, low-power consumption and improved programming properties in non-volatile PCMs devices necessitate a better understanding of the crystalline-to-amorphous phase transition in these devices [6–8], including the minimum energy input required to effect this process. Thus, great efforts have been devoted to identifying PCMs with large ON/OFF ratios to facilitate the read operation. Charge injection by the contact metal electrode is necessary for electrical switching. To date, however, there has been limited study of the effect of contact resistance on the switching properties of non-volatile PCM devices [9,10]. As the device size is scaled down, the contact resistance effects between the PCM and the metal electrode become even more important in device performances [11,12].

One-dimensional materials such as nanowire (NW) structures are an ideal model system to investigate material and scaling properties of PCM operation at the nanometre scale due to their sub-lithographic size, defect-free single-crystalline structure, and unique geometry [6,7]. The tunability of the interface between the PCM nanowire and the metal electrode enables interface

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engineering, so that charge injection is controlled by the choice of metal electrode and work function, the influence of carrier concentration in the PCM through surface chemical modification and/or doping, and through the introduction or removal of interface trap states. As a result, the SET/RESET resistance ratio of PCM can be modulated using these principles so that it is not completely dominated by the change in the bulk electrical properties induced by a phase transition [13,14].

In this study, we report on the interface switching in a nanowire PCM cell that is accompanied by no measurable change in the bulk resistance of the PCM itself. These devices are comprised of the single crystalline $Ge_9Sb_1Te_5$ (GST) nanowires, whose composition is different from that of the better known prototypical phase change material $Ge_2Sb_2Te_5$ [15,16]. The new composition was chosen because of its lower resistivity to facilitate a reduction in power dissipation during device operation. The two- and four terminal devices of $Ge_9Sb_1Te_5$-based nanowire PCM cells were fabricated in order to study the electrical properties including the contact resistance. Through repeated switching and two- and four-probe testing, we show that the applied voltage is predominantly dropped across the contacts in $Ge_9Sb_1Te_5$ (GST) nanowire devices, leaving the channel of the device unaffected. We discuss the implications for device scaling and offer new insights into the development of alternative PCMs for future PCRAM applications.

Experimental Procedure

Single-crystalline germanium antimony telluride (GST) nanowires were grown by a chemical vapour deposition setup, utilizing gold as a catalyst in a vapour-liquid-solid (VLS) growth scheme [17]. GeTe (Alfa Aesar) and Sb_2Te_3 (Sigma-Aldrich) powders were used as the precursor source, and were placed in quartz boats within the reaction chamber. The Au catalyst was prepared by evaporating a 3 nm thick Au layer on a silicon wafer that was then placed at the downstream end of the tube furnace to act as the growth substrate. The furnace was heated to 600°C and maintained for 2 hours with a constant 200 sccm flow of high purity argon gas. $Ge_9Sb_1Te_5$ NWs resulted after 2-4 h of growth time while the chamber pressure was kept constant at 150 Torr. Dilute solutions of GST wires were dispersed in 400 ml isopropanol (IPA) and deposited on the substrate using a hand-spray. While it is known that solvent processing of nanowires can result in stress and hence a modification of the inherent resistance of the nanowire material, the presence of a passivation oxide layer on PC wires mitigates against any significant level of stress modulation [18]. The diameter of the $Ge_9Sb_1Te_5$ nanowires varied between 230 and 300 nm and were approximately 60 μm in length. After spinning resist on the sample, Electron Beam Lithography (EBL) was used to define the metal contacts on the wires. Each of the four metal contacts was comprised of a 5 nm Ti adhesion layer followed by 80 nm of Au, with 1 μm separation between each contact pad. The metal contacts were approximately 700 nm wide. After preparing the sample, a Keithley 4200-SCS parameter analyser was used to carry out the electrical measurements (I-V) and ultra-fast pulsing on the devices. One of the electrodes was held at ground and used as a reference throughout. The device as fabricated was symmetric and highly resistive. To overcome the latter, the contacts were electroformed in pairs by increasing the current compliance (I_{cc}) in a stepwise fashion until the resistance reached a minimum value.

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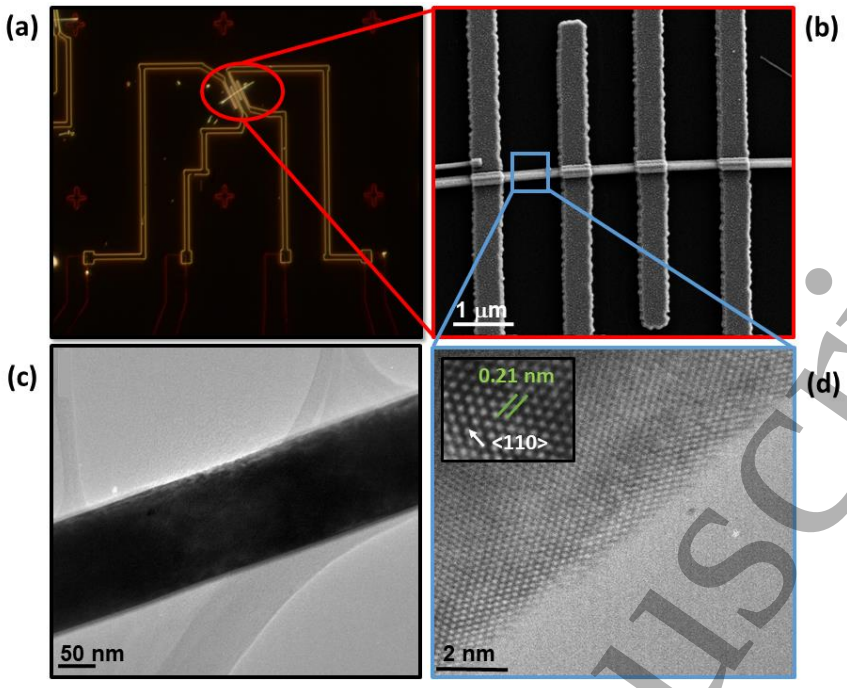


Figure 1. (a) Optical microscopy image of $Ge_9Sb_1Te_5$ device after three steps involving dropcast, EBL and contact metallization. (b) SEM image of the device, (c) TEM image of the bulk of nanowire. (d) The HR TEM image of the wire that shows hexagonal symmetry with a <110> growth direction and lattice spacing of 0.21 nm.

Figure 1(a) shows a representative optical microscopy image of an individual $Ge_9Sb_1Te_5$ NW device after EBL patterning and contact metallization. Figure 1(b) is a Scanning Electron Microscopy (SEM) image of the device contacted with four electrodes, and (c) depicts the Transmission Electron Microscopy (TEM) image of the nanowire, which shows the presence of a native oxide layer on the surface of the wire. Figure 1(d) shows a High Resolution TEM image that reveals a hexagonal symmetry pattern, similar to the hexagonal structure of $Ge_2Sb_2Te_5$ [7]. The spacing along the <110> growth direction was 0.21 nm, very similar to the prototype $Ge_2Sb_2Te_5$ nanowires reported by Jung et. al. [17]. The composition of the nanowires was confirmed by the TEM Energy Dispersive X-Ray (EDX) analysis and the atomic percentages resulting from EDX confirmed the $Ge_9Sb_1Te_5$ composition (See Fig. S1).

Results and discussion

To study the I-V characteristics of the device, we performed 5V voltage sweeps on pairs of electrodes E_{12}, E_{34} and E_{23}, respectively. Figure 2(a) shows a selection of I-V characteristics of the GST device after 31 continuous voltage sweeps between E_{12}. The value of I_{cc} is increased from 1nA to the maximum value of 20 μA in a step by step fashion. Clear hysteresis loops were observed for each sweep while the size of the loop progressively decreased. By sweep number 31 a linear response is observed and the hysteresis is eliminated, which means that the device defined by electrodes 1 and 2 has reached its lowest resistance value and exhibits ohmic behaviour. Fig. 2(b) shows the results of the same experiment between electrodes 3 and 4. The device defined by the electrodes reached its lowest resistance state without hysteresis after 41 continuous voltage sweeps. In both cases, the resistance reached a steady state value and was optimised using a compliance current of 20 μA. The resistance values defined by device sections E_{12} and E_{34} were 20 kΩ and 35 kΩ, respectively. To study the electrical status of the middle section of the device (E_{23}), which is the GST device channel, the I–V characteristics

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were measured and showed an immediate linear response without any evidence of hysteresis even after the first voltage sweep (Fig. 2(c)).

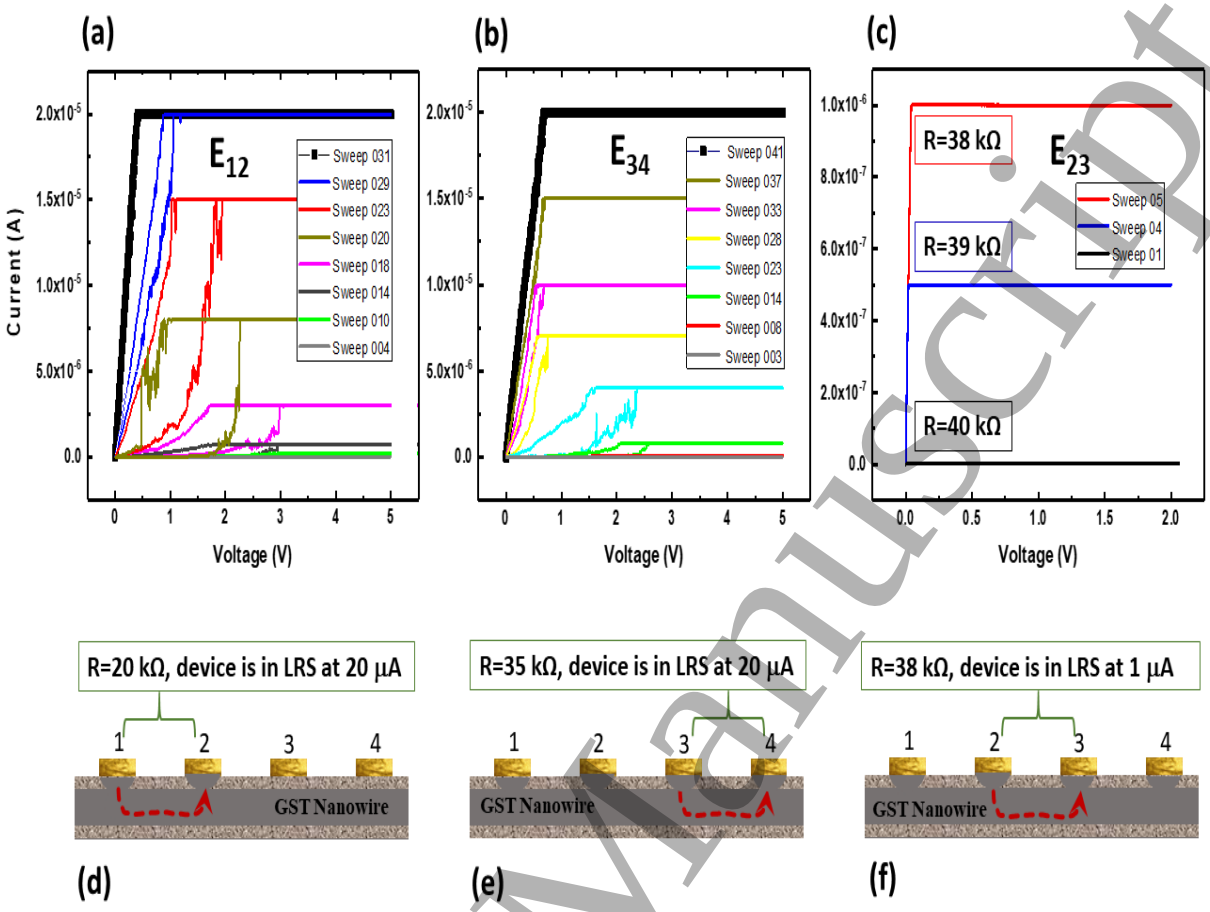


Figure 2. (a) (b) and (c) show a selection of I-V characteristics of the GST device for E_{12} and E_{34} and E_{23} at increasing current compliances. (d) (e) and (f) are schematic diagram of the device in the low resistance state (LRS).

To optimise the resistance of the GST device defined by electrodes 2 and 3, the current compliance I_{cc} was increased from 10 nA to 1 µA over 5 different voltage sweeps yielding a value of 38 kΩ at an I_{cc} of 1µA. The reason for the gradual reduction in the E_{23} resistance without the presence of hysteresis is due to the gradual change in the contact areas at electrodes 2 and 3, which had been initially formed in response to an electrical field with electrodes 1 and 4, respectively, but subsequently evolves in response to the applied field between electrodes 2 and 3. The sequential electrical activation of the GST device is shown schematically in Fig. 2(d), (e) and (f).

Four terminal electrical measurements of the GST nanowire device were performed to measure the resistance of the contacts and the resistivity of the pristine crystalline device channel, as shown in Fig. 3(a). A constant current source was applied on E_{14} while the resistance was measured across electrodes 2 and 3 (E_{23}). The objective was to determine the initial resistivity of device channel and the amount of power dissipation at the contacts. The resistance of the device channel was measured in Fig. 3(b) to be 1.8 kΩ, independent of the drive current.

Figure 3(c) shows the SEM image of the device including the details of the profile, length and diameter of the nanowire. A calculation of the resistivity using $R=\rho L/A$, yields a value $\rho = 7.8 \times 10^{-5}$ Ω.m. We note this value is significantly lower that the resistivity of $Ge_2Sb_2Te_5$, which is known to be 4.16×10^{-4} (Ω.m) [15,16]. Moreover, the resistance of the contacts to the GST

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device channel E_{23} was found to be 36.2 kΩ (38 kΩ -1.8 kΩ), some twenty times the resistance of the channel itself.

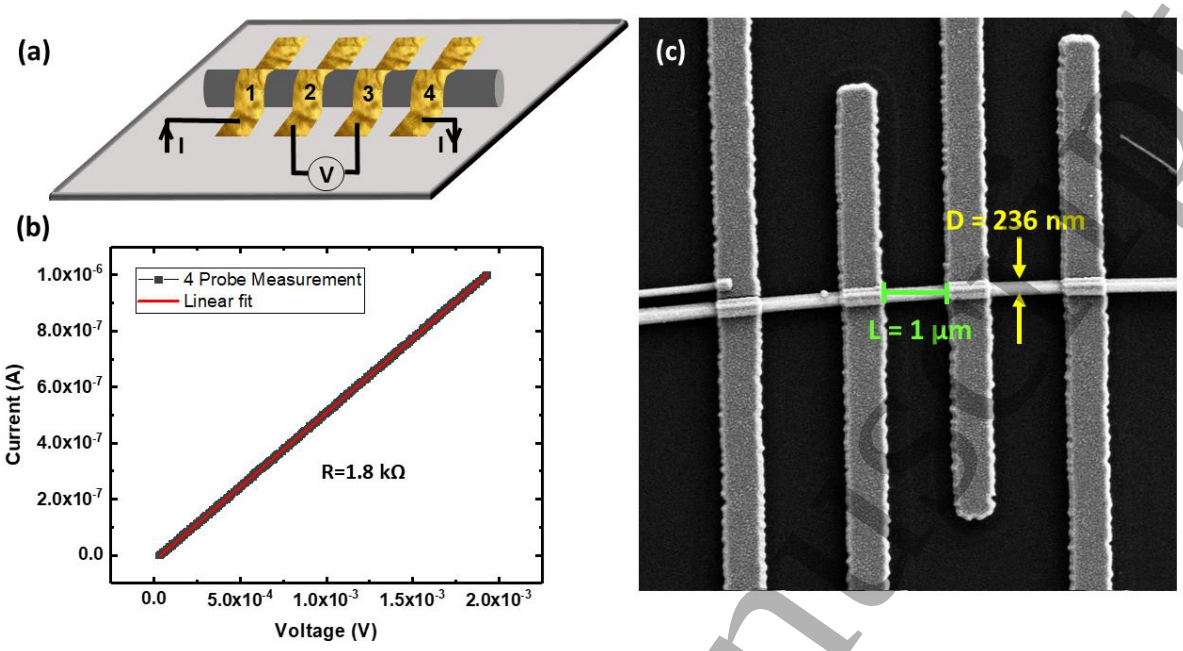


Figure 3. (a) Basic schematic showing the four-terminal resistance measurement method. (b) The I-V characteristics of middle contacts (E_{23}) showed a linear behaviour and from which 1/slope gives the resistance value (c) SEM image of the device containing the details of profile width and diameter of the device used to estimate the channel resistivity.

To study electrical switching in our device, a series of ultra-fast switching pulses (100 ns width) and of increasing voltage, were applied to E_{23} prior to the I-V measurement, with the device initially in the pristine low resistance ON state. After each measurement, the condition of the device was probed using a 20 µsec wide 300 mV triangle wave pulses (see Fig. 4). Figure. 4 (a-d) shows the status of the GST device after the application of 100 nsec pulses with amplitudes of 600 mV, 800 mV, 1.1 V and 1.2 V. The probe pulse train is shown in black and the current response in red. The device is still in the ON state after the application of sequential 600 mV and 800 mV pulses, consistent with a two-probe resistance level of around 30 kΩ similar to that found in Fig. 2(c). The application of a 1.1 V pulse results in an increase in the device resistance as measured by the reduction in the current response (see Fig. 4(c)). The application of a 1.2 V pulse caused the device to switch into a high resistance (>10^6 Ω) OFF state. The observed three order of magnitude resistance difference between the ON and OFF states is typical of PCM devices. The insets in Fig. 4(d) shows a schematic that illustrates two possible OFF states; reflecting amorphization in the body of the wire channel, i.e. normal device switching, or a failure at one or both of the contacts. In order to test which of these possibilities corresponds to the OFF state, we explore the I-V characteristics at both E_{12} and E_{34}.

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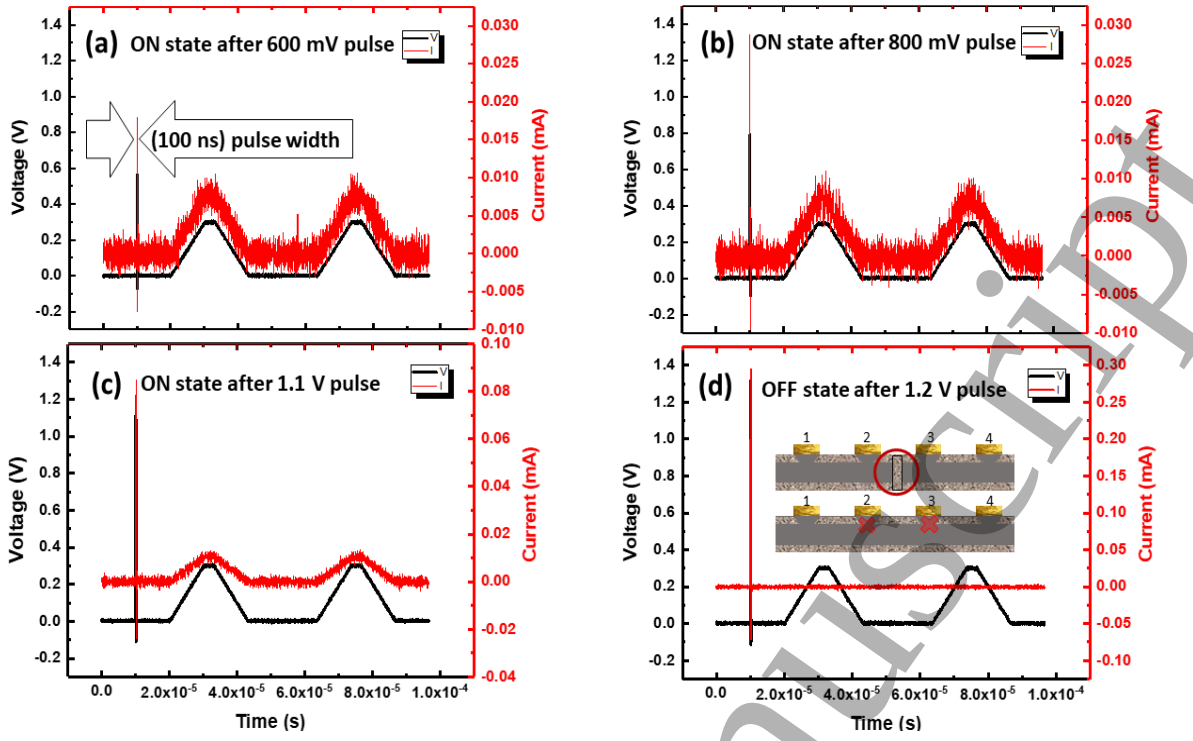


Figure 4. Illustrates the I-V characteristics of GST device after application of fast 100 ns voltage pulse of magnitudes (a) 600 mV, (b) 800 mV, (c) 1.1 V and (d) 1.2 V at E_{23}. The device current response (red curve) following each pulse is probed using a low voltage triangular pulse (black curve). After (d) the device is in the OFF state and the insets schematically shows of two different amorphization states of device, for which the dislocation lines and defects are predicted to exist either around the contacts or in the bulk of wire. The latter are depicted by red crosses and a circle, respectively.

Figure 5(a) shows the behaviour of E_{12} after voltage sweeps at current compliances of 10μA and 20μA. The section of the device is still in the ON state after the application of the 1.2 V 100 ns pulse to E_{23}, with a measured resistance is 29kΩ, which is close to the originally measured value in Fig. 2(a). Since the fast probe pulses were applied to E_{23}, we next examined the status of E_{34}. Figure 5(b) shows clear evidence of hysteresis loops and after successive I-V sweeps at increasingly higher compliance current, the resistance of this device section returned to its original value. This demonstrates that contact 3 switched during the application of the 100 ns pulses to E_{23}. To confirm that this is indeed was the case, or whether the body of the wire and contact 3 could have simultaneously switched during the pulse application, we studied the behaviour of E_{23}. Figure 5(c) clearly shows that the middle section of the device is in the ON state so that switching is confined to the contact.

Four contact I-V measurements were then carried out again as depicted in Fig. 3 to measure the resistivity of the middle section of the wire after pulsing. The resistance value was found to be unchanged at 1.8 kΩ, and conclusively demonstrates that the crystalline phase of the wire has not been affected by the pulsing operation. Comparing the 2-contact (38 kΩ) and 4-contact (1.8 kΩ) resistance measurements allows us to evaluate the power dissipation in different regions of the device. Clearly, the voltage drop associate with each pulse occurred predominantly within the contact region where it induces resistive switching rather than amorphization within the bulk of the wire.

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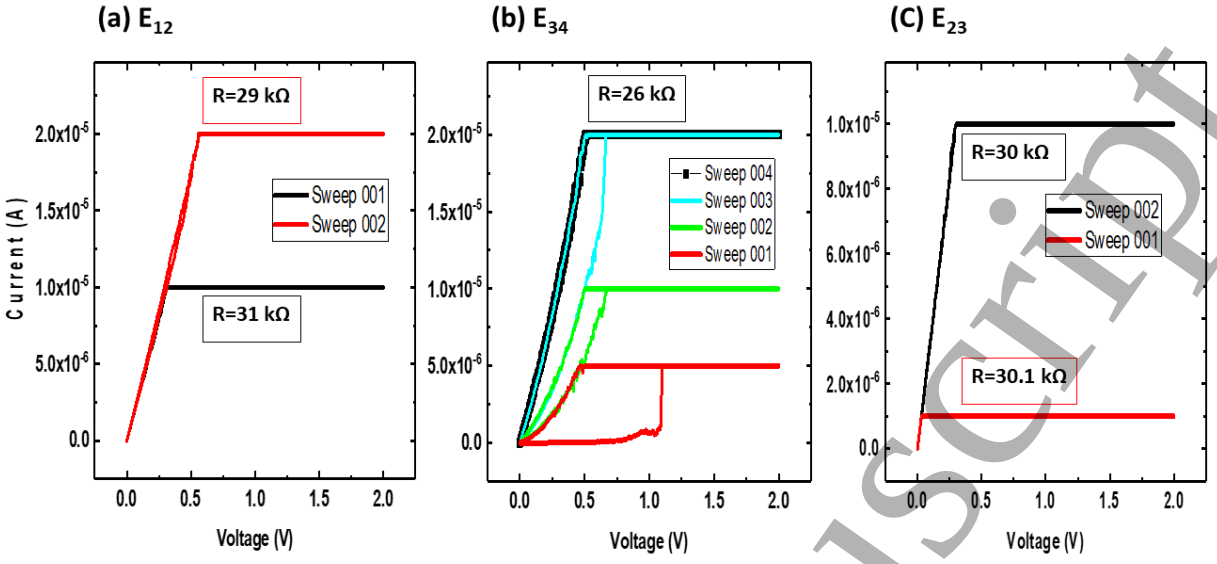


Figure 5. Sequential electrical measurements (a) E_{12}, I-V characteristics after two voltage sweeps, which illustrates the section of device, is still in the ON state. (b) E_{34}, I-V characteristics shows that switching has occurred at electrode 3 during the pulsing sequence and that the contact can be restored to its original value after successive I-V sweeps at increasing current compliance. (c) The linear behaviour of the E_{23} shows that device was switched from an amorphous phase after ultra-fast pulsing into the crystalline phase.

In scaling down memory cells, contact resistance between phase change material and the electrodes becomes a dominant factor in determining the memory cell resistance and performance [12,14,19]. To illustrate this, consider a nanowire of channel length L and radius r that is contacted by a metal electrode of width d. To maintain the resistance of the channel a reduction in channel length to $L/2$ must be accompanied by a reduction in radius by $r/\sqrt{2}$, but a commensurate reduction in the electrode width d will actually lead to an increase in the contact resistance by a factor of 4. The balance between the resistances of the contacts and the channel is crucial for device operation. In the present case, the contact resistance is approximately 20x the channel resistance, which causes the voltage drop and power dissipation to occur predominantly at the contacts [20,21]. This results in resistive switching at the contacts (presumably via the resistive oxide layer at the nanowire surface, cf. Fig. 1), preventing a current induced phase change within the wire channel. It is well established the reduction in contact resistance leads to improvement in memory cell performance [20-22]. On the other hand, device geometry is also known to influence switching and endurance of the memristor devices [22-25]. This is particularly true for nanowire devices where the contacts are on the wire surface, so that device operation requires charge injection into and out of the wire in addition to scattering in the vicinity of the contacts to effect charge transport along the wire channel itself. In contrast, for planar devices the applied electric field facilitates charge injection into the device, through the PCM and into the collector electrode. For devices of similar dimensions and materials the contact resistance will always be greater for nanowire devices compared to planar devices. In the present case, the failure of the device to switch can also be attributed to the composition of the device channel. The high concentration of Ge and low concentration of Sb in $G_9Sb_1Te_5$ is responsible for the reduced resistivity compared to $Ge_2Sb_2Te_5$ [26,27]. It is likely that switching is possible for $G_9Sb_1Te_5$ nanowire devices if the diameter can be reduced significantly below 100 nm.

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Conclusion

Four terminal PCM devices comprised of single crystalline $Ge_9Sb_1Te_5$ (GST) nanowires were fabricated and their electrical properties investigated by 2-probe and 4-probe I-V measurements. The device contacts were formed through a series of voltage sweeps at increasingly higher current compliances during which hysteresis loops in the I-V characteristics gradually evolved into an ohmic behaviour. The optimised resistance of the contacts were measured to be at least 20 times that of the wire channel. Device switching induced by 100 ns voltage pulses yielded an ON/OFF ratio in excess of 10^3, however the high resistance state was associated with resistive switching at the device contacts rather than amorphization of the PCM. This behaviour is attributed to the high contact resistance and low resistivity of the channel PCM, which results in power dissipation to be concentrated at the contacts. We speculate that voltage drop at the contacts is due to the presence of a native oxide layer on the surface of the wire. This layer was present in previously published studies of GST devices but did not impact performance. Use of more conducting materials such as those described here may be possible by eliminating the oxide layer before contact metallization using an ICP etcher with Argon gas. These result points to the challenges of scaling PCM nanowire-based device and the importance of choosing the channel materials with a resistivity and dimensions that are commensurate with the resistance of the contacts.

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