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Review

Photonic Packaging: Transforming Silicon Photonic Integrated Circuits into Photonic Devices

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Abstract: Dedicated multi-project wafer (MPW) runs for photonic integrated circuits (PICs) from Si foundries mean that researchers and small-to-medium enterprises (SMEs) can now afford to design and fabricate Si photonic chips. While these bare Si-PICs are adequate for testing new device and circuit designs on a probe-station, they cannot be developed into prototype devices, or tested outside of the laboratory, without first packaging them into a durable module. Photonic packaging of PICs is significantly more challenging, and currently orders of magnitude more expensive, than electronic packaging, because it calls for robust micron-level alignment of optical components, precise real-time temperature control, and often a high degree of vertical and horizontal electrical integration. Photonic packaging is perhaps the most significant bottleneck in the development of commercially relevant integrated photonic devices. This article describes how the key optical, electrical, and thermal requirements of Si-PIC packaging can be met, and what further progress is needed before industrial scale-up can be achieved.

Keywords: photonics packaging; silicon photonics; integrated optics; optoelectronics; photonic integrated circuits (PICs)

1. Introduction

The last decade has seen Si-photonics promoted as a platform for potentially revolutionary advances in the fields of Telecommunications, Data Communications, Medical Technology, Security, and Sensing [1–3]. The main driving force behind Si-photonics is the potential to realize small, highly integrated, photonic sub-systems that leverage off the decades of fabrication experience, technology, and scalability already developed for CMOS (complementary metal-oxide semiconductor) electronics [4]. Ultimately, the goal is the development of low-cost high-volume photonic integrated circuits (PICs) with integrated electronics, to simultaneously access the full potential of the silicon platform—i.e., Si-photonics for high-speed signaling and sensing, and CMOS-electronics for subsequent logical operations and computations [5].

An impressive array of Si-photonic elements has been demonstrated by researchers, and are now available as qualified 'building blocks' in the multi-project wafer (MPW) runs offered by several silicon foundries [6–8]. These include one-dimensional (1D) and two-dimensional (2D) grating-couplers, broadband edge-couplers, strip/rib waveguides and crossings, multi-mode-interference (MMI) splitters, echelon and arrayed waveguide (AWG) multiplexers/de-multiplexers, thermally-tunable

micro-ring resonators, high-speed Ge photodiodes, thermo-optic phase shifters, electro-absorption modulators (EAMs), etc. Literally thousands of these photonic elements, and perhaps dozens of simple Si-PIC (photonic integrated circuit) designs, can be laid-out on the single MPW 'block' (usually 10–30 mm^2) that is typically used by academic researchers and small-to-medium enterprises (SMEs) as their test-bed for photonic designs. However, developing innovative PICs, and demonstrating their functionality in a laboratory environment, either on an optical-bench or in a probe-station, is only the first step towards realizing useful devices that can attract investment and generate interest and value in the market. Very often, the technical challenges associated with transferring an Si-PIC from the laboratory to a device are underestimated, or even completely overlooked at the Si-PIC design phase, leading to significant performance penalties and unnecessarily high fabrication costs in first-generation prototypes.

'Photonic Packaging' is the catch-all term used to describe the range of techniques and technical competencies needed to make the optical, electrical, thermal, mechanical (and sometimes chemical) connections between a PIC and the outside world [9–12]. While Fiber-to-PIC coupling is perhaps the best-known aspect of photonic packaging, the field also includes the integration of laser-chips, micro-optics, electronic-chips, and micro-fluidics on PICs; the high-speed (25 Gbps) routing and impedance-matching of transmission-lines from external connectors to the microscopic photonic components on the PIC; and the efficient thermal cooling and thermal-stabilization needed to keep the PIC within its operational range—see Figures 1 and 2.

While satisfying any one of these photonic packaging requirement can be trivial, especially with the tools and resources a laboratory environment, they can be difficult to realize in a robust, stand-alone device for prototyping in the field. This is especially the case in more advanced photonic devices, where there is the simultaneous need for several different varieties of packaging, i.e., multi-channel Fiber-to-PIC coupling, a vertically integrated driver-chip, and a high-speed connection, and a thermo-electric cooler [12]. To ensure that these devices are fully-functional when fabricated and assembled requires the adoption of packaging design rules (PDRs) up front, at the Si-PIC design stage. This article provides a review of the different optical, electrical, and thermal considerations for successful photonic packaging, as a PDR 'primer' that also highlights some current trends that are helping to scale packaging to commercial volumes of photonic devices.

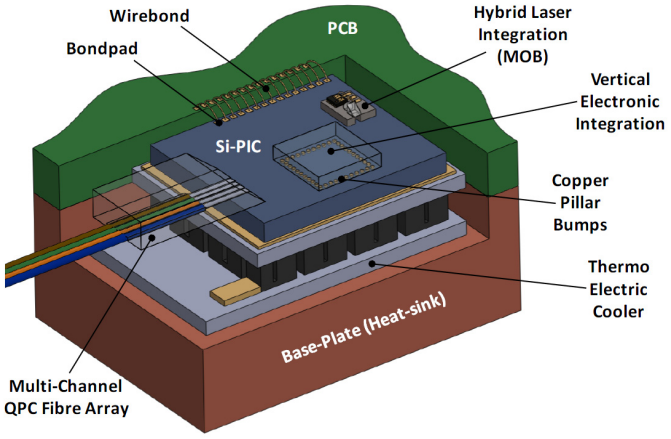


Figure 1. Schematic of a Si-PIC (photonic integrated circuit) packaged with a multi-channel quasi-planar coupled (QPC) fiber-array, a hybrid-integrated laser source based on a micro-optic bench (MOB), a vertically integrated electronic integrated circuit (EIC), and a thermo-electric cooler. Electrical connections between the PIC and PCB (printed circuit board) are made by wire-bonds, while the connections between the PIC and EIC are made using copper pillar bumps (CPBs).

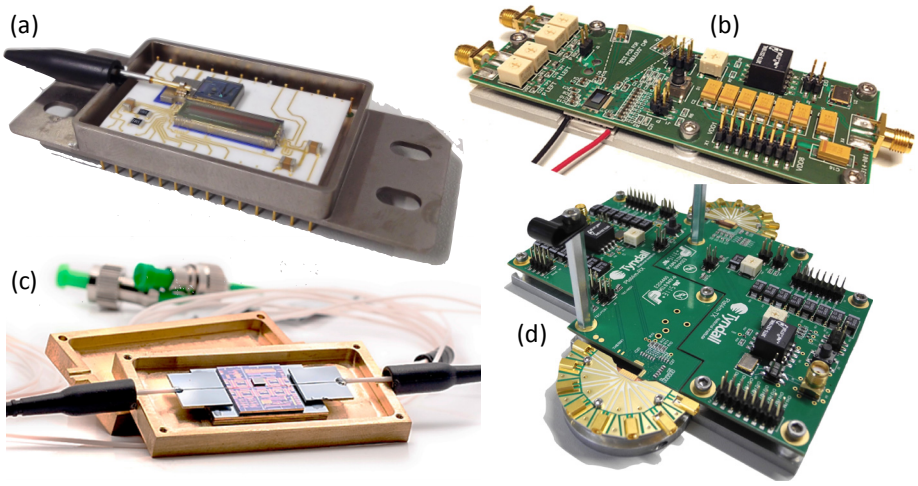


Figure 2. Examples of packaged photonic modules; (**a**) Single-channel PIC with side-by-side electronic integration; (**b**) Optical Network Unit (ONU) of the FP7-FABULOUS project; (**c**) Single-channel in/out photonic module with vertically integrated electronic chip; (**d**) 8-Channel Transceiver for the FP7-PLAT4M project.

2. Optical Packaging

As an indirect-gap semiconductor, Si offers very low direct-gap recombination for diode-laser emission. Therefore, the light signal needed to drive Si-photonics must come from an external laser source, either indirectly (i.e., the fiber-coupling of light from a discrete laser-device), or directly (i.e., the hybrid/heterogeneous integration of a III–V device/material on the Si-PIC). Many applications exist for both the indirect and direct coupling of laser light to the PIC, and each approach can be further broken down by the employed coupling scheme, i.e., grating-coupling, edge-coupling, evanescent-coupling, etc. Generally, Fiber-to-PIC coupling (indirect) is used for telecom and datacom applications, because it allows for the transfer of information over fiber networks, while integrated sources (direct) are used for security and sensing applications.

2.1. Fiber-to-PIC Coupling

The main challenge associated with transferring light between a telecom single-mode fiber (SMF) and the typical waveguides on a Si-PIC is the large difference between the mode-field diameter (MFD) of the two material systems. At telecom wavelengths (1260–1650 nm), the MFD in the fiber is approximately 10 μm and circularly symmetric, while in the PIC it is typically elliptical and 0.5×0.3 μm in size [13]. Consequently, in addition to an order of magnitude difference in the mode sizes between the two waveguides, there can also be a strong polarization dependent loss (PDL), if the unknown and unstable direction of the electric-field in the SMF-mode does not align with the fundamental polarization of the PIC waveguide (usually TE (transverse-electric) for telecoms and datacoms applications, and TM (transverse-magnetic) for sensing applications). As a result, it is often necessary to implement some form of 'polarization management' to ensure stable Fiber-to-PIC coupling—either directly in the coupler-element itself (as in the case of a 2D grating-coupler [14]), or at a later stage in the PIC (such as a wave-guide element that filters and rotates the polarization as necessary [15]). As more fully described in the following three sub-sections, there are essentially three approaches to Fiber-to-PIC coupling—edge-coupling, grating-coupling, and most recently evanescent-coupling—each having their own performance advantages and limitations, and so suiting particular photonic applications. A summary of the typical insertion-loss, bandwidth, and alignment tolerance for these different Fibre-to-PIC coupling approaches is given in Table 1.

2.1.1. Edge-Coupling

Edge-coupling is a well-established approach for the commercial packaging of laser-chips [16], but has not been widely adopted in the field of Si-photonics, despite being able to deliver broadband, polarization-agnostic insertion-losses of better than −1 dB after careful alignment [17]. A typical edge-coupler for a Si-PIC consists of an inverted taper (with a length of 100–300 μm) embedded in an integrated nitride-based spot-size-converter (SSC), or a post-process deposited polymer-based SSC, to increase the effective MFD of the on-PIC waveguide mode to approximately 3 × 3 μm [18,19]. This creates good modal-overlap with either lensed SMF-28 fibers or ultra-high numerical aperture (UHNA) fibers for Fiber-to-PIC coupling—see Figure 3.

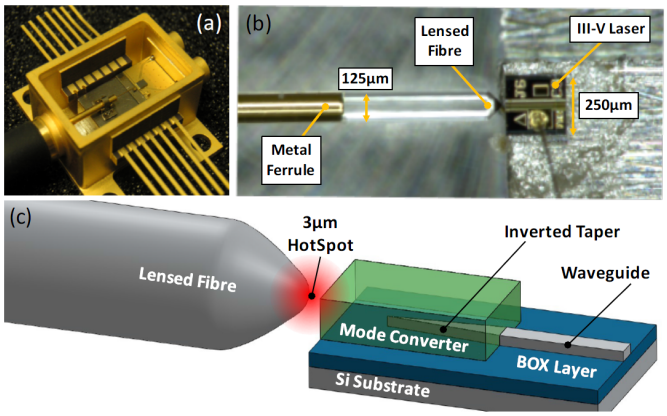


Figure 3. Fiber-to-PIC edge-coupling; (**a**) Kovar 'butterfly' package for edge-coupling. Kovar has the same thermal expansion coefficient as glass, so the Fiber-to-PIC alignment can be maintained, when the ambient temperature changes; (**b**) Microscope image of an edge-coupling to a III-V laser-chip using a lensed fiber. The fiber is mounted into a metal ferule, so it can be laser-welded to the kovar butterfly package; (**c**) Schematic of edge-coupling to a Si-PIC using a lensed-fiber and spot-size converter (SSC), or mode-converter (MC), to help bridge the gap between the mode-size in the fiber and on-PIC waveguide.

Since the back-end deposition and etching of a 3–5 μm SiON-layer needed to create an integrated mode-adapter has proven difficult to add as a standard building block (mainly because of the high strain introduced to the wafers by the SiON layer), edge-couplers are only slowly being introduced to the MPW runs being offered by the Si-Photonic foundries. Adding an edge-coupler onto a Si-PIC also increases post-fabrication processing costs, because it calls for either accurate dicing and polishing of the PIC edges, or an additional deep-etch (>60 μm) lithography to create a high-quality facet for low insertion-losses [6]. Deep etching techniques can even be taken further, to simultaneously create a facet and v-grove in which the fiber can be passively aligned with respect to the on-PIC waveguides [20]. The principle draw-back of this approach is that the v-grooves can occupy a significant fraction the Si-PIC footprint that would otherwise be available for the active part of the photonic device.

Most often, edge-coupling is carried-out between a PIC and a lensed-fiber. The lensing of the fiber facet creates a 3 μm diameter 'hot-spot' of light that better matches the fiber-mode to the MFD of the on-PIC SSC. The 1 dB alignment tolerance for such an edge-coupler is typically sub-micron (approximately ±500 nm), and so requires careful active alignment to minimize insertion-losses [18,19]. Given that this alignment tolerance is comparable to the fabrication tolerance of multi-channel fiber-arrays, edge-coupling is almost always applied only to single-channel Fiber-to-PIC coupling. In addition, laser-welding of the lensed-fiber (mounted in a metallic ferrule) and the PIC to a kovar package is usually necessary to ensure that the small displacements caused by thermal expansion/contraction do not impact the Fiber-to-PIC coupling (kovar is a Fe-Ni-Co alloy designed to have a thermal expansion coefficient that matches the glass in the fiber)—see Figure 3. In addition, this metal-to-metal bond is less prone to the small alignment-drift that sometimes occurs in epoxy-bonds

due to age or environmental effects [16]. Clearly, the alignment tolerance and material requirements of current state-of-the-art edge-coupling are too high to credibly satisfy medium-to-high volumes (10^6–10^7 devices per year).

Edge-coupling is often used for non-linear applications in Si-photonics, where high optical powers (on the order of 1 W) are needed to drive four-wave mixing and other non-linear interactions. The broadband nature of the edge-coupler means that the relative strengths of the pump, signal and idler channels can be measured accurately (because all three wavelengths experience the same insertion-loss), and this allows the non-linear conversion efficiencies to be calculated precisely. To prevent damage to the mode-adapter, modules for non-linear applications with edge-couplers must be fabricated in a hermetically sealed package. Otherwise, the electric-field gradient of the 'hot-spot' formed by the high optical power being focused by the lensed fiber can result in an optical tweezer effect that attracts micro-particles and organic contaminants in the air to the facet of the mode-adapter. If these contaminants absorb a significant fraction of the optical-power, then it can give rise to a catastrophic failure of the mode-adapter, due to localized heating of the facet. Such failures are more common for SU-8 and PMMA mode-adapters, rather than for integrated SiON mode-adapters, because the dielectric material is more resistant to thermal decomposition than the polymer photoresists.

A number of research groups and companies are working to develop schemes that reduce the alignment tolerance of edge-coupling [21,22]. The aim is to relax the alignment tolerance (or strengthen the fabrication tolerance [23]) to a level that supports multi-channel edge-coupling for telecom and datacom applications. This activity is motivated by the lower insertion losses and more broadband coupling that would be offered by these edge-coupler arrays, compared to the current (dominant) alternative of grating-coupler arrays. The losses and bandwidth of current MPW grating-couplers are routinely identified by companies and standardization bodies as significant barriers to the commercial adoption of photonic devices.

2.1.2. Grating-Coupling

The most common alternative to edge-coupling is grating-coupling, where a sub-μm periodic structure is lithographically etched into the waveguide-layer of the PIC, to create a coherent interference condition that diffractively couples the fiber-mode into the PIC waveguide [24,25]—see Figure 4. The 10 × 10 μm footprint of the grating-coupler is chosen to match the 8–10 μm MFD of a standard telecom fiber, and consists of a (periodic) array of ≈20 trenches partially-etched into the 220 nm Si-layer [12]. A simple relation exists between the peak wavelength of the coupler (λ), the pitch of the trenches (P), the effective index of the grating-coupler region (n_e), the index of the oxide-layer (n_o), and the angle-of-incidence (θ) of the fiber-mode: $\lambda = P\,(n_e - n_o \sin\theta)$, where the value of n_e is determined by the etch-depth and duty-cycle of the trenches, as well as the polarization of the fiber-mode. Typically, a near-normal angle-of-incidence ($\theta \approx 10^\circ$) is used, to provide directionality to the coupled-mode, and to reduce back-reflections into the fiber. However, from a packaging perspective, Fiber-to-PIC coupling at near-normal incidence—i.e., 'pigtailing'—can lead to a bulky device with poor mechanical performance. To address this issue, a 'quasi-planar' approach has been developed for Fiber-to-PIC coupling, where the fiber facet is polished to ≈40° to create a total internal reflection condition the directs the fiber-mode onto the grating-coupler at the correct angle of 10° [26,27]—see Figure 5. This geometry creates an almost '2D' package in which it is easier to respect the minimum-turn-radius of the telecom fibers (≈5 cm), while maintaining a reasonable device footprint.

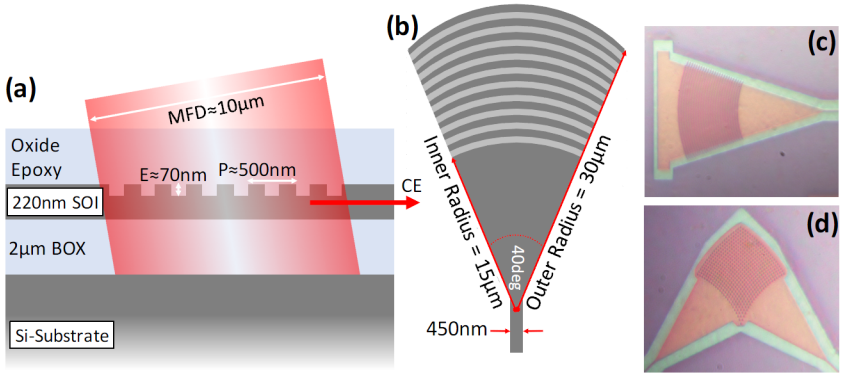


Figure 4. Fiber-to-PIC grating-coupling; (**a**) Side-view schematic of a silicon-on-insulator (SOI) grating-coupler, with a 2 μm bottom-oxide (BOX) layer. The ≈10 μm MFD (mode-field diameter) fiber-mode is incident on the grating-coupler with $a \approx 10^{\circ}$ angle-of-incidence; (**b**) Top-view schematic of a 1D focusing grating-coupler. The footprint of the coupler matches the MFD of the fiber-mode; (**c**,**d**) Microscope images of one-dimensional (1D) and two-dimensional (2D) grating-couplers, respectively.

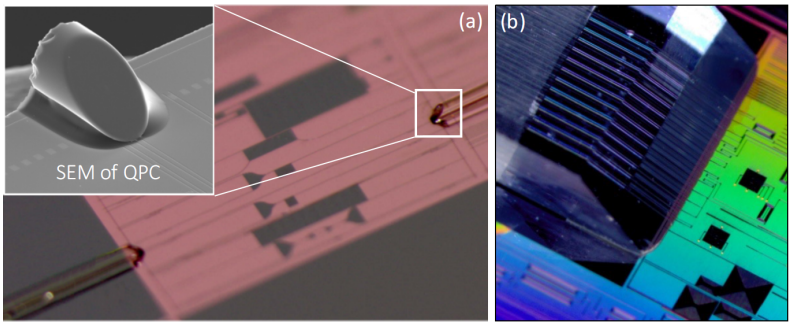


Figure 5. Quasi-planar Coupling (QPC) geometry to allow for the 'horizontal' Fiber-to-PIC grating-coupling; (**a**) Single-channel in/out QPC fiber-coupling to a Si-PIC, with an inset showing a schematic of the polished fiber facet; (**b**) QPC fiber-coupling using a multi-channel fiber-array.

Grating couplers offer significantly more relaxed alignment tolerance than an edge-coupler, typically ±2.5 μm of in-plane misalignment for a 1 dB penalty [13]. Grating-couplers can also be placed at any point on the PIC surface, not just at the edge of the chip, do not require any post-processing steps, such as precision dicing and polishing of the PIC, thereby facilitating wafer-scale testing and characterization of PIC before dicing and packaging. However, until recently, these practical advantages have been somewhat offset by minimum insertion-losses that are higher than those that can be achieved demonstrated by edge-couplers. Fortunately, recent advances in grating-coupler design have started to close this performance gap, with reports of 1.6 dB and 1.2 dB (measured) insertion-losses from uniform and apodized grating-couplers in the silicon-on-insulator platform [28,29]. More advanced, though less commercially-scalable grating-coupler designs, where a metallic back-reflector layer is added in a post-processing step, allows for insertion-losses of 0.6 dB [30], showing that best-in-class grating-couplers offer the same level of performance as the best edge-couplers, while still offering relatively relaxed alignment tolerances.

Standard, or '1D' grating-couplers usually exhibit a strong polarization sensitivity, which can make them unsuitable telecom and datacom connections, due to the unknown and unstable polarization state from telecom fibers. One solution is 2D grating-coupler, which is formed by the superposition of two orthogonally orientated 1D grating-couplers, and can accept a fiber-mode of any polarization-state, diffracting it into a pair of on-PIC waveguides that are both TE-polarized [31]. Recent work on 2D

grating-coupler optimization for Si-photonics has predicted insertion losses of 1.0 dB and 2.0 dB for designs with and without back-reflectors and polarization dependent losses as low as 0.3 dB [32,33].

For many telecom and datacom applications, it is useful to have multiple channels packaged to the same PIC, with current projects targeting even 128 and 256 channels. Instead of aligning individual channels, it is possible to use an 'optical shunt' to simultaneously align each fiber with a matching grating-coupler [34]. In this approach, a precision fiber-array is constructed, consisting of a glass-plate in which a series of parallel v-groves are precision-etched, typically with a pitch of 127 μm or 250 μm, to match the diameter of standard telecom fibers, and a flat glass 'lid'—see Figure 6. Once the fibers are inserted into the v-groove channels, and the lid is applied, the three-point-contact condition ensures the precise position and spacing of the different channels. The nominal centricity of the inner-cores of the fibers in these fiber-arrays is ±0.5 μm, which is well within the ±2.5 μm 1 dB alignment tolerance of the grating-couplers. Therefore, when the first and last grating-couplers are connected by a shunt waveguide, a single active alignment of the fiber-array that maximizes the shunt transmission also aligns all intermediate fiber-channels with respect to their grating-couplers (with a ±0.5 μm tolerance). Once the single- or multiple-channel Fiber-to-PIC alignment has been made, it is locked into place using a low-shrinkage index-matched ultraviolet (UV)-cured epoxy.

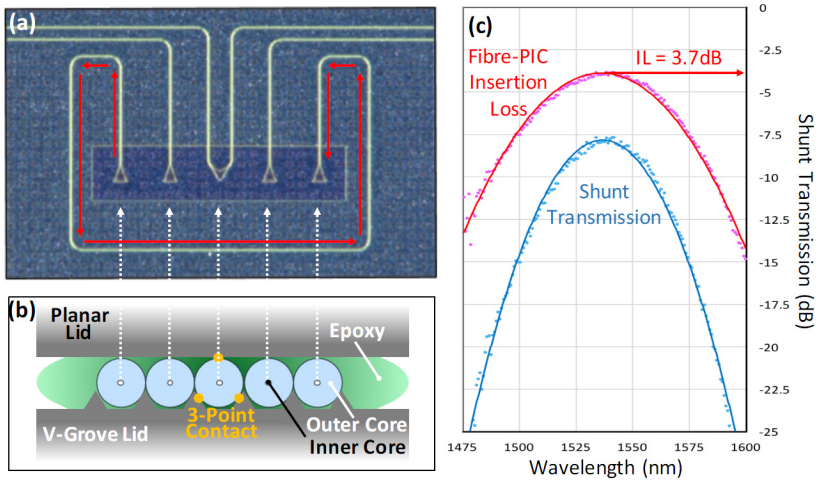


Figure 6. Optical shunt to support the active-alignment of a multi-channel fiber-array to a Si-PIC; (**a**) Microscope image of an optical-shunt and three intermediate couplers—2 × 1D grating-couplers, and 1 × 2D grating-coupler); (**b**) Schematic of a multi-channel fiber-array showing how three-point contact allows for precise alignment of the fibers in the v-grooves; (**c**) The transmission spectrum of the optical-shunt, showing the bandwidth of the grating-couplers. As the shunt is symmetric and has negligible waveguide-losses, the insertion-loss (IL) in units of dB is simply half of the optical-shunt transmission in units of dB.

Although shunt alignment helps reduce the per-channel cost of Fiber-to-PIC packaging, it still involves a single active-alignment step, while a credible route to scalable packaging calls for a passive Fiber-to-PIC alignment scheme. The recent demonstration of 'flip-chip' Fiber-to-PIC alignment is one promising approach [35]. Here, a beam-splitter system is used to visually align the inner-cores in a fiber-array to the matching grating-couplers on a PIC, with a tolerance of ±1 μm, without active alignment. Since this is within the 1 dB alignment tolerance of the grating-couplers, this approach still offers low insertion-loss, but is at least one order of magnitude faster than active alignment. Alternative schemes for passive alignment involving large-footprint (30 μm × 30 μm) grating-couplers that offer relaxed 1 dB alignment tolerances of ±10 μm are also under investigation. Here, the principle drawback is a reduction in the spectral bandwidth, which can exclude this approach for wavelength division multiplexing applications.

2.1.3. Evanescent-Coupling

A new approach to Fiber-to-PIC coupling, termed 'evanescent coupling' was first applied to Si-Photonics by IBM-Zurich in 2015 [36]. In this scheme, as in edge-coupling, an inverted-taper is used to efficiently extract the mode from the PIC waveguide. However, instead of being captured by an on-PIC SSC, the mode evanescently couples into a second waveguide on a different optical-chip, that is in very close face-to-face proximity with the PIC—see Figure 7. The refractive index and MFD on the optical-chip can then be easily matched to that of standard SMF fibers, allowing for a two-step (Fiber-Chip-PIC) coupling process. Currently, chip-to-chip evanescent coupling has only been demonstrated between a Si-PIC and a polymer-based optical-chip, but there is no clear reason why this approach cannot be transferred to glass- or SiON-based optical-chips for more robust photonic devices.

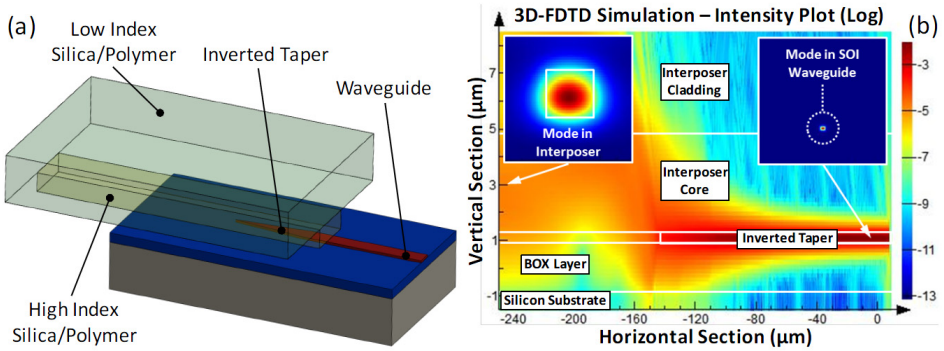


Figure 7. Evanescent coupling from an optical-chip to a Si-PIC; (**a**) Schematic of the evanescent coupling scheme, showing the inverted-taper on the Si-PIC and the wave-guiding region of the optical-chip (high-index polymer core surrounded by a low-index polymer cladding); (**b**) Mode propagation and 3D-FDTD (finite difference time domain) simulations illustrate the transfer of light between the optical-chip and Si-PIC.

Evanescent coupling is attractive, because it offers all the characteristic advantages of edge-coupling, such as low insertion-loss, broadband coupling, and low sensitivity to polarization, as well as the relaxed alignment tolerances typical of grating-coupling [36]. Additionally, unlike edge-coupling, the inverted-taper of the evanescent coupler does not need to be located at the edge of the PIC, and does not depend on precision dicing and polishing of the PIC edges, further reducing its cost to implement at volume.

2.2. Laser-to-PIC Integration

For many sensing applications in photonics, it is desirable to locally generate either a continuous wave or modulated light signal on the Si-PIC. Since there is no monolithically integrable laser-diode available for CMOS, this necessitates either (i) the heterogeneous integration of III–V material on the Si-PIC; or (ii) the hybrid integration of a III–V device on the Si-PIC.

Heterogeneous integration refers to the bonding of III-V material with optical gain onto the Si-PIC (either directly or with an intermediate polymer adhesive layer), followed by the etching of material to create a cavity condition for lasing. The cavity can be formed between two etched facets, two Bragg reflectors, or with a micro-ring, depending on the application [37,38]. The resulting laser emission is then evanescently coupled into the on-PIC waveguide. Heterogeneous integration can be regarded as a post-processing step, rather than photonic packaging, and is often used to create semiconductor amplifiers (SOAs), which provide optical gain to offset the insertion-loses and waveguide losses on the Si-PIC [39]—see Figure 8. The optical gain from these integrated SOAs has a strong (Arrhenius) thermal dependence, and so requires temperature stabilization for stable performance.

Hybrid integration involves the coupling of light from a discrete III-V laser device onto the Si-PIC, either directly or by using a μOpto-Electro-Mechanical (μOEM) stage. Hybrid integration schemes tend to have lower integration densities than heterogeneous integration schemes, but have the advantage of deploying only 'known good devices', which leads to higher yields and tighter performance profiles. Two promising hybrid laser integration schemes are the micro-optical bench, and direct vertical cavity surface emitting laser (VCSEL) integration.

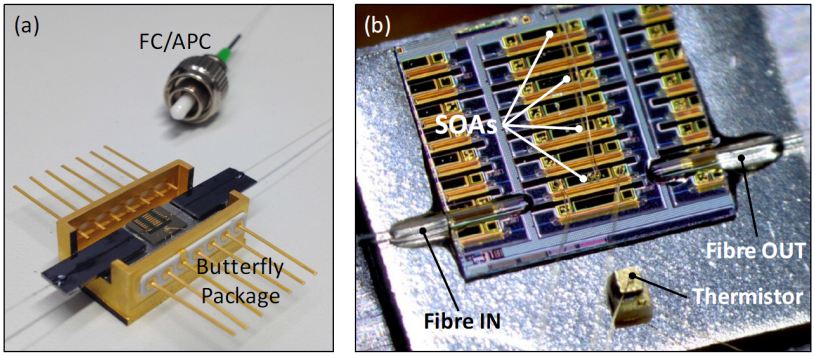


Figure 8. III–V semiconductor optical amplifiers (SOAs) integrated on a Si-PIC; (**a**) Image of a packaged SOA module, with Fiber-to-PIC grating-coupling of the input and output channels in the QPC configuration, to evaluate the optical gain of the SOA; (**b**) Microscope image of the packaged SOA showing the QPC Fiber-to-PIC coupling, and the thermistor used to provide feedback for the integrated thermo-electric cooler (TEC) mounted under the PIC.

Table 1. Typical insertion loss, bandwidth, polarization sensitivity, alignment tolerances, and MPW (multi-project wafer) availability for different Fiber-to-PIC (photonic integrated circuits) couplers.

Coupler Type	Insertion Loss	1 dB Bandwidth	Polarization Sensitivity	1 dB Alignment Tolerance	MPW Availability
1D-GC [1]	1.6 dB [28]	40 nm [13]	TE [1]/TM [1]	±2.5 μm (in-plane) [13] & 10 μm (out-of-plane) [26]	CEA-Leti &Imec
2D-GC [1]	3.2 dB [32]	35 nm [32]	TE & TM	±2.5 μm (in-plane) [32]	CEA-Leti & Imec
Edge Coupler	1.2 dB [17]	200 nm TE & 150 nm TM [17]	TE & TM	±0.5 μm (in-plane) [17]	Imec (taper only)
Evanescent Coupler	1.0 dB [36]	>>40 nm [36]	TE & TM	±2.5 μm (in-plane) [36]	Imec (taper only)

[1] 1D-GC = one-dimensional grating-coupler, 2D-GC = two-dimensional grating-coupler, TE = transverse-electric, and TM = transverse-magnetic.

2.2.1. Micro-Optical Bench

Both Luxtera and the Tyndall National Institute have demonstrated micro-optical bench (MOB) [40,41]. These MOBs consist of an AlN (or Si) sub-mount on which an edge-emitting laser-chip, a ball μLens for collimating and focusing, and a mirror (or a total internal reflection element) for beam-steering, are mounted—see Figure 9. The hermetically-sealed Luxtera MOB also includes a micro-optical isolator to reduce feedback to the laser-chip. The MOB functions by re-imaging light from the edge-emitting laser onto the grating-coupler on the surface of the PIC with the required near-normal angle-of-incidence. Standard 1D grating-couplers on the PIC can be used, but custom grating-couplers designed to better match the elliptical spot from the MOB offer even lower insertion-losses.

In the Tyndall MOB, the 300 μm ball μLens self-aligns in a precision laser-drilled hole, and which then provides a fixed reference-point for the alignment and mounting of the μPrism reflection element. The overall footprint of the MOB is approximately 1 × 1 mm, with the individual components of laser-chip, μLens, and μPrism having a maximum dimension of 300 μm. Once assembled, the

MOB is actively aligned with respect to the grating-coupler on the Si-PIC, and has a 1 dB alignment tolerance comparable to that of Fiber-to-PIC coupling (±2.5 µm). Without adequate thermal-sinking, the laser-chip on the MOB is likely to overheat, leading to reduced performance or burning-out. Good thermal contact between the MOB and the PIC, as well as thermo-electric cooler (TEC), are needed for stable operation of the MOB [42].

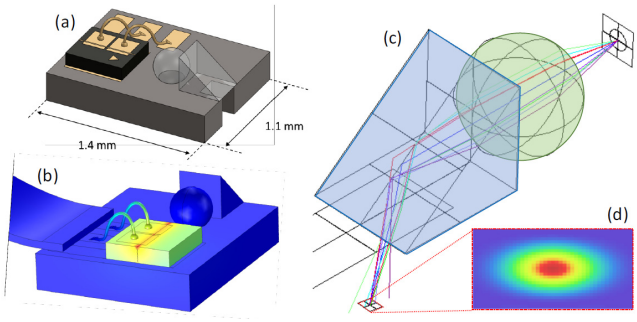


Figure 9. Tyndall micro-optical bench (MOB); (**a**) Schematic of the MOB showing the laser-chip, ball lens, and micro-prism; (**b**) *COMSOL*-software thermal model of the MOB showing the elevated temperature of the laser-chip during CW operation; (**c**,**d**) *Zemax* ray-tracing applied to the MOB shows how emission from the laser-chip is re-imaged onto the grating-coupler on the surface of the PIC. Unlike a fiber-mode, the re-imaged spot is elliptical, just like the mode form the laser-chip.

2.2.2. VCSEL Integration

Direct integration of vertical cavity surface emitting lasers (VCSELs) is also a promising avenue for hybrid integration. Here, the significantly reduced footprint of a VCSEL chip (250 × 250 µm) over the MOB (1 × 1 mm) allows for very high integration densities. Planar VCSEL-to-PIC integration has been demonstrated, where photoresist based 'wedges' are used to refract the VCSEL mode onto the grating-coupler with the required near-normal angle-of-incidence [43]. Alternatively, a grating-coupler can be designed to couple the VCSEL-mode into a pair of opposing waveguides, which can then be recombined into a single-channel, after phase-compensation [44]. A tilted-VCSEL approach can also be used, where the VCSEL is directly flip-chipped onto the PIC with an asymmetric distribution of solder balls [45]—see Figure 10. By controlling the contact area of the bond-pads available for solder wetting, the tilt-angle of the VCSEL can be optimized. This tilted-VCSEL approach allows for passive flip-chip alignment to the PIC for rapid assembly at commercial volumes.

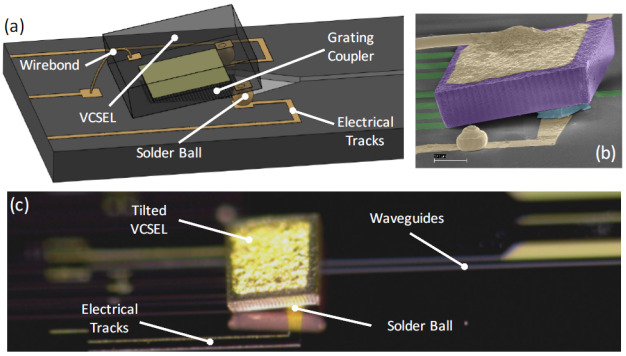


Figure 10. Tilted vertical cavity surface emitting laser (VCSEL) to Si-PIC integration; (**a**) Schematic of the tilted-VCSEL geometry, showing the VCSEL positioned above the grating-coupler on the Si-PIC, and the tilt being provided by the solder balls; (**b**) SEM (scanning electron micrsoscope) image of a tilted VCSEL on the Si-PIC; (**c**) Microscope image of a tilted-VCSEL on the Si-PIC, showing the electrical-tracks and on-PIC waveguides used for routing the electrical and optical signals.

3. Electronic Packaging

For telecom and datacom applications, photonic devices are required to operate at high speeds and with very high bandwidths. In many cases, this involves the (de-)multiplexing of several 25 Gbps electrical-channels to/from a single $N \times 25$ Gbps optical-channel, with $N = 4, 6, 12$, etc. The efficient, low-reflection, artifact-free, routing of these high-speed electrical signals from a centimeter-scale SMA (SubMiniature, version A) /SMK (SubMiniature, version K) connector to the microscopic structures on the PIC can present a design challenge. If a very high number of electrical connections to the PIC are needed, or if precise (sub-ns) control of switching is needed on multiple channels, then vertical integration of a custom electronic integrated circuit (EIC) driver-chip may also be needed.

3.1. High-Speed Routing

High-speed SMA (18–25 GHz) and SMK (46 GHz) connectors have $a \approx 1$ cm^2 footprint on the PCB, while the pitch of the electrical bond-pads on a PIC is typically 100 μm. Therefore, the pitch of the high-speed 50 Ω transmission lines must be reduced by two orders-of-magnitude between the connector and the PIC, while maintaining the path-length of different electrical-channels to preserve signal timings. This usually results in PICs surrounded by circular or semi-circular PCBs, with an area that increases proportional to the square of the number of electrical channels—see Figure 11.

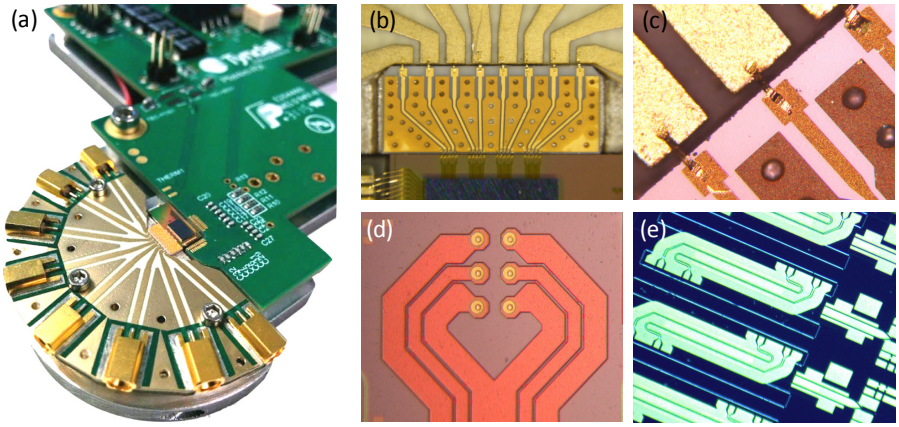


Figure 11. Examples of electrical-routing structures needed for high-speed photonic packages; (**a**) Image of the semi-circular PCB-to-PIC routing needed to ensure that multiple signals arrive at the same time; (**b**) Microscope image of a pitch-reducing ceramic interposer used to match the minimum-pitch on a standard high-dielectric PCB (300 μm) to the bond-pad pitch on the PIC (100 μm); (**c**) Microscope image of the 'tape' or 'ribbon' wire-bonds used to connect the PCB to the ceramic interposer; (**d**,**e**) On-PIC high-speed transmission lines in the co-planar ground-signal-ground geometry.

On standard high-dielectric PCB ($D_K \approx 10$), the minimum feature size limits the pitch of 50 Ω transmission lines to about 300 μm, which is a factor of three greater than the bond-pad pitch on the PIC. This 'gap' can be bridged by a pitch-reducing multi-level ceramic interposer, designed using a finite element mode (FEM) high frequency structural simulator (HFSS). The interposer offers smaller feature sizes and higher manufacturing tolerances than those possible for PCBs. The electrical connection between the interposer and the bond-pads on the PIC are made using 10–20 μm diameter Au wire-bonds. For DC (direct current) connections, circular cross-section wire-bonds are used, but for high-speed connections 'ribbon' or 'tape' wire-bonds are preferred. Ribbon wire-bonds have a higher surface area-per-unit-volume, which offers lower resistance to high-speed signals, because of the skin effect.

To reduce induction effects, all wire-bonds should be as short and straight as possible. This often means that the PIC should be recessed into the PCB, to allow for a 'flush' wire-bond. Once connected

to the PIC, wire-bonds are very sensitive to any shearing force, and so the PIC, interposer, and PCB must be rigidly connected in the the mechanical package. 'Glob top' encapsulation of the wire-bonds with silicone or epoxy can offer further protection, but can only be used in packages where it will not interfere with Fiber-to-PIC coupling, or other integrated components.

Once transferred to the PIC, the high-speed signals must be routed from the bond-pads to/from the relevant on-PIC components. Although different cross-section geometries are possible on the PCB and interposer (micro-strip, strip-line, and co-planar transmission-lines), Si foundry design rules typically restrict the high-speed transmission lines to a co-planar geometry. To avoid significant losses and reflections, HFSS must be used to optimize these on-PIC transmission lines within the boundary conditions of the very specific materials and layer-thicknesses available at the Si foundry [6–8].

3.2. Vertical Integration

Monolithic integration of photonic and electronic functionalities onto a single chip is often promoted as the ultimate goal for large-scale Si photonics [4]. However, at low-to-medium volumes (10^4–10^5 chips per year), the vertical integration of the electronic and photonic functionalities onto two separate Si chips can bring an economic-advantage, because it allows for the mixing of different CMOS technology nodes. Specifically, the fabrication tolerances of PICs can be satisfied by the 45 nm node on relatively low-cost 200 mm wafers, while high-performance cost-effective electronic-ICs (EIC) may need the 14 nm node on 300 mm wafers. The footprint of a PIC (10–30 mm^2) is usually quite large compared to a typical EIC, because of large photonic components (AWGs, delay-lines, etc.) and the space reserved for Fiber-to-PIC coupling, so not 'wasting' this space on the more expensive CMOS node can bring a significant reduction in overall cost.

The vertical integration of an EIC on a PIC can be made using either solder-ball-bump (SBBs) or copper-pillar-bump (CPBs) interconnects, which provide an electrical, mechanical, and thermal interface between the two chips [46,47]. In particular, vertical integration improves the high-speed electronic interface to the PIC, because it acts to replace long (100–500 μm) possibly curved, wire-bonds with short (≈10 μm) SBB or CPB interconnects, which minimizes parasitic induction effects [48–50]—see Figure 12. In addition to high-speed, high-density electronic integration, the mechanical connection offered by SBBs and CPBs also allows for the bridging of different functional technologies, such as MEMS (micro-electro-mechanical systems), III-V, non-CMOS ASIC (application-specific integrated circuit), etc. [3].

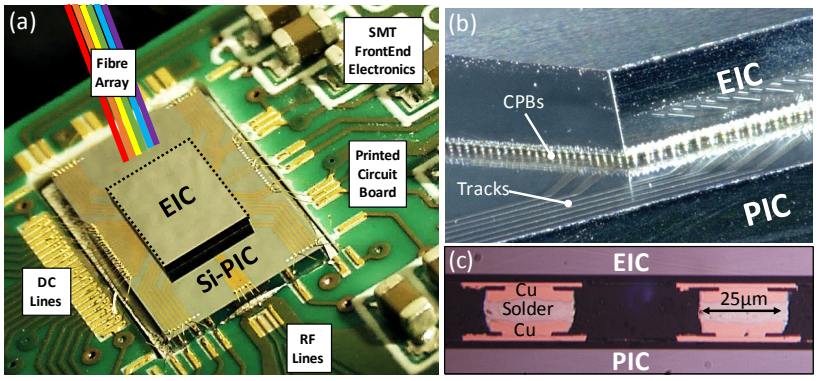


Figure 12. Vertical integration of an electronic integrated circuit (EIC) driver-chip on top of a Si-PIC; (**a**) Image of an EIC integrated on a PIC, with RF (radio frequency) and DC (direct current) signals routed from the front-end electronics on the PCB across the surface of the PIC; (**b**) Microscope image of the EIC integrated onto the PIC using several hundred discrete copper-pillar-bumps (CPBs); (**c**) Further zoomed-in microscope image of the CPB interconnects between the EIC and PIC. Solder reflow bonding with a "no clean" flux allows for very well aligned CPB interconnects with minimal "solder squeezing".

CPBs typically have a diameter of 20–30 μm, and are formed by Cu electro-plating of under-bump metal-pads on the PIC and EIC, followed by the deposition of a (lead-free) Sn-Ag-Cu solder-cap. The PIC and EIC are vertically integrated by aligning the matching pairs of CPBs on both chips using the beam-splitter camera of a flip-chip system; bringing the two chips into contact; and then applying a thermo-compression or solder-reflow cycle to fuse together the paired solder-caps. These solder-caps will be coated by a native-oxide layer that must be removed to ensure a good electrical and mechanical interconnect is formed [51]. The traditional solder-fluxes used in electronic packaging are generally not applicable in photonic packaging, because they can leave chemical residue that contaminates the optical interfaces for Fiber-to-PIC coupling. This can lead to increased insertion losses and also a weakening of the mechanical Fiber-to-PIC bond. Instead, a 'no clean' flux should be used during the solder-reflow bonding. This flux is VOC-free (volatile organic compounds) and activates and evaporates at the melting-point of the solder [52], so it does not require a post-bonding solvent-rinse that can contaminate the PIC [53,54].

After the alignment of the EIC and PIC in a flip-chip system, and applying a 'no clean' flux solder-reflow cycle (typically 250 °C for 30 s), it is possible to achieve an excellent bond between the top- and bottom-side CPBs. A variety of diagnostics—electrical resistance measurements, destructive tear-off tests, and X-ray microscopy—can be used to assess the quality of the CPB interconnect. An alignment of better than ±1 μm can be achieved, with little-to-no 'solder squeezing', which would have the potential to lead to electrical shorts between adjacent interconnects—see Figure 13.

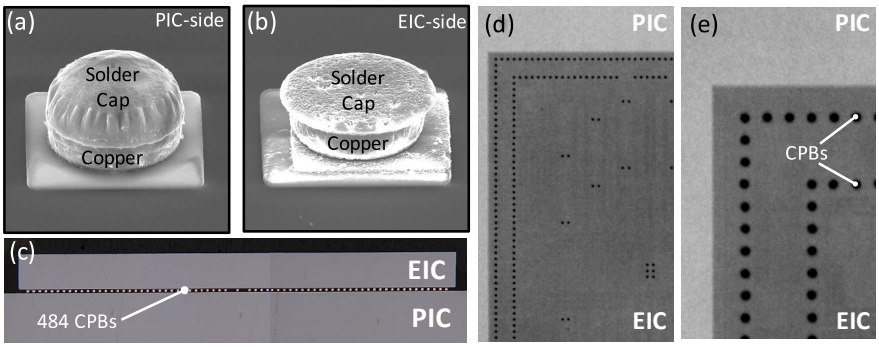


Figure 13. Analysis of the copper-pillar-bumps (CPBs) for vertical integration; (**a**,**b**) SEM images of the 'top' and 'bottom' CPBs that form the vertical interconnect between the PIC and EIC before solder-reflow bonding. The asymmetric pairing of the CPBs helps to reduce slippage during the flip-chip alignment; (**c**) Side-view image of the PIC + EIC assembly after a 'grind and polish' has been used to expose approximately 70 CPBs; (**d**,**e**) X-ray microscope images of the PIC+EIC assembly, allowing the operator to 'see through' the EIC, and identify the position of the CPBs. This diagnostic allows the operator to non-destructively identify missing or grossly malformed CPBs.

4. Thermal Management of PICs

Photonic elements, such as integrated semiconductor optical amplifiers (SOAs) and micro-ring resonators, exhibit a strong temperature-dependence that is many times greater than that of CMOS electronics. A temperature variation of 20 °C is often sufficient for a PIC to drift out of its operational profile [55,56]. Global thermal stabilization of the PIC in a photonic device, usually with a thermo-electric cooler (TEC), is essential for prototypes that need to be tested in the field, where seasonal temperature swings of ±10 °C are common. The added global stability from the TEC allows for more efficient and better reproducibility in the local temperature-tuning of individual photonic elements (e.g., micro-ring resonators, thermo-optic phase-shifters, etc.) on the PIC. Increasing the coefficient of performance (CoP) of the TEC in these modules is an important consideration for lowering the operational cost of deployed photonics.

Figure 14 shows a schematic of the typical 'thermal stack' for a module with a PIC and integrated EIC. The electrical power is delivered to the EIC, where it evolves into thermal power ($H = dQ/dt$) via Joule-heating, and then flows into the PIC through the SBB or CPB interconnect layer. From there, the heat conducts into a heat-spreading plate, and reaches the 'cold side' of the TEC, before reaching the baseplate of the module, where it is lost to the ambient environment, either through passive convection/conduction, or 'rack-based' forced-convection cooling.

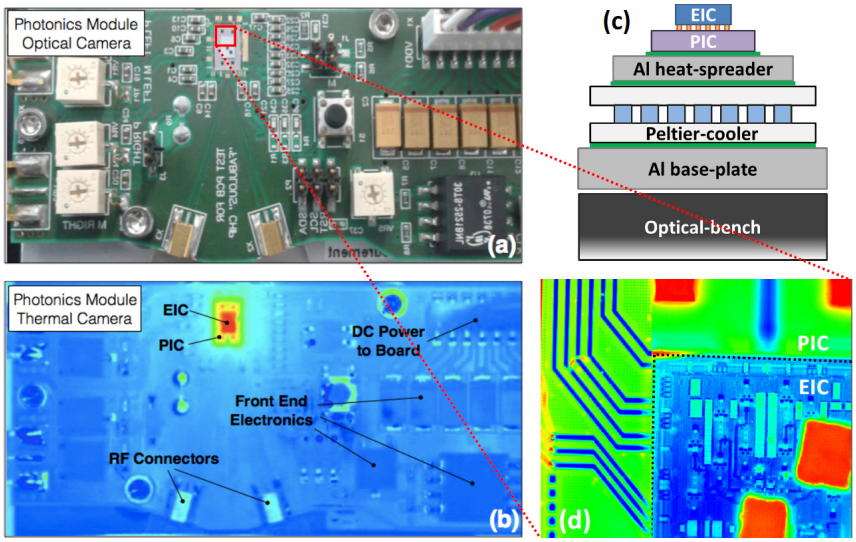


Figure 14. Thermal imaging of a photonic module and PIC; (**a**,**b**) A comparison of optical and thermal imaging of the optical network unit (ONU) packaged for the FP7-FABULOU project. Once powered-up, both the EIC and PIC experience a significant increase in temperature (34 °C and 20 °C, respectively); (**c**) Schematic of the 'thermal stack' in the ONU, showing the conduction path from the EIC to to the baseplate; (**d**) Thermal microscopy of the EIC and PIC on the ONU. Silicon is transparent in the 3–5 μm wavelength range at which the sensor operates, allowing the user to 'see through' the EIC substrates and image the metallic structures on the surface of the EIC and PIC.

The effect of unchecked Joule-heating can be illustrated by powering-up the EIC while the TEC is powered-down, as shown in Figure 15. Here, 1.1 W of power is applied to the EIC in a Si photonic optical network unit (ONU), developed for the the EU-FP7 'FABULOUS' project [57], which results in a temperature increase of 34 °C and 20 °C for EIC and PIC, respectively. These measurements were made using a thermal microscope, which allows for accurate, non-contact temperature measurements, both of the PIC (100 μm-scale) and the full photonic module (10 cm-scale). These dynamic temperature measurements provide quantitative information on both the heat-conduction and heat-capacity of the thermal stack. Broadly speaking, the 'kinks' in these dynamic measurements correspond to the time taken for the heat to 'fill' the different blocks of material in the stack, though proper modelling and data-fitting is needed to fully extract the quantitative details. In contrast, the steady-state temperature difference between the EIC and PIC (ΔT = 13.8 °C) provides a very direct measure of the thermal resistance (R_T) of the CPB interconnect layer through, $R_T = \Delta T/H$. The thermal resistance of the full CPB layer is then 12.5 K/W = 13.2 °C/1.1 W. Given that the interconnect layer consists of 484 individual CPBs, this implies a resistance of 6.1 $\times$ 10^3 K/W per interconnect. The dynamic and steady-state information from the thermal microscopy measurements can be used to validate current thermal models, and also to show how future designs can be optimized.

Once the TEC is powered-up, the PIC rapidly stabilizes to the set-point temperature (T_{SP}) programmed into the external proportional-integral-differential (PID) controller. A micro-bead or surface-mountable technology (SMT) thermistor is placed in close thermal proximity to the PIC, to provide feedback to the PID controller. For the ONU from the 'FABULOUS' project, the PIC stabilizes

to $T_{SP} \pm 0.1$ °C in 30 s, and $T_{SP} \pm 0.01$ °C in 60 s. In this steady-state, where 1.1 W of electrical power is applied to the EIC, the TEC needs to draw 0.5 W to recover the PIC to a room-temperature set-point of 18 °C. This implies a CoP of 2.2 = 1.1 W/0.5 W, and shows that thermal management accounts for 30% = 0.5 W/0.5 W + 1.1 W of the operational power-budget for the module. Increasing the CoP of TE-cooling for PICs, by improving how heat can be distributed and dissipated across the module, is an active topic of research. Finite-element simulations in *COMSOL* can be used to test and optimize new stack designs, which are then experimentally validated using the dynamic temperature measurements from thermal microscopy—see Figure 16.

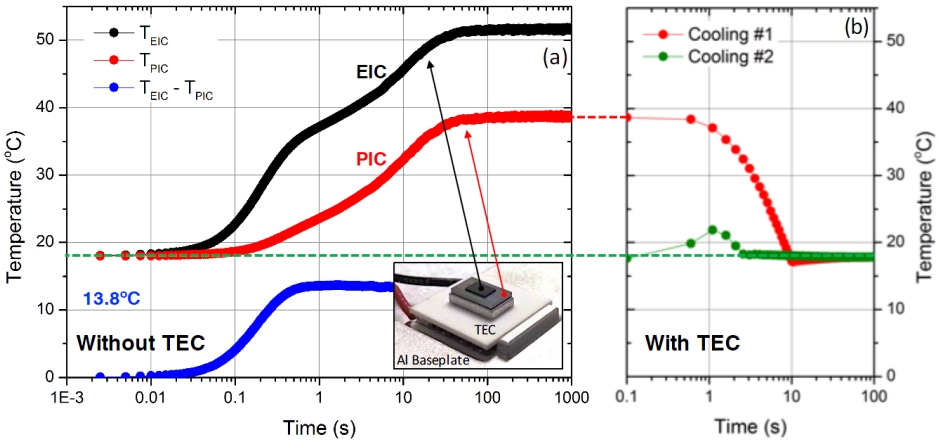


Figure 15. Temperature changes of the EIC and PIC in the FP7-FABULOUS optical network unit (ONU) from the thermal microscope analysis; (**a**) The increase in EIC and PIC temperature, when the ONU is powered-up, and the TEC (thermo-electric cooler) is not activated. After 30 s, the PIC temperature reaches a steady-state at 20 °C above the ambient; (**b**) Once the TEC is activated (in Cooling#1), the hot PIC rapidly returns to the ambient set-point temperature, reaching ±0.1 °C of the set-point in 30 s. In Cooling#2, the ONU and TEC are powered-up at the same moment, and the PIC never exceeds the set-point by more than 5 °C.

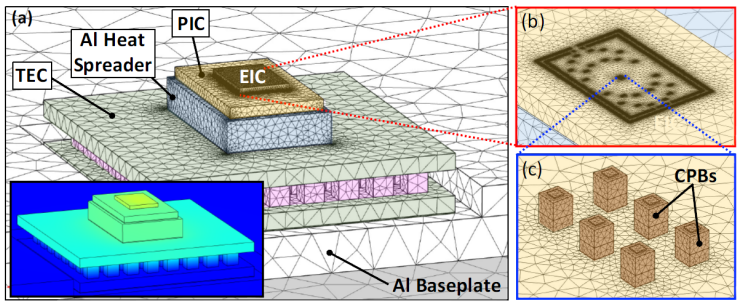


Figure 16. *COMSOL* thermal simulations of the EIC and PIC in the FP7-FABULOUS ONU; (**a**–**c**) For accurate convergent models, the simulation mesh must span from the 10 cm-scale of the full module (including TEC and baseplate) to the 10 µm-scale of the CPB interconnects. The results of these simulations can be validated against thermal-imaging, and used to test new designs for better cooling of the EIC and PIC in the photonic module.

5. Emerging Technologies for Photonics Packaging

In addition to the established technologies described in the previous sections, it is interesting to look at emerging technologies and how they may impact photonic packaging in the future. For example, the same polymer waveguide technology that has been used to demonstrate evanescent coupling can also be combined with electrical FR4 (fire-resistant, version 4) PCBs to create a platform capable

of routing electrical and optical signals from external connectors to single or multiple Si-PICs [36]. Here, the main advantages over glass interposers is improved cost-effectiveness and processing flexibility of the polymer waveguides (i.e., direct laser-writing or photolithography), especially for large areas. The anticipated propagation distances in these 'optical PCBs' is in the range of 10s of cm, so the principle challenge to be overcome is reducing waveguide propagation losses to below 0.1 dB/cm. Another highly innovative solution for PIC-to-PIC [58] and multi-core Fiber-to-PIC [59] optical connectivity is that offered by the photonic wire bonds (PWBs) developed at the Karlsruhe Institute of Technology. These PWBs are formed by tightly focused femtosecond laser pulses that expose photoresist along a freeform 3D path connecting two optical interfaces (e.g., inverted-tapers on a Si-PIC to the inner-core of a single-mode fiber). Since the shape of the PWBs can be easily adapted, there is no need for high-precision mechanical alignment between connected PICs and fibers, which is an advantage for future scale-up. Writing PWBs is currently a serial process, and it remains to be seen if it can be economically implemented at the wafer-level, where thousands or tens-of-thousands of PWBs are needed per wafer.

There are also many innovations around the basic grating-coupler designs, including replacing single-line trenches with sub-wavelength lithographic features that allow for a high degree of index engineering. In some cases, these sub-wavelength features are designed to create an apodized structure that almost perfectly matches the profile of the incident fiber-mode [60], and so allows for very low (sub-decibel) insertion losses. An alternative strategy is to use the sub-wavelength lithographic features to create a region with highly non-linear patterning that creates a patch of meta-material in the SOI (silicon-on-insulator)-layer [61]. When the pattern in this meta-material is properly optimized it can couple light from free-space into the SOI-waveguide, and can even couple light of different polarizations, in analogy to 2D grating-couplers. The efficiency of these meta-material couplers each device is at least comparable to more standard grating-couplers, and can offer a broader bandwidth, because multiple guided modes are responsible for the coupling, which makes the meta-material coupler less sensitive to wavelength shifts. The principle disadvantages of both of these sub-wavelength coupler schemes is that they can normally only be fabricated by e-beam lithography, because they require feature-sizes on the order of 100 nm, which are not readily accessible using the 193 nm deep-UV lithography typically used in the Si-Photonic foundries. Until the performance of these sub-wavelength couplers can be transferred to a scalable UV lithographic process, they cannot be developed into standardized building blocks for commercial photonic devices.

In addition to Fiber-to-PIC coupling, grating-couplers can be used for optical proximity coupling or interlayer coupling [62–64], which allows for efficient vertical chip-to-chip and even board-to-chip connections (in conjunction with optical-PCBs mentioned above). Combined with low-loss waveguides for horizontal distribution, this vertical chip-to-chip optical connection allows for the possibility of true 3D integrated routing of light across optical-motherboards to multiple Si-PICs. Even though the bandwidth of Fiber-to-PIC grating-couplers is typically rather narrow (normally, the 1 dB bandwidth is 30–40 nm), the same gratings in an optical proximity configuration will offer broadband coupling, because a near-field interaction between the gratings mediates the coupling. For the same reason, the insertion-loss between two adjacent grating-couplers is not simply the sum of two equivalent Fiber-to-PIC interfaces; it can be much lower, on the order of a single Fiber-to-PIC interface. These optical proximity couplers are expected to have a large impact on wafer-level packaging, because they allow for the flip-chip alignment and/or wafer-bonding of different photonic systems for advanced hybrid photonic devices.

6. Discussion of Trends in Photonics Packaging

The high-cost and low-speed of photonic packaging is probably the most significant bottleneck in developing competitive photonic devices. As spin-out companies work to take devices to market, and large multi-nationals enter the Si-photonics space, there is a growing need to develop automated packaging processes to enable higher volume production. The clear trend is for more compact photonic

designs with lower insertion-loss, higher levels of integration (electrical and MEMs), scalability to many multiples of 25 Gbps channels, and efficient (ideally passive) thermal stabilization. To meet this challenge, researchers in photonic packaging are transitioning from a legacy of individually customized prototypes towards developing standardized and scalable solutions. While these technology innovations of passive Fiber-to-PIC alignment, more precise flip-chip vertical integration, and better thermal-stack design all play an important role, 'soft' developments, such as the publication and adoption of packaging standards, as well as the growth and consolidation of the material and component supply-chain, are equally important.

The need to create standardized design rules and standards for photonic packaging is slowly gaining recognition in the Si-photonics community. This shift is driven by the benefit of removing application-specific design-burdens from researchers/engineers, and streamlining the design-to-device process. Photonic packaging groups are now working with industry partners to establish packaging design kits (PDKs) and rules (PDRs) that support non-expert users in developing Si-PICs that are compatible with best-practice photonic packaging. This helps new users avoid problems and avoid costly and time-consuming PIC re-designs. Examples of important PDR parameters that are often overlooked by new users are (i) the pitch of grating-coupler arrays on the Si-PIC (which should match the dimensions of the fiber-channels, i.e., 127 μm or 250 μm); (ii) the minimum pitch of the electrical bond-pads should be >100 μm for DC-connections (to maximize yield of wire-bonding) and >300 μm for RF-connections (to eliminate the need for costly ceramic pitch-reducing interposers); and (iii) the need for an 'exclusion zone' around grating-coupler array, where no electrical connections or phase-sensitive components are placed, in case of epoxy overflow. Although currently at an early stage of development, it is expected that these PDRs will be extended and formalized into standards over time, and rolled in to the design rule checking (DRC) at Si-foundries. Simple photonic packaging PDKs have already been implemented at a software level in the PIC design tools of PhoeniX BV (OptoDesigner) and Luceda (IPKISS) [65,66].

7. Conclusions

Photonic packaging is an essential step in realizing highly integrated Si photonic devices for both small-scale prototyping and commercial mass-production. The packaging of a photonic device is often the most expensive element of the overall module fabrication, and can involve major technical challenges that need to be addressed at the PIC design stage. Simultaneously satisfying the optical, electrical, and thermal design considerations for a PIC requires a 'joined up' approach that goes well beyond the most widely recognized issue of Fiber-to-PIC coupling. Researchers in packaging are increasingly working with advanced design tools, and evolving packaging equipment, to meet these challenges. As photonic devices and technologies transition out of the laboratory and into the market, photonic packaging is also maturing to keep pace—its focus is shifting from testing and prototyping towards standardized and scalable commercial implementation.

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Conflicts of Interest: The authors declare no conflict of interest.

References

1. Streshinsky, M.; Ding, R.; Liu, Y.; Novack, A.; Galland, C.; Lim, A.; Guo-Qiang, P.L.; Baehr-Jones, T.; Hochberg, M. The road to affordable, large-scale silicon photonics. *Opt. Photon. News* **2013**, *24*, 32–39. [CrossRef]
2. Soref, R. The past, present, and future of silicon photonics. *IEEE J. Sel. Top. Quantum Electron.* **2006**, *12*, 1678–1687. [CrossRef]
3. Arakawa, Y.; Nakamura, T.; Urino, Y.; Fujita, T. Silicon photonics for next generation system integration platform. *IEEE Commun. Mag.* **2013**, *51*, 72–77. [CrossRef]
4. Tsybeskov, L.; Lockwood, D.J.; Ichikawa, M. Silicon photonics: CMOS going optical [Scanning the Issue]. *Proc. IEEE* **2009**, *97*, 1161–1165. [CrossRef]
5. Sun, C.; Wade, M.T.; Lee, Y.; Orcutt, J.S.; Alloatti, L.; Georgas, M.S.; Waterman, A.S.; Shainline, J.M.; Avizienis, R.R.; Lin, S.; et al. Single-chip microprocessor that communicates directly using light. *Nature* **2015**, *528*, 534–538. [CrossRef] [PubMed]
6. Integrated Silicon Photonics ICs with MPW Service. Available online: http://www2.imec.be/be_en/services-and-solutions/silicon-photonics.html (accessed on 15 October 2016).
7. CEA-LETI Full Platform in MPW. Available online: http://www-leti.cea.fr/en/How-to-collaborate/Focus-on-Technologies/Integrated-silicon-photonics (accessed on 15 October 2016).
8. Silicon Photonics Multiple-Projects Wafer. Available online: http://www.a-star.edu.sg/ime/SERVICES/silicon_photonics_multi-projects-wafer.aspx (accessed on 1 December 2016).
9. Zimmermann, L.; Preve, G.B.; Tekin, T.; Rosin, T.; Landles, K. Packaging and assembly for integrated photonics—Review of the ePIXpack photonics packaging platform. *IEEE J. Sel. Top. Quantum Electron.* **2011**, *17*, 645–651. [CrossRef]
10. Kopp, C.; Bernabé, S.; Bakir, B.B.; Fedeli, J.-M.; Orobtchouk, R.; Schrank, F.; Porte, H.; Zimmermann, L.; Tekin, T. Silicon photonic circuits: On-CMOS integration, fiber optical coupling, and packaging. *IEEE J. Sel. Top. Quantum Electron.* **2011**, *17*, 498–509. [CrossRef]
11. O'Brien, P.; Carroll, L.; Eason, C.; Lee, J.-S. Packaging of Silicon Photonic Devices. In *Silicon Photonics III*; Pavesi, L., Lockwood, D.J., Eds.; Springer: Berlin/Heidelberg, Germany, 2016; Volume 122, pp. 217–236.
12. Lee, J.-S.; Carroll, L.; Scarcella, C.; Pavarelli, N.; Menezo, S.; Bernabe, S.; Temporiti, E.; O'Brien, P. Meeting the electrical, optical, and thermal design challenges of photonic-packaging. *IEEE J. Sel. Top. Quantum Electron.* **2016**, *22*. [CrossRef]
13. Taillaert, D.; Van Laere, F.; Ayre, M.; Bogaerts, W.; Van Thourhout, D.; Bienstman, P.; Baets, R. Grating couplers for coupling between optical fibers and nanophotonic wave-guides. *Jpn. J. Appl. Phys.* **2006**, *45*, 6071–6077. [CrossRef]
14. Taillaert, D.; Chong, H.; Borel, P.I.; Frandsen, L.H.; De La Rue, R.M.; Baets, R. A compact two-dimensional grating coupler used as a polarization splitter. *IEEE Photonics Technol. Lett.* **2003**, *15*, 1249–1251. [CrossRef]
15. Fukuda, H.; Yamada, K.; Tsuchizawa, T.; Watanabe, T.; Shinojima, H.; Itabashi, S. Silicon photonic circuit with polarization diversity. *Opt. Express* **2008**, *16*, 4872–4880. [CrossRef] [PubMed]
16. Song, J.; Fernando, H.; Roycroft, B.; Corbett, B.; Peters, F. Practical Design of Lensed Fibers for Semiconductor Laser Packaging Using Laser Welding Technique. *J. Lightwave Technol.* **2009**, *27*, 1533–1539. [CrossRef]
17. McNab, S.; Moll, N.; Vlasov, Y. Ultra-low loss photonic integrated circuit with membrane-type photonic crystal waveguides. *Opt. Express* **2003**, *11*, 2927–2939. [CrossRef] [PubMed]
18. Shoji, T.; Tsuchizawa, T.; Watanabe, T.; Yamada, K.; Morita, H. Low loss mode size converter from 0.3 μm square Si wire waveguides to singlemode fibers. *Electron. Lett.* **2002**, *38*, 1669–1670. [CrossRef]
19. Pu, M.; Liu, L.; Ou, H.; Yvind, K.; Hvam, J.M. Ultra-low-loss inverted taper coupler for silicon-on-insulator ridge waveguide. *Opt. Commun.* **2010**, *283*, 3678–3682. [CrossRef]
20. Galán, J.; Sanchis, P.; Sánchez, G.; Martí, J. Polarization insensitive low-loss coupling technique between SOI waveguides and high mode field diameter single-mode fibers. *Opt. Express* **2007**, *15*, 7058–7065. [CrossRef] [PubMed]
21. Romero-Garcıa, S.; Marzban, B.; Merget, F.; Shen, B.; Witzens, J. Edge couplers with relaxed alignment tolerance for pick-and-place hybrid integration of III–V lasers with SOI waveguides. *IEEE J. Sel. Top. Quantum Electron.* **2014**, *20*. [CrossRef]

22. Papes, M.; Cheben, P.; Ye, W.N.; Schmid, J.H.; Xu, D.X.; Janz, S.; Benedikovic, D.; Ramos, C.A.; Halir, R.; Ortega-Moñux, A.; et al. Fiber-chip edge coupler with large mode size for silicon photonic wire waveguides. In Proceedings of the SPIE (9516), Integrated Optics: Physics and Simulations II (95160K), Prague, Czech Republic, 1 May 2015.
23. Solutions for Si-Photonics Connection. Available online: http://www.teemphotonics.com/ioc/offer-and-products/solutions-for-si-photonics-connection.html (accessed on 15 October 2016).
24. Van Laere, F.; Claes, T.; Schrauwen, J.; Scheerlinck, S.; Bogaerts, W.; Taillaert, D.; O'Faolain, L.; Van Thourhout, D.; Baets, R. Compact focusing grating couplers for silicon-on-insulator integrated circuits. *IEEE Photonics Technol. Lett.* **2007**, *19*, 1919–1921. [CrossRef]
25. Roelkens, G.; Vermeulen, D.; Selvaraja, S.; Halir, R.; Bogaerts, W.; Van Thourhout, D. Grating-based optical fiber interfaces for silicon-on-insulator photonic integrated circuits. *IEEE J. Sel. Top. Quantum Electron.* **2011**, *17*, 571–580. [CrossRef]
26. Snyder, B.; O'Brien, P. Planar fiber packaging method for silicon photonic integrated circuits. In Proceedings of the Optical Fiber Communication Conference, Optical Society of America (OM2E.5), Los Angeles, CA, USA, 4–8 March 2012.
27. Li, C.; Chee, K.; Tao, J.; Zhang, H.; Yu, M.; Lo, G. Silicon photonics packaging with lateral fiber coupling to apodized grating coupler embedded circuit. *Opt. Express* **2014**, *22*, 24235–24240. [CrossRef] [PubMed]
28. Vermeulen, D.; Selvaraja, S.; Verheyen, P.; Lepage, G.; Bogaerts, W.; Absil, P.; Van Thourhout, D.; Roelkens, G. High-efficiency fiber-to-chip grating couplers realized using an advanced CMOS-compatible Silicon-On-Insulator platform. *Opt. Express* **2010**, *18*, 18278–18283. [CrossRef] [PubMed]
29. Xia, C.; Chao Li, L.; Fung, C.K.Y.; Lo, S.M.G.; Tsang, H.K. Apodized waveguide grating couplers for efficient coupling to optical fibers. *IEEE Photonics Technol. Lett.* **2010**, *22*, 1156–1158.
30. Zaoui, W.S.; Kunze, A.; Vogel, W.; Berroth, M.; Butschke, J.; Letzkus, F.; Burghartz, J. Bridging the gap between optical fibers and silicon photonic integrated circuits. *Opt. Express* **2014**, *22*, 1277–1286. [CrossRef] [PubMed]
31. Pathak, S.; Vanslembrouck, M.; Dumon, P.; Van Thourhout, D.; Bogaerts, W. Compact SOI-based polarization diversity wavelength de-multiplexer circuit using two symmetric AWGs. *Opt. Express* **2012**, *20*, B493–B500. [CrossRef] [PubMed]
32. Carroll, L.; Gerace, D.; Cristiani, I.; Menezo, S.; Andreani, L. Broad parameter optimization of polarization-diversity 2D grating couplers for silicon photonics. *Opt. Express* **2013**, *21*, 21556–21568. [CrossRef] [PubMed]
33. Carroll, L.; Gerace, D.; Cristiani, I.; Andreani, L. Optimizing polarization-diversity couplers for Si-photonics: reaching the -1 dB coupling efficiency threshold. *Opt. Express* **2014**, *22*, 14769–14781. [CrossRef] [PubMed]
34. Snyder, B.; O'Brien, P. Packaging process for grating-coupled silicon photonic wave-guides using angle-polished fibers. *IEEE Trans. Compon. Packag. Manuf. Technol.* **2013**, *3*, 954–959. [CrossRef]
35. Pavarelli, N.; Lee, J.-S.; Rensing, M.; Scarcella, C.; Zhou, S.; Ossieur, P.; O'Brien, P. Optical and Electronic Packaging Processes for Silicon Photonic Systems. *J. Lightwave Technol.* **2015**, *33*, 991–997. [CrossRef]
36. Dangel, R.; Hofrichter, J.; Horst, F.; Jubin, D.; La Porta, A.; Meier, N.; Soganci, I.; Weiss, J.; Offrein, B. Polymer waveguides for electro-optical integration in data centers and high-performance computers. *Opt. Express* **2015**, *23*, 4736–4750. [CrossRef] [PubMed]
37. Van Campenhout, J.; Rojo Romeo, P.; Regreny, P.; Seassal, C.; Van Thourhout, D.; Verstuyft, S.; Di Cioccio, L.; Fedeli, J.; Lagahe, C.; Baets, R. Electrically pumped in P-based microdisk lasers integrated with a nanophotonic silicon-on-insulator waveguide circuit. *Opt. Express* **2007**, *15*, 6744–6749. [CrossRef] [PubMed]
38. Keyvaninia, S.; Roelkens, G.; Van Thourhout, D.; Jany, C.; Lamponi, M.; Le Liepvre, A.; Lelarge, F.; Make, D.; Duan, G.; Bordel, D.; et al. Demonstration of a heterogeneously integrated III-V/SOI single wavelength tunable laser. *Opt. Express* **2013**, *21*, 3784–3792. [CrossRef] [PubMed]
39. Park, H.; Fang, A.W.; Cohen, O.; Jones, R.; Paniccia, M.J.; Bowers, J.E. A Hybrid Al-Gainas-Silicon evanescent amplifier. *IEEE Photonics Technol. Lett.* **2007**, *19*, 230–232. [CrossRef]
40. Mack, M.; Peterson, M.; Gloeckner, S.; Narasimha, A.; Koumans, R.; De Dobbelaere, P. Method and System for a Light Source Assembly Supporting Direct Coupling to an Integrated Circuit. US Patent 8,168,939 B2, 1 May 2012.

41. Snyder, B.; Corbett, B.; O'Brien, P. Hybrid integration of the wavelength-tunable laser with a silicon photonic integrated circuit. *J. Lightwave Technol.* **2013**, *31*, 3934–3942. [CrossRef]
42. O'Carroll, J.; Phelan, R.; Kelly, B.; Byrne, D.; Barry, L.; O'Gorman, J. Wide temperature range 0 < T < 85 °C narrow linewidth discrete mode laser diodes for coherent communications applications. *Opt. Express* **2011**, *19*, B90–B95. [PubMed]
43. Kaur, K.S.; Subramanian, A.Z.; Cardile, P.; Verplancke, R.; Van Kerrebrouck, J.; Spiga, S.; Meyer, R.; Bauwelinck, J.; Baets, R.; Van Steenberge, G. Flip-chip assembly of VCSELs to silicon grating couplers via laser fabricated SU8 prisms. *Opt. Express* **2015**, *23*, 28264–28270. [CrossRef] [PubMed]
44. Ferrara, J.; Yang, W.; Zhu, L.; Qiao, P.; Chang-Hasnain, C.J. Heterogeneously integrated long-wavelength VCSEL using silicon high contrast grating on an SOI substrate. *Opt. Express* **2015**, *23*, 2512–2523. [CrossRef] [PubMed]
45. Lu, H.; Lee, J.-S.; Zhao, Y.; Scarcella, C.; Cardile, P.; Daly, A.; Ortsiefer, M.; Carroll, L.; O'Brien, P. Flip-chip integration of tilted VCSELs onto a silicon photonic integrated circuit. *Opt. Express* **2016**, *24*, 16258–16266. [CrossRef] [PubMed]
46. Worhoff, K.; Heideman, R.G.; Gilde, M.J.; Blidegn, K.; Heschel, M.; Van den Vlekkert, H. Flip-chip assembly for photonic circuits. In Proceedings of the SPIE 5454, Micro-Optics: Fabrication, Packaging, and Integration, Strasbourg, France, 8 September 2004.
47. Zhang, X.R.; Zhu, W.H.; Liew, B.P.; Gaurav, M.; Yeo, A.; Chan, K.C. Copper pillar bump structure optimization for flip chip packaging with Cu/Low-K stack. In Proceedings of the 11th International Conference on Thermal, Mechanical & Multi-Physics Simulation, and Experiments in Microelectronics and Microsystems (EuroSimE), Bordeaux, France, 26–28 April 2010.
48. Chen, K.M.; Lin, T.S. Copper pillar bump design optimization for lead free flip-chip packaging. *J. Mater. Sci. Mater. Electron.* **2010**, *21*, 278–284. [CrossRef]
49. Garrou, P.; Bower, C.; Ramm, P. *Chapter1: Introduction to 3D Integration in Handbook of 3D Integration Volume 1—Technology and Applications of 3D Integrated Circuits*; Wiley-VCH: Weinheim, Germany, 2008.
50. Fedeli, J.M.; Di Cioccio, L.; Marris-Morini, D.; Vivien, L.; Orobtchouk, R.; Rojo-Romeo, P.; Seassal, C.; Mandorlo, F. Development of silicon photonics devices using microelec-tronic tools for the integration on top of a CMOS wafer. *Adv. Opt. Technol.* **2008**. [CrossRef]
51. Wang, Y.-H.; Howlader, M.R.; Nishida, K.; Kimura, T.; Suga, T. Study on Sn-Ag Oxidation and Feasibility of Room Temperature Bonding of Sn-Ag-Cu Solder. *Mater. Trans.* **2005**, *46*, 2431–2436. [CrossRef]
52. Multicore MF210 VOC-free No Clean Flux. Available online: http://www.henkel-adhesives.com (accessed on 15 October 2016).
53. Horibe, A.; Lee, K.-W.; Okamoto, K.; Mori, H.; Orii, Y. No Clean Flux Technology for Large Die Flip Chip Packages. In Proceedings of the IEEE Electronic Components & Technology Conference, Las Vegas, NV, USA, 28–31 May 2013.
54. Choon-Mei, S.L.; Marbella, C.; Min, T.A. No-clean Polymer Flux Evaluations and its Impact on BGA Solder Joint Quality and Board Level Reliability. In Proceedings of the 34th International Electronic Manufacturing Technology Conference, Melaka, Malaysia, 30 November–2 December 2010.
55. Baehr-Jones, T.; Pinguet, T.; Guo-Qiang, P.L.; Danziger, S.; Prather, D.; Hochberg, M. Myths and rumours of silicon photonics. *Nat. Photonics* **2012**, *6*, 206–208. [CrossRef]
56. Kaspar, P.; Brenot, R.; Le liepvre, A.; Accard, A.; Make, D.; Levaufre, G.; Girard, N.; Lelarge, F.; Dan, G.-H.; Pavarelli, N.; et al. Packaged hybrid III-V/silicon SOA. In Proceedings of the European Conference on Optical Communication (ECOC), Cannes, France, 21–25 September 2014; pp. 1–3.
57. FDMA Access by Using Low-Cost Optical Network Units in Silicon Photonics. Available online: http://www.fabulous-project.eu (accessed on 15 October 2016).
58. Lindenmann, N.; Balthasar, G.; Hillerkuss, D.; Schmogrow, R.; Jordan, M.; Leuthold, J.; Freude, W.; Koos, C. Photonic wire bonding: A novel concept for chip-scale interconnections. *Opt. Express* **2012**, *20*, 17667–17677. [CrossRef] [PubMed]
59. Lindenmann, N.; Dottermusch, S.; Goedecke, M.L.; Hoose, T.; Billah, M.R.; Onanuga, T.; Hofmann, A.; Freude, W.; Koos, C. Connecting silicon photonic circuits to multi-core fibers by photonic wire bonding. *J. Lightwave Technol.* **2015**, *33*, 755–760. [CrossRef]

60. Benedikovic, D.; Cheben, P.; Schmid, J.H.; Xu, D.-X.; Lamontagne, B.; Wang, S.; Lapointe, J.; Halir, R.; Ortega-Monux, A.; Janz, S.; et al. Subwavelength index engineered surface grating coupler with sub-decibel efficiency for 220-nm silicon-on-insulator waveguides. *Opt. Express* **2015**, *23*, 22628–22635. [CrossRef] [PubMed]
61. Shen, B.; Wang, P.; Polson, R.; Menon, R. Integrated metamaterials for efficient and compact free-space-to-waveguide coupling. *Opt. Express* **2014**, *22*, 27175–27182. [CrossRef] [PubMed]
62. Yao, J.; Zheng, X.; Li, G.; Shubin, I.; Luo, Y.; Thacker, H.; Mekis, A.; Pinguet, T.; Sahni, S.; Raj, K.; et al. Grating-coupler-based optical proximity coupling for scalable computing systems. *SPIE Proc.* **2011**. [CrossRef]
63. Sodagar, M.; Pourabolghasem, R.; Eftekhar, A.A.; Adibi, A. High-efficiency and wideband interlayer grating couplers in multilayer Si/SiO2/SiN platform for 3D integration of optical functionalities. *Opt. Express* **2014**, *22*, 16767–16777. [CrossRef] [PubMed]
64. Bernabé, S.; Kopp, C.; Volpert, M.; Harduin, J.; Fédéli, J.-M.; Ribot, H. Chip-to-chip optical interconnections between stacked self-aligned SOI photonic chips. *Opt. Express* **2012**, *20*, 7886–7894. [CrossRef] [PubMed]
65. PhoeniX Software—Solutions for Micro and Nano Technologies. Available online: http://www.phoenixbv.com (accessed on 15 October 2016).
66. Luceda Photonics—Software and Services for Integrated Photonic Designers. Available online: http://www.lucedaphotonics.com/en (accessed on 15 October 2016).



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