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Title	Design and fabrication of silicon-on-silicon-carbide substrates and power devices for space applications
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Publication date	2017-05-23
Original Citation	Gammon, P. M., Chan, C. W., Gity, F., Trajkovic, T., Kilchytska, V., Fan, L., Pathirana, V., Camuso, G., Ben Ali, K., Flandre, D., Mawby, P. A. and Gardner, J. W. (2017) 'Design and Fabrication of Silicon-on-Silicon-Carbide Substrates and Power Devices for Space Applications', ES3 Web of Conferences., 16, pp. 12003. doi: 10.1051/e3sconf/20171612003
Type of publication	Article (peer-reviewed)
Link to publisher's version	10.1051/e3sconf/20171612003
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DESIGN AND FABRICATION OF SILICON-ON-SILICON-CARBIDE SUBSTRATES AND POWER DEVICES FOR SPACE APPLICATIONS

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ABSTRACT

A new generation of power electronic semiconductor devices are being developed for the benefit of space and terrestrial harsh-environment applications. 200-600 V lateral transistors and diodes are being fabricated in a thin layer of silicon (Si) wafer bonded to silicon carbide (SiC). This novel silicon-on-silicon-carbide (Si/SiC) substrate solution promises to combine the benefits of silicon-on-insulator (SOI) technology (i.e device confinement, radiation tolerance, high and low temperature performance) with that of SiC (i.e. high thermal conductivity, radiation hardness, high temperature performance). Details of a process are given that produces thin films of silicon 1, 2 and 5 µm thick on semi-insulating 4H-SiC. Simulations of the hybrid Si/SiC substrate show that the high thermal conductivity of the SiC offers a junction-to-case temperature *ca*. 4× less that an equivalent SOI device; reducing the effects of self-heating, and allowing much greater power density. Extensive electrical simulations are used to optimise a 600 V laterally diffused metal-oxide-semiconductor field-effect transistor (LDMOSFET) implemented entirely within the silicon thin film, and highlight the differences between Si/SiC and SOI solutions.

1. INTRODUCTION

Space is an expanding and changing market for power electronics. This is in part due to the rise of all electric propulsion systems for fine orbit control, as demonstrated for ESA mission GOCE, where a 600W/1.5kV QinetiQ T5 ion thruster [1] has been employed, and more widely for the orbit control of Geostationary Earth Orbit (GEO) telecommunications satellites. Furthermore, the big brother of the T5, the 5kW T6, has been developed to provide the impulse during the cruise phase of ESA's BepiColumbo mission to Mercury [2]. Another driver for space power electronics is the potential to move to high voltage transmission, beyond the 120 V maximum used today. This would allow harness weight, which can be up to 10% of satellite weight, to be greatly reduced given the reduction in I^2R losses [3]. Furthermore, 300 V solar cell output could open up the possibility of a direct drive power unit, the solar cells connected directly to hall thrusters without the need for an intermediate PPU, so saving significant weight and boosting efficiency.

A 2007 report entitled "*Extreme Environments Technologies for Future Space Science Missions*" by NASA's Jet Propulsion Laboratory [4] reviewed the state of space electronics and produced a roadmap for technology development if we are to explore some of the solar system's harshest environments. This described the benefit that could be gained from producing electronics that could survive and work reliably outside of the temperature controlled chamber; thus exposing the electronics to extreme highs, lows, and cycles of temperature. The potential system benefit of this approach would improve the efficiency of the cooling system, and increase the overall lifetime, reliability, and science capability of the mission.

The roadmap [4] cited wide bandgap semiconductors as the future for high temperature missions predicting performance up to 500°C, while low-voltage technology will continue to be dominated by silicon-on insulator (SOI) technology up to a maximum temperature of 300°C. Nearly ten years on from the publishing of this roadmap, silicon (Si) and silicon-on insulator (SOI) solutions remain almost entirely dominant in space power applications [5]. By confining the active area of the device, SOI devices achieve low leakage at high temperature [6]. SOI is often the rad-hard choice at low voltage too, the small volume of active material leading to excellent single event immunity [7]. However, a thick buried-oxide, which is required to support high voltage devices, make SOI devices much more sensitive to total ionizing dose (TID) effects.

Nearly ten years on from [4], wide bandgap semiconductors such as silicon carbide (SiC) and gallium nitride [8] are yet to make a significant impact on the space power market, though SiC Schottky diodes are being integrated into the solar inverter solution on BepiColombo [9]. SiC, in particular, has the potential to produce power systems that are smaller and lighter with improved efficiency, and high radiation and thermal tolerances. However, integration of full SiC solutions that include switching devices such as metal-oxide-semiconductor field-effect transistors (MOSFETs) are still held back by problems with long term reliability (particularly concerning the oxide), stability (threshold voltage and on-resistance drift) and packaging still hold back the continued integration of SiC both in space and terrestrially. Alternative solutions using JFETs [10]

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have been suggested, but not yet widely adopted.
In this paper, we introduce a new generation of lateral power electronic semiconductor devices that are being developed for the benefit of both space and terrestrial harsh-environment applications. The silicon-on-silicon carbide (Si/SiC) semiconductor substrate will attempt to improve upon current SOI technology by removing the buried oxide (BOX) layer that prevents efficient heat removal and causes poor TID tolerance. In its place will be a semi-insulating SiC substrate, with its high thermal conductivity and radiation hardness.
We will first introduce this concept showing the potential thermal benefits of the solution. We will then briefly summarise the results of simulations showing the advantages of this solution over conventional SOI. Furthermore, we will show for the first time the method used to fabricate our wafer bonded Si/SiC solution and the resulting wafers. At the conference, we will present the results of currently on-going device fabrication trials that are producing Si/SiC power devices in this substrate, specifically for space applications. The devices will include a 600 V LDMOSFET power transistor, and Schottky and PiN diodes.

2. THE Si/SiC CONCEPT

Lateral power devices including laterally diffused MOSFETs (LDMOS), lateral insulated gate bipolar transistors (LIGBT), and Schottky and PiN diodes, rated from 50 to 600 V will be implemented within a Si thin film 2 µm thick. The thin Si film sits directly on the surface of a high resistivity, semi-insulating 4H-SiC substrate. This can be pictured in Figure 1 alongside a proposed LDMOS Si/SiC transistor.
The Si/SiC solution benefits from the advantages of both materials, where thermally it is most akin to the highly thermally conductive SiC substrate, but

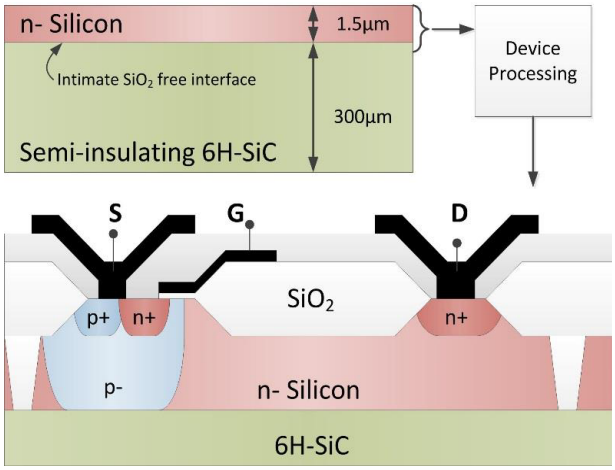


Figure 1: Top, the Si/SiC material system that has been developed. Bottom, proposed Si/SiC LD-MOS transistor.

electrically these devices are Si, or SOI devices. This can be summarised as follows:

SiC-like Thermal Performance: The thermal performance of the substrate is almost equivalent to SiC, resulting in a much lower temperature difference (ΔT) between the Si/SiC device's internal junction temperature and the local ambient temperature [11], compared to bulk Si or SOI. This can be exploited in one of three ways. In comparison to bulk Si or SOI, a Si/SiC device can operate either:

- in exactly the same ambient temperature, dissipating the same power, but with improved performance due to a reduction in the effects of self-heating;
- at a much higher temperature (as much as 100°C higher) for the same performance;
- or at the same temperature but at much higher power (as much as 4×), for the same performance.

Si Electronics. Electrically devices implemented in a Si/SiC substrate are akin to those in SOI or much closer, silicon-on-sapphire. Trapped charge at the SiC-oxide interface results in a MOSFET channel resistance that becomes limiting at voltage ratings of 600 V or below [6, 8]. The Si/SiC device will not suffer this problem, its channel being at a conventional Si/SiO_2 interface. Similarly, diodes and LIGBTs will benefit from the low built in potential at a Si p-n junction (~0.7 V) compared to SiC (~3 V). Furthermore, the processing of Si rather than SiC means that it is compatible with more conventional cleanroom equipment and procedures.

Radiation Immunity. The Si/SiC substrate is expected to offer high radiation hardness. Immunity to single event effects is expected for the same reason as SOI, due to the small volume of active material. Compared to SOI, Si/SiC devices are expected to have a higher TID tolerance due to the absence of a thick BOX layer under the active Si film and thus a lesser effect from radiation-induced oxide charge trapping on device performance. Furthermore, the SiC substrate itself has a high Si-C bond energy (large bandgap energy of 3.2 eV) and a high atomic displacement threshold in SiC of 21.8 eV [12], which is significantly higher than in Si.

Previous studies on Si/SiC electronics have concentrated on demonstrating MOSFET behaviour [13, 14] and the implementation of RF devices [15, 16]. Both showed that the effects of self-heating on the forward characteristics can be suppressed, unlike equivalent SOI devices power devices. These studies have shown experimentally [14] that the channel mobility of a Si/SiC MOSFET at 300°C and hence its channel resistance was just 10% worse than it was at room temperature, compared to an 83% reduction for an equivalent Si bulk device. Experimental results from RF devices implemented in a complicated Si/poly-Si/poly-SiC substrate [16], show that the negative-resistance effect of self-heating (whereby device resistance increases with voltage due to a rise in internal temperature) is minimised in the Si/SiC device, unlike an equivalent SOI device. However, breakdown voltage,

leakage current and maximum oscillation frequency were all shown to worsen. Other groups have considered SOI where the BOX and Si top layer is transferred onto a SiC substrate [17]. However, this is a methodology that our own modelling [11] proves to only fractionally reduce the self-heating problems of conventional SOI.

3. FABRICATING Si/SiC SUBSTRATES

100 mm Si/SiC wafers were fabricated by wafer bonding Norstel semi-insulating ($\geq 1.10^7$ Ω-cm) on-axis 4H-SiC to Icemos Technology Ltd SOI with a buried oxide 5 µm thick, and a lightly n- doped device layer (5 - 45 Ω-cm). Wafers have been produced with a device layer thicknesses 1, 2 and 5 µm thick. The full process used to develop the wafers can be seen in Figure 2.

Initial trials directly bonding the two virgin wafers via a number of methods (hydrophilic, hydrophobic, with and without a deposited interfacial oxide, and with and without a pre bonding anneal to limit outgassing) all resulted in either the handle wafer shearing under the strain, or in a high density of voids, visible in the hydrophobic bonded wafers the inset to Figure 3.

The problem of the voids was suspected to be the result of outgassing while the layers were undergoing a long high temperature anneal to form a permanent bond between the wafers. To overcome this problem, the first step taken in the bonding process (Figure 2) was to etch a grid of trenches 2 µm deep into the SiC surface prior to bonding, giving any gas an escape route during annealing. Next, after a proprietary surface plasma treatment, a hydrophobic bonding process was performed to form a temporary bond between the wafers.

A 2 hour, 1200°C anneal then formed a permanent bond between the wafers. However, the lattice mismatch between the materials resulted in a visible bow, the Si side of the wafer being convex. This still allowed, in the fourth step, for the Si handle wafer to be ground away down to the oxide later, which is simply removed with hydrofluoric acid.

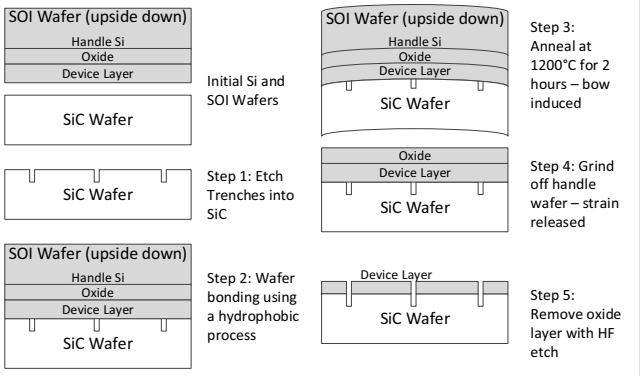


Figure 2: The Si/SiC substrate fabrication process.

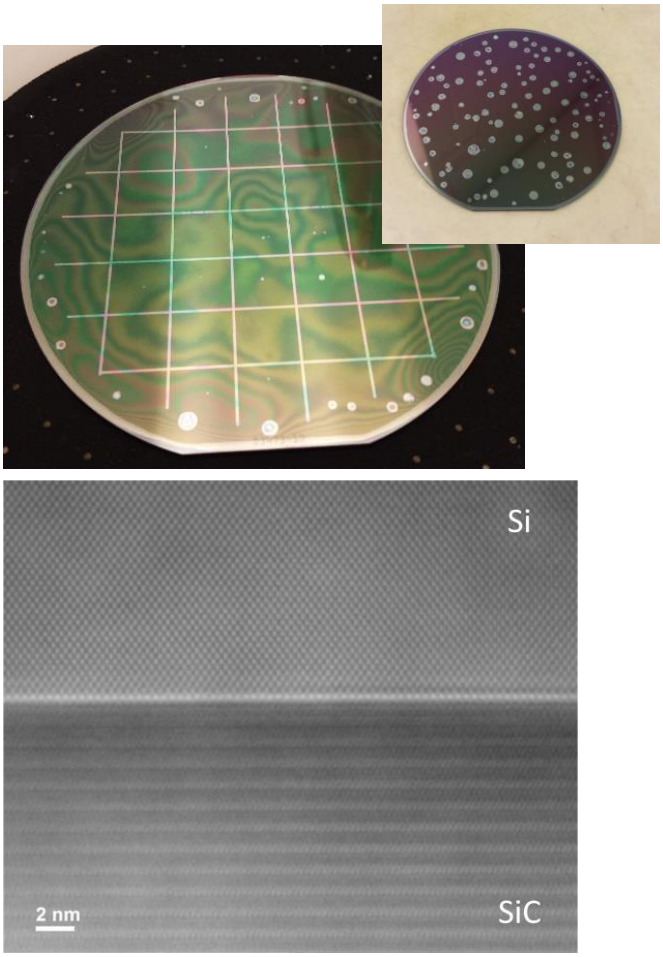


Figure 3: Above, a 100 mm wafer bonded Si/SiC wafer with a 1 µm Si device layer. Inset, the results of bonding without the grid etching. Below, a TEM image of the Si/SiC interface showing no sign of a SiO_2 interfacial layer.

A 2 hour, 1200°C anneal then formed a permanent bond between the wafers. However, the lattice mismatch between the materials resulted in a visible bow, the Si side of the wafer being convex. This still allowed, in the fourth step, for the Si handle wafer to be ground away down to the oxide later, which is simply removed with hydrofluoric acid.

The resulting 100 mm Si/SiC wafer can be seen in Figure 3. This particular wafer had a 1 µm Si device layer. 2 and 5 µm Si layers have also be successfully transferred. Transmission electron microscopy was used to analyse the interface between the wafers. This found that some voids were present at the interface, which may have an effect on current transport at this interface. Also, while the image in Figure 3 shows a clean oxide-free interface, some areas viewed did have a thin amorphous layer up to 2 nm thick which is highly likely to be silicon dioxide. Efforts will be made in the future to remove this by high temperature annealing as has been successful elsewhere [18]. X-ray diffraction analysis revealed no strain in the resulting device layer.

4. SIMULATING Si/SiC DEVICES

Recent work published by the authors [19] revealed the ability of devices implemented on Si/SiC substrates to dissipate effectively heat, and therefore operate at greater efficiency. 600 V LDMOS devices were implemented in the Si/SiC substrate and compared with very similarly implemented devices in SOI. The two layouts are shown in Figure 4. The physical structure of the two active regions of the devices were initially identical, each 42 µm-long, 0.2 µm-thick and with the same "IOS" layout that sees the gate contact extend over a thick field oxide over the drift region. These are based on SOI devices originally developed by Philips in the 1990s [20].

Despite their identical origins, for both devices to support the same blocking voltage (600 V) the linear doping used in the Si/SiC had to be half that of the SOI doping. This is because the drift region in the SOI solution is effectively narrower than that in the Si/SiC, the comparatively thin BOX having sufficient capacitance to form a depletion region in the drift region above.

The results of the simulation study [19] showed that both these devices would break down above 640 V at both room temperature and at 300°C. I-V results from the forward DC characteristics of the devices are shown in Figure 5. Comparing for each device the difference between simulations that ignore the effects of temperature (isothermal) and those that take it into account (non-isothermal), reveals the impact of removing the buried oxide. The isothermal and non-isothermal simulations for the Si/SiC devices are nearly identical with minimal junction temperature, the waste heat generated in the layer having been efficiently channelled through the SiC substrate. However, the SOI can be seen to suffer so-called negative resistance, with the devices failing to remove the heat from the device effectively, so resulting in significant decreased current at a given gate and drain voltage, and significant internal heating.

Further detailed simulations are shown in [19].

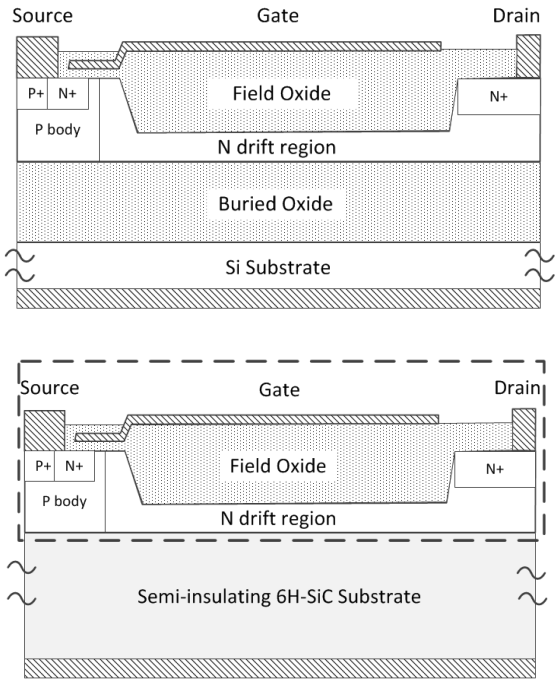


Figure 4: The layout of the simulated SOI (above) and Si/SiC (below) LDMOS transistors.

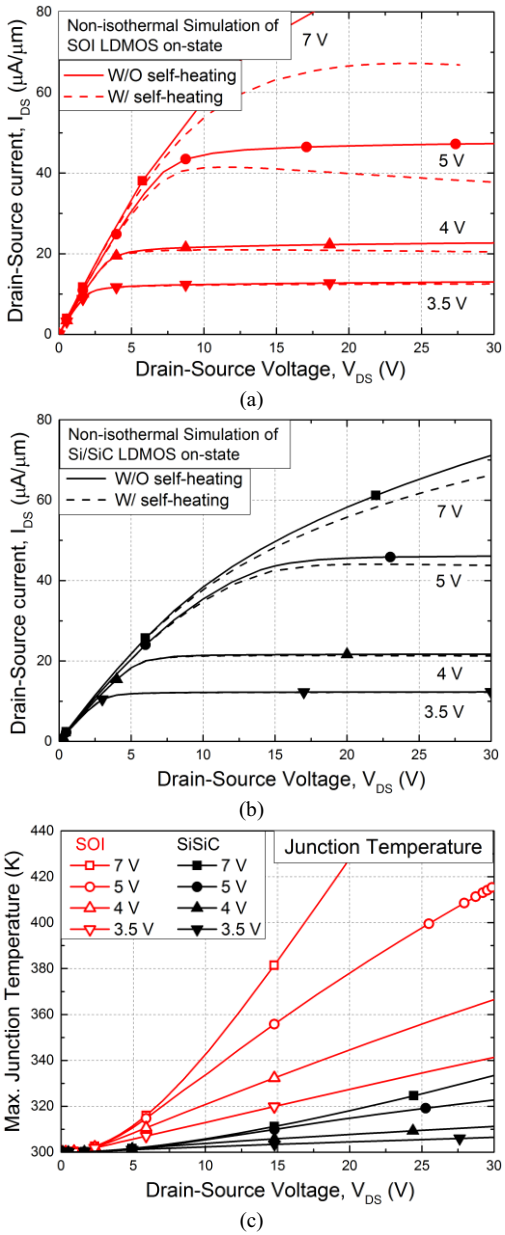


Figure 5: The effect of self-heating on (a) the forward characteristics of the SOI and (b) the Si/SiC LDMOS, as well as (c) their junction temperature. (a) and (b) show both isothermal results ignoring the effects of self-heating (solid) and non-isothermal results including the effects of heating (dashed).

5. FABRICATING AND TESTING Si/SiC DEVICES FOR SPACE APPLICATIONS.

At the conference, the results of on-going fabrication trials will be presented. Power devices including Schottky and PiN diodes, and LDMOS devices akin to those in Figure 4 have been fabricated, leading to some very interesting, and unexpected results.

We will present the results of these entirely new devices at the conference for the first time.

6. CONCLUSION

The results presented detail an on-going project to fabricate the first lateral power devices in a Si/SiC substrate. The novel combination of materials offers significant thermal benefits over current state of the art SOI power electronics, reducing self-heating effects, which will improve maximum operating temperature, and efficiency at any given temperature. These devices will be of particular interest to the space sector; the low volume of active material, the absence of a BOX and the wide bandgap substrate all adding to the radiation tolerance of the final solution. Novel Si/SiC wafer bonding has led to the development of 1, 2 and 5 µm thin films of silicon directly bonded to semi-insulating 4H-SiC. Efforts to produce the first power diodes and transistors in this substrate are on-going.

7. ACKNOWLEDGMENTS

The work presented in this paper has been carried out as part of the EU funded SaSHa Project (Si on SiC for the Harsh Environment of Space): www.sashaproject.eu/. We gratefully acknowledge the support of the European commission for this funding.

Dr. Peter Gammon would also like to acknowledge support from the Royal Academy of Engineering, and from the EPSRC (Project EP/N00647X/1).

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