# Investigation of High-*k*/$In_xGa_{1-x}As$ Interfaces

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The quality of the high-*k*/$In_xGa_{1-x}As$ interface is a crucial factor in achieving high electron mobility compound semiconductor field effect transistors. Capacitance and conductance characterisation methods were employed to evaluate different high-*k*/InGaAs interfaces. This paper will first discuss the specificity of capacitance voltage characteristics of compound semiconductor MOS structures, and then the recent progress in the study of high-*k*/$In_xGa_{1-x}As$ interfaces will be presented. The capacitance and conductance measurements are combined to provide a picture of the interface state density. We have also investigated the merit of using intermediate *k* value dielectrics such as $Al_2O_3$ and MgO as interface control layers between the semiconductor and the main high *k* layer.

## Introduction

The recent introduction of $HfO_2$ in the gate stack of Si CMOS devices has led to significant transistor performance enhancement [1]. However, the incorporation of a high dielectric constant (high-*k*) material into the gate stack combined with future device scaling indicates that the near ideal $Si/SiO_2$ interface will no longer be at the heart of future MOSFETs. This has opened new opportunities for high electron mobility compound semiconductors to replace Si as an n-channel material for future MOSFETs. The low quality native oxides of III-V semiconductors and the absence of dielectrics exhibiting excellent III-V semiconductor/dielectric interfaces have always been a major obstacle to the advance of large scale III-V ICs. In recent years there have been breakthroughs in the field of deposited dielectrics on III-V materials, such as a very low interface state density being achieved using *in situ* MBE grown $Ga_2O_3$ on GaAs [2] or by using a silicon passivation layer between the GaAs surface and the oxide layer providing a significant improvement in the capacitance interface state response [3].

## Capacitance Characteristics of Compound Semiconductor MOS Structures

Several electrical characterisation techniques to investigate the oxide/semiconductor interface have been successfully employed for many years [4]. All these methods were established and developed to study the $Si/SiO_2$ system which has been at the heart of MOSFET devices for more than four decades. With the introduction of new high-*k* dielectrics in the gate stack and the search for alternative high mobility channel materials to replace Si, a need has emerged to understand, adapt and appropriately interpret the specific features of conventional electrical measurement techniques when applied to compound semiconductor MOS structures. In this section, we will briefly describe the capacitance voltage techniques and the specific considerations when applying these to compound semiconductors devices.

The contribution of interface states to the measured capacitance

The capacitance voltage characteristic of a MOS capacitor consists of three main components: the oxide ($C_{ox}$), the semiconductor ($C_s$) and the interface states ($C_{it}$) capacitance contributions. Each capacitance component exhibits different dependence upon applied bias, temperature, and measurement frequency. Assuming a constant capacitance contribution for the oxide, both the semiconductor and interface state capacitance responses vary with bias and frequency [4]. The semiconductor capacitance is strongly voltage dependent in the entire voltage range and also shows frequency dependence in the inversion region depending on the ability of the minority carriers to follow the measurement frequency. The interface states capacitance contribution varies also with voltage and frequency. This dependence is related to the Fermi level position at the interface which defines the portion of the band gap which is probed, as well as defining the response time associated with the capture and emission of free carriers at the interface.

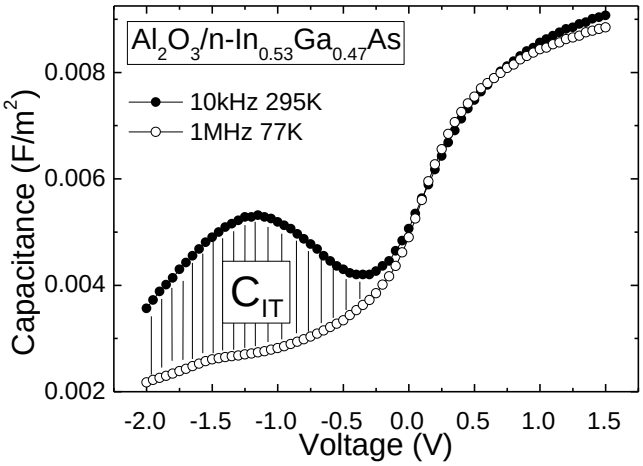


Figure 1. $Al_2O_3/In_{0.53}Ga_{0.47}As$ CV characteristics measured at high frequency and liquid Nitrogen temperature compared to room temperature CV measured at lower frequency to demonstrate the interface states response.

When all the interface states are able to respond to the measurement frequency, their associated capacitance is added to the semiconductor differential capacitance which in turn is in series with the oxide capacitance. The total measured capacitance can then be expressed as:

$$C_m = \left( \frac{1}{C_{ox}} + \frac{1}{C_s + C_{it}} \right)^{-1} \qquad [1]$$

When the interface states are not able to follow the measurement frequency, they do not contribute to the differential capacitance. In this case the interface states cause a

stretch out of the CV characteristics induced by their charging when the Fermi level is swept across the band gap. The frequency and temperature measurement parameters can be used to either maximise or eliminate the $C_{it}$ component. Figure 1 illustrates this method.

The density of interface states for each gate voltage condition is then extracted using the following equation [4]:

$$C_{it} = \left( \frac{1}{C_{LF}} - \frac{1}{C_{ox}} \right)^{-1} - \left( \frac{1}{C_{HF}} - \frac{1}{C_{ox}} \right)^{-1} \quad [2]$$

where $C_{LF}$ and $C_{HF}$ are the measured capacitance characteristics at low frequency (room temperature ~ 295K) and high frequency ($LN_2$ temperature ~ 77K) respectively. The temperature dependence of other parameters could affect the results obtained using this method, for instance if the oxide presents border traps or if the semiconductor exhibits carrier freeze out (usually observed in wider band gap materials or lower temperature) the $C_{LF}$ and $C_{HF}$ difference can be then caused by other sources than interface states. In the case presented in figure 1, the comparison is justified since both CVs are identical in accumulation and part of the depletion region. By comparing the low temperature CV with a simulated ideal CV curve without an interface state component (figure 2) the Fermi level position at the interface for a given gate voltage can be extracted. This allows the density of interface states as a function of the band gap energy to be constructed. The noticeable asymmetry in the simulated CV will be discussed later.

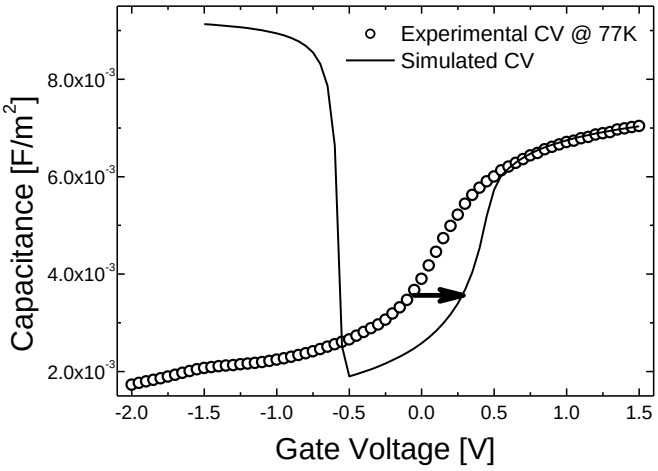


Figure 2. Comparison of the $Al_2O_3/In_{0.53}Ga_{0.47}As$ CV response measured at 77K and 1MHz with a simulated CV curve to show the stretch out originating from the charging of interface states as the Fermi level is swept towards the conduction band.

Capacitance voltage characteristic in the presence of a very large interface state density

When measuring the CV characteristics of a silicon MOS capacitor, rarely is the magnitude of $D_{it}$ so high that it prevents clear observation of the inversion, depletion, and

accumulation regimes. However, certain processing conditions could generate very high $D_{it}$ levels in Si MOS capacitors. Figure 3a presents the CV response of a Ni(100)/$HfO_2$(3.5nm)/$SiO_x$(3nm)/n-Si MOS capacitor. The 3.5nm $HfO_2$ film was formed by electron beam evaporation from a solid source of $HfO_2$ under a film densifying Ar plasma. These processing conditions not only generate a thick $SiO_x$ (3nm) interlayer but also cause significant lattice damage at the interface [5]. It is clear from figure 3a that the CV characteristics must be measured over a large frequency range in order to get an idea of the level of the interface state contribution. This example illustrates the case that is very often encountered when investigating oxide/compound semiconductor interfaces. Figure 3b presents the CV characteristics of a Pd(100nm)/$HfO_2$(11.4nm)/n-GaAs MOS structure measured at different frequencies. Despite a three stage chemical passivation step [6] and the ALD growth of $HfO_2$ as opposed to the harsher electron beam evaporation technique, the frequency dispersion is still very large. The GaAs interface does not reach true accumulation as might be inferred if one analyses the low frequency (1 kHz) CV characteristic alone.

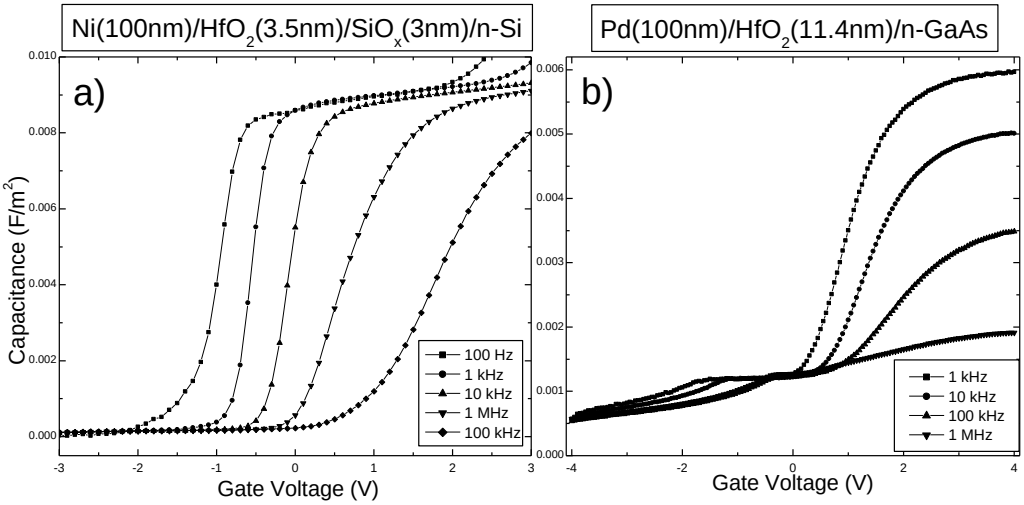


Figure 3. a) Multi frequency CV characteristics of Ni(100)/$HfO_2$(3.5nm)/$SiO_x$(3nm)/n-Si. The $HfO_2$ film was formed using electron beam evaporation under Ar ion assist. b) Multi frequency CV characteristics of Pd(100nm)/$HfO_2$(11.4nm)/n-GaAs. The $HfO_2$ film was formed by ALD.

Compound semiconductor capacitance voltage characteristics

The investigation of oxide/compound semiconductor interfaces using CV techniques often requires the simulation of the ideal CV of the studied structure. The $In_{0.53}Ga_{0.47}As$ MOS theoretical CV curves obtained using 1D Schrodinger-Poisson solvers present a very significant difference when compared to conventional CVs on Si MOS structures. Figure 4 shows the simulated CV for an Au/$Al_2O_3$(8nm)/n-$In_{0.53}Ga_{0.47}As$ structure [7]. The large asymmetry in the CV is the most remarkable feature as compared to a conventional CV on a Si MOS device. This difference is due to the lower effective density of states in the conduction band ($Nc \sim 2x10^{17} cm^{-3}$) than in the valence band ($Nv \sim 5x10^{18} cm^{-3}$) for $In_{0.53}Ga_{0.47}As$. In order to visualise the origin of this asymmetry we

have plotted the surface potential as a function of gate voltage. Figure 4 shows that the surface potential increases at higher rate with voltage in accumulation than it does in inversion. This means the Fermi level at the surface moves well into the conduction band. The semiconductor capacitance $C_s$, which is the surface charge differential with respect to the surface potential, is therefore considerably reduced in accumulation relative to $C_s$ in inversion (for n-type $In_{0.53}Ga_{0.47}As$). Similar effects have been described for MOS structures fabricated on narrow band gap II-VI compounds [8].

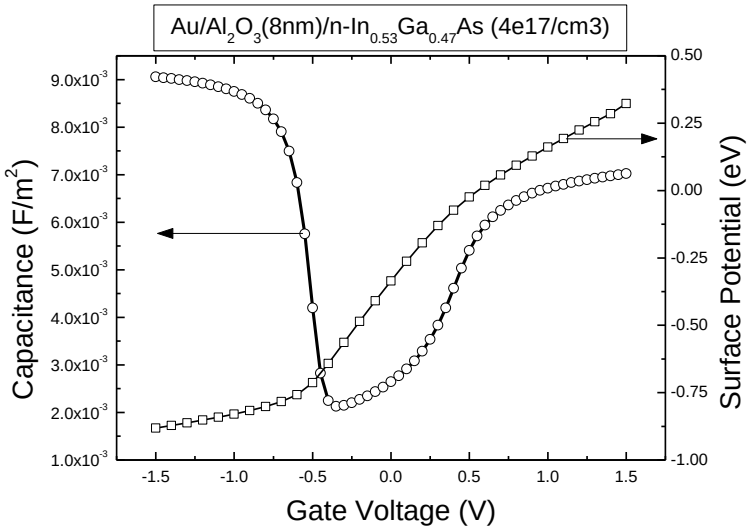


Figure 4. Simulated CV curve for a $Au/Al_2O_3(8nm)/n\text{-}In_{0.53}Ga_{0.47}As$ structure. The surface potential dependence upon gate voltage is also presented. No quantum confinement effects were included in the simulation.

In the case of Si, $C_s$ in accumulation or inversion is much greater than $C_{ox}$ due to the large Nc and Nv values for Si ($Nc(Si)\sim 3x10^{19}cm^{-3}$ and $Nv(Si)\sim 2x10^{19}cm^{-3}$). Considering equation (3), $C_{max}\sim C_{ox}$ for Si whereas the correction factor is significant for $In_{0.53}Ga_{0.47}As$ and different from accumulation to inversion.

$$C_{max} = C_{ox}\left(1+\frac{C_{ox}}{C_s}\right)^{-1} \qquad [3]$$

It is interesting to note that the asymmetry and the large capacitance correction are present in the theoretical CV curve (figure 4) while the quantum effects are not included in the simulation. The confinement of free carriers at the interface further increases the divergence of $C_{max}$ from $C_{ox}$.

## High-*k*/InGaAs Interfaces

In this section we will present a study carried out on three different oxides stacks on $In_{0.53}Ga_{0.47}As$ interfaces where the characterisation methods described in the previous section were employed. The sample set consisted of one $HfO_2$ control sample and two bi-layer samples: $HfO_2/Al_2O_3$ and $HfO_2/MgO$. Both $Al_2O_3$ and MgO interlayers are selected

for their wide band gap compared to $HfO_2$. The aim of this study is to investigate the electrical properties of the oxide/$In_{0.53}Ga_{0.47}As$ with and without interlayers.

Experimental Details

The sample set used in this study consisted of: Pd/$HfO_2$(5nm)/$In_{0.53}Ga_{0.47}As$, Pd/$HfO_2$(5nm)/$Al_2O_3$(1nm)/$In_{0.53}Ga_{0.47}As$ and Pd/$HfO_2$(5nm)/MgO(1nm)/$In_{0.53}Ga_{0.47}As$. The 2μm thick $In_{0.53}Ga_{0.47}As$ epilayer was grown by MOVPE lattice matched on n+ InP. The Si n type doping in the $In_{0.53}Ga_{0.47}As$ epilayer was $3.5x10^{17}cm^{-3}$. The samples were preserved under $N_2$ ambient prior to loading in an ALD reactor for oxide deposition, in order to minimise the ambient exposure time pre-ALD. The InGaAs surface was untreated prior to ALD. The precursors used for the $HfO_2$, MgO, and $Al_2O_3$ films were $Hf[N(C_2H_5)(CH_3)]_4$, $(C_5H_5)_2Mg$, and $Al(CH_3)_3$ respectively in combination with $H_2O$. The growth temperature was 250°C. The 200nm Pd gate electrodes were formed by electron beam evaporation and lift off lithography process.

Results and discussion

The current density measured at positive gate bias shows uniform leakage properties across all three samples (figure 5). As expected the $HfO_2$ control sample (smallest physical thickness) presents the lowest breakdown voltage. The $HfO_2/Al_2O_3$ stack shows the highest breakdown voltage. In the 1V to 4V bias range the control sample exhibits a lower leakage current density than the $MgO/HfO_2$ despite the extra ~ 1 nm MgO layer. This could be explained by the presence of a trap assisted tunnelling current mechanism, as is the subject of further investigations.

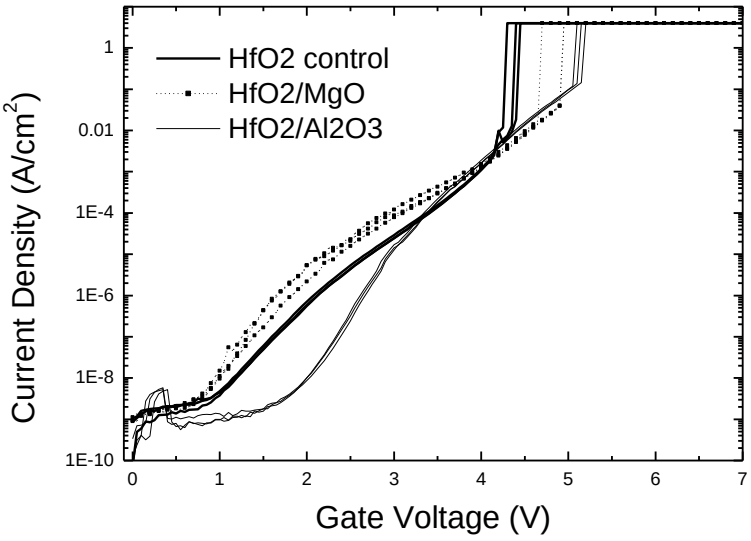


Figure 5. Leakage current densities measured on several 50x50 $\mu m^2$ sites on each sample.

Figure 6 (a, b and c) presents the CV characteristics of the three samples measured over a wide range of frequencies. The capacitance equivalent oxide thickness is highest for the control sample and lowest for the $Al_2O_3/HfO_2$ bi-layer. This result correlates with the breakdown trend for this set of samples. Assuming the interlayer and $HfO_2$ physical

thickness to be identical for both bi-layer samples this indicates that the MgO film has a higher dielectric constant than the $Al_2O_3$. The frequency dispersion in the accumulation region for the three samples could be induced by oxide border traps which are able to respond to the measurement frequency [9]. This effect should be less prominent in MOS structures with thicker oxides as the oxide traps contribution to the capacitance could be dominant regardless of its fluctuation with frequency and as a result the measured capacitance will tend to $C_{max}$ with less dispersion.

All three samples also display significant frequency dependence in the depletion/inversion region of the CV. In the case of an interface defect with a discrete energy level in the band gap, the CV curve is expected to go through a peak (observed at intermediate frequencies in figures 6a, 6b and 6c). The continuous increase of capacitance in inversion at low measurement frequency could be attributed either to the minority carriers being able to respond to the low frequency or to the presence of more interface states deeper in the band gap.

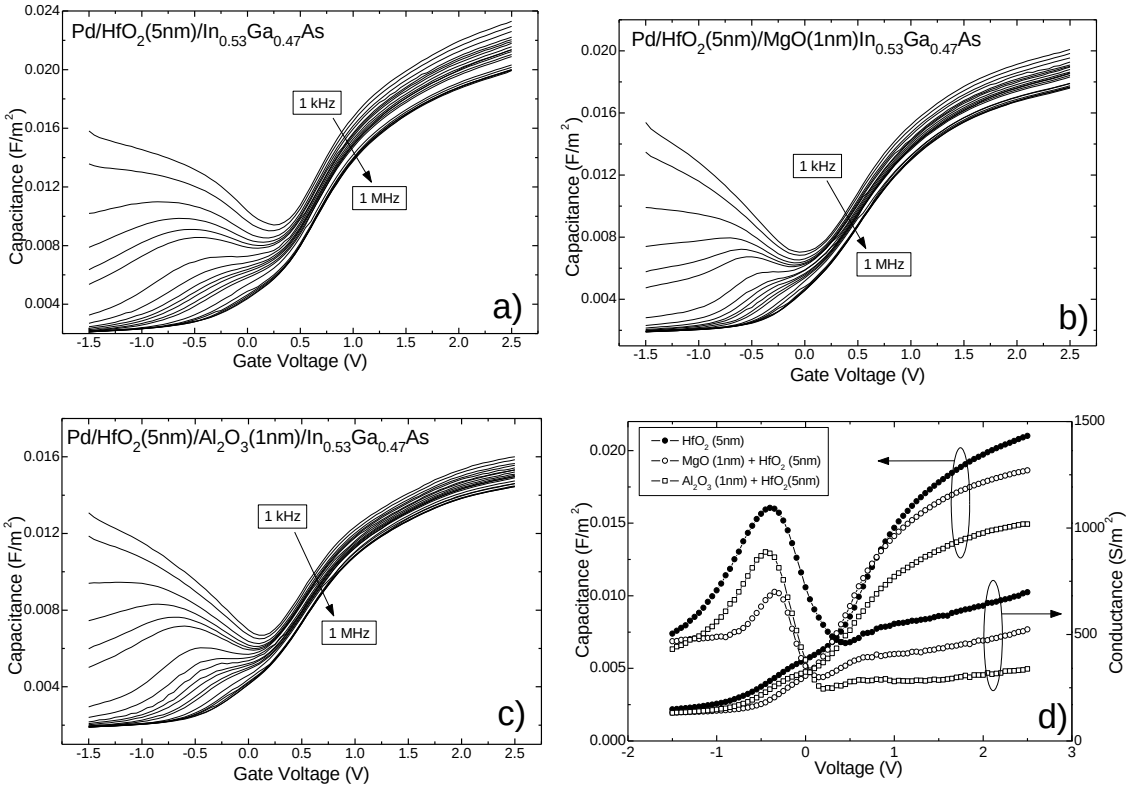


Figure 6. Capacitance voltage characteristics measured over a range of frequencies (1kHz to 1MHz) for a) $HfO_2$ control sample, b) $MgO/HfO_2$ bi-layer and c) $Al_2O_3/HfO_2$. d) is a CV and GV comparison of all three samples at 100 kHz.

Figure 6d compares the Capacitance and Conductance voltage characteristics measured at 100 kHz on the three samples. The peak conductance (from -1V to 0V) falls in the same bias range as the frequency dependent shoulder in the CV characteristics confirming the conductance loss originates from the interface states. The fact that the interface states behaviour is very similar on all three samples indicates that the dominant interface defect originates from the $In_{0.53}Ga_{0.47}As$ surface as opposed to the oxide. It must

be emphasised that these electrical characteristics are similar to already published results on $In_{0.53}Ga_{0.47}As$ MOS structures with unpassivated [10], sulphur passivated [11], and $(NH_4)OH$ passivated surfaces [12]. The $In_{0.53}Ga_{0.47}As$ surface in the current study received no chemical passivation treatment, no post deposition anneal, and no forming gas ($N_2/H_2$) annealing. The fact that the results are comparable with those obtained for chemically passivated surfaces is due to careful preparation of the MOVPE $In_{0.53}Ga_{0.47}As$ epilayers and the fast transfer to the ALD reactor for oxide deposition where exposure to ambient air is kept to minimum.

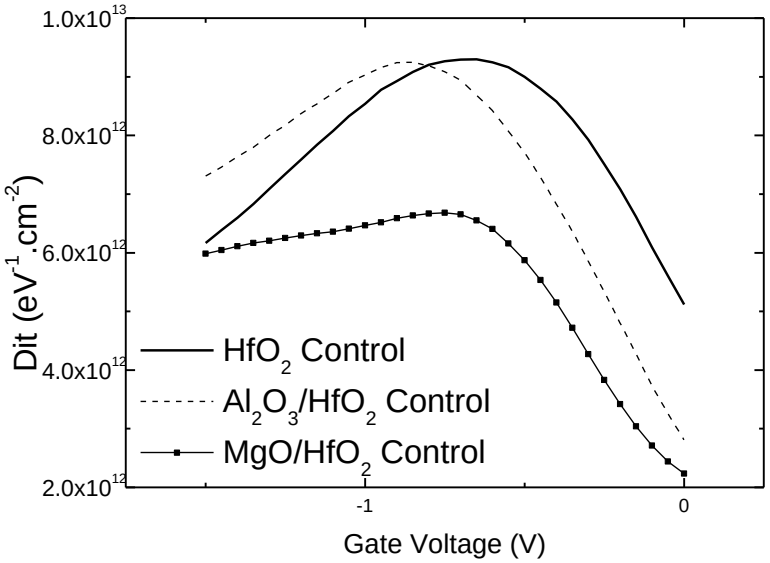


Figure 7. Estimated interface state densities extracted using equation (2) and the relation $D_{it} = C_{it}/q$. The low and high frequency CVs were measured at 6 kHz and 1MHz respectively (room temperature).

The high-low frequency method described in the first section was applied to these samples. Figure 7 shows the extracted density of states profiles as a function of gate bias for the three samples using equation (2) and the relation $D_{it} = C_{it}/q$. In this study the lowest frequency measurement available couldn't be exploited for this analysis. As the measurement frequency is reduced in order to maximise the interface states response other contributions are also brought into play. In the depletion region, minority carriers will produce a capacitance which will affect the $D_{it}$ curve [13]. The data presented in figure 7 was extracted using the capacitance measured at 6 kHz and at 1 MHz. It must be emphasised that the profiles generated using intermediate frequencies could lead to a slightly underestimated density of interface states. However, these profiles are useful for a comparative evaluation of the interface state densities present in the different samples since they are obtained under the same conditions. In addition the densities extracted using this CV method confirm the conductance results of figure 6d for which the $HfO_2$/MgO sample presents the lowest $D_{it}$. The peak $D_{it}$ position was found to be located ~ 0.4eV above the $In_{0.53}Ga_{0.47}As$ valence band using the simulated surface potential dependence upon gate voltage (not shown).

## Conclusion

We have described capacitance voltage characterisation techniques when applied to compound semiconductors. Some of the significant differences as compared with common Si MOS characteristics were discussed. In the second part, the efficacy of three high-*k*/$In_{0.53}Ga_{0.47}As$ MOS structures in terms of device electrical behaviour was compared. The benefit of using an $Al_2O_3$ or an MgO interlayer between the $HfO_2$ film and the $In_{0.53}Ga_{0.47}As$ surface was compared in terms of leakage current and interface state density. The MgO material presented the lowest interface state density ($\sim 6x10^{12}$ $eV^{-1}.cm^{-2}$) of all three samples examined.

## Acknowledgments

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