

Integration of Edge Emitting Quantum Dot Laser onto Silicon Photonics Platforms by Transfer Printing

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Abstract

Photonic integrated circuits (PICs) enable the implementation of complex optical systems with a small footprint, opening up new applications and minimising energy consumption. Similar to electronic circuits, PICs can be manufactured in foundries at decreasing costs with increased volume, following the successful trend observed in the electronics industry. Currently, the primary applications for PICs are in transceivers for the data communications industry, driven by the growing demand for higher bandwidths. This demand necessitates increased bandwidth density for server-to-server interconnects while reducing energy dissipation and costs per Gbps. However, the absence of an integrated light source imposes limitations on silicon-based photonic integrated circuits. The development of on-chip lasers that can operate at high ambient temperature with low-loss coupling to PICs is crucial.

This research focusses on the development of transfer-printable InAs/GaAs quantum dot (QD) based edge-emitting lasers and their integration onto various silicon photonics platforms by micro transfer-printing (MTP). Firstly, the fabrication process flow to realise transferable QD lasers on native GaAs substrate has been developed and standardised to enable low-threshold, high-efficiency QD lasers. We deal with the development and optimisation of various processes including plasma etching of facets to obtain a smooth and vertical mirror, stress management of laser coupons, design of tethering system, and release etch process based on HCl for the AlGaAs sacrificial layer with varying Al content ranging from 90 to 95 % to release the devices from the native substrate with high selectivity. Receiver waveguides are then designed and simulated on various platforms including 220 nm SOI, 3 μm SOI and 300 nm SiN with an SU-8 spot size converter (SSC). These waveguides are optimised to achieve effective light edge coupling from the laser into the waveguides with relaxed alignment tolerance.

Here, transfer printed laser diodes on Si substrate with 70 nm BCB exhibit a threshold current of 15 mA and provide an output power of more than 60 mW at an injection current of 160 mA. This implies that there is no degradation in device performance after transfer printing. The same device delivered an output power of 43 mW at 70°C in continuous-wave (CW) mode. In addition, integration of 4.5 μm thick 65 μm wide QD laser devices up to 2.4 mm long is demonstrated on the above platforms with a >95% yield. At 100 mA, waveguide coupled powers of 7.7 mW, 2.0 mW, and 1.2 mW are measured after out-coupling from the 220 nm SOI, 3 μm SOI and 300 nm SiN waveguides, respectively. The integration and optical coupling challenges and proposed solutions are discussed.

This work presents a potential path for achievement of integrated light sources for silicon photonics by demonstrating the versatility of the technology with the same lasers integrated onto different waveguide platforms.

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Ali

List of Publications

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Abbreviations

2D	Two-Dimensional
2DEG	Two-Dimensional Electron Gas
3D	Three-Dimensional
5G	Fifth Generation Cellular Broadband Network Technology
Al	Aluminum
AlGaAs	Aluminum Gallium Arsenide
AlInP	Aluminum Indium Phosphide
AI	Artificial Intelligence
AlF₃	Aluminum Fluoride
BCB	Benzocyclobutene
BOE	Buffered Oxide Etch
BOX	Buried Oxide
CF	Cleaved Facet
CMOS	Complementary Metal Oxide Semiconductor
CW	Continuous Wave
DC	Directional Coupler
DFB	Distributed Feedback
DI	Deionized
DBR	Distributed Bragg Reflector
EF	Etched Facet
ES	Excited State
EIC	Electronics Integrated Circuit
FP	Fabry-Perot
FIB	Focused Ion Beam
FWHM	Full Width Half Maximum
GaAs	Gallium Arsenide
Ge	Germanium
GS	Ground State
HCl	Hydrochloric Acid
HR	High Reflectivity
IC	Integrated Circuit
IoT	Internet of Things
InAs	Indium Arsenide
InGaAs	Indium Gallium Arsenide
ICP	Inductively Coupled Plasma
IPA	Isopropyl Alcohol
InP	Indium Phosphide
InGaP	Indium Gallium Phosphide
LiDAR	Light Detection and Ranging

LNOI	Lithium Niobate on Insulator
MD	Misfit Dislocation
MTP	Micro Transfer Printing
ML	Machine Learning
MMI	Multi-Mode Interference
MIR	Multi-Mode Interference Reflector
MME	Molecular Beam Epitaxy
MMF	Multi-Mode Fiber
MOCVD	Metal Organic Chemical Vapor Deposition
PIC	Photonics Integrated Circuit
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PGMEA	Propylene Glycol Monomethyl Ether Acetate
PDMS	Polydimethylsiloxane
OSA	Optical Spectrum Analyser
QD	Quantum Dot
QW	Quantum Well
RIE	Reactive-Ion Etching
Si	Silicon
SiPh	Silicon Photonics
SEM	Scanning Electron Microscope
SiN	Silicon Nitride
SiO₂	Silicon Dioxide
SOA	Semiconductor Optical Amplifier
SOI	Silicon on Insulator
SiNOI	Silicon Nitride on Insulator
SMSR	Side Mode Suppression Ratio
TE	Transverse Electric
TMAH	Tetramethylammonium hydroxide
TDD	Threading Dislocation Density
VCSEL	Vertical Cavity Surface Emitting Laser
WG	Waveguide

I, Ali Uzun, certify that this thesis is my own work and I have not obtained a degree in this university or elsewhere on the basis of the work submitted in this thesis.

Ali Uzun

Chapter 1

Introduction

Over the past century, electronic integrated circuits (ICs) have had a significant impact on the world and individuals. They can be found almost everywhere, such as mobile phones, cars, smart watches, etc. This has been made possible by the extraordinary development of complementary Metal-Oxide-Semiconductor (CMOS) manufacturing and the microelectronics industry, which has led to exponential improvements in device performance, size and efficiency. The explosion of internet traffic due to the growth of cloud computing and data-intensive platforms such as social networking and video streaming requires more bandwidth and data rates. Recent developments in the Internet of Things (IoT) and Artificial Intelligence (AI) are putting even more pressure on the current data centres infrastructure where almost all of these services run in some way. This requires the development of a more scalable infrastructure to meet the enormous demands while maintaining energy efficiency and complexity. Silicon (Si)-based photonic integrated circuits (PICs) offer a means of reducing complex optical systems to the scale of a chip, enabling optical transceivers with higher bandwidth and data rate. PICs can be manufactured at lower cost with increasing volume, as demonstrated by the success of electronic circuits.

One of the key components for PICs are the light sources, the lasers, which until now have had to be integrated in a back-end step. It is important that the chosen laser technology can withstand the high-temperature environment typically found in the racks of large data centres in order to realise the full potential of silicon photonics. This thesis focusses on the design, fabrication and characterisation of InAs/GaAs quantum dot (QD)-based edge-emitting O-band lasers integrated on various silicon photonics (SiPh) platforms using micro-transfer printing techniques. In this introductory chapter, the reader is introduced to the motivation behind this dissertation. An overview of optical interconnects in the data centre is briefly discussed. Photonic integrated circuits for telecommunications are then discussed, with particular emphasis on QD based devices. A brief history of QD lasers is

presented, followed by the state of the art of InAs/GaAs lasers. The chapter ends with the objectives and an overview of the rest of the thesis.

1.1 Silicon Photonics in Data Centers

The fast-growing data traffic generated by fifth generation (5G) applications and cloud services is driving bandwidth demand, increasing the need for advanced internet and data centre infrastructure to handle zettabyte-scale data transfers. Due to the rapid increase in the use of AI and Machine Learning (ML), it is predicted that the amount of annual data traffic will increase more than 100 times in the next 5 years, as shown in Fig. 1.1 [1, 2].

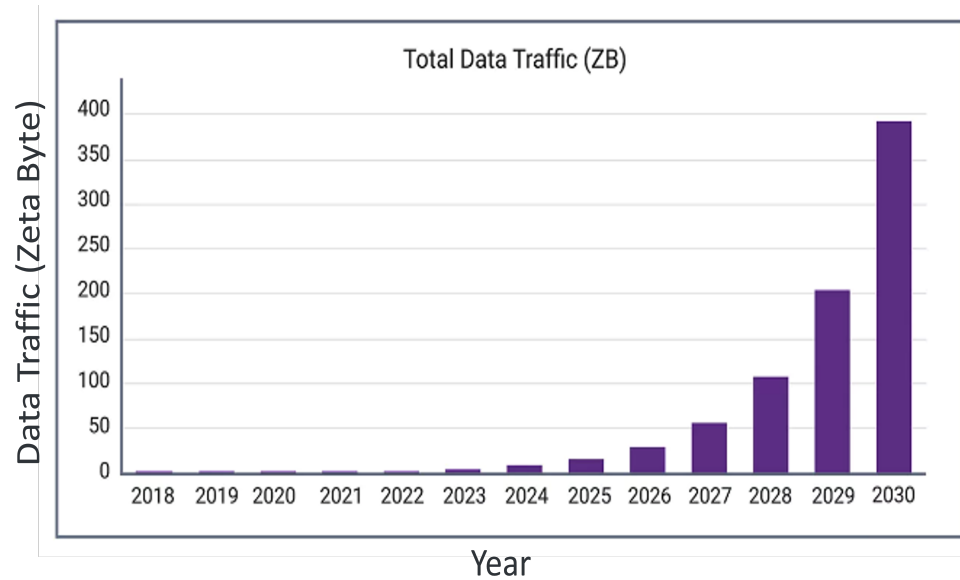


Figure 1.1: Total Data Traffic Forecast. 380 ZB of IP traffic by 2030.[1]

The optical interconnects that carry almost all of this traffic are also widely deployed to connect racks within and between data centres. An optical transceiver is required at both ends of each fibre to facilitate signal conversion between electrical and optical signals. Optical transceivers are named for being both optical transmitters and optical receivers, which convert electrical signals into light signals and light signals back into an electrical signals, respectively. The length of these optical links can range from a few metres to hundreds of kilometres. Vertical cavity surface emitting laser (VCSEL) based optical links with multimode fibre (MMF) have been the dominant optical interconnect technology for short distance intra-rack connections under 300 *m*. The trend is moving from 40 gigabits per second (Gbps), 40G, to higher network speeds with 100G and 400G becoming more common. For intra-rack interconnects (< 30 *m*), direct attach copper cable is still the dominant technology due to its low cost, simple construction and low power consumption [3]. Long-span interconnects (500 *m* to 10 *km* links), usually based on edge-emitting lasers, typically use single-mode fibre with

network speeds of 100G and beyond. Traditional indium phosphide (InP) [4] and silicon photonics [5] material platforms are seen as promising candidates enabling higher speed with this technology. The trend for these interconnects is towards even large network speeds of 800G and beyond. Component sales by key industry players support the predicted trends as shown in Fig. 1.2. It is clear that there is a need for a faster and more efficient optical transceiver with an on-chip light source.

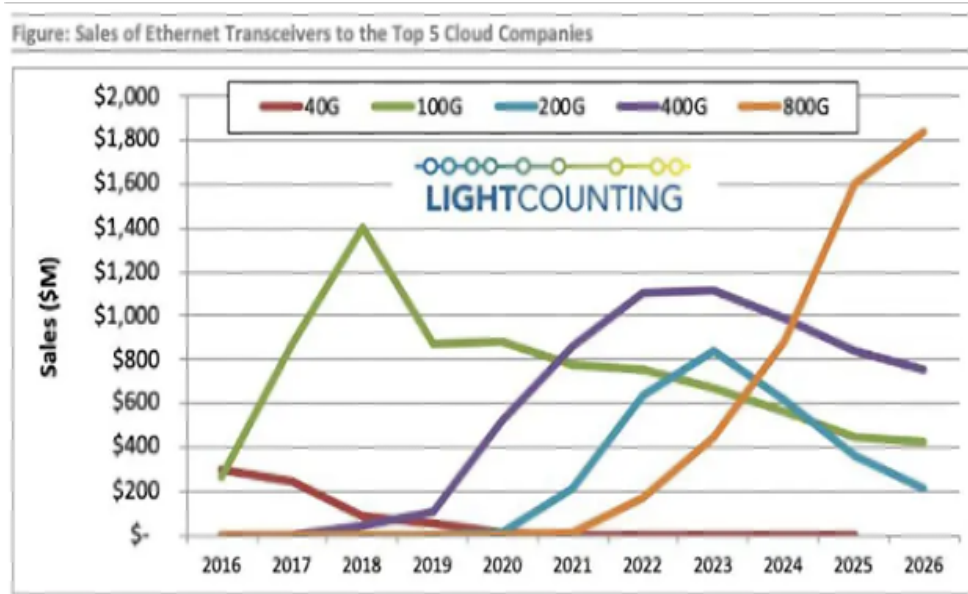


Figure 1.2: Sales of ethernet transceivers. 800G optical modules are expected to dominate this market segment by the end of the 2025 time-frame [6].

In this work, transfer-printable edge-emitting InAs/GaAs quantum dots (QD) lasers operating around 1310 nm are developed. The developed lasers are targeted to be used to demonstrate an 800G transceiver under the scope of the CALADAN project [7]. CALADAN is a European H2020 project focussing on micro-transfer printing technology to integrate optical (i.e. GaAs quantum dot lasers) and electrical (high speed SiGe BiCMOS chips) components on 300 mm silicon photonic wafers. The required specification for the laser is an emission wavelength range of 1304.5 nm to 1317.5 nm with 6 nm drift from 0 to 70°C and power in the waveguide of > 10 mW at 70°C. Considering the thermal requirements, there is a need for a light source with better thermal insensitivity to further improve the transceiver performance. QD-based light sources are promising candidates due to their excellent thermal stability that reduces the need for complex cooling systems. In addition, the O-band light source operates near the zero dispersion wavelength of standard single-mode fiber (approximately 1310 nm). This minimises dispersion effects, making it ideal for high-speed data transmission over short distances without the need for complex dispersion compensation. This thesis investigates the development of transfer-printable O-band etched facet QD lasers and their integration onto various photonics platforms via micro-transfer printing and light edge-coupling into the

receiving waveguides on these platforms.

1.2 Photonics Integrated Circuits

The currently available CMOS platform provides a cost-effective design environment for photonic integrated circuits (PICs) due to the exceptional interfaces and refractive index contrasts achievable between Si, SiO₂, Si₃N₄ and other dielectrics. Using different combinations of these materials on an insulator substrate (i.e. SOI, SiNOI), it is possible to design waveguides that can span optical wavelengths from ultraviolet to infrared [8–10]. PICs offer a means of reducing complex optical systems to the scale of a chip, opening up new applications, and reducing energy consumption. PICs can be manufactured at a lower cost because of their high compatibility with CMOS technology, enabling scaled production. Currently, the main application for PICs is in transceivers for data communications. However, PIC technology is increasingly being applied to signal processing, 5G, LiDAR, metrology, sensing, neuromorphic and machine learning applications, with future prospects for high-volume consumer applications.

PICs are being developed on a variety of material platforms. The InP-based platform offers excellent functionality, but its integration is complex and proprietary. InP technology is ideal not only for light generation but also for the realisation of all essential optical functionalities, including passive waveguiding, detection, amplification, and modulation. Waveguide propagation losses of 0.45 dB/cm at 1.55 μm have been reported for passive device performance on this platform [11]. However, the expensive and small-sized substrate can be listed as the main drawbacks in this platform [12]. The advantage of silicon photonics over InP is its CMOS compatibility, which allows integration processes to be performed in CMOS foundries. This provides a well-controlled and highly scalable fabrication environment with technical expertise. In addition, the larger size of silicon substrates (such as 200 and 300 mm diameter wafers) compared to InP substrates (75 - 150 mm diameter wafers) increases its potential for high-volume production with reduced cost per die. However, silicon photonics is severely limited by the lack of integrated light sources and amplifiers, which limits its suitability for large-scale integration.

The main focus of industry is on the silicon-on-insulator (SOI) platform, since silicon is an ideal waveguide for near-infrared wavelengths due to its high index contrast (refractive index of Si ~ 3.5 at 1.31 μm) with the surrounding silicon dioxide (SiO₂, $n_{\text{SiO}_2} \sim 1.5$). This high index contrast waveguide enables more compact designs with waveguide bends having radii $< 5 \mu\text{m}$. In addition, waveguide propagation losses of 0.1 dB/cm (at 1.55 μm) make it a promising low-loss platform [13]. The thickness of the Si waveguide layer ranges from 220 nm to 3 microns. The silicon nitride (SiN) platform allows PICs to cover a wider wavelength range (0.4 to 2.35 μm) with

ultra-low waveguide loss, i.e. 0.0005 dB/cm at $1.58 \mu\text{m}$, with a waveguide bend radius down to $165 \mu\text{m}$ [14]. The low index contrast of SiN ($n_{\text{SiN}} \sim 2$ at $1.31 \mu\text{m}$) results in a larger footprint. Finally, Lithium Niobate on Insulator (LNOI) is an emerging alternative platform due to its strong non-linear/electro-optic properties [15].

1.3 Light Sources for Silicon Photonics Circuits

Given the inefficiency of Si-based materials as light sources, alternative semiconductors such as III-V semiconductors are required. The challenge of integrating a silicon light source lies in its indirect bandgap, which results in a low rate of radiative recombination upon excitation. In contrast, direct bandgap materials such as III-V alloys exhibit efficient radiative recombination, making them superior light emitters when carriers in the conduction band are externally pumped. Although it is possible to tune the bandgap of germanium to direct by strain and heavy doping, the lasing performance of these materials falls short of that of III-V alloys. III-V compound semiconductors offer operational advantages and wavelengths suitable for efficient laser sources in silicon photonics.

The integration of III-V light sources into silicon photonics requires a simple integration layout and high-efficiency light coupling to maximise performance. This integration can be external or on-chip, using different coupling methods and integration layouts. External laser setups, such as fibre-to-PIC or external cavity lasers, and on-chip solutions, such as monolithically grown III-V lasers or heterogeneously integrated lasers, are used. These configurations are considered hybrid when the laser mirrors are outside the III-V, typically on the SOI waveguide. Different types of light coupling strategies together with the selected approach are discussed in detail in chapter-3 in section 3.1.

Considerable efforts have been made to establish low-cost integration technologies for III-V based devices on Si PICs. Various approaches including direct epitaxial growth, die-to-wafer/wafer-to-wafer bonding, flip-chip bonding and micro-transfer printing are being explored and an overview of these techniques is given in the next section.

1.3.1 Monolithic Laser

The concept of monolithic integration of III-V semiconductors on a silicon substrate by hetero-epitaxial growth is considered the ultimate approach, enabling Si photonic chips with large-scale processing and dense integration. However, this method presents greater integration challenges due to the significant lattice mismatch between direct bandgap III-V materials and Si, as well as variations in thermal expansion coefficients and polar/non-polar interface properties [16–18].

Germanium (Ge)-based monolithic light sources are considered a good candidate because of their lattice constant, similar to that of Si, and their availability in CMOS foundries. The lasers developed using this technique have a threshold current density around three times higher than III-V based counterparts [19, 20]. The poor device performance makes them unsuitable for commercial applications. The growth of III-V materials on Si offers a more promising route with several challenges for the growth of high quality III-V epitaxial layer stacks on Si substrate. Due to the significant lattice mismatch between Si (5.431 Å) and common III-V compounds (lattice constant ranging from 5.6 Å to 6.5 Å), the integration of III-V on Si remains a major bottleneck for high-volume and low-cost manufacturing. Such a large lattice mismatch leads to defects such as antiphase boundaries, threading dislocations, and misfit dislocations in the resulting III-V epilayers on Si. Several approaches have been developed to mitigate the formation of defects. Employment of intermediate buffer layers, trapping layers, and asymmetric step-graded filters to minimise threading dislocation densities (TDDs) and block misfit dislocations (MDs) in bulk III-V material [17, 21]. The monolithic integration of III-V lasers on Si by heteroepitaxial growth using molecular beam epitaxy (MBE) and metal organic chemical vapour deposition (MOCVD) has gained considerable attention in recent years. All these techniques enable the growth of high-quality material only when very high control over thickness, composition, and doping is achievable during the growth process [22, 23]. The use of off-cut with a small angle (typically 4°- 6°) towards the (011) plane on a Si(001) substrate with a thick buffer layer moderate performance lasers is demonstrated [24, 25]. An alternative approach is the planar hetero-epitaxy of GaAs [26, 27] and InP [28, 29] on V-grooved Si substrates. The monolithic integration of III-V QD lasers on Si is the most promising light source due to their high insensitivity to defects. InAs quantum dots (QDs) for high-performance O-band lasing has been realised with up to 100°C continuous-wave (CW) lasing operations [30, 31]. A significant issue in this techniques is the lack of a suitable coupling schemes into the Si waveguides. More recently, selective area growth hetero-epitaxy that facilitates light coupling to a Si waveguide without needing a thick buffer layer has been developed. In this techniques, a SiO₂ hard mask is used to grow the III-V layer on the target area by taking advantage of the difference in growth rate on top of the silicon and SiO₂ mask using a MOCVD process. The III-V / SiO₂ interfaces block defects as they cannot protrude through the SiO₂ layer [32].

1.3.2 Heterogeneous Laser

A significant effort has been invested in low-cost integration of high-performance III-V devices including, lasers on different photonics platforms. It is considered a mature technology that is used in commercial applications in comparison to monolithic integration. Several approaches have been explored including wafer/die bonding,

flip-chip technique, and micro-transfer printing (MTP).

1.3.2.1 Wafer/Die Bonding Technology

Wafer/die bonding involves integration of an unpatterned III-V die or wafer onto an SOI wafer in an upside-down configuration [33, 34]. Bonding can be done directly, by molecular bonding, by plasma-assisted surface activation, or with an adhesive layer. This technique has attracted considerable attention because of the high alignment accuracy of the III-V structure to the waveguide using a wafer-scale lithographic process.

After III-V bonding, the substrate is removed by grinding and wet etching, leaving only the functional device layer on the SOI wafer. The wafers/dies are then converted into devices following the III-V device fabrication process. Lithographically aligned III-V devices to the underlying waveguide can be achieved with high throughput. The need to remove the III-V substrates prior to processing can be a significant cost in high-volume production. In addition, the lack of pre-integration testing of devices and the limitation of cointegration of devices from different III-V epitaxial structures on the common PIC can be listed as challenges of the approach. It should be noted that this technology is commercialised by Intel.

1.3.2.2 Flip-chip Bonding Technology

Flip-chip integration technique is a mature technology and is mostly adopted in the electronic ICs industry. Solder bumps deposited on the device are employed to enable the bonding to the host substrate. These bumps also facilitate electrical connection. The chip was then bonded in a p-side-down configuration to the correct pads on the target substrate, as shown in Fig. 1.3. A re-flow process is needed to melt the bumps and form a reliable electrical path. An alignment accuracy below $0.5\ \mu\text{m}$ with a waveguide coupled power of $10\ \text{mW}$ is reported through a passive alignment using markers on both chips using a flip-chip bonding tool [35]. A self-aligned process through mechanical alignment of flipped-chip to receiving waveguide would allow a better alignment [36]. Using similar mechanical alignment steps, InP- and GaAs-based lasers [37, 38] have been bonded to the flip chip on SiN platforms with insertion loss below -3 dB and waveguide-coupled power above $10\ \text{mW}$.

This approach allows processing of the active photonic devices on the source wafer using III-V technology and testing the devices prior to integration, ensuring integration of working devices. Wafer scale integration is also achievable with this technique. However, the sequential assembly process makes this technique slow and costly.

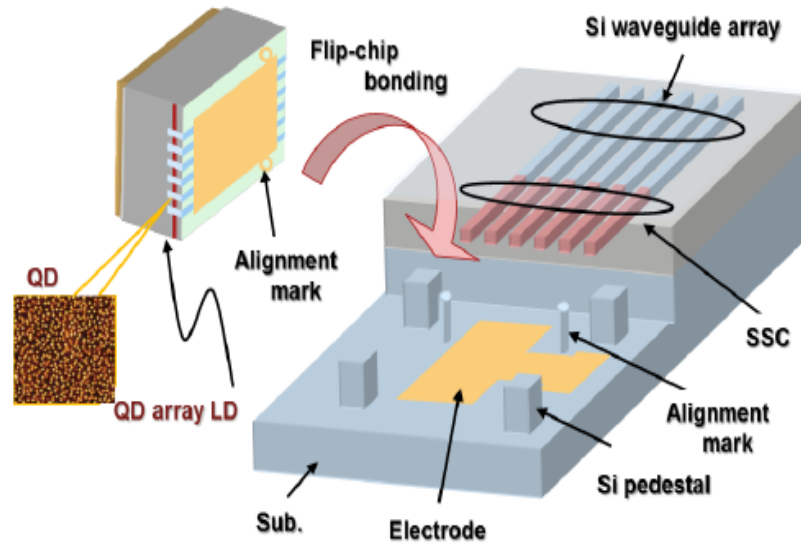


Figure 1.3: Illustration of GaAs QD laser array flip-chip integrated onto Si platform. Edge coupling of light into the Si waveguide and alignment tolerance is improved by the Spot Size Converter (SSC), which acts as a temporary waveguide [38].

1.3.2.3 Micro-Transfer Printing Technology

micro-transfer printing (MTP) is a relatively new approach with a powerful technology developed at the University of Illinois in 2004 [39]. This technique allows heterogeneous integration of a thin film material, also called a device layer and coupon, from a source wafer where these films are grown and processed, onto a target substrate with a typical placement accuracy of $< 1.5 \mu\text{m}$ at 3σ distribution with respect to the target location by passive alignment [39, 40]. Sub-micron alignment precision is also possible with alignment markers on both the coupon and the target using image recognition-assisted auto-alignment [41–43]. If the device structure is processed after transfer-printing, lithographic alignment of features is also achievable. Each print cycle takes less than 1 min including alignment. The material or device, called a coupon, is transferred to locally flat patterned substrates in an epitaxial side-up fashion. The prefabricated coupons (either partially or fully fabricated) on their native substrate in dense arrays with $< 100 \mu\text{m}$ pitch allows efficient use of expensive III-V materials. It also enables the integration of coupons based on very different layer arrangements and thicknesses on a single chip. This means that lasers, modulators and detectors grown and fabricated in different material systems can be integrated on the same target PICs. A further advantage of this integration is that no modification to the Si photonics back-end process flow is required other than the local opening of the trenches that accommodate the coupons. It combines the advantages of flip-chip integration and die-to-wafer bonding. For example, similar to flip-chip assembly, MTP allows pre-testing of device coupons on their native substrate prior to integration on a target wafer. In addition, the availability of wafer-scale parallel

integration of coupons using multi-post stamps, resulting in very high throughput, has led to MTP attracting a lot of attention in recent years.

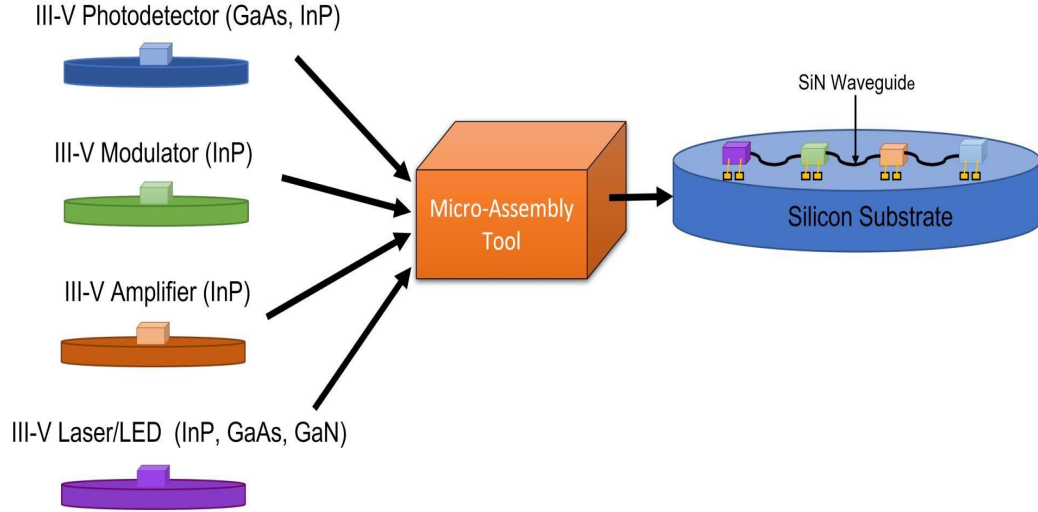


Figure 1.4: Three main components of MTP: Sources (Left), Transfer-printer (Centre), and Target (Right) [44].

This technique has a very high compatibility and can be applied to almost all materials as long as a release process is adapted to separate them from their native substrate. Due to its versatility and high-volume potential, MTP has been demonstrated for wide-range of material including InP [42, 45], GaAs [46, 47], GaN [48, 49] as well as electronic integrated circuits (EICs) [50]. Similarly, the coupons can be transfer-printed onto the different silicon photonics platforms including SOI, SiNOI, LNOI. This thesis presents micro-transfer printing of fully fabricated InAs/GaAs QD based edge-emitting lasers onto different waveguiding platforms such as 3 μm SOI, 220 nm SOI and 300 nm SiNOI.

MTP involves three main components such as source coupon preparation, target preparation, and transfer printing. The source wafer contains dense arrays of coupon devices based on different materials, which are first fabricated on their native substrates. After release etching of the coupons on the III-V source wafer, the coupons are ready for integration. The target wafers that will host the multi-material coupons are prepared for bonding. The primary requirement for successful integration is a flat and planar surface on the target, with or without a thin adhesive layer to aid bonding. Once the source and target are ready, the final component is a transfer printing tool (stamp) that facilitates the pick-and-place operation, as summarised in Fig.1.4. The transfer printer is the tool that allows devices to be picked up from the source wafer and printed onto the target wafer at the desired location using a polydimethylsiloxane (PDMS) stamp. The stamp, which contains single or multiple posts, allows specific coupons to be integrated onto the target wafer in a sequential or parallel manner.

1.3.2.4 Working Principle of MTP

The stamp is one of the key enablers of this technology. The PDMS stamp is an elastomeric material with visco-elastic properties that allow the adhesion strength to be tailored to the other surface according to the separation speed. It allows devices to be picked up or released by varying the speed of retreat of the PDMS stamp [51–53].

The adhesion strength between the stamp and the coupon is tuned by varying the velocity of the stamp motion and quantified in terms of the separation energy ($G_{stamp}(v)$) as a function of the peel-off speed (v) between the stamp and the coupon as:

$$G_{stamp}(v) = G_0 \left[1 + \left(\frac{v}{v_0} \right)^n \right] \quad (1.1)$$

where G_0 is the separation energy at rest (when v approaches zero), v_0 is the reference velocity at which G_{stamp} is twice the value of G_0 , n is a scaling parameter that can be experimentally determined.

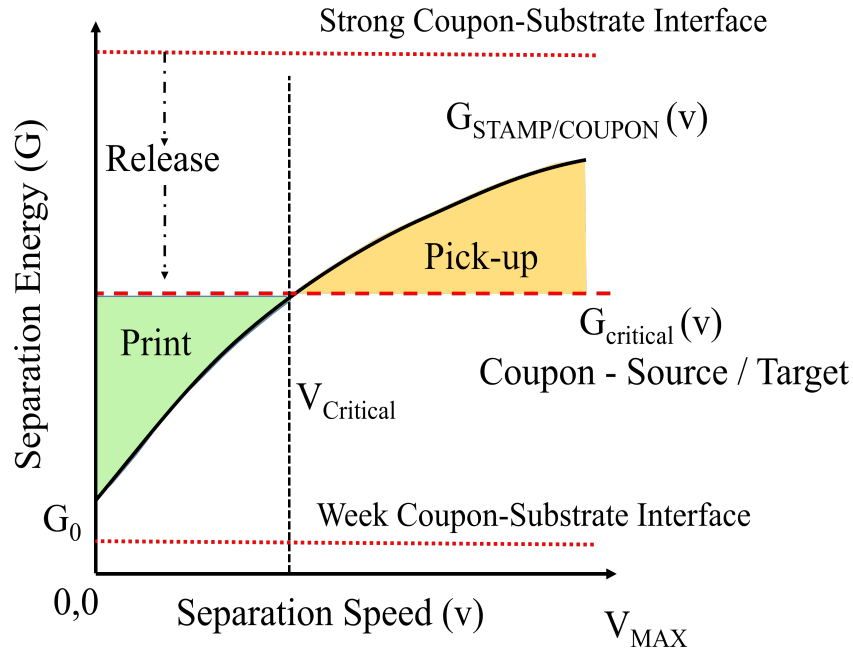


Figure 1.5: Schematic illustration of the speed-dependent adhesion strength between the stamp and coupon during pick-up and print. The dashed-red line indicates the critical release energy rate at the interfaces between coupon and both source and target substrate. The dotted-horizontal lines at the bottom and top represent the release rate the weak and strong coupon to substrate interfaces. The intersection of the horizontal line in the middle with the curve represents the critical peel velocity for the kinetically controlled transfer printing. (adapted from [51]).

From equation 1.1 it can be concluded that the separation energy (G) increases steadily with the velocity (v). The change in adhesion energy as a function of separation speed is schematically illustrated in Fig.-1.5. The vertical line represents

the critical velocity at which $G_{critical}$ equals $G(v_{critical})$. In order to pickup a coupon the adhesion of the PDMS stamp to the coupon defined by its separation energy, G_{stamp} , must be greater than the adhesion of the coupon to its substrate, G_{source} . Unlike pick-up, the G_{stamp} should be lower than the adhesion of the coupon to the target substrate, G_{target} . Thus, it needs to satisfy $G_{stamp} > G_{source}$ and $G_{target} > G_{stamp}$ to facilitate pickup and transfer printing, respectively.

These conditions can be satisfied by tailoring the retract velocities of the stamp, which is expressed as:

$$v_{critical} = v_0 \left(\frac{G_{critical} - G_0}{G_0} \right)^{\frac{1}{n}} \quad (1.2)$$

It is clear that the retract velocity of the stamp should be greater than the critical velocity ($v > v_{critical}$) for the pick-up and lower than the critical velocity ($v < v_{critical}$) for printing.

The pick-up and print of the coupon is schematically illustrated in Fig. 1.6. First, the devices, also known as coupons, are fabricated on their native substrate and made ready for integration following the release etch. The fabrication process of the QD lasers are presented in chapter-2 (section 2.3). The PDMS stamp, designed to match the size of the coupons in width and length, touches the top surface of the coupon for pick-up. A stamp can have a single post to pick-up and print one device at a time, or multiple posts for transfer-printing of array of devices in one cycle. Single or array printing does not change the overall printing process. During pick up, the adhesion between the coupon and the stamp must be higher than the adhesion between the coupon and the substrate. An overdrive of a few 10 microns (the typical overdrive value used in this work is 20 to 30 μm) is required to ensure the good contacts at the stamp - coupon interface during pick-up. The stamp pick-up speed used in this work is $\sim 100 \text{ mm/sec}$. Increasing the stamp speed will enhance the adhesion strength of the stamp to the coupon and break the tethers. The picked-up coupons are then transferred to the desired location on the target wafer. Following the alignment of the coupon with the receiving waveguide using the markers on both the coupon and the substrate through the transparent PDMS stamp, the printing takes place. In contrast to the pick-up, the adhesion between the coupon and the stamp during the print-step must be less than the critical value, which corresponds to the adhesion between the bottom surface of the coupon and the target surface. Successful printing can be achieved by reducing the retreat speed of the stamp and applying a shear force in the planar direction to detach the coupons from the stamp. The speed of the stamp during printing in this work is $\sim 30 \mu m/sec$. The target circuit can have a planar surface or a topography surface with recess for transfer printing of the devices. In this work transfer printing of QD laser coupons up to 2.4 mm long is transfer-printed onto

various targets including blank Si and glass wafers with a planar surface and SOI wafer with and without recess. The print yield above 90% was achieved during integration on the surface with an adhesive layer at clean-room temperature (typically $\sim 20^\circ\text{C}$).

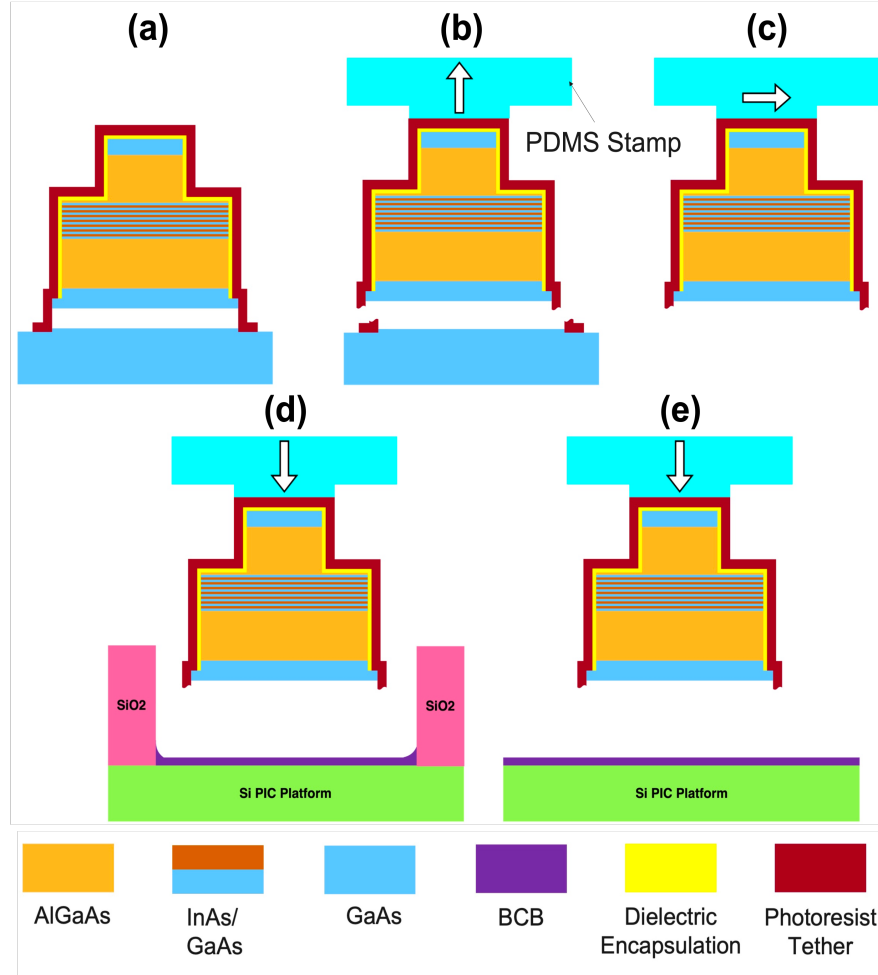


Figure 1.6: (a) Fully released coupon anchored with tethers on III-V substrate. (b) Pick-up of the coupon with a PDMS stamp, (c) Transfer of the coupon and (d)-(e) printing of coupons into a recess on SOI or onto a planar surface, respectively.

1.3.3 Choice of the Integration Strategy for InAs/GaAs QD lasers

Each integration technique has its own advantages and limitations. Table 1.1 presents a summary of common integration techniques and compares the MTP technique with them. Wafer/die and flip-chip bonding have shown excellent integration capabilities and matured enough for commercial use in the industry. Thus, there is an established supply chain. This approach provides high alignment of the waveguide to the SOI due to post-integration. Although the efficiency of the III-V material can be considered high, further improvement is needed for large-scale production. The lack of device pre-testing prior to integration to the target PIC is the main limitation of this technique. A sub-micron alignment accuracy can be achieved through flip-chip and

MTP integration via passive alignment. Additionally, both of these techniques provide pre-testing that would improve the integrated III-V yield on SOI by eliminating the non-functional devices. The sequential integration process of the die in the flip-chip technique is the significant drawback that limits throughput.

Table 1.1: Comparison of different techniques for the heterogeneous integration of III-V to SOI (Based on [50]).

Key metrics	Integration techniques			
	Wafer/Die Bonding	Flip-Chip	Epitaxial Growth	MTP
Integration Density	● ●	●	● ● ●	● ● ●
III-V Usage	● ●	● ●	● ● ● ●	● ● ●
Alignment Accuracy	● ● ●	● ●	● ● ●	● ●
Throughput	● ● ●	●	● ● ●	● ● ●
Cost	● ●	● ● ●	●	●
Technology Maturity	Mature	Mature	R&D	R&D
● - Low, ● ● - Medium, ● ● ● - High, ● ● ● ● - Very High				

Although still in an early stage of maturity, MTP offers parallel integration of small III-V coupons with less than $1\ \mu\text{m}$ lateral misalignment. It can be applied to a wide range of material systems and feature sizes with very efficient material usage. Its high-throughput potential for wafer-scale integration of PICs and EICs at low cost makes it a promising technique for ultracompact integration.

This strategy provides the flexibility to realise light coupling into receiving waveguides through different coupling mechanisms such as edge-coupling and evanescent coupling. In this work, different edge coupling configurations on three silicon photonics platforms (see section 3.2) are investigated. In addition, MTP allows the integration of a thin device layer (typically $< 5\ \mu\text{m}$) with a reduced footprint ($65\ \mu\text{m}$ wide and $< 2.4\ \text{mm}$ long in this work) with efficient consumption of III-V materials. Improved heat dissipation from the laser to the Si substrate can be achieved by designing the edge-coupling configuration in such a way that the laser coupons to be printed are closer to the Si substrate within the trenches on the SOI. In addition, the strategy offers integration freedom over SOI by exploiting the advantages and flexibility of etch facet laser technology. In particular, fully prefabricated and tested QD lasers allow micro-assembly of known devices on SOI.

1.4 Quantum Dots

Currently, most commercial photonic integrated circuits (PICs) use quantum wells (QWs) as the gain medium. However, the high thermal sensitivity of QW-based devices, which leads to significant performance degradation, remains an obstacle in datacom applications. Over the last two decades, considerable effort has been devoted to the growth and realisation of high-efficiency QD devices that can operate at high temperatures and their integration on silicon photonics platforms. The QD-based

lasers can be considered as a very attractive candidate for the next generation of optoelectronic devices, even replacing conventional QW-based lasers in certain applications. In addition, the suitability of high-quality QDs grown on a GaAs substrate, which has a wafer size larger than InP, can be considered as another advantage in terms of cost.

The concept of QD lasers was first proposed by Arakawa and Sakaki in 1982 [54]. The important discovery of molecular beam epitaxy (MBE) growth [55] allowed the development of self-assembled InAs QDs on GaAs substrates. Consequently, the first QD lasers emitting at $1\ \mu\text{m}$ were realised in 1994, a decade after the first concept [56, 57]. A few years later, the first QDs lasers operating at room temperature were demonstrated at the O-band emission wavelength, $1310\ \text{nm}$, [58]. Recently, these lasers exhibit significant performance improvements over their quantum well (QW) counterparts.

QD lasers have attracted significant attention due to their superior properties, including

- Low bias currents [59].
- Remarkable insensitivity to temperature [60].
- Reduced susceptibility to crystalline defects [61].
- Improved stability against optical feedback [62].

These desirable properties of QD laser are attributed to the three-dimensional (3D) carrier confinement, provided by the band offsets between the narrow bandgap QD and the surrounding materials, results in a quantised line shape of the density of states distribution. The density of states for different quantum structures is shown in Fig. 1.7(a). This differs from the step-like density of states characteristic of quantum wells (QWs). The spatial quantisation leads to a significant density of states in a narrow energy range, which results in a high gain of the material under optical or electrical pumping of the devices. In theory, this effect should lead to a lower threshold current density and reduced influenced of temperature in the QD-based lasers when compared to a bulk or a quantum wells counterparts.

The energy levels of a QD are influenced by the dot size and the height of the potential barrier. The delta function-like density of states is for a single quantum dot (QD) emitter. In practice, a QD active region contains a large number of individual dots with inhomogeneous distributions of dot size [63], strain profiles, and compositional fluctuations due to the randomness of self-assembled growth, therefore the density of states deviates from the ideal delta function profile. These factors lead to an inhomogeneous broadening, (ΔE) , of the optical properties within a dot ensemble. This broadening creates a quasi-band of states representing the weighted

superposition of the discrete states of individual dots, as shown in Fig. 1.7(b). Fortunately, the energy spacing between the principal quantum states is often significantly larger than that of the inhomogeneous broadening, preserving the quantized separation. Given that the quantized separation of the density of states is preserved, quantum dot (QD) lasers exhibit greater tolerance to temperature-induced broadening and are less sensitive to temperature variations. The inhomogeneous broadening also leads a broader gain spectrum and can be advantageous for applications that requires a broad bandwidth such as optical semiconductor amplifiers (OSA), tunable lasers, and mode-locked lasers. In addition, the thin wetting layer required for most QD material systems grown by the Stranski-Krastanov technique [64] connects all the dots in a layer. Thus, a more realistic density of states of a quantum dot structure can be represented as shown in Fig. 1.7(c).

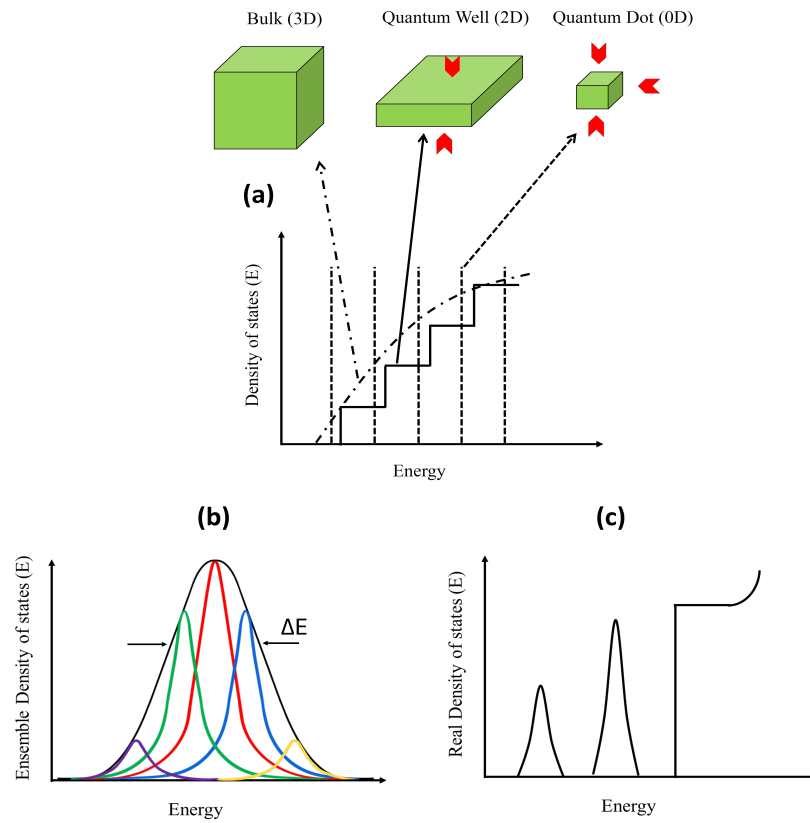


Figure 1.7: (a) Electronic density of states (DOS) of a semiconductor structures as a function of dimensionality; bulk, quantum well and quantum dot materials. (b) Schematic illustration of inhomogeneous broadening for a quantum dot state. (c) A schematic of the density of states of a QD structure considering inhomogeneous broadening, the wetting layers and excited state. (Based on [65])

InAs-based QDs can be grown on both GaAs and InP substrates by self-assembled QDs grown using the Stranski-Krastanov mode. Today, both GaAs and InP are well-developed and mature material platforms for applications including VCSELs for 3D sensing, datacom and telecom [66]. InAs QD growth on InP is more challenging than that on GaAs. The formation of self-assembled quantum dashes (QDash) is a

common phenomenon on InP due to the small lattice mismatch coefficient (3%) between InAs and InP, which leads to asymmetric adatom diffusion lengths on the growth surface, resulting in QDs that are elongated [67]. 1310 nm lasers are mostly grown on GaAs substrate due to its higher lattice mismatch with the InAs QD (~ 7%). Therefore, GaAs does not require the mismatch work that InP does. Another advantage is that GaAs is a mature platform with a wafer size larger than that of InP. Recent development shows that Si-based InAs QD lasers on larger wafers (i.e. 300 mm) would further reduce cost per die and paving for future low-cost PICs with on-chip highly efficient light source [68].

1.4.1 Quantum Dots Lasers - state of the art

In theory, QD lasers should outperform both bulk and quantum well (QW) lasers due to their superior properties including material gain, lower threshold current, narrower linewidth enhancement factor, lower wavelength chirp, lower intensity noise and increased resistance to optical feedback. However, it took many years for the QD laser to surpass the performance of the state-of-the-art QW laser. Typically QD lasers require a longer cavity length ($> 1\text{ mm}$ in this work) for stable ground-state emission due to limited gain. The impact of cavity length on device performance will be discussed in more detail in chapter-5.

Multiple ways of integrating InAs/GaAs quantum dot lasers with silicon photonic circuits have already been demonstrated [69–74]. Typical integration schemes include wafer bonding, heteroepitaxial growth, and recently MTP.

To date, the wafer or die bonding approach is well established with a mature technology and is being adopted for QW based devices in industry by Intel [81]. InAs/GaAs QD based lasers can also be realized using wafer bonding on SOI. The first InAs/GaAs QD laser based on this technology was reported by Tanabe et. al. from Tokyo University in 2012. The Fabry-Perot lasers are fabricated on patterned Si rib structures following the direct GaAs/Si wafer bonding and the GaAs substrate removal. The cleaved facet lasers showed a CW operation at 1.28 μm with a threshold current density of 480 A/cm^2 at room temperature [75]. A high temperature operation up to 100°C is reported with threshold current densities as low as 271 A/cm^2 [69]. In 2018, the first single mode heterogeneously integrated InAs/GaAs QD laser on Si photonics waveguide circuit was reported. The adhesive bonded InAs/GaAs epi material is demonstrated on the SOI with a single mode lasing around 1300 nm. The lasers showed a side-mode suppression ratio greater than 40 dB with a threshold current densities of 205 A/cm^2 and CW mode lasing up to 100°C [70].

Epitaxially grown III-V lasers on Si substrates have been considered as the ultimate approach to realise a cheaper PIC solution. However, the large material dissimilarities and the difference in thermal expansion coefficient between Si and III-V materials

(such as InP and GaAs) lead to the formation of various defects in the resulting III-V layer, such as threading dislocations, thermal cracks, and antiphase domains [71, 76, 77]. These defects cause the III-V materials to suffer from increased non-radiative recombination in their active regions, leading to low performance lasers with shorter lifetime [72]. In addition, III-V QD materials grown on Si have shown a high tolerance to defects, which is promising for direct growth of III-V on Si. The effect of defects on QW and QD active layer materials is illustrated in Fig. 1.8.

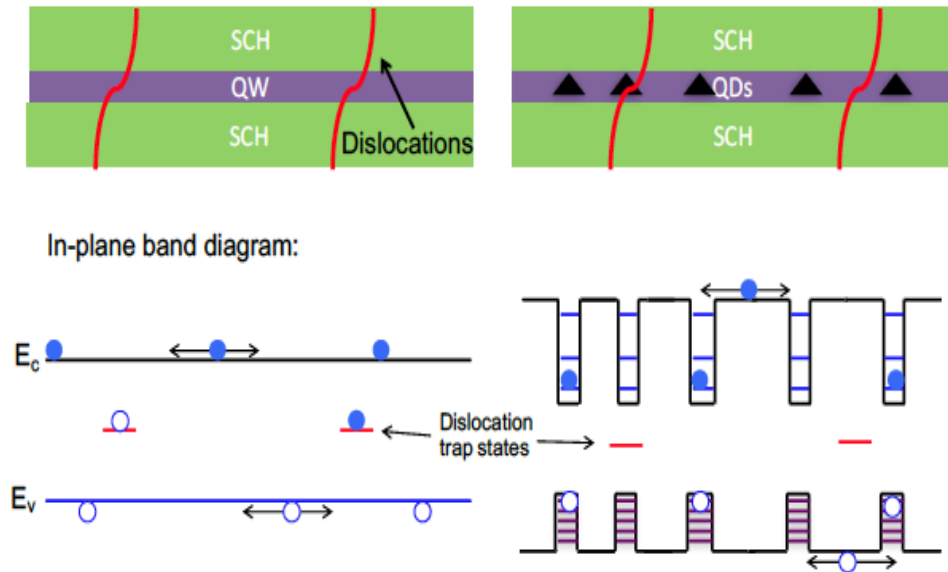


Figure 1.8: Schematic illustration of the impact of threading dislocation on QWs and QDs. The three dimensional confinement of carriers in QD significantly reduces carrier migration to defect states, unlike the quantum well [78].

The epitaxial growth of the GaAs III-V material on a Ge on Si substrate has been demonstrated, taking advantage of the small lattice constant of Ge [77, 79]. In 2012, Lee et al. reported the first electrically pumped monolithic InAs/GaAs quantum dot laser on Si with CW operation at $1.3 \mu\text{m}$ up to 30°C using this approach [77]. The lasers showed a threshold current density of 163 A/cm^2 . Then in 2014, cleaved-facet ridge waveguide lasers showed CW lasing up to 119°C using the same technique by UCSB researchers [71]. Because Ge prevents light coupling into the Si waveguide as a result of its absorption at telecom wavelengths, direct growth of III-V on Si is required to achieve efficient light coupling. InAs/GaAs QD lasers grown on Si are demonstrated using different techniques including the GaP buffer layer instead of Ge [80] and the $4\text{-}6^\circ$ off-cut towards the [011] plane [81, 82].

In 2020, electrically pumped CW InAs/GaAs QD lasers grown directly on Si substrate without using a Ge or GaP buffer layer are demonstrated with a threshold current density of 173 A/cm^2 and lasing temperature of 80°C . The III-V QD material is grown on a Si substrate with very small off-cut using a combination of metalorganic chemical vapor deposition (MOCVD) and molecular-beam epitaxy (MBE) techniques [83].

Light coupling into the Si waveguide is a major challenge in the lasers based on this technique. More recently, edge-coupled InAs/GaAs QD lasers grown on trench SOI with V grooves were studied by Wie et al. [84]. A maximum waveguide coupled power of 6.8 *mW* and CW lasing of up to 85 °C are obtained.

InAs/GaAs QD lasers grown on native GaAs substrate are also integrated on SOI by micro-transfer printing technique. Prefabricated O-band QD on Si DFB lasers is obtained with waveguide coupled powers above 0.5 *mW*. The lasers demonstrated single-mode operation at 1300 *nm* with a side-mode suppression ratio (SMSR) of 48 *dB*, as reported by Zhang in 2022 [73]. In a follow-up study by the same author, the waveguide-coupled power was increased to 3.5 *mW* [85]. The same group also reported QD SOAs transfer-printed on imec's iSiPP50G platform with 6.5 *dB* on-chip gain at 110 *mA* drive current [86]. Recently, the first hybrid QD distributed Bragg reflector (DBR) laser has been demonstrated with a threshold current of 47 *mA* and stable operation up to 80°C under pulse mode operation [74]. In this thesis, the first transfer-printable edge-emitting InAs/GaAs QD lasers up to 2.4 *mm* in length are heterogeneously integrated on different SOI platforms through MTP [87]. The etched-facet QD lasers exhibit a threshold current of 15 *mA* and deliver more than 32 *mW* at 70°C under CW operation. A waveguide-coupled power of 7.5 *mW* through edge coupling is achieved at room temperature.

Key metrics	imec-[73]	imec-[85]	Tokyo Uni.-[74]	This Work
Operation Mode	CW	CW	Pulse	CW
Coupling Schemes	Evanescent	Evanescent	Evanescent	Butt
Threshold Current Density ($J_{th}(A/cm^2)$)	1266	2000	587	400
Power (<i>mW</i>)	0.5	3.5	2.5	7.5
Series Resistance (Ω)	5	3	12.6	8
Coupon Size (<i>mm</i> X μ m)	1.7 X 40	2.16 X 45	1.6 X 147	2.4 X 80
Emission(<i>nm</i>) & SMRS (<i>dB</i>)	1300 & 48	1300 & 45	1250 & 14	1310 & FP

Table 1.2: Performance comparison of transfer-printed InAs/GaAs QD based laser

1.5 Research Objectives

The lack of an integrated light source on silicon photonics circuits is the driving force behind this work. This thesis contributes to the development of a releasable O-band QD laser and its heterogeneous integration to different silicon photonics platforms using micro-transfer printing. The laser is edge-coupled to the waveguide in different configurations. This research includes the following key aspects.

- Realisation of the first butt-coupled transfer-printable InAs/GaAs QD laser coupons/devices. The work includes the design of epitaxial layer stacks and process flow development for the fabrication of the QD laser coupons on the native GaAs wafer.
- Development of hydrochloric acid (HCl) based release etch process for AlGaAs sacrificial layer for undercut of the devices from the native substrate. Tether system design and coupon stress management are also performed.
- Investigation of high reflective (HR) mirrors based on a metal-dielectric reflector and multimode interference (MMI) coupler.
- Demonstration of high yield transfer printing of the QD lasers onto three silicon photonics platforms including 220 nm SOI, 3 μ m SOI and 300 nm SiN.
- Comprehensive characterisation of different edge coupler configurations based on these waveguiding platforms. The aim was to achieve high performance edge coupling to the receiving waveguides with relaxed alignment tolerance.
- Development of transfer-printable laterally coupled (LC) distributed feedback (DFB) lasers with single-mode operation around 1310 nm.

The research was supported by the CALADAN Project in collaboration with various partners, including Innolume, which provided QD material, imec for the fabrication of 300 nm SOI, EV Group for the adhesive spray coating and X-Celeprint for technical support in transfer printing development.

1.6 Thesis Outline

This work finds its main motivation in the development and integration of a InAs/GaAs quantum dot (QD)-based edge-emitting light source for silicon photonics. The structure of this work is summarised in 7 chapters, including the introduction and conclusion chapters. Following the introduction, the descriptions of the QD epilayer stacks and process developments for QD laser fabrication are presented. Then we investigate different waveguide platforms in which transfer-printable QD etched-facet lasers are to be integrated by micro-transfer printing. Next, transfer-printing of lasers on these platforms and related process developments are discussed. The following two chapters discuss the performance of developed lasers on their native GaAs substrate and after being transferred to the host substrate. These aspects will be discussed in more detail in the following chapters.

✓ **Chapter 1:** The first part of this chapter focusses on the motivations behind this work. It starts with the high demand for data traffic in data centres and the potential of PICs for high-bandwidth optical transceivers. Then, the lack of an integrated light source on PICs is explained together with the approaches for heterogeneous

integration. A brief history of QD lasers and a literature review on InAs/GaAs QDs are presented. The strategy selected in this work for the integration of a QD laser to different photonics platforms is described in the final section.

✓ **Chapter 2:** reports the description of the general laser layout and fabrication of the QD lasers. The III-V epitaxial layer structures used for transfer printable GaAs QD devices, and the fabrication flow of the etched facet laser diodes and the process optimizations are described. In addition to the design, technological issues including etched-facets, metal contacts, and reflective mirror are reported.

✓ **Chapter 3:** starts with a discussion on different light coupling approaches from a laser to waveguide. The design, simulation and fabrication of different edge-coupling configuration strategies such as 220 nm SOI, 3 μm SOI and 300 nm SiN with SU-8 polymer waveguides are presented. Next, the studied configurations are compared with each other based on their advantages and disadvantages.

✓ **Chapter 4:** In this chapter, micro-transfer printing of QD laser is discussed. The challenges and proposed solutions during coupon release etch are discussed. The process development on targets with and without adhesive layers and the adhesion enhancement methods are described. Finally, a patterned adhesive process developed for recessed targets is described. Integration of QD lasers onto targets with different adhesive layers is reported.

✓ **Chapter 5:** In this chapter, the electro-optical and the thermal characterisation of the QD ridge lasers are presented. The iterative development of QD lasers is presented by the characterisation of three generations of lasers. The performance of devices before and after transfer printing is investigated to evaluate the effects of transfer printing on device performance. The thermal characteristic of the devices is also investigated.

✓ **Chapter 6:** In this chapter, the analysis of integrated InAs/GaAs QD lasers onto different waveguide platforms is presented. The performance of the QD lasers on each platform is discussed on the basis of the measured waveguide coupled power, misalignment, and coupling efficiencies. In the end, the challenges and potential solutions to improve the coupling performance are discussed.

✓ **Chapter 7:** This section outlines the key findings of this research, highlighting its technological significance. Future developments and potential applications of this technology are discussed.

✓ **Appendix-A:** describes the main epitaxial structures used in this study for quantum dot (QD) lasers. It outlines the difference between different laser structures along with the reasons. It also provides detailed fabrication processes for the fabrication of transfer-printable GaAs Fabry-Perot laser coupons, both with and without ledge. The ledge-less laser coupon is designed for perfect alignment of the emitting facet of the

laser to the receiving waveguide in longitudinal direction.

✓ **Appendix-B:** provides an overview of the patternable adhesive process (using InterVia) developed to remove excess material that interferes with light coupling from the laser to the waveguide, particularly towards the recess sidewall. The appendix presents experiments and process parameters carried out on bare silicon and recessed silicon-on-insulator (SOI).

✓ **Appendix-C:** presents developments in laterally coupled distributed feedback QD lasers. The fabrication and characterisation of laterally coupled InAs/GaAs quantum dot DFB lasers are discussed. The lessons learnt from the test devices and suggestions for improvement are discussed in detail.

✓ **Appendix-D:** provides the Python code that controls the instruments used during device characterisation.

Chapter 2

Fabrication of Edge-Emitting QD Lasers

This chapter presents the process developed for the fabrication of transfer-printable edge-emitting InAs/GaAs QD lasers. This development includes device fabrication related processes such as the dry etching process for facet mirrors, high-reflectivity mirrors, and ledge-less coupons, and transfer printing related processes such as tether system design and stress management. The chapter begins with the introduction of III-V epilayer stacks used for laser fabrication. The design of epilayer stacks is discussed, focusing on the layers specifically required for transfer printing and edge coupling. Next, the device layout and the different laser coupons with different cavity lengths, ridge widths, and rear mirror designs are explained. A brief description of the standard process flow for transfer-printable QD laser diodes is presented. All process development activities are carried out in the clean-room at Tyndall National Institute.

2.1 Epitaxial Structure

In a III-V epilayer stack for transfer-printable devices, additional layers may be required to facilitate the release and transfer process. Typically, in addition to the active and cladding layers, a special layer, called a sacrificial layer or release layer, needs to be included in the layer stacks to enable III-V device layer separation from the substrate. The GaAs-based quantum dot layer stacks used in this work were grown by INNOLUME GmbH [88] in a molecular beam epitaxy (MBE) reactor on 3 inch n-doped GaAs substrates. The epitaxial layer stack was designed in a collaboration with INNOLUME to optimise the device performance and sacrificial layer for undercut etch. The composition of transfer-printable epitaxial layers is presented in table-2.1. The detailed data of the laser structures grown are given in Appendix-A.

The growth begins with a 200 nm GaAs buffer layer that ensures surface smoothness

Order	Layer	Mole Fraction (x)	Thickness (nm)	Doping Type
15	p-GaAs contact		50	P
14	$Al_xGa_{1-x}As$	0.4 - 0	10	P
13	$Al_xGa_{1-x}As$	0.4	1100	P
12	$Al_xGa_{1-x}As$	0 - 0.4	10	P
11 14X	GaAs barrier		-	-
10 14X	InGaAs		-	-
9 14X	InAs		-	-
8	GaAs		-	-
7	GaAs		300	N
6	$Al_xGa_{1-x}As$	0.3 - 0	10	N
5	$Al_xGa_{1-x}As$	0.3	1140	N
4	$Al_xGa_{1-x}As$	0 - 0.3	10	N
3	n-GaAs contact		500	N
2	$Al_xGa_{1-x}As$ sacrificial	0.95 / 0.93	500	N
1	GaAs		200	N
0	GaAs Substrate	N+ GaAs 3 inch		

Table 2.1: Epitaxial layer stack of the InAs/GaAs QD laser.

on top of an n-doped GaAs substrate wafer. Then a 500 nm thick $\text{Al}_{0.95}\text{Ga}_{0.05}\text{As}$ layer, which acts as the sacrificial release layer, is grown. The Al content is set to 0.93 in the final epilayer structure. The release layer is n-type doped to allow device characterisation without release on the native substrate prior to undercut etching. This is critical to assess the effect of release and transfer printing on device performance. This is followed by a 500 nm heavily doped GaAs n-contact layer, 1.42 μm n-type $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ lower cladding. The active region is composed of a stack of 14 InAs/GaAs QD layers lying within $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$ layers. It should be noted that the number of QD layers in the first-generation was 12, but this was increased to 14 in the later epilayers. The QD layers are separated by a p-doped GaAs spacer to enhance the thermal stability of the lasers. The epitaxial structure is completed with a 1.2 μm p-doped $\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$ upper cladding and a 50 nm heavily doped GaAs p-contact layer. The growth thicknesses need to be accurately controlled to enable the alignment in the vertical direction between the lasers to waveguide. A number of epilayers have been grown throughout the project to optimise device performance, and the main differences are tabulated in table-2.2.

	Laser Structure		
Key metrics	Epitaxy-A	Epitaxy-B	Epitaxy-C
p-cladding	720 nm $\text{Al}_{0.8}\text{Ga}_{0.2}\text{As}$	1170 nm $\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$	1170 nm $\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$
number of QD layers	12	14	14
GaAs buffer thickness	-	300 nm	250 nm
n-cladding	1220 nm $\text{Al}_{0.8}\text{Ga}_{0.2}\text{As}$	1160 nm $\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$	980 nm $\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$
n-GaAs thickness	-	500 nm	600 nm
Sacrificial layer	-	500 nm $\text{Al}_{0.95}\text{Ga}_{0.05}\text{As}$	500 nm $\text{Al}_{0.93}\text{Ga}_{0.07}\text{As}$

Table 2.2: Summary of the main differences between the laser epitaxial layers used in this thesis.

Weak hole confinement leads to performance degradation at high operating temperatures, despite the superior theoretical performance of quantum dot (QD) lasers. Introducing p-doping into the GaAs barrier layer is a well-known technique to provide more holes in the active QD region, thereby improving the thermal performance and overall efficiency of QD lasers [89]. In addition, p-doping helps to provide a high built-in hole concentration, allowing a shorter laser cavity length. This in turn mitigates gain saturation effects, allowing ground state (GS) lasing to be maintained in shorter cavities even at higher current densities [90, 91].

A 1.2 μm deep ridge waveguide is dry etched into the p-clad layer, providing lateral confinement of the laser modes. Vertically, the laser modes are confined by the refractive index difference between the active region and the cladding layers. The

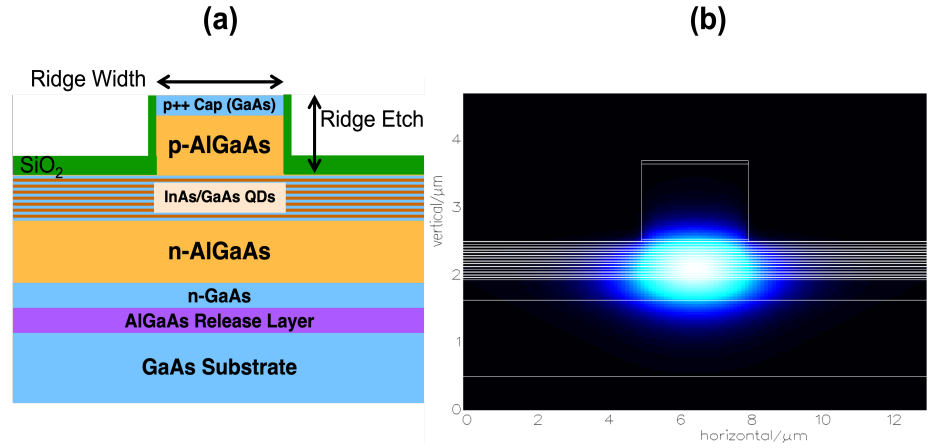


Figure 2.1: (a) Ridge waveguide structure used for simulation of the laser mode profile. (b) Mode profile of the fundamental transverse electric (TE) optical mode for 3 μm wide ridge laser at 1310 nm.

ridge waveguide has a width of 2.5 and 3.0 μm . The optical lithography resolution of 1.5 μm plus 1 μm margin determines the minimum ridge width. The simulated mode field diameters (MFD) of the TE mode are 3.6 μm and 1 μm in the lateral and vertical directions, respectively. In addition, the thickness of the AlGaAs cladding layers must be adjusted so that the optical mode is vertically aligned with the receiving waveguide and does not interfere with the GaAs contact layer or substrate.

2.2 General Laser Device Layout

A robust and repeatable fabrication process is developed with a corresponding set of lithographic masks. Dense arrays of Fabry-Perot (FP) lasers with more than 1000 devices per chip (quarter piece of a 3" wafer) with fixed pitch in the Y direction are fabricated on the native GaAs substrate. QD laser coupons are designed to be 65 μm and 80 μm wide and up to 2.4 mm in length. The dimensions of the coupons are determined by considering recesses on the SiPh target chip where the devices will eventually be integrated on a 300 mm SOI wafer. The recess on the SOI wafer will accommodate the lasers and facilitate edge-coupling of the light into the Si waveguides. The mask contains a variety of lasers with different ridge widths and cavity lengths. Both mirrors of the laser are formed by an ICP dry etched facets. The output facet has a dielectric protective coating. Two types of rear mirror are investigated in the lasers including a metal-coated high-reflection (HR) mirror and a multimode interference reflector (MIR) based HR mirror.

In addition to the transfer-printable laser coupons, reference lasers with etched facets and cleaved facets are included in the design for comparison of device performance on its native substrate and on the hosting target after transfer-printing. The only difference between these lasers and transfer-printable coupon devices is the n-metal contact configuration. Transfer-printable devices have top p-metal and n-metal

contacts. However, reference lasers have their n-metal contact on back-side of the chip after thinning down to 120 μm .

2.2.1 Mask Layout

Two mask sets have been developed for transfer-printable QD laser devices. The laser coupons are oriented parallel to the major flat for simplicity and better utilisation of the material. It should be noted that the etch rate for undercutting the sacrificial layer is another parameter to consider when deciding the orientation of the devices on the wafer. Further discussion of the dependence of the etch rate on the crystallographic orientation is discussed in chapter-4 under the sacrificial etch section (4.1). Coupons of the same length are grouped in the same columns with a Y-axis spacing of 160 μm . This facilitates the transfer printing process by allowing for rapid alignment of the stamp to the coupon using automation. The vertical spacing can be determined by considering the spacing in the target to allow parallel integration of coupons. Figure 2.2 shows the complete mask layout. All transferable laser coupons have an etch facet defined in an ICP dry etch process. The physical length of the coupons ranges from 1.5 mm to 2.4 mm with a cavity length corresponding to 1 mm to 2 mm .

In addition, the mask contains a number of other structures such as alignment markers, in-situ etch monitor sites, transmission line measurement (TLM) pads, and dummy circles and coupons. These components allow the devices to be checked after each of the critical process steps such as dry etch, metallisation and release etch. Alignment markers, consisting of vernier rectangles, are used to accurately align the current step with the previous step. Monitoring the etch depth in III-V epilayer stacks is critical to achieving high performance lasers. The square (a few 100 μm wide) in-situ etch monitors are used to stop at the correct layers during the dry etch process. TLM pads are used to check contact resistance and sheet resistance for the n and p contacts. The distance between the contacts pads varies from 8 to 200 μm . Circular and rectangular dummy coupons are used to assess the progress of the etchant flow during release etching.

Reference lasers of the same design with transfer-printable devices are included in the same mask. In addition to etched facet lasers, several mm long laser bars are contained that will be used as cleaved facet lasers of various lengths. These devices will allow performance evaluation of the cleaved and transfer printed lasers.

2.3 QD Laser Fabrication Process Flow

The fabrication process is shown schematically in Fig. 2.3, with a top view and a cross section at various stages. Edge-emitting 1310 nm QD lasers are manufactured using a 9-step lithography process. The reference lasers are fabricated on the same chips.

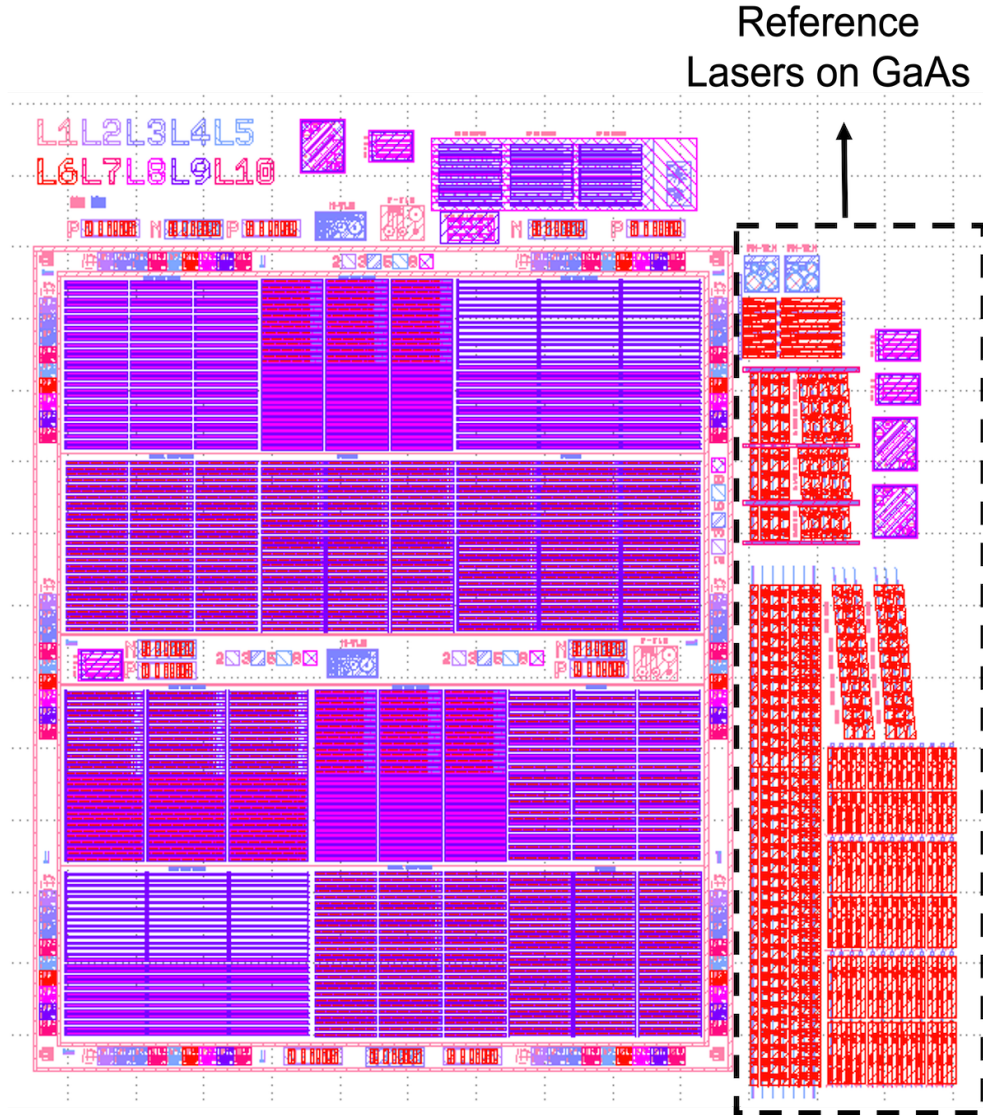


Figure 2.2: Full mask layout for Fabry-Perot laser coupons. The reference lasers are fabricated on the same chip with transfer-printable devices.

They go through the same steps as coupon devices but are protected during the last two steps required for transfer-printable devices. The definition of the laser devices starts with a Ti/Pt/Au p-metal deposition. The deposition of p-metal prior to any processing on the chip enables an ohmic contact. In this step, alignment markers, device labels, and TLM pads are also defined. The ridge waveguides are then formed in the p-clad layer using a $1.2\ \mu\text{m}$ deep inductively coupled plasma (ICP) dry etch with a PECVD SiO_2 hard mask. The ridge waveguides are $2.5\ \mu\text{m}$ and $3.0\ \mu\text{m}$. The next step is the definition of the emitting and rear facets through dry-etch. Smooth and vertical facets are defined by an ICP etch process using $\text{BCl}_3\text{-Cl}_2\text{-N}_2\text{-Ar}$ chemistry together with the recess to the n-contact. The development of the etch recipe and process optimisation is discussed in the following section. The rear facets of the lasers including the MIR mirrors are also defined in the same etch step. The facet etch stops

at the n-GaAs layer with 50-100 nm overetch. Stopping the etch before reaching the n-GaAs layer or etching too deep into n-GaAs would result in high resistance. Then the facets and coupon sidewalls are passivated with a PECVD SiN or SiO₂ to protect the facets and other epitaxial layers during subsequent fabrication steps and release etch. A lift-off process is used to open the dielectric mask and deposit an Au/Ge/Au/Ni/Au metal stack on the n-GaAs layer in the etched n-metal contact well. After the dielectric is opened on the p-contact, Ti/Au bonding pads are deposited on the anode and cathode for electrical probing. The resulting etched-facet laser coupons have the electrical top contact pads for direct device probing. To accommodate these pads on top of the devices, the coupons must be a few 100 μm longer than the laser cavity length. A final ICP dry etch is required to remove the remaining n-type GaAs layer and sacrificial layer. The coupon boundaries are also defined in this step by etching 100-200 nm into the GaAs substrate using a resist mask. It is important to avoid over-etching too deeply into the substrate to minimise the step-height that the tethers have to climb. This process forms 2.5 μm wide ledge around the coupon. Another process was developed in which the ledge is removed from the front of the coupon to address misalignment issues in integration and coupling. This is achieved by means of a self-aligned process in which the thickness of the dielectric on the coupon is adjusted. The ledges on the coupons and ledge-less front facet is shown in Fig. 2.3(e). The final step before release etching is the definition of the anchor system (also called tethers) that will keep the coupons in position and suspended during and after the undercut process.

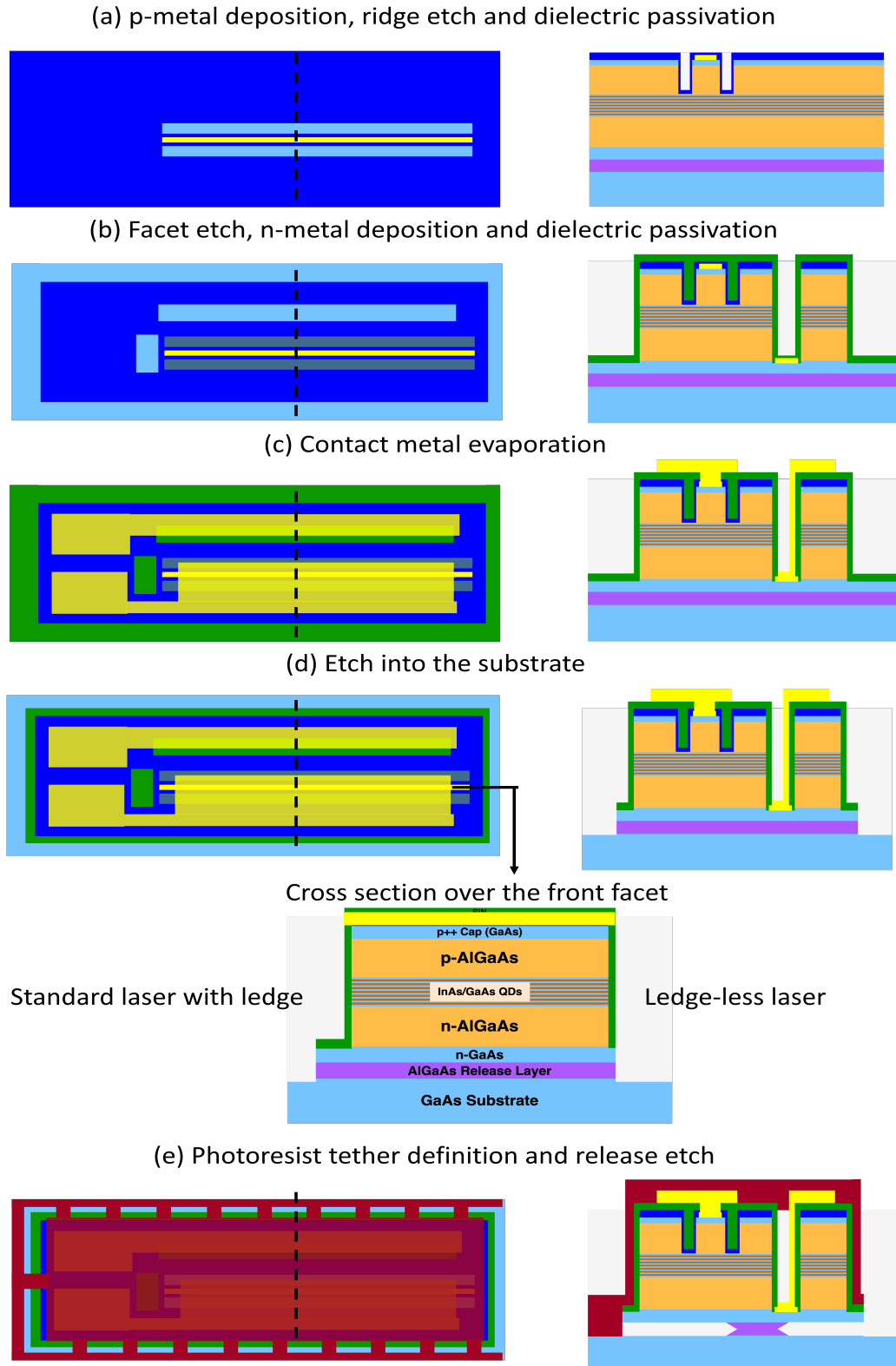


Figure 2.3: Process flow for the transfer-printable QD lasers showing top view and cross-sections view (over dashed-line) at the various processing steps. The resulting laser coupons are 65 or 80 μm wide and up to 2.4 mm long. At step (d) the extension around the coupon (ledge) is removed from the front facet of coupon in the final-generation. The front-facet profile for a standard (left) and ledge-less (right) laser coupon is shown. Finally, the photo-resist based tethers are defined in step (e).

Tethers are defined using a 3-4 μm thick photo-resist in this work. More details on tether design are given later in this chapter. A schematic of the final laser coupon is given in Fig. 2.4.

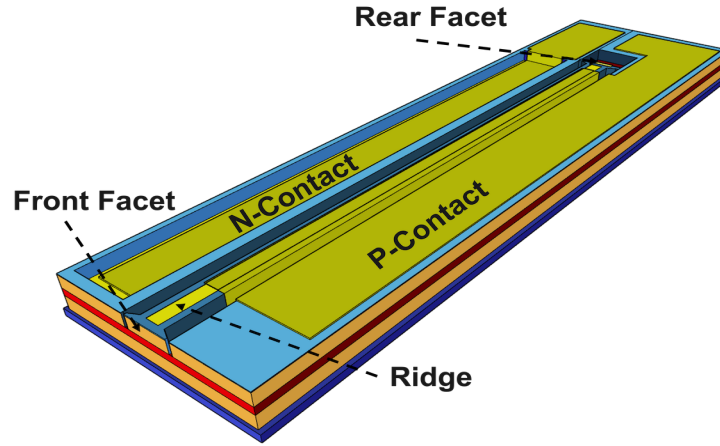


Figure 2.4: A schematic of the final laser coupon geometry. The laser has its p and n contacts on the top of the device.

2.3.1 Facet Etch Development

Throughout the development of transfer-printable InAs/GaAs QD lasers, several optimisations are investigated in different process steps to improve the device performance. These include the development of the ICP dry etch recipe and associated fabrication process, optimisation of the device resistance with p- and n-metal top contacts, improvement of the highly reflective mirror, stress management, tether definition process, and release etch. In addition, the developed process is adapted to a ledge-less coupon process. Developments related to laser fabrication are discussed in this chapter. Those related to laser micro-transfer printing and target wafer are mainly presented in chapter-4.

Transfer-printable lasers require an etched facet mirror on both the front and back facets. A Fabry-Perot resonator is formed between two etched sidewall facets. A particular challenge is the development of a smooth and vertical profile facet to realise lasers with lower mirror loss and threshold current. Dry etching recipes for inductively coupled plasma reactive ion etching (ICP-RIE) were first developed to achieve a vertical facet with a smooth surface profile close to the cleaved facet. An etch recipe optimisation study is performed considering plasma parameters such as gas mixtures, gas flow rate, plate power, temperature, and chamber pressure. In addition, since the preparation of the samples for dry etching has a huge effect on the results, various tests and optimisations are carried out to develop a fabrication process that gives the best facet profile. Two vertical profile photo-resists including AZ5214E [92] and SPR220-4.5 [93] are investigated to pattern the dielectric hard masks. During development, different dielectric layers such as PECVD SiO_2 and SiN , sputter SiO_2

have been evaluated. The resulting etched facets are evaluated based on the facet profile in terms of repeatability, smoothness and verticality, etch rate, and selectivity.

The experiments are carried out in an Oxford ICP etcher (PlasmaPro 100 Cobra). The gases used in this study are BCl_3 (boron trichloride)- Cl_2 (chlorine)- N_2 (nitrogen)-Ar (argon). A 15-minute cleaning procedure, consisting of a 5-minute SF_6 and a 10-minute O_2 clean, is performed at the beginning of each run to remove any residue from the reactor sidewalls of the previous user. This minimises the chance of contamination and maintains process repeatability. A 15 minute conditioning run is performed after the cleaning procedure and before the first run. The gas flow rate is varied throughout with different chamber pressures, ICP and platen power. During etching, the temperature is set at 20°C .

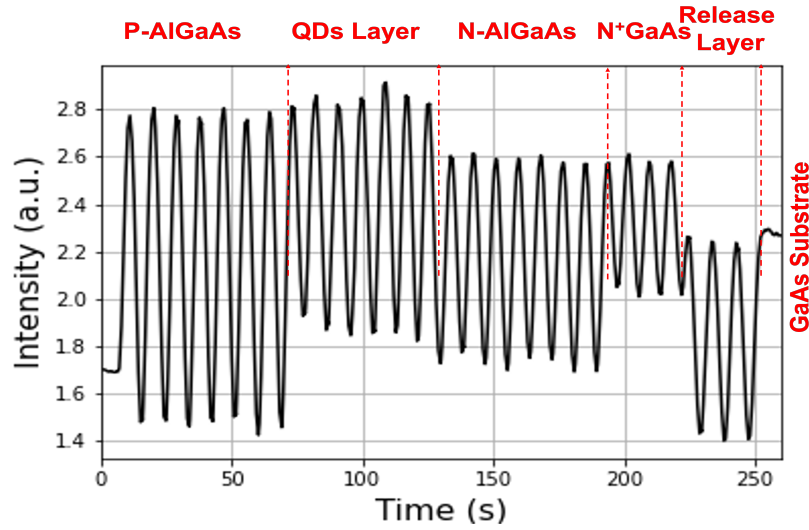


Figure 2.5: (a) The full EPD trace of the epilayer structure when all layers are etched in one step. The changes in intensity indicates the switch from one layer to next one.

The samples are loaded into the reactor on a 100 mm Si carrier wafer with a bonding oil to ensure good thermal contact. The GaAs samples with rectangular and/or T-shaped mesas are examined after dry etching using optical microscopy and scanning electron microscopy (SEM). A typical end-point detection (EPD) trace for the epitaxial layer when fully etched into the substrate is shown in Fig. 2.5. To obtain this signal, a laser (850 nm) is directed at an opening in the sample surface, and a sensor measures how much of the light bounces back. As there are a number of layers in the III-V sample, the interference of light between the surface and the layer below it produces this signal. The majority of samples are etched down to the n-contact layer or down to the substrate during the etch development process.

Several different etch recipes are studied and the typical parameters for these recipes are summarised in table-2.3. The etch results of each recipe are compared and evaluated to determine the best process. An existing recipe used in a previous tool is

taken as the base recipe for development. This recipe (R1) consists of BCl_3 and Cl_2 and showed a poor etch profile with a very rough sidewall and many grass-like features. The formation of these features is due to micromasking phenomena and can be seen in Fig. 2.6 R1. Then a previous study [94] for GaAs/AlGaAs dry etching is adapted to the ICP dry etching tool. Starting from recipe R2, the flow rates of the gases BCl_3 , Cl_2 , N_2 and Ar gases are optimised together with the chamber pressure and plate power of the recipe. After several etches, the recipe is converged to the optimum region at 2.5 *mTorr* pressure, 100 W plate power and gas flow rates of 10 *sccm*, 10 *sccm*, 4 *sccm*, 10 *sccm* for BCl_3 , Cl_2 , N_2 and Ar respectively. The recipe is then fine-tuned to achieve an acceptable etch rate and a repeatable process.

Parameters							
Recipe No	Pressure (mTorr)	BCl_3 (sccm)	Cl_2 (sccm)	N_2 (sccm)	Ar (sccm)	Power (W)	Etch rate ($\mu\text{m}/\text{min}$)
R1	5	-	20	5	-	50	NA
R2	10	5	5	4	20	50	2
R3	10	10	10	4	10	50	1.65
R4	2.5	10	10	4	5	100	1.18
R5	2.5	10	10	4	10	100	1.26
R6	2.5	10	5	4	10	100	1.2
R7	1.5	10	5	4	10	80	0.91
R8	2.0	10	10	4	10	100	1.23
R9	2.0	10	10	4	10	80	1.15

Table 2.3: Recipe parameters and the measured etch rate using SiO_2 hard-mask with AZ5214E photo-resist.

The optimisation process is completed with recipe R9. The corresponding sidewall SEM images for the samples etched using the developed recipes are shown in Fig. 2.6. In addition to the visual evaluation of the facet, the threshold current of the lasers fabricated using recipe R9 is compared to lasers with the same size cleaved facet. When a comparable threshold is obtained, the optimisation is complete. The etch profile is highly sensitive to pressure changes, but changes in Ar flow and plate power did not have a large effect on sidewall verticality. However, the material etch rate varies from 0.9 $\mu\text{m}/\text{min}$ to 1.6 $\mu\text{m}/\text{min}$ and can be tuned by controlling the platen power, pressure, and the Cl_2 flow rate.

Another important parameter is the selectivity of the solution to the dielectric hard mask. It is estimated by calculating the ratio of semiconductor etch rate to hard mask etch rate (dielectric or photo-resist) and is measured to be above 14 for the best recipe. The etch rate of the best recipe (R9) for different dielectrics and investigated photo-resists is given in table - 2.4. Given the target etch depth in the III-V epilayer and the required dielectric thickness, the selectivity value is suitable for this process.

However, the selectivity can be further tuned by changing the recipe parameters.

Material	Etch rate (nm/min)
PECVD SiO ₂	70
Sputter SiO ₂	50
PECVD Si ₃ N ₄	85
AZ5214E	<50
SPR220-4.5	<50

Table 2.4: The measured etch rate of the investigated resists and dielectric hard mask when using the best recipe (R9) in dry etching.

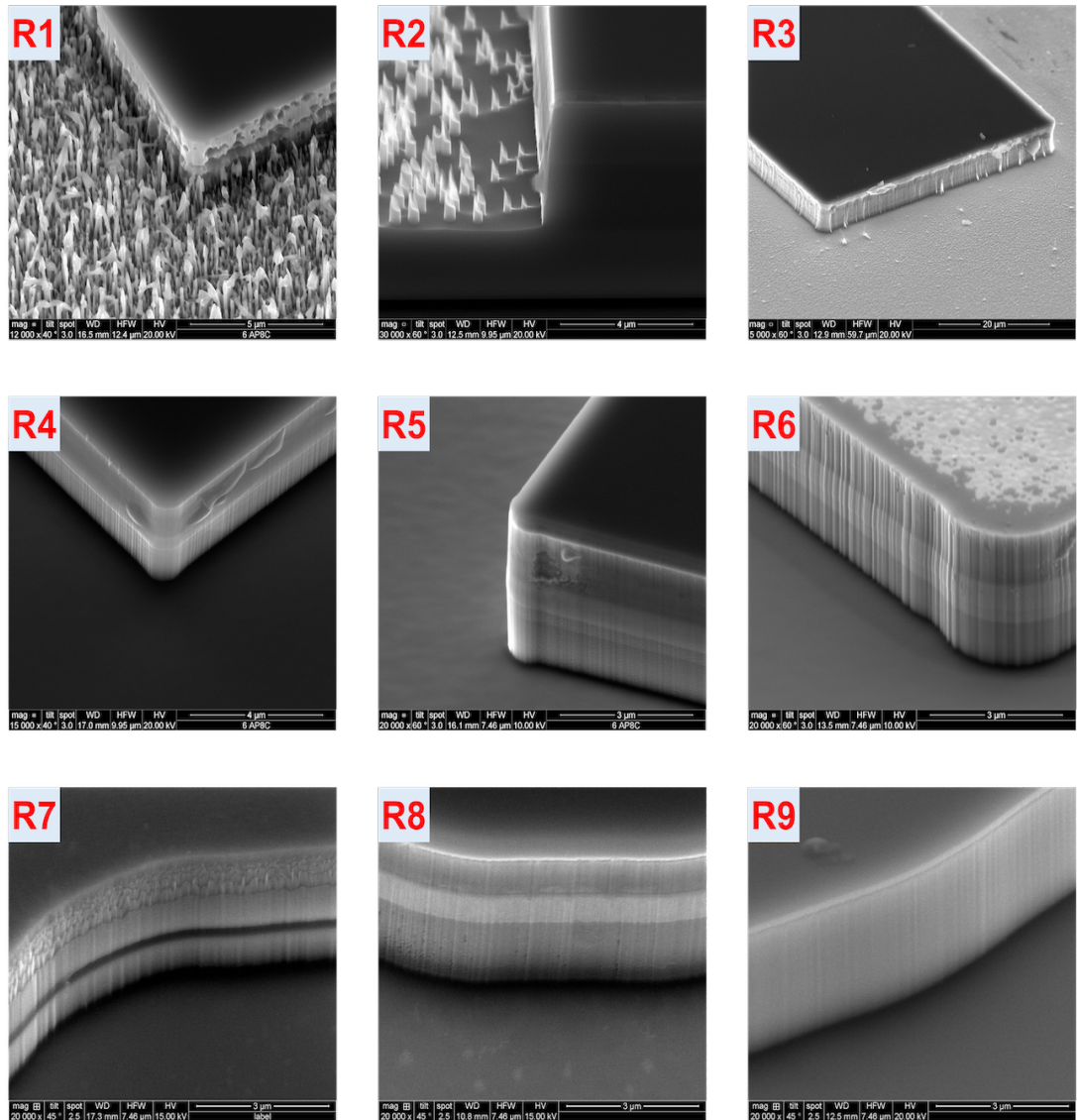


Figure 2.6: Scanning electron microscope image of facets formed by a SiO₂ hard mask patterned with an AZ5214E resist mask in vacuum contact mode. A smooth and vertical sidewall facet is achieved with optimised parameters in the dry etch recipe.

Due to the high Al content in $\text{Al}_{0.95}\text{Ga}_{0.05}$ as sacrificial layer, the formation of aluminium fluoride (AlF_3) crystals is observed when this layer is exposed during the encapsulation etch. The presence of Al and F in the energy dispersion of X-ray spectroscopy (EDX) shown in Fig. 2.7(a) and (b) confirms the presence of the AlF_3 crystal. The source of fluorine (F) is the SF_6 used during chamber cleaning. AlF_3 crystals can be avoided or minimised by an additional 30 minute O_2 plasma cleaning prior to the actual etch. In addition, these crystals can be dissolved in a few minutes with a solvent or photo-resist developer such as MF26A and MF319 containing tetramethylammonium hydroxide (TMAH). Figure 2.7(c) and (d) show the AlF_3 crystals on a sample after dry etching and their complete removal with a 3 min MF319 dip, respectively.

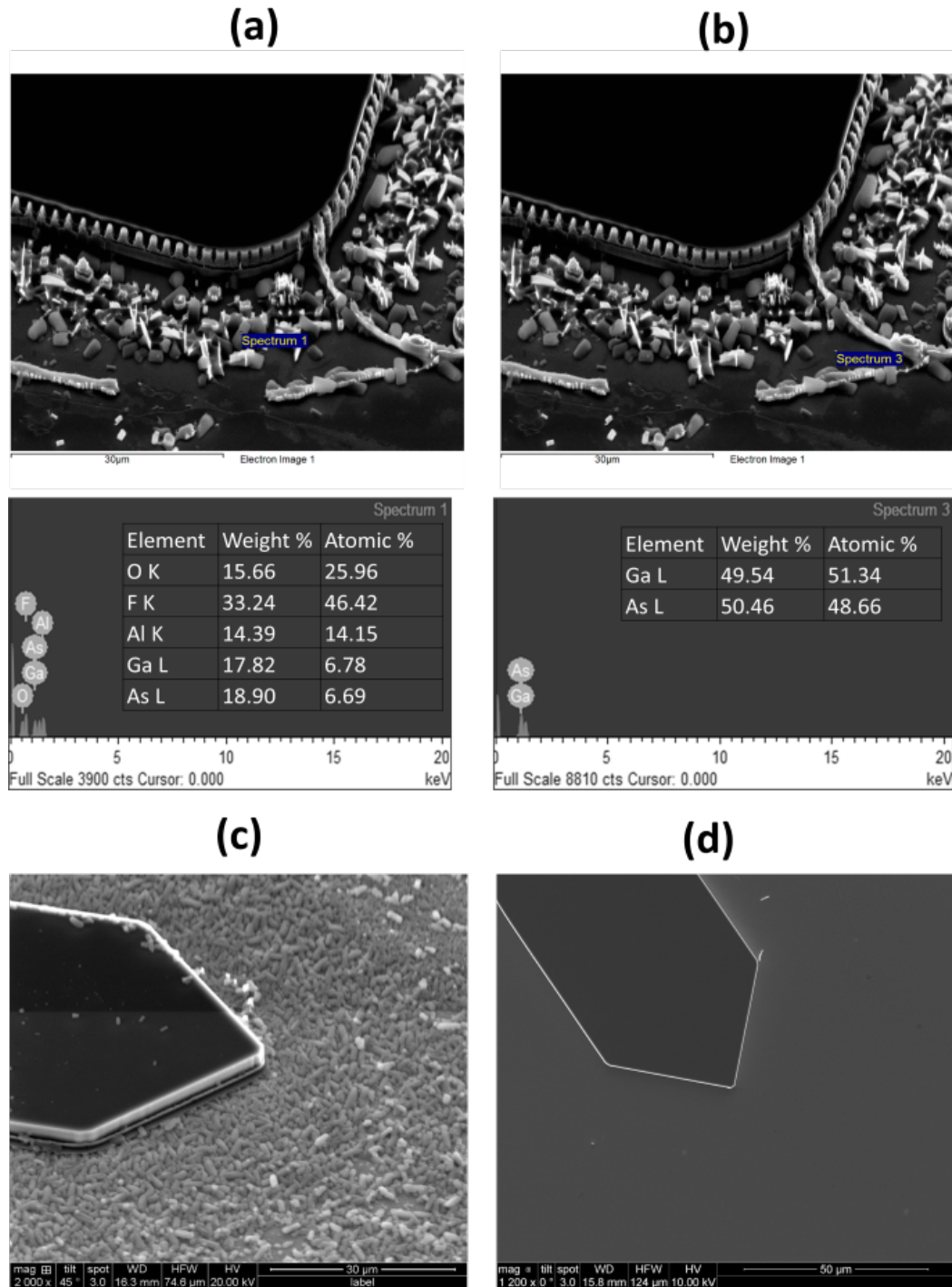


Figure 2.7: EDX spectra of (a) on the observed crystal and (b) on GaAs substrate. SEM images of a sample with AlF_3 crystals (c) before and (d) after MF319 developer dip. All the crystal is dissolved.

In addition to the III-V dry etch recipe, the etched facet profile is also highly dependent on the sample preparation process. The resist, dielectric, and etch recipes together define the facet profile. The resist first transfers its profile to the dielectric hard mask in the dielectric dry etch, and then the same profile is transferred from the dielectric hard mask to the III-V material.

First, two commonly used resists for vertical profile sidewalls are investigated. The dielectric hard masks are etched using AZ5214E and SPR220-4.5 photo-resists and the resulting sidewalls are compared in terms of verticality and smoothness. Two sample chips with SiO_2 hard masks are prepared for dielectric dry etching using AZ5214E and SPR220-4.5 resists in vacuum contact mode. Then both samples are etched together using the same SiO_2 etch recipe, followed by III-V etching. After cleaning the resist in 1165 remover [95] the resulting facets are examined in the SEM. Both resists give a very similar facet profile with vertical sidewalls and lateral ripples as shown in the SEM images in Fig. 2.8. No significant differences are observed between the two photo-resists. Thus, each resist can be used as a hard mask for vertical sidewall etching in dielectric patterning and direct material etching.

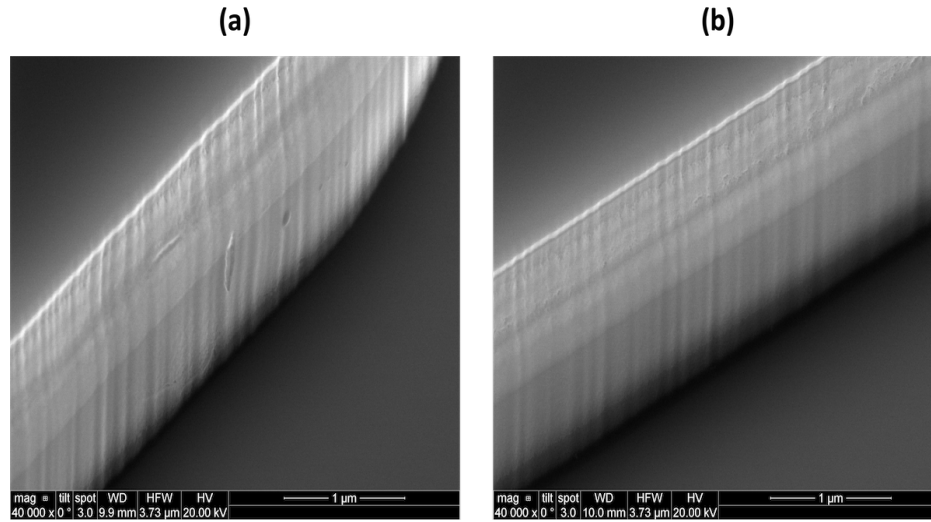


Figure 2.8: SEM images of GaAs sidewall etched with a Si_3N_4 hard mask patterned with (a) AZ5214E ($1.4 \mu\text{m}$ thick) positive tone resist and (b) SPR220-4.5 ($4 \mu\text{m}$ thick) resist mask.

Next, the effect of mask contact type on the lithography machine (Karl Suss MA6 Mask Aligner) is evaluated by varying contact types between low-vacuum ($\sim 0.5 \text{ bar}$) and high-vacuum ($> 0.75 \text{ bar}$) during lithography to investigate its effect on the resulting facet profile. Two GaAs samples with SiO_2 hard mask are prepared for the etch test. While one sample is patterned in low-vacuum contact mode, the other sample is prepared in vacuum contact mode using the same photo-resist (AZ5214E). After resist development, the dielectric hard mask is etched using the same recipe, and the resists are stripped. Then both samples are etched using the same etch recipe in the same tool. SEM images of both samples are shown in Fig. 2.9(a) and (b) for the low-vacuum and vacuum contact samples, respectively. Although both chips have a similar vertical facet profile, the vacuum contact sample has slightly less lateral ripples on its facet sidewall compared to the low-vacuum contact sample. In addition, another sample with the same dielectric hard mask is prepared for facet etching using e-beam lithography exposure for dielectric etching. After resist removal, facet etching

is performed using the same etch recipe. Figure 2.9 (c) shows an SEM image of the facet obtained from this process. The facet obtained is quite similar to that obtained in optical lithography. Similar corrugations are also observed in this sample. Further optimisation on this would improve the facet quality, but this is not investigated in this thesis as the achieved facet quality is acceptable for the purpose. Moreover, the presence of these corrugations on the mesa sidewall is a well-known feature and is due to the roughness phenomena of the line edge in the photo-resist [96]. When chemically amplified resists are exposed to light, acids are formed by diffusion of photoacids and catalytic reaction to form coiled polymer chains or polymer aggregates, resulting in a rough sidewall during development [97]. It can therefore be concluded that the roughness on the facet is not significantly related to the lithography tool and mode but to the photo-resist. Thus, the formation of roughness can be minimised with optimisation, but not fully avoided.

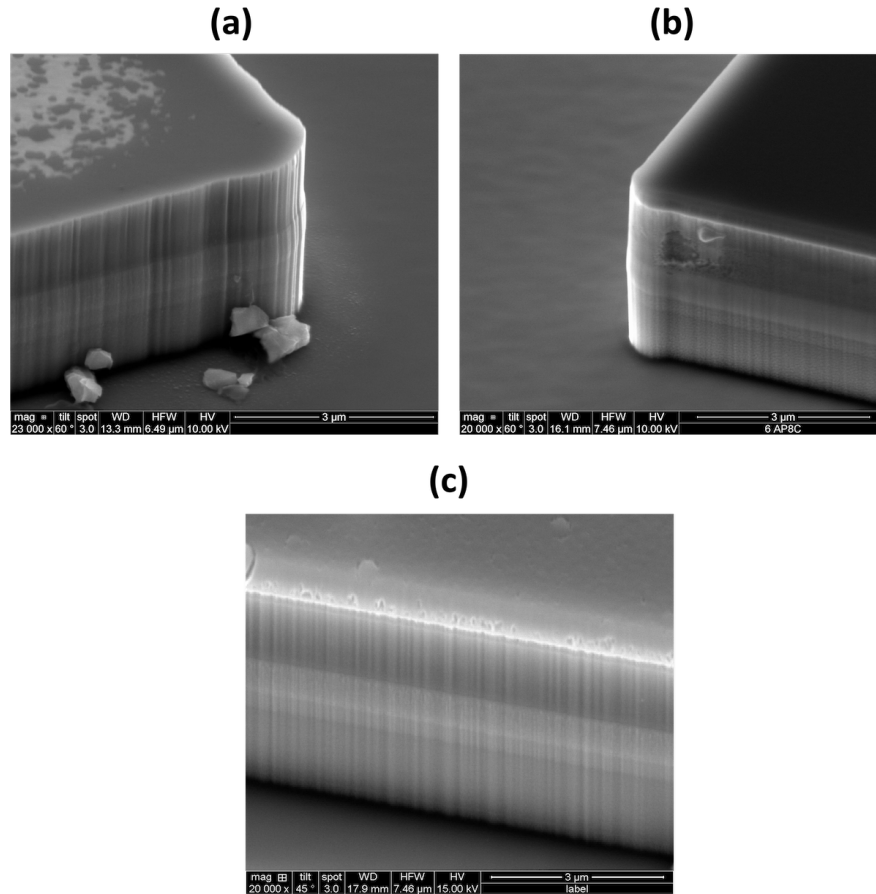


Figure 2.9: SEM images of obtained facet etch from samples with (a) low-vacuum mode and (b) vacuum mode in lithography process. (c) A similar sample with e-beam lithography exposure for dielectric etch.

Further optimisation of the roughness on the III-V facets is carried out by repeating the etch process with different dielectric hard masks including PECVD SiO_2 , sputtered SiO_2 and PECVD Si_3N_4 . The experiments show that the corrugation profile is different

for the different dielectrics studied. Because the samples are prepared using the same process with the same photo-resist, the only difference between the samples is the dielectric dry-etch recipes. The sample with a SiN hard mask appears to have less corrugation on the dielectric sidewall compared to the sample with PECVD SiO₂ mask, as shown in Fig. 2.10(a) and (b) respectively. It can be concluded that the curtain features on the dielectric are strongly related to the dielectric etch recipe. A mild etch recipe (low peak-to-peak voltage, V_{pp}) would significantly reduce the ripple on the dielectric sidewall. The SiN hard mask is dry etched using a dielectric etch recipe (active gas: SF₆) with 86 V peak to peak voltage. The SiO₂ hard mask in the other sample is etched using an oxide etch recipe (active gas: C₄F₈, H₂ and He) with a peak to peak voltage of 285 V.

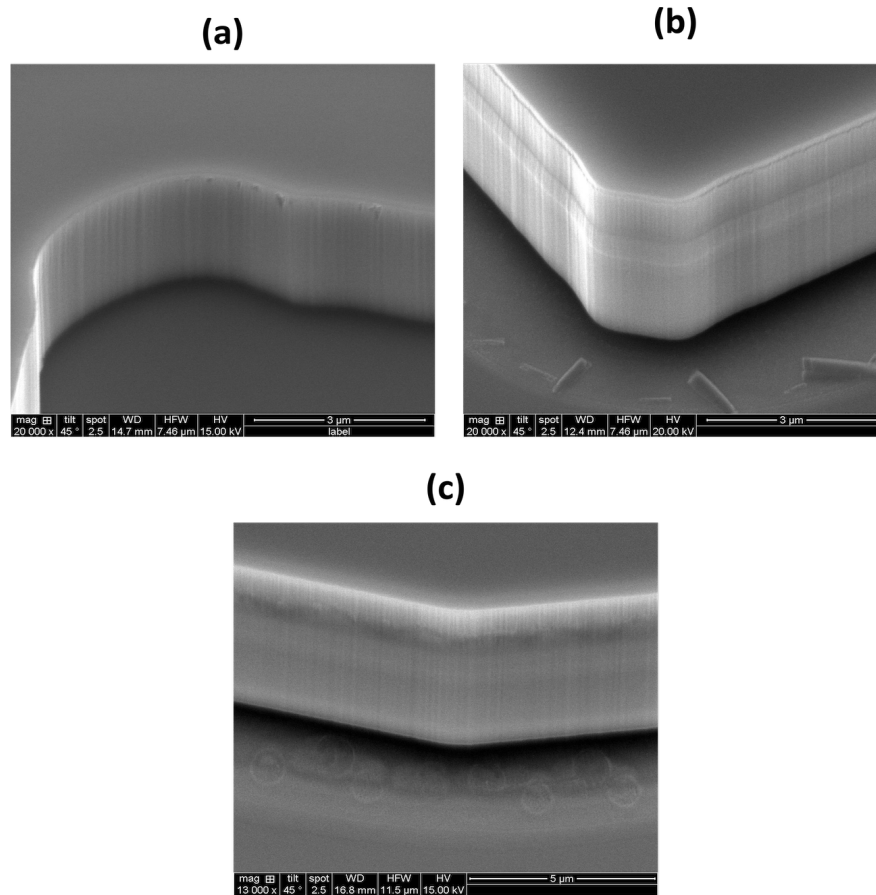


Figure 2.10: SEM images of obtained facet etch from samples with (a) PECVD SiO₂, sputtered SiO₂, (b) PECVD Si₃N₄, and (c) Sputtered SiO₂, sputtered SiO₂.

Sputtered SiO₂ shows the least corrugation effects compared to PECVD SiO₂ and SiN, despite using the same preparation process and etch. This suggests that the chemical structure of SiO₂ also has some effect on corrugation formation. However, in the actual device fabrication process, sputtered SiO₂ is not used because of its poor adhesion to the GaAs surface, which leads to delamination of the dielectric film and

the formation of air bubbles on the coupons. The high compressive stress of this film is another reason why we did not use this dielectric. The first-generation lasers reported in chapter-5 are fabricated using a PECVD SiN hard mask in the facet etch step. However, the lower stress and more repeatable SiO₂ recipe in PECVD results in a dual layer hard mask (PECVD SiO₂ and SiN) being used for the final-generation lasers. Figure 2.11 illustrates the facet in the final-generation lasers.

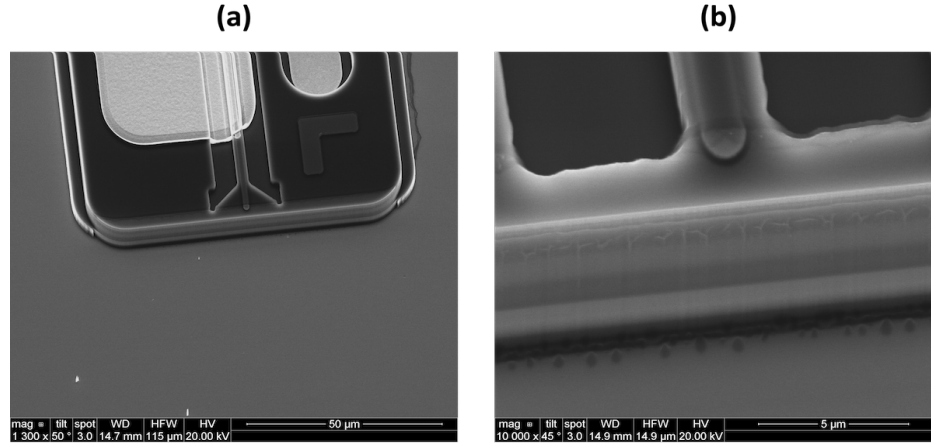


Figure 2.11: SEM images of facet etch obtained using a dual dielectric layer and dry etch recipe R9 in the final-generation laser process.

2.3.2 Ledge-less Coupon Process

Standard transfer-printable QD laser devices have a protruding ledge around the coupon. The ledge provides improved dielectric encapsulation and better adhesion of the photo-resist tether to the coupon. This increases the overall strength of the tethering system during release etching. Figure 2.12(a) schematically shows the side view of a coupon facet with the ledge (left) and without the ledge (right). However, a disadvantage of the 2-3 μm ledge is the limited proximity of the emitting facet to the SOI waveguide facet during edge coupling of the light. The standard fabrication flow used in the second generation laser (transfer-printable laser) coupon run is modified to remove the ledge from the emitting facet of the coupons while retaining the ledge on the other side of the coupon. SEM images of two coupons with and without ledge in the front facet are given in Fig. 2.12(b) and (c), respectively.

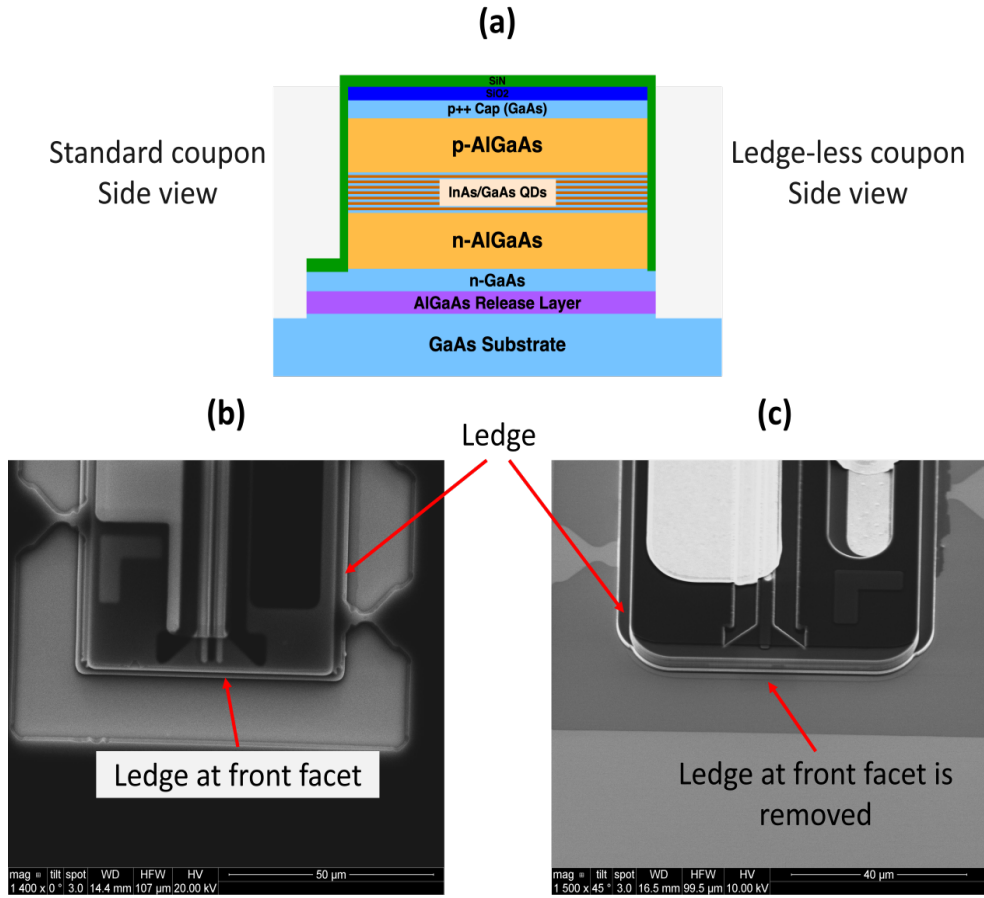


Figure 2.12: (a) Schematic of front facet cross-section for a coupon coupon with a ledge (patio) on left-size and without a ledge on right side. SEM images of fabricated laser coupons (b) with and (c) without a front-ledge. The ledge surrounds the coupon, but in the coupon without ledge, the ledge is removed at the emitting facet.

However, eliminating the front facet ledge with a self-aligned process caused some process problems during fabrication. As the dielectric thickness at the edge of the front facet of the laser coupon is thinner than that of the on-coupon, the plasma etch starts to erode the p-cladding layer, as shown in Fig. 2.13. The notch on the facet leads to an increase in threshold and rollover at higher injection currents for transfer-printable lasers. This problem is solved by reducing the overetch time in the dielectric layer etch prior to the encapsulation etch and increasing the dielectric thickness.

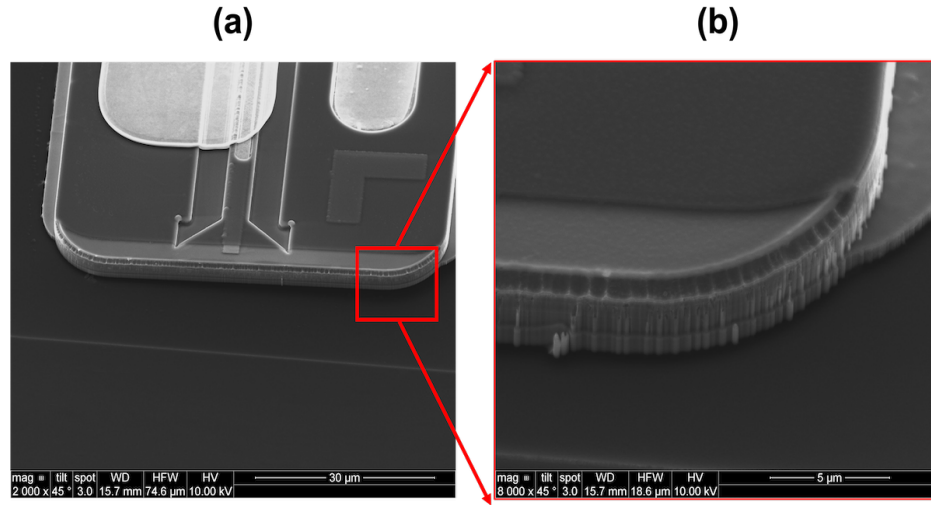


Figure 2.13: (a) SEM image of a ledge-less laser coupon showing the etch into p-cladding after encapsulation etch. (b) A zoom on the facet with notch on upper cladding.

2.3.3 High Reflectivity Mirror

In Fabry-Perot cavity-based etched facet lasers, one of the two facets acts as the emitter (partially reflective) facet and the other is the high reflective (HR) facet, as shown in Fig. 2.14(a). The transfer-printable lasers in this work have etched-facet with different rear mirrors including metal-dielectric based HR and multimode interference (MMI) coupler-based reflectors, also called MIR. To achieve a laser diode with high-performance laser characteristics (i.e. reduced threshold current and increased output power), a smooth and vertical facet with an efficient HR mirror coating on the back facet is required. The development of a high-quality etched facet is discussed in the previous section. A thin layer of SiO_2 or SiN passivation on the facets is useful to protect the facets from damages in subsequent processing and to reduce facet loss by improving the roughness of the sidewall. The simulated reflectivity of the output facet with dielectric passivation layer (SiO_2 or SiN) by varying thickness is shown in Fig. 2.14(b). The thickness of the SiO_2 passivation layer is set to $\sim 60 \text{ nm}$ in the final-generation laser run to achieve a reflectivity of over 20% from the emitting facet.

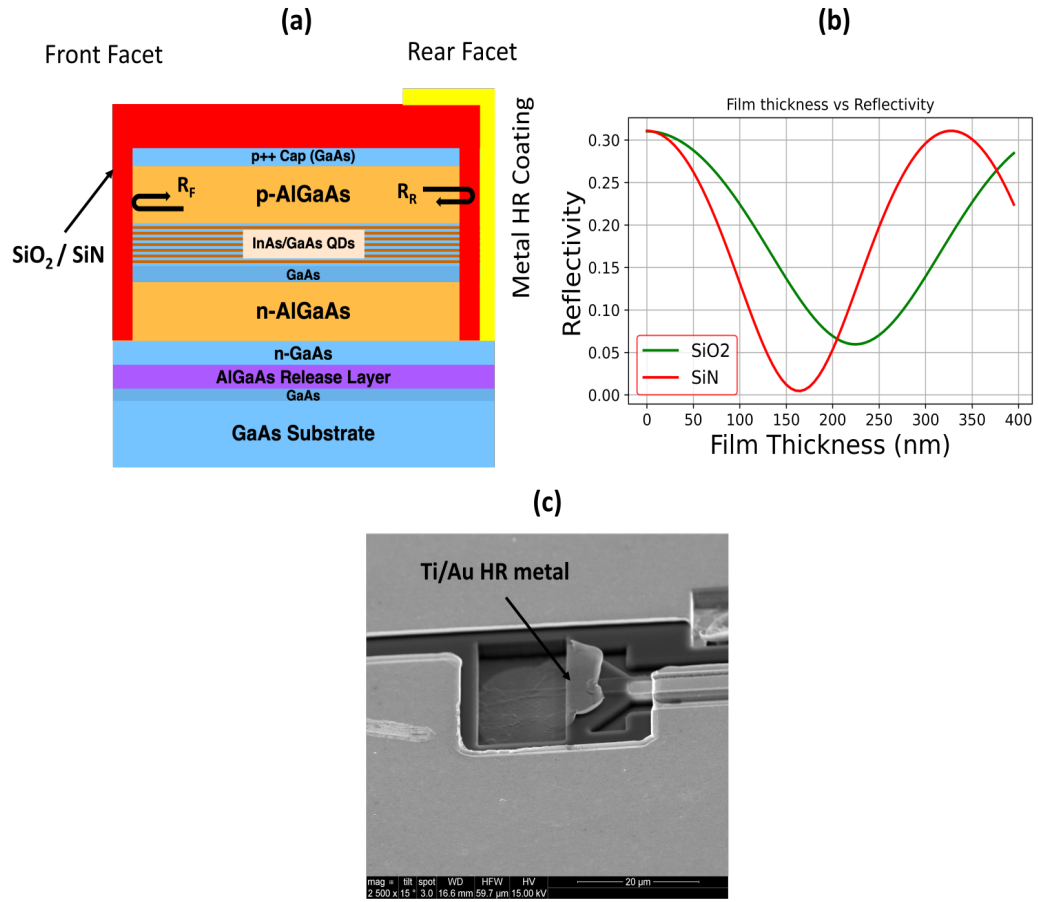


Figure 2.14: (a) Schematic illustration of dielectric passivation on front facet sidewall and additional HR coating on rear facet. (b) Emitting facet reflectivity as a function of dielectric film thickness. The simulated reflectivity from the rear facet is over 93% with HR coating at 1310 nm.

In this work, two different metal-dielectric HR coatings are investigated. In second generation lasers, a metal dielectric HR mirror consisting of a 240 nm SiN passivation layer and e-beam deposited Ti-Au (5 nm - 100 nm) metal layers on the back facet. The thickness of the Ti layer has to be adjusted so that the absorption resulting from this material is low while at the same time providing sufficient adhesion for the Au HR layer. The measured reflectivity of the front and back facets of these lasers is estimated to be 19% and 46% respectively, with a $\pm$ few percent error. These values are obtained from similar reference cleaved-facet ridge lasers by measuring the inverse differential quantum efficiency at different cavity lengths. The low reflectivity could be due to the high absorption in the Ti layer. The second HR coating process is developed using a dielectric layer (60 nm SiO₂ passivation) in conjunction with a sputtered Al (150 nm) mirror. The absence of an absorbing layer in this method improves the mirror performance with a measured reflectivity of 88%. The performance of lasers based on both HR coatings is presented with a discussion of reflectivity calculation in chapter-5.

The other type of reflective rear mirror studied in this work is MIR. These mirrors are derived from a 1x2 Multimode Interference (MMI) coupler by terminating the output

ports with two 45° etched mirrors [98, 99]. A schematic illustration and a scanning electron microscope (SEM) image of the MMI mirror are given in Fig. 2.15(a) and (b), respectively. Light is imaged back onto the input waveguide by reflections from the etched mirrors that are placed at the location where two spots occur, as given in Fig. 2.15(c) and (d). A schematic illustration and a scanning electron microscope (SEM) image of the MMI mirror are given in Fig. 2.15(a) and (b), respectively. The MIR mirrors are defined in the same etch step as the standard facets. A similar reflectivity of 46% is estimated for this type of rear mirror compared to the TiAu-based HR mirror.

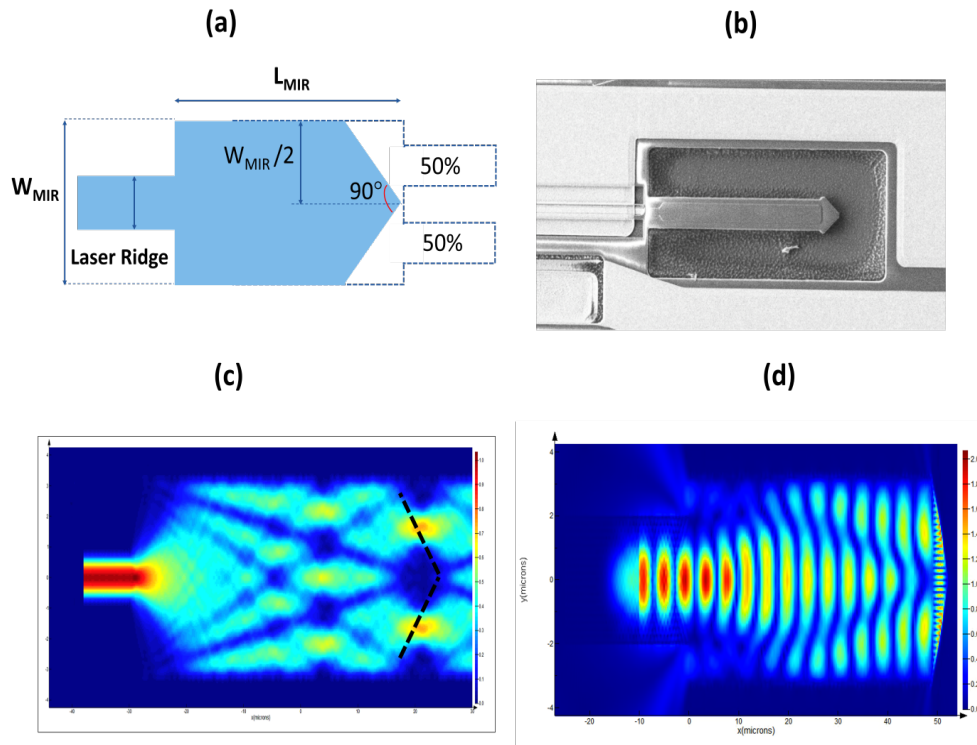


Figure 2.15: (a) Schematic illustration of MIR derivation from a 1x2 MMI and design parameters (b) E-field plot of a 2D simulation of 1x2 MMI showing where the two 45 degree mirrors are placed. (c) SEM images of a fabricated MIR on a laser coupon. (d) E-field plot for a 1x2 MIR in LUMERICAL varFDTD [100].

MMI reflectivity above 90% is simulated for lasers with an MIR mirror of $6 \mu m$ and $6.5 \mu m$ wide and $48 \mu m$ to $52 \mu m$ long. An advantage of MIR mirror over the etched-facets mirror with metal coating is that one step in the process can be eliminated. However, the MIR is more sensitive to manufacturing imperfections and misalignment between the laser waveguide and the MMI. The reflection of the MIR is simulated as a function of width and length variation and is shown in Fig. 2.16(a) and (b), respectively. The design has an acceptable misalignment tolerance of about $1 \mu m$ in width and $15 \mu m$ in length with a reflectivity greater than 90%. Although performance is more dependent on the MIR width than on the length, simulated tolerances are readily achievable in optical lithography. Fig. 2.16(c) shows the reduction in reflection as a function of fabrication misalignment between the laser

ridge waveguide and the MMI during optical lithography. 300 nm misalignment would result in a 6% decrease in reflection. In addition, the rounding effect at the MIR tip where the two 45° mirrors meet due to lithography is the main source of loss, as shown in Fig. 2.16(d).

The effect of fabrication on MIR can be optimised by adjusting the width of the laser ridge (also known as the access waveguide). A wider waveguide (i.e. an up-tapered waveguide) reduces scattering and helps MIR to become more robust to fabrication mismatch in terms of length and width, as well as misalignment. However, the effect of corner rounding becomes more dominant with a wider waveguide as the gap between two lobes of equal intensity is reduced [101].

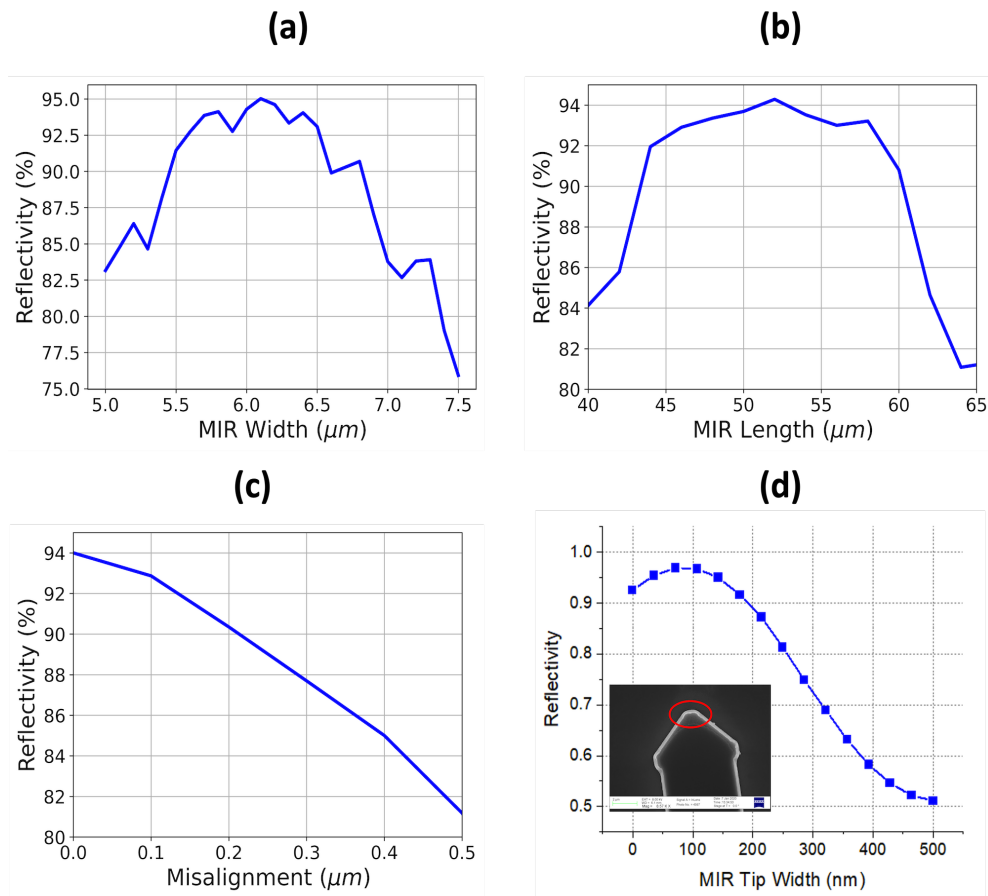


Figure 2.16: Reflectivity of an 1x2 MIR with 2.5 μm wide ridge waveguide as a function of variation in (a) MMI width (the length is set to 52 μm), (b) MMI length (the width is set to 6 μm) and (c) misalignment between access waveguide and MMI body (the length is set to 52 μm, the width is set to 6 μm). (d) Reflectivity as a function corner rounding effect on MIR.

The estimated reflectivity in fabricated MIR is ~46% for second-generation lasers. This is around half of the simulated values, which can be explained by misalignment (300 nm) and facet roughness. In the final-generation laser, using the same MIR design, Al metal is sputtered on the MIR mirror sidewall, similar to the standard etched-facet mirror. The characterisation shows an improved MIR performance with a

reflectivity of around $\sim 75\%$ compared to MIR with only a dielectric coating. It can be concluded that MIR mirrors also require HR coatings for high reflectivity, since the etched facet mirror with Al HR coating also showed similar reflectivity.

2.3.4 Stress Management

One of the main failure risks for MTP coupons is the unbalanced stress in the dielectric layers accumulated during fabrication processes such as facet etching, passivation and encapsulation. These stresses can be tensile or compressive, causing the coupons to bend, which above a certain threshold can overcome the adhesion strength to the print substrate. It is therefore important to consider the net stress induced by the dielectric and metal layers on the coupons during design and fabrication. Flat coupons or devices are required to enable high integration yields on the target substrates during transfer printing. Unbalanced stress on the devices can cause the coupon to bend upwards or downwards depending on the net stress on the device. The bending can also be due to geometric stress, as the dimensions of the laser devices are less than $100\ \mu\text{m}$ wide and up to $2.4\ \text{mm}$ long with a thickness of $< 5\ \mu\text{m}$. Thus, geometric stress is the dominant stress mechanism in this work as the thickness/length aspect ratio is > 500 . Because the bow is parabolic, any additional stress induced by the deposited dielectric and metal layers must be tailored by adjusting their net stress during the fabrication process to obtain essentially stress-free coupons.

An experimental study is carried out on lasers from different generations, which are held by bulk polydimethylsiloxane (PDMS) at one end of the coupon. The laser coupons have an upward curved profile. The evolution of the stress optimisation on the QD laser coupons is shown in Fig. 2.17. The stress on the second-generation laser coupons results in an upward bend of $\sim 150\ \mu\text{m}$ over a distance of $1.2\ \text{mm}$, while the final-generation laser is bent upward by $\sim 100\ \mu\text{m}$ over a distance of $2\ \text{mm}$. The upward bending characteristics of the coupons indicate a net tensile stress in the laser coupons. Minimising the stress in the coupons allows for a smooth bottom surface and reduced pillar formation in the coupons after release etching [102]. This also improves the integration yield. These phenomena are discussed in more detail in the section on release etching in chapter-4. In addition, coupon devices with unbalanced stress can lead to unstable integration and cause device displacement during post-processing (i.e. resist cleaning or lithography) and characterisation (i.e. electrical probing).

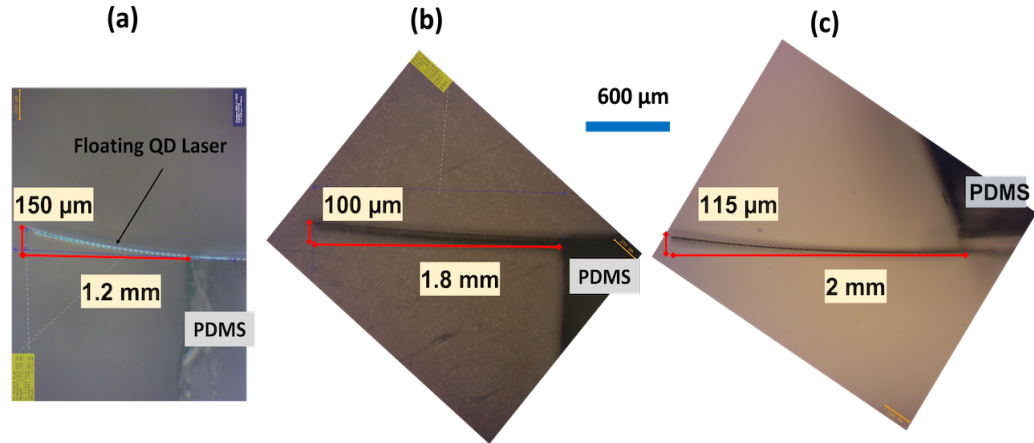


Figure 2.17: Free hanging functional QD laser coupons are bending upwards due to net tensile stress in (a) second-gen coupon, (b) second batch of second-gen coupon and (c) final-gen laser coupons. More bending in the coupon over the distance indicates a larger stress.

Effective stress management can be achieved by tailoring both the thickness and the stress characteristics (whether compressive or tensile) of each dielectric and metal layer on the coupon. However, this requires that the fabrication process is matched to the required dielectric film thickness and corresponding stress. Stress management is done as follows. First, the final dielectric layers accumulated and their thickness are estimated by simulating all the fabrication steps and etching process that the laser devices will go through. The same dielectric layers are then sequentially deposited on 4-inch blank Si wafers. Before and after each deposition, the curvature on the wafer is recorded using Tencor stylus profilometers [103]. Stress is then estimated by comparing the change in radius of curvature before and after film deposition using the cantilever beam technique developed by G. Gerald Stoney. Finally, taking into account the stress induced by the p- and n-metal layers, the dielectric thickness of the coupon is deliberately set so that the net stress is compressive and approximately 60 MPa. The purpose of this deliberate stress is to minimise bowing in the final coupons, resulting in a significantly high print yield of over 90%.

2.3.5 Tether Design

An essential part of micro-transfer printing is the anchoring system, also known as the tether system, which is designed to maintain the stability of the devices in position on the source substrate during and after the release etch. During the removal of the sacrificial layer, the tethers are subject to intermolecular forces, also known as the capillary effect, between the bottom surface of the coupon and the substrate. The anchor system should be strong enough to withstand this force during the drying phase following the release etch. This force is present only at this stage in the drying process. An anchor system consists of a number of individual photo-resist tethers, which in this study are defined around the coupon with a pitch of 40 μm . One end of

the tether is attached to the source substrate, while the other end is attached to the coupon. The tethers on a coupon can be made of a variety of materials, including photo-resist, dielectric, or a combination of both, depending on the process used. When selecting a tether material, the impact of the tether material on the process should be considered. For example, a resist tether is easy to apply, but must be removed after transfer printing of the coupons on the target wafer. The use of a dielectric tether does not need to be removed after integration, but the thickness required for a strong anchor system and the corresponding stress on the coupon need to be considered as it could degrade the transfer printing process. In this study, we focus on photo-resist tethers made from S1828 and SPR220-4.5.

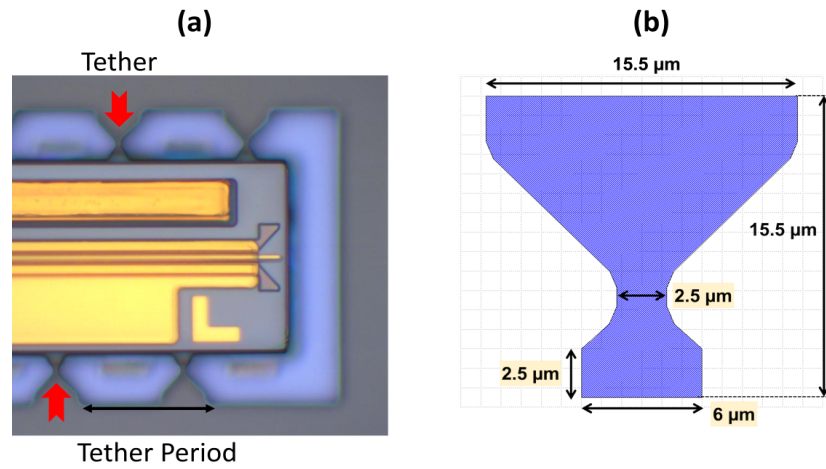


Figure 2.18: (a) Image of coupons after tether definition using S1828 photo-resist. The tethers are defined with an anti-phase arrangement where one of the tethers in a tether pair is shifted by a half-tether period. (b) Dimension of the funnel neck tether used in this thesis.

The tethers are arranged in an anti-phase configuration by shifting the tether on one side of the coupon by half a tether period. An optical image of the S1828 tether on a $65\ \mu\text{m}$ wide laser coupon with this configuration is given in Fig. 2.18(a). The idea behind the anti-phase tether design is to give the etchant asymmetric access to the sacrificial layer from both sides of the coupon. The dimension of an individual tether is shown in Fig. 2.18(b). During coupon pick-up in micro-transfer printing, the tether is expected to be broken at the weakest point (i.e. $2.5\ \mu\text{m}$ neck) by leaving its foot, the wide section, on the GaAs source substrate.

The same coupon and tether design is used in another batch of laser coupons with SPR220-4.5 photo-resist as the tether material, and a high survival rate of over 95% is achieved after the same release etch. Another reason for switching from S1828 to SPR220-4.5 is the reduction in pillar formation at the bottom of the coupon. This is related to the strength of the tether system and more details can be found on this in the section-4.1. In addition to the $65\ \mu\text{m}$ wide coupons, the final-generation laser includes $80\ \mu\text{m}$ wide coupons to provide more space for metal pads on the coupon

that facilitate electrical probing during characterisation. Despite using the same tether design and resist, most of the $80\ \mu\text{m}$ wide coupons collapse during release etching. This suggests that the design and density of the tether are not suitable for coupons larger than $65\ \mu\text{m}$.

Tether Period (μm)	40			60		
	Tether Weakest Point Width (μm)					
Coupon Width (μm)	2.5	5	8	2.5	5	8
30	NC	NC	NC	NC	NC	NC
50	NC	NC	NC	NC	NC	NC
100	CL	NC	NC	CL	CL	NC
150	CL	NC	NC	CL	CL	NC
200	CL	NC	NC	CL	CL	NC

CL: Collapsed, NC: Not collapsed

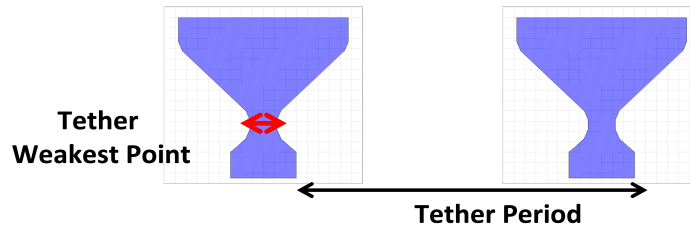


Figure 2.19: Coupon collapse as a function of tether neck width (the narrowest part) and duty cycle. As coupons become wider, the tether neck must be wider or denser (more tethers in the same distance) to survive the release and drying process.

A new set of masks is designed to investigate the correlation between the width of the coupon and the width of the weak points on the tethers. $1\ \text{mm}$ long coupons have varying widths ranging from $30\ \mu\text{m}$ to $200\ \mu\text{m}$. Tethers with narrow point widths (namely $2.5\ \mu\text{m}$, $5\ \mu\text{m}$ and $8\ \mu\text{m}$) are arranged on these coupons in different duty cycles of $40\ \mu\text{m}$ and $60\ \mu\text{m}$. After release etching, the coupons are inspected for collapse. Figure 2.19 shows the coupon collapse as a function of the width and period of the tether. Coupons with the standard tether ($2.5\ \mu\text{m}$ wide neck) tend to collapse at coupon widths of around $100\ \mu\text{m}$ and wider. In actual device coupons, $80\ \mu\text{m}$ wide coupons also collapsed. For the $5\ \mu\text{m}$ wide tether, coupons wider than $100\ \mu\text{m}$ collapsed when the tether period was $60\ \mu\text{m}$. This suggests that as the tether expands or the tether period is shorter, the tether system becomes stronger and more resistant to collapse.

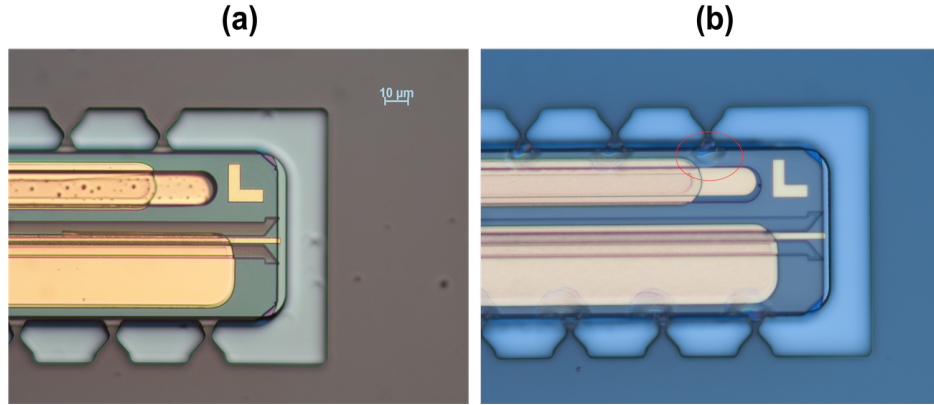


Figure 2.20: Optical images of tethers on $80\ \mu\text{m}$ wide coupons (a) before and (b) after release etch of sacrificial layer. Collapsed coupons have discolouration at the junction of the coupon body and the tether.

The presence of discolouration at the junction between the coupon body and the tether indicates the collapse of the coupons after the release etching. The change in coupon and tethers before and after the release and drying process is shown in Fig. 2.20(a) and (b) respectively. Following the experiment, the tether was redesigned by increasing its narrowest neck width from $2.5\ \mu\text{m}$ to $6\ \mu\text{m}$. This modification increases the strength of the individual tether, and therefore the tether system, and prevents the collapse of the $80\ \mu\text{m}$ wide coupons in the final-generation of laser coupons. The release or undercut etch process is discussed in detail in section 4.1.

2.4 Conclusion

This chapter describes the epitaxial structure used for InAs/GaAs QD lasers, general layout design, and the fabrication process for transfer-printable QD lasers. The additional layers required in a transfer-printable III-V epilayer are indicated. An AlGaAs layer with 95% and 93% Al is used as the release layer in the epilayer used in this work. The geometry of the fabricated laser coupons and devices, including the variation of ridge width, cavity length, and reflective mirror, is explained. The physical length of the transfer-printable coupons is up to $2.4\ \text{mm}$ with a waveguide width of 2.5 and $3.0\ \mu\text{m}$. In addition, the various process developments and optimisations for high-power transfer-printable edge-emitting FP lasers are discussed. The developed ICP dry-etch recipe, which produces smooth and vertical facets, together with the sputtered Al-based HR rear mirror, allowed a significant improvement in the output power of the transfer-printed lasers. The ledge-less coupon process allowed us to reduce the longitudinal misalignment between the laser and the receiving waveguide and to improve the light-coupling efficiency. By optimising the stress on the coupon device and tether system, the release etch yield was increased by preventing coupon collapse during the undercut and drying process. The balanced stress also enabled QD laser coupon integration with higher print yield.

Chapter 3

Optical Coupling Schemes

The light coupling schemes from the III-V laser to the receiving waveguide play a critical role in the realisation of efficient PICs. This chapter begins with an overview of common light coupling schemes to waveguides. It examines three different configurations of edge-coupled waveguides selected for quantum dot (QD) laser integration. The waveguide platforms studied include 220 nm SOI, 3 μm SOI and 300 nm SiN with SU-8 polymer spot size converters (SSCs). A schematic illustration of the side view and cross-section (at the facet) for the edge coupling configuration implemented in this work, with the QD device integrated next to a receiving waveguide, is shown in Fig. 3.1. Edge-emitting QD lasers are fabricated and integrated onto these photonic platforms using micro-transfer printing (MTP). The chapter presents simulated coupling efficiencies and misalignment tolerances for each platform, along with a detailed explanation of the configurations studied. In addition, the fabrication and integration challenges using MTP are identified for each platform, along with the associated opportunities. The level of alignment achieved in each configuration is discussed, along with suggestions for improvement. Finally, the chapter concludes with a comparison of the advantages and limitations of each coupling approach.

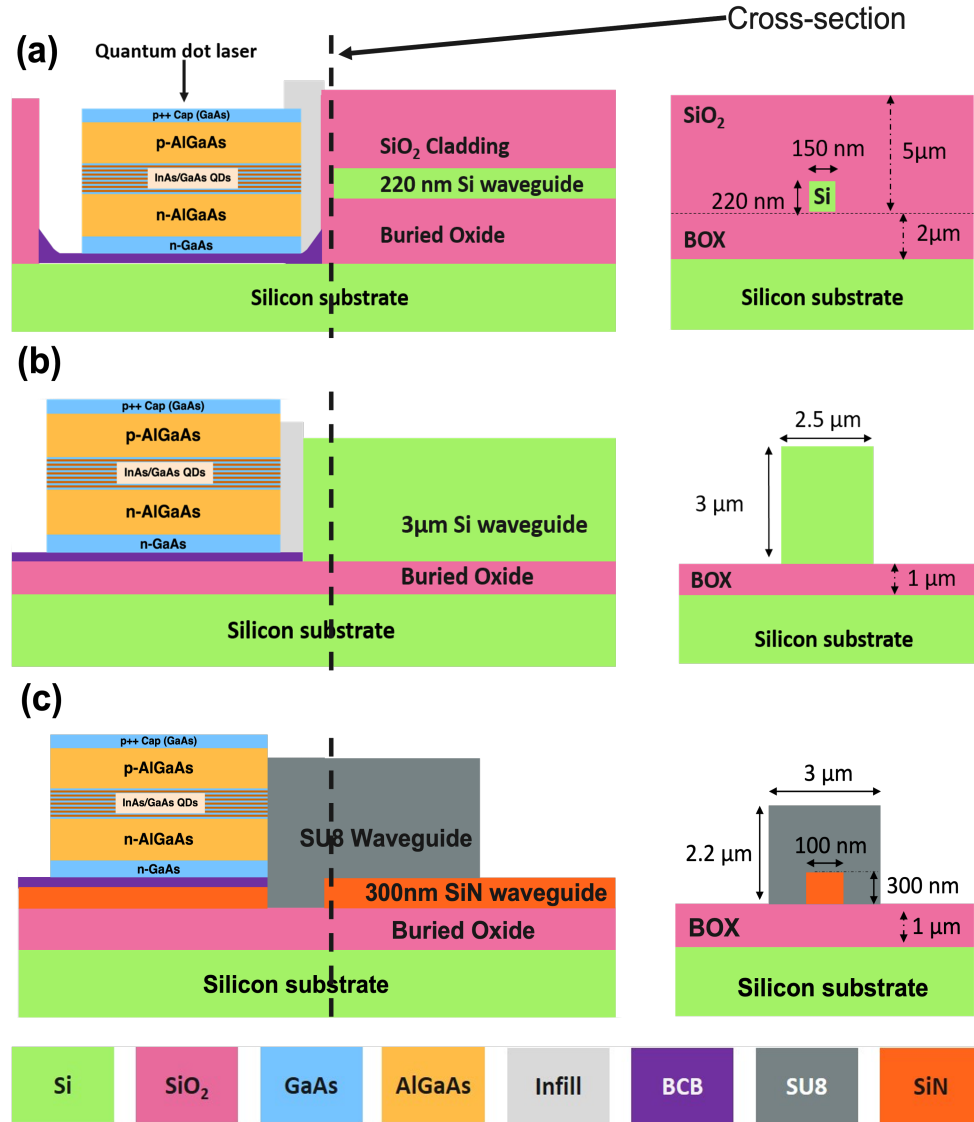


Figure 3.1: Edge-coupling configurations of the studied waveguide platforms. (a) QD laser transferred inside a deep recess where light is coupled to 220 nm Si waveguide. Cross-section of thin Si waveguide with 2 μm BOX layer and 5 μm top SiO₂ cladding (right). (b) Integrated laser next to a 3 μm Si waveguide on the BOX layer and cross-section of 2.5 μm wide waveguide (right). (c) Laser printed on remaining SiN layer and coupled to SiN waveguide via SU-8 down-coupler and waveguide cross-section at the start of SiN (right).

3.1 Optical Coupling Schemes

Light transmission between two dissimilar waveguiding platforms remains one of the main sources of coupling losses. The optical loss incurred when coupling light from a single mode fibre to a single mode waveguide or from an active component (i.e. integrated laser) to a single mode waveguide is referred to as the coupling loss. This loss depends on the mismatch of the mode shape and the misalignment between the fibre and the waveguide [104, 105]. Considerable effort has been invested in various coupling approaches to improve coupling performance with relaxed alignment

tolerance. These approaches can be grouped into three categories; grating coupling, evanescent couplers, and edge couplers.

3.1.1 Grating Couplers

The grating couplers would be used to drive a PIC circuit by providing the light signal from a discrete laser device or to characterise a PIC circuit that already has an integrated light source. In the communications wavelength range (1260-1650 nm), the mode field diameter (MFD) of a fibre is approximately 8-10 μm with circular symmetry. The MFD is the point at which the mode power density is reduced to $1/e^2$ of the maximum power density. In contrast, the MFD of a photonic integrated circuit (PIC) is typically elliptical and about $0.5 \times 0.3 \mu\text{m}$ [106]. The grating coupler with a $10 \times 10 \mu\text{m}$ footprint can match the mode sizes between the two media.

A grating coupler consists of a periodic refractive index modulation on the surface of the waveguide, which scatters light in a constructive interfering manner as a vertically radiated wave, allowing the fibre mode to be matched. These sub-micron periodic structures create a coherent interference condition that allows light to be coupled between the waveguide and the fibre and vice versa. The incoming or outgoing light is typically directed at a 10° angle [107] to minimise the fundamental first order back reflection to the PIC / fibre and maximise the injection efficiency according to the Bragg law. Lithographically defined gratings are formed by shallow etched trenches (typically 70 nm deep etch on 220 nm SOI) on the SOI waveguide as shown in Fig. 3.2. The peak wavelength of the coupler can be determined by tuning the pitch of the trenches, the effective index of the grating-coupler region, the index of the oxide layer and the angle of incident light.

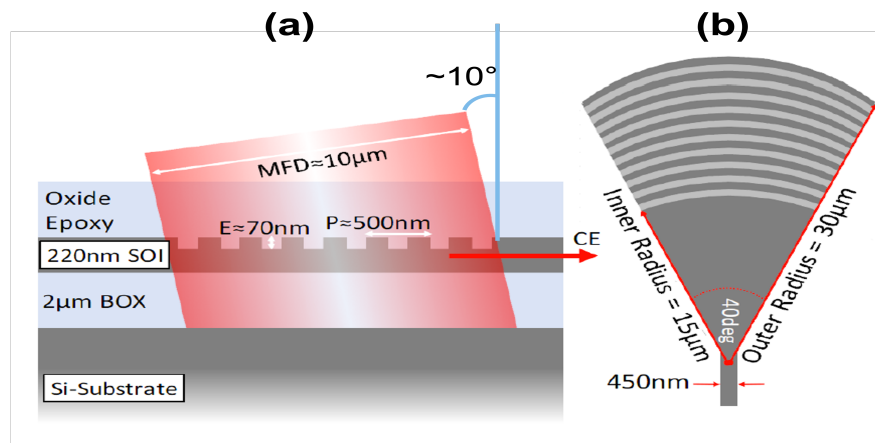


Figure 3.2: Fiber to PIC grating-coupling structure: (a) Side-view schematic of the grating-coupler defined on the SOI. (b) Top-view schematic of a 2D focusing grating-coupler [108].

The coupling efficiency of typical grating couplers is $\sim 30\%$ at the peak wavelength with a 3 dB bandwidth of less than 80 nm [109, 110]. More recently, a coupling

efficiency of less than 1 dB has been reported using back-reflected grating coupler designs [111]. The flexibility of positioning the gratings on the chips, allowing wafer-scale testing, is an advantage of this approach. However, the strong polarisation dependence is a drawback.

In this work, surface grating couplers from Imec's standard iSiPP50G photonics design kit (PDK) library are used for characterisation. The measured insertion loss of the gratings and the characterisation results are discussed in chapter-6.

3.1.2 Evanescent Coupling

Evanescent coupling is attractive because of its low insertion loss, broadband coupling, and insensitivity to polarisation. It also shares the relaxed alignment tolerances characteristic of grating coupling. In particular, unlike edge coupling, the inverted taper in the evanescent coupler does not need to be placed at the edge of the photonic integrated circuit (PIC). This eliminates the need for precision dicing and polishing of the PIC edges, resulting in a cost-effective implementation at scale.

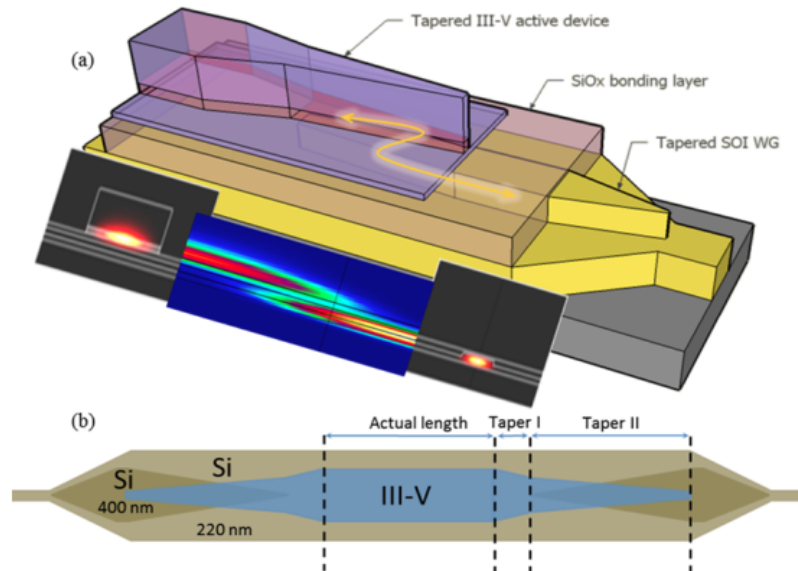


Figure 3.3: Schematic of adiabatic evanescent coupling between III-V active device and SOI waveguides. (a) The simulated optical mode distribution at different sections of the waveguides. (b) The gradual tapers in the III-V squeeze the mode and push it into the SOI waveguide. [112].

This approach offers a low insertion-loss of <1 dB with a relaxed alignment tolerance of ± 2 m between the top and underlying single mode waveguides [113]. The inverted taper of the evanescent coupler can be positioned anywhere on the SOI, but the need for millimetre-long tapers increases the footprint and must be considered when designing a PIC. Multiple tapers in both waveguides might be needed for higher coupling efficiency as shown in Fig. 3.3. This approach is used in this paper between

the light coupling from a SU-8 polymer waveguide to a SiN waveguide in the section 3.2.3.

3.1.3 Edge-Coupling

Edge coupling (also known as butt-coupling) is a widely used approach that involves the positioning of optical elements in the plane at the edges of the PIC. It allows both TE and TM polarised light signals to be coupled over a wide wavelength bandwidth. The inversely tapered waveguide, which expands the mode by reducing its effective index close to that of the waveguide tip, provides better mode size matching with improved alignment tolerance, as shown in Fig. 3.4(a). A spot size converter (SSC) can be used as a temporary waveguide to convert the highly confined mode from silicon to a larger low-index waveguide, which provides much better coupling efficiency, or vice versa. The light signal is first edge coupled to the SSC waveguide and then evanescently coupled to the underlying inverse-tapered SOI waveguide [114]. An SU-8 polymer-based SSC is used for the SiN platform studied in this thesis.

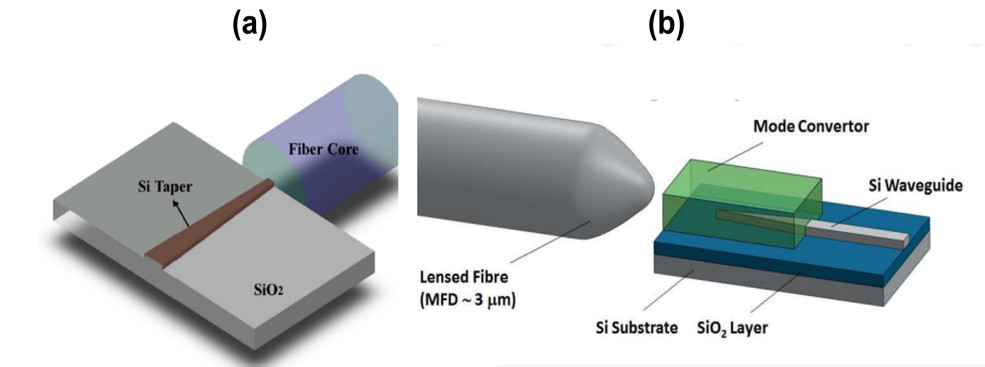


Figure 3.4: Schematic of edge coupling between fiber and SOI waveguides. (a) The inverted taper without overlay waveguide expands the optical mode for better mode-size matching [115]. (b) Inverted taper with polymer overlay waveguide, also called spot size converter (SSC) utilizes the edge coupling of light to a overlay waveguide via edge-coupling and then evanescent coupling and mode size conversion to the waveguide on SOI. The SSC can be made of polymer, SiN, or SiO_x [108].

Typically, edge coupling requires sub-micron ($< 1 \mu m$) misalignment tolerance for such an edge coupler to achieve insertion loss better than -1.5 dB [116]. A $\pm 1 \mu m$ lateral misalignment can introduce an excess loss of 3 dB . To relax the alignment tolerance and improve the modal overlap between the waveguide and the fibre or laser for better coupling efficiency, multi-tip receiving waveguides are used [117–119]. Although edge couplers have higher coupling efficiency, wider bandwidth, and lower polarisation dependence, they have some limitations including a comparatively larger footprint, a fixed coupling position, and the requirement for etched facet technology on both III-V and SOI.

In this thesis, three different edge-coupling configurations based on three waveguiding platforms are investigated. The next session presents the design and

fabrication of these platforms. The simulated and measured coupling efficiencies are discussed together with the misalignment tolerance for each design.

3.2 Investigated Edge Coupler Configurations

The advantages of edge coupling are low wavelength and polarisation dependence with only a single interface between the waveguides. The coupling efficiency depends on the mode size mismatch between the laser and the passive waveguide, the refractive index in the gap between the laser and the waveguide, and any misalignment in the lateral, vertical, and longitudinal dimensions. The light emitted from the active III-V device is coupled into the waveguide, which is levelled vertically (Y). In addition, alignment of the laser to the waveguide in lateral (X) and longitudinal (Z) directions also needs to be addressed for improved coupling performance.

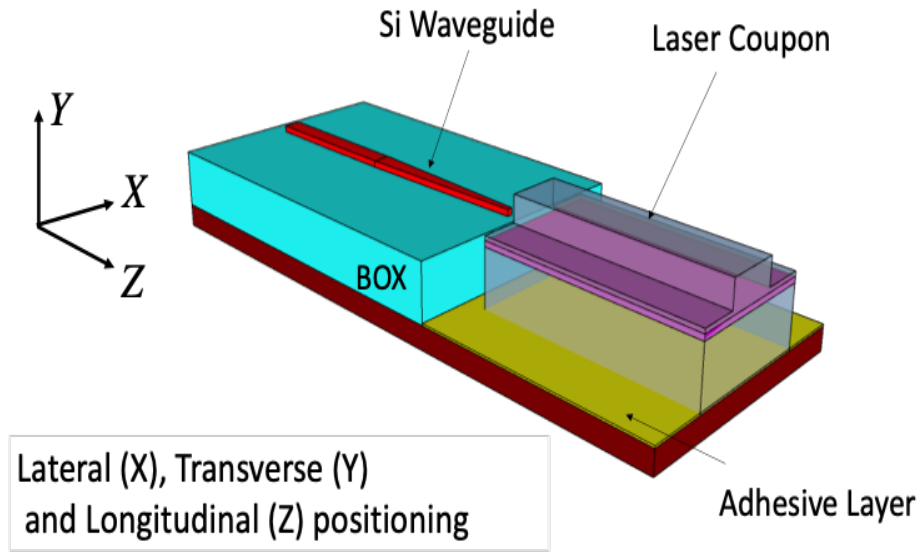


Figure 3.5: Schematic illustration of butt-coupling between an active device and receiving waveguide. The positioning of the laser with respect to the waveguide in X, Y and Z direction is critical for efficient light coupling.

The coupling efficiency is given as the fraction of the total power of the light source that is coupled into the waveguide. The coupling efficiency between a laser and a waveguide through edge-coupling can be expressed as the product of two factors; the modal overlap between the III-V laser mode and the edge coupler mode at the waveguide facet (η_1) and the mode conversion efficiency of the coupler from the superimposed mode at the facet to the final waveguide (η_2) as shown in eq. 3.1 [119].

$$\eta = \eta_1 * \eta_2 \quad (3.1)$$

The modal overlap efficiency (η_1) when there is a single dominant mode can be defined as eq. 3.2 [120].

$$\eta_1 = \frac{|\int E_1 * E_2 dA|^2}{\int |E_1|^2 dA * \int |E_2|^2 dA} \quad (3.2)$$

where E_1 and E_2 are the electric fields of the optical modes in the facets of the laser and waveguide, respectively, and A is the area of the modal distribution. The coupling efficiency can be maximised when the mode at the SOI facet is spatially matched to that of the laser. The mode conversion efficiency (η_2) quantifies the extent of light conversion from the SOI waveguide facet to the tapered waveguides. This efficiency is determined by tuning the length and width of the taper structure assuming no reflection loss. Among these, η_1 primarily determines the overall coupling efficiency, making η_2 a secondary factor. More details on the design and optimisation of the tapers are provided in the next section. We can also represent the coupling efficiency in terms of dB as a coupling loss:

$$\text{Coupling Efficiency (dB)} = 10 \cdot \log_{10} \left(\frac{P_{\text{out}}}{P_{\text{in}}} \right) \quad (3.3)$$

where P_{out} is the power delivered by the laser and P_{in} is the power coupled into the waveguide. Thus, the coupling efficiencies between the laser and the waveguides presented later in chapter-6 are calculated as according to 3.3.

This approach can be applied for waveguide sizes ranging from a few 100 nm to a few microns. Here, the edge-emitting QD lasers are integrated on a number of different edge-coupled waveguide platforms. These edge-coupling configurations are based on (a) 220 nm SOI, (b) 3 μm SOI and (c) 300 nm SiN with SU-8 polymer SSC. The simulated electric field profiles of the fundamental TE mode at the facet of the QD laser and the corresponding waveguides at a wavelength of 1310 nm are shown in Fig. 3.6. The mode size in the QD region of a laser with a 3 μm wide ridge is 0.99 μm in the vertical direction and 4.1 μm in the lateral direction. The mode profiles of the different waveguides show the mismatch between the modes at the laser and the couplers.

In the next section, the design and fabrication process of the investigated waveguide platforms is explained, together with the various figures of merit for each configuration, including coupling efficiency, misalignment tolerance, and manufacturing and integration complexity.

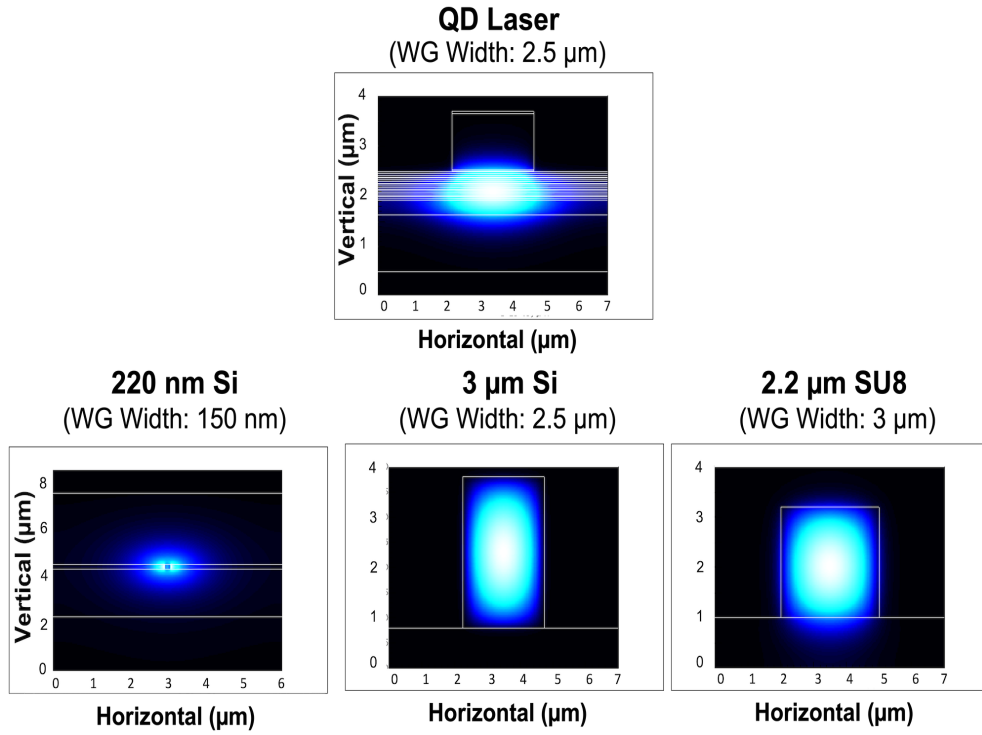


Figure 3.6: Simulated electric field profiles of the fundamental TE mode at the facet of the QD laser and the respective waveguides at the wavelength of 1310 nm.

3.2.1 220 nm SOI Waveguide

The first platform is based on imec's iSiPP50G technology [121] and consists of a 220 nm thick crystalline Si device layer. The SOI consists of a 2 μm buried oxide layer and a ~5 μm SiO₂ over-cladding. The rectangular trenches are 120 μm wide and 2.5 mm long and are formed by a two-step etch to accommodate the laser coupons for edge coupling of the light signal into the Si waveguide. The trenches are about 7 μm deep and are precisely stopped at the Si-substrate interface. A top view of the recesses with 280 vertical pitches μm is shown in Fig. 3.7(a). The spacing between the recesses depends on a number of factors, including foundry density rules and the uniformity of the adhesive spray coating. The Si waveguides are terminated by the surface grating couplers placed 600 μm away from the SOI facet as shown in Fig. 3.7(a). Figure 3.7(b) shows zoomed view of the surface grating couplers and transfer-print alignment markers. The light coupled in the waveguide is collected from a fibre by these grating structures. The grating coupler design is taken from imec's standard 220 nm waveguide library. Reference test structures with this surface grating are defined at both ends of the waveguide with different lengths across the wafer for calibration purposes.

The 300 mm SOI wafers are fabricated on a standard silicon-on-insulator platform at imec as part of the CALADAN project [7]. A zoom-in photo of one end of the recess is shown in Fig. 3.8(a). A pair of T-shaped alignment markers along both sides of the

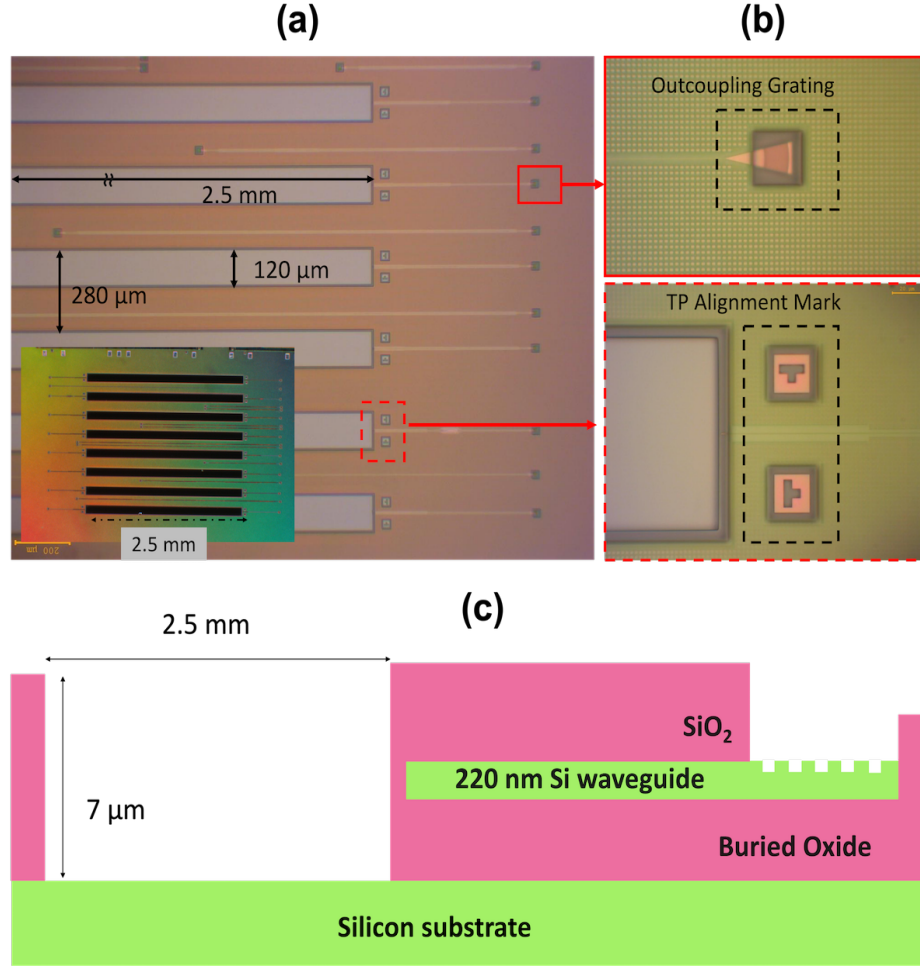


Figure 3.7: (a) Planar optical microscope image of the $7\ \mu\text{m}$ deep recesses defined in the SOI. The recesses are $120\ \mu\text{m}$ wide and $2.5\ \text{mm}$ long with a vertical pitch of $280\ \mu\text{m}$. The inset shows a zoomed view of the recesses. (b) The receiving waveguides are terminated with a surface grating coupler (top) and T-shaped transfer-print alignment markers (bottom) that allow automatic alignment of the coupon to the waveguide during integration. (c) Schematic cross section showing a recess, waveguide and grating coupler.

waveguide (as seen in Fig. 3.8(a)) are placed next to the recess to be used during transfer printing to determine the position of the laser relative to the Si waveguide. A similar marker is defined on the emitting side of the laser coupon. The width of the Si waveguide is $380\ \text{nm}$ in the non-tapered region. The Si waveguide is $220\ \text{nm}$ thick and the center height is $2.1\ \mu\text{m}$ from the Si substrate. A schematic cross-section is given in Fig. 3.8(b) and (d). The width of the Si waveguide is tapered down to $150\ \text{nm}$ at the SOI facet to improve coupling performance as given in Fig. 3.10(a). The facet profile on the SOI after the deep etch down to the Si substrate shows a 83.5° angle.

Different Si receiving waveguides are designed with single, double, and triple tips on the same SOI. Figure 3.9(a)-(c) show the schematic diagram of the Si coupler designs with their cross-section at the waveguide tip (left) and a plan view (right). The waveguide width is tapered down to $150\ \text{nm}$ toward the SOI facet to expand the mode

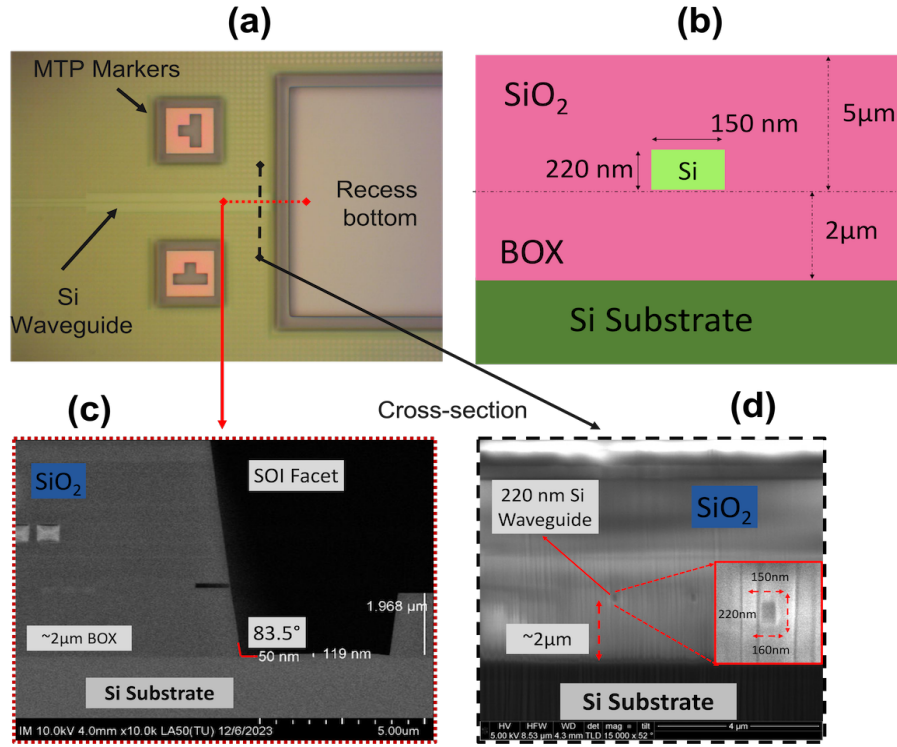


Figure 3.8: (a) A zoom of the SOI facet with transfer-printing alignment marks. (b) Schematic cross-section of the SOI waveguide with a single tip at the taper start (along the black dashed line) of the waveguide showing the 2 μm BOX layer with 5 μm SiO₂ overclad. (c) and (d) show FIB cross sections parallel and perpendicular to the Si waveguide near the tip. The SOI facet has a profile with an angle of 83.5. The center of the 220 nm thick Si waveguide from the Si substrate is $\sim 2.1 \mu\text{m}$ high.

and reduce its effective index close to that of SiO₂ for a better mode size matching and an improved misalignment tolerance for all designs. In addition, multi-tip waveguides, which enlarge the modal overlap efficiency, are joined into a final waveguide by one or two stage tapered coupler. The taper lengths in these sections are the same as the tapered waveguides at the coupler tips and are 100 μm . The final Si waveguide width is 380 nm. A multi-tip taper with multiple tips can relax the alignment requirements and increase the tolerance for larger misalignment and manufacturing variations. The superimposed mode profiles on the coupler facets are given for the design in Fig. 3.9(d). The coupling efficiencies and misalignment tolerances for each configuration are simulated in FIMMWAVE [122] and LUMERICAL MODE [100].

Firstly, the Si waveguide dimensions, including tip width and spacing between adjacent waveguides, were simulated for each design to achieve a coupler that gives maximum performance with low loss optical coupling and flexible alignment tolerance. The first step is to determine the optimum width of the tapered tip. The light source for all these simulations is a QD laser with 3 μm ridges. Figure 3.10(a) shows the coupling efficiency as a function of the taper tip width for the inverse single-tip tapered coupler. The coupling reaches its maximum value of 65% when the tip width is between 150 and 160 nm when the waveguide is tapered up to 380 nm

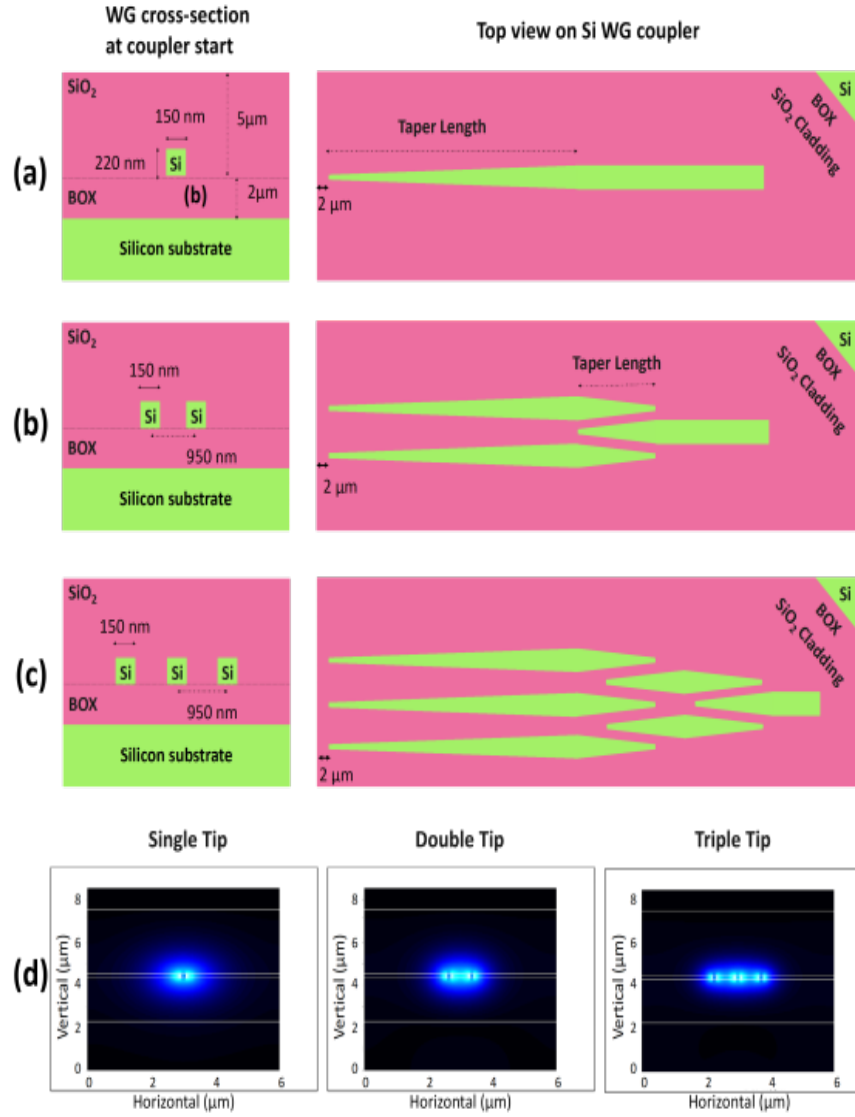


Figure 3.9: Schematic of (a) single, (b) double and (c) triple tip Si waveguides inverse tapered from 150 nm to 380 nm over a distance of 100 μm distance. The waveguide tips are recessed from the etched facet by 2 μm. Double and triple waveguides are combined into a final waveguide with one or two stage inverse taper coupling structures. (d) The electric field distribution of the single, double and triple tip edge couplers, respectively.

over 100 μm. The length of the taper is fixed to 100 μm for all designs. The same taper tip width of 150 nm is then used to determine the optimal distance between adjacent tips in multi-tip designs. The coupling efficiency curves as a function of taper tip spacing with a constant taper tip of 150 nm are shown in Fig. 3.10(b) and (c) for double and triple tip coupler designs, respectively. A gap of 800 nm (center to center gap is 950 nm) is selected for both couplers.

It should be noted that the reported coupling efficiencies are based on the assumption that there is no lateral or vertical misalignment between the laser and the Si waveguide. The misalignment tolerances in these directions are simulated separately.

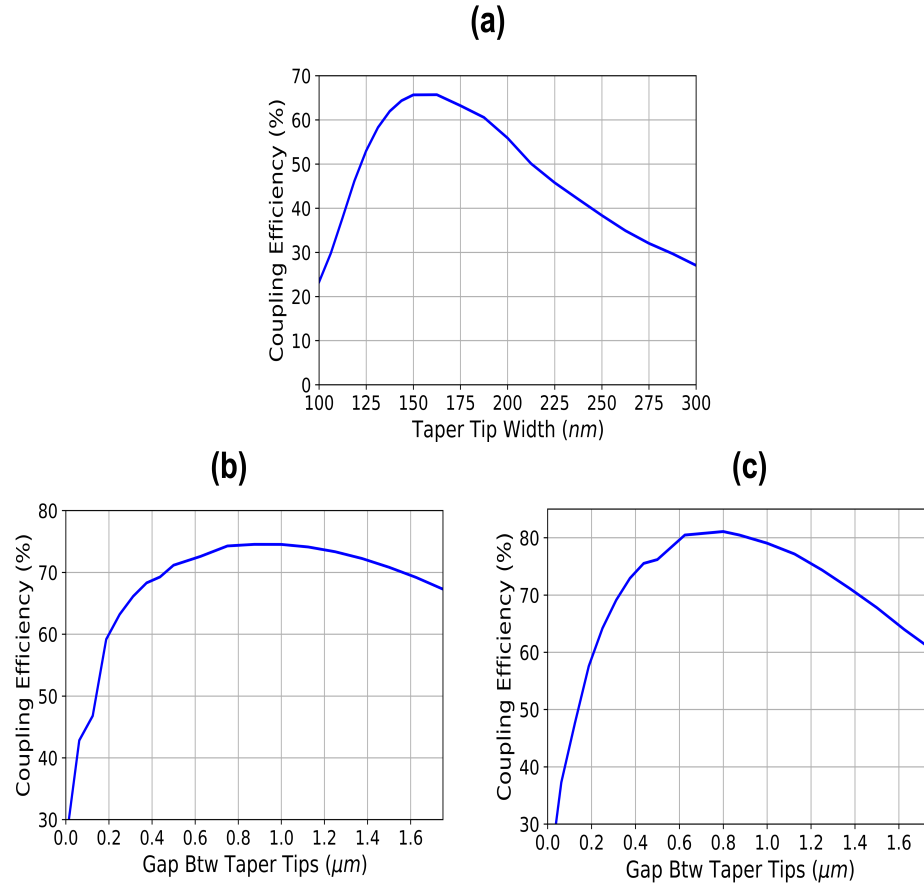


Figure 3.10: (a) Mode coupling efficiency between a 3 μm ridge laser and 220 nm Si waveguide as a function of taper width for the inverse taper single tip design. A taper tip around 150 nm wide gives maximum coupling. Using a 150 nm wide taper, the distance between multiple taper tips is simulated for (b) double and (c) triple tip couplers.

All simulation results refer to a constant QD laser ridge width of 3 μm . The 3 dB lateral misalignment tolerance for the single-tip design is simulated as $\pm 1.27 \mu\text{m}$. Couplers with multiple tips, similar to that of a trident fork, show improved performance in terms of both coupling efficiency and lateral misalignment tolerance compared to a single-tip coupler design with the same tip width. This is due to the improved modal overlap between the laser and receiving waveguide modes, as explained above. Coupling efficiencies of 75% and 80% are simulated for double- and triple-tip Si couplers, respectively, under the same assumption of no misalignment in the lateral or vertical direction. The 3 dB lateral misalignment tolerances for these coupler designs are $\pm 1.32 \mu\text{m}$ and $\pm 1.39 \mu\text{m}$. The width of the tapered tips in the multiple-tip coupler is 150 nm , the same as in the single coupler, with an 800 nm gap between the adjacent waveguides. The coupling efficiencies as a function of lateral and vertical misalignment are shown in Fig. 3.11(a) and (b) for the 3 different coupler types. Given the positioning accuracy of $<1 \mu\text{m}$ achievable during MTP integration, all designs provide sufficient lateral tolerance.

The 3 dB vertical tolerances are about $0.637 \mu\text{m}$ for single tips, $0.541 \mu\text{m}$ for double tips, and $0.481 \mu\text{m}$ for triple tips. This is due to the strong vertical mode confinement of the QD active layers. It is easy to see that vertical alignment is the most sensitive dimension, as a few 100 nm misalignment between the laser and the Si waveguide can cause a significant loss. However, vertical alignment can be tailored by precise control of epilayer thickness and Si etch depth with $\pm 100 \text{ nm}$. The bonding layer for transfer printing would be another parameter that could be tuned to minimise misalignment in the vertical direction.

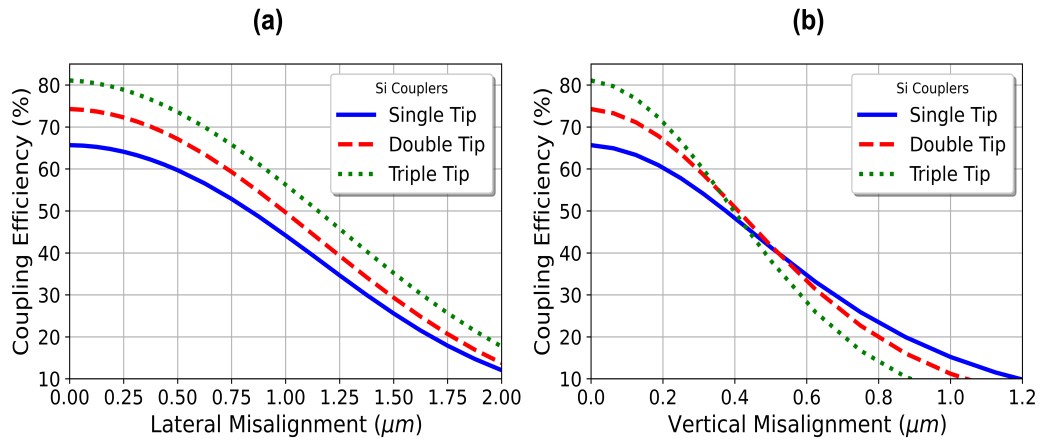


Figure 3.11: Simulated coupling efficiencies versus (a) lateral and (b) vertical positioning of waveguides with respect to the laser ridge.

Another misalignment is in the longitudinal direction, corresponding to the distance between the SOI facets and the laser. The lateral and vertical misalignment plots shown in Fig. 3.11 assume that the longitudinal misalignment is 0. However, since the Si waveguide tips are $2 \mu\text{m}$ recessed from the SOI facet, there is a minimum longitudinal gap of $2 \mu\text{m}$ from the waveguide tip to the SOI facet filled with SiO_2 . This results in a gap of $>2 \mu\text{m}$ between the laser and the waveguide in the best case. This is due to the process design rule that aims to avoid any damage to the waveguide facet. In the final loop SOI wafer, this gap is reduced to $\sim 1 \mu\text{m}$. In reality, this gap would be more due to a tilted profile of the SOI facet (as seen in Fig. 3.8(c)), the transfer printing placement limitation ($< 2 \mu\text{m}$) and the laser design-related extension such as a few microns of patio around the laser (see 2.3.2 for more details). However, filling the gap with an index-matching material would increase the efficiency of light coupling, as shown in Fig. 3.12(a). The coupling efficiencies as a function of longitudinal misalignment when the gap is filled with air ($n = 1$) and polymer (Norland 61 UV-sensitive fibre adhesive with a refractive index of 1.56 [123]) simulate an improvement of around 20% at $2 \mu\text{m}$ longitudinal misalignment. The polymer requires 4 minutes of exposure to a 365 nm LED to fully cure. The oscillation in the coupling curve when the gap is filled by air is due to an undesired FP modes formed between the facets and can be reduced by infill. However, it is challenging to

have a repeatable and reliable filling process as it is difficult to ensure that there is no airlock between the facets. Despite the higher coupling efficiency of multi-tip coupler designs with $>2 \mu\text{m}$ polymer filled gap, all designs show a similar coupling efficiency in the 50-55% range as seen in Fig. 3.12(b). Thus, a similar performance would be expected in all three coupler designs. In fact, the measurement results indicate that all designs have comparable coupling performance as discussed in chapter 5. In this work, longitudinal misalignment contributes the most loss for this platform, given the achieved alignment accuracy of $<0.5 \mu\text{m}$ in the lateral direction and $<0.2 \mu\text{m}$ in the vertical direction.

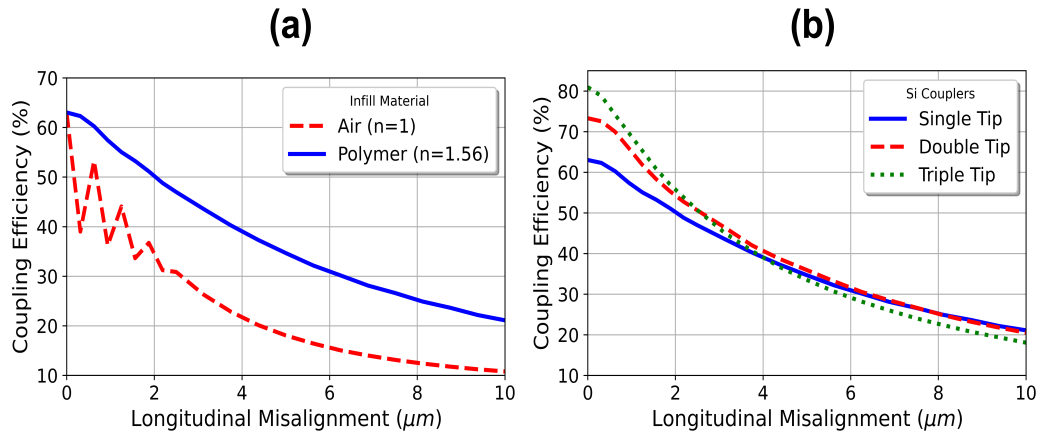


Figure 3.12: (a) Coupling efficiencies versus longitudinal misalignment due to the gap between laser and SOI facets when the gap filled with air and polymer for single tip coupler. (b) Comparison of coupling performance for three coupler designs with respect to longitudinal misalignment.

Although the thickness of the n-cladding (mode-center height from the bottom surface of the n-GaAs layer after etching) in the epitaxial layers and the height of the Si waveguide center from the Si substrate are considered in the design of both structures, a cross section check is performed to verify the actual alignment in the vertical direction. Figure 3.13 shows the measured and simulated center height of the mode from the bottom surface for the III-V and SOI layers. In both structures, the mode center is around $2.1 \mu\text{m}$ from the bottom surface. There would be $\pm 100 \text{ nm}$ variation in the simulated center due to the potential fabrication variation in SOI (i.e. the BOX layer etching may result in a shallow or over-etch on the Si substrate) and variation in the adhesive layer thickness spray-coated prior to laser integration.

A summary table comparing the tolerance for 3 dB misalignment of the different coupler designs is given in table-3.1. The tolerance of 3 dB misalignment in the lateral and vertical directions is compared together with the simulated coupling efficiencies with a longitudinal gap of $2 \mu\text{m}$ filled with SiO_2 as explained above. All coupler designs provide more than $1 \mu\text{m}$ tolerance in the lateral direction, with the triple-tip coupler being the most relaxed design as expected. The misalignment is assumed to be 0 in the other direction when the tolerance is simulated. Vertical

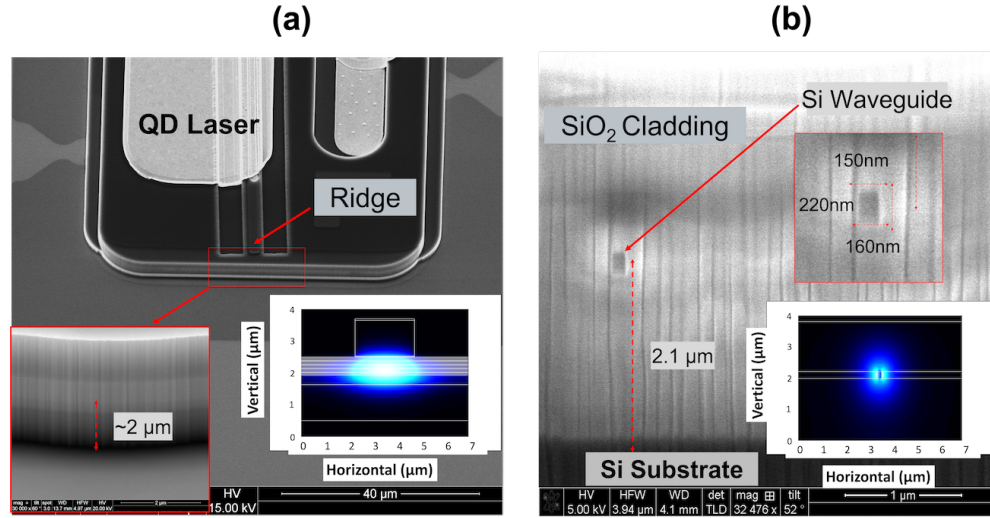


Figure 3.13: (a) SEM image of the front facet for a QD laser on GaAs substrate. Left-Inset shows a zoom-in on facet showing the center height of QD active layer to coupon bottom after MTP. Right-Inset shows the simulated mode center for QD laser and the mode profile. (b) The mode center in 220 nm Si waveguide is 2.1 μm from the Si substrate. Insets show the mode profile in the waveguide (bottom) and measured dimension of waveguide around the tip (top).

tolerances are also comparable and below 0.6 μm . The coupling efficiencies with a minimal 2 μm longitudinal gap indicate that all designs have similar performance when using a laser with 3 μm ridge.

Designs	Lateral (μm)	Vertical (μm)	CE (with 2 μm Longitudinal Offset)
Single Tip	± 1.27	± 0.62	50% (-3.0 dB)
Double Tip	± 1.32	± 0.54	54% (-2.67 dB)
Triple Tip	± 1.4	± 0.48	56% (-2.52 dB)

Table 3.1: Comparison of the different couplers designs based on 220 nm SOI. For better comparison, the 3 dB misalignment of the designs are calculated assuming the same misalignment (0 misalignment for lateral and vertical) but the coupling efficiencies are with the 2 μm longitudinal misalignment.

The main advantage of edge-coupling on this platform is its compatibility with the foundry using imec's 300 mm silicon photonics line, which increases its potential for commercialisation in various products. In addition, the integration of lasers with a thin layer of BCB on the substrate ensures efficient heat dissipation because of the proximity of the devices to the Si substrate. However, the technical challenges including adhesive pooling towards the cavity sidewall, which is discussed in detail in section 4.2.2.2, and the need for infill for longitudinal spacing are listed as some drawbacks of this platform that need to be addressed to improve coupling efficiencies.

3.2.2 3 μm SOI Waveguide

The second platform considered is a 3 μm thick silicon waveguide with a 1 μm BOX layer, as used by VTT [124, 125]. This platform configuration is known for its low

propagation loss, low polarisation dependence, and ability to tolerate high power compared to sub-micron Si waveguide. In this thesis, fully etched ridge waveguides are fabricated in a single step process at Tyndall. Figure 3.14(a) shows the schematic side view of the Si waveguide. The final waveguide is $3\ \mu\text{m}$ thick and $2.5\ \mu\text{m}$ wide, as shown in Fig. 3.14(b). There is no taper structure in this waveguide. An SEM image shown in Fig. 3.14(c) shows the sidewall quality achieved on the waveguide. The facet where the light is coupled to the waveguide is defined by dry etching. The other end of the waveguide is cleaved after laser integration to capture the light. Emitting facet of the transfer-printed lasers next to the Si waveguide is shown in Fig. 3.14(d).

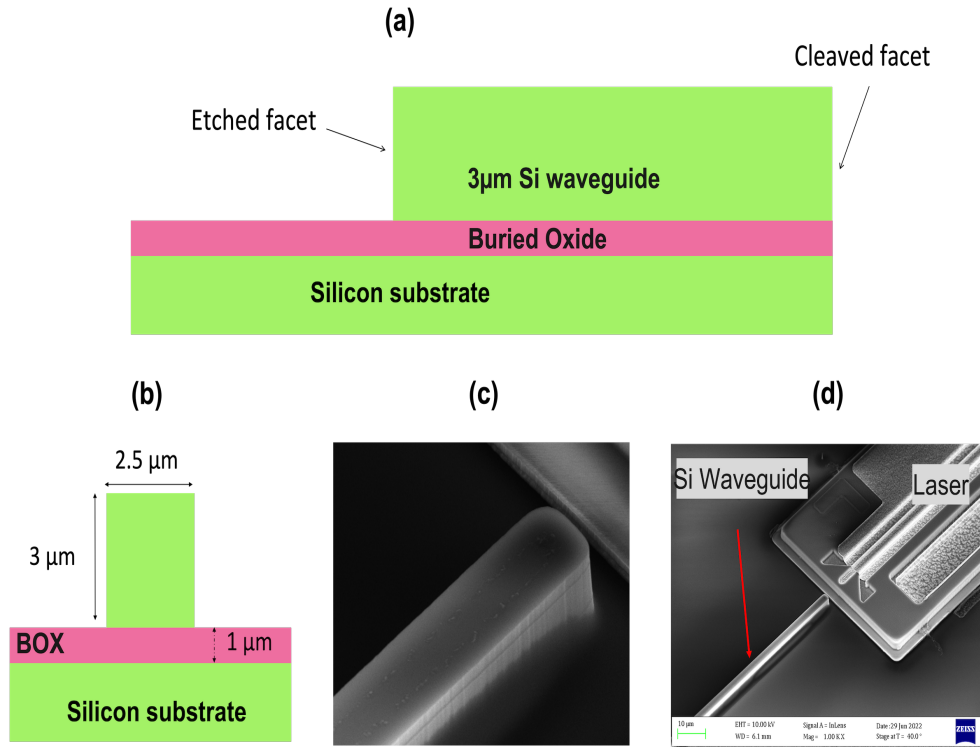


Figure 3.14: (a) Schematic of side-view for 3 micron Si waveguide on $1\ \mu\text{m}$ thick BOX layer. (b) Cross section of the waveguide perpendicular to propagation direction shows fully etched waveguide is $2.5\ \mu\text{m}$ wide. (c) Sidewall of the waveguide after the Si etch. (d) QD laser transfer-printed next to the $3\ \mu\text{m}$ waveguide.

The coupling efficiency between a QD laser with a $3\ \mu\text{m}$ wide waveguide into a $2.5\ \mu\text{m}$ wide deep-etched receiving Si waveguide is simulated to be 50% without any misalignment. This platform provides a $3\ \text{dB}$ positioning tolerance of $1.3\ \mu\text{m}$ in the lateral direction and $0.8\ \mu\text{m}$ in the vertical direction, as shown in the coupling efficiency with respect to misalignment in Fig. 3.15(a). There is a default mismatch of $0.67\ \mu\text{m}$ in the vertical direction between the modes in the QD laser with respect to the Si waveguide. This is due to the difference between the mode center in the laser ($2.1\ \mu\text{m} + 0.07\ \mu\text{m}$ BCB adhesive layer) and Si waveguide ($1.5\ \mu\text{m}$). The maximum coupling efficiency is 32% when including the vertical misalignment achieved. However, a better vertical alignment could be achieved by adjusting the etch depth in

the BOX layer without changing the laser epitaxial structure. In this work, there is no over-etching in the BOX layer implemented.

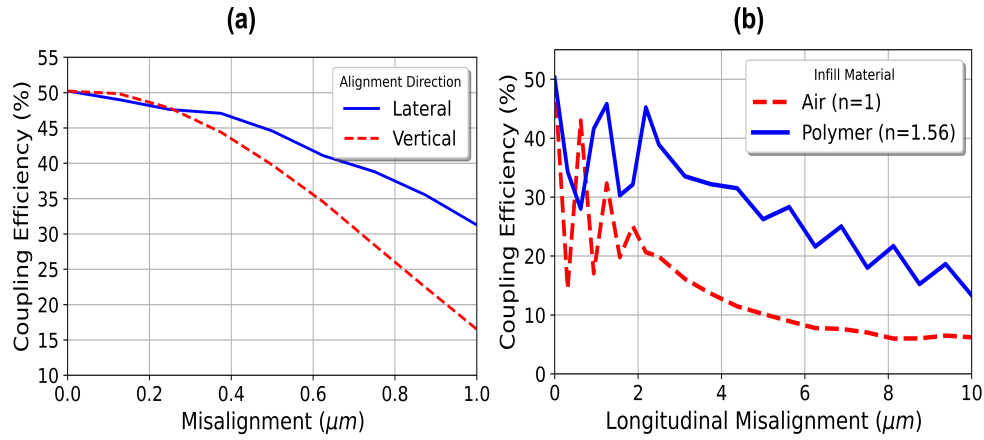


Figure 3.15: (a) Simulated coupling efficiency as a function of misalignment in lateral and vertical direction. (b) Coupling into the fundamental mode versus longitudinal misalignment between laser and Si waveguide with air and polymer in-fill.

Similarly to the 220 nm SOI, an infill is required between the transmitting and receiving facets to improve the coupling efficiency. The same optical adhesive is applied to the laser-waveguide interface to minimise coupling losses. In addition, the formation of cavities in the gap between the two facets, which leads to the strong reflections that cause the kink in the coupling efficiency versus longitudinal gap plot shown in Fig. 3.15(b), can be reduced. The longitudinal alignment of 3 μm , which gives about 35% coupling efficiency, is achieved in this platform due to the 2.5 μm ledge on the laser front facet. However, the longitudinal alignment would be improved with a ledge-less laser coupon.

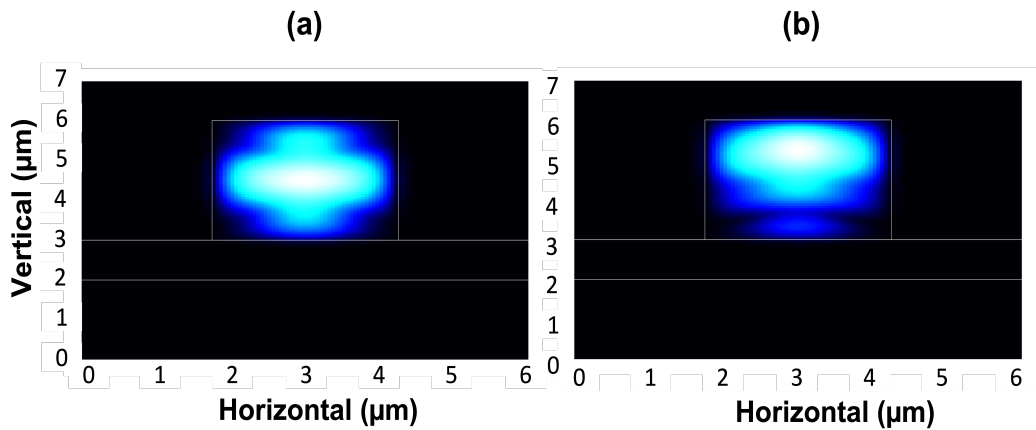


Figure 3.16: Simulated TE polarized electric field (E_x) profiles of the exited mode in the waveguide after light-coupling from laser to waveguide with (a) no misalignment and (b) 0.67 μm misalignment in vertical direction.

A vertical misalignment would cause additional loss due to higher-order modes in the waveguide being excited because it supports their propagation. The electric field of

(E_x) of the excited mode in the Si waveguide when the light is coupled to the receiving waveguide with a vertical misalignment of 0 and $0.67 \mu m$ is given in Fig. 3.16(a) and (b), respectively. Better vertical alignment also improves mode overlap and prevents higher-order modes from being excited in the waveguide. In addition, this design provides a relatively poorer thermal conductivity when the laser is integrated directly on the BOX layer, as it has a much lower thermal conductivity than Si. However, by properly designing the epitaxial stack, the laser could be transferred to the Si substrate (with or without an adhesive layer) after removal of the BOX layer. The need for an index-matching infill between the laser and the waveguide can be listed as another drawback, as it introduces an extra step after laser integration and repeatability issues. The simple fabrication steps are two major advantages of this platform.

3.2.3 300 nm SiN & SU8 Polymer Waveguide

The final platform investigated in this thesis is the 300 nm SiN waveguide combined with an SU-8 polymer waveguide. Unlike the first two edge couplers, this design uses an SU-8 polymer spot size converter (SSC) [114, 126] where the light is first edge coupled from the laser into the SU-8 waveguide and then evanescently coupled from the SU-8 waveguide to the underlying SiN waveguide. The evanescent coupling between the SU8 and SiN waveguide layers is achieved by an adiabatic taper structure where the SU8 is tapered downwards and the SiN is tapered upwards [127, 128]. Figure 3.17 shows a top and side view schematic of this platform with an integrated laser.

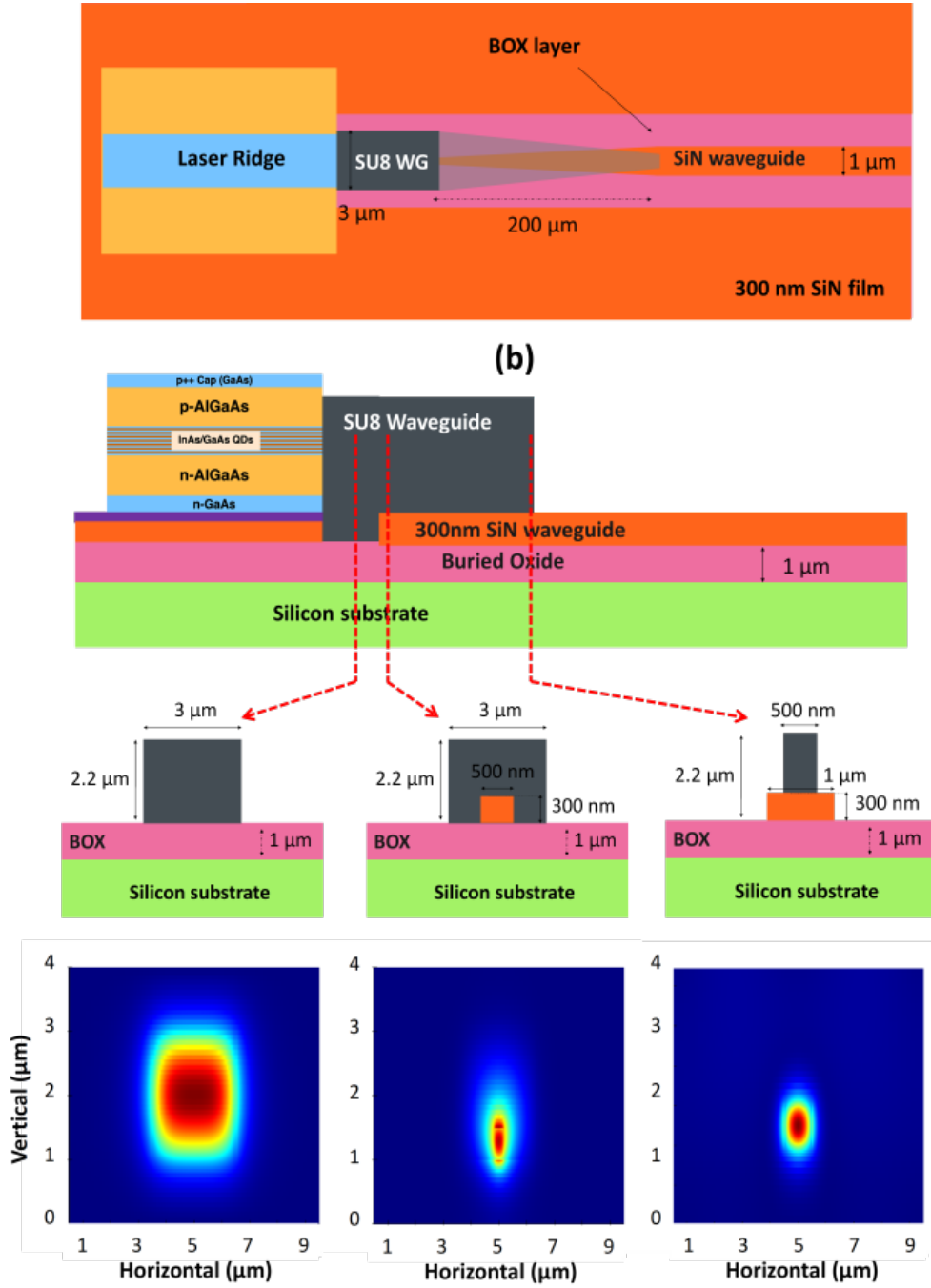


Figure 3.17: (a) Top view of the platform including integrated QD laser, SU-8 and SiN waveguide arrangement. (b) Light coupling schematic from laser to SU-8 polymer waveguide and SiN waveguide. Light from the cleaved end of 4 mm long SiN waveguide is collected. Cross-section of the SU-8 & SiN waveguides at different location and the corresponding the electric field distribution.

The waveguide consists of a 300 nm thick SiN waveguide layer deposited on a 1 μm BOX layer on a Si substrate. The 1 μm wide waveguides are first defined by dry etching 2 μm wide trenches around them following e-beam patterning. The SiN waveguide is tapered from 1 μm to 0.5 μm over 200 μm toward the laser facet. In this step, the alignment marks for transfer printing are also defined. The QD lasers are

then transfer-printed 10 μm away from the SiN waveguide tip after 70 nm BCB spin-coating as an adhesive layer. Figure 3.18(a) shows an optical image of the SiN waveguide with transferred laser on this platform. The inset shows a magnified image of the SiN waveguide tip. SU-8 polymer is spin coated after BCB curing following laser transfer printing. The SU-8 waveguides are then defined by e-beam exposure. Although the target thickness was 3 μm , the resulting SU-8 waveguide thickness is measured at 2.2 μm . This could be due to the spin coating parameters and the shrinkage of the polymer during the post-exposure bake. The polymer waveguide consists of a straight section with a constant width of 3 μm and a tapered section narrowed down to 0.5 μm . Figure 3.18(b) shows an SEM image of an SU-8 waveguide starting from the laser facets and ending 200 μm away over the SiN waveguide where its width reaches 1 μm .

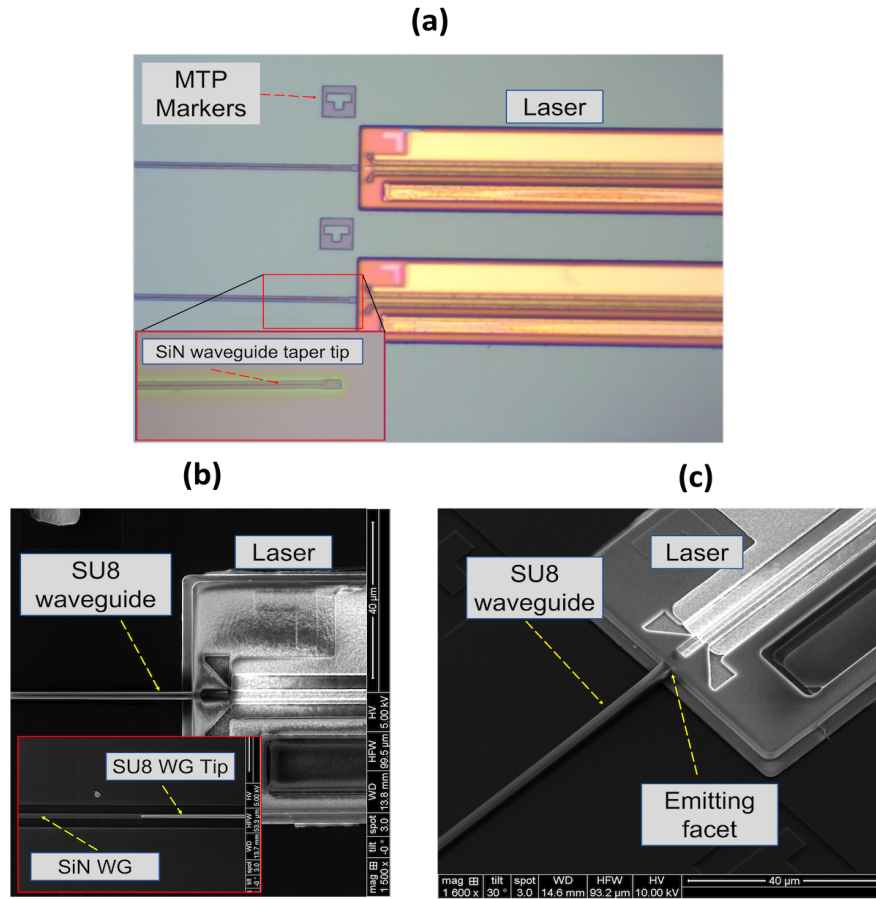


Figure 3.18: (a) Transfer-printed laser on 70 nm BCB layer after SiN waveguide definition. The inset shows the SiN waveguide tip tapered from 1 μm down to 500 nm over 200 μm distance. (b) SEM image of a laser after SU-8 polymer waveguide definition. There is no gap between the laser facet and receiving SU-8 polymer waveguide. The inset shows the termination tip of SU-8 waveguide on top of the μm . (c) SEM images of laser SU-8 waveguides defined on QD lasers. There is no air gap between the two facets.

The simulated coupling efficiency in this configuration is approximately 35% as shown in Fig. 3.19(a). The transmission from the laser to the SU-8 waveguide (35%) limits

the total coupling, with the simulated coupling from the SU-8 SSC to the underlying SiN waveguide being $> 90\%$ as given in Fig. 3.19(b). Simulation suggests that the laser-to-SU-8 waveguide coupling could be increased to 50% simply by increasing the polymer thickness to $3\ \mu\text{m}$. The positioning tolerances for 3 dB excess loss in the lateral and vertical directions are $1.25\ \mu\text{m}$ and $0.75\ \mu\text{m}$, respectively. Here, the vertical mismatch is $\sim 0.7\ \mu\text{m}$ given the difference in the centre of the modes between the laser ($2.17\ \mu\text{m}$ including the BCB adhesive layer) and the SU-8 waveguide at the laser-SU-8 interface ($1.5\ \mu\text{m}$ including the waveguide climbs over the remaining n-GaAs layer of $\sim 400\ \text{nm}$).

However, a better vertical alignment could be achieved by adjusting the etch depth into the BOX layer or engineering the SU-8 waveguide thickness for higher modal overlap without any changes in laser epitaxial structure. In this thesis, the laser is transfer-printed onto the $1\ \mu\text{m}$ thick BOX layer without over-etching toward the Si substrate.

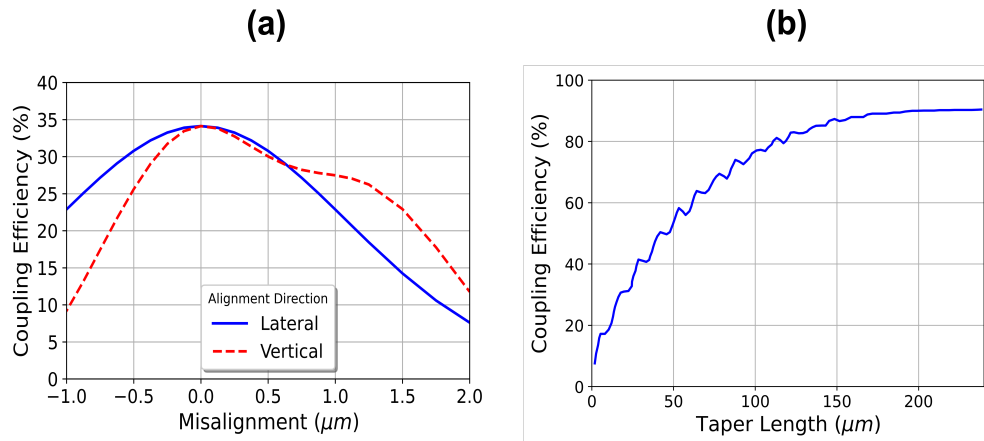


Figure 3.19: (a) Simulated coupling efficiency as a function of misalignment in lateral and vertical direction. (b) TE polarized E_x profiles of the exited mode in the waveguide after light-coupling from laser to waveguide with $0.7\ \mu\text{m}$ misalignment in vertical direction.

There is no longitudinal spacing between the emitting facet and SiN waveguide as the SU-8 polymer waveguide starts from the laser facet as seen in Fig. 3.18 (c). As long as there is no misalignment in the polymer patterning step (optical lithography or e-beam exposure), no in-fill application is required in this configuration.

3.3 Conclusion

The design and simulation of the waveguide platforms studied are discussed in this chapter. A summary and comparison of these platforms is given in table-3.2. The first platform is based on $220\ \text{nm}$ SOI with several microns deep trenches, which accommodates the QD lasers and facilitates edge coupling from the laser to the Si waveguide. In this platform, the Si coupler designs with different numbers of

waveguide tips are investigated. Overall, the edge-couplers demonstrate a simulated coupling efficiency of about 50%, including the default $2\ \mu\text{m}$ longitudinal misalignment. A $> 1\ \mu\text{m}$ lateral $3\ \text{dB}$ tolerance is demonstrated. The second platform is $3\ \mu\text{m}$ SOI with $2.5\ \mu\text{m}$ wide rectangular ridge waveguides with a relatively simple fabrication process. A coupling efficiency of 32% is simulated with a vertical misalignment of $0.67\ \mu\text{m}$. A $3\ \text{dB}$ positioning tolerance of $1.3\ \mu\text{m}$ in the lateral direction and $0.8\ \mu\text{m}$ in the vertical direction is simulated. The final platform is $300\ \text{nm}$ SiN waveguides using a polymer (SU-8) SSC to edge-couple the light first from the laser to the SU-8 waveguide and then evanescently couple from the SU-8 waveguide to the SiN waveguide through adiabatic tapers. The coupling efficiency of 35% is simulated in this configuration. The overall coupling efficiency is limited by the coupling between the laser and the SU-8 waveguide, which is strongly dependent on the size of the SU-8 SSC (thickness and width). The resulting SU-8 waveguide is thinner than the target, which degrades vertical alignment. The $3\ \text{dB}$ positioning tolerances in the lateral and vertical directions are $1.25\ \mu\text{m}$ and $0.75\ \mu\text{m}$ respectively for this platform. The simulated coupling efficiencies after including the losses due to positioning misalignment are 11%, 15% and 12% for $220\ \text{nm}$, $3\ \mu\text{m}$ SOI, $3\ \mu\text{m}$ SOI and $300\ \text{nm}$ SiN platforms, respectively.

Key metrics	Waveguide Platforms		
	220 nm SOI	3 μm	SiN & SU8
Coupling Efficiency (% / dB)	54 / -2.76)	32 / -4.95)	35 / -4.55)
3 dB Misalignment Tolerance (Lateral / Vertical) (μm)	$\pm 1.32 / \pm 0.54$	$\pm 1.3 / \pm 0.8$	$\pm 1.25 / \pm 0.75$
Scale production	● ● ●	● ●	● ●
R&D and Prototyping	● ●	● ● ●	● ● ●
Fabrication complexity	● ● ●	●	● ●
Heat dissipation	● ● ●	●	●
Adhesive accumulation	● ● ●	●	●
Longitudinal Misalignment	● ● ●	● ●	●
Coupling to higher-order mode	●	● ●	● ●
● - Low / Poor, ● ● - Medium, ● ● ● - High / Good			

Table 3.2: Comparison of the different edge-coupling configuration on the investigated platform in this thesis.

From simulations with the best possible alignment at integration, it can be concluded that all three edge coupling configurations would result in similar coupling performance. Considering the actual misalignment achieved after integration, there is room for improvement in all platforms. For example, reducing longitudinal misalignment in $220\ \text{nm}$ SOI and improving vertical alignment in $3\ \mu\text{m}$ and $300\ \text{nm}$ SiN platforms could result in better light coupling efficiency. A key advantage of the

220 nm SOI platform is its potential for mass production, as it is compatible with imec's 300 mm silicon photonics line. The relatively simple fabrication process of the 3 μm and 300 nm SiN platforms could be an advantage for R&D and prototyping, followed by a smooth transition to volume production. In addition, the thin Si waveguide platform offers the best heat dissipation because the laser coupons are printed on the Si substrate with a thin layer of adhesive. In contrast, the lasers are integrated on the remaining BOX layer, which reduces the heat sink and thus the degradation of device performance in the thick Si and SiN waveguide platform. However, better heat dissipation can be achieved in these platforms by reducing the thickness of the BOX layer with proper engineering of the integration configuration without any adjustment in the epitaxial layers. Longitudinal alignment can be challenging for 220 nm SOI due to the accumulation of adhesive on the side wall of the recess. This is addressed by the development of a ledge-laser and adhesive patterning process and is discussed in chapter-4. This is less of an issue for thick Si and SiN platforms, as they do not contain a recess for laser integration. When designing, it should be noted that the vertical misalignment could cause additional losses by exciting the higher-order modes more in 3 micron SOI and SU-8 waveguides, as these waveguides support higher-order mode propagation.

Chapter 4

Transfer Printing of Quantum Dot Lasers

This chapter describes the final steps needed to prepare the laser coupons on the source and the process of preparing the target wafers for transfer printing. The fabrication process of the QD lasers is described in chapter-2. One of the most important steps in the preparation of transfer-printable devices is the use of a special layer, called the sacrificial or release layer, which allows selective removal of the device structure from the native substrate. This process, called release etching, selectively removes the sacrificial layer, leaving the coupon suspended and supported by an anchoring system called tethers. The design of the tethers, along with other corresponding changes or additions required in the epitaxial growth and device fabrication process, is discussed in detail in chapter-2. The laser coupons are detached from their native GaAs substrate after release etching by removal of AlGaAs release layers with different Al contents in dilute HCl here.

The preparation of the host substrates for bonding with a polymer adhesive layer is then discussed. The need for a bonding layer in transfer-printing and the materials that can be used as an adhesive bonding layer are explained. The quality of the bonding interface between the coupon and the target substrate is critical to optimising the adhesive material coating and transfer-printing. In addition, the challenges that affect the proper transfer of lasers for edge coupling after adhesive coating on wafers with deep topography and the solution developed are discussed. Finally, the post-printing processes, which include photo-resist removal, adhesive curing, and bond testing, are explained.

4.1 Release Etch

Laser coupons are ready for integration by micro-transfer printing after the sacrificial layer is selectively removed while protecting the adjacent layers. Following this step, rectangular device coupons are detached from the native GaAs substrate and can be transferred to the host substrates. The aim is to achieve a flat and smooth bottom surface of the coupon to facilitate a high printing yield on the new substrate. It is critical to define what yield means in this thesis. The yield indicates the successful transfer printing rate of the coupons onto the target substrate. The yield does not take into account the misalignment achieved during integration or the functional performance of the devices.

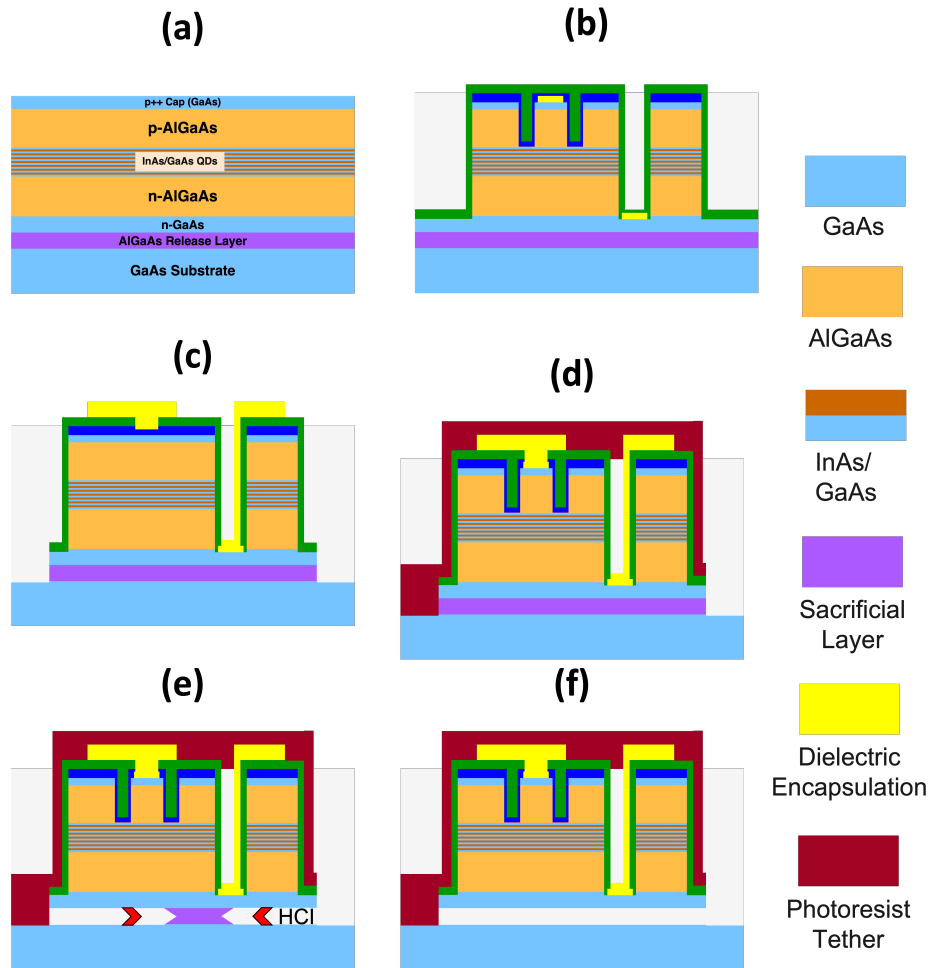


Figure 4.1: Process flow of coupon fabrication and release. (a) The initial III-V layer stack, (b) Definition of the device (ridges and facets) and first mesa and dielectric passivation, (c) Second mesa definition and etch through the sacrificial layer into substrate, (d) Tether definition using photo-resist, (e) Under etch of the release layer in HCl, (f) Ready device coupon for pick-up after sacrificial layer removal.

A number of different materials can be used as the sacrificial layer, such as AlInAs and InGaAs [45, 129] for InP and AlGaAs [130, 131], AlInP [132], InGaP [133] for GaAs-based devices. The sacrificial layer and corresponding etchant can be selected

considering the etch rate and selectivity to the adjacent layers in the epilayer stack. A 500 nm AlGaAs layer is chosen as the sacrificial layer in the epitaxial structure used in this work, as the ability to vary the aluminium (Al) content of AlGaAs provides great flexibility in tuning its etch properties to suit specific process requirements. A tether system is defined on the coupons to anchor the coupons to the source substrate during and after the release etch. Detailed discussion on tether design and related issues is presented in section 2.3.5.

The coupon preparation and release etching process is summarised in Figure 4.1. Detailed fabrication steps for QD lasers are presented in Appendix A. Briefly, the fabrication process starts with p-metal deposition. The ridge and facet definition is then completed in an ICP dry etch step. After bond metal evaporation, a dielectric layer is deposited by PECVD to protect the facets and epilayers from subsequent process steps. This layer, also called encapsulation, covers the coupon and prevents unwanted etching of all layers in the epi stack except the sacrificial layer. After tether definition, the coupon is ready for release etching.

500 nm thick $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer with high aluminium concentration ($x = 0.9, 0.93$ and 0.95) is used as a release layer. Traditionally, hydrofluoric acid (HF) has been used to wet-etch the AlGaAs sacrificial layer because of its high selectivity for GaAs. However, the formation of H_2 bubbles during this process can interfere with etching and damage the delicate device structure and lead to their collapse. In addition to the H_2 other gas phase by-products such as AsH_3 and low solubility etch products such as AlF_3 can also interfere with the etching process. However, HCl-based solutions have shown promise, demonstrating a higher selectivity between GaAs and $\text{Al}_x\text{Ga}_{1-x}$ layers with $x > 90\%$ and causes less damage to floating structures [134, 135]. In addition, the high selectivity of dilute HCl to dielectric encapsulation layers (SiO_2 and SiN) used in coupon fabrication is another advantage. Therefore, in this thesis, an HCl-based solution is chosen over HF to selectively wet-etch the high-Al composition $\text{Al}_x\text{Ga}_{1-x}$ layer with an x-value of > 0.9 . The first factor, the etch rate, is the amount of material that is etched laterally by the solution. The etch rate also depends on the crystallographic orientation of the coupons. Thus, coupons with different arrangement need to be evaluated. The other important parameter is selectivity, which is the ratio of the etch rates in the sacrificial layer to the cladding layer above and below it (which is GaAs in this case) and the encapsulation dielectrics and photo-resist. Higher selectivity is preferred to avoid infiltration into the device layers.

A number of chips with test coupon structures are fabricated with these release layers to investigate etch rates as a function of Al concentration and crystallographic dependence. Figure 4.2(a) illustrates the arrangement of the coupons with respect to the major flat. Each chip consists of 1 mm long rectangular coupons with varying widths from 50 to 200 μm and different orientation of 0° (or 90°) and 45° (or -45°)

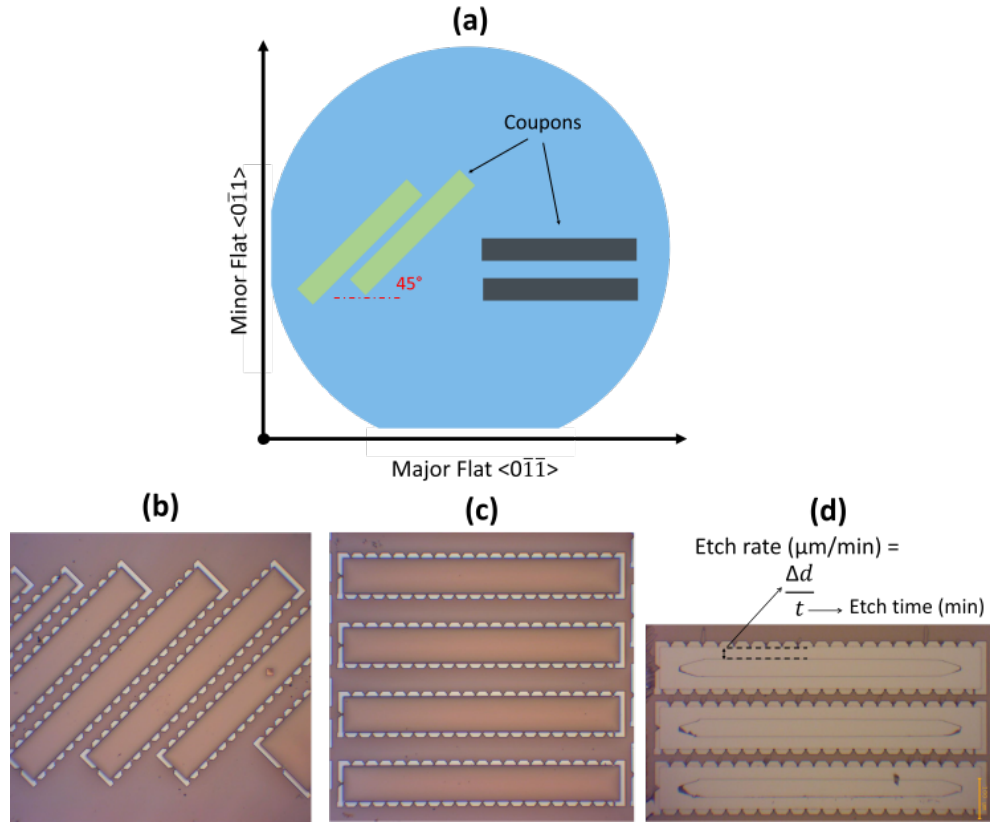


Figure 4.2: (a) Arrangement of the rectangular coupons with respect to the crystal planes of the wafer. Optical images of coupons ready for release etch on the same chip with (b) 45° and (c) 0° (parallel) orientation with respect to the major flat on GaAs substrate. (d) The etch rate is calculated by dividing the distance eroded by the solution (Δd) by the etch time (t).

with respect to the major flat as shown in Fig. 4.2(b) and (c), respectively. All samples have the same resist-based tether defined using SPR-220 photo-resist. The samples were then released in an HCl (37%) 1 to 1 de-ionized water (DI) dilution, HCl:DI (1:1), at 19°C for 25 min. The mixture was cooled for approximately 15 min and reached clean-room temperature. To measure the amount of undercut in the lateral direction, the fragile under-etched device layer is removed with Scotch tape, leaving only the epilayers above the remaining AlGaAs layer that connects it to the substrate in the center of the mesa. The result is a clear step that separates the undercut region from the rest. The boundary of the remaining part of the coupon at center of the mesa indicates how far the etch has progressed. The distance from the initial coupon boundary to the final boundary indicates the lateral etch depth. The etch rate is then determined by dividing the lateral etch depth (from the long side of the coupon) by the etch time as shown in Fig. 4.2(d). The lateral etch depth is measured at several locations to minimise variation in etch rate.

In addition, the etch rate in different planes, including the 0°, 45°, 90°, and -45° planes, was investigated using rectangular coupons defined on the GaAs samples. The samples were then immersed in HCl:DI (1:1) for 25 min to remove the sacrificial layer.

Figure 4.3(a) and (b) show the mesas before the release etch. The progress of sacrificial layer etching in $0^\circ/90^\circ$ and $45^\circ/-45^\circ$ directions on the mesas with 95% Al containing AlGaAs layer is shown in Fig. 4.3(c) and (d), respectively. The lateral etch depth was determined by measuring the distance between the initial mesa boundary (outer line) and the final mesa boundary after release and peeling of the undercut epilayer (inner line) as $\sim 41 \mu\text{m}$ and $\sim 56 \mu\text{m}$ in the $0^\circ/90^\circ$ and $45^\circ/-45^\circ$ directions. The corresponding etch rates are $1.64 \mu\text{m}/\text{min}$ and $2.24 \mu\text{m}/\text{min}$ for $0^\circ/90^\circ$ and $45^\circ/-45^\circ$ directions (with $\pm 0.15 \mu\text{m}/\text{min}$ experimental error), respectively.

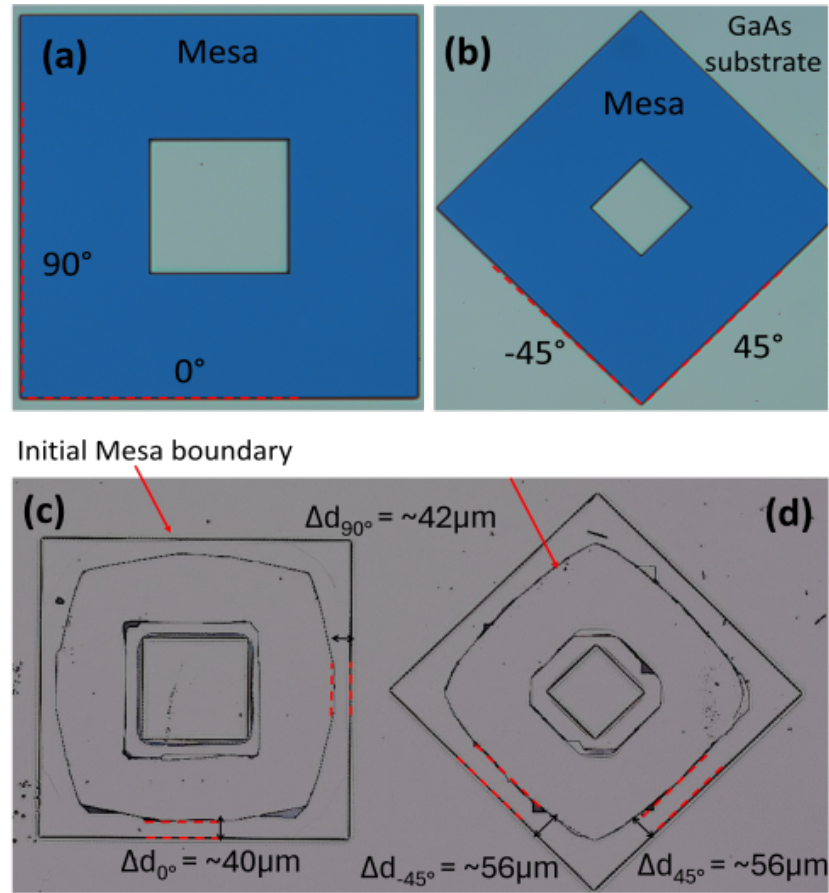


Figure 4.3: Optical images of rectangular mesas (a) parallel (and 90°) and (b) 45° (and -45°) rotated with respect to the major plane. The mesas are formed by etching down to the GaAs substrate and open the AlGaAs release layer, which contains 95% Al. The release etch is performed in HCl:DI (1:1) at 19°C for 25 min. The undercut part of the coupons is removed with a tape. The red dotted line indicates the initial coupon boundary and the progress of etchant for planes at (c) parallel (and 90°) and (b) 45° (and -45°) rotation.

The etch rates of $\text{Al}_x\text{Ga}_{1-x}\text{As}$ sacrificial layers with $x = 0.9, 0.93$ and 0.95 in HCl:DI at 19°C are measured for coupons arranged at $0^\circ/90^\circ$ and $45^\circ/-45^\circ$ with respect to the major plane as shown in table-4.1. These values are calculated by measuring the etch distance (perpendicular to the long side of the coupon) of coupons $100 \mu\text{m}$ wide and 1 mm long. It is evident that as the Al concentration in the AlGaAs sacrificial layer increases, the etch rate becomes faster for both parallel and rotated coupons. In

addition, the etch rate is higher for rotated coupons with layers containing 95% and 93% Al. The reason for the observed trend could be variations in atomic-scale arrangements. These variations can affect the chemical reaction by changing the orientation of bonds and the atomic densities [135]. A comparable etch rate is observed for coupons oriented at $0^\circ/90^\circ$ and $45^\circ/-45^\circ$ in the sample containing a 90% AlGaAs sacrificial layer. This can be due to the $1\ \mu\text{m}$ thick release layer in this sample as opposed to the 95% and 93% AlGaAs layers which are only $500\ \text{nm}$ thick. The increased thickness of the layer may also influence the release etch rate, as highlighted in [135]. It is important to note that variation in the accuracy of the Al content in the sacrificial layer (typically up to $\pm$ a few%) may also cause some variation in the etch rate. Taking into account all of the above factors, more experiments are required to reach a reliable conclusion.

Al content (%)	Etch rate ($\mu\text{m}/\text{min}$)	
	$0^\circ/90^\circ$ Coupons	$45^\circ/-45^\circ$ Coupons
90	~ 1.1	~ 1.0
93	~ 1.2	~ 1.6
95	~ 1.6	~ 2.2

Table 4.1: Measured etch rate of AlGaAs sacrificial layer with 90%, 93% and 95% Al concentration in HCl:DI (1:1) at 19°C . The etch time for 93% and 95% is 25 min and for 90% for 27 min. Note that the experimental measurements include an error margin of $\pm 0.15\ \mu\text{m}/\text{min}$.

4.1.1 QD Laser Coupon Release

The actual device coupons are up to $2.4\ \text{mm}$ long and $65\ \mu\text{m}$ and $80\ \mu\text{m}$ wide. The release etch is performed in an HCl solution prepared by mixing DI water and concentrated HCl solution (37%) in a volume ratio of 1:1 at 19°C for 35 min and 45 min for $65\ \mu\text{m}$ and $80\ \mu\text{m}$ wide coupons, respectively. Since the etch rate is above $1\ \mu\text{m}/\text{min}$ for both 93% and 95% Al containing AlGaAs layers, more than 10% over-etch time allows full release of the coupons. Figure 4.4(a) shows a top view of a coupon ready for release etching after the definition of the tether. This step requires special care to avoid blocking the etchant access to the sacrificial layer. A cross section of a coupon on a tether is shown in Fig. 4.4(b). The etchant begins to erode the sacrificial layer from the $500\ \text{nm}$ thick window on the sidewall, as this layer is etched down to the GaAs substrate everywhere except under the coupon.

The formation of a thin oxide layer on the $\text{Al}_{0.95/0.95}\text{Ga}_{0.05/0.07}\text{As}$ when exposed to ambient air, due to the high Al content in the sacrificial layer, requires a short ($<45\ \text{sec}$) de-oxidation dip in [Ammonium Hydroxide (25%): DI (1:10)] prior to release etch in HCl. The cross-section of the coupon over the tether schematically illustrates the oxidation layer on the sidewall of the sacrificial layer in Fig. 4.4(b). Once this oxidation is removed, the coupons are then released in the prepared HCl dilution. The

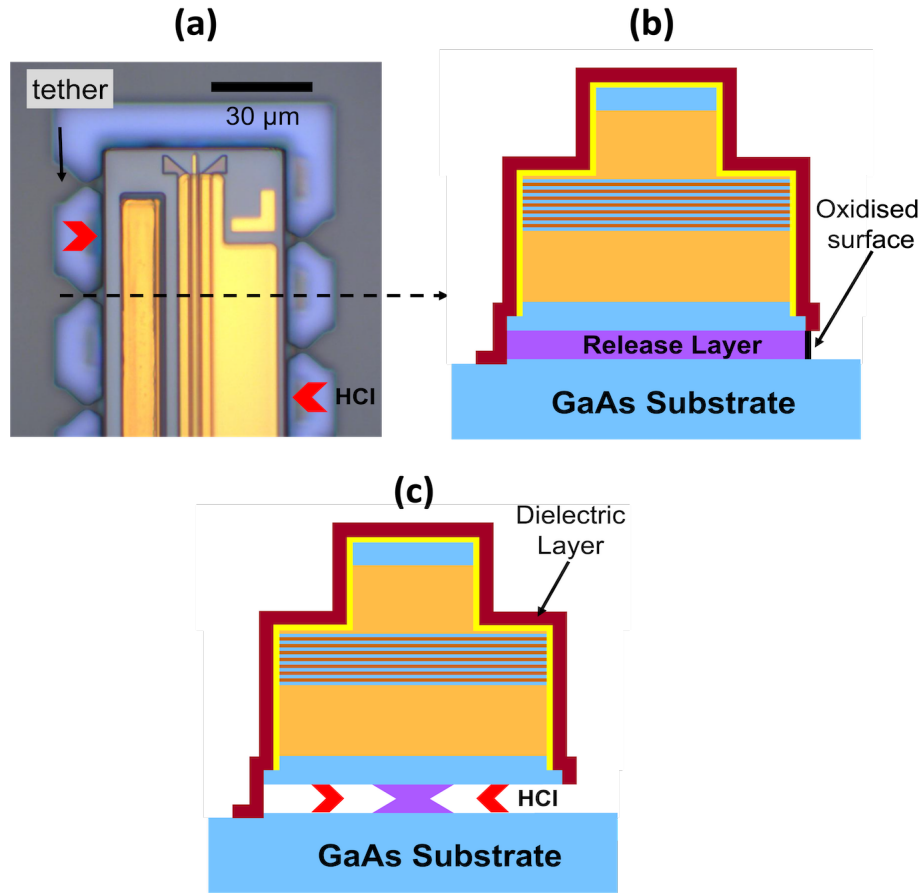


Figure 4.4: (a) Photo-resist tether defined with anti-phase configuration on 65 μm wide coupon. (b) The AlGaAs layer, which has a high Al content, oxidises quickly when exposed to air. This layer would have to be removed. (c) Undercut etch of sacrificial layer starts from both sides in HCl.

progress of undercut etching on a coupon is given in Fig. 4.4(c). The opening between the adjacent tethers allows the etchant access to the sacrificial layer. The uneven progression of the etching in the sacrificial layer also minimises irregular stress on the coupon induced by capillary forces during undercutting, thereby preventing the formation of defects on the bottom surface of the coupons [45]. Once the sacrificial layer has been completely removed, the HCl solution is further diluted by adding DI to the etchant mixture. The excess material is poured out while adding the fresh DI water to gradually reduce the HCl concentration from the solution and the sample. The sample remains in the beaker throughout this process. The sample is then immersed in DI water for a few minutes. It is important to note that rinsing the sample in running DI would be risky as it may cause the tethers to break during this step. Subsequently, the sample is allowed to air dry at clean-room temperature ($\sim 19^\circ\text{C}$) or low temperature ($<35^\circ\text{C}$) for ~ 15 min. High temperature drying on a hot plate will speed up the process but sudden evaporation might cause the coupon to collapse. The samples are placed at an angle during drying. In this way, gravity may help to remove the remaining liquid underneath the coupon. As the last and also

critical step of the III-V coupon process is the release etch, it is crucial to avoid coupon collapse after undercutting. Collapse can occur when the sample is removed from the etchant during drying due to weak tether systems and unbalanced stress on the coupon, which cannot withstand the capillary force. Following the drying process, the coupons are now ready for pick-up and transfer-printing.

Successful release etching without collapse is essential to achieve a clean and smooth surface at the bottom of the coupon, which is critical for improved bonding yield. The released surface can be quickly inspected after picking-up a few coupons using either a stamp with the transfer printer or a piece of flat polydimethylsiloxane (PDMS) manually by hand. Figure 4.5(a) and (b) show optical images of some coupon stubs after the coupons have been removed using a PDMS by gently touching the coupons. The smooth and particle-free surface on the stub indicates a clean bottom surface on the coupons. The optical images in Fig. 4.5(c)-(d) present the bottom surface of the coupon on PDMS.

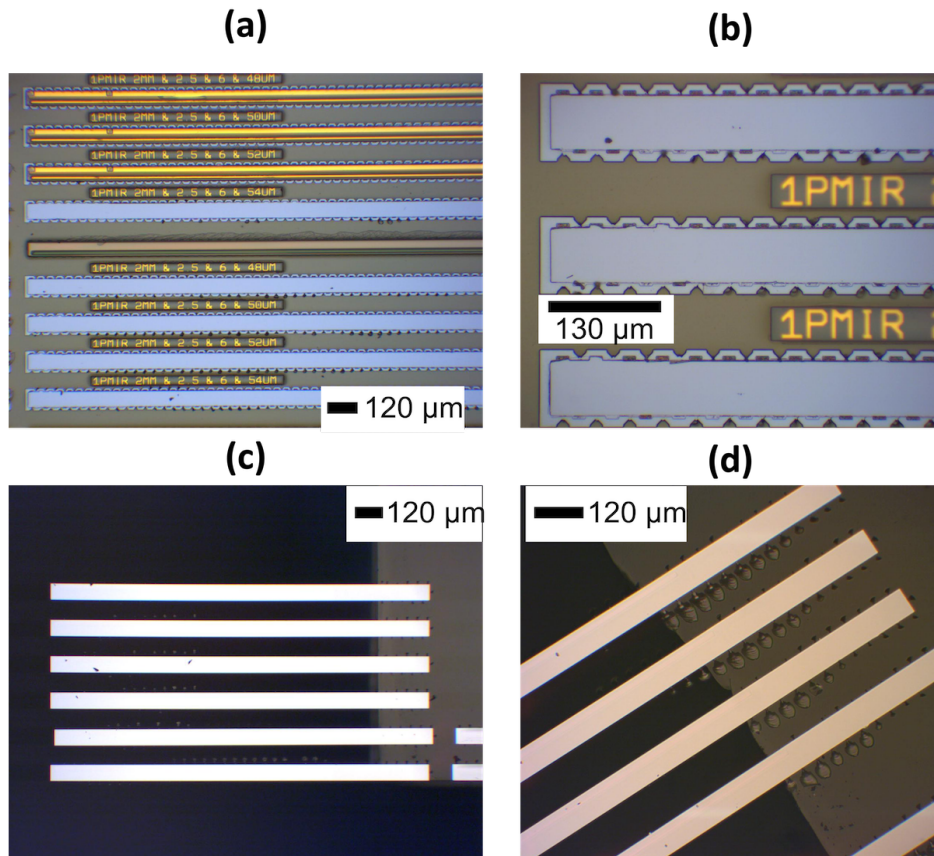


Figure 4.5: (a)-(b) Microscope image of released coupon with resist tethers held in place. After pickup of few devices, the remaining GaAs stub and resist anchors. (c)-(d) Image of the coupon bottom surface of coupons after the release etch.

4.1.2 Challenges in AlGaAs Release Etch and Fixes

Several issues can arise during the release etching, including coupon collapse and penetration into unwanted layers within epitaxial stacks. The resulting coupons with any of these issues cannot be used. Mitigating such problems requires effective management of the net stress on the coupon, careful design of the tethering system, and optimisation of the release conditions.

First, the dry etch step that removes the sacrificial layer over the areas where the tethers are to be defined must be free of the release layer residue. A thin residual film of the sacrificial layer can also lead to tether delamination. A few 100 nm of over-etching into the GaAs substrate ensures complete removal of the sacrificial layer. However, one should note that too much over-etch into the substrate may lead photo-resist tethers to stick out at the corner of the coupon and prevent perfect adhesion of the coupon edges to the target surface.

A particular challenge for AlGaAs sacrificial layers with a high Al content is the rapid oxidation of this layer when exposed to air. A de-oxidation dip in ammonium hydroxide (25%) prior to release prevents any complications for samples exposed to air for long periods. For samples exposed to ambient air for a long time or to an O₂ rich environment (i.e. O₂ plasma) in the subsequent fabrication step, a strong oxidation on the surface of the sacrificial layer could prevent the etchant from penetrating into the sacrificial layer. A longer ammonium dip would be an option, however it can attack and cause delamination of the photo-resist tether. Eventually, it may lead to coupon collapse. Figure 4.6(a) shows the resist tethers after a straight 3 min ammonia:DI (1:10) dip. The white colour indicates the ammonia attack on the resist causing the coupon to collapse due to the weakened tethering system. Another consequence of the weak tethering system is the formation of pillars on both the coupon stub and the back-side, as shown in Fig. 4.6(b) and (c) respectively. The SEM image of these pillars, also called pitting, on the coupon stub on the source substrate after undercutting shows that they consist of holes and spikes in a repeating pattern as shown in Fig. 4.6(d). The design of the tether is an important parameter in ensuring that the tether is strong and rigid. The widening of the tether base on the substrate would increase the tolerance to small undercuts.

The pitting effect also occurs when there is an unbalanced stress on the coupon, typically >100 MPa. In the final stage of release etching, tiny pieces of the remaining sacrificial layer material can break under stress and pinch off parts of the cladding layers, creating stress-induced spikes and holes. This breaks even leads to etchant penetration into the unwanted layers. The same phenomenon is also observed in the release of InP-based coupon devices and is discussed in [102].

A higher etch rate can be achieved by increasing the concentration of HCl or by increasing the temperature of the solution. A twofold increase in the etch rate is

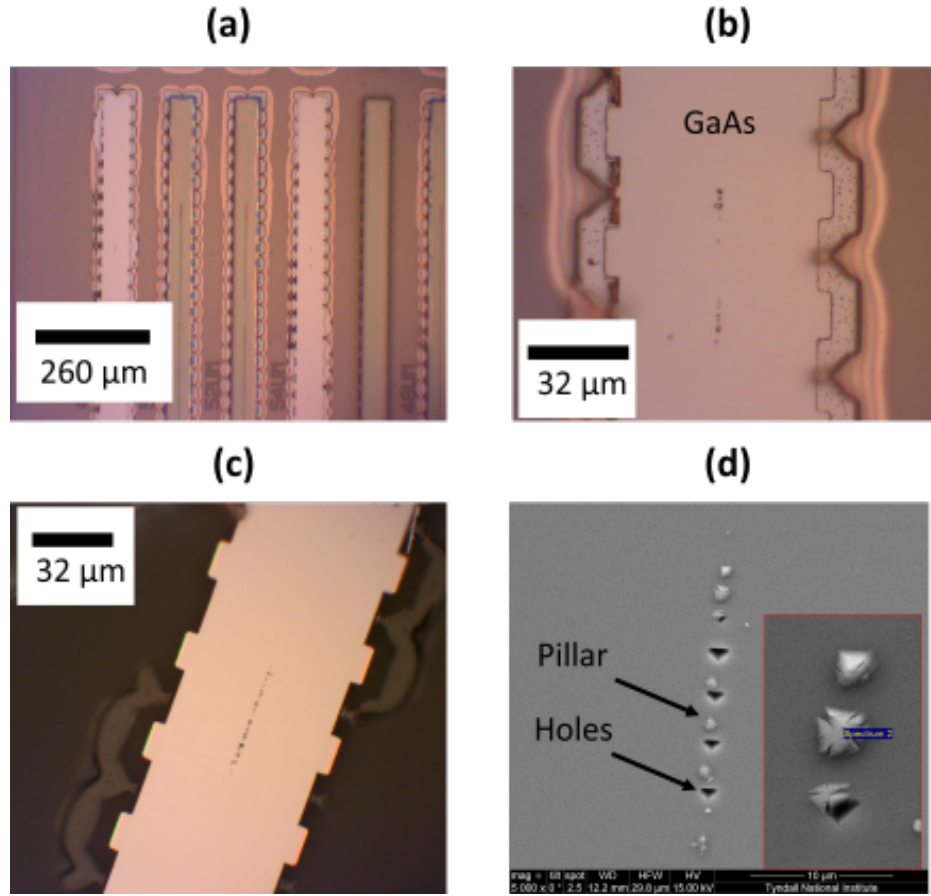


Figure 4.6: (a) Resist tether delaminated after a 3 minute immersion in a mixture of ammonia and DI (1:10). (b) The image of the coupon stub on the GaAs substrate after coupon pickup shows the spikes along the center. (c) The same pitting also appears on the underside of the coupon. (d) SEM images of the pillars show that there are spikes and holes. (Inset) Close-up of the pillars.

recorded at 19°C using an AlGaAs (95% Al) sacrificial layer when the HCl concentration doubles in volume (2HCl: DI) in the mixture. Release etch in concentrated HCl at an elevated temperature could result in an aggressive etchant that may attack the resist tether and other layers if the release time is longer than a few hours. Dilute HCl at an elevated temperature would be a safer option for such a scenario. In addition, the etch rate increases from $1.1 \mu\text{m}/\text{min}$ to $\sim 4.0 \mu\text{m}/\text{min}$ when the temperature of the etchant solution increased from 19 to 50°C for an AlGaAs release layer containing 90% Al.

Finally, the ledge-less process developed in this work is achieved by removing the tether on the emitting facet side of the laser coupon. In this way, we retain the few micron ledge on the other sides of the coupon and increase the tether strength to prevent collapse in the release etch, but eliminate the protrusion in the front facet. A completely ledge-less coupon is possible and straightforward in terms of fabrication with a small change in the mask using a self-aligned process. However, a significant problem with this method is that the coupons tend to collapse during the release etch

process. This is associated with the weak anchor system due to the substantial step height that a tether must climb, which is approximately $5\ \mu\text{m}$ in this thesis, in a single step instead of the first climb a $\sim 1\ \mu\text{m}$ and the rest in the second step. This weakens the connection between the tethers and reduces their strength as a system. This hypothesis is tested experimentally by fabricating the same coupons using an identical process flow and tether (S1828 photo-resist) on a standard coupon with a ledge and a completely ledge-less coupon. After following the same release etching procedure, it is found that the majority of the ledge-less coupons are collapsed. Figure 4.7(a) and (b) show an optical top view of coupons before and after release etching, respectively. The presence of a pink colour on the edge of the ledge-less coupon indicates the collapse. The survival rate on the standard coupon is over 95%. A step height scan over both types of coupon is shown in Fig. 4.7(c). A ledge-free coupon could be successfully applied to coupons with a thinner epilayer where the step height is less, or by using a stronger tether system.

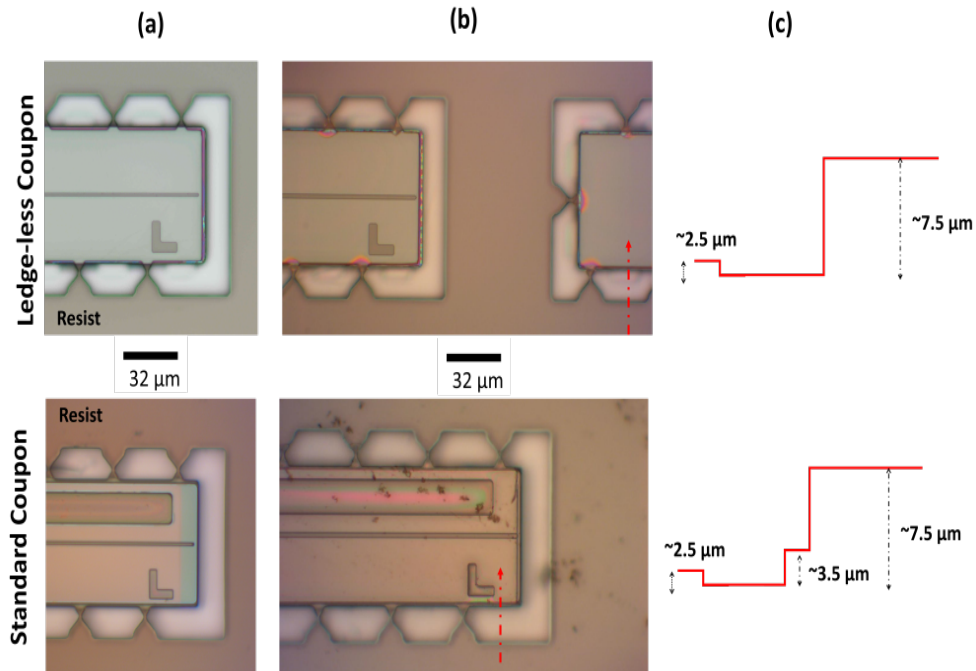


Figure 4.7: Optical images of coupons with no ledge (top) and $2.5\ \mu\text{m}$ ledge (bottom) coupons before (a) and after (b) release etching. Both coupons have the same tether design and material, S1828 photo-resist. (c) The step height profile that shows the step that a tether climbs on a ledge-less (top) and ledged coupon (bottom).

4.2 Target Wafer Preparation for MTP

Heterogeneous integration of optical components via MTP requires adhesion of coupons to the target that depends on the properties of the mating surfaces. Smooth and clean surfaces play a critical role during source and target preparation. In some cases, where there is a strong Van der Waals force between the two surfaces,

integration without adhesive would be an option, as shown for InP coupons transfer-printed on Si targets [136]. A thin polymer bonding layer such as Benzocyclobutene (BCB) [137] or InterVia [138] between III-V and the target surface might be necessary for a reliable and repeatable integration. These materials act as excellent planarization and adhesive layers as a result of their low viscosity. They fill in surface irregularities, providing a smooth interface for bonding. In addition to their excellent adhesive characteristics, these polymers can be employed as a stress buffer. The thickness of the adhesive layer is determined by considering the thermal and mechanical properties needed to accommodate stress. The adhesive thickness in this work varies from 5 nm to 200 nm.

4.2.1 MTP without Adhesive Layer

Direct printing, also known as adhesive-less printing, of coupons requires both surfaces to be flat and smooth. Direct printing provides excellent heat dissipation for the devices, as shown in [70] for InP lasers. In addition to cleaning both surfaces, a O_2 plasma-assisted bonding technique is used to improve adhesion at low temperatures for direct bonding of III-V wafers or dies to SOI [139–141]. Based on this work, adhesive-free integration by micro-transfer printing is developed as reported in [142]. In this strategy, the native oxide on the Si and III-V bonding surfaces has to be removed by wet etch exposure to the HF-based dilute (buffered oxide) BOE solution. The subsequent O_2 plasma treatment converts the sample surfaces from hydrophobic to hydrophilic by growing a thin layer of highly reactive native oxide that provides a high density of -OH (i.e. hydroxyl) groups. A few hours of annealing at around 300°C in a high vacuum are required to form a strong bond. In addition, the deposition of a thin layer of SiO_2 as an interfacial layer between two surfaces would be beneficial in reducing the formation of voids by preventing the formation of gaseous by-products such as H_2O and H_2 .

Figure 4.8(a) and (b) illustrate the direct integration of QD lasers on a blank Si and a recess on SOI, respectively. First, QD laser coupons are directly printed on a blank Si. A transfer-print test is carried out and out of 5 coupons, only 2 coupons were successfully printed on the Si blank target. However, in the subsequent resist cleaning step, a coupon flies away. This corresponds to a print yield of 20%. The optical image of the remaining coupon on the Si wafer after resist removal is shown in Fig. 4.8(c). The same coupons are then transfer-printed onto the SOI wafer with recess. Even worse results are obtained in this case because of the resulting rough surface on the Si substrate inside the recesses compared to that of non-processed blank Si. The low print yield suggests that an adhesive layer is required for strong bonding, resulting in higher print yield and stable integration of GaAs based devices.

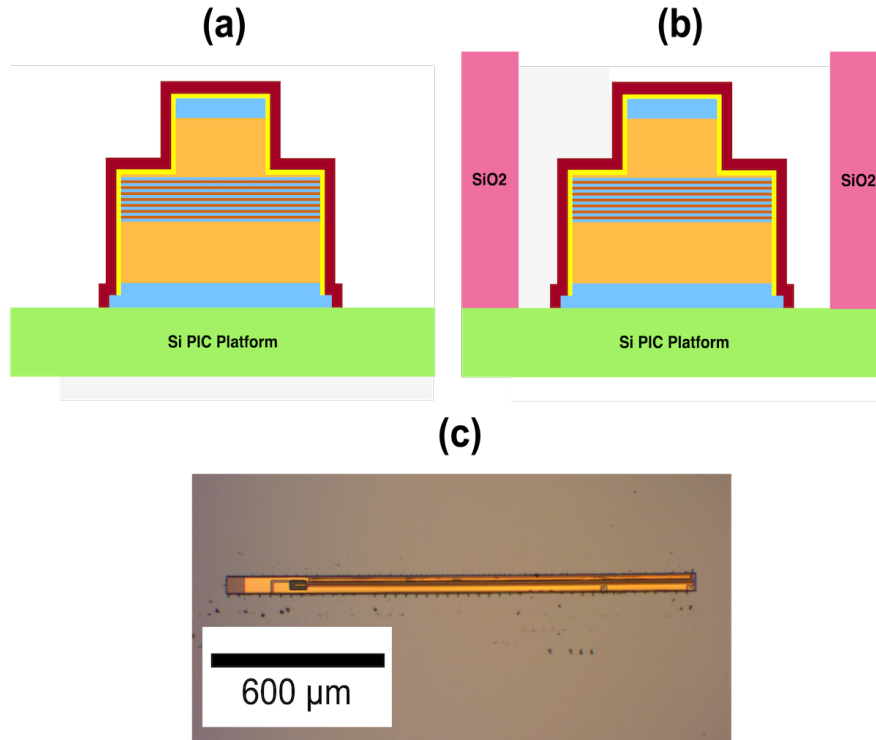


Figure 4.8: Schematic illustration of a QD laser transfer-printed directly onto (a) blank Si and (b) recess on SOI without polymer adhesive coating. (c) Optical image of the transfer-printed laser coupon on a blank Si wafer.

4.2.2 MTP with Adhesive Layer

In this thesis a thin adhesion layer (typically $< 200 \text{ nm}$) is used between the III-V device and the target surface to improve the printing yield and repeatability and reliability of the integration. However, the low thermal conductivity of this layer compared to that of Si can reduce the thermal heat sink. Several materials can be used as adhesive layers, but BCB and InterVia are investigated in this work. These materials are in liquid form at room temperature and in elastic solid form at elevated temperatures. Typical crystallisation temperatures after curing are in the range of $150 - 340^\circ\text{C}$ for BCB and $175 - 200^\circ\text{C}$ for InterVia. No by-product formation is reported after curing, so the bonding interfaces remain in full contact.

BCB is widely used in electronics, and its thermal and electrical properties have been well studied. However, InterVia is a relatively new material and offers a lower curing temperature and better thermal conductivity ($\sim 0.006 \text{ W/cm}^\circ\text{C}$) than BCB ($0.0029 \text{ W/cm}^\circ\text{C}$). Thermal cure recipes for both materials are provided in section 4.3 on the post-print process. In addition, rework is relatively easy with BCB as it can be removed in Mesitylene or Ti1100 solvent [143] if it is not fully cured. Since InterVia cannot be easily removed as BCB, it is more difficult to re-work. There is a thickness shrinkage with both materials during full curing, which would result in vertical misalignment if the printing were done at room temperature. For applications that

require very sensitive vertical alignment or evanescent coupling, a shrinkage factor could be studied, taking into account the overdrive pressure in transfer-printing and hard curing. Depending on the thickness, both materials reduce the thermal heat sink of the III-V devices. However, a thickness below 100 nm can allow sufficient heat transfer to the substrate, based on the experiment in this work.

The adhesive layer can be obtained on the target surface by spin coating or spray coating. By diluting BCB with Mesitylene (Ti1100), very thin films can be obtained. The BCB solution used in this work is diluted with Mesitylene in a ratio of 1 to 5 and spin coated at 4000 rpm for 50 seconds followed by 3 min hop-plate bake at 120°C in air ambient. The resulting film thickness on the blank Si is measured to be 70 nm. The lasers to be used as reference devices, which have undergone the same release and printing process, are then transfer-printed onto the resulting 70 nm BCB on Si wafer.

Similarly, InterVia can be diluted with propylene glycol monomethyl ether acetate (PGMEA) [144] in the appropriate ratio to achieve film thicknesses down to 50 nm. In this work, diluted InterVia with PGMEA in ratios of 1 in 4 and 1 in 20 is investigated. The dilution is spun on the Si wafer at 4500 rpm for 40 seconds and then baked on a hot plate for 1 minute at 110°C in air.

A non-uniform adhesive layer can be detrimental to device performance. A uniform adhesive layer can be easily achieved on target wafers with no topography or a shallow topography by spray or spin coating. However, targets with deep recesses and more complex topography may require special care to deposit a uniform adhesive layer due to surface dynamics. Although spin coating is simple and gives good uniformity on wafers without topography, the minimum achievable thickness can be limited. Spray coating of the adhesive film theoretically offers more flexibility in terms of thickness with better uniformity on both blank and patterned wafers.

4.2.2.1 MTP of QD Lasers on Blank Target

Initially, glass and Si wafers with different BCB thicknesses ranging from 5 nm to 200 nm were prepared to evaluate the thickness required for the optimal MTP of QD laser coupons. The adhesive layer is deposited on the wafers by spray coating by EV Group. These wafers do not have patterns on them. 30 QD laser coupons (65 μm wide) with a length of 1.8 and 2.4 mm are transfer printed on these targets with a print yield of 100% as shown in Fig. 4.9.

Coupons were printed on glass wafers of 5 nm, 35 nm and 200 nm spray-coated BCB to investigate the impact of the adhesive layer thickness on the print yield and bonding quality at the interface through the glass substrate. 5 coupons of each length were printed on each BCB thickness with 100% yield. The high print yield for all thicknesses indicates the well-balanced stress on the coupon. Then, the bond achieved between the bottom of the coupon and the wafer surfaces is inspected through the

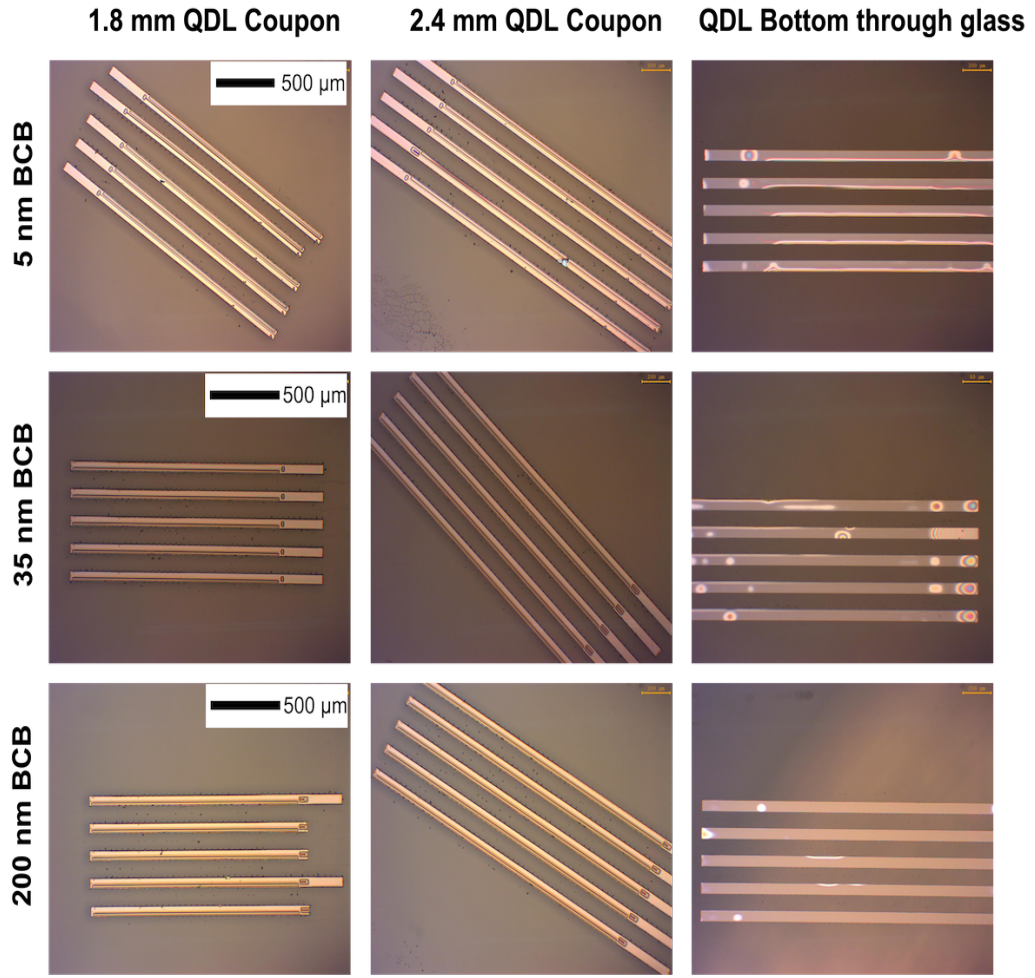


Figure 4.9: Optical images of QD laser coupons on 5 nm, 35 nm and 200 nm BCB on glass substrate. Transferred coupons are 65 μm in width and 1.8 and 2.4 mm in length. Coupon back side through glass wafer showing the bonding quality between the two interfaces.

glass substrate. Although the print yield is very high, there are several discoloured points at the coupon-substrate interface. The white colour indicates the absence of contacts at the bonding interface. These voids can be caused by a number of reasons, including residual particles on the target substrate, pillars on the bottom surface of coupons, and lack of enough pressure on the coupon during printing.

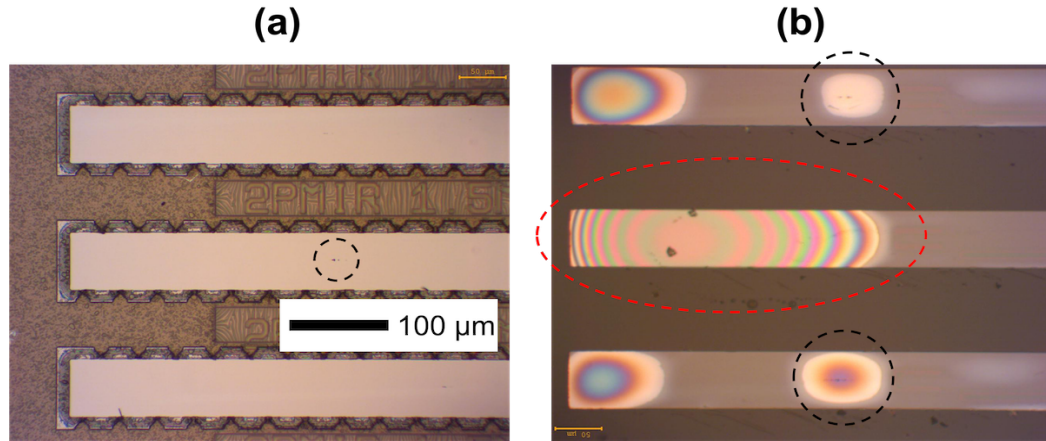


Figure 4.10: (a) Optical image of stubs on GaAs after the coupons picked-up showing the occurrence of pillars in few of them. (b) Image of bonding interface through glass substrate shows the same pillars present on coupon back side. Also end of coupons have poor bonding due to the use of short stamp that leads insufficient pressure at these locations.

Inspection of the poor bond interfaces reveals that the pitting on the underside of the coupons or particles on the target wafers is the cause of these voids. The formation of the pits is related to the release etch, as discussed in section 4.1 of this chapter. The particles on the substrate wafers are mostly associated with target preparation and the MTP process, where some debris might be generated in the tether break during pick-up. Figure 4.10(a) and (b) show the pillar (black circle) on both the coupon stub on GaAs and on the backside of the coupons. The lack of pressing force on the end coupon due to the use of a stamp shorter than the length of the coupon during the printing process is the reason for the white areas in the red circle shown in Fig. 4.10(b). The printing of all coupons is done using a stamp with a 1.8 mm long post to simplify the process. This can be simply addressed by using an equal or slightly longer stamp than that of coupon. Pillar formation can be reduced by using a stronger tethering system, as discussed in chapter-2 in section 2.3.5.

Finally, the same experiment is repeated for Si wafers with 5 nm and 35 nm spray-coated BCB. A total of 10 coupons from the chip are transfer printed onto blank Si targets with 100% print yield. The coupon lengths are 1.5 mm, 1.8 mm and 2.4 mm. Figure 4.11(a) and (b) show images of laser coupons printed on Si targets with 5 nm and 35 nm BCB, respectively. As a result, the appearance of voids at the bonding interface may be an indication of poor adhesion of the coupon to the target substrate and may affect the device performance. The achieved bonding strength is good enough to characterize the devices integrated on the Si wafer in this thesis.

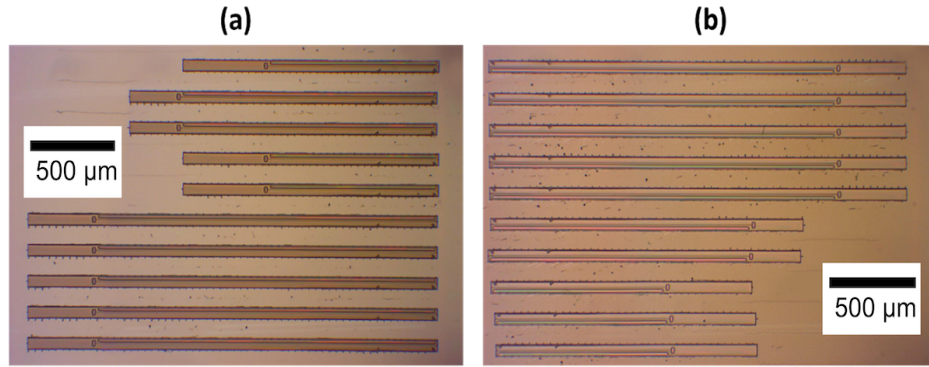


Figure 4.11: Images of laser coupons on (a) 5 nm and 35 nm thick spray-coated BCB. The coupons are 65 μm wide and 1.5 mm, 1.8 mm and 2.4 mm long.

4.2.2.2 Patterned Polymeric Adhesive

In particular cases for edge-coupling from laser to waveguide, there is a need for several micron deep trenches on the SOI wafer with varying depths of recess. Coating the adhesive material on such substrates might create some issues that need to be addressed for improved coupling performance. Regardless of the coating technique, spray or spin coating, a significant amount of adhesive material is observed accumulating toward the sidewall of the 7 μm deep trenches. Figure 4.12(a) shows an image of the trench prior to adhesive coating. The adhesive polymer pools and forms a ramp in the spray and spin coating processes, as shown in Fig. 4.12(b) and (c), respectively. The pooling starts from several microns away from the SOI facet and reaches to a few microns in thickness towards the sidewall of the recess. This excess material prevents the laser coupons from being printed closer than 5 μm from the SOI facet and causes significant coupling loss as discussed in chapter-3 in section 3.2.1. Although the accumulation length is shorter in the spray coating process, a similar pooling profile is observed in both techniques using different adhesive polymers including BCB and InterVia. To address this issue, a patterned adhesive process is developed using BCB and InterVia.

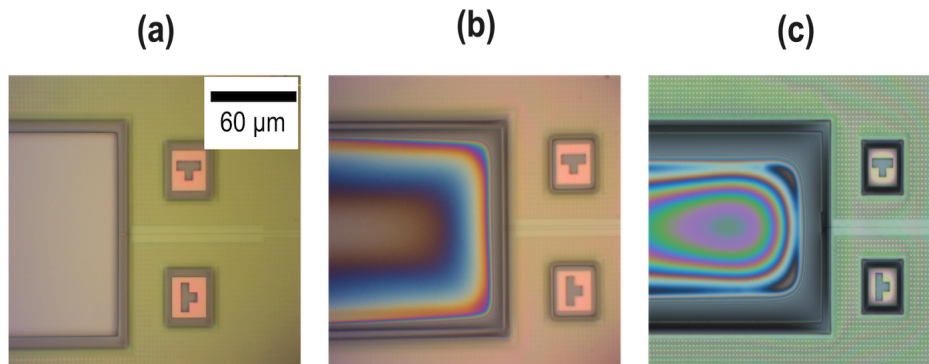


Figure 4.12: Photo of cavity (a) before and after adhesive coating through (b) spray-coating and (c) spin-coating. A significant amount of adhesive material pools towards the sidewall during (b) spray coating and (c) spin coating of InterVia.

A series of adhesive patterning and transfer printing experiments have been carried out using both BCB and InterVia layers. The first patterning test was performed with 100 nm BCB and 200 nm InterVia spray-coated onto flat Si and then patterned by the EV Group. Figures 4.13 (a) and (b) show the patterned BCB and InterVia on a flat Si wafer through an optical lithography process following the spray coating. A visible contrast difference between the patterned and unpatterned adhesives on Si indicates that patterning of the adhesive layer below 200 nm is achievable by photolithography. Subsequently, 5 coupons were transfer printed on the patterned layer of both adhesive materials to evaluate the adhesion properties after patterning. Transfer print yields of 20% and 100% are achieved on BCB and InterVia respectively. Optical images of the transferred coupons on the targets are shown in Figure 4.13(c) and (d). Although a very high print yield was achieved on the unpatterned BCB, the print yield on the patterned BCB layer decreased to 20%. This suggests that the BCB layer loses its adhesion strength once it is exposed to the developer. However, in the InterVia layer, no decrease in yield was observed after patterning. Therefore, further optimisation was performed using InterVia as the adhesive layer.

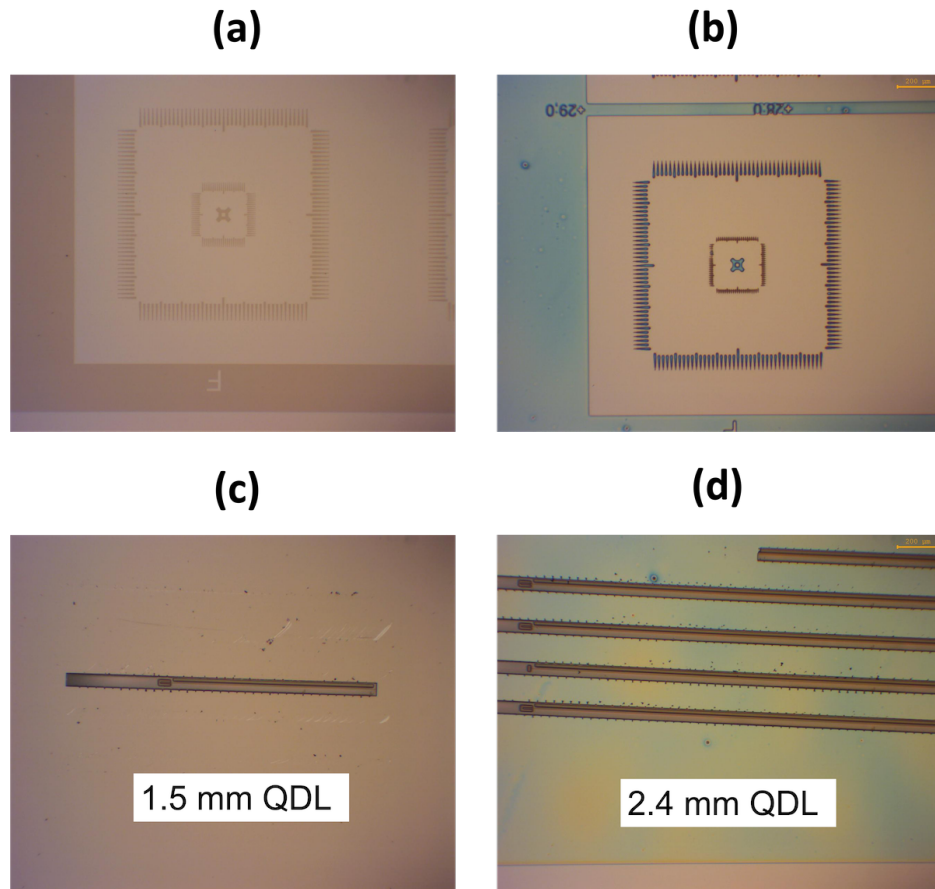


Figure 4.13: (a) 100 nm BCB is spray-coated and patterned on flat Si. (b) 200 nm spray-coated InterVia is patterned on Si. (c) MTP of 1.5 mm test coupons transfer-printed with 20% yield on patterned BCB. (d) 2.4 mm long coupons are transferred on 200 nm patterned InterVia with a 100% yield.

Based on the learning from the first experiment, a thinner InterVia layer (50 nm) was sprayed onto a blank Si wafer and then patterned by optical lithography. The film thicknesses on the unexposed (removed) and exposed (remained) areas are measured with Nanospec 3000 as 20 nm and 45 nm, respectively, as shown in Fig. 4.14(a). The step height measurement (15 nm) confirms that the material is not completely removed during the patterning process. A similar result is observed on a 200 nm InterVia spray-coated SOI chip with a deep recess, as shown in Fig. 4.14(b). Although there is a visible constant difference after patterning, a thin layer of adhesive material remains in the exposed area where it should be completely removed. Increasing the development time does not remove the remaining adhesive, but starts to thin the material on the unexposed area, where it is supposed to stay. The patterning is partially effective and is not sufficient to remove excess material that has accumulated on the sidewall of the recess. It is important to note that film thicknesses below 200 nm require a very high dilution rate in PGMEA (typically 1 to 50 by weight) for spray coating, making the patterning of the InterVia quite challenging. This is due to the very small amount of photoactive material in the solution, with a high degree of non-uniformity. Then, the dummy QD laser coupons are transfer-printed onto the target wafer with patterned InterVia layer. Print yields of 100% and 75% are achieved for lasers printed on the exposed (InterVia remaining) and unexposed (InterVia removed) parts of the wafer, respectively, as shown in Fig. 4.14(c) and (d). Furthermore, the high print yield in the unexposed area confirms the presence of the remaining adhesive layer.

Due to the difficulties in patterning highly diluted InterVia, a low-dilution InterVia solution is prepared using PGMEA in a ratio of 1 to 4. The reference blank Si and SOI wafers are spin-coated and patterned in Tyndall's clean room. Figure 4.15(a) and (b) schematically illustrate the adhesion profile after spin coating and patterning, respectively. As InterVia 8023-10 is a negative tone material, the unexposed area is removed in tetramethylammonium hydroxide (TMAH) containing developers such as MF319 and MF26A. A patterning process has been developed that results in complete removal of InterVia at the edge of the trench, leaving a 150 nm thick InterVia layer in the center of the trench. Further process details related to coating and optical lithography can be found in the Appendix C. Figure 4.15(c) and (d) show the trench on an SOI wafer after InterVia spin coating and patterning by optical lithography, respectively. The removal of the accumulated material can be clearly seen from the sidewall of the recess.

One challenge with the InterVia patterning process is that the adhesion of the remaining adhesive material on the target surface is weakened by its exposure to the developer during the patterning process, making the printing yield more sensitive to coupon quality (i.e., stress and smooth backside). That reduces the bonding strength of the coupon to the substrate. To restore adhesion, a 30 second O₂ plasma treatment

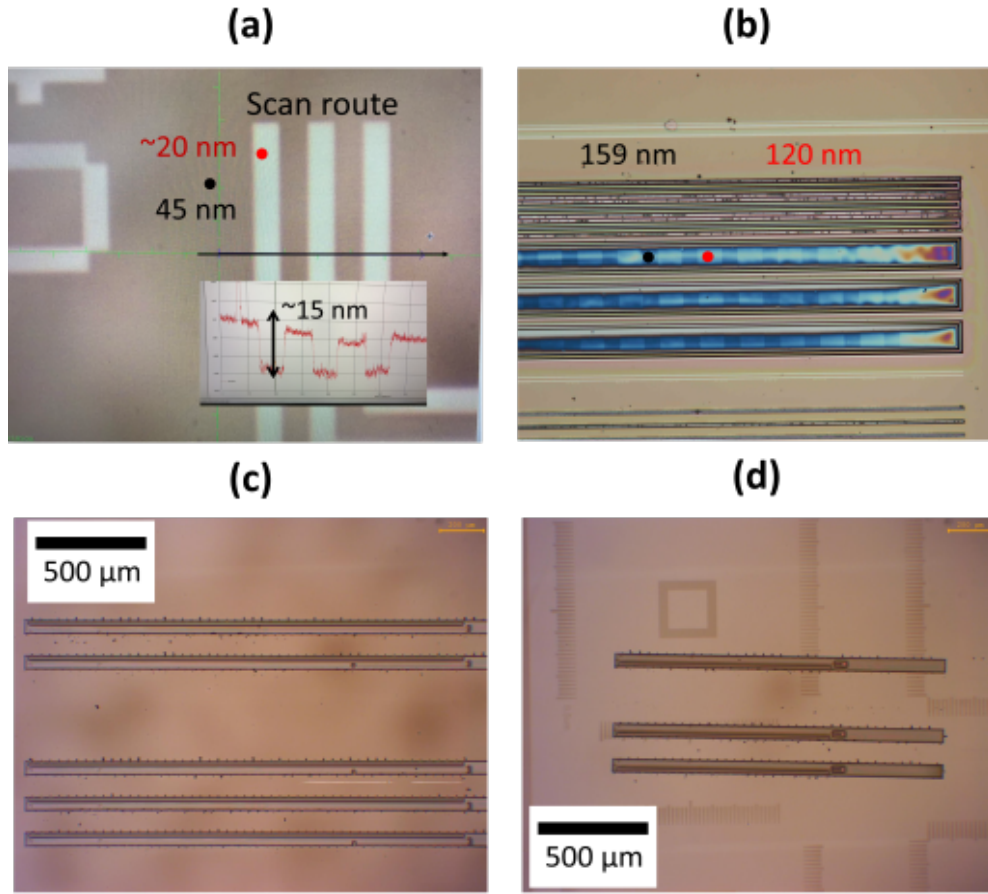


Figure 4.14: (a) Optical image of 50 nm sprayed InterVia on Si substrate after patterning. The measurement shows that there is a step height difference of 15 nm over rectangular features where InterVia has been removed and where it remains. (b) Partial patterning is achieved on a 200 nm InterVia coated SOI wafer with a recess. (c) Transfer-printing of the 2.4 mm long coupons on the remaining InterVia following the patterning with a 100% print yield. (d) Same coupons are transferred on an area where InterVia has been removed by patterning. 4 out of 3 coupons are successfully printed.

is applied to the target wafers with patterned InterVia prior to transfer-printing. It is important to note that high power plasma could completely remove the thin adhesive layer, so it may be safe to keep the power level low. The power of the plasma asher is set at 50 W. However, it is not guaranteed that the short O₂ in low-power plasma treatment always solves this problem. In this thesis, final generation coupons with optimised stress level and good surface roughness result in a high printing yield on the target with patterned InterVia. In addition, the second issue with this approach is the limited minimum thickness achievable through spin-coating at low dilution rates (i.e., 1 to 4), where the patterning process is more robust. A thinner layer of InterVia can be achieved at higher dilution rates via spray-coating, however, the patterning becomes more challenging in this case. Thus, there is a tread-off between the adhesive layer thickness and the reliable patterning process.

Given the patterning challenge of InterVia-PGMEA (1 to 50) and the limited minimum thickness of InterVia-PGMEA (1 to 4), a mixture of InterVia-PGMEA with 1-20 was

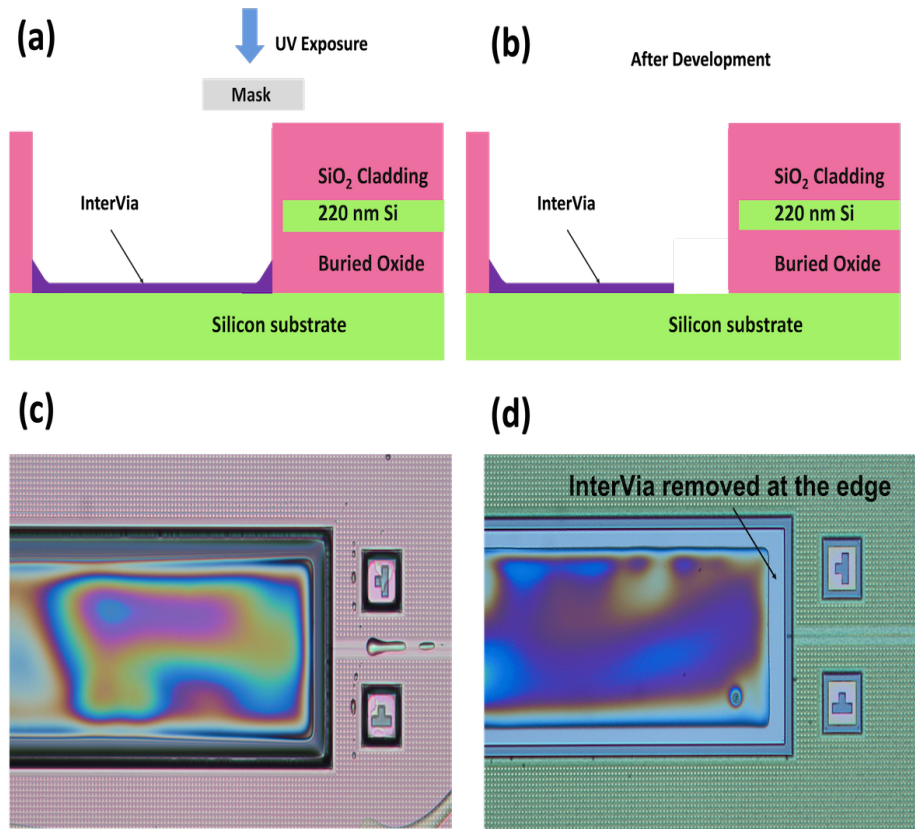


Figure 4.15: (a) Schematic illustration of adhesive patterning through optical lithography. (b) The piled adhesive towards sidewall is removed after 45 sec development in MF26A. (c) Spin-coated InterVia-PGMEA (1-4) solution on 7 μm deep recess on SOI. (d) After the removal of the accumulated adhesive on the sidewall of the cavity by optical lithography.

investigated to achieve a reliable patterning process with a sufficiently thin adhesive. The solution is spin-coated at 4500 *rpm* for 40 seconds followed by a soft bake at 110°C for 1 minute. The resulting InterVia thickness is measured approximately 60 *nm* at the bottom of the trench. Figure 4.16(a) and (b) show an optical image of a recess before and after InterVia coating. In addition, the resulting adhesive layer is not pooling on the sidewall of the recess after soft bake. This eliminates the need for patterning, which exposes the adhesive to the developer. This adhesive coating approach was used for laser integration on final SOI wafers.

4.3 Post-Print Process

Once the coupons are transfer-printed onto the target wafer, additional processing might be required to complete the integration, including photo-resist tether removal, contact metal deposition, or further fabrication for partially fabricated coupons. It is better to have a minimum number of post transfer-printing processing steps as they carry some risks such as damage to the device or delamination of the integrated coupon from the host surface. Processing on the source wafer is often less complex

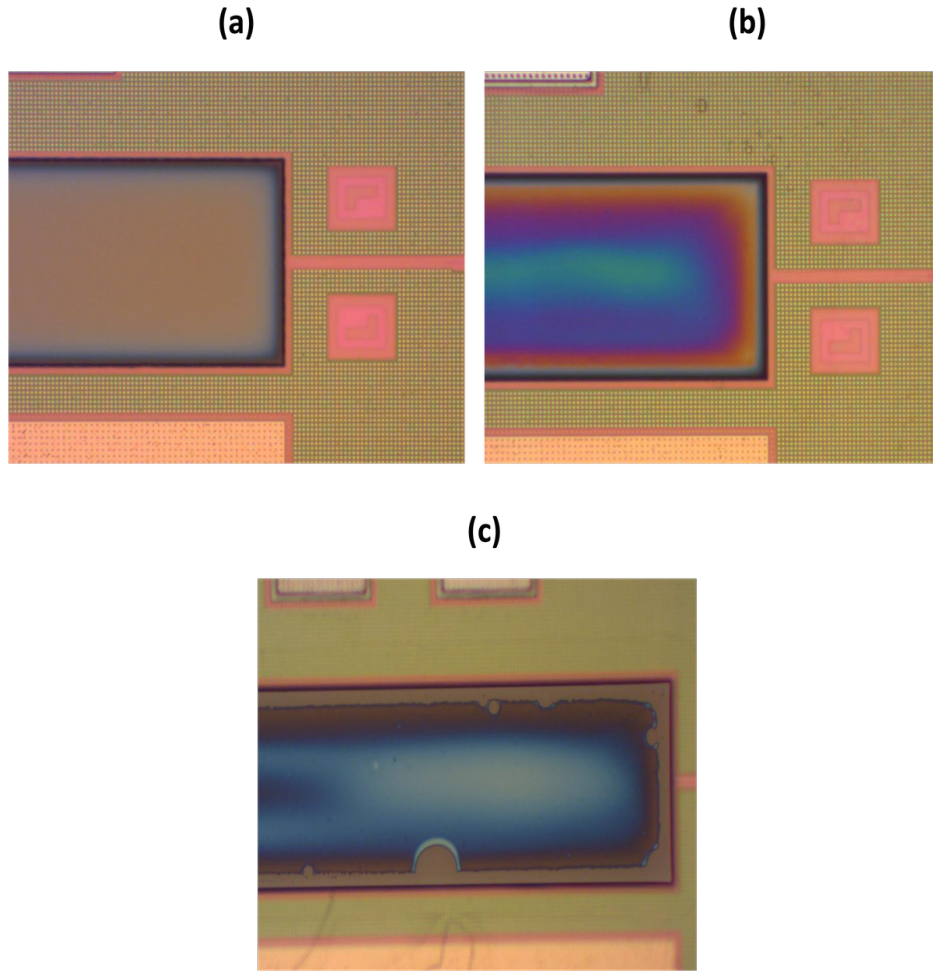


Figure 4.16: Image of a recess (a) before and (b) after InterVia-PGMEA (1-20) spin-coating. (c) Image of a recess with poor adhesion resulting in a non-uniform coverage of the InterVia PGMEA (1 - 20) film.

than on the host substrate. In addition, having the pre-fabricated devices on the source with less post-processing allows characterisation of the devices prior to integration to improve the functional device yield. In this work, the laser coupons are fully fabricated on III-V wafers and ready for use. The only post-processing is the removal of the resist tether and the curing of the adhesive after transfer-printing. Contact metal evaporation for easier characterisation can also be listed as post-print process, but is not mandatory.

4.3.1 Tether Removal

The first step after transfer-printing of coupons is the removal of the polymer tether. In this work, photo-resist based tether with a typical thickness of 3-4 μm is used. The polymer tether can be removed by isotropic dry-etch under low power oxygen plasma in an Asher. However, it can take up to several hours to fully remove the resist depending on its thickness and the power of the plasma etch. In addition, an ICP based O_2 plasma etch can be used as a faster alternative. This approach has been used

for the final generation laser devices to clean the photo-resist tether in this work.

The resist tether can also be removed using liquid solvents (Acetone, Isopropyl alcohol (IPA) and 1165 Remover) which dissolves and cleans the resist anchor. Another possible strategy for the removal of photo-resist based tether using acetone vapour is described in [142].

4.3.2 Adhesive Thermal Cure

The polymer materials used as adhesive layers exist in either a liquid or semi-liquid form when coated on the target substrate. After laser integration, a thermal treatment process known as curing is applied to fix the coupons in their position and prevent sliding during the post-process and characterization. This process polymerises the adhesive layer, transforming it into a long-term stable and inherently polymerised dielectric layer. Curing creates chemical bonds between the polymer chains, creating a network structure that enhances the material's mechanical strength, thermal stability, and resistance to environmental factors.

Following complete removal of the resist tether, the BCB bonding layer is fully cured at 250°C for 60 min in a N₂ environment at a flow rate of 100 *sccm*. The temperature is ramped up from room temperature to 250°C and then slowly cooled to room temperature after curing. The InterVia curing step is carried out at 175°C for 3 hours in the same N₂ environment (flow rate set to 150 *sccm*). The steps for both recipes are given in table-4.2.

Steps	Thermal Cure Recipe	
	BCB	InterVia
1	15 min ramp to 100°C	15 min ramp to 90°C
2	15 min soak at 100°C	30 min soak to 90°C
3	15 min ramp to 150°C	15 min ramp to 175°C
4	15 min soak to 150°C	180 min soak to 175°C
5	60 min ramp to 250°C	Cool down to < 150°C
6	60 min soak to 100°C	
7	Cool down to < 150°C	

Table 4.2: Thermal cure recipes used for BCB and InterVia bonding layer after resist removal from the coupons.

After thermal curing of the bonding layer, the laser coupons are ready for further processing and probing for electrical characterisation. These coupons typically remain in place throughout this process if the bonding between the coupons and the target substrate is properly established.

4.4 Conclusion

This chapter reports on the process development and optimisation for transfer printable prefabricated GaAs laser coupons. Development of HCl based release etching for AlGaAs sacrificial layers with 90%, 93%, 95% Al content. The QD laser coupons are released in a HCl:DI (1:1) mixture at 19°C with a smooth and clean bottom surface, which is critical for high-yield integration. Problems encountered in QD laser release etching, such as coupon collapse, pitting, and oxidation, are discussed, along with preventive measures to minimise them. The preparation of target substrates for MTP is also discussed. The need for a bonding layer and the polymer materials investigated as bonding layers are presented along with the coating parameters. Transfer-printing of laser coupons printed on BCB coated Si and glass wafers with very high print yields above 90%. The thickness of the BCB varies from 5 nm to 200 nm. The bond quality of the printed coupons on the glass wafers is inspected through the backside to ensure device integration. A particular challenge of adhesive accumulation associated with recessed SOI wafers for edge coupling is tackled to reduce the longitudinal misalignment between the laser and the receiving waveguide. Two solutions were developed, namely adhesive patterning and spin coating with high dilution rate (1xInterVia-20xPGMEA) adhesive to address this issue. Finally, post-printing processes including resist stripping, thermal curing of the adhesive layers, and bond testing are presented.

Chapter 5

Characterisation of Transfer-Printable QD Lasers

This chapter presents characterisation and performance evaluation of the QD lasers developed in chapter-2. The laser diodes undergo electrical, optical, and thermal characterisation before and after transfer-printing. High-performance, low-threshold laser diodes are developed through iterative fabrication-integration-characterisation cycles. The corresponding process optimisation and development for fabrication is described in detail in chapter-2. Initially, the measurement setup and equipment used during the characterisation are explained. Then electro-optical analysis of the lasers for each generations is carried out for non-released devices on GaAs substrate and transfer-printed devices on blank Si substrate. The effect of transfer-printing on device performance is observed.

5.1 Introduction

Several generations of laser diodes have been designed, fabricated, and characterised to achieve the best devices with low threshold and high output power. Laser diodes from each generation were characterised and evaluated by comparing their performance with the reference cleaved and etched facet devices on the same chip. To enable this comparison, identical non-released cleaved and etched facet devices are included in the same run on the same chip with transfer printable laser diodes. Laser diodes with different cavity lengths, ridge widths, and reflective mirror types, including etched facet metal-coated mirrors and multi-mode interference reflector (MIR) mirrors, were fabricated and characterised.

Laser diode characterisation consists of the determination of the electrical, optical, spatial, and spectral properties of the device [145, 146]. The electrical characterisation provides valuable insight into the material efficiency, laser diode

electrical efficiency, which is the ratio of optical output power to electrical input current, and some thermal characteristics. The electrical properties of a laser can be determined by measuring its light-current (L-I) and voltage-current (V-I) characteristics. The L-I characteristics provide valuable information about the lasers, such as the threshold current (I_{th}), which is the current at which lasing starts, and the threshold current density (J_{th}) can be determined by dividing the experimental threshold current (I_{th}) by the area of the laser. This is a useful parameter that gives a direct indication of the quality of the materials used in laser construction and when comparing different laser devices, as it is independent of the geometric design of the laser diodes. Determining the slope efficiency from the L-I curve allows other parameters to be extracted such as the external differential quantum efficiency (η_d - efficiency in converting electron-hole pairs into emitted photons from the device), the internal quantum efficiency (efficiency in converting electron-hole pairs into photons within the device), the internal losses (represents the proportion of generated photons within the laser cavity that cannot escape the device and contribute to the emitted output light of laser diodes) [145]. The temperature dependent L-Is allow the extraction of the characteristic temperature (T_0 and T_1), which are parameters that describe the temperature dependence of the laser's threshold current and slope efficiency, respectively. In addition, the V-I characteristic shows the relationship between the laser's electrical current and the voltage applied across it, and allows the series resistance of the device to be determined. The spectral properties are related to the emission spectrum of the laser diode and provide information about the type of laser, the spectral width, the central emission wavelength, the free spectral range, the thermal behaviour and the thermal impedance [146].

5.2 Measurement setup

The electro-optical and spectral characterisation of the edge-emitting laser diodes is performed using the setup, shown in Fig. 5.1. The setup consists of a temperature controlled stage with a Peltier element for sample positioning, optical lenses mounted on an X-Y-Z alignment stage, electrical probes with 5-20 μm tips diameter for electrical connection, a source meter, a thermal control unit, a photodiode (PD), a power meter and spectrometers for emission wavelength detection.

A Keithley 2600 source meter was used to bias the devices using a pair of DC probes. Collimating lenses are mounted on a micrometer positioning stage and can be moved around the platform with micron precision. The light emitted by the laser diodes is collected using a sensing element with a 3 mm diameter germanium (Ge) detector (Thorlabs S122C Ge photodetector) and a flat cleaved fibre for L-I and spectral measurements, respectively. Optical power was measured using a Thorlabs PM100C handheld optical power meter. The diodes were driven by applying a bias current of

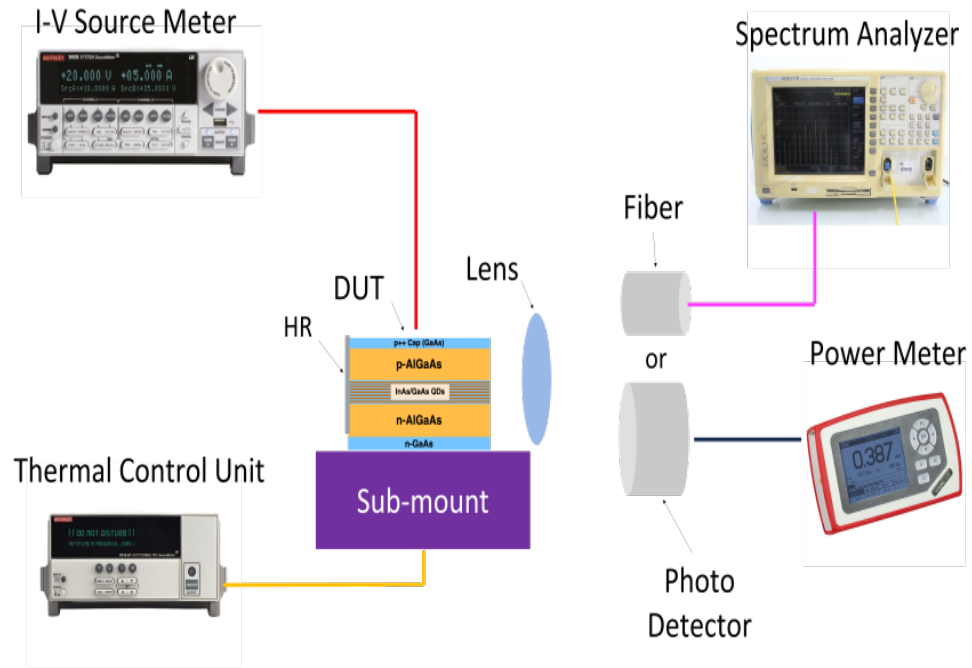


Figure 5.1: Schematic of characterisation setup including a central chuck, electrical contact probes, microscope camera, current sources, power meter, optical spectrum analyser (OSA) and a thermal control unit.

up to 200 mA . The optical spectrum was recorded using an ANDO AQ6317B optical spectrum analyser (OSA) with a resolution bandwidth of 0.01 nm . Collimating lenses were used for both measurements to facilitate alignment. The laser devices, either non-released devices on a GaAs substrate or transferred onto a Si substrate, are placed at the edge of the chuck as shown in Fig. 5.2. A collimating lens and a detector or a fibre at the end of the lens collect the emitted light from the laser diodes.

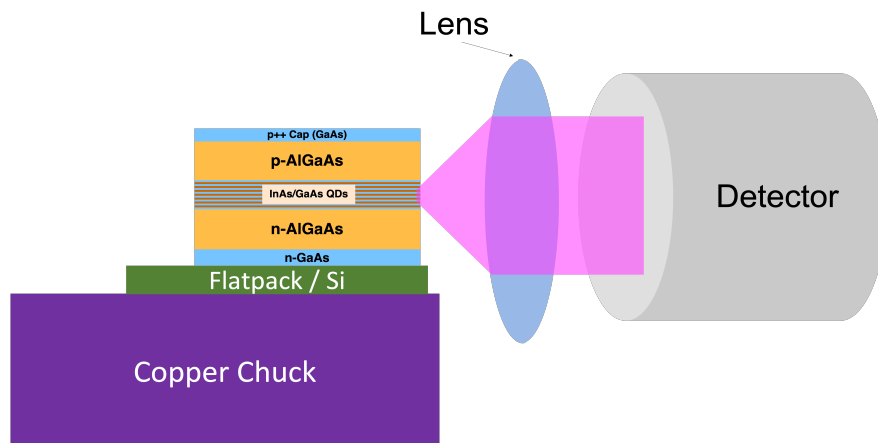


Figure 5.2: Schematic of an edge-emitting GaAs laser mounted on a flatpack or Si substrate on the copper chuck. The positioning stage controls the collimating lens and detector.

Typical measurements include L-I and V-I characterisation of devices in continuous-wave (CW) modes, spectral detection, and their temperature dependence

characteristics. The devices in the setup were controlled by Python [147] scripts and can be found in the Appendix D.

The temperature of the stage on which the chip is placed can be operated up to 120°C. Several devices on the GaAs substrate (before MTP) and on Si wafer (after MTP) have been characterised from each source chip (> 10 lasers) to ensure that the reported values are representative of a particular process.

5.3 QD Lasers Characterisation

5.3.1 First Generation Lasers

5.3.1.1 Design and Purpose

The first-generation lasers are designed to evaluate the baseline material and understand the optimal device dimensions (cavity length and ridge width) for a high-performance single spatial-mode device. The first-generation laser diodes are fabricated on an epitaxial structure (see Epitaxy-A.1). This structure does not contain a sacrificial layer in its layer stack. Thus, non-releasable laser diodes on the GaAs substrate are fabricated by following similar fabrication steps, except for the tether definition and release process as discussed in chapter-2. Once fabrication is complete, the GaAs substrate has been thinned from 480 μm to 120 μm and n-metal has been deposited on the backside of the chips. Subsequently, the Fabry-Perot (FP) laser bars including cleaved and etched-facet mirror devices were then cleaved into different cavity lengths. It is important to note that there is no wavelength control on these devices.

Both cleaved and etched facet lasers with various optical cavity sizes and ridge widths were included in this fabrication run. Due to the necessity of the etched facet in transfer printable lasers, different reflective mirrors were investigated, including conventional etched facet with dielectric coating mirror (no HR metal is implemented in these lasers) and multimode interference reflector (MIR) [98, 148]. The design and fabrication of both mirrors were explained in chapter-2 (section 2.3.3). Based on the findings from the characterisation and performance analysis of the lasers in this run, the transfer printable epitaxial layer stacks and laser diodes were designed and fabricated.

5.3.1.2 Characterisation

Firstly, cleaved facet FP lasers are characterised to understand the material quality without the effect of the etched facets on the mirror. The laser diodes are cleaved into bars of varying cavity lengths ranging from 500 μm to 2.5 mm after substrate thinning and backside n-metal evaporation. There is no coating on the mirror of cleaved-facets

lasers. Both cleaved and etched facet lasers have ridge widths of $2.5\ \mu\text{m}$ and $3.0\ \mu\text{m}$. Etched facet lasers have dielectric protection on both front and rear facets. An optical image of a laser bar is shown in Fig. 5.3(a). The bars are then epitaxy-side-up mounted on ceramic sub-mount (as shown in Fig. 5.3(b)) using a silver conductive epoxy adhesive to handle the chips without damaging the facets during characterisation. The silver epoxy is cured at 125°C for 25 min on a hot-plate in air ambient to improve the adhesion, thermal, and electrical conductivity on the sub-mount.

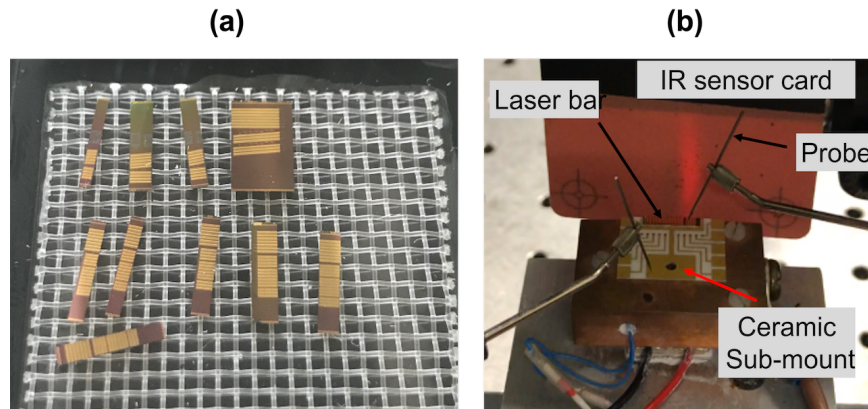


Figure 5.3: (a) Optical image of a laser arrays cleaved into few mm long bars (b) A laser bar under characterisation after being mounted onto a ceramic sub-mount with thermal conductive epoxy.

The light and voltage versus current (L-I-V) curves for the laser diodes were obtained by sweeping a drive current from 0 to $200\ \text{mA}$. Figure 5.4(a) shows the L-I plots of cleaved facet lasers with different cavity lengths, including $700\ \mu\text{m}$, $1.2\ \text{mm}$, $1.7\ \text{mm}$, $2\ \text{mm}$ and $2.5\ \text{mm}$. Lasers with cavity lengths shorter than $700\ \mu\text{m}$ showed non-lasing characteristics. In addition, $700\ \mu\text{m}$ diodes showed an output power of $4\ \text{mW}$ per facet and a threshold current of $50\ \text{mA}$. Laser diodes with cavity lengths of $1.2\ \text{mm}$ and $1.7\ \text{mm}$ show the best performance with a low threshold current of $20\ \text{mA}$ with a slope efficiency of $0.19\ \text{W/A}$ and $0.17\ \text{W/A}$ per facet, respectively. These devices are capable of producing more than $20\ \text{mW}$ per facet with an injection current of $125\ \text{mA}$. As the cavity length increases, the lasers tend to have lower output power at same injection current due to the reduced slope efficiency. In addition, the threshold current increased to $30\ \text{mA}$. The lasers have a turn-on voltage of $1.2\ \text{V}$ with a differential resistance of $\sim 5\ \Omega$ measured in the flat part of the I-V curve ($50\ \text{mA}$ to $150\ \text{mA}$) as shown in Fig. 5.4(b).

The spectral measurements showed that the lasers with $700\ \mu\text{m}$ long cavities exhibit a sole excited state (ES) lasing with a gain peak around $1195\ \text{nm}$ as shown in Fig. 5.5(a). ES emission in QD lasers is typically observed at increased injection current when the ground state (GS) is saturated and unable to provide sufficient gain. Shortening the device length also prevents stable GS stimulated emission due to low material gain and high mirror loss. As the cavity length increases, the threshold

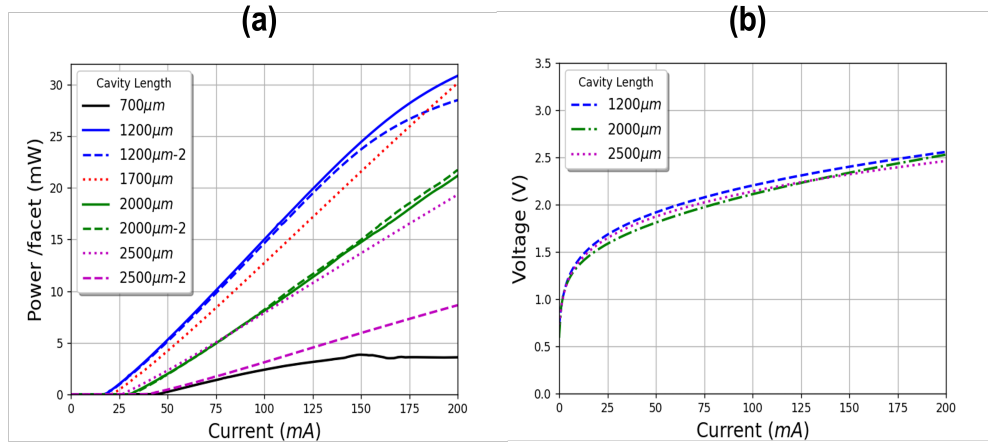


Figure 5.4: (a) L-I plots of the cleaved facet lasers with cavity length from $700\mu\text{m}$ to 2.5 mm . (b) I-V curves show that the devices have turn on voltage of 1.2 V . The lasers with cavity length in 1.2 mm to 1.7 mm exhibits the best performance indicating the optimal cavity size is between 1 to 2 mm .

current for GS emission drops to 20 mA . This is a common behaviour in QD-based lasers, as reported in previous work [91, 149, 150]. The limited gain in the QD active region to compensate for the total loss leads to saturation in the GS gain and an increased population of the ES due to Pauli blocking [151, 152]. This saturation reduces the available states for further carriers transitions in the GS, forcing carriers to populate the excited state (ES). As a result, the ES transitions become more pronounced because the GS cannot accommodate additional carriers for further lasing.

Laser devices with cavities longer than one millimetre emit in the range $1275\text{--}1280\text{ nm}$ with no evidence of peak wavelength switching from the GS to the first ES at pump currents up to 150 mA . Figure 5.5(b) shows the emission of 1.7 mm long cavity lasers at 30 mA and 70 mA drive current. Increasing the injection current leads to a red-shift in the lasers as a result of Joule heating effect. The recorded spectra for 1.2 mm and 2.5 mm long cavity lasers at current density are given in 5.5(c). The peak emission wavelength shows a similar red shift from 1275 nm to 1285 nm with increasing cavity length. This can be attributed to the reduced mirror loss, which allows the laser to lase at lower energy states, corresponding to higher wavelengths, with a low carrier density. Therefore, it is crucial to control the cavity length and improve the heat dissipation capabilities during the design and integration process to achieve an improved wavelength control.

The ultimate laser diodes need to have etched facet mirrors to achieve high-density heterogeneous integration by micro-transfer printing. In this context, a dry etching process is developed for smooth facets and different high-reflective rear mirrors for improved device performance. Further details of the facet etch process and the HR mirrors are presented in chapter-2 (section 2.3.1 and 2.3.3). The performance of these devices has been evaluated by comparing them with similar size cleaved facet

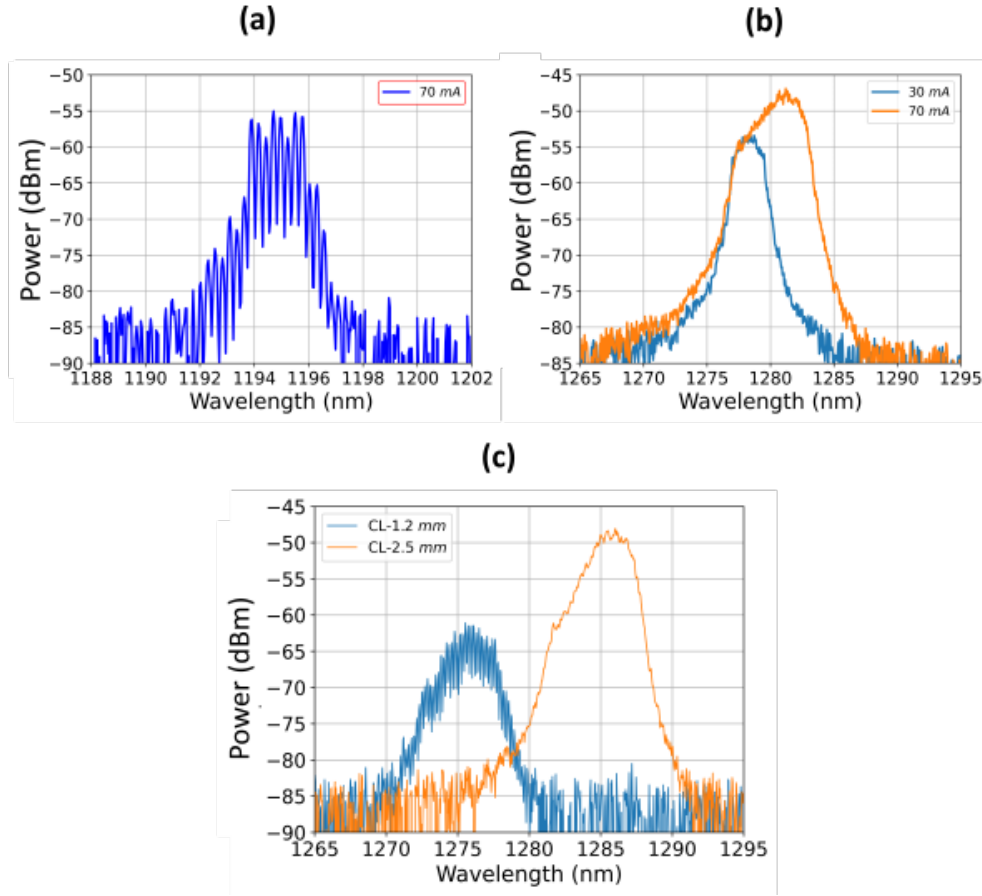


Figure 5.5: Spectrum of cleaved facet lasers with (a) $700\ \mu\text{m}$ and (b) $1.7\ \text{mm}$ long cavity at different bias current. (c) Spectral recording from laser diodes with $1.2\ \text{mm}$ and $2.5\ \text{mm}$ long cavity length at injection current density of $1390\ \text{A}/\text{cm}^2$.

reference lasers.

No lasing was observed in the etched devices with cavities shorter than one millimetre, in contrast to the cleaved facet lasers with similar cavity lengths. This is due to the increased mirror loss and the reduced reflection of the etched facets. Figure 5.6(a) shows several L-I curves for $1\ \text{mm}$ long-cavity etched facet lasers. The laser based on conventional etched facet and MIR with dielectric protection coating mirrors shows similar threshold currents in the range of 30 to $35\ \text{mA}$. As the injection current increases, kinks are observed in most devices after $100\ \text{mA}$ drive current. A few laser devices without kink in their L-I curves show thermal rollover at higher pump currents. This kink indicates ES emission, as discussed in detail below. As the cavity length increases, the kink disappear in the L-I plots as given in Fig. 5.6(b) for the lasers with $1.5\ \text{mm}$ and $2\ \text{mm}$ long cavity and $2.5\ \mu\text{m}$ wide ridge. This suggests that the optimum cavity length for an etched facet laser diode will need to be greater than $1\ \text{mm}$ for stable ground state (GS)-only emission. Very little or no rollover was observed from these devices at the same current levels due to the reduced mirror loss. The lasers with dielectric coating as the rear mirror have a threshold current of $30\ \text{mA}$

with an output power above 15 mW at 150 mA drive current. The increased threshold current compared to cleaved facet lasers is due to the reduced reflectivity of etched facet mirrors.

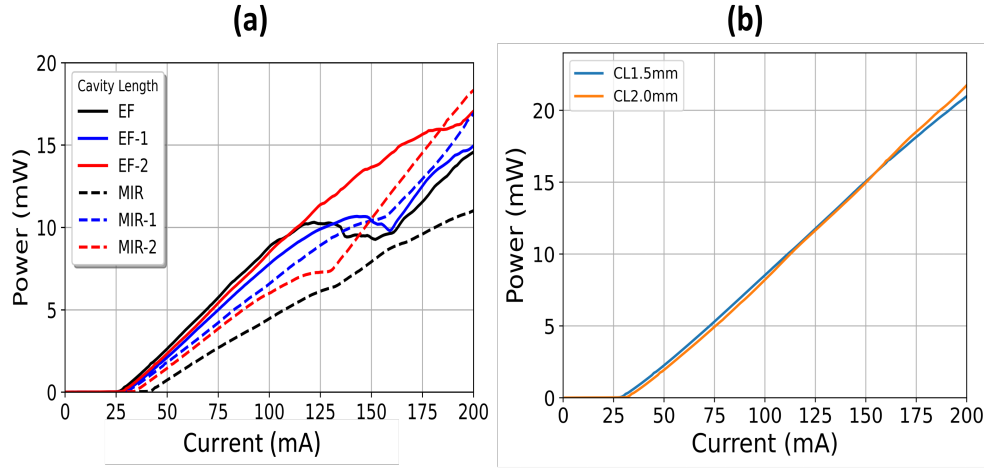


Figure 5.6: (a) L-I curves for 1 mm long cavity etched facet lasers (2.5 μm wide ridge) with different reflective rear mirrors (EF-etched facet with dielectric coating and MIR with dielectric coating) Most lasers show a kink at increased drive current. (b) L-I curve for etched facet lasers with different cavity length of 1.5 mm and 2 mm show similar threshold.

In etched facet lasers with a kink in the L-I curve, two different phenomena are observed. Either saturation in GS and then emission shift from GS (~ 1280 nm) to ES (~ 1200 nm) or dual-state emission. The majority of devices have a flat pattern followed by another rise in the L-I curve corresponding to GS state saturation and dual state (GS + ES) emission, as shown in Fig. 5.7(a). An example spectrum for this laser is shown in Fig. 5.7(b). Above the injection current where the flat is observed, a second peak typically appears around 1200 nm. The second behaviour is only observed in a few lasers where the lasers initially lase in the GS state and then fade out followed by a second lasing as shown in Fig. 5.7(c). The corresponding spectra confirm the initial emission around 1275 nm and the emission fade-out around 100 mA drive current. Then the lasing starts again in the ES state at a wavelength of 1200 nm as shown in Fig. 5.7(d).

This behaviour was not observed for the etched facet lasers that have a cavity length longer than 1 mm, even at high injection current levels. This is due to the higher available gain and reduced mirror loss in the waveguide.

5.3.1.3 Conclusion

This section presented characterisation of first-generation non-transfer printable lasers. The purpose is to evaluate the QD epilayer and the performance of the device. The optimal cavity length and performance of the etched facets formed by ICP dry etching are investigated. Cleaved facet lasers are characterised as reference lasers to

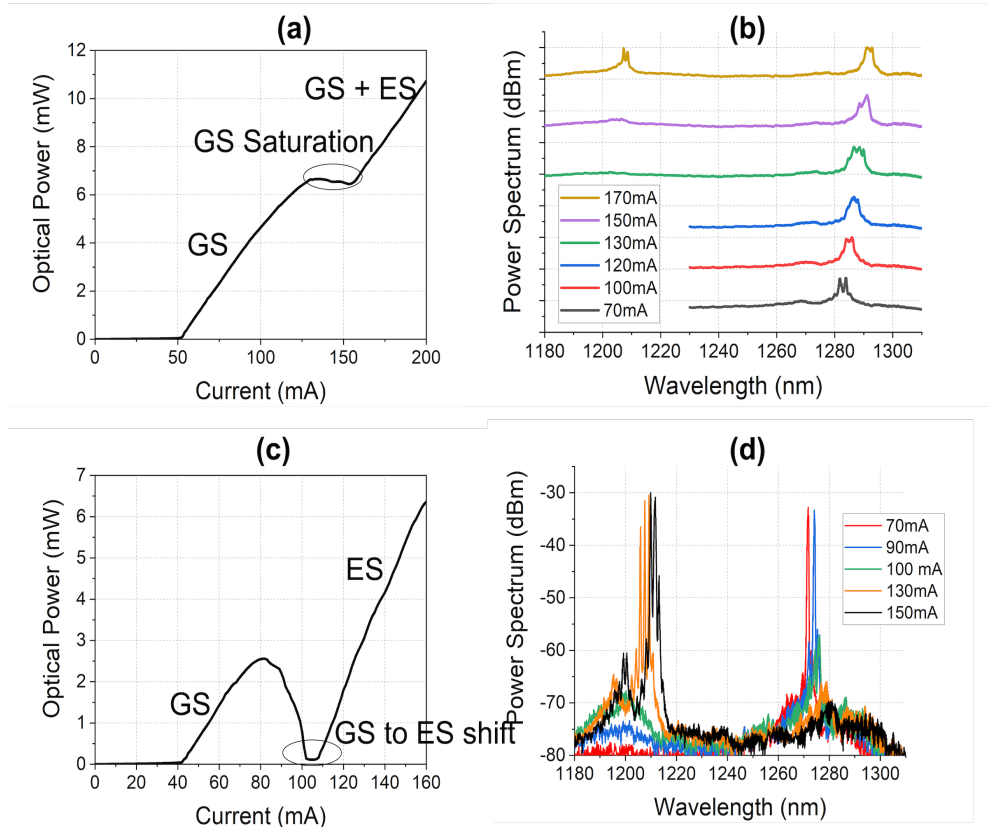


Figure 5.7: (a) L-I curve of 1 mm long etched facet lasers with dual Gs + ES state lasing and (b) the corresponding spectrum. (c) Laser with single GS and ES lasing and (d) the corresponding spectrum.

evaluate the material and etched facet devices of similar size. The analysis shows that the cavity length of the lasers must be at least 1 mm and less than 2.0 mm to obtain the best performing lasers. For cavity lengths longer than 2 mm, internal losses dominate and device efficiency decreases. Typical threshold currents for the laser diodes are between 20-30 mA with up to 30 mW output power per facet. Similar etched facet lasers using dielectric mirrors showed a slightly higher threshold current of 30 mA with a total power of 20 mW. However, 1 mm long etched facet lasers exhibited dual-state lasing or only excited-state lasing due to limited modal gain in the QD ground state. The main learning from the characterisation is that the cavity length of the etched facet lasers should be longer than 1 mm in order to achieve stable GS lasing.

To overcome this problem, the number of QDs in the active regions is increased from 12 to 14 in the transfer-printable materials used for the second- and third-generation lasers, and the device length is set to be at least 1 mm. In addition, further optimisations and process developments in the facet etching process and the metal-dielectric HR and MIR mirrors are carried out as reported in chapter-2.

5.3.2 Second Generation Lasers

5.3.2.1 Design and Purpose

This section describes the characterisation of second-generation transfer printable lasers. The lasers were developed based on the findings of the first-generation of lasers. The second-generation lasers are fabricated using a new-generation epitaxial layer grown by Innolume with 14 QDs layers (see Epitaxy-A.2) in the active region to increase the modal gain. To make these lasers transfer printable, a 500 nm $Al_{0.95}Ga_{0.05}As$ sacrificial layer is included in the epitaxial layer stacks between the device layer and the GaAs substrate. The rectangular laser devices are 65 μm wide and 1.5 mm, 1.8 mm and 2.4 mm long. The corresponding cavity lengths in the lasers are 1.0 mm, 1.5 mm and 2 mm. The ridge widths in the lasers are 2.5 μm and 3 μm . Additionally, reference non-transfer printable cleaved and etched facet lasers with the same size are fabricated in parallel with transfer printable laser coupons on the same chip. The transfer-printable laser diodes are characterized after being transferred to a Si wafer piece with a thin adhesive layer of ~ 70 nm.

5.3.2.2 QD Laser on GaAs Substrate

Initially, the reference cleaved and etched facet lasers on GaAs after substrate thinning and n-metal deposition are characterised. These layers are not transfer-printable and are fabricated on the same epi-layer as the transfer-printable devices. The 500 nm thick AlGaAs sacrificial layer remains in the device structure. Figure 5.8(a) illustrates the recorded L-I curves for the cleaved facet lasers with 1.5 mm and 2 mm cavity lengths. The lasers have a ridge width of 3 μm and threshold currents of 14 and 17.5 mA with a slope efficiency of 0.19 and 0.21 W/A per facet, respectively. These devices did not have a coating on the cleaved facets and produced more than 21 mW of power per facet at a 125 mA drive current. When the performance of the lasers was compared to that of first-generation lasers of similar size, the second-generation cleaved facet lasers showed a 4 mA reduction in their threshold current with a 5 mW increase in output power. The second-generation cleaved facet lasers showed a comparable and slightly better performance than the similar devices in the first-generation. It can therefore be concluded that there is no noticeable degradation in material quality due to the inclusion of the sacrificial layer required for transfer printable lasers. It is also important to note that the epi structures in which the lasers are fabricated are not exactly the same, so a direct comparison is not possible. The second-generation lasers are used as benchmarks for the transfer-printed lasers to evaluate their performance. In addition, the spectrum of a 1.5 mm long cavity laser is shown in Fig. 5.8(b). The emission peak is centred at 1288 nm.

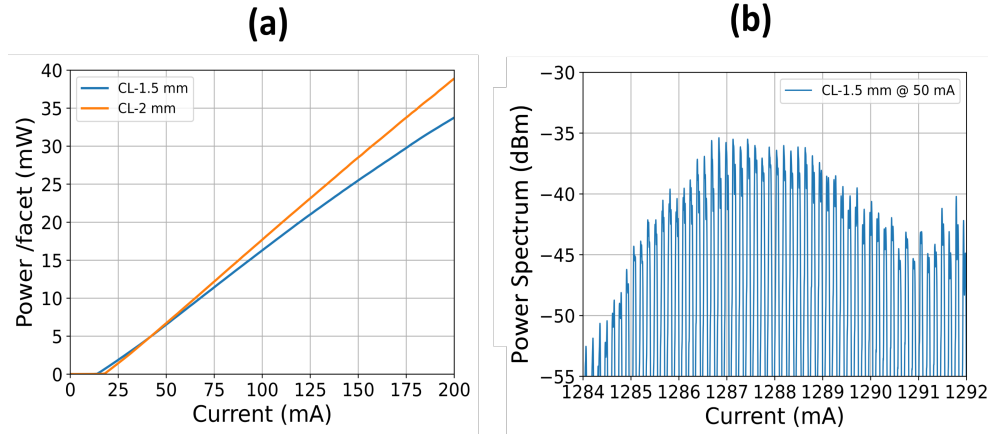


Figure 5.8: (a) L-I plots for cleaved facet lasers without any coating at room temperature. The lasers have a low threshold current below 20 *mA*. (b) Spectrum of a 1.5 *mm* long laser at 50 *mA* bias current showing emission centred around 1288 *nm*.

Reference etched-facet lasers on the GaAs substrate have a dielectric coating on both the front and rear mirrors and a Ti-Au metal HR or MIR mirror on the rear mirror. LI plots for 1 *mm* and 1.5 *mm* cavity lasers are shown in Fig. 5.9(a). These devices exhibit a threshold current between 15-18 *mA* with >20 *mW* output power at 125 *mA* pump current. In addition, although short cavity length devices exhibit better performance with slightly lower threshold and higher output power at lower bias current levels compared to long cavity length devices, a more pronounced rollover is observed in these lasers at higher injection current levels due to GS saturation, as seen for both types of laser. The device has an emission peak of around 1280 *nm* at a 50 *mA* drive current, as shown in Fig. 5.9(b). The emission shift to the excited state (~ 1200 *nm*) that is seen in etched-facet first-generation lasers, is not observed in these lasers at injection current of ~ 170 *mA* where the power saturates (roll-over) because of the increased number of QD layers (in other words, gain) in the epi structure.

Lasers with both metal coated HR and MIR mirrors show comparable performance, indicating similar reflectivity from both types of HR mirrors at the back facets. The facet mirror reflectivity is estimated using the reference cleaved facet ridge lasers by measuring the inverse differential quantum efficiency (η_d) at different cavity lengths L and applying the equation shown in Fig. 5.10. First, the reflectivity of the etched facet mirror is estimated for lasers consisting of an etched facet front mirror and a cleaved facet rear mirror. The GaAs/AlGaAs cleaved facet reflectivity is assumed to be 31%. The reflectivity of the etched facet front mirror is calculated to be 19% with a small percentage error. The high reflectivity metal dielectric coated and MIR based rear mirrors are then estimated using the same approach. Both types of mirrors show similar performance with a reflectivity of 46% with a $\pm 5\%$ error. The high margin of error is due to the use of narrow ridge lasers for the extraction of η_i and α_i in CW mode, which introduce a self-heating effect. The internal differential quantum

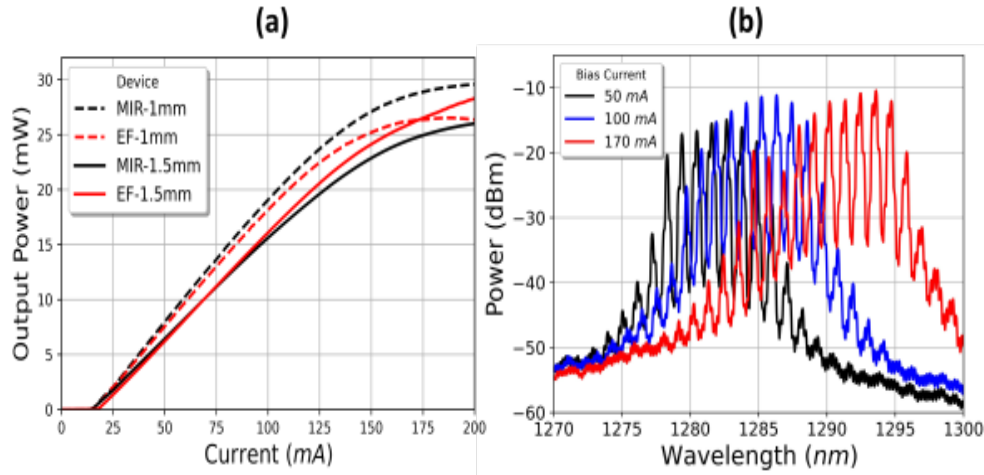


Figure 5.9: (a) L-I plots for etched facet lasers with 1 mm and 1.5 mm long cavity showing a low threshold current below 18 mA. (b) Spectrum of a 1 mm long EF laser at different bias currents shows multi-longitudinal modes around 1282 nm under 50 mA injection current. As the injection current increases the lasers shows a red shift in the emission wavelength due to self-heating.

efficiency (η_i) and the internal loss α_i are given as 79% and 2.5 cm^{-1} , respectively, for the same epi structure using wide area lasers (i.e. $80 \mu\text{m}$ wide ridge) in pulsed mode, providing a more accurate estimate. The difference between the provided and extracted η_i (75%) and α_i (8.4 cm^{-1}) may be related to other factors such as injection efficiency and additional losses. However, the estimated rear mirror reflectivity suggests that more performance can be achieved by improving the reflectivity of both the metal-coated HR and the MIR rear mirror.

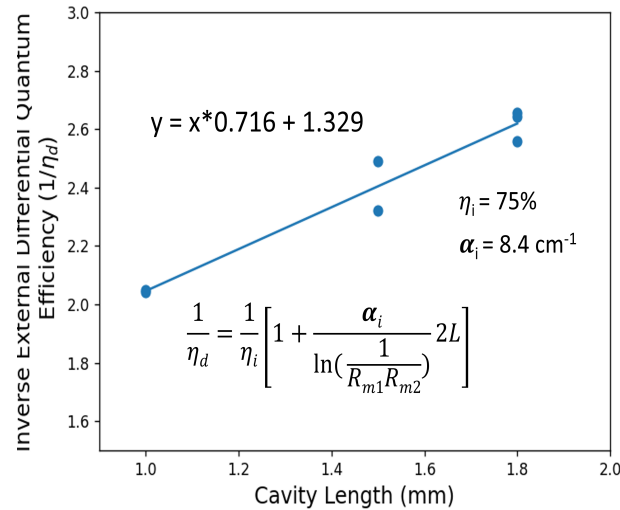


Figure 5.10: Cavity length dependence of the inverse external differential quantum efficiency ($1/\eta_d$) for cleaved facet QD lasers ($3 \mu\text{m}$ wide waveguide) at room temperature in CW mode. The circle indicates experimental data collected from the lasers with different cavity lengths. The blue solid line is the linear fit of the experimental data. The internal quantum efficiency, η_i , is determined from the vertical axis intercept ($1/\eta_i$) of the linear fit line. Inset: The equation used to extract the internal loss (α_i), reflectivity of facets (R_{m1} and R_{m2}). L is the cavity length of the laser.

In addition, no kink and emission shift to 1200 nm are observed in the L-I curves and spectrum of 1 mm long lasers from second-generation devices, even at high injection current. Increasing the number of QDs results in higher modal gain, which leads to stable GS lasing in 1 mm long cavity lasers. Furthermore, the maximum ground state modal gain is estimated to be $\sim 18 \text{ cm}^{-1}$ for the material used in this work. Although QDs lasers with higher modal gain (i.e. $> 46 \text{ cm}^{-1}$) have been reported [153, 154], the devices developed in this thesis showed very good slope efficiency ($> 0.4 \text{ W/A}$).

5.3.2.3 Transfer Printed QD Laser on Si Substrate

Following the characterisation of QD lasers on native GaAs substrate (the sacrificial layer remains in this laser as there is no undercut etch), identical transfer-printable lasers from the same chip have been characterised after they are micro-transfer-printed onto Si host targets. The fabrication, release and transfer printing of these laser diodes is discussed in chapters 2 and 4. First, laser coupons were transferred to the edge of a flat Si substrate with 70 nm BCB adhesive layers to investigate their performance after transfer printing. It should be noted that the Si wafer is a blank wafer and does not contain any waveguide structure on it.

An output power of 21 mW at 100 mA bias current is measured with a threshold current of 16 mA as shown in Fig. 5.11. The etched facet laser has a 6.5 μm wide and 54 μm long MIR back mirror. The diodes have a slope efficiency of 0.24 W/A with a device resistance of 14 Ω . The emission wavelength at 25 mA bias current is around 1284 nm at 20°C and is given in Fig. 5.11(b).

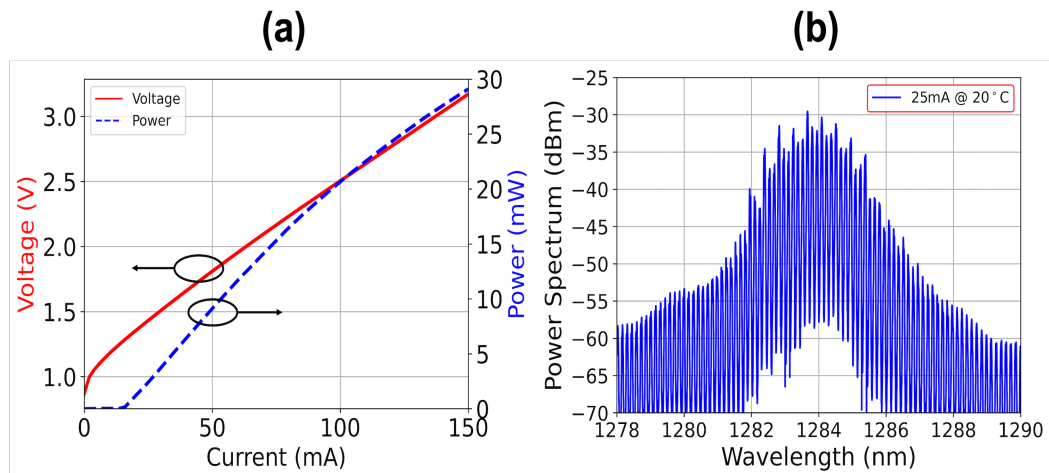


Figure 5.11: (a) L-I-V characteristics for a 1.5 mm long and 2.5 μm ridge QD laser diode transfer-printed on BCB coated Si. The device exhibits 16 mA threshold current with output power above 20 mW at 100 mA injection current. (b) Spectrum of the laser at 25 mA drive current at 20°C.

The performance of the transferred device is compared with that of an identical non-released (and transfer-printed) laser on GaAs substrate fabricated on the same

chip to confirm that there is no degradation in device performance due to under-etching and transfer printing. Both types of laser are fabricated using the same epitaxial layer structure (see Epitaxy-A.2). The laser on the GaAs substrate has its substrate thinned to $120\mu\text{m}$ while the sacrificial layer remains in the epi stack. Both lasers have shown similar threshold currents with slightly different thermal rollover characteristics as shown in Fig. 5.12(a). This is due to the different thermal conductivity of Si and GaAs. A detailed performance comparison of these devices at elevated temperatures is discussed in more detail in later this section.

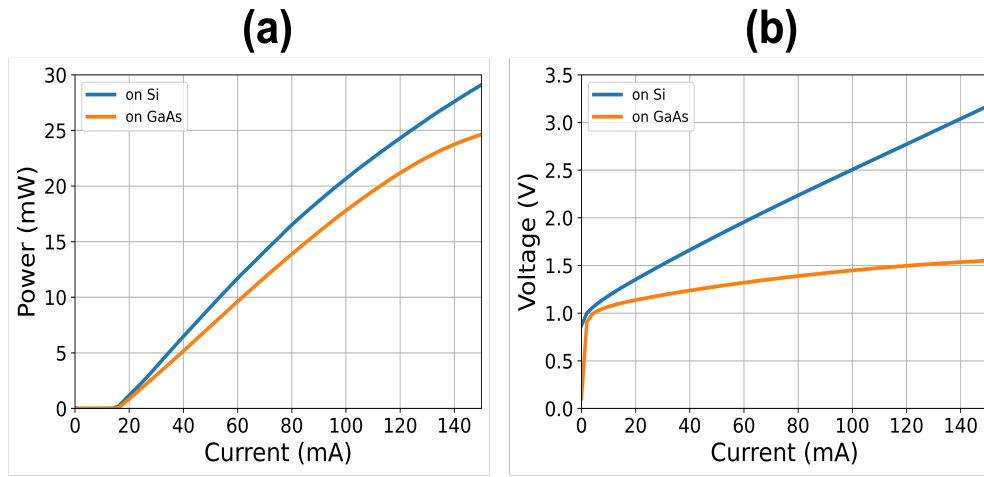


Figure 5.12: (a) L-I and (b) I-V characteristics for a 1.5 mm long cavity QD laser on GaAs substrate and identical transfer-printed device on BCB coated Si substrate at room temperature. Both device exhibits 16 mA threshold current with output power above 25 mW at 150 mA injection current.

The main difference between the two devices is the differential series resistance, which is $3.5\ \Omega$ for the laser on the GaAs source wafer and $14\ \Omega$ for the transferred laser on Si. This is mainly due to the different electrical contact configuration in the devices, as shown schematically in Fig. 5.13(a). The transferred device has its two contacts (n and p metal) through the top of the device (Path-1). The laser on GaAs (non-released), on the other hand, has a p-contact at the top but an n-metal contact at the bottom after the substrate has been thinned to $120\ \mu\text{m}$ (Path-2). As the n-metal must be deposited in a trench that is $16\ \mu\text{m}$ wide and $3.2\ \mu\text{m}$ deep, the precision of stopping at the correct layer (500 nm thick n-GaAs layer) is critical during trench etching. Having too much over-etch into the n-GaAs layers can significantly increase the lateral resistance. Figure 5.13(b) shows an SEM image of a laser cross section showing the laser ridge and the remaining n-GaAs layer with n-metal. The n-GaAs thickness is much thinner in the centre than at the edges because of the footing effect in ICP dry etching. In this laser run, the thickness of the remaining n-GaAs layer is measured to be $\sim 100\ \text{nm}$ and can cause an increase in series resistance of up to $4\ \Omega$. It is also important to note that due to the challenge of direct probing on $30\ \mu\text{m}$ wide contact pads defined on the lasers, poor contacts can add a few Ω of resistance.

Post-print metallisation, which provides a wide contact metal for probing on the sample rather than a direct laser, can mitigate this problem but has not been implemented here.

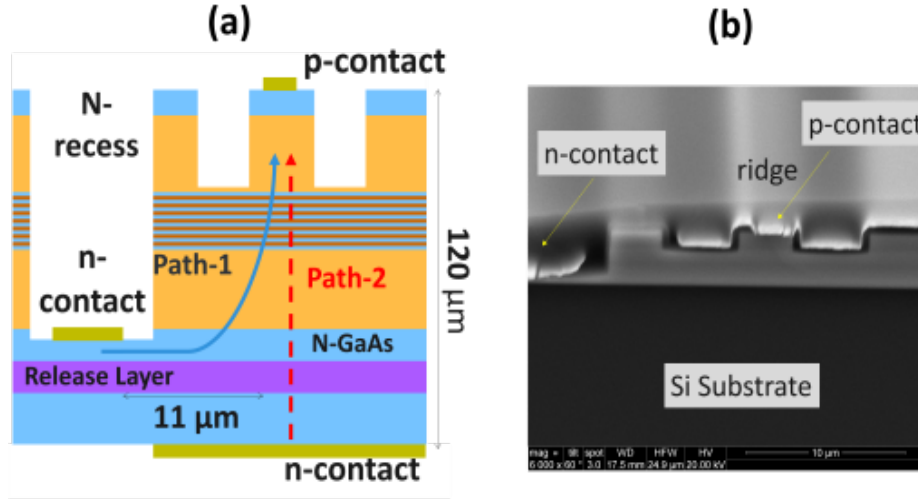


Figure 5.13: (a) Schematic of the electrical contact configuration and current path for both lasers. (b) SEM images of a cleaved laser transfer printed on a piece of Si showing the n-metal inside the trench and the p-metal on the laser ridge.

Another important aspect to consider is how temperature affects the performance of laser diodes. Factors such as threshold current, optical output power, and the spectrum of the FP laser can be greatly affected by the temperature of the active region. Typically, the efficiency of the laser diodes decreases as the operating temperature increases due to the increased thermal escape of the carriers and non-radiative recombination processes [155]. The optical power delivered by the lasers (on the GaAs substrate for non-transfer printed and on the Si substrate after MTP) was measured as a function of drive current for various operating temperatures in CW mode on a temperature controlled stage. Figure 5.14(a) shows the temperature dependence of the L-I curves for etched facet MIR rear mirror ($6 \mu\text{m} \times 54 \mu\text{m}$) lasers on GaAs substrate and on Si with 70 nm BCB. Both lasers have the same cavity length of 1.5 mm and ridge width of $2.5 \mu\text{m}$. The threshold current for the laser diode on the Si substrate was measured as 14 mA at 20°C and increased to 40 mA at 80°C . A similar trend is observed in the laser on the GaAs substrate with a threshold currents of 15 mA and 42 mA at 20°C and 80°C , respectively. The laser transferred to a Si substrate has a few mA lower threshold currents and delivers 15 mW output power at a bias current of 150 mA while the stage temperature is set at 80°C . The identical laser on GaAs delivers 9 mW output power at the same bias current and temperature. The improved thermal performance of the laser on Si compared to the laser on GaAs is due to the superior thermal conductivity of Si ($1.3 \text{ W/cm}^\circ\text{C}$) compared to GaAs ($0.52 \text{ W/cm}^\circ\text{C}$). This also suggests that QD lasers integrated with a thin adhesive layer ($< 100 \text{ nm}$) are not significantly affected. Similarly, improved thermal properties have

been reported for a transfer-printed InP on Si substrate in [136]. In addition, the LI curves for identical (same-size) transfer-printed and non-transfer-printed lasers given in Fig. 5.14(a) also demonstrate that transfer-printed devices have no degradation in performance (i.e. threshold current) after integration onto another substrate.

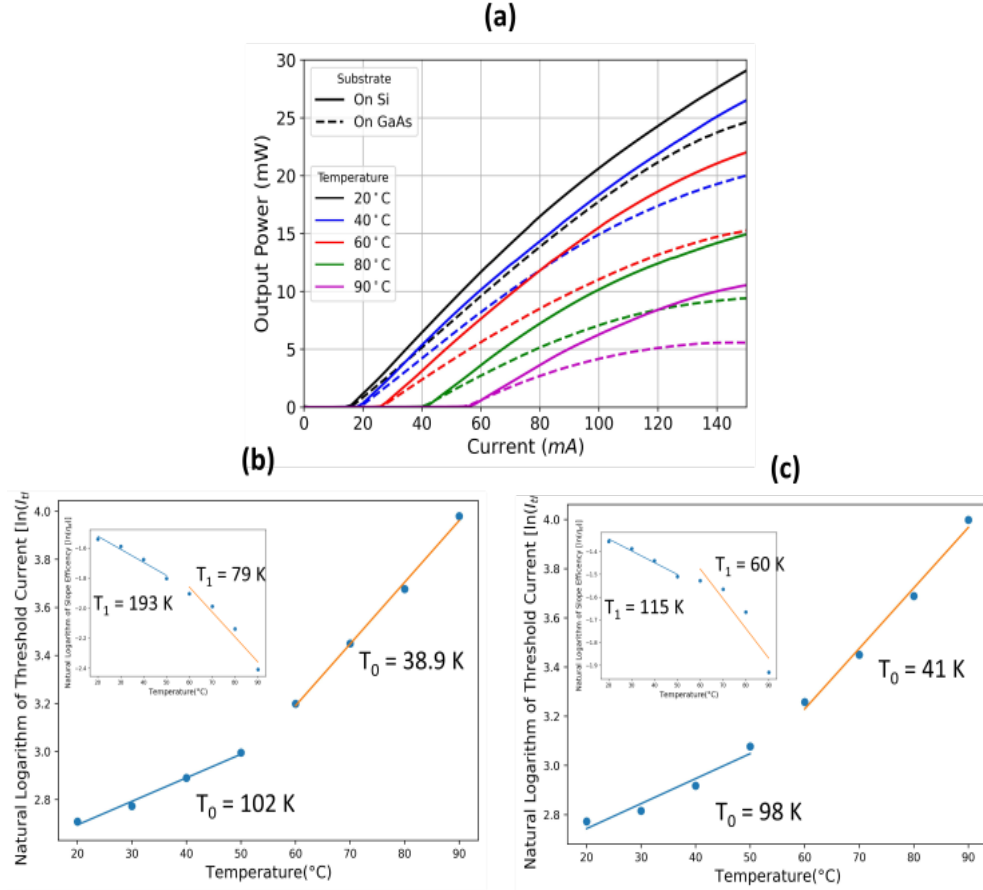


Figure 5.14: (a) Temperature-dependent L-I characteristics as a function of current for lasers on GaAs and on Si with 70 nm BCB. The etched facet lasers have the same size (with 2.5 μm wide ridge and 1.5 mm cavity length) and MIR rear mirror. (b) The characteristic temperature (T_0) of the lasers was determined from the logarithmic threshold current versus temperature plots using the LIs plots shown in (a). The inset shows T_1 that is similarly calculated from the logarithm of the slope efficiency versus temperature plot. (b) T_0 and T_1 (inset) for the laser GaAs substrate.

The thermal properties of the lasers on both native GaAs and Si substrates and their heat sink properties were assessed by measuring the characteristic temperatures (T_0) and (T_1) based on data from Fig. 5.14(a). T_0 represents the temperature sensitivity of the threshold current (I_{th}), which is calculated using the eq. 5.1. Higher T_0 indicates good temperature stability and less carrier leakage at elevated temperatures and is calculated using eq. 5.2. T_1 describes how the external quantum efficiency (η_d) or the slope efficiency changes with respect to temperature. Higher T_1 indicates good temperature stability of the laser's efficiency.

$$I_{th} = I_0 e^{\frac{T}{T_0}} \Rightarrow T_0 = \frac{\Delta T}{\Delta \ln(I_{th})} \quad (5.1)$$

$$\eta_d = \eta_0 e^{-\frac{T}{T_1}} \Rightarrow T_1 = -\frac{\Delta T}{\Delta \ln(\eta_{th})} \quad (5.2)$$

I_{th} is the threshold current, η_d is the slope efficiency, I_0 and η_0 are the fitting parameters, T is the stage temperature and T_0 is the characteristic temperature.

The threshold current of the lasers gradually increased between 20°C and 50°C as shown in Fig. 5.14(b) and (c). T_0 for this temperature range is 102 K and 98 K for the laser on Si and GaAs substrates, respectively. T_1 of the lasers for this range is calculated to be 193 K and 115 K. However, an aggressive increase in I_{th} is observed above 60°C for both lasers on Si and GaAs substrates, with a resulting T_0 of 38.9 K and 41 K between 60°C and 90°C, respectively. This is due to the increased thermal escape of the carriers at elevated temperatures. Although both lasers on Si and GaAs have a similar threshold current, the decrease is more pronounced for the laser on GaAs due to its lower thermal conductivity, as seen in the Fig. 5.14(b) and (c)-insets. At temperatures above 60°C, carrier leakage from the quantum dots becomes significant as the carriers gain sufficient thermal energy to overcome the conduction band offset. This leads to increased carrier leakage into the wetting layer and barrier, resulting in a large increase in the threshold current due to degraded carrier confinement and increased non-radiative recombination.

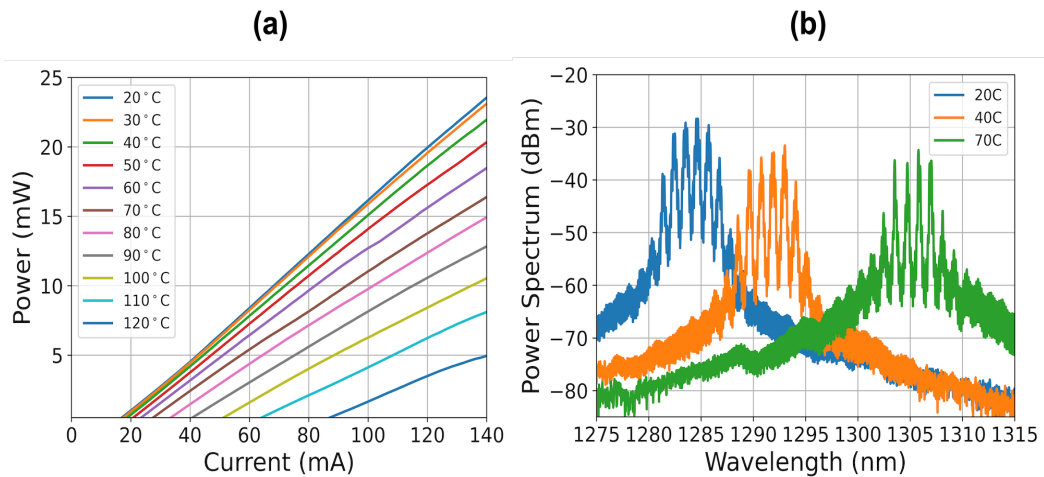


Figure 5.15: (a) Experimental temperature dependence L-I characteristics (L-I-T) for the laser on GaAs substrate in CW mode. 1.5 mm long cleaved facet laser with 3 μ m wide ridge waveguide is operated up to 120°C and delivered 5 mW single facet power at 140 mA injection current. (b) Spectra of the same laser under 50 mA current injection at 20°C, 40°C and 70°C stage temperature.

In order to assess the laser efficiency under different heat-sink configuration, a laser bar (non-released device on GaAs substrate after substrate thinning) is placed directly

on a copper chuck (normally lasers are mounted on a carrier using silver epoxy) and characterised at elevated temperature. The cleaved facet laser (1.5 mm long and 3 μm ridge) with the best L-I-T delivers 5 mW single facet output power at a stage temperature of 120°C, as shown in Fig. 5.15(a). However, similar lasers mounted on ceramic submounts begin to fade at around 100°C (LI curve in Fig. 5.14 with dashed line). This indicates that an improved heat sink allows the laser diodes to operate in a higher temperature environment above 120°C. In addition, analysis of the FP mode wavelength shift can provide valuable insight into the thermal characteristics of the device. The peak wavelength of the laser exhibits a red shift towards longer wavelengths with increasing temperature, as shown in Fig. 5.15(b). A wavelength shift of 0.35 nm/°C and 0.46 nm/°C is measured between 20°C and 40°C and 40°C and 70°C, respectively. The increase in shift at higher temperatures is due to a decrease in the band gap energy and increased Joule heating and carrier leakage [156]. The corresponding band-gap shift is about 15 meV between the emission wavelength at 20°C and 70°C. It is important to note that the LI curves and spectrum are measured in CW mode, which causes the actual temperature in the active layer to be higher than that provided by the temperature-controlled stage.

5.3.2.4 Conclusion

This section reports on the characterisation of second-generation InAs/GaAs QD lasers developed on the basis of first-generation non-transfer printable lasers. The fabricated chip contains transfer printable lasers and reference lasers (non-released device on GaAs substrate) with the same design. Initial characterisation of the reference lasers, including cleaved-facet and etched-facet diodes on the GaAs substrate, allowed evaluation of the epitaxial material quality and laser performance. These devices exhibited a threshold current below 18 mA and an output power above 20 mW at an injection current of 125 mA at 20°C. The emission peak shift from the GS to the ES observed in the first-generation laser with a cavity length of 1 mm is not observed in the second-generation lasers due to the increased number of quantum dots (QDs) that provides more gain. The reflectivity is estimated to be 19% for the etched facet front mirror and 46% for the metal dielectric coated and MIR based rear mirrors. This indicates that the MIR mirror has a similar performance to that of a metal dielectric based HR mirror.

In addition, transfer printable lasers fabricated in the same run with reference non-transfer printable devices are also characterised and compared with the reference lasers. Performance analysis showed that the laser diodes showed no sign of performance degradation after transfer to Si wafers. The laser (1.5 mm long cavity with MIR rear mirror) transferred to Si showed a threshold current of 16 mA with an output power of 24 mW at 120 mA drive current. This device exhibited superior results at elevated temperatures with an output power of 12 mA at the same injection

current at 80°C stage temperature. However, the increased series resistance in transfer-printed lasers (14 Ω) and the low reflection from the metal-dielectric HR rear mirrors still need to be addressed.

5.3.3 Third Generation Lasers

5.3.3.1 Design and Purpose

A third generation of transfer printable laser coupon fabrication was carried out to address issues such as high series resistance and poor HR performance. The first-generation lasers were used to determine the optimal cavity length for the QD-based light source. The second-generation lasers were then used to investigate the performance of the transfer-printable light source and reflective mirrors. Based on these findings, a new mask set is designed for the final generation laser, with a corresponding process improvement reported in chapter-2. For this run, a new epitaxial layer structure was grown that included small changes in its layer stack, such as reducing the Al content from 95% to 93% in the AlGaAs sacrificial layer to reduce oxidation and increasing the thickness of the n-GaAs layer from 500 nm to 600 nm to relax the etch-depth control to reduce the lateral resistance (see Epitaxy-A.3). In addition, the fabrication process has been updated with some modifications to improve the device performance and light-coupling efficiency into the waveguides. The aim is to improve the facet profile using a dual dielectric-hard mask layer during ICP dry etching and the reflectivity in the rear facet using a sputtered Al high-reflection (HR) coating, as well as to reduce the series resistance of the laser diodes. Another issue addressed in this run is the elimination of the front ledge on the coupon to improve longitudinal alignment during integration for better edge coupling to the Si waveguide. More details of these developments and optimisations are discussed in chapter-2 in section 2.3.2.

5.3.3.2 QD Laser on GaAs Substrate

Initially, the reference cleaved/etched facet lasers on GaAs after substrate thinning and n-metal deposition are characterised. This laser has a cleaved-facet front mirror and etched-facet rear mirror with metal HR coating, as shown in Fig. 5.16(a). The laser diode shows a threshold current of 17 mA and an output power above 30 mW at an injection current of 120 mA. LI plot for the measured laser is given in Fig. 5.16(b). Although the threshold current is similar to that of the laser in second-generation, the final-generation devices exhibit improved output performance with more than 30 mW power (the power for a similar size second generation laser is 22 mW) at 120 mA injection current. Laser without any wavelength control emit around 1285 nm as seen in Fig. 5.16(c).

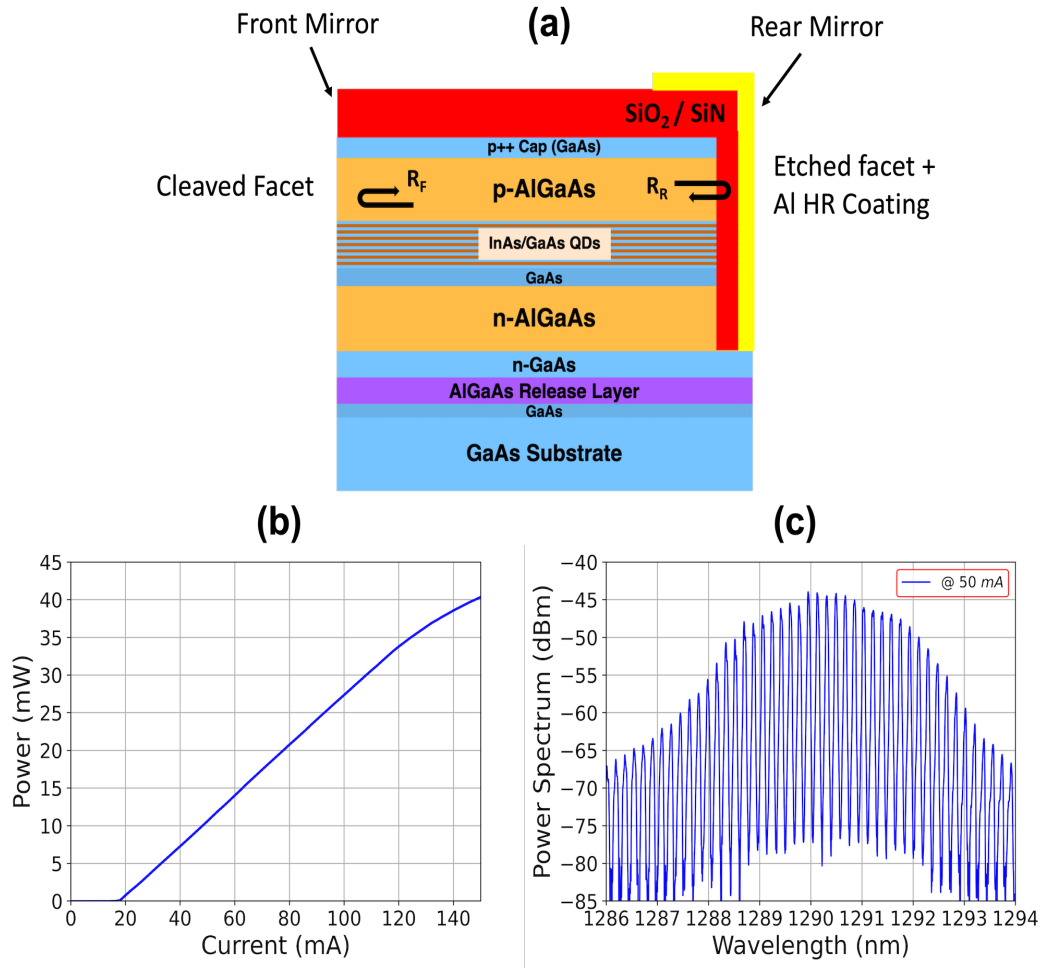


Figure 5.16: (a) Schematic diagram of the facet configuration in the reference lasers. (b) L-I plot of a 1.2 mm long cavity and 3.0 μm ridge laser with cleaved front facet and metal-dielectric coated etched rear facet showing a threshold current of 17 mA. (c) Recorded spectrum of the same device at 50 mA injection current at 20°C.

The implemented mirror configuration (seen in Fig. 5.16(a)) also simplifies the evaluation of the Al HR coating performance given that the front facet reflection is $\sim 31\%$ for cleaved-facet GaAs. A set of identical lasers with and without Al HR mirrors is fabricated and characterised. All of these lasers have cleaved front facets with no coating, while a protective dielectric coating is applied to the etched-facet rear mirror. The Al HR mirror is then sputtered on top of the dielectric layer in every second device. Characterisation of adjacent devices reveals that the Al mirror almost doubled the output power until 100 mA drive current. LI plots of two lasers with a 1.2 mm long cavity and a 3 μm wide ridge are given in Fig. 5.17(a). The lasers have threshold current of 18 mA and 27 mA for dielectric + HR coated (blue) and only dielectric coated (orange) mirrors, respectively. The reflectivity of Al HR is estimated as 89% with a $\pm 5\%$ error following a similar analysis in Fig. 5.10. In addition, Fig. 5.17(b) compares the same size of the etched facet laser with Ti-Au HR coating (from 2nd generation) and Al HR coated (from 3rd generation) lasers. There is a ~ 2 mA

reduction observed in the threshold current of the same-size lasers in 3_{rd}-generation device. In addition, a significant improvement in output power and slope efficiency is achieved with a >40% increase. The 3_{rd}-generation laser delivered 30 *mW* of power at 120 *mA* of drive current with a slope efficiency of 0.29 *W/A*. At the same bias current, the laser from 2_{nd}-generation showed a total output power of 21 *mW* with a slope efficiency of 0.20 *W/A*. It should also be noted that although the epitaxial structures contain the same number of QDs, they are grown with slight modifications in their stacks, including different Al content 93% (was 95%) and n-GaAs thickness 600 *nm* (was 500 *nm*). This may have an impact on the reported values and makes it difficult to directly compare devices of different generations.

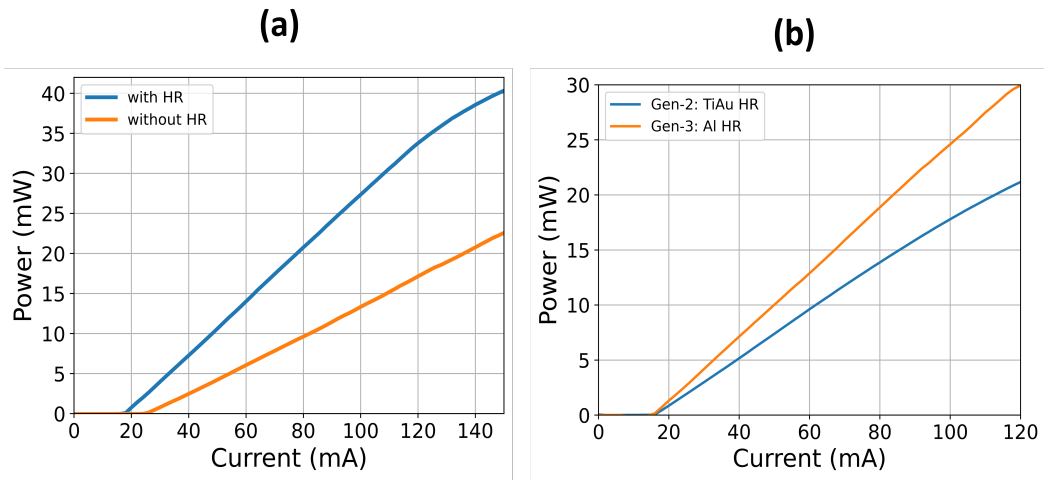


Figure 5.17: (a) LI records for lasers (1.2 *mm* cavity and 3.0 μm ridge) with cleaved front-facet but dielectric + Al HR or only dielectric coated etched facet. HR coating doubles the amount of output power.(b) Comparison of etched facets same size devices (1 *mm* long cavity with 3.0 μm ridge) with dielectric + Al and dielectric + Ti-Au coating on GaAs substrate.

The temperature dependence of the LI characteristic for etched-facet with an HR mirror laser (with 1.8 *mm* long cavity and 2.5 μm ridge) placed directly on a copper chuck is recorded up to 130°C as shown in Fig. 5.18(a). The laser can deliver over 10 *mW* of power at 130°C with a 175 *mA* injection current. The threshold current gradually increased from 24 *mA* to 50 *mA* as the stage temperature increased from 20°C to 100°C with the laser operating in CW mode. Above 100°C, the effect of temperature on device performance is more prominent. The main emission peak is shifted to a longer wavelength in the CW mode operation and is about 16 *nm* when the stage temperature increases from 20°C to 70°C as shown in Fig. 5.18(b). The change in emission wavelength within the specified temperature range is measured as 0.32 *nm/°C*. The shift is slightly lower compared to the second-generation where it was 0.35 *nm/°C*. The reduction in red shift with respect to bias current in the final lasers is due to improved rear mirror reflectivity, which enables the laser to achieve the gain required for lasing at a lower carrier density.

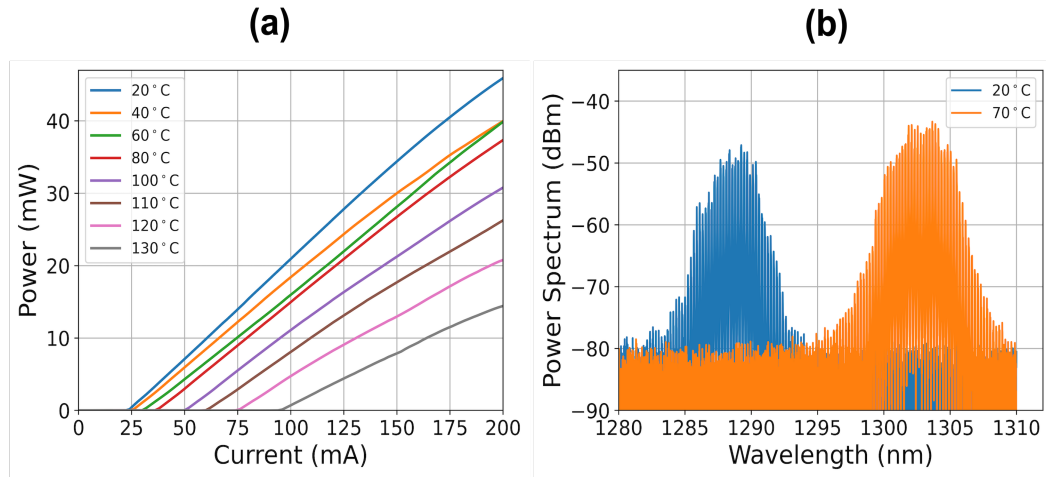


Figure 5.18: (a) LI curve of etched facet laser (1.8 mm long cavity and 3 μm wide ridge) with Al HR mirror on GaAs substrate at different stage temperature. (b) Spectrum of the same device under bias current of 50 mA at 20 C and 70 C.

5.3.3.3 Transfer Printed QD Laser on Si Substrate

The transfer printable etched facet laser coupons are characterised after transfer printing on the edge of a Si wafer with 70 nm BCB adhesive layer as shown in Fig. 5.19(a)-inset. The output light is collected from the cleaved side of the Si substrate. The etched facet laser with 1.5 mm long cavity and 3 μm ridge waveguide has a threshold current of 15 mA at 20°C. The laser has an Al HR coating on its rear facet. The laser produces an output power of 56 mW at 150 mA drive current with a slope efficiency of 0.42 W/A. At the same bias current, the second-generation laser on Si had a power of 29 mW with a slope efficiency of 0.24 W/A. This indicates that the output power is almost doubled with a 75% increase in slope efficiency. The temperature dependence of the LI characteristic of the device is recorded up to 70°C as shown in 5.19(a). The output power drops to 41 mW at 70°C stage temperature. The T_0 of the laser is calculated to be 129 K between 20 to 60°C as shown in Fig. 5.19(b)-Inset. The resistance of the transfer-printed laser is measured to be 8 Ω . It was 14 Ω for the previous generation lasers (see Fig. 5.11(b)). The improvement is achieved by precise control of the dry etch depth and by changing the pre-treatment before n-metal evaporation from ammonia:DI (1:10) for 15 sec to BOE for 5 sec. The spectrum of the laser at 40 mA drive current with emission peaks centred around 1285 nm is shown in 5.19(c).

The third-generation lasers show a significant improvement in terms of device performance. The improvement is achieved by several optimisations, including facet-etching, Al-based HR mirrors, and reduced series resistance.

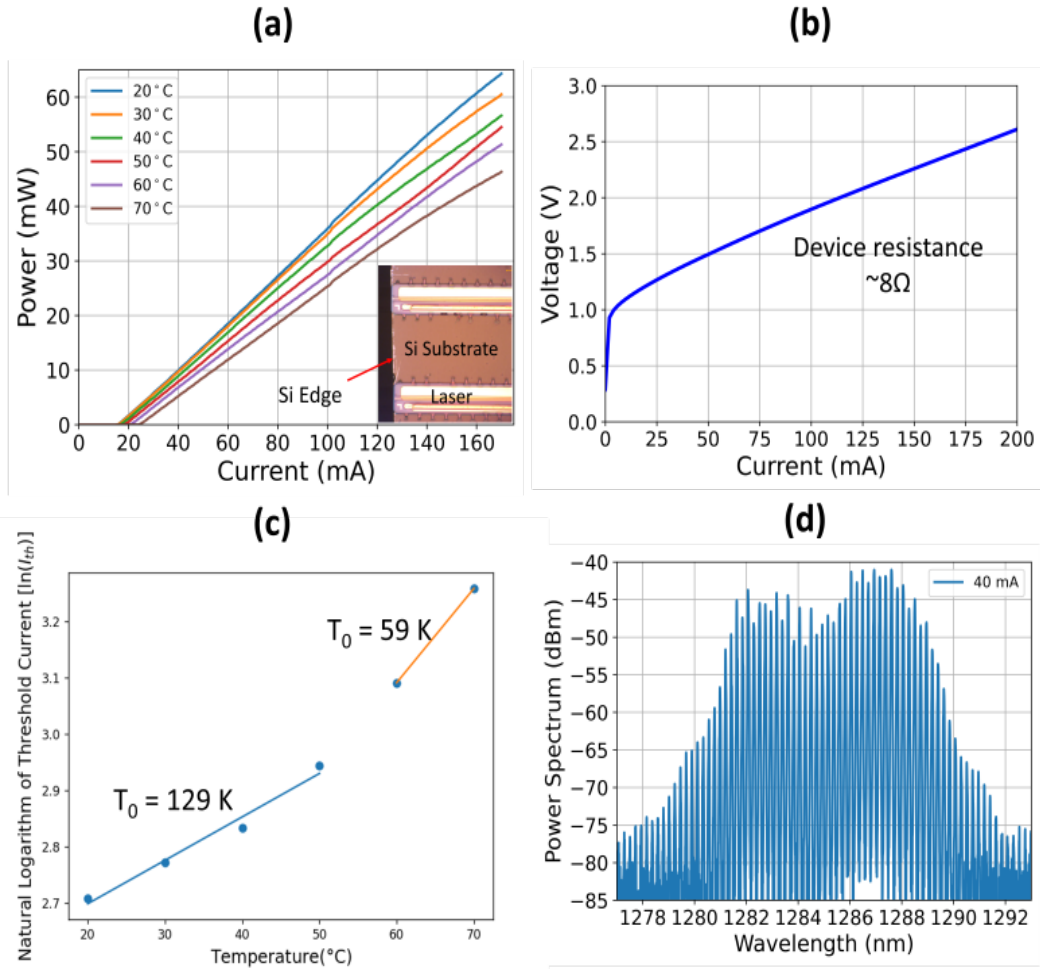


Figure 5.19: (a) LI curve of a transfer-printed etched facet laser (1.5 mm long cavity and 3 μ m wide ridge) with an Al HR back mirror on a Si substrate at stage temperatures of 20 °C and 70 °C. The inset shows the lasers printed at the edge of a Si wafer. (b) IV curve of the same laser at room temperature. The device has a turn-on voltage of 1 V and a series resistance of 8 Ω (between 50 to 125 mA). The inset shows the extraction of the characteristic temperature for the device in the given temperature range. (c) Spectrum of the same device at a bias current of 40 mA at 20 °C.

5.3.3.4 Conclusion

This section reports on the characterisation of the third generation of transfer printable QD lasers. The improvements and resulting device performance are discussed and compared with previous second-generation lasers. First, the reference lasers, including cleaved facet and etched facet diodes, on the GaAs substrate are characterised to evaluate the Al-based HR and to estimate its reflectivity. The cleaved front facet and dry etched Al coated back facet lasers exhibited a threshold current below 20 mA and an output power above 35 mW at an injection current of 125 mA. The emission peak was centered around 1285 nm. The Al HR mirror reflectivity is estimated to be 89%.

The lasers printed on Si with a 70 nm thick BCB adhesive layer are then characterised and compared with reference lasers on GaAs. The devices show a threshold current of

15 mA with an output power of 60 mW with a bias current of 200 mA. The lasers on Si exhibit better performance than those on GaAs as a result of improved thermal conductivity. Similar behaviour has also been observed in second-generation lasers on Si substrates with a thin adhesive layer. In addition, the developed laser can deliver more than 40 mW at 70°C. This indicates that the latest generation of etched-facet transfer-printed lasers can deliver over two orders of magnitude more output power than a similar second-generation device. The high series resistance in transfer-printed lasers is reduced from 14 Ω to 8 Ω in the final laser run. This allows the devices to operate at a lower thermal load with improved efficiency.

5.4 Conclusion

This chapter presents a characterisation and performance evaluation of the developed transfer printable QD lasers. Three generations of lasers were designed and fabricated for the incremental development of transfer printable laser diodes. Laser diodes on GaAs substrates after substrate thinning and n-metal evaporation were characterised and used as a benchmark for transfer-printed lasers to inspect the impact of transfer-printing. Characterisation of identical devices (fabricated on the same chip with the same dimensions) transfer printed on Si substrate revealed that these devices showed better performance in terms of threshold current and efficiency. That indicates that there is no degradation in device performance due to transfer printing. The first-generation of lasers allowed material and etched facet laser evaluation with determination of the optimum laser cavity length. The tendency of the emission shift from the ground state to the excited states in short cavity etched facet lasers indicates that the cavity length should be longer than 1 mm. Based on these findings, the number of dot layers in second-generation laser structures is increased to provide more optical gain, and the cavity length is set at 1 mm to 2.0 mm for best performance. In addition, an AlGaAs release layer is included in the epilayer stacks to enable the fabrication of transfer-printable laser coupons.

Key metrics	Number of Laser Generation					
	Generation-1		Generation-2		Generation-3	
Substrate	GaAs	Si	GaAs	Si	GaAs	Si
$I_{th}(mA)$	30	-	18	16	16	15
$P_{out}(mW)@120mA@20^{\circ}C$	11	-	21	24	30	42
$P_{out}(mW)@120mA@70^{\circ}C$	-	-	7.5	12	20	32
Slope Efficiency(W/A)	0.125	-	0.23	0.24	0.29	0.42
HR Reflectivity(%)	17	-	44	44	87	87
Series Resistance(Ω)	5	-	3.5	14	3.5	8

Table 5.1: Summary of device performance from different generations. An etched facet laser with 1.5 mm cavity length from each generation is used for comparison.

Characterisation of transfer printable devices on Si substrate shows that the lasers are capable of producing optical powers of up to 24 *mW* at 120 *mA* drive current with a threshold current of 16 *mA*. The laser on Si substrate delivers an optical power of 12 *mW* at an elevated stage temperature of 70°C. However, the high series resistance (14 Ω) and the low reflectivity of the metal mirrors (46%) are the two main problems with these devices. Following a series of design and process optimisations to overcome these problems, the latest generation of lasers is fabricated. The characterisation of the lasers on Si substrate shows a threshold current of 15 *mA* with an output power of over 42 *mW* at 120 *mA* bias current. This indicates a 75% increase in the delivered power when compared to the same size second-generation device at the same drive current. The same device produces an output power of 32 *mW* at 70°C. In addition, the series device resistance is reduced to $\sim 8 \Omega$ and the HR mirror reflectivity is increased to 89%. A summary of performance evaluation of the lasers is presented in table-5.1.

Chapter 6

Micro Transfer Printed QD Lasers on Different Silicon Photonics Platforms

This chapter presents characterization and performance evaluation of the QD lasers integrated onto the waveguiding platforms discussed in chapter-3 (section-3.2). The edge-emitting GaAs QD laser coupons are integrated on these platforms through micro-transfer printing technique. The devices are transfer-printed using a pre-patterned single-post PDMS stamp, which allows a single device to be picked-up and printed onto the hosting substrate in one cycle. The post size is selected based on the coupon size to maximise print yield. Most of the prints are made in manual mode sequentially with an overall print yield of over 90% for each of the platforms studied. In addition, the achieved alignment accuracy and proposed solutions for improvement are presented along with the coupling efficiencies, alignment tolerances, and integration advantages and disadvantages for each platform.

6.1 220 nm SOI Waveguide

The first platform is the imec 220 nm silicon photonics platform (iSiPP50G). The 220 nm thick Si waveguide is cladded between a 2 μm buried oxide (BOX) and a 5 μm thick SiO₂ over-cladding. The rectangular trenches on SOI that facilitate edge-coupling are 120 μm wide and 2.5 mm long to accommodate the QD lasers up to 2.4 mm long. These recesses are 7 μm deep and accurately stop at the interface to the Si handle wafer surface. The target SOI wafers are diced into smaller pieces with one or two reticles to be handled on the lab-scale transfer printer. After acetone-IPA cleaning, the samples were sent to EV Group for spray-coating adhesive bonding layers (BCB and InterVia).

Several QD laser coupons from second-generation (36 coupons in total, 12 for each length) are transfer printed into the trenches with a 100 nm BCB adhesive layer. A 100% pick-up and print yield was achieved for all lengths (1.5 mm, 1.8 mm and 2.4 mm) using a 60 μm wide PDMS stamp of the corresponding length. The width of the coupons is fixed at 65 μm . Figure 6.1(a) illustrates the trenches on the photonic chip populated with one laser per recess on the 100 nm BCB spray-coated adhesive layer on the SOI wafer. The emitting facet of the laser coupon is printed as close as possible to the receiving Si waveguides buried in the trench sidewall. There are different Si receiving waveguides with single, double, and triple tips on the same SOI as discussed in section-3.2.1 in details.

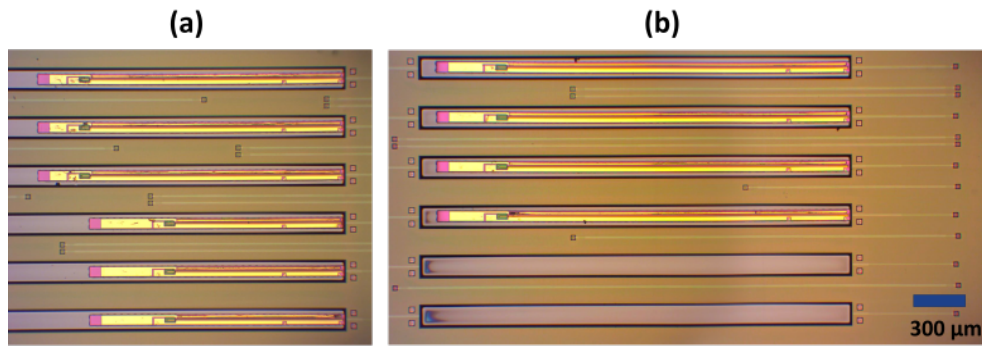


Figure 6.1: Images of transfer-printed QD laser coupon with (a) 1.5 mm & 1.8 mm and (b) 2.4 mm length onto BCB coated trenches on SOI wafer. Focused images of laser printed next to (c) single tip inverse tapered, (d) double trident and (e) triple trident waveguides.

Following the tether photo-resist removal and BCB curing, the electrical and optical measurements of the integrated laser diodes are conducted in CW mode at room temperature. The longitudinal spacing between laser and waveguide is in-filled with a refractive index matching polymer (Norland 61 UV sensitive fiber glue with refractive index of 1.56) followed by 4 min cure under 365 nm LED. Figure 6.2 schematically illustrates a transfer-printed laser inside a recess on SOI with the in-fill. The light emitted by the laser is first coupled into the Si receiving waveguide and then the waveguide coupled power is collected using a 10° tilted flat cleaved single mode fiber through surface grating. The power values reported in this work correspond to the waveguide-coupled power, after calibration of the loss in the surface grating coupler. The coupling efficiency of the grating couplers is determined by measurement of the reference waveguide structure with two gratings at each end on the same chip.

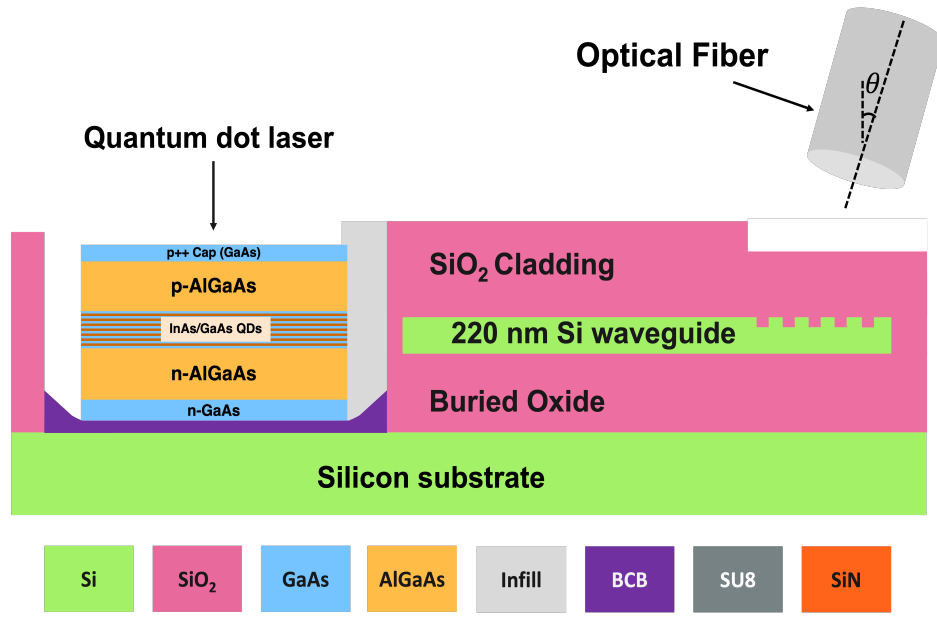


Figure 6.2: Schematic of coupling from a laser printed in SOI trench to 220 nm Si waveguide and then to single mode fiber through the out-coupling grating.

Figure 6.3(a) shows an optical image of the laser placed in the cavity. A pair of probes provides the electrical current to the device and a flat cleaved fibre collects the light through a surface grating structure. A fibre glue covers the front facet of the laser and fills the gap between two facets as shown in Fig. 6.3(a)-inset. It is worth noting that it is difficult to ensure that the gap is completely filled without gaps or bubbles. In this work, the infill material is applied manually and visually inspected under an optical microscope.

The waveguide-coupled output power of the lasers as a function of the injection current is shown in Fig. 6.3(b) for receiving waveguides with different tip configurations (single, double and triple tips waveguide. The best performing device for each coupler design is shown in this plot. The experiment was performed in CW mode at room temperature without being the chuck temperature controlled. More than 1 mW waveguide coupled power is recorded from all devices at 100 mA injection current with a threshold current ranging from 20 mA to 25 mA. It is important to note that the power reported in this thesis is the internal waveguide power (waveguide-coupled power), which is estimated after taking into account the loss due to chip-to-fiber coupling. The chip-to-fiber coupling efficiency through the surface grating coupler (GC) is measured to be around -6 dB for these samples. The variation in coupled power and threshold current could be related to these variations in misalignment and laser performance. In addition, the Si waveguide with the triple-tip configuration shows slightly better coupling performance compared to the double-tip and single-tip Si waveguides, as seen in Fig. 6.3(b). The measured coupling efficiency for the best performing device is calculated to be 6% (-12 dB) by

dividing the waveguide coupled power, after calibration using the GC loss, by the power measured from the reference laser printed on Si at the same injection current of 80 mA. The L-I curves of the reference lasers for the second- and third-generation transfer-printable devices are shown in Fig. 6.3(c). The variation in the coupled power into the waveguide can be because of variation in laser performance and misalignment, and grating coupler to fiber coupling loss.

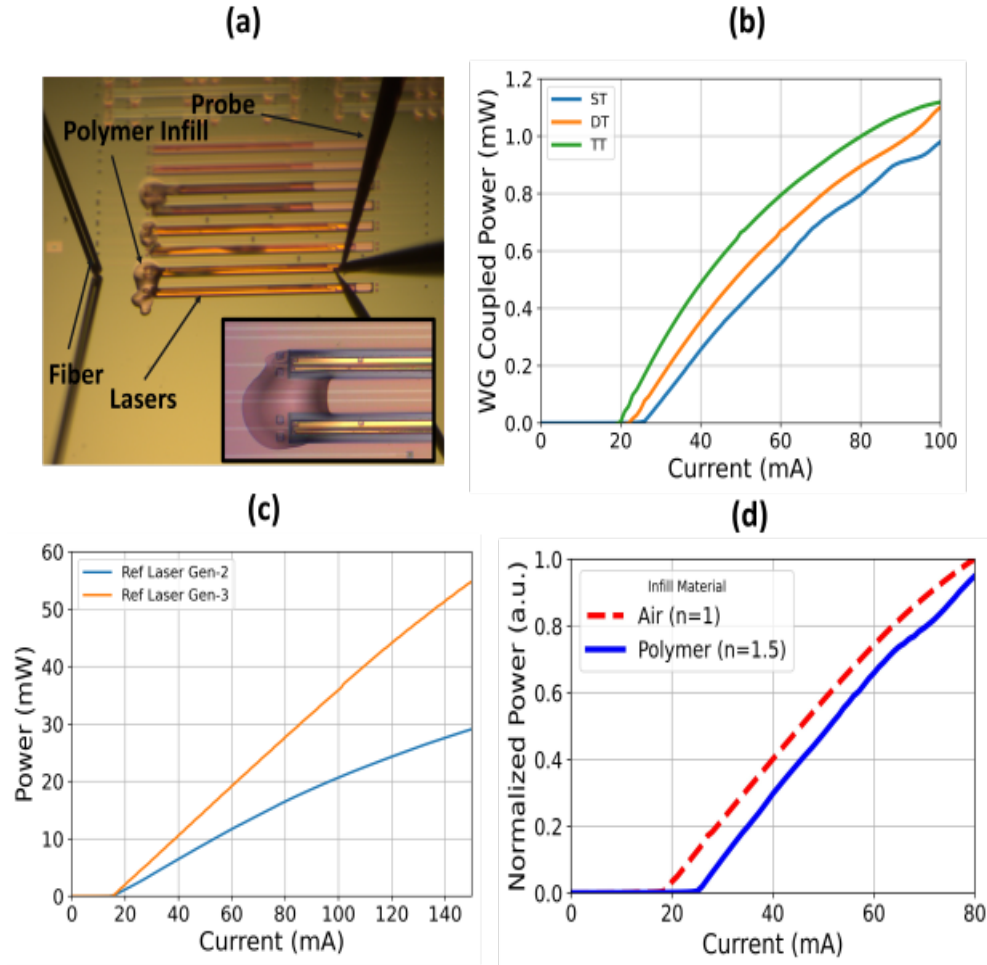


Figure 6.3: (a) Optical image of a laser under test being probed and a flat cleaved fibre collecting the light. The inset shows the laser after polymer infill applied to cover the gap between the facets. (b) LI curves of the lasers integrated on 220 nm waveguides with single tip (ST), double tip (DT) and triple tip (TT) waveguide configurations. (c) L-I plots for the reference transfer-printed lasers on edge of a Si substrate for second and third generation devices. (d) The L-I curve shows the change in threshold current before and after filling the longitudinal gap with an index-matching polymer. The optical power is normalised for better comparison.

Filling the longitudinal air gap between the lasers and the Si receiving waveguides with fibre glue helped to improve coupling with only a few mA increases in the threshold current. This is due to the reduced reflection from the front facet as the light sees a material index of 1.5 instead of air (refractive index of 1). Figure 6.3(d) shows the LI plot before and after applying the infill and its effect on the threshold current.

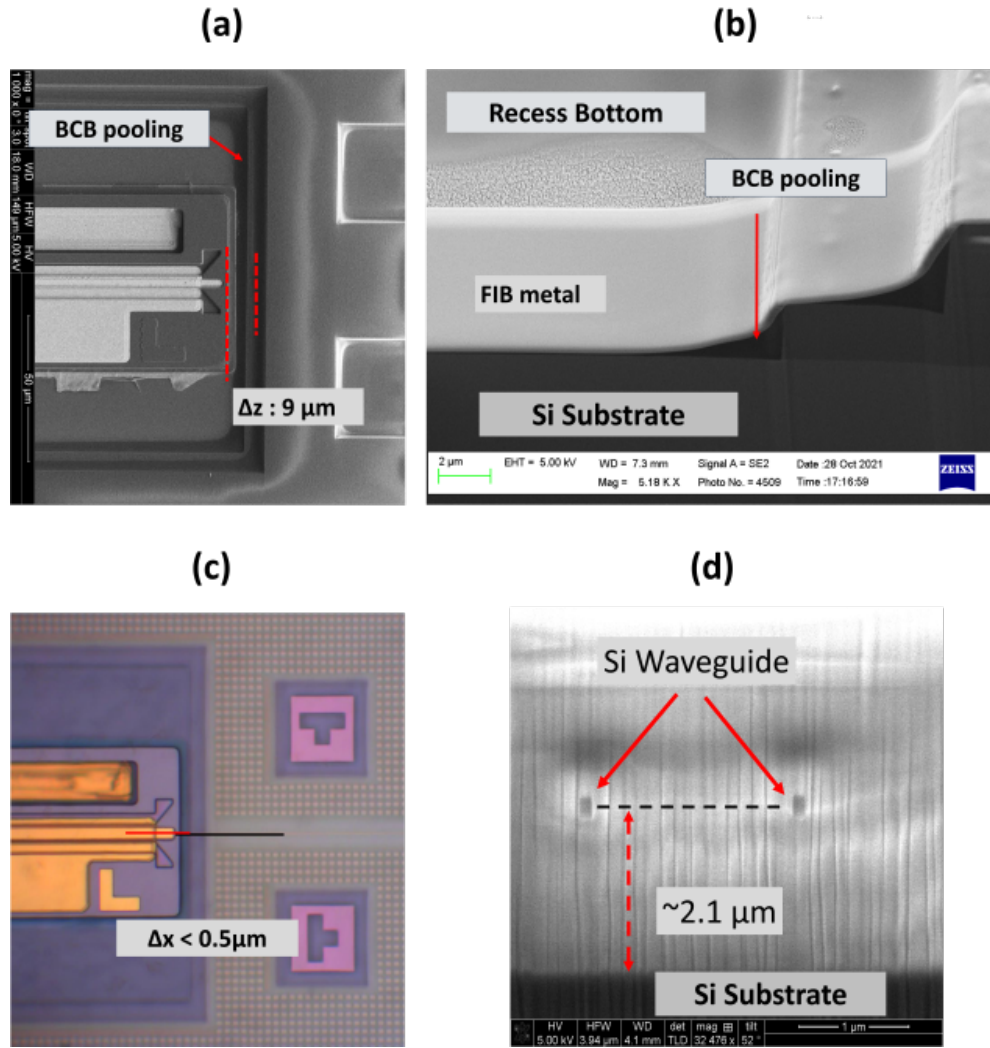


Figure 6.4: (a) SEM image of a coupon inside deep trench shows $9 \mu\text{m}$ longitudinal spacing between laser and SOI facet due to BCB pooling at recess edge. (b) The FIB cross section perpendicular to the receiving SOI facet shows the ramp of adhesive material towards the sidewall. (c) Detail of the lasing facet shows a lateral misalignment of $\Delta x < 0.5 \mu\text{m}$. (d) FIB cross section image near the Si waveguide tip shows the Si waveguide is 150 nm wide and 220 nm thick

Given the amount of power that the laser produces (see the reference laser in Fig. 6.3(c), where I_{th} is 16 mA , and P_{out} is 16 mW @ 80 mA bias current), the amount of power coupled into the Si waveguide suffers from high loss due to misalignment. Figure 6.4 illustrates the measured misalignment in the lateral (X), vertical (Y), and longitudinal (Z) directions for the laser printed onto a trench with single tip inverse tapered waveguide. Although an alignment accuracy of $< 0.5 \mu\text{m}$ is achievable with MTP, there is a several micron misalignment in the longitudinal direction in this case, corresponding to the large gap between the two facets of the light source and the SOI. As the divergence of the optical beam is relatively large, especially in the vertical direction, the coupling from the transfer-printed laser to the Si waveguide is very sensitive to the in-plane alignment accuracy and the longitudinal distance between

the two facets. Inspection reveals that such a large gap is due to the accumulation of adhesive material toward the cavity sidewall during adhesive spray-coating. This pooling limits the closer integration of the lasers without degrading the vertical alignment. The longitudinal misalignment in the transferred coupons is measured $\sim 9 \mu\text{m}$ including the $2 \mu\text{m}$ SiO₂ block between the Si taper and the SOI facet, as seen in the SEM image in Fig. 6.4(a). The simulated coupling efficiency drops from 65% (assuming 0 misalignment in the three directions) to 23% with $9 \mu\text{m}$ misalignment in the longitudinal direction. Figure 6.4(b) illustrates a focused ion beam (FIB) cross section cut that is carried out at different locations to assess the pooling across the recess. The BCB ramp varies in length and typically $>4 \mu\text{m}$. The variation in BCB thickness can be related to spray coating parameters (i.e. sample orientation during coating) and different surface properties and conditions (wetting condition prior to coating). In this situation, the printing of the laser closer would result in the laser's facet to be tilted upward, deteriorating the coupling.

The lateral misalignment of the laser facet to the Si waveguide is measured to be $<0.5 \mu\text{m}$ as given in Fig. 6.4(c) using image-recognition during MTP that utilizes the alignment markers on both SOI target and laser. The corresponding loss due to the misalignment in this direction is estimated as 7%. Vertical alignment is achieved by tailoring the mode center in both the QD laser and the SOI waveguide. The etch depth of the recess on the SOI wafer and the adhesive interlayer thickness can also be used to adjust their heights. Figure 6.4(d) indicates a vertical misalignment of $< 200 \text{ nm}$ caused by the variation in the recess etch depth and adhesive thickness. The loss due to misalignment in this direction is estimated as $<4\%$. The coupling efficiency after including all losses due to positioning misalignment in all three directions is simulated as $\sim 11\%$ for the best device on this platform. The measured coupling efficiency ($\sim 6\%$) is almost half of the simulated value. The difference between simulated and measured coupling efficiencies can be attributed to the other potential loss mechanisms such as angled SOI facet, variations in performance and misalignment of the laser diodes, and grating coupler to fiber coupling loss.

The analysis shows that the larger longitudinal mismatch is the main reason for the low coupling efficiency. The simulation results in section 3.2.1 predict more than a 3-fold increase in the coupling efficiency by reducing the longitudinal gap. It can be further increased by improving the alignment in the vertical and lateral directions. The gap between the laser and the SOI facet can be reduced by eliminating the accumulated adhesive toward the recess sidewall and front-ledge on the laser coupon. To address this issue, a patternable adhesive process was developed to minimise the longitudinal gap and is discussed in detail in chapter-4 (section 4.2.2.2). In addition, the third generation laser coupons are designed without a ledge on the emitting front facet (see section 2.3.2 for more details). The results are discussed in the following section.

6.1.1 Ledge-less QD Lasers on 220 nm SOI Waveguide

The ledge-less QD lasers (from the third-generation device) are transfer printed onto SOI targets with patterned InterVia (1-4) as shown in Fig. 6.5(a). A print yield of $>90\%$ is achieved on a 150 nm thick InterVia layer. An image of the recess with an integrated laser shows that all the adhesive is removed from the sidewall of the recess, while a thin bonding layer in the centre remains as shown in 6.5(b). This results in a large improvement in the longitudinal misalignment between the laser and the waveguide. The gap is reduced from several microns to $\sim 1 \mu\text{m}$ as shown in Fig. 6.5(c). In these coupons a lateral misalignment of $0.2 \mu\text{m}$ is achieved. Figure 6.5(d) shows the waveguide coupled power as a function of the drive current from ledge-less coupons. Although power above 2 mW is coupled into the Si waveguide, there is still room for further improvement of the coupling efficiency.

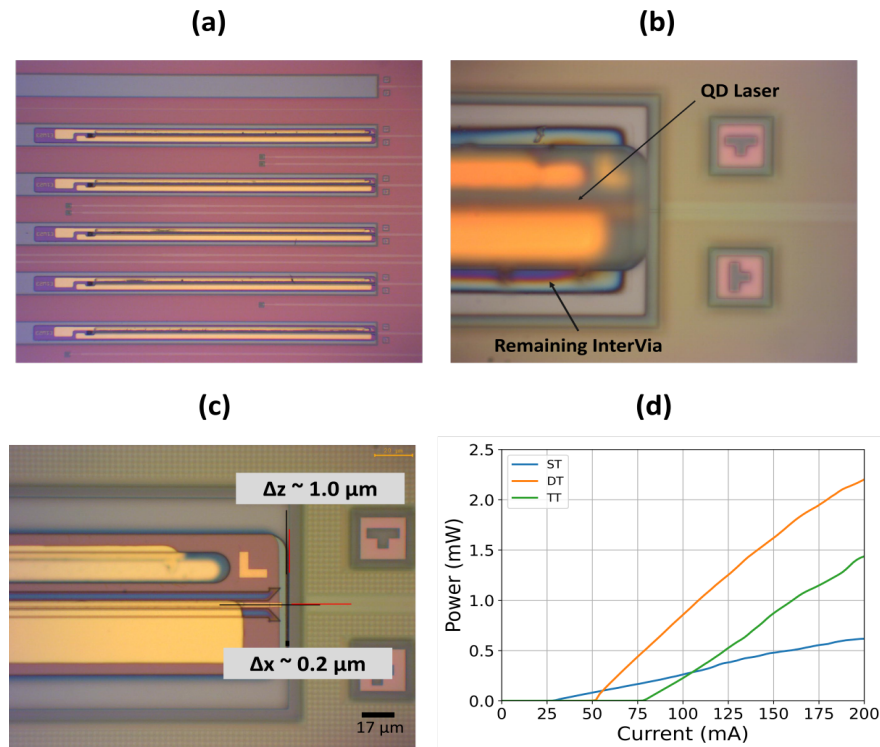


Figure 6.5: (a) Top view optical microscope image of QD lasers printed into the recesses on the SOI wafer. (b) A magnified image of a coupon printed on remaining InterVia layer after patterning process. (c) The achieved misalignment in lateral and longitudinal direction are $\sim 0.2 \mu\text{m}$ and $\sim 1 \mu\text{m}$, respectively. (d) Optical power coupled to Si waveguides as a function of drive current up to 200 mA for different Si waveguide couplers.

Further investigation shows that the lasers integrated in this SOI chip have an over-etch problem on the front facet, which creates a notch on the p-cladding layer and results in an increased threshold current with poor output power performance. This issue is addressed in the second batch of lasers and discussed in the development of ledge-less coupons. In addition, some coupons experienced drift during characterisation due to reduced adhesion of the InterVia (1:4) bonding layer after

patterning. This problem makes it difficult to accurately characterise the integrated lasers on these targets. The limited minimum resulting InterVia thickness after patterning was another challenge that could hinder vertical alignment. These issues are addressed using an InterVia (1:20) adhesive layer and are discussed in the following section.

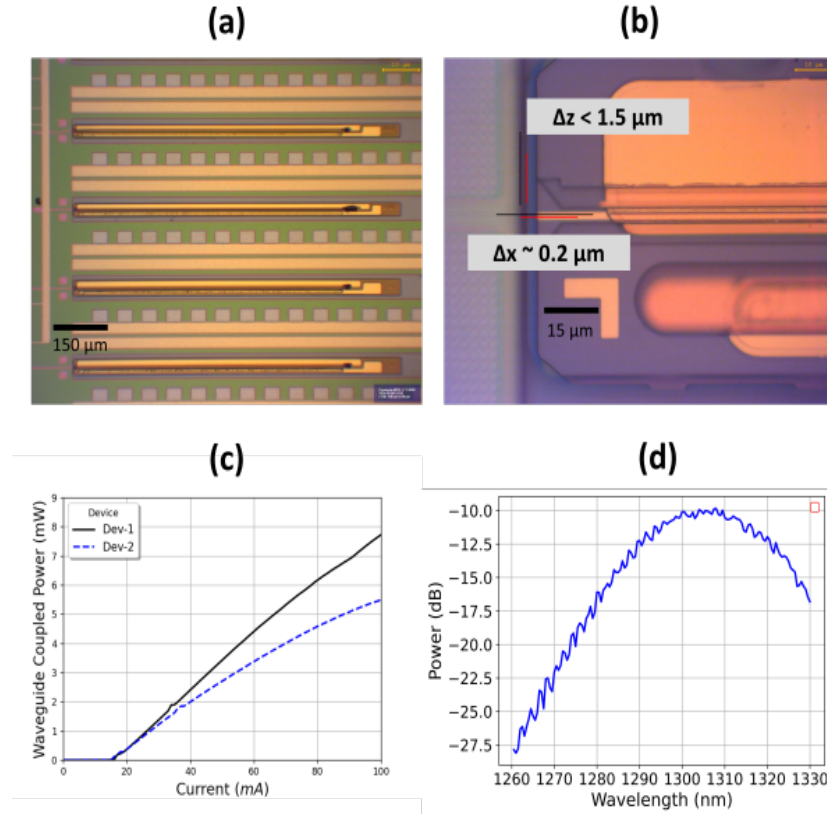


Figure 6.6: (a) Transfer-printed lasers from final generations onto recess after spin-coating of 60 nm InterVia layer diluted with PGMEA at 1 to 20 rate. (b) Lateral and longitudinal misalignment in the laser coupon inside the recess with 60 nm InterVia. (c) The optical power in the silicon waveguide after the coupling as a function of drive current. (d) Transmission spectrum of the surface grating coupler on a reference waveguide. The transmission loss per grating coupler is measured to be around -7.5 dB at 1285 nm.

The second batch of final generation lasers with notch-free facets is transfer printed onto SOI samples after spin coating with a highly diluted InterVia solution (1:20). This process does not cause a pooling effect, resulting in an adhesion layer approximately 60 nm thick that does not require patterning. This avoids the weakening of adhesion that typically causes coupons to drift during printing and characterisation. This method achieves a very high transfer print yield of over 90% with these laser coupons. Figure 6.6(a) shows an image of laser coupons printed inside the trenches. Since there is no adhesive build-up in the trench and at the edge of the emitting facet of the lasers, the gap between the two facets is less than 1.5 μm, as shown in Fig. 6.6(b). The resulting longitudinal misalignment is $\sim 3 \mu\text{m}$ including the SiO₂ block from the Si waveguide tip to the SOI facet. The lateral misalignment is

measured as $\sim 0.2 \mu\text{m}$. The improvement in the alignment and the device performance results in greater than a 6 times increase in the waveguide coupled power. Fig. 6.6(c) shows the optical power in the Si waveguide as a function of the bias current with a waveguide power greater than 7.5 mW at 100 mA drive current. The waveguide coupled power is calibrated using the transmission loss ($\sim 7.5 \text{ dB}$ per grating at the emission wavelength (1285 nm)). Figure 6.6(d) shows the transmission plot of a reference waveguide with two grating couplers at each end between 1260 nm and 1330 nm . The reference laser transferred on Si substrate is given for the third-generation device in Fig. 6.3(c). The measured coupling efficiency for the best device is 23% while the simulated efficiency is 37% considering the actual misalignment. There is 14% difference between the simulated and measured efficiency that can be due to variation between the reference and actual laser performance, the 83°C slope on the SOI facet which is not considered in simulation.

Transfer printing of QD lasers on SOI targets with deep trenches is discussed using different bonding layers including $100\text{--}200 \text{ nm}$ BCB, 150 nm patterned InterVia (1-4) and unpatterned 60 nm InterVia (1-20). Overall, a very high print yield of $> 90\%$ is achieved on all types of bonding layer. The resulting misalignment in the lateral, vertical, and longitudinal directions is presented with the corresponding loss. Lateral misalignment of $< 0.5 \mu\text{m}$ is achieved for all bonding layers with vertical alignment of $< 0.2 \mu\text{m}$. Longitudinal misalignment is reduced from $9 \mu\text{m}$ to $< 3 \mu\text{m}$ by the use of ledge-less coupons and removal of accumulated adhesive material from the recess sidewall with patternable adhesive and high dilution InterVia bonding. The measured coupling efficiency increases from 6% to 23% on this platform after optimising the coupons and the target.

6.2 3 μm SOI Waveguide

The second platform is a $3 \mu\text{m}$ thick SOI with a $1 \mu\text{m}$ BOX layer. Fabrication details on the target SOI wafer are discussed in the previous section 3.2.2. After waveguide definition, a 70 nm BCB solution diluted 1:5 with mesitylene is spin-coated on the SOI wafer. A total of 12 laser coupons of different lengths are then transfer-printed next to the Si waveguide facets with a print yield of 100%. Alignment of the transferred devices to the waveguides is done by visual inspection, as there was no transfer-print alignment mark defined on the target wafer to simplify fabrication. An image of the transferred coupons on this platform is shown in Fig. 6.7(a). A magnified optical and SEM image of an emitting facet of the coupon and the receiving Si waveguide are shown in Fig. 6.7(b) and (c) respectively.

After filling the gap between the facets of the laser and the Si waveguide with an optical adhesive, the light coupling characterisation is performed in CW mode at room temperature. The waveguide-coupled power is collected from the cleaved end of the

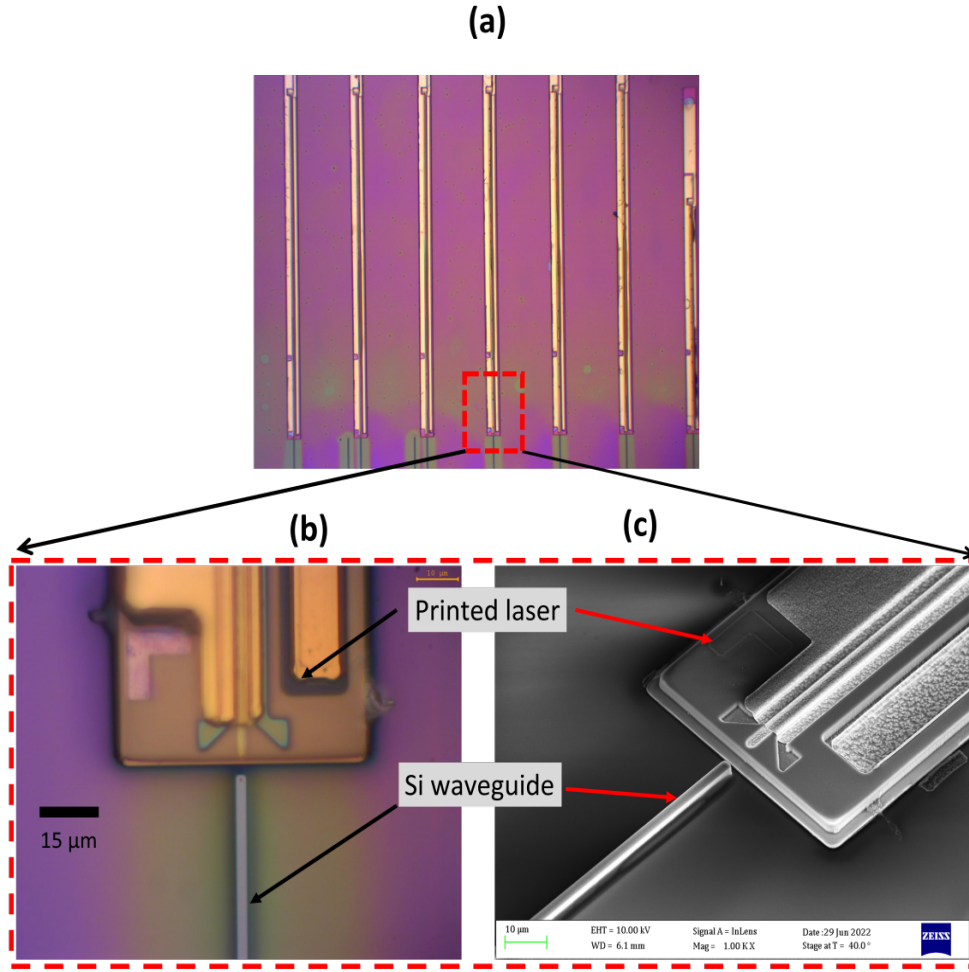


Figure 6.7: (a) Optical microscope image of the lasers printed next to 3 μm SOI waveguides with 100% yield. (b) Optical and (c) SEM image of the emitting facet of the lasers next to Si waveguide after transfer printing.

Si waveguide facet with a collimator lens and a free space detector directly in front of the chip, as schematically shown in Fig. 6.8. It is worth mentioning here that there is no anti-reflection (AR) coating on the cleaved Si waveguide facet where the light is collected.

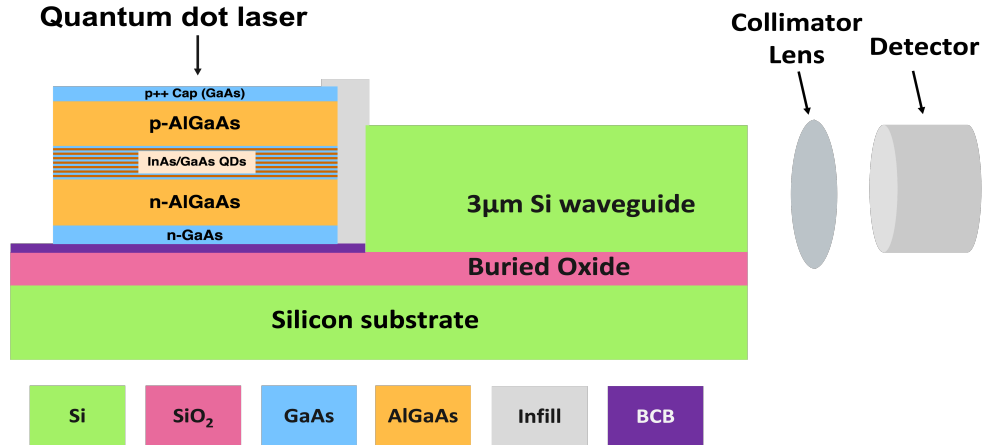


Figure 6.8: Schematic of coupling from a transfer-printed laser next to 3 micron Si waveguide. Waveguide coupled light is collected from the cleaved end of several mm long Si waveguide by a broad area detector using a collimating lens.

The LI curves show that the best laser has an I_{th} of 21 mA with an waveguide coupled power of above 2 mW as shown in Fig. 6.9(a). The ripples in the LI curve are due to strong back reflection from the Si waveguide facet. Due to the lack of an AR coating on the facet where the light is collected, a cavity is formed in the waveguide, leading to fluctuations in the measured powers. The spectra of dev-1 (in Fig. 6.9(a)) is presented in Fig. 6.9(b) at a bias current of 50 mA . The spectra is centred mainly around 1286 nm , with another band at 1281 nm .

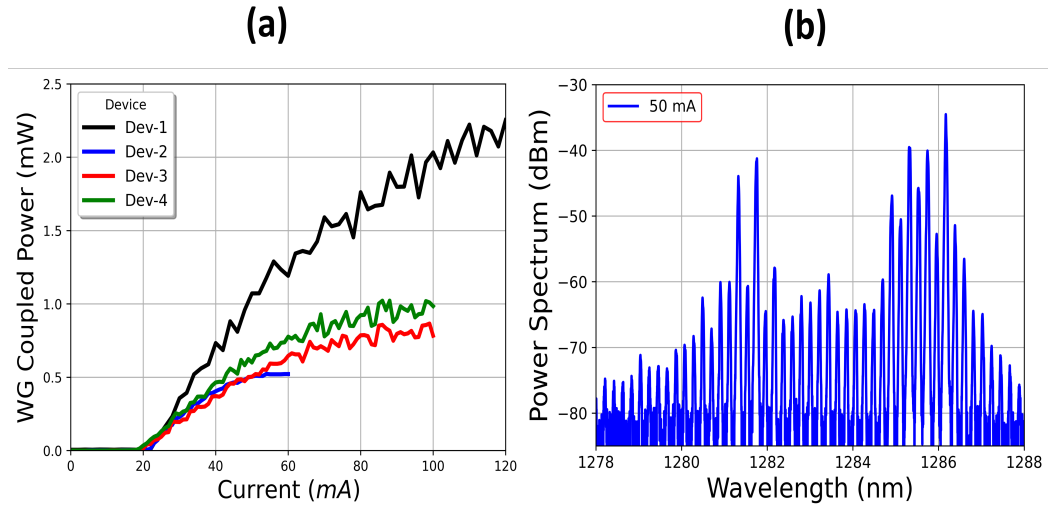


Figure 6.9: (a) Waveguide coupled power as a function of injection current plots for lasers on 3 μm SOI. (b) Optical spectrum of Dev-1 at 50 mA drive current shows emission around 1286 nm .

Similarly to the 220 nm SOI platform, the waveguide coupled power in this platform suffers misalignment in the longitudinal direction. The longitudinal misalignment is measured to be 4 μm as shown in Fig. 6.10(a). Since there is no adhesive material pooling problem on this platform, the 2.5 μm wide front edge of the laser coupon is

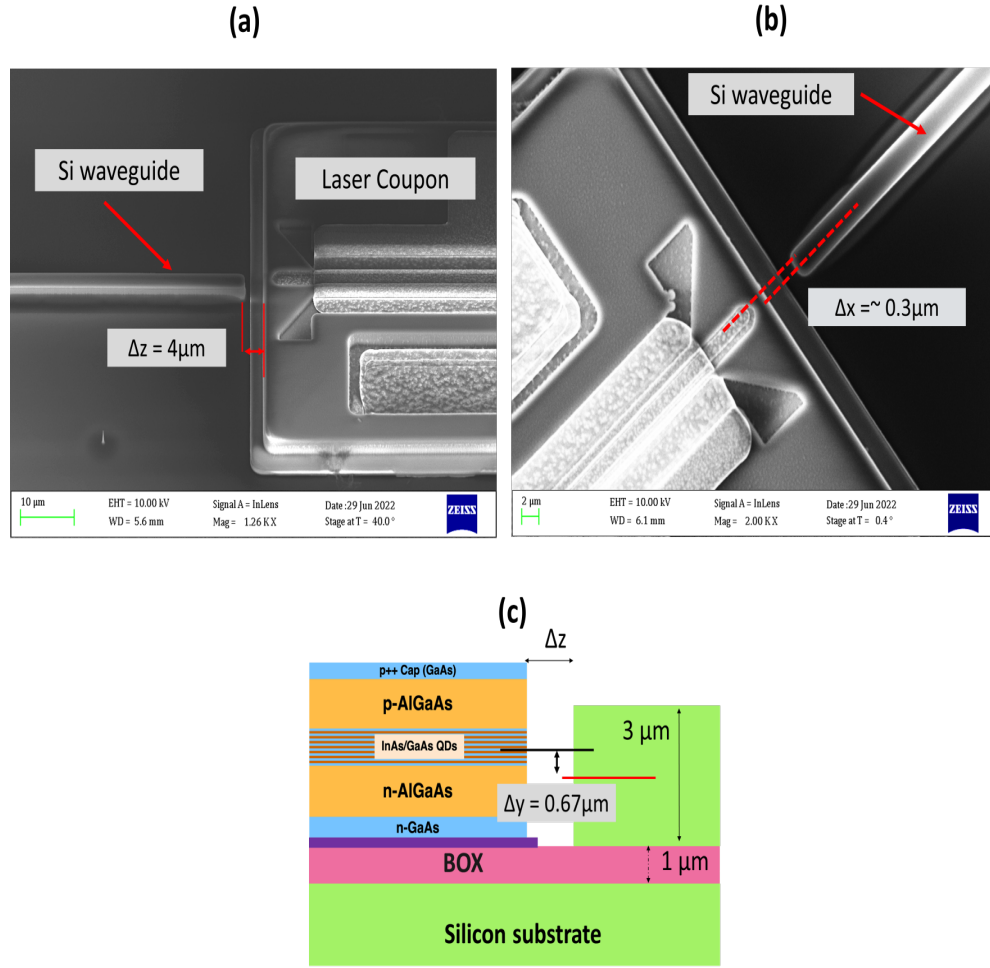


Figure 6.10: (a) SEM image of a coupon inside deep trench shows 9 μm longitudinal spacing between laser and SOI facet due to BCB pooling at recess edge. (b) Detail of the lasing facet shows a lateral misalignment of $\Delta x < 0.5 \mu\text{m}$. (d) FIB cross section image near the Si waveguide tip shows the Si waveguide is 150 nm wide and 220 nm thick.

the main reason for such a large misalignment. A lateral misalignment of $\sim 0.3 \mu\text{m}$ is measured in several transferred devices, as given in Fig. 6.10(b). This value is similar to the misalignment achieved on the 220 nm SOI substrate and within the specification. However, misalignment in the vertical direction in the platform is a major problem and causes an additional $\sim 25\%$ loss. The mismatch in this direction is calculated to be $0.67 \mu\text{m}$ due to the difference between the mode center in the laser ($2.1 \mu\text{m} + 0.07 \mu\text{m}$ BCB) and the Si waveguide ($1.5 \mu\text{m}$) as schematically shown in Fig. 6.10(c). The measured coupling efficiency for these devices is calculated to be 12% (-9.2 dB) by dividing the waveguide coupled power by the power measured from the reference laser (Gen-2) printed on Si at the same injection current of 80 mA (shown in Fig. 6.3(c)). The simulated coupling efficiency after taking into account the actual misalignment is calculated to be 15%.

Lateral alignment can be further improved by using image-assisted printing. This requires the definition of transfer print alignment marks on the target wafer. The

longitudinal misalignment in this platform is mainly due to the $2.5\ \mu\text{m}$ wide front-ledge on the laser coupons. This can be reduced by a structural change to the coupon removal of the front ledge, as implemented in the latest generation of lasers. However, these devices have not been integrated in these platform. The vertical alignment between the laser and waveguide can be further improved by adjusting the etch depth in the BOX layer and the adhesive thickness without changing the laser epitaxial structure as explained in section 3.2.2. It should be noted that etching into the BOX layer or the Si substrate can result in a material pooling toward the waveguide facet, similar to the $220\ \text{nm}$ SOI platforms.

6.3 300 nm SiN & SU-8 Polymer WG

The final platform where the QD lasers are transfer printed is the $300\ \text{nm}$ SiN waveguide with the SU-8 polymer spot size converter (SSC) as the intermediate waveguide. In contrast to the first two edge-couplers, this design employs a SU-8 polymer spot size converter (SSC) [126] where the light is first edge-coupled from the laser into the SU-8 waveguide and then evanescently coupled from the SU-8 waveguide to the underlying SiN waveguide by tapering down and up both SU-8 and SiN waveguides, respectively. The final SiN waveguide is $1\ \mu\text{m}$ wide.

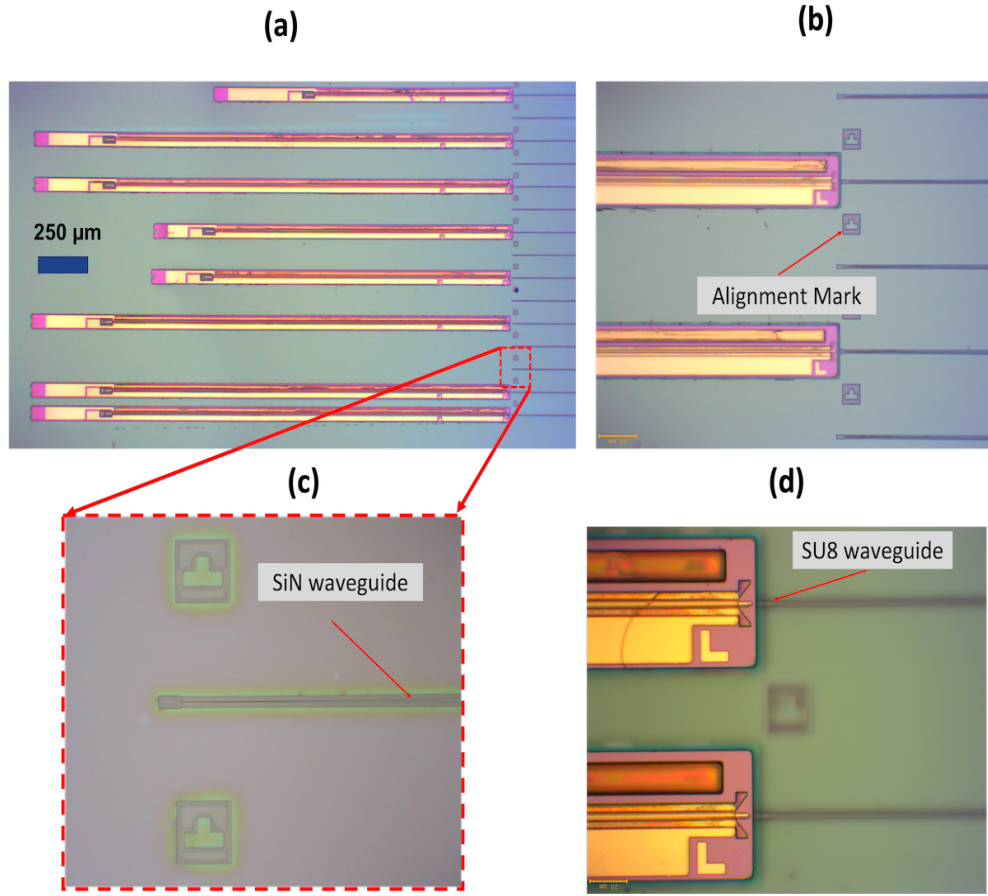


Figure 6.11: (a) QD laser coupons up to 2.4 mm are transfer-printed on 70 nm BCB. (b) The SiN waveguide that starts from 10 μm away from the laser facet and tapered up to 1 μm. (c) SiN waveguide and transfer-print alignment markers before laser integration and (d) SEM image of a laser after SU-8 polymer waveguide definition.

After the definition of the SiN waveguide, 70 nm BCB is spin coated on the sample for better integration yield. QD laser coupons with various lengths (1.5 mm, 1.8 mm and 2.4 mm) are transfer-printed next to SiN waveguide as shown in Fig. 6.11(a) and (b). The 300 nm thick SiN waveguide and alignment markers are defined at the same level as shown in Fig. 6.11(c). After removal of the photo resist tether in O₂ plasma and BCB curing, the SU-8 polymer waveguide is defined starting from the emitting facet of the laser and continuing over the underlying SiN waveguide by tapering for evanescent coupling of the light to the SiN waveguide. Figure 6.11(d) shows the lasers after the SU-8 waveguide definition.

Figure 6.12 illustrates the edge-coupling schematic from the laser to the SU-8 waveguide and evanescent coupling from the SU-8 waveguide to the underlying SiN waveguide. The output light is collected by a free space broad area detector with a collimating lens. The 300 nm thick SiN waveguide is inverse-tapered from 500 nm to 1 μm over a 200 μm distance, while the SU-8 polymer waveguide is tapered from 3 μm to 500 nm over the same distance to enable evanescent coupling. The chip is

cleaved 4 mm away from the laser and measured at room temperature without any temperature control under CW operation.

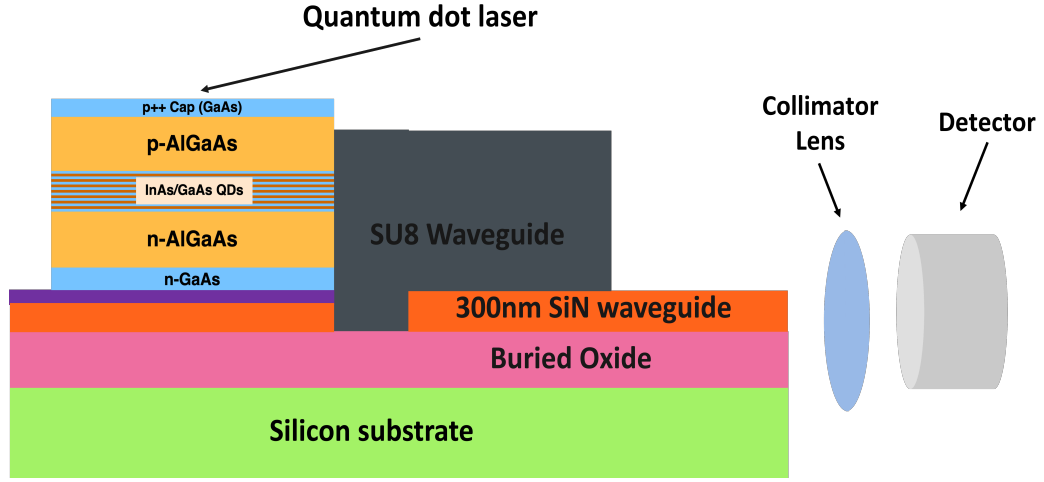


Figure 6.12: Light coupling schematic from laser to SU-8 polymer waveguide and SiN waveguide. Light from the cleaved end of 4 mm long SiN waveguide is collected by a broad area detector using a collimating lens.

The recorded LI curves show that the lasers have a threshold current ranging 25 to 30 mA and up to 1.2 mW waveguide coupled power at 120 mA at room temperature, as shown in Fig. 6.13(a). There is no AR coating on the SiN facet where light is collected by a detector. The interface of the laser with the SU-8 waveguide (with effective index of ~ 1.6) results in a similar threshold current increase as observed in other waveguide platforms after filling the gap between two facets with fiber-glue. Due to a lower refractive index of SiN ($n \sim 2$) than that of Si ($n \sim 3.5$), the ripple in the SiN waveguide is less pronounced compared to the 3 μm SOI platform, owing to the reduced back reflection from the cleaved facet. The spectrum of laser shows multi-mode emission around 1286 nm at 50 mA drive current and is given in Fig. 6.13(b).

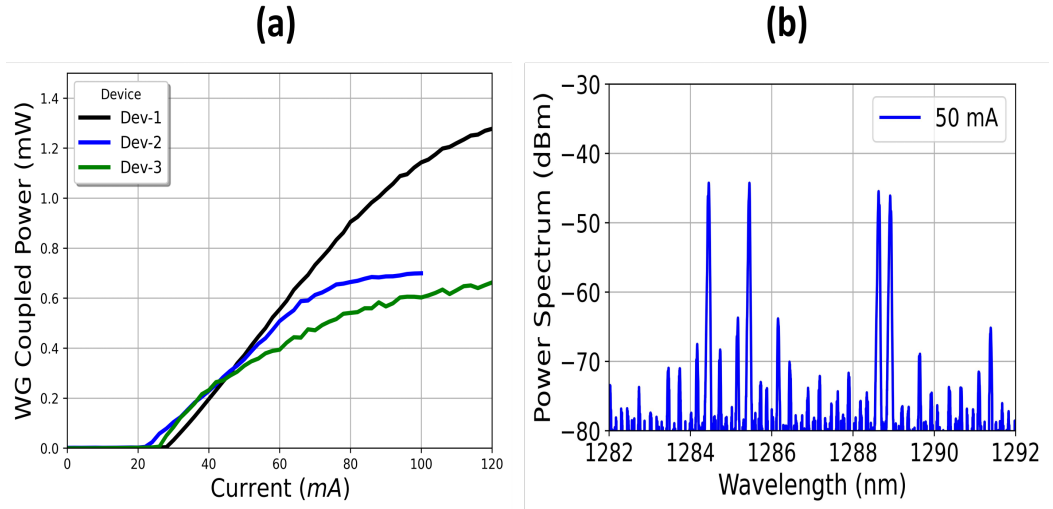


Figure 6.13: (a) Measured L-I characteristics from 1.5 mm long laser coupons integrated with the SU-8 & SiN waveguides. Signal is first edge-coupled into 3 μm wide and 2.2 μm thick SU-8 waveguide, and then evanescently coupled to the underlying SiN waveguide. (b) The spectrum of Dev-1 under injection current of 50 mA at 20°C.

The laser emission at 50 mA is captured using an IR camera shown in Fig. 6.14. The bright spot at the bottom indicates the light leaving the waveguide from the cleaved end of the 4 mm long SiN waveguide. The bottom-right inset shows the SiN waveguide facets after cleaving. The light spot at the top is the light that escapes from the rear mirror due to reduced reflection. This also implies that the HR mirror in second generation lasers needs to be improved. The spots expanding along the SiN waveguide is the light scattering at the laser - SU-8 polymer waveguide interface and along the SU-8 waveguide. The top-right inset shows an SEM image of the laser - SU-8 waveguide interface.

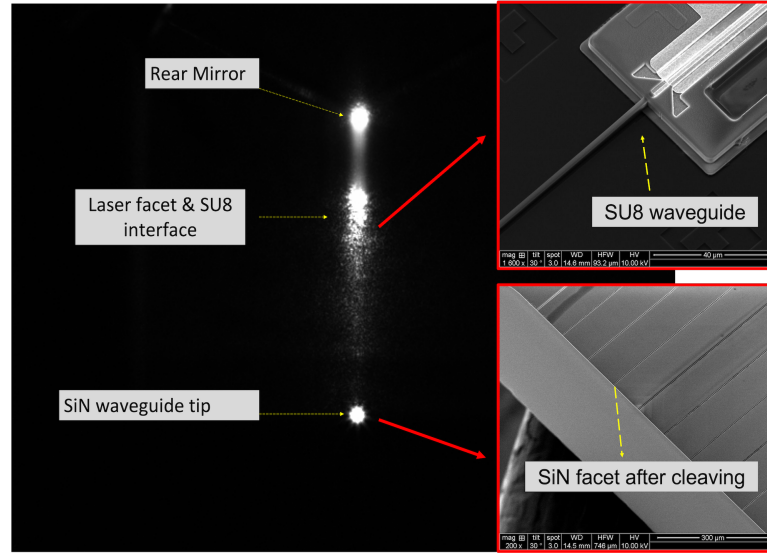


Figure 6.14: Infra-red camera plan view image of the laser and SiN when the laser is biased at 50 *mA*. The three other bright spots are seen in the image corresponding to the rear facet, the laser – SU-8 interface (Top Inset) and Si waveguide cleaved facet (Bottom Inset).

There are two lateral misalignments that need to be taken into account in this platform. The first is the misalignment of the laser ridge with respect to the SiN waveguide and is measured to be Δx of 0.3 μm as given in Fig. 6.15(a). The second lateral misalignment is the misalignment of the laser waveguide with respect to the SU-8 polymer waveguide. This is measured as $\Delta x \sim 0.5 \mu m$ and shown in Fig. 6.15(b). The thickness of the SU-8 waveguide defines the vertical misalignment. Here, the mismatch in the vertical direction is $\sim 1.07 \mu m$ given the difference between the mode center in the laser (2.1 μm + 0.07 μm BCB) and the Si waveguide (1.1 μm). Moreover, there is no longitudinal spacing between the emitting facet and SiN waveguide as the SU-8 polymer waveguide starts from the laser facet. The measured coupling efficiency in the best device on this platform is estimated to be 7% (-11.5 *dB*) by dividing the power in the waveguide by the emitted power in the reference laser at 80 *mA* drive current. The simulated coupling efficiency for the best device, including the misalignment achieved in transfer printing, is 12%.

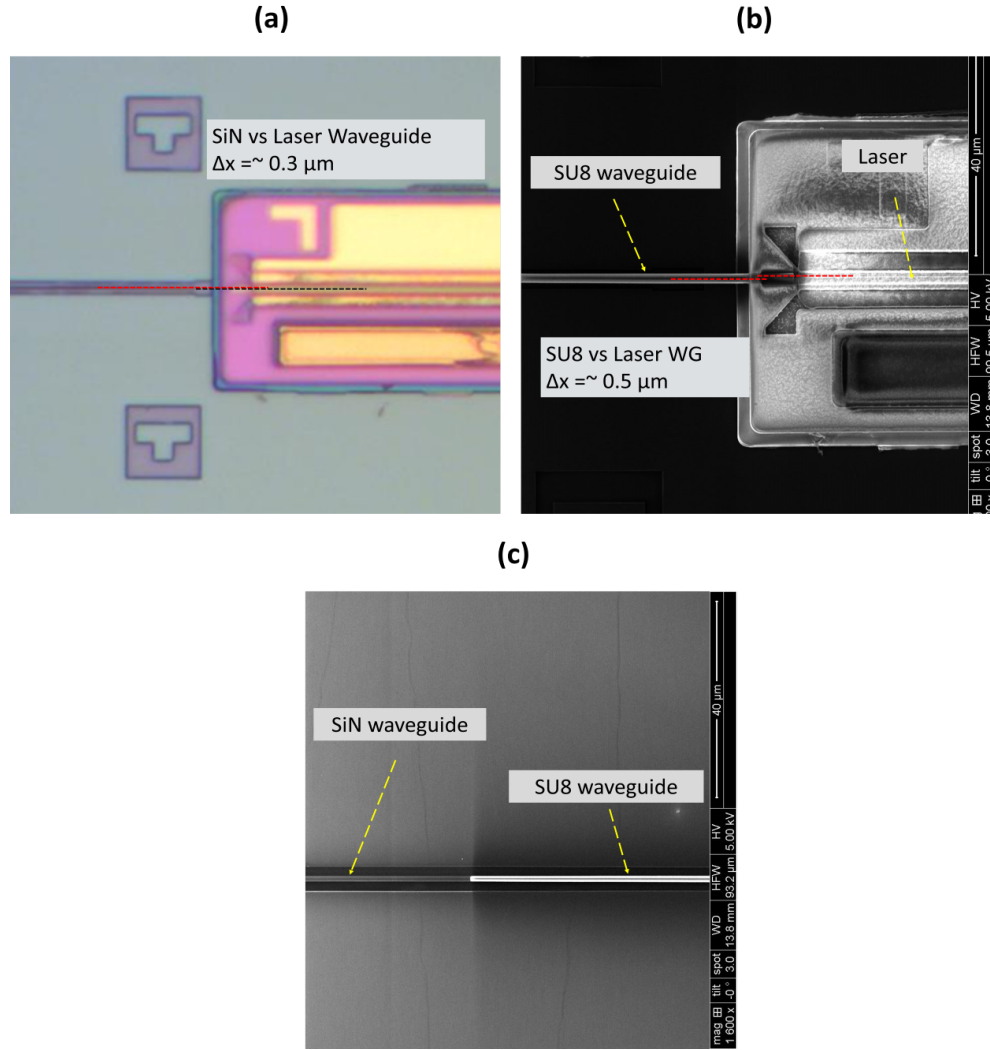


Figure 6.15: (a) Top view on a laser transfer-printed next to a Si waveguide. The lateral misalignment between the Si waveguide with respect to laser waveguide is 300 nm. (b) SEM image of SU8 SSC defined on top of Si waveguide. The lateral misalignment between the SU-8 waveguide and laser waveguide is 500 nm. There is no gap between the laser facet and receiving SU-8 polymer waveguide. (c) SEM image of 1 μm wide SiN waveguide and SU-8 waveguide termination tip.

The lateral alignments can be improved by using image-assisted printing. However, the coupling between the laser and the SU-8 waveguide determines the overall coupling efficiency as the evanescent coupling from the SU-8 to the underlying SiN waveguide is above 90% at the achieved misalignment. Thus, optimizing the vertical alignment between the laser and the SU-8 waveguide can be prioritised. The mismatch in this direction can be improved by controlling the etch depth into the BOX layer and adhesive thickness. In addition, engineering the dimensions of the SU-8 polymer waveguide with optimal thickness would result in higher coupling. This also reduces the scattering along the SU-8 waveguide.

6.4 Conclusion

This chapter has presented the performance of QD laser integrated edge couplers based on 220 nm SOI, 3 μm SOI and 300 nm SiN & SU-8 platforms. The platforms are evaluated based on their coupling performance and the misalignment. The measured coupling efficiencies are estimated using the measured waveguide coupled power and the power delivered by the reference laser at the same bias current (80 mA). In addition, the alignment accuracy between the laser and the receiving waveguide achieved during integration is discussed along with proposed solutions for improvement. The simulated coupling efficiencies are calculated including the achieved misalignment and compared with the measured efficiencies. Table-6.1 shows the simulated and measured coupling efficiencies and the simulated loss taking into account the actual misalignment in the integrated devices.

Key metrics	Waveguide Platforms			
	220nm Si	220nm Si ¹	3 μm Si	SiN&SU8
Simulated CE (%) ²	65	65	50	50
P_{out} at ref. laser @80mA (mW)	16.5	27	15	13
Power in WG @80mA (mW)	1	6.25	1.75	0.9
Loss due to misalignment in X (%)	7	7	5	11
Loss due to misalignment in Y (%)	4	4	12	16
Loss due to misalignment in Z (%)	43	13	18	-
Simulated CE (%) ³	11	37	15	12
Measured CE (%)	6	23	12	7

¹ Experiment with ledge-less QD laser

² Without any misalignment in X-Y-Z irections

³ Actual misalignment is taken into account

Table 6.1: Simulated and measured coupling efficiencies for each platform investigated in this thesis.

The simulated coupling efficiencies, taking into account losses due to misalignment, are 11%, 34%, 15% and 12% for the 220 nm SOI, 220 nm SOI (with ledge-less laser), 3 μm SOI and 300 nm SiN platforms, respectively. However, the corresponding measured coupling efficiencies are 6%, 23%, 12% and 7%, respectively. The significant discrepancies between the simulated and measured efficiencies suggest the presence of additional loss mechanisms that are not fully captured in the simulations. These possible loss mechanisms include;

- Variations in laser power: Variations in the laser power used during measurements can introduce inconsistencies not accounted for in the simulations.
- Waveguide losses: Inherent losses within the waveguides, such as scattering and

absorption, can reduce the coupling efficiency and can vary between fabricated devices and ideal simulations.

- Substrate Coupling: Losses resulting from coupling to the substrate, which may involve unwanted interactions between the waveguide modes and the substrate material, can reduce the measured efficiency. This can be an important factor in the SiN waveguide as it has a $1\ \mu\text{m}$ thick BOX layer.
- Higher-order mode coupling losses: Coupling to higher-order modes, which are less efficient and more lossy, can further reduce the measured coupling efficiencies compared to the simulations. Vertical misalignment in the $3\ \mu\text{m}$ SOI and SiN waveguide can excite these modes.

These factors contribute to the observed differences, indicating that a more comprehensive analysis is required that includes these additional loss mechanisms to accurately predict coupling efficiencies.

Finally, the QD lasers are integrated at $220\ \text{nm}$ without any ridge on their emitting facets after removing the excess material accumulated at the edge of the cavity. These two developments allowed the longitudinal misalignment to be reduced from $9\ \mu\text{m}$ to below $3\ \mu\text{m}$. The power coupled to the waveguide increased from $1\ \text{mW}$ to $6\ \text{mW}$ at a drive current of $80\ \text{mA}$. Recently, a coupling efficiency of 77% ($-1.1\ \text{dB}$) was reported using an InP laser at $1550\ \text{nm}$ integrated on SiN waveguide by the flip-chip technique [37]. This suggests that the coupling efficiency can be further improved with improved alignment and air gap filling with index-matching epoxy.

Chapter 7

Conclusion and Outlook

7.1 Conclusion

Photonic integration is becoming increasingly important in the communications industry in order to meet ever-increasing capacity demands. The dense integration of multiple optical components on a single chip not only reduces the size of photonic systems, such as optical transceivers, but also significantly reduces power consumption and cost. However, despite significant advances over the past two decades, the lack of a low-cost integrated light source capable of operating at high ambient temperatures with low-loss coupling to the SOI/SiNOI waveguide continues to hinder the widespread adoption of this technology. This work demonstrates high performance InAs/GaAs QD edge-emitting lasers and their integration onto a number of waveguiding platforms with different edge-coupling configurations based on 220 nm SOI, 3 μm SOI and 300 nm SiN with SU-8 polymer spot size converter (SSC) by micro transfer printing.

High performance transfer-printable QD lasers are developed using a quarter of a 3" GaAs wafer through several iterations of the fabrication process. First generation lasers, which are non-transfer printable, used to explore the baseline laser material and determine the optimum device dimensions. Characterisation of these lasers revealed that the cavity length of the lasers must be longer than 1 mm to avoid ES emission and early roll-over at higher injection currents due to the low modal gain in the QD layer. The cavity length also must be shorter than 2.5 mm for optimal device performance.

The QD epitaxial layer stack is re-designed to allow release etching and integration of the laser device by transfer printing. Additionally, the number of InAs/GaAs QD layers increased to 14 (was 12) for higher modal gain. Next, the second generation lasers are fabricated following an extensive optimization on ICP dry etch for facet formation. The resulting transfer-printable QD lasers delivered 24 mW of output power with a

threshold current of 16 *mA* at room temperature. Comparison of the printed device with non-transferred reference lasers on the GaAs substrate shows that there is no degradation in device performance due to transfer printing. Performance improvement is observed for the transferred lasers on Si at elevated temperature compared to the reference laser on GaAs due to higher thermal conductivity of the Si substrate. The etched facet lasers had a Ti-Au based metal HR and MIR mirrors in their rear facets. Both types of mirrors showed similar performance with 46% reflectivity. The high series resistance (14 Ω) and poor HR reflectivity were the main issues in these devices.

Further optimisations are implemented in various fabrication processes to achieve better performing devices with smooth facet etch, high reflectivity HR mirror, and low device resistance. Metal HR reflectivity is increased by replacing TiAu based HR metal with sputtered Al. Increasing the n-GaAs contact layer thickness and precise etch depth control in the n-GaAs opening etch allowed the resistance of the device to be reduced. After optimisation, the series resistance in third-generation transfer-printed lasers is reduced from 14 Ω to 8 Ω , while the reflectivity of the rear mirror is increased from 46% to 89%. The output power of a transfer-printed laser on Si with a 1.5 *mm* long cavity is increased from 24 *mW* to 42 *mW* at a drive current of 120 *mA*. A significant improvement in device performance is achieved with an output power of 32 *mW* at 70°C stage temperature.

An HCl-based release etch process is developed for AlGaAs sacrificial layers with 90 to 95% Al content. A release etch at 19°C in dilute HCl with DI in a one to one ratio allowed full undercutting of the 65 μm and 80 μm wide coupons without coupon collapse and without attacking other layers including the epi stack and photo-resist tether. The lateral etch rate is measured above 1 $\mu\text{m}/\text{min}$. In addition, by tailoring the dielectric thickness on the coupons for balanced stress and optimal tether system design, the coupon collapse and formation of pillars at the bottom of the coupons, which could degrade integration, were minimised. The high Al content in AlGaAs release layers causes oxidation on the release layer surface when exposed to ambient air and reacts with gases (i.e. fluorine) to form AlF₃ crystals during ICP dry etching. An ammonia based de-oxidation dip is developed prior to etching the sample. The AlF₃ crystals are removed in a THMA-based developer.

The edge coupling of the QD laser to different waveguides based on 220 *nm* SOI, 3 μm SOI and 300 *nm* SiN was achieved by integrating the pre-fabricated devices in recess or next to the waveguide on the SOI. At 80 *mA*, waveguide coupled powers of 6.0 *mW*, 1.75 *mW* and 0.9 *mW* are measured after outcoupling from the 220 *nm* SOI, 3 μm SOI and 300 *nm* SiN waveguides, respectively. Investigations suggest that all couplers suffer from misalignment. The vertical misalignment in the 3 μm SOI and 300 *nm* SiN waveguides is the main reason for the high coupling loss. This can be

addressed by etching further down to the BOX layer to level the mode center for both platforms. The problem in the 220 nm SOI platform is several microns of longitudinal misalignment due to adhesive accumulation toward the sidewall of the deep trenches. A patternable adhesive and a high dilution rate (1xInterVia-20xPGMEA) adhesive process were developed to solve this problem. In addition, the 2.5 μm long ledge on the emitting side of the laser is removed by modifying the standard fabrication flow. These developments allowed the longitudinal distance between the laser facet and the SOI facet to be reduced. This development improved the waveguide-coupled power by a factor of 5. However, it should be noted that there is still room to improve the coupling performance for all three platforms by further improving the alignment.

Integration of the QD laser on different silicon photonics platforms without any changes in the lasers proves that MTP is a versatile solution for enhancing the functionality and applicability of emerging PICs. The QD lasers can be fabricated in a III-V fabrication facility, while the Si PICs can be realised in open-access CMOS foundries, allowing heterogeneous integration of optimised devices using MTP. It also provides sub-micron positional control in the device through machine learning-based automated printing. The stamps can be designed to enable transfer-printing arrays of discrete coupons in a single pick-up and print cycle and increase the throughput by adjusting the pitch on the source and target wafers. The MTP technique also allows for working with different sizes of wafer that suit best for the device of interest. Finally, different devices such as lasers, modulators, and detectors fabricated on their native III-V wafers can be integrated in close proximity on the same target. This makes it a versatile integration strategy for various applications such as data-com, sensing.

7.2 Future Work

This work provides a roadmap for the integration of the QD lasers with different edge-coupling platforms using micro-transfer printing. However, there is still a lot of work to do to improve the performance of the integrated device. Further work is needed to improve the light coupling efficiency, and it would be advisable to work on the following points for future development:

1. **Improvement in alignment:** The main reason for low coupling efficiency is misalignment between the emitting facet of the laser and the SOI waveguide. Among the three directions, the longitudinal and vertical misalignments dominate and cause the most loss in light coupling. Although the accumulated glue and the ledge on the front facet of the laser are removed, the measured coupling efficiency indicates that there is still room for further improvement. Further analysis of misalignment in other directions is required to fully understand the additional loss mechanism.

2. **Improvement in coupon:** Print yield is highly dependent on the stress level of the coupon. The resulting stress can be compensated by the adhesive bonding layer, however there can be other side effects on the process. It is therefore crucial to adjust the process flow so that the accumulated dielectric and metal layers on the coupon result in an almost stress-free coupon.
3. **Transfer-printable DFB Laser:** A proof-of-concept laterally coupled sidewall grating QD DFB laser on GaAs substrate has been completed with learnings. While keeping the process flow largely the same, an improvement of the grating pattern along the laser ridge is required for stable single mode operation as suggested in the Appendix B.1. This will also require the development of an AR coating or tilt for the front facet to minimise the back reflection.
4. **Others:**
 - (a) Post-print metallisation can be applied to p and n metal contacts for DC probing rather than probing directly onto the device. This makes characterisation easier and provides a more accurate resistance measurement. Of course, this requires an additional step in the process.
 - (b) Development of an infill application process to ensure that the gap is completely filled with a material of a suitable refractive index.
 - (c) Thermal characterisation of the transfer printed laser on the SOI waveguide can be useful for evaluation of the thermal properties of each platform.
 - (d) Repeating the experiment for 3 μm SOI and 300 nm SiN using lasers of the latest generation would improve the waveguide coupled power due to the improved device performance and the removal of the front ledge on the coupon.

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Appendix A

QD Lasers Structure used in this Thesis

In this appendix, the epitaxial layer and summary of the main fabrication process for transfer printable InAs/GaAs QD lasers are reported.

A.1 InAs/GaAs Quantum Dots Epitaxial Layer Structure

The epilayers are designed for O-band emission with a target emission around 1300 *nm*. The different epilayers grown by Innolume and listed in Table-A.1, Table-A.2 and Table-A.3 are used for the fabrication of three different generations of lasers. Based on the knowledge gained from the characterisation of the fabricated devices, changes are made to the epilayers. The first generation epi (Epitaxy-A) contains 12 layers of InAs/GaAs QDs and 80% Al concentration in the p- and n- AlGaAs cladding, but does not have a release layer as it is designed to evaluate the material in a shorter fabrication loop. The releasable epilayers (Epitaxy-B and Epitaxy-C) contain a 500 *nm* AlGaAs sacrificial layer between the substrate and device layers. The Al content of these materials is 95% and 93% respectively. The number of QDs in the other materials is also increased from 12 to 14. This is done for higher modal gain, which prevents the emission transition from the ground state (GS) to the excited state (ES) in short cavity (< 1 *mm*) lasers, as discussed in chapter-5. In addition, the Al content in the cladding is reduced from 80% to 40% for the top cladding and 30% for the bottom cladding to improve the release etch selectivity. In the final generation material, the n-GaAs thickness is increased from 500 *nm* to 600 *nm* to reduce lateral resistance.

Table A.1: Epitaxy-A layer stack for non-transfer printable InAs/GaAs QD laser device. The number of QD in the material is 12.

#	Layer	Mole Fraction (x)	Thickness (nm)	Doping Type
12	p-GaAs contact		50	P
11	$Al_xGa_{1-x}As$	0.8 - 0	10	P
10	$Al_xGa_{1-x}As$	0.8	650	P
9	$Al_xGa_{1-x}As$	0 - 0.8	10	P
8 12X	GaAs barrier		-	-
7 12X	$In_xGa_{1-x}As$	-	-	-
6 12X	InAs		-	-
5	GaAs		-	-
4	$Al_xGa_{1-x}As$	0.8 - 0	10	N
3	$Al_xGa_{1-x}As$	0.8	1200	N
2	$Al_xGa_{1-x}As$	0 - 0.8	10	N
1	GaAs		500	N
0	GaAs Substrate		N+ GaAs 3 inch	

Table A.2: Epitaxy-B, first transfer printable epitaxial layer stack of the InAs/GaAs QD laser. This epilayer contains 500 nm release layer and 14 QD layers.

#	Layer	Mole Fraction (x)	Thickness (nm)	Doping Type
15	p-GaAs contact		50	P
14	$Al_xGa_{1-x}As$	0.4 - 0	10	P
13	$Al_xGa_{1-x}As$	0.4	1100	P
12	$Al_xGa_{1-x}As$	0 - 0.4	10	P
11 14X	GaAs barrier		-	-
10 14X	InGaAs		-	-
9 14X	InAs		-	-
8	GaAs		-	-
7	GaAs		300	N
6	$Al_xGa_{1-x}As$	0.3 - 0	10	N
5	$Al_xGa_{1-x}As$	0.3	1140	N
4	$Al_xGa_{1-x}As$	0 - 0.3	10	N
3	n-GaAs contact		500	N
2	$Al_xGa_{1-x}As$ sacrificial	0.95	500	N
1	GaAs		200	N
0	GaAs Substrate		N+ GaAs 3 inch	

Table A.3: Epitaxy-C, final transfer printable epitaxial layer stack of the InAs/GaAs QD laser. The main change from the previous generation material is a 100 nm increase in the thickness of the n-GaAs contact layer.

#	Layer	Mole Fraction (x)	Thickness (nm)	Doping Type
15	p-GaAs contact		50	P
14	Al _x Ga _{1-x} As	0.4 - 0	10	P
13	Al _x Ga _{1-x} As	0.4	1100	P
12	Al _x Ga _{1-x} As	0 - 0.4	10	P
11 14X	GaAs barrier		-	-
10 14X	InGaAs		-	-
9 14X	InAs		-	-
8	GaAs		-	-
7	GaAs		250	N
6	Al _x Ga _{1-x} As	0.3 - 0	10	N
5	Al _x Ga _{1-x} As	0.3	970	N
4	Al _x Ga _{1-x} As	0 - 0.3	10	N
3	n-GaAs contact		600	N
2	Al _x Ga _{1-x} As sacrificial	0.93	500	N
1	GaAs		200	N
0	GaAs Substrate		N+ GaAs 3 inch	

A.2 Fabrication Process Flow for transfer-printable QD Laser

This section outlines the primary process used to fabricate transfer printable QD lasers. The process represents the results of optimisations achieved over several fabrication runs and experiments. The main steps listed below are organised according to their level in lithography layer. The final step is to undercut the devices from the native substrate using a wet chemical, after which they are ready for mTP. A process flow chart is provided at the end of the appendix.

Level-1: P-Metal + Alignment Markers Definition The first level of lithography defines the ridge metal (down to $1.5\ \mu$ wide and several mm long) p-contacts. The vernier alignment markers for the subsequent lithography steps and the transfer print markers for alignment during MTP are also patterned in this level by the metal evaporation.

- Create a lift off resist structure with LOR-3A layer and S1805 resist layer.
- Lithography L1, expose with a dose of $50\ mJ/cm^2$ dose at $405\ nm$ wavelength.
- Develop the sample in MF319 for 40 sec and rinsed under running DI for 45 sec.
- BOE-DI (1-10) dip for 10 sec before loading the chips for evaporation.
- Flat evaporation of Ti/Pt/Au ($20/10/100\ nm$) metal layer for p-contact.
- 90 min lift-off in 1165 at $90^\circ C$.

Level-2: Ridge Etch The second lithography defines two $6\ \mu m$ wide trenches on either side of the p-metal strip for lateral mode confinement. There is a $0.5\ \mu m$ margin on each side. The etch is carefully stopped before reaching the QD laser.

- $200\ nm$ thick low stress SiO_2 deposition in PECVD as hard mask.
- Spin coat of AZ5214E resist with vertical sidewall.
- Lithography L2, expose with a dose of $100\ mJ/cm^2$ dose at $405\ nm$ wavelength.
- Develop the sample in MF26A for 50 sec and rinsed under running DI for 45 sec.
- SiO_2 hard mask dry-etch with $C_4F_8:H_2:He$ chemistry.
- Dry-etch $1.2\ \mu m$ deep trenches with $BCl_3-Cl_2-N_2-Ar$ chemistry.
- Deposit $100\ nm$ thick low stress SiO_2 in PECVD for sidewall passivisation.

Level-3: Facet Etch and Recess to Access n-GaAs Layer The third lithography defines the front and rear facets of the laser. The etch is carefully stopped once the n-GaAs is exposed. The recess that allows access to the n-GaAs layer is also created in the step.

- Deposit 240 nm thick low stress mix frequency (MF) SiN in PECVD as a hard mask.
- Spin coat SPR220 resist with vertical sidewall.
- Lithography L3, expose with a dose of 320 mJ/cm² dose at 405 nm wavelength.
- Develop the sample in MF26A for 70 sec and rinsed under running DI for 45 sec.
- SiN hard mask dry-etch with SF₆ chemistry.
- SiO₂ hard mask dry-etch with C₄F₈:H₂:He chemistry.
- Dry-etch ~3.2 μm deep trenches with BCl₃-Cl₂-N₂-Ar chemistry.
- Deposit 100 nm thick low stress SiO₂ in PECVD for facet passivisation. The total SiO₂ thickness on the coupon is around 380 nm.

Level-4: n-metal Evaporation The fourth lithography defines the n-metal within the 14 μm wide recess along the ridge on only one side. This recess was created in the same etch with facet formation.

- Spin coat a dual resist layers of PMGI SF11 and S1828.
- Lithography L4, expose with a dose of 320 mJ/cm² dose at 405 nm wavelength.
- Develop the sample in MF319 for 120 sec and rinsed under running DI for 45 sec.
- SiO₂ hard mask dry-etch with C₄F₈:H₂:He chemistry.
- BOE dip for 5 sec before loading the chips for evaporation.
- Flat evaporation of Au/Ge/Au/Ni/Au (14/14/14/11/200 nm) metal layer for n-contact.
- 90 min lift-off in 1165 at 90C.

Level-5: HR Mirror Deposition The fifth lithography defines HR mirror at the rear facets of the lasers.

- Spin coat a dual resist layers of PMGI SF11 and S1828.
- Lithography L5, expose with a dose of 320 mJ/cm² dose at 405 nm wavelength.
- Develop the sample in MF319 for 120 sec and rinsed under running DI for 45 sec.
- HR metal deposition:
 - 360rotation evaporation of Ti/Au (5/100 nm) metal layer (for Gen-2 Laser).
 - Deposit 250 nm Aluminum and 100 nm SiO₂ in Sputter(for Gen-3 Laser).

- 90 min lift-off in 1165 at 90C.

Level-6: Open p-metal The sixth lithography opens the p-metal by removing the dielectric hard-mask on top of it for bond-pad metal deposition.

- Spin coat a resist layer of S1828.
- Lithography L6, expose with a dose of 280 mJ/cm^2 dose at 405 nm wavelength.
- Develop the sample in MF319 for 35 sec and rinsed under running DI for 45 sec.
- SiO_2 hard mask dry-etch with $\text{C}_4\text{F}_8:\text{H}_2:\text{He}$ chemistry.
- Resist removal in 1165 at 90C.

Level-7: Bond Metal Deposition The seventh lithography defines the bond metals on p- and n-metals for device probing through a dual layer lift-off resist structure.

- Spin coat a dual layer resist layers of PMGI-SF11 and S1828.
- Lithography L7, expose with a dose of 320 mJ/cm^2 dose at 405 nm wavelength.
- Develop the sample in MF319 for 85 sec and rinsed under running DI for 45 sec.
- 360angled evaporation of Ti/Au ($50/250 \text{ nm}$) metal layer.
- 90 min lift-off in 1165 at 90C.

Level-8: n-GaAs Etch and Coupon Profiles The eighth lithography defines the final coupon boundaries by etching the remaining n-GaAs, leaving a $2.5 \mu\text{m}$ wide strip around the coupon. The sacrificial layer is also etched into the GaAs substrate with a few 100 nm over-etch to ensure that no remnants of the release layer are left.

- Spin coat a thick resist layer of SPR220 with vertical sidewall.
- Lithography L8, expose with a dose of 320 mJ/cm^2 dose at 405 nm wavelength.
- Develop the sample in MF26A for 70 sec and rinsed under running DI for 45 sec.
- SiO_2 hard mask dry-etch with $\text{C}_4\text{F}_8:\text{H}_2:\text{He}$ chemistry.
- Dry-etch $\sim 3.2 \mu\text{m}$ deep trenches with $\text{BCl}_3\text{-Cl}_2\text{-N}_2\text{-Ar}$ chemistry.
- Resist removal in 1165 at 90C.
- * After this step the sacrificial layer is exposed to air, so it is recommended to have the release etch as soon as possible and avoid O_2 plasma treatment on the samples to minimize oxidation.

Level-9: Tether Definition The next lithography is the last step in the fabrication and defines the polymer tether system around the coupons. The tethers will hold the coupons after the sacrificial layer is removed during the release etch.

- Spin coat a thick resist layer of SPR220.
- Lithography L9, expose with a dose of 320 mJ/cm^2 dose at 405 nm wavelength.
- Outages for 45 min at room temperature.
- Develop the sample in MF26A for 70 sec and rinsed under running DI for 45 sec.

Level-10: Wet Etching of the AlGaAs Release Layer The aim of this step is to undercut the devices to release them from their original substrate. The suspended coupons are then ready for MTP.

- Cut a piece of the chip for the undercut test (if required).
- Prepare an HCl-DI (1-1) solution and allow to cool to clean-room temperature.
- Prepare an ammonia DI (1-10) mixture for the deoxidation dip prior to release etch.
- Dip the sample in the Ammonia-DI (1-10) solution for 30-45 seconds (may be less or more depending on the time the sample was exposed to air).
- Release etch in the HCl-DI (1-1) solution at 19°C .
- Rinse the samples several times very gently with a pipette in DI water until the acid was completely removed.
- Allow the sample to dry naturally by placing it at an angle. The sample can also be dried gently with an air gun, but this can be risky depending on the strength of the tether.

Appendix B

Laterally Coupled Distributed Feedback QD Lasers

B.1 Single Mode QD Lasers

The Fabry-Perot (FP) laser is a basic semiconductor laser made with a waveguide and two mirrors at each end. When the electric current flows through it, light is produced. Some of this light stays inside the cavity because of the reflective mirrors, and more light is added through stimulated emission. When the gain equals the losses, the FP laser starts emitting with multiple longitudinal modes. However, most applications require a laser that operates at a single wavelength. Single-mode lasing operation could be achieved by forming an external cavity via SOI platforms [157] or employing corrugations on III-V (i.e. sidewall grating) [158].

In this work, we investigated laterally coupled distributed feedback grating (LC-DFB) on III-V to achieve single mode lasing of the lasers around 1310 nm. The process development for fabrication and the characterisation of the designed lasers together with the challenges faced in the trial-run transfer printable.

B.2 Design of LC-DFB Laser

Distributed feedback (DFB) is implemented by dry etching the gratings on the surface of the III-V to achieve longitudinal single mode emission in QD lasers. The refractive index modulation on the guide could be realised by a re-growth process or a post-growth process. The first technique requires the definition of the gratings by etching very close to the active layer, followed by filling them with upper-cladding deposition. The second technique involves dry etching the gratings into the top cladding layer. The buried gratings via regrowth provide a strong mode - grating interaction and are demonstrated on InP based 1550 nm lasers [159, 160] as well as

GaAs based QD lasers [161, 162]. Poor repeatability, process complexity, and contamination issues remain a challenge. The surface gratings allow for relatively simple processing with more flexibility. Surface gratings can be defined on the laser ridge ([163] and along the ridge. In this study, QD lasers with grating structure on the ridge sidewall have been fabricated as shown schematically in Fig. B.1.

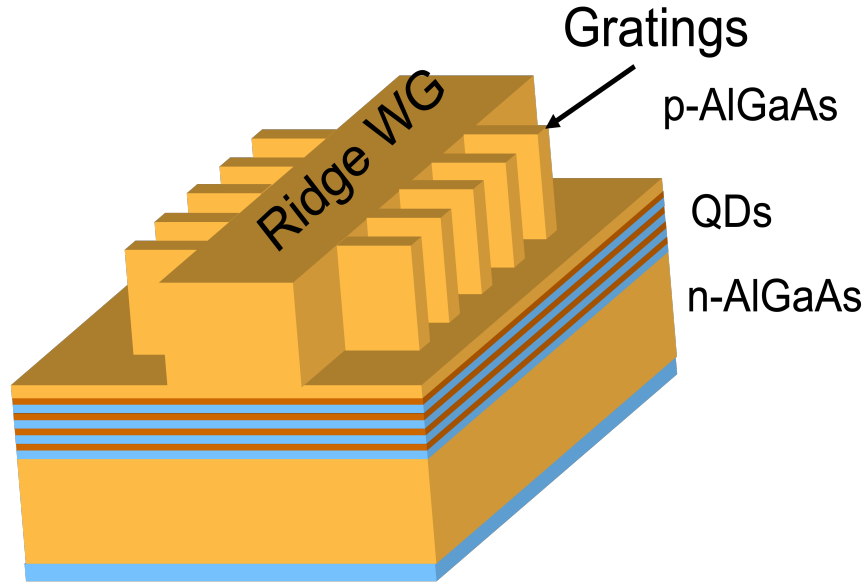


Figure B.1: Schematic diagram of the lateral coupled distributed feedback (LC-DFB) grating defined on QD laser surface in the same etch with the ridge.

Similarly to FP lasers, a DFB laser starts single mode lasing once one of the supported longitudinal modes in the cavity satisfies the gain condition (B.1). In other words, the laser emits at the mode that experiences the largest gain and/or the lowest mirror losses.

$$\Gamma_A g_A = \alpha_i + \alpha_m \quad (\text{B.1})$$

where α_i is the internal loss, α_m is the mirror loss, g_A is the gain of the active medium and Γ_A is the optical mode confinement factor in the active layer.

Extensive research has been carried out on gratings, resulting in comprehensive models describing distributed reflections using both the transfer matrix method and the coupled mode theory [164, 165]. A Bragg reflector is a wavelength-dependent mirror that favours only one longitudinal mode that satisfies the Bragg condition B.2.

$$\Lambda = \frac{m\lambda_B}{2n_{\text{eff}}} \quad (\text{B.2})$$

where Λ is the grating period, λ_B is the wavelength of light propagating within the structure (Bragg wavelength), n_{eff} is the effective refractive index of the mode and m

is the order of the grating. In this work, we only investigated the first-order grating when m equals 1.

This condition will provide constructive interference for back-reflected waves at the Bragg wavelength. The calculation suggested that the grating period should be 194 nm to achieve lasing around 1310 nm, assuming the effective index (n_{eff}) of the mode is 3.41. Figures B.2(a) and (b) show the schematics of the features of the patterned grating next to the ridge on the side wall of the ridge and in the groove of the ridge next to the laser ridge, respectively. The cross section on the gratings is given for both approaches. A $\lambda/4$ phase shift section is placed in the centre of the gratings to maintain stable single-mode operation. The process development and challenges for both techniques are discussed in this section.

The ratio of the semiconductor portion (σ) to a grating period (λ) determines the duty cycle of a Bragg grating and is shown schematically in Fig. B.2. The duty cycle (w) is set at 50% in the design, but in this work it is measured to be around 60% after fabrication. A higher duty cycle results in an increased coupling strength in the gratings, but it becomes difficult to etch the grating pattern in the semiconductor. It is important to ensure that the gratings provide sufficient feedback without being a source of additional losses in the laser.

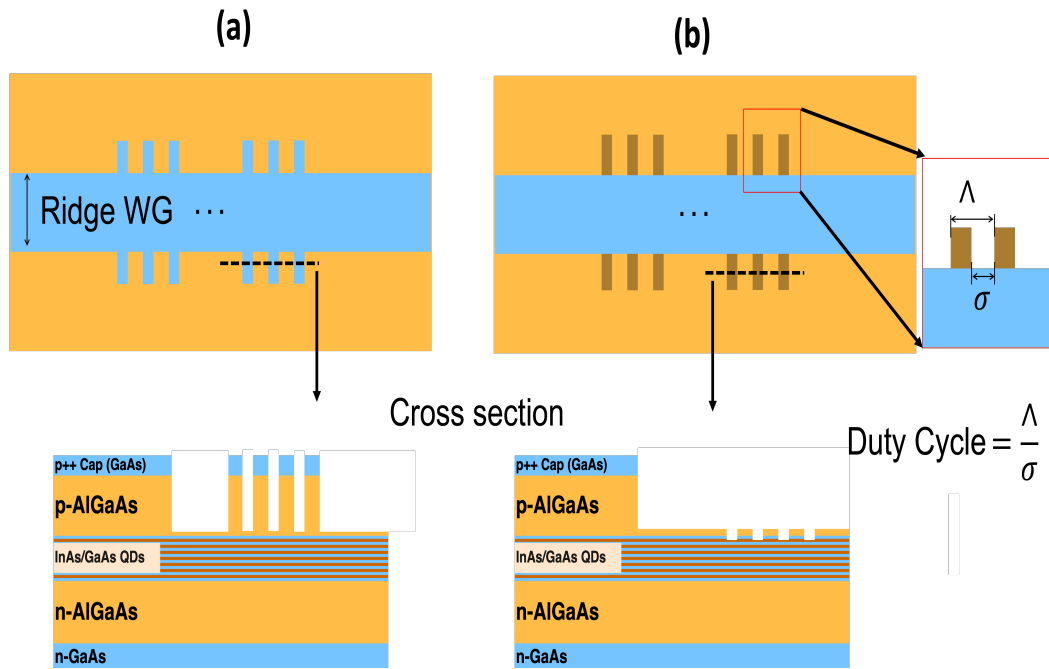


Figure B.2: The rectangular gratings features defined (a) on ridge sidewall and (b) in ridge recess. The cross-section over the gratings for both types are given.

Another very important parameter for DFB lasers is the coupling coefficient κ and can be described by eq. B.3. This represents the strength of the coupling between the optical mode of the laser and the grating. To realise a single mode laser with good

performance, the coupling intensity κL (L is the laser cavity length) is usually around 1-2.

$$\kappa = \frac{(n_1^2 - n_2^2) \sin(m\pi w)}{n_{\text{eff}} \lambda} \Gamma_{\text{grating}} \quad (\text{B.3})$$

where n_1 and n_2 are the average refractive index of the III-V section (high index) and the dielectric section with a lower index that compose the grating, n_{eff} is the effective index of the guided mode, λ is the wavelength in free space, w is the duty cycle of the grating, m is the order of the grating, and Γ_{grating} is the field overlap integral with the grating region, which is around 0.108% in this case.

Figure B.3(a) shows the changes in refractive index with respect to the ridge width of 2 and 3 μm with a grating extension of 500 nm on both sides. Based on effective index modulation, the simulated coupling coefficient κ as a function of the etch depth is given in Fig. B.3(b). As shown in simulation, increasing the depth of the etch in the active region increases the mode coupling with the gratings and κ . Selecting the proper etch depth that could provide sufficient feedback while not being an additional loss source in the laser.

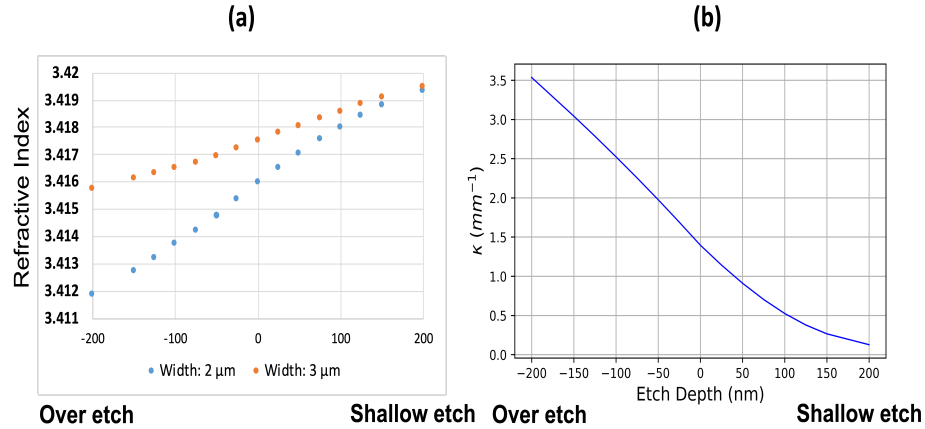


Figure B.3: (a) The changes in simulated refractive index with respect to change in ridge width. (b) Coupling coefficient κ as a function of etch depth into the active layer. 0 indicates etch stops right above the QD layers.

The simulated transmission and reflection for the DFB design with two different grating etch depths (50 nm and 100 nm) are given in Fig. B.4. The additional dips on the high-frequency side of the spectrum is due to coupling to the backward first-order cladding mode and radiation [166].

B.3 Fabrication of DFB Laser

The first approach shown in Fig. B.2(a) starts with the deposition of 450 nm SiO_2 hard mask on the GaAs sample. Then e-beam lithography exposure patterns the 2 μm

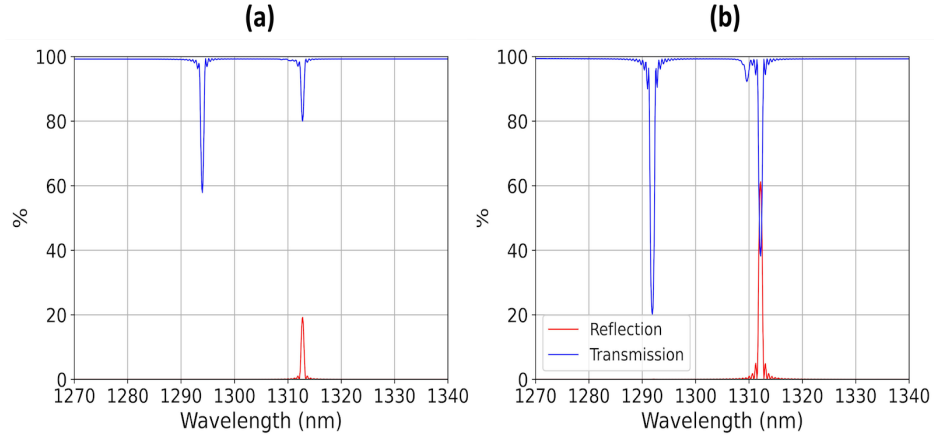


Figure B.4: Simulated transmission spectra of the gratings with 194 nm period and 50% duty cycle, designed to be centered at 1310 nm. (a) 50 nm shallow and 100 nm over etched grating results different coupling strengths and reflection. Number of grating periods N is 2000.

wide ridge waveguide with 500 nm wide and 97 nm long rectangular grating extensions (σ) on both sides of the ridge using a ZEP520A [167] positive tone electron beam resist. After development in ZED-N50 [168] for 60 seconds, 50 nm Ti is evaporated on the sample as a hard mask for the subsequent dielectric and III-V etch step. After lift-off in 1165 resist remover for 45 minutes, the dielectric hard mask is dry etched. Next, ridge etching is performed using the chemistry developed in section 2.3.1. Then the ridge sidewall is passivated with a 100 nm thick SiO₂ layer. A Ti/Au (50 / 300 nm) p-contact layer is deposited following the optical lithography. This is followed by Au/Ge/Au/Ni/Au n-contact metal deposition on the backside of the GaAs substrate, which has been thinned to 120 μ m. Finally, the 7° tilted lasers are cut into bars and measured without any facet coating. As this is an investigation run, the lasers are not transfer printable, so the fabrication process is relatively simple compared to a standard coupon run. Characterisation results for these devices are presented in section B.4.

Figure B.5(a) shows an SEM image of a ridge with lateral grating patterns after the e-beam exposure and development. Following the ridge etching using a Ti + SiO₂ mask, the resulting ridge and gratings are shown in Fig. B.5(b). 50 nm Ti is fully etched during the ridge etching and the remaining SiO₂ is thick enough to protect the highly doped p-contact layer.

The issue in this approach is the non-uniform etch depth control between the grating teeth. Due to the high aspect ratio of the grating features ($\sim$ 90 nm wide and 1.2 μ m tall), the etch depth varies across the teeth of the grating, becoming shallower towards the laser ridge due to the footprint effect and the RIE lag inherent in dry etching. This phenomenon results in different etch depths between open surfaces and narrow areas. Specifically, the etch depth is 1.5 μ m at the far end of the grating and decreases to 0.7 μ m near the root of the laser ridge, as shown in Appendix-B with

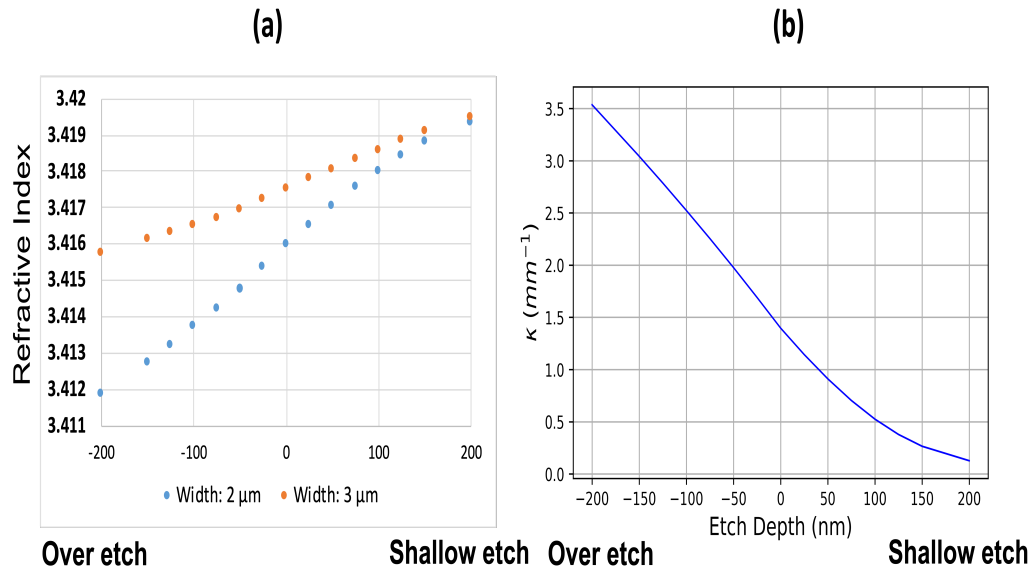


Figure B.5: (a) SEM images of the rectangular gratings features defined on the ridge sidewall after developed in ZED N50 for 60 seconds. (b) After the ridge etch.

more details. Achieving a uniform etch depth would be achieved by reducing the aspect ratio of the grating features.

The second approach investigated in this thesis is shown in Figure B.2(b). Given the high aspect ratio of the width and depth of the grating in the first approach, this design aims to achieve better uniformity in the grating etch by reducing the aspect ratio. The process starts with the evaporation of Ti / Au (50 / 110 nm) p-metal evaporation. This helps mitigate potential resistivity issues by exposing the surface to only one layer of lithography. This is followed by the deposition of 120 nm SiO₂ and then the definition of the grating patterns perpendicular to the p-metal with 1 μm gap between two grating patterns in a pair. The features are transferred to the SiO₂ mask by dielectric dry etching. The p-cladding layer is etched during the 20-second semiconductor etch, corresponding to 300 nm of material etch. After resist removal, fabrication continues as per the standard fabrication steps. This pre-etch maintains the same grating patterns that will be transferred into the active region during the ridge etch, and provides etch depth modulation along the ridge recess. The rationale for the 300 nm pre-etch is determined by the difference in etch rate in the ICP for open surface and narrow features. A 150 nm over-etch is estimated in the rectangular grid trench compared to the rest of the ridge surface.

One challenge in this approach is the resist collapse during the dielectric etch. The resist mask is approximately 90 nm wide and continues for a 1 μm long distance. Only in a few devices are the gratings successfully transferred to the hard-mask as given in Fig. B.7(a). The majority of the grating features collapse during the dielectric etch and results in a distorted pattern as shown in Fig. B.7(b). In addition, different

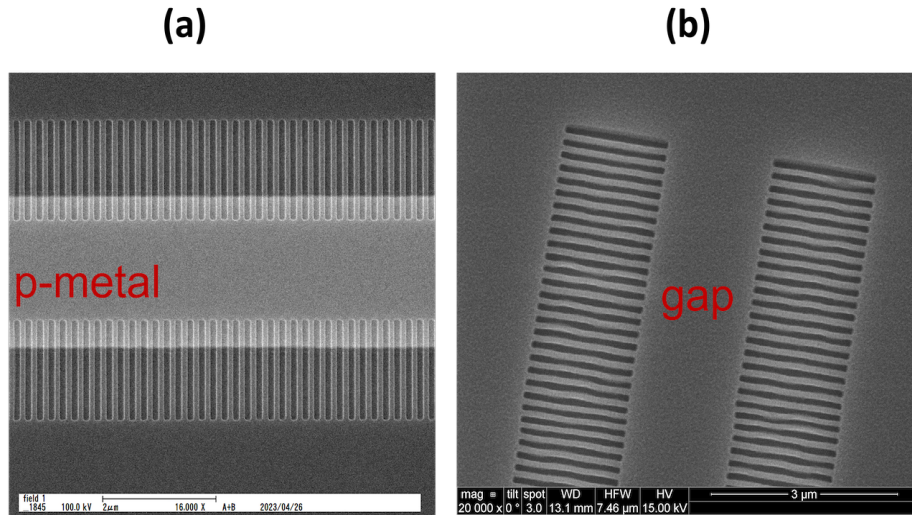


Figure B.6: SEM images of grating features after e-beam expose (a) on either side of p-metal and (b) on black surface. The rectangular gratings are split into two sections with a gap in between to enhance mechanical strength of the narrow lines.

exposure doses were tested to optimise the e-beam write to achieve a robust resist mask for dielectric etch. Although the resist looks fine before the etch, it mostly collapsed during the SiO₂. The dielectric thickness is also reduced from 120 nm to 60 nm to minimize the time that the resist is exposed to the etch recipe, but it also ended up with wavy gratings pattern. It requires more investigation to optimize the process. Another option to try would be to change the dielectric from SiO₂ to SiN mask as the SiN mask recipe (V_{pp} is 86 V) does the etch in a more gentle environment compared to the SiO₂ recipe (V_{pp} is 285 V). The reason behind the use of SiO₂ is the film stress.

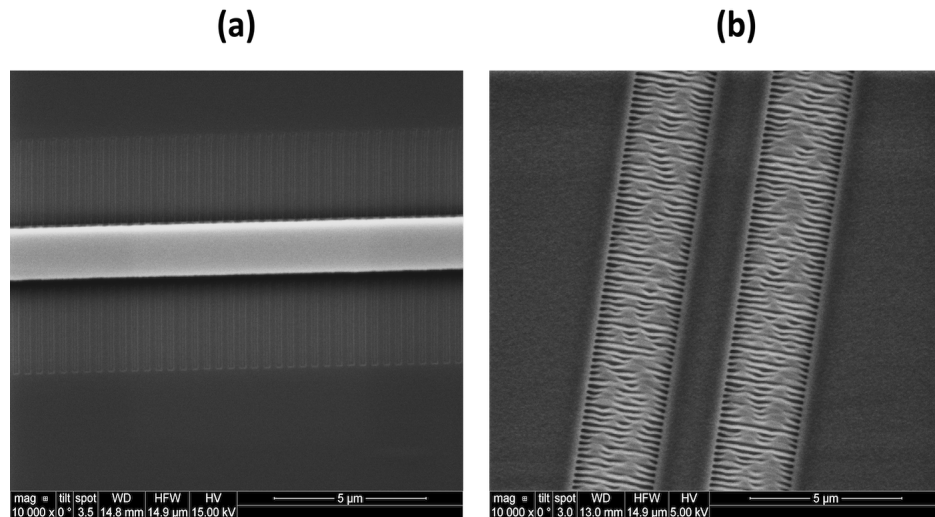


Figure B.7: (a) SEM images of rectangular grating features on QD laser. (b) The resist mask collapsed during dielectric etching, resulting in a distorted grating pattern on the devices.

B.4 Characterization of LC-DFB Lasers on GaAs

As mentioned above, the lasers presented above have no wavelength control and therefore exhibit multi-longitudinal mode emission. One approach to achieving single-mode emission from this device is to etch Bragg gratings along the ridge waveguide to form a laterally coupled distributed feedback (LC-DFB). The design and fabrication of the single mode laser using this approach is presented in section-B.2. Figure B.8(a) shows a schematic of the laser with grating structures defined in the p-cladding on the ridge waveguide laser. The SEM image of the actual device is shown in Fig. B.8(b).

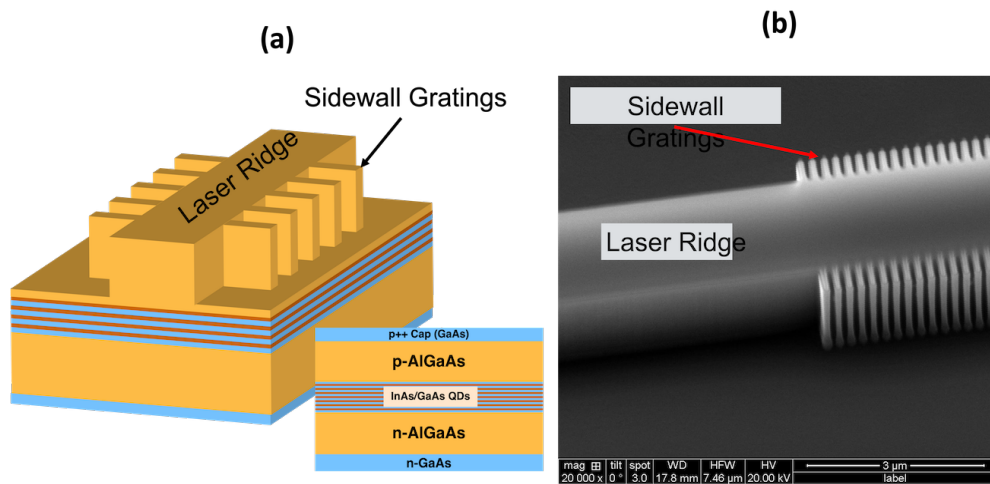


Figure B.8: (a) Schematic of the DFB laser with laterally coupled grating structure along the ridge waveguide. (b) Side view SEM images of sidewall corrugations on GaAs QD laser.

The $2\ \mu\text{m}$ wide ridge waveguide together with the $500\ \text{nm}$ long grating extension are fabricated with a 7° tilt with respect to the cleave line. Since the facets do not have an anti-reflective (AR) coating, the angled waveguide is used to minimise reflection from the facets. Figure B.9(a) shows the recorded spectrum of a $1.8\ \text{mm}$ long laser with a grating structure at different bias currents. The corresponding LI curve is shown in figure B.9(b). The device exhibits a threshold current of $32\ \text{mA}$ and roll-over after $125\ \text{mA}$ injection current. The device then fades out and stops lasing at higher current injection levels as a result of self-heating. As the refractive index changes, the wavelength of the feedback from the sidewall grating can shift, causing the lasing mode to be detuned from the gain peak.

Characterisation of the lasers shows that there is a large variation in device performance. Only few devices showed a stable lasing with side-mode suppression ratio (SMSR) up to $-35\ \text{dBm}$ as given in Fig. B.9(a). Most of the devices struggle to achieve stable single-mode operation. They have a spectrum with multiple- peaks or chaotic lasing as seen in Fig. B.10(a) and (b). These devices show an initial single mode emission at lower bias current but then get multi-moded even moderate

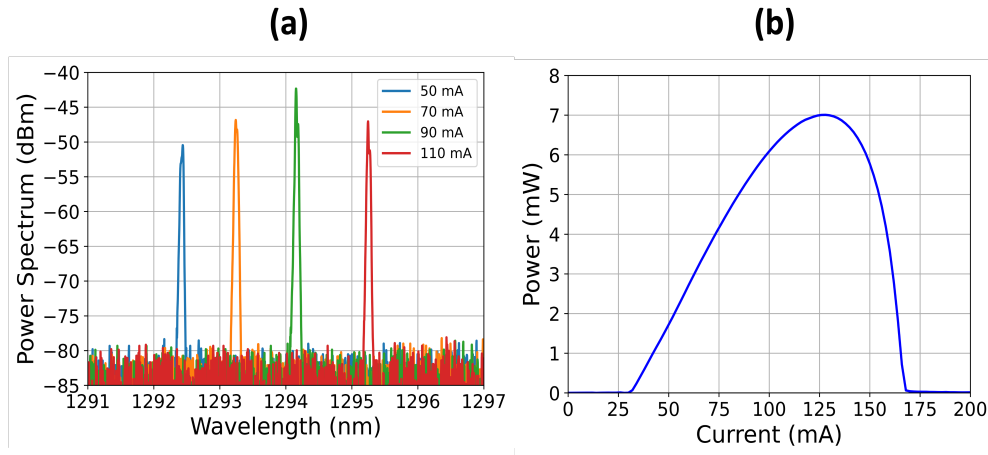


Figure B.9: (a) Recorded optical spectra of the single DFB laser operating at different drive current from 50 mA to 110 mA. (b) Light-current (L-I) characteristics of the fabricated laser with a length of 1.8 mm under continuous-wave (CW) condition at room temperature.

injection current levels. An typical LI curve for such lasers is given in Fig. B.10(c).

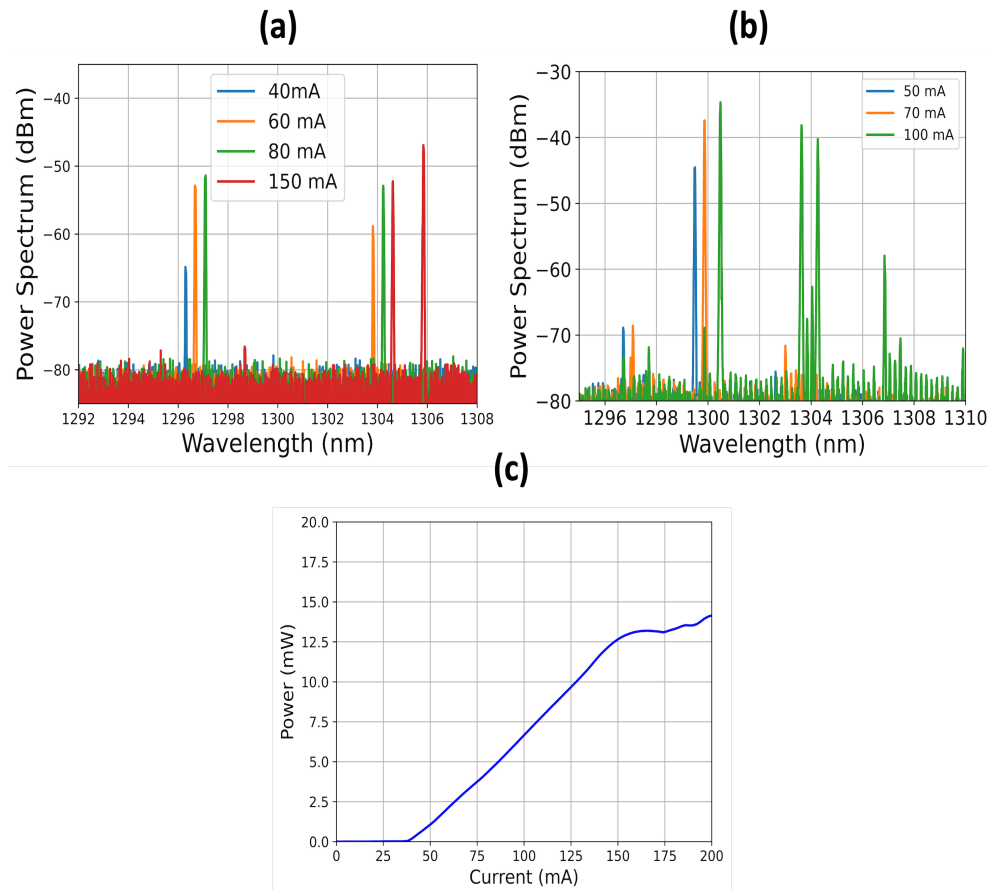


Figure B.10: Optical spectra of the single DFB lasers with cavity length of (a) 1.2 mm and (b) 1.8 mm operating at different injection current levels. (c) L-I plot for the laser in (b) showing a threshold current of 40 mA.

Further investigations are carried out using focused ion beam (FIB) cross section

analysis on the gratings features. FIB cuts show that there is a non-uniform etch profile within the grating tooth depth, which causes the stability problem in the lasers, as shown in Fig. B.11. The etch depth varies across the grating teeth and is shallower toward the laser ridge due to the footprint effect and RIE lag of dry etching. This is a common phenomenon in dry etching and results in a difference in etch depth between an open surface and a narrow area. The etch depth is measured as $1.5 \mu\text{m}$ at the far end of the grating and becomes shallower to $0.7 \mu\text{m}$ at the root of the laser ridge. A uniform etch depth would be achieved by reducing the etch depth between two adjacent grating teeth.

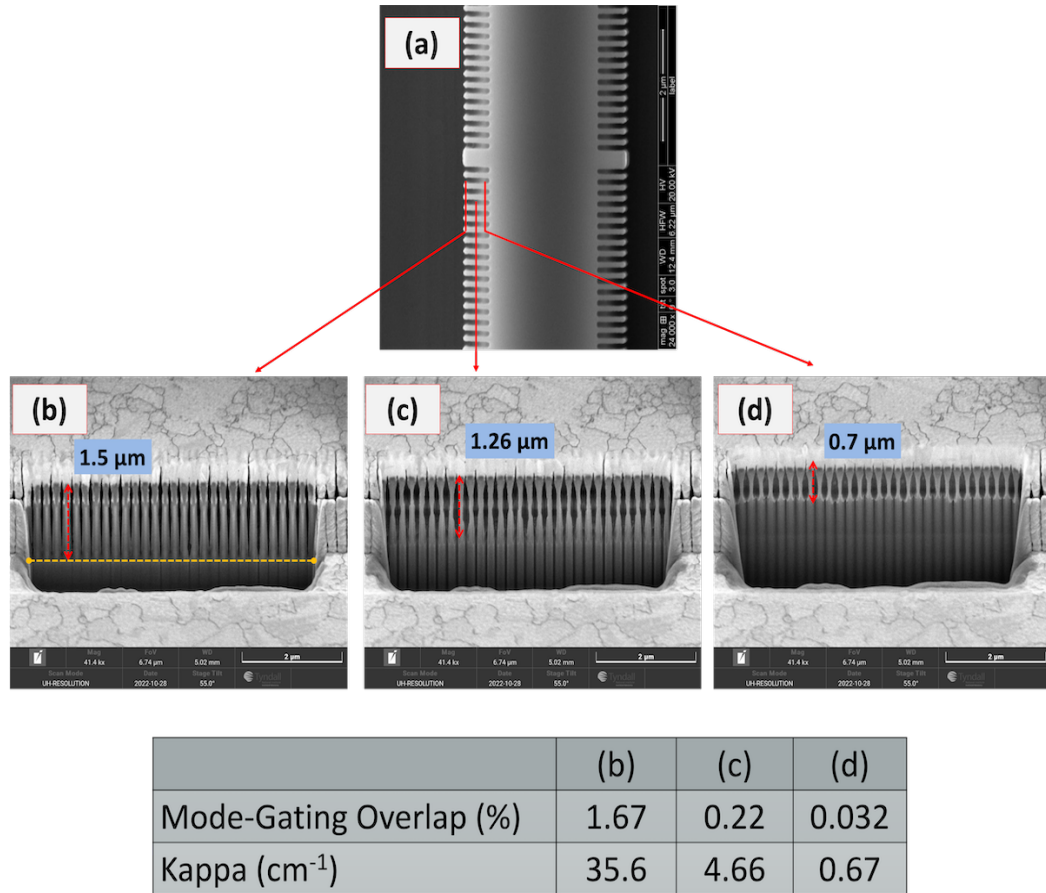


Figure B.11: (a) Plane view of a DFB laser with lateral sidewall gratings. (b)-(c)-(d) Measured etch depth at grating tooth after a gradual FIB cross section cut on grating teeth at different distance to the laser ridge. Etch depth gets shallower as it gets closer to the ridge. The table shows the kappa and mode overlap with the grating as a function of etch depth. As the etch depth becomes shallower, the kappa and mode overlap with the grating decreases.

A deep-etched active waveguide experiences higher surface recombination and optical scattering loss. In addition, a waveguide of practical width can support multiple transverse modes. The unwanted higher-order modes are often favoured for lasing as they have higher κ values [169]. Simulated κ values for different grating etch depths are given in the table in Fig. B.11. Given the huge aspect ratio of the grating trench (194 nm wide and $>1.2 \mu\text{m}$ high), it is challenging to ensure uniformity of the etch

depth across the devices. In this respect, a second process with a shallower grating is designed on the basis of the learning from the first run to achieve optimal etch depth control for wavelength selection. However, a device-level demonstration is not achieved in this work due to process-related challenges and is discussed as future work.

B.5 Conclusion

The design and process development for single mode lasers using laterally coupled distributed gratings patterned on the ridge sidewall is explained. The characterisation of laterally coupled distributed feedback grating (LC-DFB) lasers is discussed in this section. The non-uniform etch depth across the grating makes it difficult to achieve stable mode operation. The second fabrication approach suffers from resist collapse that degrades the pattern during dielectric dry etching. The fabrication challenges and the corresponding solutions and improvements are proposed.

Appendix C

Patternable Adhesive Layer for MTP

This section reports on how to pattern InterVia with a thickness below 500 *nm* using the standard photo-lithography technique. Intervia is a kind of photodielectrics which is spin-coated, negative tone, TMAH(aq) developable and curable at low temperatures. It is widely used for advanced packaging applications, e.g. redistribution of bond pads on wafer-level. The products available on the market are Intervia 8023-10 and 8023-2 which have different dilution ratios in PGMEA dissolve. In this thesis, Intervia 8023-10 is used with PGMEA diluted to achieve a thickness of only a few 100 *nm*. Patterning experiments are conducted using a blank Si wafer and SOI with 7 μm deep trenches.

Lithography Parameters

- Prepare the InterVia-PGMEA (1-2)/(1-4) mixture.
- Spin coat at 4500 rpm for 50 sec.
- Soft bake for 1 min @ 100C.
- Expose in MA6 for 15-30 sec in Low Vacuum Mode
- Post expose bake for 1 min @ 100C.
- Develop 45 sec in MF26A.
- Resulting thickness 480 *nm* / 200 *nm*

Figure C.1 shows optical images of patterned rectangles of different sizes on blank Si with InterVia diluted in PGMEA by 1 to 2 and 1 to 4 in weight. The best results are obtained at these dilution rates with an after-development thickness of 480 *nm* and 200 *nm* respectively. Although InterVia produces thinner films at higher dilution ratios, patterning becomes more difficult. In addition, adhesion of the film can be an issue at higher ratios in spin-coating. In addition, spray coating also allows film

coating with thickness down to 50 nm but it is possible with a very high dilution rate of 1 to 50. Partial or no patterning were typical issues on these samples.

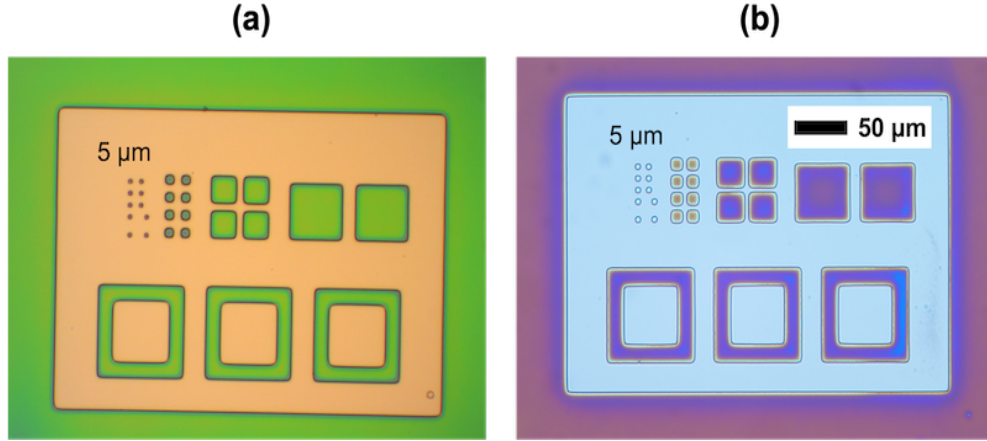


Figure C.1: Dilute InterVia at a ratio of (a) 1 to 2 and (b) 1 to 4 in PGMEA after patterning using the above recipe. Features down to 2 μm in size were successfully patterned.

The same recipe is applied to SOI wafers with deep trenches as shown in Fig. C.2(a). The material accumulated towards the sidewall of the groove (shown in Fig. C.2(b)), which results in a longitudinal misalignment of several microns during laser integration, is completely removed as shown in Fig. C.2(c).

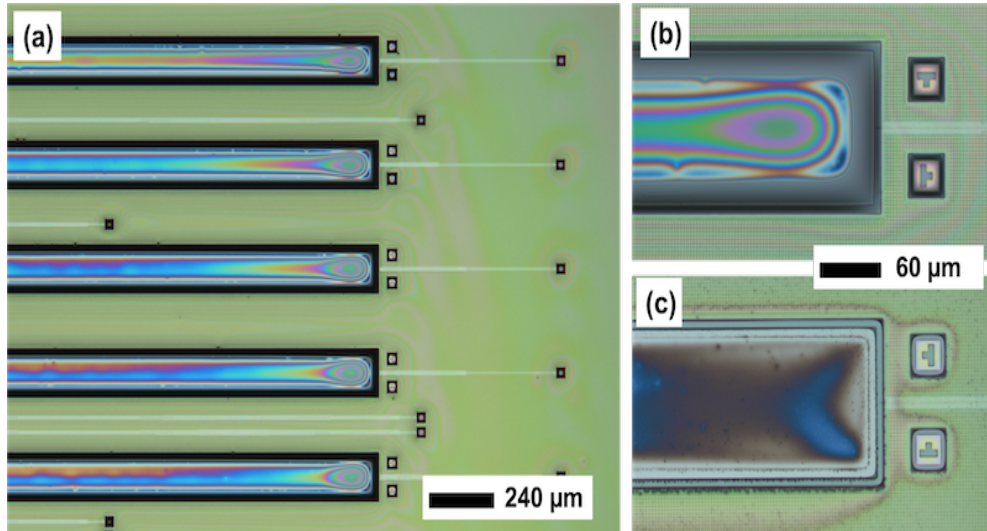


Figure C.2: (a) Spin-coated InterVia on SOI wafer with deep trenches. (b) Zoom-in one of recess shows the material accumulation towards the recess sidewall. (c) Image of another recess after patterning shows the removal of the excess material.

The patterning process is very sensitive to the age of the InterVia and the compound. An aged solution could make repeatability very difficult and result in thinning of the film during development after lithography. In addition, the concentration of TMAH in the developer is another important factor to optimise. For example, an aggressive development characteristic is observed when using MF319 compared to MF26A.

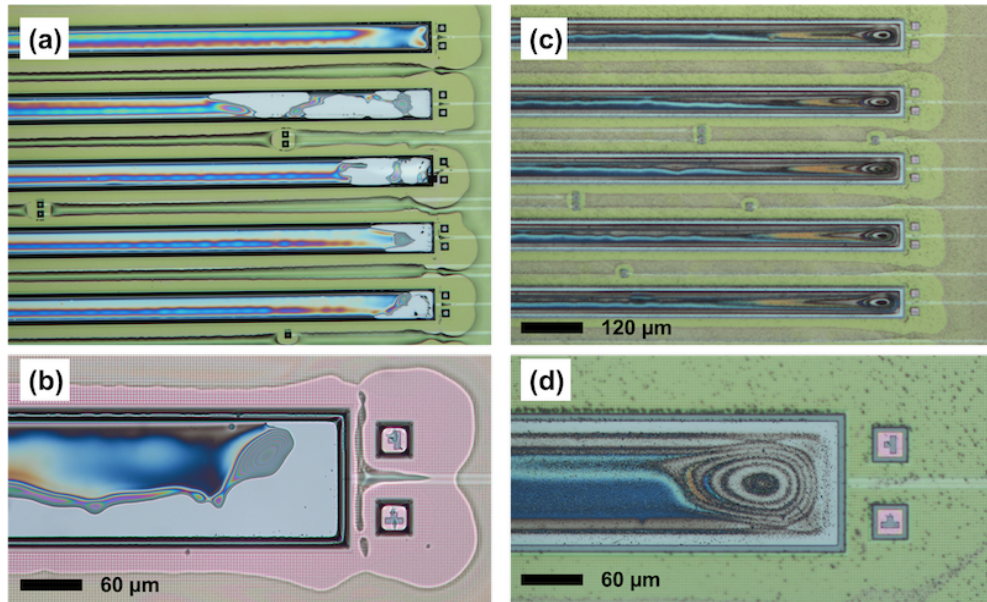


Figure C.3: (a) Image of a sample with adhesion problems showing the non-uniform material coating on the recessed SOI. (b) Magnified view of one of the recesses. (c)-(d) Image of a sample with InterVia thinning during development due to ageing.

Appendix D

Python Codes Used for the Measurements

The Python scripts developed for automated instrument control during device characterization and analysis are provided in this section. The complete scripts are available at the following [GitHub repository](#).