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Design and Fabrication of a Circular Digital Variable Optical Attenuator

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ABSTRACT

The second generation circular digital variable optical attenuator (CDVOA) with an effective area of 1500 μm diameter has been designed and fabricated based on SOI technology. C-band incoming Gaussian light can be reflected to an outgoing fiber from a shiny circular area, which is divided into sectors that can be individually tilted and addressed electrostatically to achieve variable light attenuation. Using a delay mask process, each movable component i) has an underlying ridge frame to maintain flatness, ii) is suspended by two micro beams at a bridge structure that connects to a handle where aluminum electrode is located underneath, and iii) is separated by wall structures at the handle area to reduce crosstalk from adjacent electrodes. Critical fabrication processes including the mirror and chip release are performed using a HF vapor phase etcher. Fluidic pressure and chip-dicing shocks are avoided. Initial results show that a mirror sector suspended by two 345 μm long beams with a cross-section of about 5×5 μm^2 can be tilted to 2.8° at about 18 V driving voltage. Initial interferometric measurement gives estimated individual mirror flatness after metallic reflective coating to be about $\lambda/15$. The assembled chips are ready for further testing and characterization.

Keywords: SOI, VOA, HF vapor-phase-etcher, DRIE, and delay-mask process.

1. INTRODUCTION

As described in the work of Brackett et al.[1] that intensity deterioration over distant transmission lines is inevitable, signal amplifiers[2] are needed to retain the original energy level. The wavelength dependency of these components has been well known and thoroughly studied[3−6]. For a wavelength division multiplexed (WDM) system where multiple optical signals can be multiplexed to transfer along a single optical fiber, one objective is to maintain a flattened transmission bandwidth by gain equalizers for example. However, if the input optical power varies, the output profile is also distorted. Variable optical attenuator (VOA) was designed to solve this problem. By adjusting the attenuation level of individual wavelength channel, output profile that is equalized and independent to the input optical intensity variation can be obtained. As the telecommunication network becomes more densely developed, the number of multiplexed input is expected to be rapidly expanding. Such growth demands more durable, accurate, compact, and fast-response VOAs for numerous de-multiplexed wavelength channel outputs. Increasing novice MEMS-based VOAs will be available to suite various needs as fabrication technology advances. Riza et al.[7−9] proposed a digital paradigm which inspired this project as an attempt to extend the work.

2. OPERATION PRINCIPLE

The circular digital VOA is the 2nd generation device designed to improve the shortcomings we observe from the 1st generation[10, 11]. A 4-bit device is illustrated in Fig. 1 as an example. It consists of 6 mirror sectors that are arrayed to form a circle with a radius R of 750 μm. The gap between adjacent mirrors is 2 μm. The area of each sector is computed such that the reflected intensity corresponds to a certain portion of the overall intensity.
In general, the intensity reflected from the k^{th} bit mirror should be twice as much as the $(k+1)^{th}$ bit mirror as described in the concept of the rectangular digital VOA[12]. In Fig. 1, each of the two 3rd bit mirror is identical to the 4th bit, therefore tilting the two mirrors of the 3rd bit should have twice the optical effect of tilting the single 4th bit mirror. The Gaussian intensity volume above the 4th bit sector V_{G4} can be expressed in terms of the Gaussian amplitude A, the half Gaussian beam waist w =

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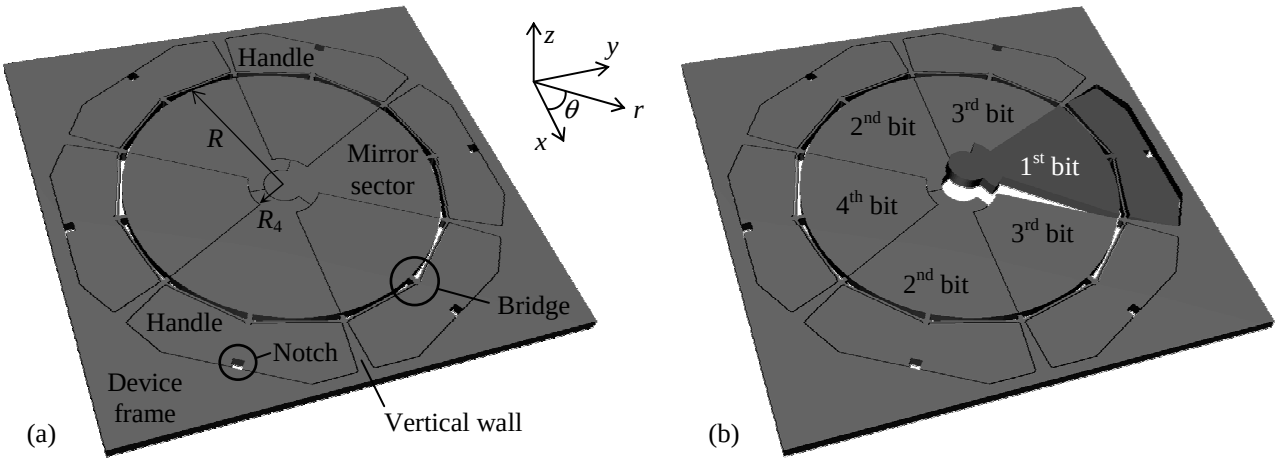


Fig. 1. The operation principle of the 4-bit device. The layout in the *x*-*y* plane is directly taken from the mask editor program. The *z*-scale is exaggerated for illustration purpose. (a) The 4-bit device consists of 6 mirror sectors. Each mirror sector is linked to handle via a bridge structure where suspension beams are connected from the vertical walls of the frame. (b) The 1st mirror bit is actuated. Light reflected from the actuated bit will be diverted away from the outgoing fiber, which is not shown here.

250 μm, the inner radius R_4, the outer radius R = 750 μm, and the 60º span angle. A close form solution can be obtained by using the polar coordinates r and θ as shown in the following equation.

$$V_{G4} = \int_0^{\frac{\pi}{3}} \int_{R_4}^{R} \left(A \cdot e^{-2\frac{r^2}{w^2}} \right) r \cdot dr \cdot d\theta = \frac{\pi A w^2}{12} \left(e^{-2\frac{R_4^2}{w^2}} - e^{-2\frac{R^2}{w^2}} \right) \tag{1}$$

A C-band incoming signal from above the device with 500 μm Gaussian beam waist can be collimated and pointed at the center of the circular area with metallic coating and reflected to an outgoing optical fiber that is not shown in the illustration. An advantage of a circular array is that the illumination orientation in the *x*-*y* plane is independent due to the symmetric layout. Each sector is bridged to a handle where an aluminum electrode will be located underneath after assembling the device chip and the electrode chip. The bridging structure is where the suspension beams link between the tiltable mirror-bridge-handle component and the vertical walls, which serve as electrostatic barriers between adjacent electrodes to reduce crosstalk. The two suspension beams are placed in a V-shape configuration not only to conform to the outer radius of the circular sector. Compared to a "cross" design with the "+" shape where the two suspension beams are coaxially connected and orthogonal to the bridge's longitudinal axis, the V-shape beams help reduce beam buckling and constraint planar mirror movement. All junctions of the suspension beams are rounded to reduce stress concentrations.

The mirror-bridge-handle configuration provides mechanical leverage to generate large optical effect with low driving voltage. Compared to the design in the 1st generation VOA, the larger handle area is definitely more efficient in consuming the electrostatic energy to tilt the mirror. We are also aware that intrinsic stress in the device layer of a SOI wafer is inevitable. Even at stationary stage without actuation, supporting the mirror from the device frame directly with suspension beams would result in mirror bending possibly due to slight frame contraction upon sacrificial oxide release. Greywall proposed the usage of a T-bar stress reliever[13] at the junction where the suspension beam meets the frame. This method might not be applicable to us as the extra degree of freedom from the T-bar would allow the entire mirror to be pulled down as well as tilted. Applying electrostatic force on the handle and joining the suspension beams to a bridge structure would solve mirror bending problems that occur during actuation and from intrinsic SOI stress, respectively. Fig. 1b illustrates how the 1st bit mirror is actuated and tilted. A notch at the handle provides a path for the electrode routings to avoid short-circuiting when the edge of the handle is in contact with the electrode wafer.

Another advantage of a symmetric circular configuration is that the algorithm used in computing the mirror areas is less complicate compared to previous work with rectangular mirrors. Although not visually obvious, the intensity reflected from the 1st mirror bit that consists of a small circle, a 120º small sector, and a 60º large sector is computed to be equal to the sum of all other bits and twice as much the intensity from the two mirrors of the 2nd bit. With a given sequence to actuate these 6 mirrors, this device is capable of providing 16 attenuation levels. For visualization purpose, 4 of the 16 possible configurations showing the reflected Gaussian intensity volume are illustrated in Fig. 2.

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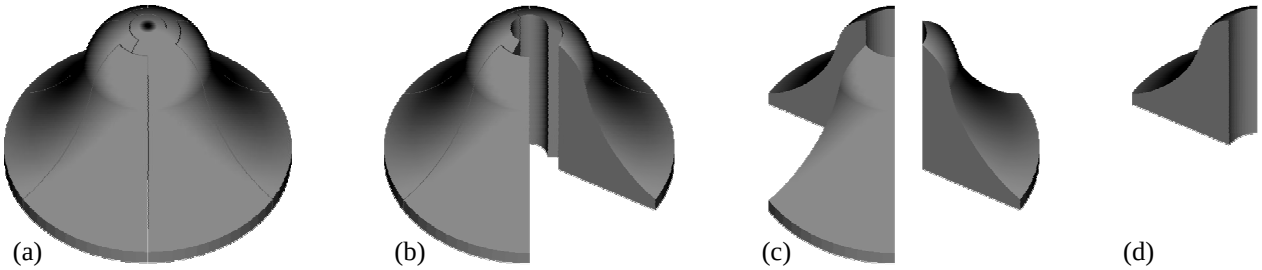


Fig. 2. Visualized Gaussian intensity volume reflected from the circular digital VOA as viewed from a perspective angle different from that in Fig. 1. (a) Stationary or the 0000 configuration. All mirrors are at "on" state. Attenuation is 0%. (b) The 1000 configuration where the 1st bit is actuated or at "off" state. Attenuation is $2^3/16 = 50\%$. (c) The 1100 configuration where both the 1st and the 2nd bit are at "off" state. Attenuation is $(2^3+2^2)/16 = 75\%$. (d) The 1110 configuration where only the 4th bit is at "on" state. Attenuation is $(2^3+2^2+2^1)/16 = 87.5\%$

3. FABRICATION

The fabrication begins with a 15 μm frontside, 2 μm buried oxide (BOX), and 250 μm backside SOI wafer, which is first oxidized by 1 μm. Photoresist is spincoated on the backside and photolithographically patterned. Exposed oxide is etched in BHF solution. The pattern on the backside oxide is transferred to the backside handle layer by DRIE. A patterned backside view is rendered in Fig. 3a. A circular block at the center of each chip is designed to cover the openings from the frontside mirror pattern. It provides protection to the buried oxide by minimizing the fragile thin film area that is accessible from both the frontside and the backside. It is possible to fabricate several height steps on the frontside device layer with multiple mask and successive DRIE using the delay-mask process introduced by researchers including Bourouina[14]. A similar process is used that creates 2 height differences to reduce the suspension beam thickness to 5 μm while maintaining wall barriers to be 15 μm between adjacent electrodes. Spacers separating the device chip and the electrode chip are therefore not needed. The fabrication continues by growing thin 200 nm oxide on the processed wafer. Photoresist is spincoated on the frontside and photolithographically patterned with alignment to existing backside marks. After immersing the wafer in BHF to pattern the frontside oxide, photoresist is stripped in acetone. The wafer is then dried, spincoated a new layer of photoresist, and patterned photolithographically for the 3rd time with alignment preferable to the frontside marks.
After the 1st DRIE at 5 μm depth, the photoresist is stripped by oxygen plasma, leaving behind a partially patterned frontside device layer and an oxide mask. When the 2nd DRIE is completed for the rest of the 10 μm depth, the mirrors and the chips

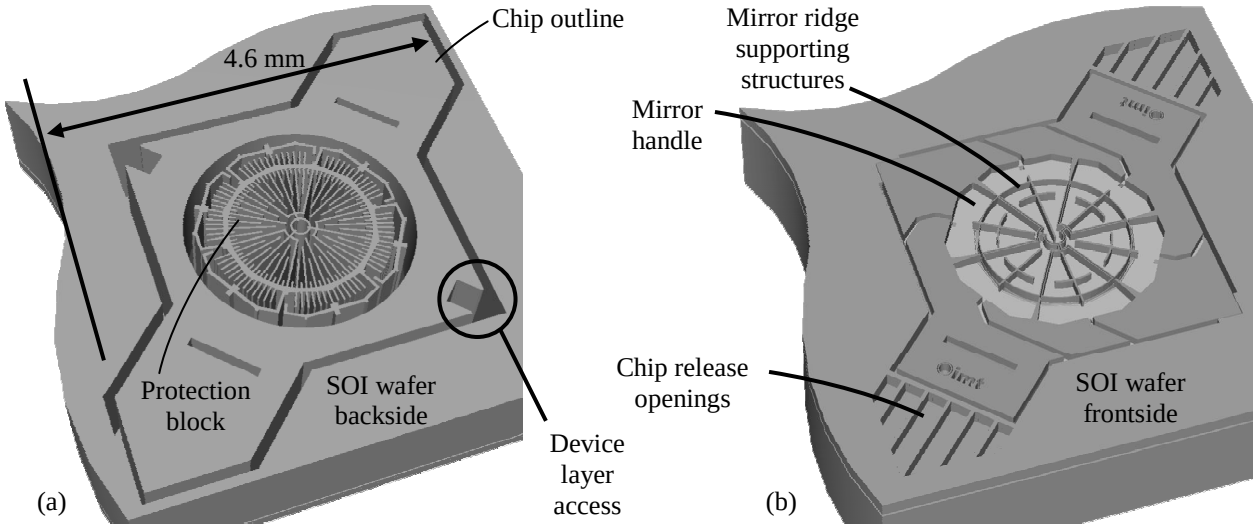


Fig. 3. (a) The pattern on the backside of the SOI wafer. The chip outline can already be seen. The chip dimension is within $4.6\times4.6\ mm^2$. (b) Two height steps on the frontside with a delay mask process gives more flexible suspensions and thinner mirrors with less weight and inertia while maintaining a frame height for the chip.

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are ready for release, for which we custom built a HF vapor phase etching system similar to the setup described by Anguita et al.[15]. The corresponding frontside appearance of the wafer is rendered in Fig. 3b.
The chips are released based on the process proposed by Overstolz[16]. The wafer is placed in contact with a heated chuck with frontside facing down over a beaker of 50% HF solution. The embedded oxide will be under-etched anhydrously to release the mirrors. The wafer is then flipped to have the backside facing down until all protection blocks are dropped by the gravity effect as illustrated in Fig. 4a. Afterwards the wafer is reversed for the last time until all chips are released. The grid structures on the frontside of the wafer provide safety nets to prevent the chips from falling into the HF solution. Slight tapping might be necessary to detach the chips from the wafer, which can be lifted to separate from the chip as illustrated in Fig. 4b. To prevent excessive liquid condensation and stiction during the vapor phase HF release, the wafer temperature must be elevated between 30°C to 34°C to etch directly exposed oxide at about 4 μm/hr. We also fabricate using the same process 8-bit and 16-bit devices with 12 and 24 mirror sectors, respectively. Before assembly, 700 Å gold is deposited on the chips as reflective material with 100 Å titanium as the intermediate adhesive layer.
For the electrode wafer, a shallow tub is needed for spacing to allow vertical displacement of the ridge structure when a mirror is tilted. A quartz wafer is photolithographically patterned and immersed in BHF to etch 10 μm-deep tubs as illustrated in Fig. 4c. After aluminum is deposited and patterned as electrodes, the quartz wafer is diced.
An alignment setup with a long working distance microscope is built to assemble the quartz electrode chip to the device chip, which is held in place to a rotation chuck by slight vacuum suction. The quartz chip is clamped by a pair of tweezers mounted to a XYZ table. Electrode wires are visually aligned as illustrated in Fig. 4d via the transparent quartz chips to the electrode routing tunnels on the device chip. The horizontal clearance between an electrode wire and each side of a routing tunnel is 15 μm. Once acceptable alignment is reached, the quartz chip is pressed against the device chip to ensure no relative motion. A tiny droplet of UV glue can be applied at the corners where the two chips overlap. Due to the capillary action, the glue will run through the gap into the filling area. The cliff where the 15 μm-high frontside device layer meets the backside handle layer platform interface can also be a glue stop to temporarily prevent excessive glue from running into the mirror cavity. Once UV light is shined to cure the glue, conductive adhesive can be applied to i) electrically connect the device layer access corners (see Fig. 3a) to the grounding wirepads as illustrated in Fig. 4e and ii) adhere the assembled chip to a PCB, which is then cured in a 100°C oven for about an hour before wirebonding.

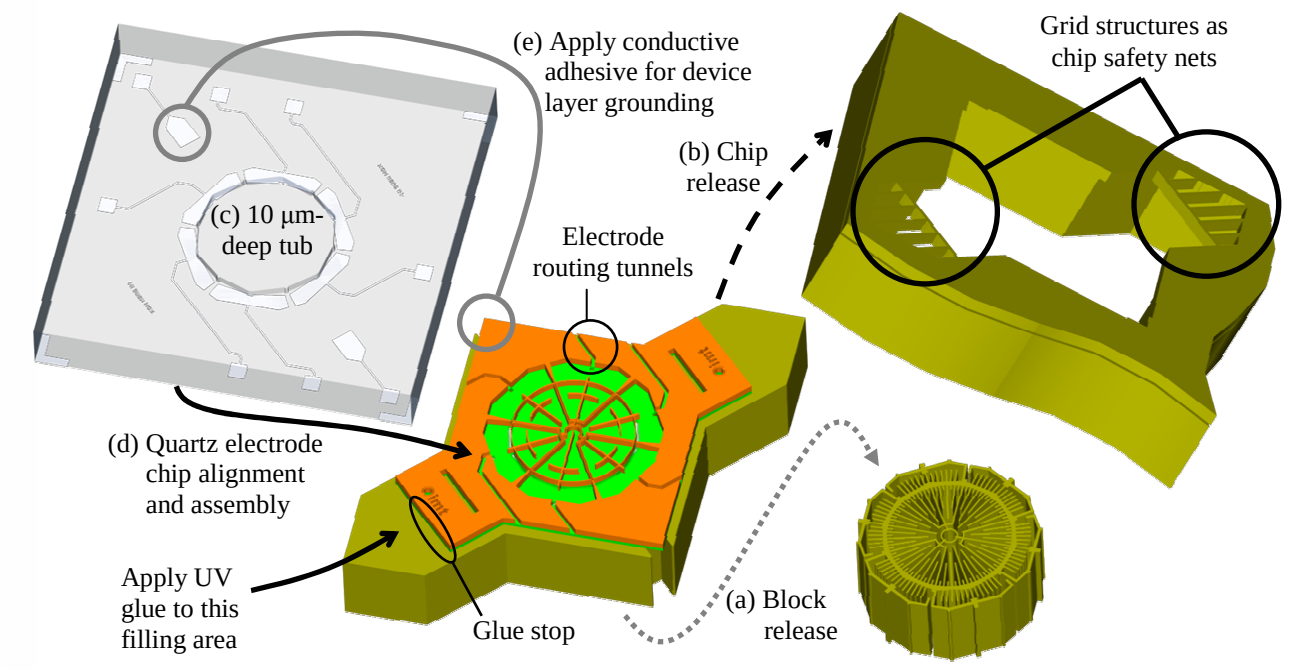


Fig. 4. Illustration of the chip release and assembly. (a) Protection blocks are dropped after releasing the mirros. (b) The wafer can be lifted to leave detached chips on the chuck. (c) Shallow tubs are fabricated on the quartz electrode. (d) Electrode wires are visually aligned to ensure no contact with the routing tunnels. (e) Tiny droplet of UV glue runs into the filling area. UV light is shined to cure the glue. (f) Conductive adhesive is applied to electrically connect the device layer access corners to the grounding wirepads.

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SEM picture of a 16-bit device is shown in Fig. 5. Several of the 24 mirror-bridge-handle components can be clearly seen. Stiction is not as severe as the 1st generation VOA with rectangular mirrors and parallel suspension possibly because the V-shape beams help reduce planar motion. A dropped protection block of an 8-bit device is shown in Fig. 6a. The backside is etched by DRIE for 250 μm and some slight over-etching at the silicon-oxide interface is observed. Apparently some oxide areas do not have full protection from both the frontside and backside, which makes the crack on the oxide film easier to propagate and damages the thin frontside beams. It is necessary to fine-tune the DRIE parameter to achieve a more desirable outcome and increase the yield.

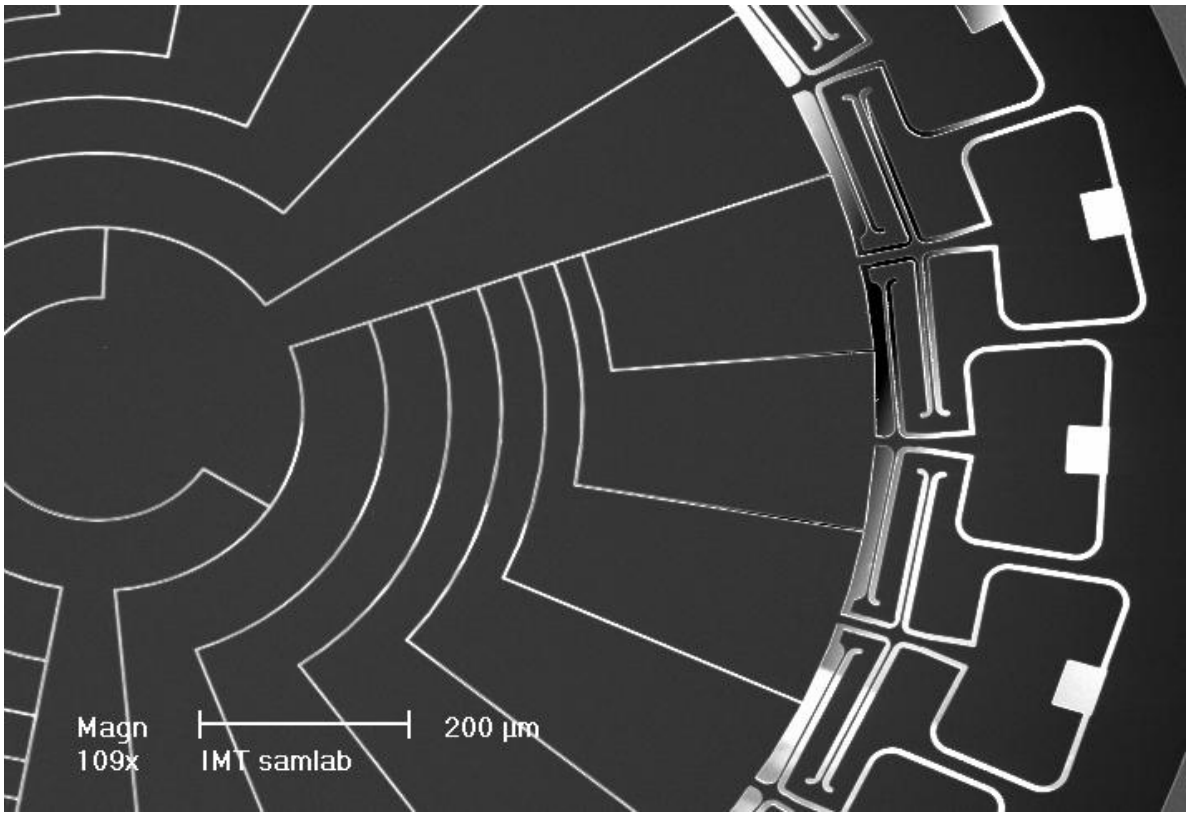


Fig. 5. SEM picture of a 16-bit device with 24 mirror sectors. Gap between adjacent mirror sector is 2 μm. The suspension beams are interdigitated to maximize the length.

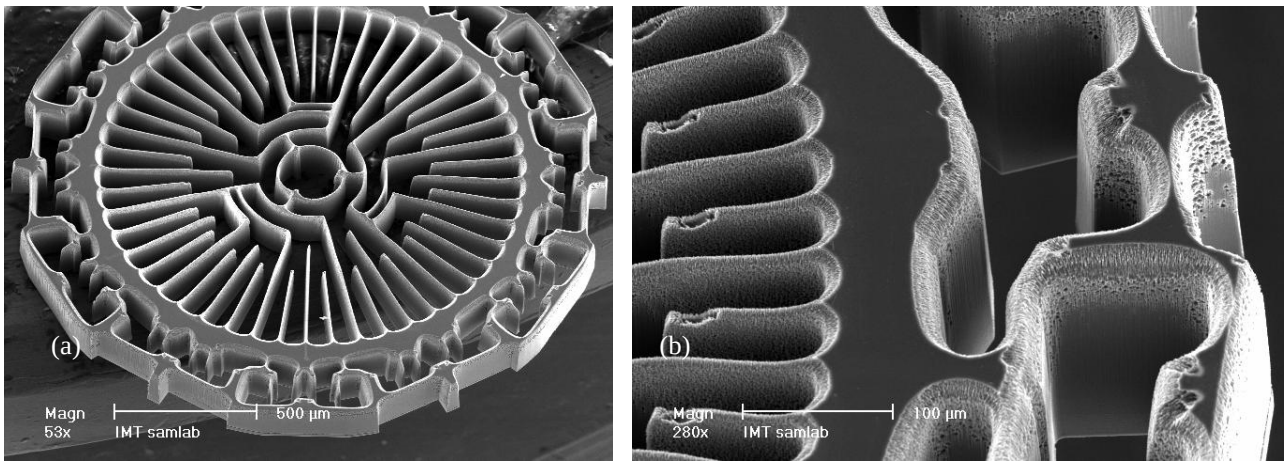


Fig. 6. (a) SEM picture of a dropped protection block from an 8/bit device. (b) Over-etch is observed at the Si-oxide interface.

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4. MEASUREMENT

The mirror flatness of the pre-assembled chips with metallic coatings is measured using the WYKO white light interferometer. A 4th bit mirror sector of a 4-bit device has 4 corners as shown in Fig. 1. A vertical scan using the phase-shift interferometry (PSI) mode is shown in Fig. 7a. The profile with a larger height difference is shown in Fig. 7b with a value at 23.34 nm. A 1st bit mirror sector has 8 corners. Its vertical scan is shown in Fig. 8a. The height variation is 97.17 nm shown in Fig. 8b. Flatness measurement for the 2nd bit mirror sector also with 8 corners from a 4-bit device is also taken. The height variations along the two orthogonal profiles are also about 100 nm. It appears that the flatness of a mirror sector with fewer corners is higher than that with more corners, where more stress concentration causes larger degree of mirror bending.
For the suspension beam of an 8-bit device, the length and the cross section are approximately 345 μm and 6×5 μm^2, respectively. With proper device grounding, a mirror of an 8-bit device can be successfully tilted at about 18 V. Hysteresis is observed that the mirror flips back to the stationary state when the voltage drops below 5 V. For a 16-bit device, the length and the cross section of a suspension beam are about 157 μm and 2×5 μm^2, respectively. The tilting voltage is higher at about 28 V and the restoring voltage is also below 5 V.

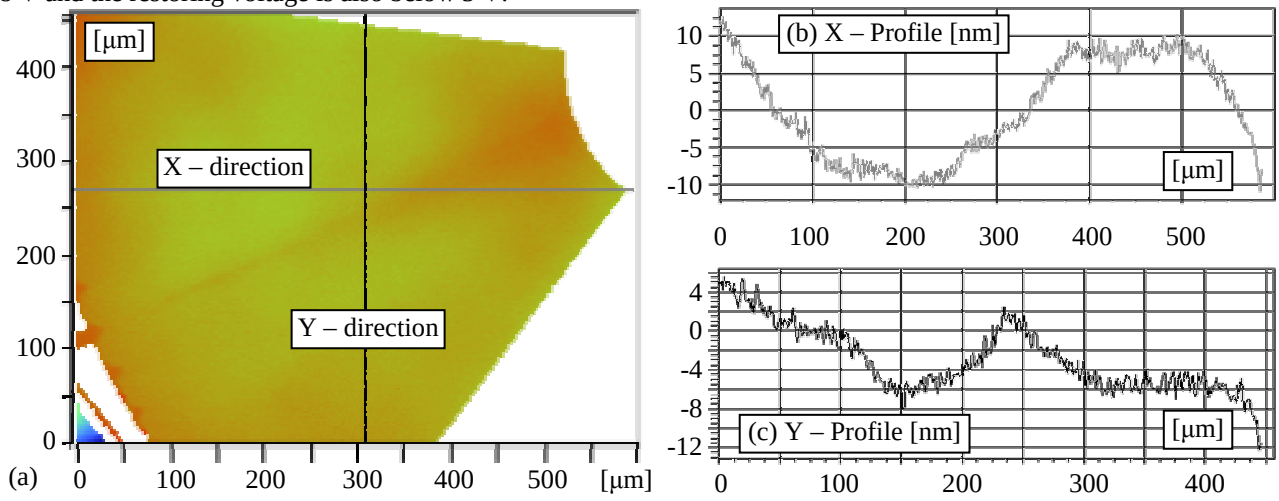


Fig. 7. (a) WYKO interferometric image of the 4th bit of a 4-bit device as viewed from the top. Effective magnification is 10.3X. The underlying ridge structure can be barely observed. The profile along the X -directions is shown in (b). Total height variation is 23.34 nm. The profile along the Y-direction in (c) has a total height variation of 17.78 nm.

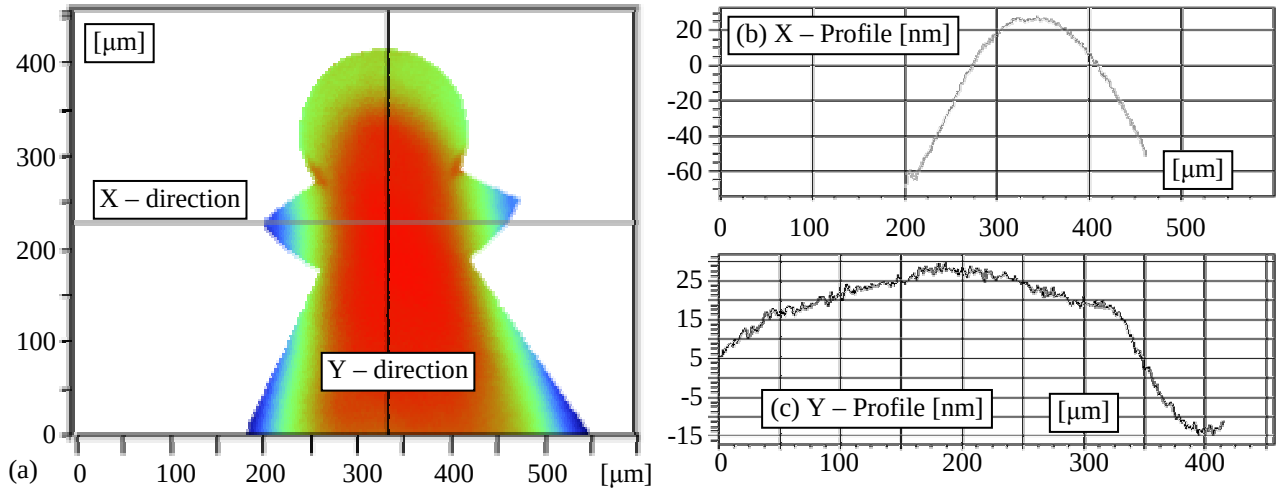


Fig. 8. (a) WYKO interferometric image of the 1st bit of a 4-bit device as viewed from the top. Effective magnification is 10.3X. The profile along the X -directions is shown in (b). Total height variation is 97.17 nm, which corresponds to within the $\lambda/15$ range. The profile along the Y-direction in (c) has a total height variation of 44.56 nm.

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5. DISCUSSION

The DRIE parameters need to be fine-tuned to reduce the backside over-etch at the Si-oxide interface. We believe such improvement would greatly enhance the yield. For the chip release process, attention must be paid when designing the stripe widths at the protection block and the chip release openings as shown in Fig. 3b. The mirrors must be the first group of components to be released; otherwise the dropping protection block would pull along the mirrors and fracture the fragile suspension beams. In addition, for batch processing purpose it is recommended to have the protection blocks dropped before the chips are released. The overlapping area must be carefully designed to ensure a correct timing sequence.

At the lower left corner of Fig. 7a, the image of a suspension beam is also captured. The beam width can be estimated with higher magnification, but measurement on narrow structure is not recommended, especially when the narrow object could be rounded from fabrication process. Taking the interferometric measurement on the topmost layer might not reflect the true width of the beam.

The metallic reflective layer of the rectangular VOA in the previous work was coated also with gold but the adhesive layer was chrome, which is known to cause stress and noticeable mirror curvature difference before and after the coating. Titanium is selected to be the replacement and shows good conformability.

Some mirrors are occasionally tilted even when no voltage is applied. Possible cause is residual charge build up at the non-conductive quartz surface. Proper grounding is therefore a primary requirement to operate the device in a satisfactory manner. Continuation of voltage increase after tilting would cause the entire mirror-bridge-handle component to snap down but no beam facture is observed. The cross-talk effect on a target mirror is not noticeable when the same driving voltage is applied to an adjacent electrode.

6. CONCLUSION

The 4-bit, 8-bit, and 16-bit circular digital variable optical attenuator (VOA) are designed and successfully fabricated based on the SOI technology, delay mask process, and the HF vapor phase etcher. Compared to the rectangular VOA in previous work, each mirror sector is actuated at the handle and suspended at a narrow bridge structure. These features bring individual mirror flatness of the 4-bit device to the $\lambda/15$ range even after metallic reflective coatings. The current combination of 100 Å titanium intermediate adhesive layer and 700 Å gold layer gives acceptably low curvature influence and reasonably good reflectivity. Large electrode and its long distance from the suspension pivot create an effective leverage which cause 2.8° mirror tilting at below 18 V for a 8-bit device and below 28 V for a 16-bit device, respectively. Further characterizations will be conducted.

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