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Frontiers of Cu Electrodeposition and Electroless Plating for on-chip Interconnects.

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1. Introduction

In the electronics industry interconnect is defined as a conductive connection between two or more circuit elements. It interconnects elements (transistor, resistors, etc.) on an integrated circuit or components on a printed circuit board. The main function of the interconnect is to contact the junctions and gates between device cells and input/output (I/O) signal pads. These functions require specific material properties. For performance or speed, the metallization structure should have low resistance and capacitance. For reliability, it is important to have the capability of carrying high current density, stability against thermal annealing, resistance against corrosion and good mechanical properties.

Over the past 40 years the continuous improvements in microcircuit density and performance predicted by Moore's Law has led to reduced interconnect dimensions. Until the mid 1990's Al interconnect was sufficient for VLSI circuit processing [1]. Further developments in miniaturization of IC interconnect required a more conductive material than Al to minimise the RC (resistance-capacitance) delay which is in effect a time-delay between the input and output for a signal or potential applied to a circuit. When coupled with the poor resistance to electromigration (transport of material caused by the gradual movement of the ions in a conductor due to the momentum transfer between conducting electrons and diffusing metal atoms) and poor mechanical properties for application in ultra-large-scale integrated (ULSI) circuits it was clear that an alternative to Al was required [2].

Only three metals, Ag, Au and Cu have lower resistivity than Al. For practical applications it is clear that using Cu rather than Ag or Au is more realistic. The resistivity of Cu is 1.67 μΩ cm, about 40% lower than Al, which when coupled with the new low k dielectrics introduced for the processing led to significant improvement in the RC delay. Cu also has advantages of higher melting point 1083ºC by comparison with 660ºC for Al and higher barrier to migration of an atom from its lattice position in a crystal, Al (1.4 eV) and Cu (2.2 eV). Despite these advantages Cu had not been used for on-chip interconnect to that point because of device reliability concerns and processing difficulties. It can diffuse rapidly through SiO_2 in the presence of an electric field [3], decreasing transistor reliability. It also oxidises significantly at low temperatures but unlike Al it does not self-passivate [4]. However, one of the largest obstacles to its introduction was the fact that it cannot be etched readily in plasma. Therefore an entirely new approach to interconnect processing had to be developed.

In 1997 IBM developed the electrodeposition technique for Cu metallization [5]. The required breakthrough was damascene plating in which the dielectric is first patterned before infilling with the Cu conductor, which enabled Cu electrodeposition to be utilised for on-chip interconnect. It has since become the standard method for Cu metallization with demonstrated wafer scale uniformity, high aspect ratio gap filling capability and low temperature processing. Semiconductor manufacturers have gradually adopted the electroplating technique for Cu interconnect deposition in electronic devices and continue to work on miniaturization of device and feature sizes. In the dual damascene technique, lines

and vias can be filled with electrodeposited Cu at the same time. Fig. 1 shows a schematic diagram of via filling with Cu and the requirement to achieve ‘superfilling‘ or ‘bottom-up fill‘ (BUF) deposition. This is achieved through the use of suitable additives in the plating bath [6-8], and is required because subconformal or conformal plating would lead to voids or seams in the Cu.

The additives typically required to achieve this superfilling are a suppressor such as polyethylene glycol (PEG) which in conjunction with chloride ion and an accelerator such as sulphopropyl disulphide (SPS) result in enhanced deposition within the feature while minimising overgrowth or a pinch off of the feature at the top surface. Detailed examinations of the mode of operation of the additives (discussed below in section 3.2.1) and their interactions have been performed and has facilitated remarkable and predictable control of the deposition in sub 100 nm dimensions.

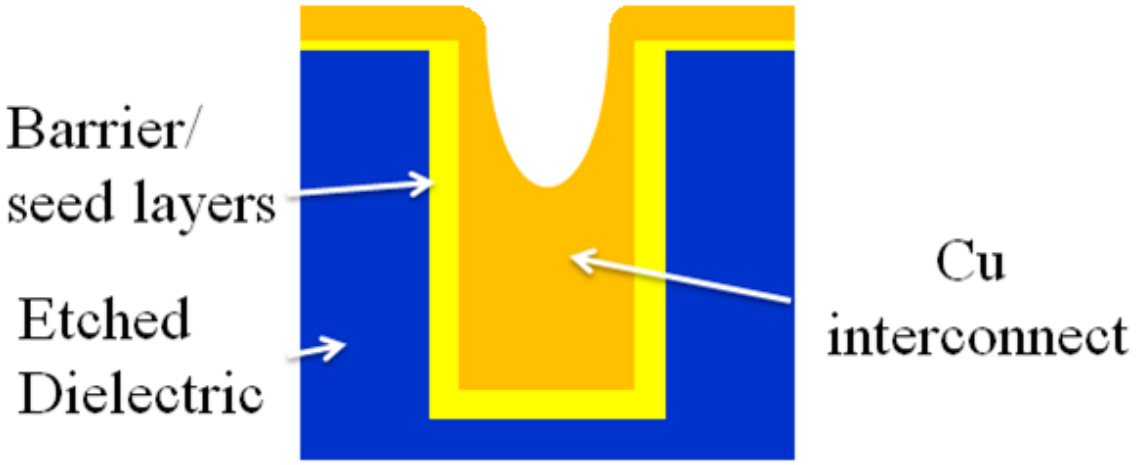


Fig. 1. Cross section schematic of interconnect trench or via showing ‘superfilling’ or ‘bottom-up filling’ of features through the use of specific plating bath additives for optimum void-free profile evolution in damascene processing [5].

Improved barrier layers were also required and introduced with Cu in the damascene process. Refractory metals or their alloys such as TaN deposited by a standard physical vapour deposition (PVD) process have been sufficient to date. This layer covers the entire surface to act as a barrier to Cu diffusion. The low conductivity of TaN has required Cu seed layers for the subsequent electrodeposition, and these have also been processed by PVD [9]. However, PVD suffers from poor step coverage in deep sub-micrometer vias and trenches. An alternative process, chemical vapour deposition (CVD) remains a candidate for Cu deposition but requires the use of combustible precursors which has limited the implementation of Cu deposition by CVD [10] in IC processing to date. Once the barrier layer is in place the active interconnect material can also be deposited by CVD and Moffat et al have shown that a similar superfilling can be achieved using this approach [11]. For future device architectures, particularly at the lower metal layers of the interconnect, new processing routes must be established with even greater control over nucleation and layer growth to achieve the material dimensions required. This may necessitate a combination of new processing routes involving vacuum deposition techniques and wet chemistry processing.

2. Required future dimensions.

The International Technology Roadmap for Semiconductors (ITRS) lists the dimensions for interconnect processing required over the next number of d**e**vice generations [12]. Fig. 2 has an illustrative cross-section adapted from the ITRS of a typical microprocessor where the interconnect of different lines and vias between two adjacent layers are filled with Cu. The metal 1 pitch is also illustrated.

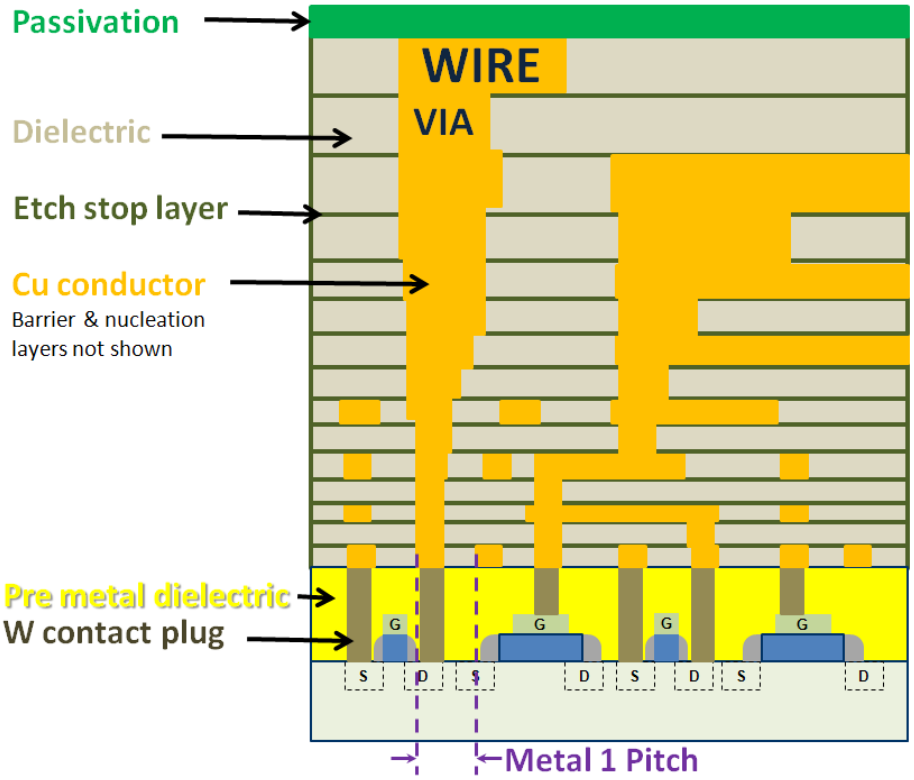


Fig. 2. Typical cross section illustrating hierarchical scaling methodology [adapted from the ITRS technology roadmap, 2011 update for interconnect].

The microprocessor metal 1 ½ pitch dimension in future device generations requirements are summarised in Table 1. It is clear that manufacturable processes are not yet known for metal 1 interconnect and barrier layer material past 2014 (highlighted in red squares). By 2020 IC interconnect at the smallest dimension will be 12 nm with an expected aspect ratio of 2 and barrier layer thickness of only 1.1 nm. The interconnect issues require urgent attention to enable further Cu scaling. This requires the combined assessment of novel barrier and seed layer processing and the active device interconnect material deposition.

Year of production	2014	2016	2018	2020	2022	2024	2026
Metal 1 (1/2 pitch) / nm	24	**19**	**15**	**12**	**10**	**8**	**6**
Barrier cladding thickness for metal 1 / nm	2.1	**1.7**	**1.3**	**1.1**	**0.9**	**0.7**	**0.5**

Table 1. Metal 1 (1/2 pitch) dimensions and barrier cladding thickness for metal 1 [ITRS technology roadmap, 2011 update for interconnect].

As the feature sizes decrease and consequently the operating currents increase, electromigration becomes a serious issue once more [13], particularly where high direct current densities are used, such as in high performance processors. It has been reported that Cu vias are the weak link in the interconnect metallization [14]. The Cu via connects directly to the Cu metal below. Consequently, if a void forms in the Cu underneath the via, there is no redundant layer available for current shunting. This is the primary cause of early failure in Cu interconnects. For the 22 nm technology node or below, the interconnect metal should have current carrying capability of more than 10^7 A/cm^2 to overcome the electromigration issue which is at the limit of pure Cu capability.

3. New processing to extend Cu

The decrease in cross sectional area of the interconnect pushes the current density of the Cu wire towards the electromigration limit. To extend the use of Cu at the smaller dimensions a decrease is required in the material stack that functions as barrier layer, in the adhesion or liner and/or in the conductive metal seed layer. This can be achieved through the use of more conductive and better adhered barrier layers and seed layers eventually possibly being thinned to a single plateable barrier. A graphical representation of the influence of the thickness of the barrier/adhesion/conductor seed stack on the percentage of available active Cu conductor cross sectional area is shown in Fig. 3 for a simple 1:1 aspect ratio. It can be seen that a very significant proportion of the via or line will be consumed by low conductivity barrier stack materials unless the materials function can be optimised and decreased in dimension.

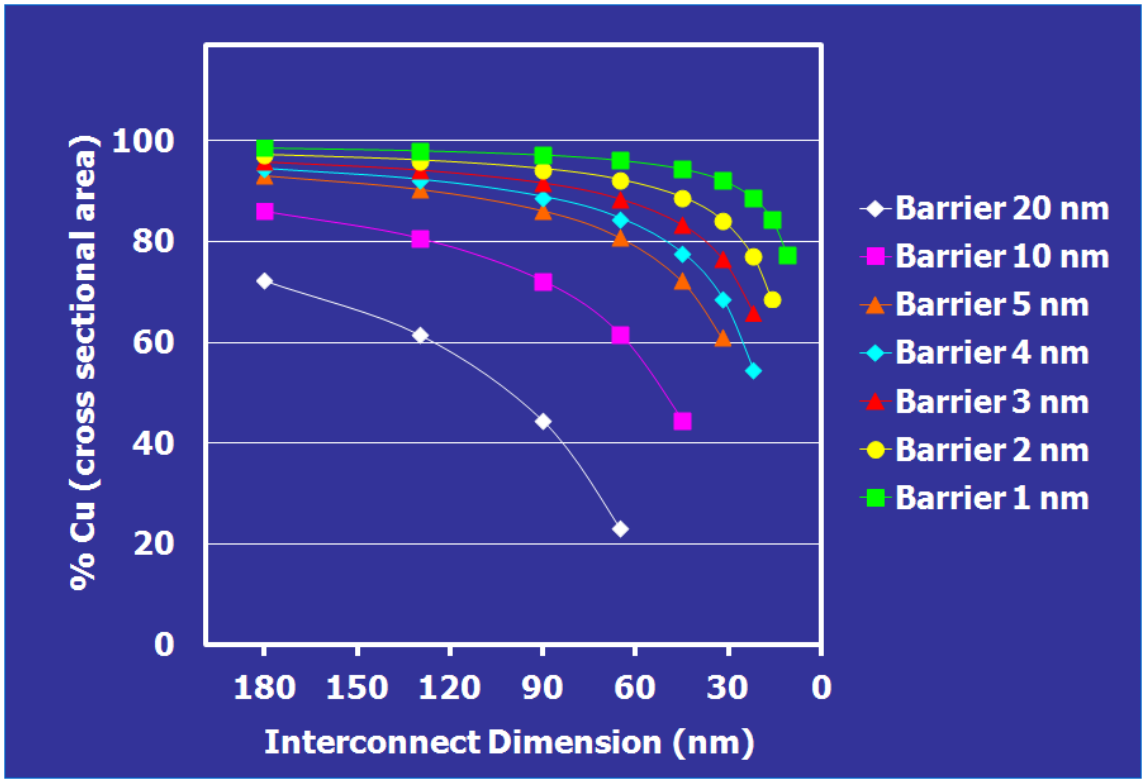


Fig. 3. The effect of thinning barrier/seed layer stacks for Cu interconnect based on the cross sectional area of a 1:1 aspect ratio feature at decreasing interconnect dimensions.

3.1. Barrier layer studies

Two potential solutions to the issue of decreasing the barrier/seed layer dimension have received the most attention to date. One is the use of higher conductivity 'plateable' barriers. The other is the use of self-forming barriers through the deposition of a Cu based alloy. When the alloy is deposited, a stable nanoscale barrier forms between the alloying element and the low-k dielectric material upon heat treatment.

3.1.1. Plateable barriers

Potential plateable barriers must fulfil a number of criteria to be considered as replacements for the current TaN barrier layer for Cu. The material must

- function as a barrier to Cu diffusion
- form a coherent, conformal nanoscale deposit
- have significantly better electronic conductivity to enable nm scale layer use at 300 mm and the future 450 mm diameter wafers without terminal effects [15] (where non uniform Cu electrodeposition occurs across the wafer)

Lower conductivity plating solutions have also been introduced to minimise variation across the wafer by counteracting the resistive seed. The lower acid content of such solutions also enhances the Cu seed layer stability by reducing corrosion while improving the Cu solubility. Candidate barrier/seed materials are listed according to bulk resistivity in Table 2.

Metal	**Bulk resistivity / Micro ohm cm**
Rh	4.3
Ir	4.7
W	5.0
Co	6.0
Ni	6.8
Ru	7.1
Os	8.1
Pt	10.6
Ta	13.5
Ti	40
Mn	144
TaN	180

Table 2. Bulk resistivity of candidate materials for Cu seed layers.

The materials must also

- be non-oxidising
- be competitive in cost
- be scalable to 1.7 nm by 2016, 1.1 nm by 2020 and 0.5 nm by 2026 in accordance with the ITRS roadmap

Amorphous materials have in general been shown to function well as barrier layer materials and the introduction of nitrides or alloying elements has also been considered although high conductivity remains a concern when using an alloy or nitride.

Meeting each of the conditions listed above is a significant challenge and has resulted in the assessment of new and combined deposition techniques such as atomic layer deposition for the ultimate control over the barrier layer dimension. In atomic layer deposition a cyclical process of metal precursor and reactant introduction to a vacuum chamber is performed to deposit materials atomically layer by layer. This is readily achieved for materials such as Al_2O_3 where first the Al precursor is introduced before the second active material pulse of water terminates the deposited Al with oxygen leading to a non catalytic surface for the next phase of deposition [16]. This process encourages the completion of the first atomic layer and minimises island or 3D growth. In the deposition of 'plateable' barrier layer metals the first pulse deposits material that is by design maintained conducting which leads to difficulties with the second phase of the process in which identical material is reacted on the deposit. This can lead to a catalytic process and the growth of islands or non-continuous layers.

Detailed studies of Ru deposition demonstrate many of the challenges with the introduction of a plateable barrier. It can be deposited by PVD, CVD or ALD. However, as a pure material it generally deposits in a columnar arrangement with grain boundaries through which the Cu can readily diffuse and is thus a poor barrier layer material. It also experiences oxidation which requires additional processing prior to Cu nucleation and growth in subsequent stack depositions. To alleviate some of the issues multilayer solutions have been proposed such as layering Ru with TaN [17], the inclusion of phosphorus [18], nitrogen, boron and/or carbon [19] or forming alloys such as with tungsten [20]. Binary barrier layers prevent the columnar deposit while only marginally impacting the conductivity. Some of these layers have demonstrated sufficient barrier layer capability at 5 nm when deposited by PVD or CVD. Investigations will continue in this area targeting long term barrier functionality of the layers, which would be deposited preferably through novel ALD processing capable of scaling the plateable seed layer to the dimensions that will be required for future device generations. The improved barrier materials may also be integrated further up the metal stack as improvements in the lower metal stack combinations are introduced.

3.1.2. Self forming barriers

An alternative approach to future barrier layer processing is the use of self-forming barriers [21]. To realise a self-forming barrier, the alloying element must be in a simple solid solution phase with Cu. Elements that form intermetallics (such as Al, Mg, Sn and Ti) tend to remain in the Cu and result in increased resistivity. The diffusivity of the alloying element must also be faster than the self-diffusivity of Cu, so that the alloying element preferentially migrates to the dielectric interface. Ta, W and Mo which are slow diffusing cannot form a barrier layer before significant diffusion of Cu to the dielectric. The third requirement is that the standard free energy of oxide formation should be sufficiently large and negative but not much larger than SiO_2. The oxide formation energy provides a driving force for the element to migrate to the interface and ensures that SiO_2 is not strongly reduced. The activity coefficient of the element in a Cu solid solution should be close to or larger than unity. Elements of this type can be removed easily out of the Cu film, leading to a substantial decrease of resistivity.

Manganese has been shown to fulfil these criteria forming $MnSi_xO_y$ at the interface with the dielectric material. The manganese self forming barrier process is being investigated to more fully understand the mechanism and potential for use in future generations. Other issues being assessed are the scalability of the process, the uniformity, the barrier layer functionality with decreasing thickness and the interaction with current and future dielectric materials.

3.1.3. Self aligned electroless barrier/capping layers for on-chip interconnect.

Electroless processing has already shown significant potential for IC interconnect applications in self aligned capping layer deposition on Cu. Grain boundaries were the fastest diffusion path for electromigration in Al (activation energy 0.6 eV for grain boundary diffusion and 1.0 eV for interface diffusion). On the other hand, a metal/barrier layer interface is the fastest diffusion path for Cu (activation energy 1.2 eV for grain boundary diffusion and 0.7 eV for interface diffusion) [22, 23]. The interface electromigration mechanism placed a different focus for reliability improvement with Cu interconnect by comparison with the methods traditionally utilised for Al. In damascene processing overdeposited Cu is removed by chemical mechanical polishing (CMP). The CMP produced top Cu surface is the fast Cu diffusion path which needs to be tightly capped. A nonconductive barrier layer is generally applied as the cap layer (e.g. silicon nitride, silicon carbide, nitride silicon carbide etc) to cover the Cu line top surface. However, there are some issues with using dielectric caps to passivate Cu. As devices become smaller, the current density through the interconnect increases leading to the requirement for better electromigration resistance. The dielectric cap generally also has a higher dielectric constant than the interlevel dielectric, resulting in an increase in line-to-line capacitance. Improved Cu electromigration resistance has been reported for Cu lines protected with thin conductive surface capping layers of self-aligned electrolessly deposited CoWP or CoSnP [24, 25].

3.2. Electroless on-chip interconnect materials deposition.

Electroless plating has also been investigated as a means to deposit Cu for ULSI applications. Initial studies indicated that sub micron features could be filled with electroless Cu from formaldehyde solutions with typical electroless Cu additives such as EDTA and wetting agents to remove hydrogen gas during deposition [26, 27]. Alternative reducing agents have also been investigated such as glyoxylic acid [28, 29] and dimethyl amine borane [30]. Void free deposits were generally achieved although in the larger dimension features a more conformal deposit was observed than the superconformal deposits required for current and future device generations. An example of conformal deposition in a 0.36 μm trench is shown below in figure 4 for electroless Cu deposited on TaN from a DMAB based bath.

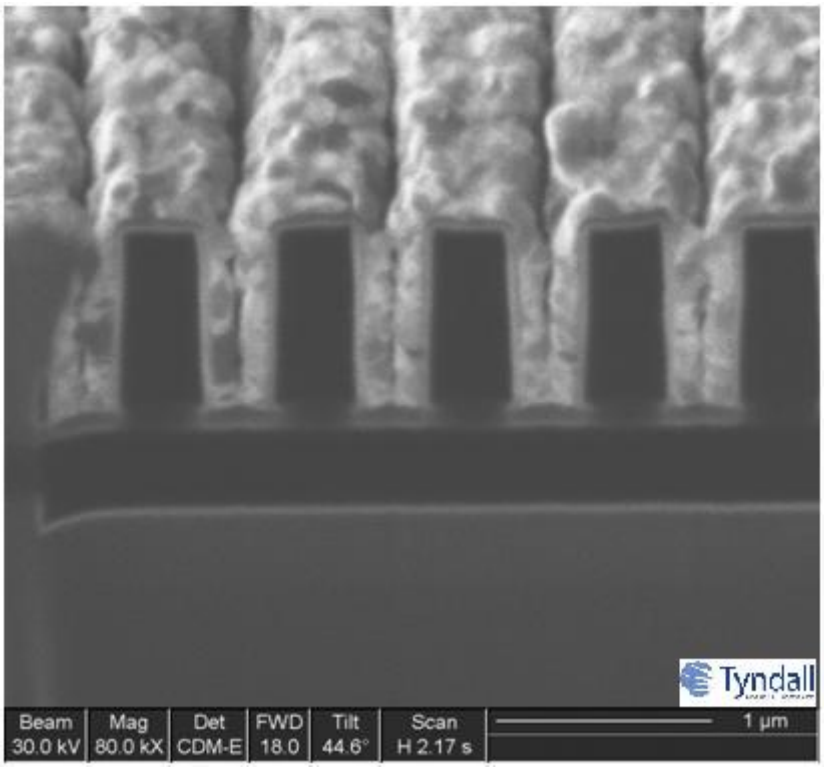


Fig. 4. Conformal electroless Cu from a DMAB bath deposited on TaN (0.36 μm trench).

3.2.1. Superconformal electroless Cu deposition.

The achievement of BUF using similar additives to those used in electrolytic baths was reported by Shingubara et al for 310 nm diameter openings [31]. They found that SPS concentration and PEG with a molecular weight in excess of 800 could be used to encourage BUF even from this very different plating solution when compared to the electrolytic baths. They used glyoxylic acid at pH 12.5 (using tetra methyl ammonium hydroxide to modify pH) and common to all electroless baths no potential was imposed on the substrate. A 1 nm ICB deposited Pd layer was utilised to activate the substrate for electroless Cu deposition. Similar results were achieved in a formaldehyde bath for trench features with 400 nm openings [32] where lower concentrations of SPS (0.5 mg/L) gave BUF through an acceleration of the electroless deposition while for SPS concentrations in excess of 5 mg/L a suppression effect was observed which prevented BUF. PEG was not utilised in [32]. In a subsequent report [33] 2,2 dipyridyl was added to enhance the deposition characteristics and BUF with 2 to 10 mg/L of SPS while above 25 mg/L a suppression of the electroless Cu deposition reaction was observed.

Similar baths using glyoxylic acid, 2,2 dipyridine and sulphur containing organic acids with three different chain lengths were investigated [34]. The researchers concluded that enhanced diffusion of the lower molecular weight mercapto acids to the base of the etched structure promoted BUF. A study which assessed the effect of dilute 1 ppm PEG (MW 4000) on electroless Cu deposition from Glyoxylic acid also revealed BUF which they proposed was promoted within the etched structure (130 nm opening, 350 nm depth onto which a 35 nm PVD Ti/Cu seed layer was deposited) by the differences in PEG concentration that result from the diffusion characteristics and relatively slow diffusion for PEG by comparison with the ten times smaller EDTA complexed Cu ion [35]. Lee et al [36] investigated the influence

of 2-mercapto-5-benzimidazolesulfonic acid on BUF in a formaldehyde electroless Cu bath with 500 nm wide trenches. They also incorporated 2,2 dipyridyl and PEG (MW 8000). Like their other studies the authors found an acceleration effect with low concentration of the sulphur containing additive while at high concentration of the additive a suppressor effect was observed. Yang et al [37] studied the synergistic effects of SPS and PEG (MW 4000) in a formaldehyde bath at pH 12.5 with trench openings of 150 nm and depth of 470 nm onto which Ti (10nm) and Cu (40 nm) were sputtered. They found that inhibition by PEG at the top surface and acceleration by SPS within the trench promoted BUF in the feature sizes studied.

Each of these studies resulted in deposition similar to that observed in sulphuric acid electrolytic Cu deposition baths. The general characteristic of deposition suppression at the top surface by the adsorption of slower diffusing bulky species is common to deposition through both electrolytic and electroless means. In some cases this appears to be assisted by an accelerator reaction within the trench though there is little evidence for the overfilled bump predicted by the curvature enhanced accelerator coverage model [38]. It should also be noticed that while chloride is always present in the electrolytic tests to enhance the functionality of the suppressor molecule, it is not used in the electroless studies. Healy et al [39] showed the influence of chloride on the deposition from a typical strongly acidic sulphate electrolytic bath. At open circuit they suggested the adsorption of a Cu(I)-Cl complex with PEG as a ligand. They proposed that the complex forms a film at the Cu surface that hinders the Cu deposition rate. However, the potential region where Cu is deposited (typically in the range -0.5 to -0.6 V vs. $Hg/HgSO_4$ in such solutions) Cl^- no longer adsorbs and the PEG is adsorbed as a neutral molecule. In a formaldehyde electroless Cu bath operating in alkaline solution (pH 12.5) Cu has been shown to deposit in the region of -0.96 V vs. $Hg/HgSO_4$ [40]. It is also of interest to observe that the rest potential for a Cu electrode in the formaldehyde solution in the absence of added Cu ion is approximately -1.4 V vs. $Hg/HgSO_4$. [41]. Detailed analysis of each of the contributing bath additives and their interaction at the potential and pH of interest has not been performed to date for electroless Cu BUF.

Recent analysis of electroless Cu deposition from borane solutions [42] has shown the importance of designing cells that permit monitoring of the various components in the deposition process. The electroless plating baths are complex solutions typically involving multistep oxidation [43] and metal reduction. To fully describe the reaction mechanism more characterisation is required that will provide data on the individual components and their distributions in full cells. Complicating the analysis is the need to determine reactions at a single substrate. A further complicating factor is that the new phase deposited becomes the active electrode in electroless deposition experiments. It is also important to attempt to standardise the analysis to enable data comparison and mechanistic interpretations. Some of the variables that have hindered the derivation of mechanisms for electroless Cu deposition include bath pH, concentration of active materials, metal salts, additive types and concentration, substrate material, temperature, agitation, dissolved oxygen, impurity species and substrate to solution volume ratio.

3.2.2. Electrochemical deposition for future on chip interconnect.

Electrolytic and electroless deposition have both been shown to fill structures with a required BUF mechanism. To date relatively few studies have been performed on electroless processing in the low nm range. Seed layers based on Pd or Cu have also been used and future interconnect architectures will not facilitate thick seed layers for initial nucleation and

layer growth. Suitably activated electroless Cu deposition could be utilised on current TaN based barrier layers given that a complete seed layer is not required and an electrical terminal effect will not influence the uniformity of the deposit. However, it is still unclear what the limits are for the seed layer required in electroless processing and what the capabilities of BUF are in sub 20 nm features. Plateable barriers based on more conductive materials may also be relevant for electroless processing and provide uniform seed layers for electroless Cu deposition. Electroless Cu for seed layer repair of PVD deposited seeds is currently under investigation and similar investigation may be required for CVD or ALD deposited barrier/seed layers as the achievement of ultrathin coherent conducting layers is not a trivial matter even with these vacuum based high temperature processing routes.

More detailed analysis over the coming years is required to precisely control the electroless processing as has been achieved in the electrolytic case. The ability to then model and predict nucleation and growth mechanisms will greatly benefit future device fabrication. On non conducting barrier layers existing electroless Cu baths require a catalyst deposition and this is typically achieved using a Sn based sensitization step. In a recent study [44] an 18 nm coherent electroless Cu film was deposited from a formaldehyde based solution. The limiting factor proposed for this film thickness was the need to achieve well dispersed nuclei of Pd catalyst on the Sn sensitizer which were in turn on Ta on a TaN barrier layer. In that work Pd particle density was increased (to 6.8×10^{10} particles/cm^2) by the addition of PEG-3400 to the Sn sensitisation solution. They attributed this increase to PEG acting as a surfactant and stabilising agent for the Sn colloids. For electroless processing to be utilised in future on-chip interconnect even greater control of the nucleation density and layer growth dimension will be required, with the fundamental lower limit set by the Cu atom diameter of 0.245 nm.

Common to both electrolytic and electroless deposition for future Cu based IC interconnect is the need to utilise additives to enhance the deposition characteristics. The additives typically employed in damascene plating are based on the interaction between PEG type materials and an accelerator. The size and shape of these additives will become more significant as the feature size for the structure decreases. A typical PEG material used in many of the studies reported has a molecular weight of 3350 based on 75 repeat units of the C-O-C unit. FE-SEM has been used to investigate PEG 7500 [45] in which particles 10 nm in diameter were attributed to PEG. Kondo et al [46] using AFM observed adsorbed PEG (MW 7500) on Cu in the presence of Cl^- with a cone shape where the bottom radius was about 15-25 nm and the height was 2-4 nm. Kelly and West [47] had suggested a collapsed sphere 1.7 nm in diameter based on the molecular weight for PEG 3350 and assuming no voids in the collapsed structure. Alternative polyethers have also been investigated [48] and shown to facilitate void free deposition in high aspect ratio features exhibiting superior BUF capability than PEG 1000 for example.

Molecular dynamics computer simulations can be used to calculate intra- and inter-molecular forces at the nanoscale and determine the structure, dynamics and energetics of macromolecules [49]. The computed structure of PEG (Fig. 5) [50] with MW 3362 (75 CH_2OCH_2 repeat units) shows that an estimated diameter of 1.7 nm [47] for a tightly-folded PEG polymer of MW ~ 3350 is reasonable. The structure was calculated using the NAMD program [51] with the CHARMM force field [52] supplemented by literature data for PEG [53]. Four nanoseconds of room temperature Langevin molecular dynamics was performed in a NVT ensemble (constant number of particles, constant volume and constant temperature) using a two femtosecond time step for dynamics.

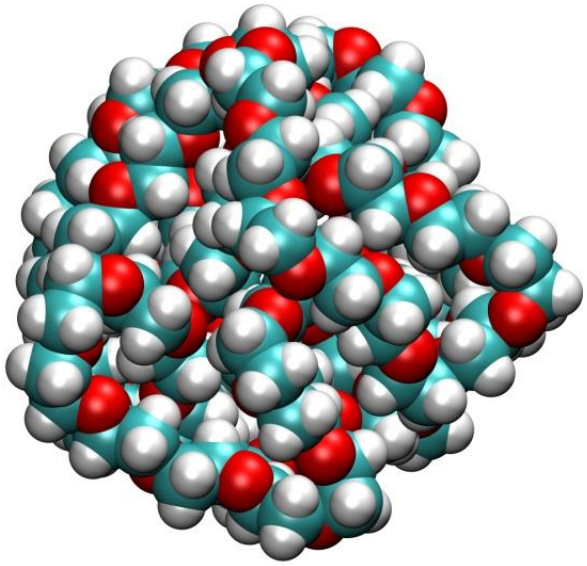


Fig. 5. Computed room temperature structure of $HOCH_2$-$(CH_2OCH_2)_{75}$-CH_2OH (M.W. = 3362). Carbon, oxygen and hydrogen atoms are blue, red and white spheres. The computed PEG structure exhibits a radius of gyration of 0.86 ± 0.01 nm (averaging over 100 structures, sampling every ten picoseconds during the final nanosecond of dynamics), corresponding to a diameter of 1.72 nm.

Such computed properties can be used to better understand and guide experiments in the development of functional nanomaterials for electronics [54-56]. Further models that include the Cu surface and water could be used to determine the size and structure of the polymer in Cu deposition experiments [47], including also the effect of ions [57] on the structure of the PEG (or similar functioning polyethers), to assist with prediction of the viability of materials processing for future electrolytic or electroless on-chip interconnect.

Electrochemical deposition for on-chip interconnect has over the past 15 years inspired many aspects of nanoscale electrochemical processing. The detailed analysis of the electrolytic route has resulted in a continuous scaling that has matched the requirements of the ITRS for sub 100 nm deposition. As the issues of barrier/seed layers and nucleation become more critical electroless deposition must also be considered for future on-chip interconnect applications and combinations with ALD or CVD may be required to deliver the future scaling requirements. Novel electroless plating solutions and detailed electrochemical and microstructural characterisation are required. Computer simulations of bath constituents and interactions will assist greatly in the continued implementation of electrochemical solutions for applied nanotechnology.

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