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Publication date	2025-03-20
Original Citation	Hall, M. L., He, X., Chiu, C.-P., Morrissey, P. E., Gradkowski, K., Jayaram, V., Cheng, F., Hoang, T. T., Bergman, K., O'Brien, P. and Hosseini, K. (2025) 'Innovations in fibre array coupling and integration for high-bandwidth FPGA multichip packages', Proceedings of SPIE, 13372, Optical Interconnects and Packaging 2025, 1337204 (7pp). https://doi.org/10.1117/12.3040471
Type of publication	Conference item;proceedings-article
Link to publisher's version	10.1117/12.3040471
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Innovations in fibre array coupling and integration for high-bandwidth FPGA multichip packages

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ABSTRACT

The FPGA-based hardware accelerator multi-chip packages (MCPs) presented in this study showcase the first example of 168 edge coupled fibers to one side of an FPGA-based package with a small shoreline of 26.5 mm, which will enable co-packaged technology to push towards 50 Tbps of aggregated bandwidth on one side of the MCP.

The presented study examines the mechanical and optical design constraints of a compact edge coupled MCP, consisting of 3 PICs each with 56 optical channels with narrow spacing between, 3 EICs, and an FPGA. Stress relief designs were developed for robust fiber attach to the PIC and the package substrate while minimizing the package size.

The die-attachment of the PIC to the substrate introduces a mechanical warpage (bending) of the PIC, which was investigated along with the subsequent effect on optical coupling during fiber array integration. An automated fiber array unit (FAU) attachment process was developed that provided FAU-to-MCP packaging with repeatable results (-2.21±0.43 dB insertion loss measured across 48 loopbacks after fiber attachment to 24 packages). This process can also be used for rapid indirect PIC warpage measurements, which allowed additional warpage-induced coupling losses to be estimated for channels without loopbacks, so that specified optical channels could be prioritized during assembly. Methods to mitigate for warpage-induced optical coupling losses were also investigated.

The presented automated high channel-count FAU-to-PIC integration procedure and PIC warpage analysis demonstrates a push towards higher-volume manufacturing of co-packaged FPGA multi-chip platforms and higher aggregated bandwidths than previously reported.

Keywords: Photonics packaging, Co-packaging, FPGA, Multi-chip package, Hardware accelerator, Silicon PICs

1. INTRODUCTION

Co-packaged electronic-photonic modules have the potential to match the demands of the exponentially increasing power and bandwidth requirements of high-performance computing and data centres [1]. Electronic integrated circuits (EICs), photonic integrated circuits (PICs) and field-programmable gate arrays (FPGAs) can be integrated into a single multi-chip package (MCP) [2], [3] to create FPGA-based hardware accelerators in data centre and radar applications.

Previous work has focused on multiple EIC chip integration [4] or, in the case of multiple PIC integration, grating couplers as a means of optically interfacing with the package [5]. Integrating multiple ultra-high-bandwidth PICs in an MCP significantly increases the number of optical I/Os while maintaining advantages in wafer-yield associated with smaller chip sizes due to significantly increased MCP edge bandwidth density. The advantages of edge couplers are well known, typically offering higher coupling efficiencies, a broader bandwidth, and polarisation independence when compared to grating couplers [6], [7]. With multiple edge-coupled PICs implemented on a single MCP, it is anticipated that even higher bandwidths can be attained than previously possible with grating couplers, at a lower energy consumption.

The work in this paper examines the mechanical design constraints of a compact edge-coupled FPGA multi-chip package and investigates warpage induced by the die-attachment method to the package substrate. As a proof of concept, an automated fiber array unit (FAU) attachment process is introduced that provides FAU-to-MCP packaging with repeatable results. Although the packaging process development attempts to minimise bending of the PIC during the die-attachment, some level of warpage remains after electronic packaging. The FAU alignment process therefore also measures local PIC warpages indirectly to enable specified optical channels to be prioritised during assembly – an aspect of FAU integration that has not been previously reported.

Optical Interconnects and Packaging 2025, edited by Ray Chen, Henning Schröder,
Proc. of SPIE Vol. 13372, 1337204 · © 2025 SPIE · 0277-786X
doi: 10.1117/12.3040471

2. COMPACT FPGA MULTI-CHIP PACKAGE DESIGN

The optical input/output interface of each PIC consisted of an array of 56 edge couplers at a pitch of 127 µm. There were 4 groups of 12 functional waveguides providing optical connections to the electronics within the FPGA package, and 4 two-channel loopback waveguides for active optical alignment at Channels 1-2, 27-28, 41-42, and 55-56. A section of the PIC (Channels 1-14) is shown in Figure 1, with one loopback (Channels 1-2) and one functional group (Channels 3-14).

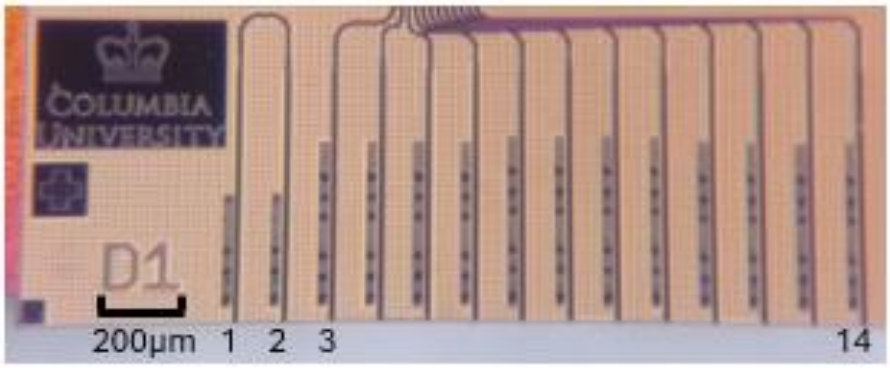


Figure 1: Microscope image of PIC edge coupler layout with loopback channels for optical alignment.

Figure 2 demonstrates three PICs implemented on a single substrate within the MCP. As illustrated in the figure, the PICs are placed in the MCP with minimal spacing between them to maximize the total number of fiber channels for the available MCP shoreline. The FAU design was carefully considered to allow sufficient space for positional adjustment during the optical assembly process.

Ensuring that the package was as compact as possible and compatible with a test socket system meant that the fiber integration process had to be considered alongside the mechanical and thermal design. A new edge-coupling process was developed, which involved directly attaching a glass block to the chip prior to FAU attachment to ensure the total package height was minimised. This approach significantly reduces the package size compared to conventional edge coupling methods while retaining a higher bond strength than direct-to-chip attachment [8].

To further improve the mechanical strength of the fiber-to-MCP bond, a mechanical strain relief (SR) was attached to the PCB substrate. The fiber array ribbon was secured to the strain relief with epoxy after FAU-to-PIC attachment. Numerous SR configurations were tested, and stainless steel was chosen for its high stiffness to prevent flexion of the thin beam feature (0.6 mm). A strong mechanical epoxy was selected to mount the SR to the MCP after strength tests indicated forces of approximately 160 N were required to break the bond.

The integrated heat spreader (IHS) was designed as a separate module to the SR with a thermal break between the IHS and SR. This allowed copper to be used for the IHS, as the higher thermal conductivity provides better thermal control of the system. The copper IHS also protects the electronic and photonic components on the MCP.

Each of the 56-channel FAUs required three 24-channel MPO connectors, as individual FC/APC connectors would have significantly increased the weight and bulk of the overall package. The fiber-to-MPO connector mapping was designed so that all loopback channels were routed to a single MPO connector, simplifying optical power monitoring during packaging.

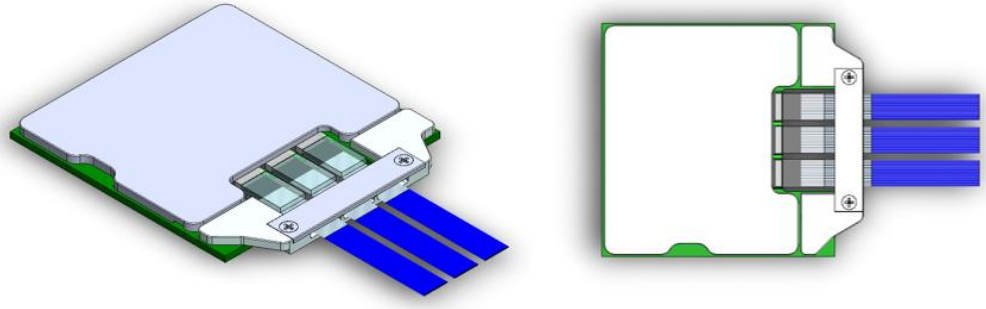


Figure 2: Computer-aided Design (CAD) drawing of the multi-chip package with three fiber arrays attached.

3. OPTICAL FIBER ARRAY TO CHIP ASSEMBLY

A programmable computer-controlled six-axis alignment stage, capable of sub-micron precision, was used for the FAU-to-PIC attachment procedure. Utilising camera systems mounted on the alignment arms, glass block attachment, FAU alignment (passive and active), epoxy dispense, UV curing, and proxy-warpage measurement procedures were largely automated using script-based software and machine vision. An FAU gripped by the machine is shown in Figure 3.

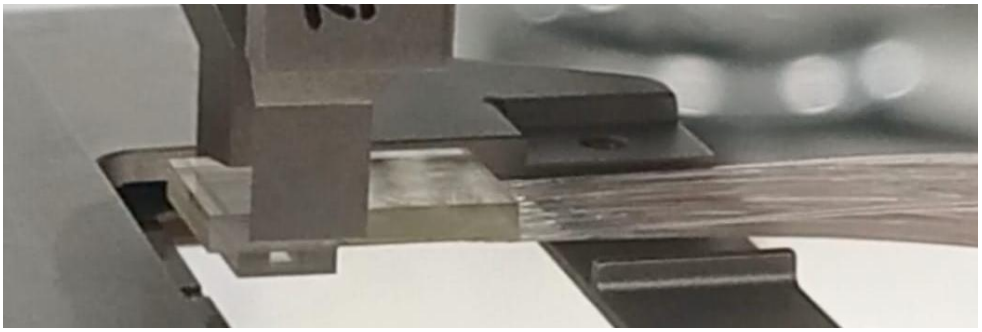


Figure 3: FAU gripped by a 6-axis alignment arm during packaging as it is brought close to the multi-chip package

Figure 4 shows an example dry-alignment tolerance graph with the FAU butt-coupled and aligned to outer loopbacks Ch1-2 and 55-56. The peak coupling for this example was -2.07 dB, with a 1 dB alignment tolerance of ±2.42 µm and ±2.14 µm in the horizontal and vertical directions, respectively.

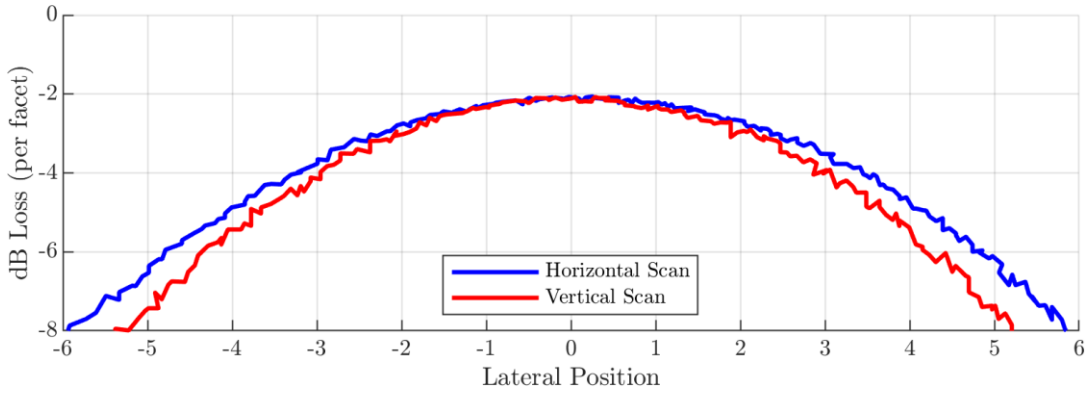


Figure 4: FAU alignment optical loss (per facet) vs lateral distance from optimized optical position.

4. EFFECT OF LOCALISED PIC WARPAGE ON COUPLING EFFICIENCY

As shown in Figure 5a, three PICs are implemented on a single organic substrate. Due to differing coefficients of thermal expansion of the PIC and package materials, warpage is introduced to the components of the package during the high temperature die-attachment process once the package has returned to room temperature. Removing the slope of PICs 1 and 3 due to the global warpage yields a symmetric local warpage of these PICs, although the magnitude is lower than that of the centre PIC 2.

Sub-micron FAU alignment to edge couplers necessitates warpage consideration during optical packaging, as warpage-induced height difference across a PIC can yield significant additional coupling losses between central and outer loopback edge couplers when coupled to an FAU.

PIC warpage was simulated using finite element analysis (FEA) and the normalised results are shown in Figure 5b (y-axis not to scale). The graph demonstrates that the PICs are subject to both global warpage of the PCB and local warpage of the PICs and the global warpage is symmetric about the centre of the package. Considering the outer loopbacks (Ch1-2, Ch55-56) as a zero-reference point, the maximum local warpage of PIC2 according to the FEA results was 4.25 µm.

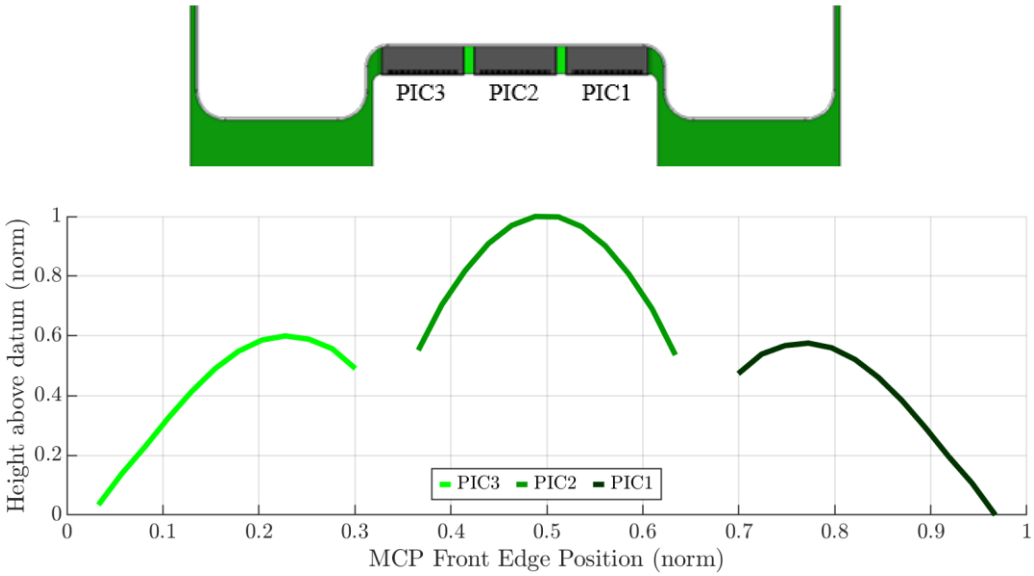


Figure 5: (a) Top-view of MCP. (b) Normalised FEA results indicating global warpage of the PCB substrate and local PIC warpage.

As previously stated, large additional optical losses are associated with a warped chip, so it is essential to determine PIC warpage to direct packaging decisions. These decisions may include prioritising the maximum coupling efficiency of functional waveguides at specific sections of the PIC by aligning to intermediate loopbacks in cases with high warpage. As a result, proxy warpage measurements were used along with tolerance scan results to estimate expected coupling losses for functional waveguides where the optical power could not be directly measured.

The proxy warpage measurements were performed by first aligning the FAU to the outer loopbacks and setting this height as the zero-reference point. The position of the FAU was then vertically scanned to find the height of the optimum coupling of the two centre loopbacks (Ch27-28 and Ch41-42). An example package scan result for PIC2 (centre PIC) is given in Table 1 alongside the FEA results. Although the magnitude is different between the two sets of results, the height ratio of the two centre loopbacks is comparable, implying a similar PIC curvature.

Table 1: Height of central loopbacks above outer loopbacks zero-reference position (Ch1-2, Ch55-56)

	Ch27-28	**Ch41-42**	**Ratio**
FEA warpage	4.25 µm	3.28 µm	1.30
Proxy warpage	3.30 µm	2.49 µm	1.32

Combining this proxy warpage measurement with the tolerance graph in Figure 4, an estimated additional loss of the central loopbacks can be calculated when the FAU is aligned to the outer loopbacks. This is given in Table 2 along with the actual loss measured when the FAU was aligned to loopbacks Ch1-2 and Ch55-56 (i.e. the zero-reference position).

Table 2: Additional coupling loss at the central loopbacks due to warpage

		Ch27-28	**Ch41-42**
Additional coupling loss	**Estimated**	2.31 dB	1.41 dB
	Measured	2.09 dB	1.48 dB

The comparability between the estimated and measured results imply that this proxy-warpage method can be used to estimate losses at edge couplers that cannot be directly measured, such as the functional groups between the loopbacks.

5. FULLY ASSEMBLED MULTI-CHIP PACKAGES

Figure 6 shows a fully packaged compact edge-coupled FPGA multichip package, with three FAUs individually attached to the PICs. In total, 5 full packages (three FAU attachments each) were assembled, as well as 9 single FAU attachment packages, giving optimised coupling results for 48 loopbacks (24 FAU attachments).

The best coupling result was 1.22 dB (per facet). Across all results, the mean optical coupling was -2.21 dB, with a standard deviation of 0.43 dB. Chip warpage, as well as PIC and fiber interface variation may have contributed to the higher coupling efficiencies within the results. Methods to reduce both the mean and standard deviation will be investigated in future work.



Figure 6: A fully packaged edge-coupled FPGA multichip package demonstrating three 56-channel FAUs attached to the MCP

6. MITIGATION STRATEGY FOR REDUCING EFFECT OF LOCALISED CHIP WARPAGE

The most effective intervention to reduce the effect of localized PIC warpage on optical coupling is to significantly reduce the mechanical warpage of the die in the first instance. The reduction in warpage induced by the die-attachment method is the subject of ongoing investigations and future work in the electronic MCP packaging of this project.

However, if warpage cannot be entirely eliminated, it is proposed that the use of pitch-reduced fiber arrays will significantly reduce the impact of warpage on the optical coupling loss of the centre loopback (Ch27-28) with the FAU aligned to the outer loopbacks (Ch1-2, Ch55-56). Using corrosive methods to thin down the fiber cladding, FAU manufacturers can narrow the fiber-to-fiber pitch of the v-groove blocks used in FAU assemblies. For polarization maintaining fiber, the stress rod locations limit the minimum pitch to 82 µm. However, for SMF28, the pitch can be reduced even further, which would increase the impact of the intervention method described in this section.

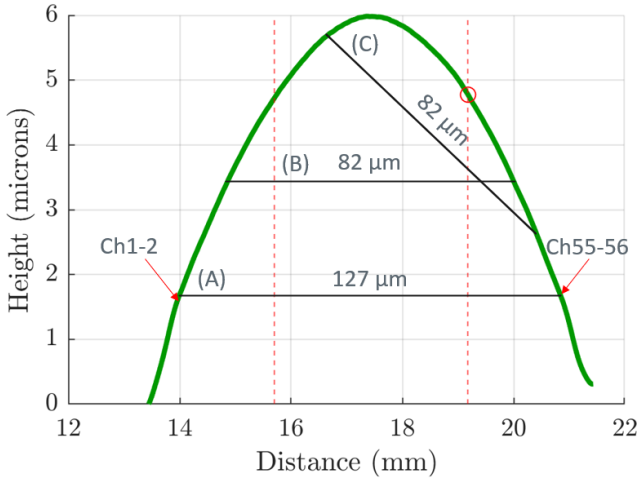


Figure 7: Localised chip warpage of an example centre PIC (PIC 2) with three proposed FAU pitches: (A) 127 µm, (B) 82 µm, and (C) 82 µm off-centre.

Figure 7 shows an example centre PIC (PIC 2) surface measurement with a maximum mechanical chip warpage of 6 µm from the edge of the die. The effective warpage is given as the maximum height of the centre loopback (Ch27-28) above. In this example, for a standard 127 µm pitch fiber array, the effective warpage of this chip was 4.4 µm. As indicated by Table 3, narrowing the pitch from 127 µm to 82 µm reduces the effective warpage to 2.1 µm, reducing the centre loopback loss estimate from 6.08 dB to 2.95 dB per facet (using the data from Figure 4). By moving the couplers off-centre, the effective warpage can be reduced further by moving the fiber array (a straight line) to a part of the warpage curve with a larger local radius (i.e. a flatter part of the curve). The dashed red lines on Figure 7 show the furthest left and right positions that the FAU can be placed for a pitch of 82 µm, and the red circle indicates the position with the lowest effective warpage. Moving the 82 µm pitch FAU off-centre reduces the effective warpage to 1.8 µm, gaining an addition 0.24 dB in coupling per facet (2.71 dB estimated coupling loss) compared to a centrally positioned fiber and coupler array.

Table 3: Effective warpage and central loopback loss estimate for pitch-reduced fiber arrays (*loss estimate assumes 2.21 dB peak)

Fiber-to-fiber Pitch (µm)	Effective warpage from outer loopback position (µm)	Ch28-29 Coupling Loss Estimate*
127	4.4	6.08 dB
82	2.1	2.95 dB
82 (off-centre)	1.8	2.71 dB

7. CONCLUSION

This work presents recent optical packaging innovations and considerations for FAU integration to edge-coupled FPGA multichip packages. Using more automated methods than previously reported and custom low-loss edge couplers, the mean optical loss per facet of the aligned loopbacks was -2.21 dB across 48 loopbacks after packaging, with a standard deviation of 0.43 dB.

Proxy-warpage measurements of the PIC, using centrally located intermediate loopbacks, enable specific optical channels to be prioritised during assembly. The automation was provided as a proof of concept, and further optimisation of this process is required to push co-packaging of FPGA multi-chip platforms towards high-volume.

A mitigation strategy to reduce the effect of localised PIC warpage on optical coupling using pitch-reduced fiber array units has been proposed. By narrowing the fiber-to-fiber pitch from 127 µm to 82 µm, the effective warpage can be reduced by a factor of two, which has a significant impact on the optical coupling of central waveguides.

This work showcases the first MCP with 168 fibers coupled to one side with a small shoreline, which will enable co-package technology to push beyond 10s of Tbps of aggregated bandwidth.

8. ACKNOWLEDGEMENTS

This work was supported in part by the Defence Advanced Research Projects Agency (DARPA) under Common Heterogeneous Integration and IP Reuse Strategies (CHIPS) program contract number R00111830002.

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