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Article

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Understanding the Impact of Annealing on Interface and Border Traps in the $Cr/HfO_2/Al_2O_3/MoS_2$ System

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Abstract Top-gated, few-layer MoS_2 transistors with HfO_2 (6 nm) / Al_2O_3 (3 nm) gate dielectric stacks are fabricated and electrically characterized by capacitance-voltage (C-V) measurements to study electrically active traps (D_{it}) in the vicinity of the Al_2O_3/MoS_2 interface. Devices with low D_{it} and high D_{it} are both observed in C-V characterization, and the impact of H_2/N_2 forming gas (FG) annealing at 300˚C and 400˚C on the D_{it} density and distribution is studied. A 300˚C anneal is able to reduce the D_{it} significantly while the 400˚C anneal increases defects in the gate stack.

Simulation with modeled defects suggests a sizable decrease in D_{it}, half the amount of positive fixed charge in the dielectric, and slightly increased unintentional doping in MoS_2 after a 300˚C anneal. In the as-fabricated devices displaying high D_{it} levels, the energy distribution of the D_{it} located at Al_2O_3/MoS_2 interface is continuous from the conduction band edge of MoS_2 down to 0.13eV - 0.35eV below the conduction band edge. A plausible D_{it} origin in our experiments could come from the unexpected oxygen atoms that fill the sulfur vacancies during the UV-O_3 functionalization treatment. The border trap concentration in Al_2O_3 is the same, both before and after the anneal, suggesting a different origin of the border traps, possibly due to the low-temperature ALD process.

Keywords Molybdenum disulfide (MoS_2), high-k dielectrics, Al_2O_3, interface traps, border traps, capacitance-voltage (C-V).

Introduction

MoS_2 transistors with atomic-layer-deposited (ALD) Al_2O_3 as the dielectric layers[1–7] have been fabricated, which demonstrates that Al_2O_3 is a promising dielectric candidate to boost the electrical performance of MoS_2 transistors due to potentially lower charge trap densities at MoS_2/Al_2O_3 interface.[3] Cho, et al. [3] reported that back-gated MoS_2 transistors with Al_2O_3 dielectric have significantly smaller I-V hysteresis and stress-induced $\Delta V_{T,}$ compared to MoS_2 transistors on SiO_2, which indicates a low density of charge traps at the MoS_2/Al_2O_3 interface. Bolshakov, et al.,[4,5] demonstrated high performance top-gated few-layer MoS_2 transistors fabricated on high-quality Al_2O_3, with an intrinsic mobility $\mu_0 = 145$ cm^2/V·s and a low subthreshold swing SS = 69 mV/dec. Furthermore, dual-gate transistors encapsulated by an Al_2O_3 dielectric have demonstrated a near-

ideal SS of 60 mV/dec,[7] and improved interface quality by reducing the net fixed positive oxide charge,[7] compared to HfO_2/MoS_2 interface. Li, et al. [6] also showed high performance MoS_2 transistors with $HfO_2/Al_2O_3/MoS_2$ top-gate stacks due to low oxide trap density at the interfacial region.

High-k dielectric deposition on Si [8] and III-V materials[9–12] has been widely studied, focusing on the interface analysis and engineering. Recently, capacitance-voltage (C-V) characterization on MoS_2 transistors for HfO_2/MoS_2 interface study has been reported,[13,14] which demonstrates that C-V measurements are a reliable method to understand the properties of interface traps[13] and border traps[14] in high-k/TMD gate stacks. However, there are limited studies focusing on the Al_2O_3/MoS_2 interface using C-V measurement and analysis. Park, et al. [15] reported C-V characteristics of capacitors with Al_2O_3 on 100-200 nm thick MoS_2, extracting a density of interface traps (D_{it}) values of 10^{11} $cm^{-2}eV^{-1}$ to 10^{14} $cm^{-2}eV^{-1}$. Takenaka, et al.,[16] used the Terman method to analyze and compare C-V characterization of MoS_2/SiO_2, MoS_2/HfO_2 and MoS_2/Al_2O_3 interfaces. The extracted D_{it} peak values were reported to be about 1×10^{13} $cm^{-2}eV^{-1}$ regardless of the dielectric selection for back-gated devices on semi-bulk MoS_2.

In this work, we study the interface properties of Cr / HfO_2 (6 nm) / Al_2O_3 (3 nm) / MoS_2 top-gated stacks on transistor structures by C-V characterization, with an UV-O_3 treatment[17,18] as the surface functionalization method. The annealing effect is also studied with the temperatures at 300˚C and 400˚C. Interface traps and border traps in the gate stacks are the focus, which show significantly different behavior after the anneals, compared to HfO_2/MoS_2 gate stacks.[19] Forming gas annealing (FGA, N_2/H_2=95/5) at 300 ˚C is recognized as a promising anneal treatment for Al_2O_3/MoS_2 after gate metal deposition, based on the observation of a drastic D_{it} reduction after the anneal. Physics-based device simulations are performed based on defect modeling,[20–22] which

is designed to investigate the impact of defects on semiconductor device performance. From the simulation results, we are able to understand the energetic and spatial distribution of the interface and border traps observed in the experiments.

Experiments and Simulation Methods

Top-gated MoS_2 field effect transistors (FETs) are fabricated as the test structure in this work. Few-layer (5-15 layers) MoS_2 flakes were mechanically exfoliated from commercial synthetic MoS_2 crystals and transferred onto 270 nm SiO_2 on Si wafers. Using photolithography with a lift-off process, the source and drain of the transistors were formed with Au/Ti (130/20nm) by e-beam evaporation. An ultra-high vacuum anneal[19] was performed to remove contaminants from the MoS_2 surface. A 15-minute in-situ UV-O_3 surface functionalization[17,18] was performed without breaking the vacuum. Al_2O_3 (3nm) and HfO_2 (6nm) were deposited at 200˚C using ALD[17,18] immediately after the treatment, with precursors of TMA/H_2O and TDMA-Hf/H_2O, respectively. E-beam evaporated Au/Cr (130/20nm) was patterned as the transistor gate by lift-off. To study the annealing effects after the initial measurements, a forming gas (FG: N_2/H_2=95/5) anneal at 1 atm was conducted at 300˚C or 400˚C for an hour. Electrical measurements were performed using a Keithley 4200 SCS and an Agilent E4980A LCR meter. Variable frequency C-V measurements were conducted to investigate the high-k gate stacks, with the source and drain of a transistor connected together as the negative electrode, the top gate as the positive electrode, and the wafer substrate floating. A schematic cross section of the MoS_2 FET and a TEM image of a gate stack ($HfO_2/Al_2O_3/MoS_2$) for multi-layer MoS_2 are shown in Fig. 1. The gated area of each transistor is about 10 μm × 10 μm, or larger, which ensures an appropriate signal to noise ratio in proper C-V measurements. The TEM image clearly shows that there is no visible interfacial layer between MoS_2 and Al_2O_3, and both Al_2O_3 and HfO_2 layers are uniform. While the Al_2O_3 dielectric mostly

affects the carrier transport in the MoS_2 channel, the HfO_2 layer ensures a higher dielectric constant and acts as a capping layer during the development step (for photoresist patterning).

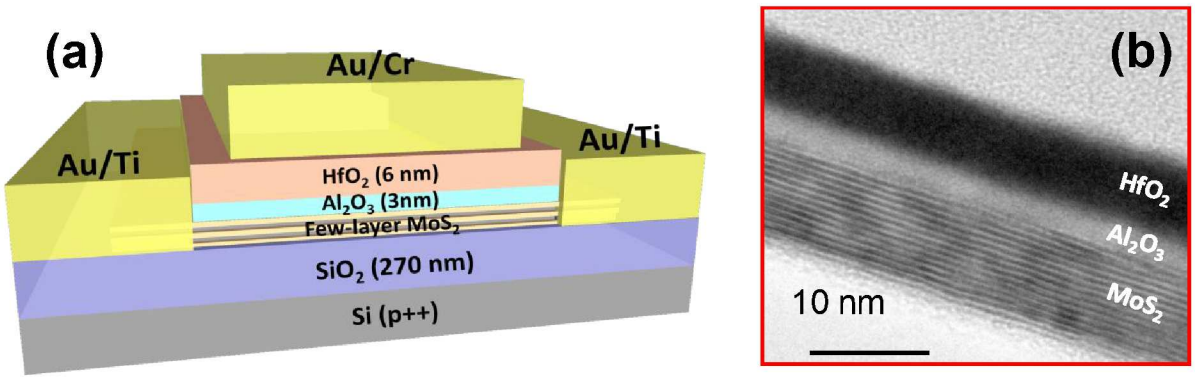


Figure 1. (a) A schematic cross section of the top-gated MoS_2 FET with HfO_2 /Al_2O_3 as the dielectric. Gate stack: Au/Cr/HfO_2/Al_2O_3/MoS_2. (b)Transmission electron microscopic image of the cross section of a transistor gate stack. 3 nm Al_2O_3 and 6 nm HfO_2 layers are uniformly deposited a multi-layer MoS_2 flake, showing no evidence of unintentional interfacial layer on the MoS_2 surface.

Physics-based device simulations are performed based on defect modeling work.[20–22] This tool solves the Poisson and charge continuity equations self-consistently while accounting for a variety of charge carrier transport mechanisms such as drift-diffusion, thermionic emission, direct/FN tunneling[23] and trap-assisted tunneling (TAT) theory[20,21,24]. Charge quantization effects at the interface are also included. The quantum-mechanical, multi-phonon trap-assisted tunneling (TAT) model[20,21,24] implemented in the simulation accounts for the electron-phonon coupling that corresponds to the atomic-scale lattice rearrangement (relaxation) occurring upon charge carrier trapping and emission, which allows estimating the impact of defects on semiconductor device performance. In addition, the simulation of the device electrical response allows extracting key defect properties such as relaxation and thermal ionization energies, which can assist in identifying their atomic structure.

Experimental Results

Typical current-voltage characteristics (i.e., I_{DS}-V_{GS} and I_{DS}-V_{DS} measurements) for devices reported herein are shown in Figs. S2 and S3 demonstrating transistor action and quite low gate leakage current; however, the focus is on C-V frequency dependence (1 kHz to 1 MHz) for electrically active defect detection. An example of an as-fabricated $HfO_2/Al_2O_3/MoS_2$ gate stack FET is plotted in Fig. 2(a). The depletion region shows a frequency dispersive C-V response due to the existence of D_{it} at semiconductor/dielectric interfacial region. The fact that these interface traps respond to lower frequency AC signals while not able to respond to the higher frequency AC signals causes this frequency dispersion. A 300˚C FG anneal was performed on this device, and the C-V characterization after this anneal is shown in Fig. 2(b). The dispersion in the depletion region disappears possibly due to the hydrogen in the FG passivating the interface defects during the anneal. By using the conventional high-low frequency (H-L) method,[13] the D_{it} can be extracted from the C-V measurement [Fig. 2(c)]. The D_{it} peak is 4.5×10^{12} $eV^{-1}cm^{-2}$ before the anneal, and extremely low – lower than the H-L method can accurately determine – after the anneal. However, in the accumulation region, a dispersion is observed, which does not show a significant change after the anneal. This dispersion is likely related to the border trap response[14] – traps in the dielectric layer, which trap/de-trap electrons through a tunneling process during the electrical measurement. In addition, there is a noticeable lateral shift to more positive V_g for the C-V curves after the anneal. This means that the 300˚C FG anneal can significantly reduce the positive charges in the dielectric layers in addition to the D_{it} reduction, as shown before [4,5,14,19].

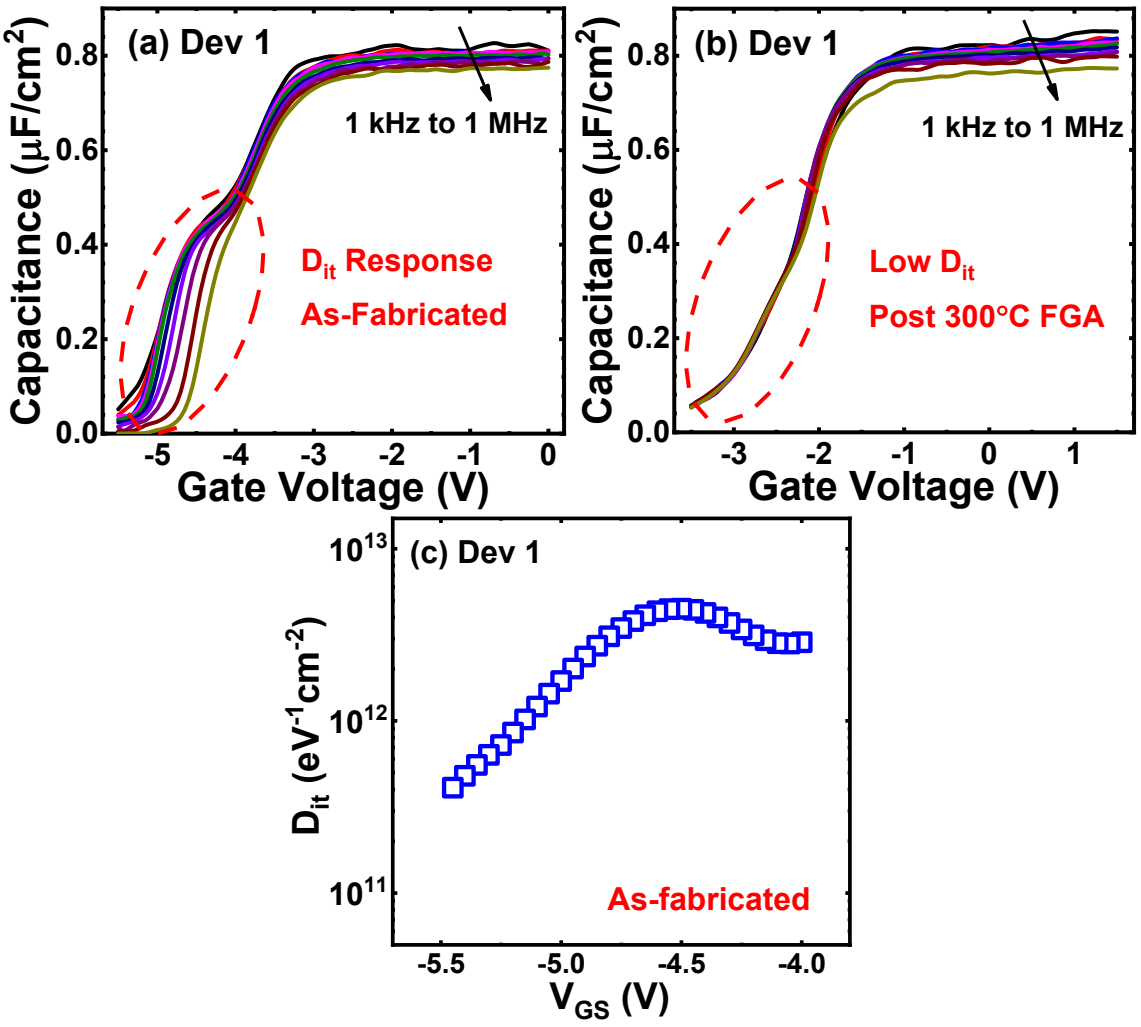


Figure 2. C-V characterization and D_{it} extraction on a $HfO_2/Al_2O_3/MoS_2$ gate stack (1 kHz - 1 MHz) before/after 300˚C FG anneal, (a) before the anneal, showing high interface trap density. (b) after the 300˚C FG anneal, the dispersion disappears, showing a significant reduction in D_{it}. (c) D_{it} extraction by using the high-low frequency method. The D_{it} peak is 4.5×10^{12} $eV^{-1}cm^{-2}$ before the anneal, and extremely low after the anneal (less than 1×10^{9} $eV^{-1}cm^{-2}$).

Another device showing a D_{it} response is annealed at 400˚C in FG (Fig. 3). Contrary to the 300˚C anneal, the 400˚C results in a degraded device, demonstrating significantly increased C-V dispersion. This indicates that the 400˚C anneal creates large numbers of defects at Al_2O_3/MoS_2 interface. D_{it} before and after the anneal is extracted by the multiple-frequency method,[13,25] along with the interface trap time constants (τ_{it}) [shown in Figs. 3(c) and (d)]. Before the anneal, interface

traps with D_{it} values ranging from 1.2×10^{12} to 8.8×10^{12} $eV^{-1}cm^{-2}$ in the depletion region are extracted. After the anneal, the peak D_{it} value increases almost an order of magnitude, to 8.3×10^{13} $eV^{-1}cm^{-2}$. Based on the difference in the extracted τ_{it} values, two groups of interface traps are found from the C-V measurement, similar to what W. Zhu et al.[25] reported previously. The highly dispersed C-V curves (high D_{it}) indicates that a temperature at 400˚C might be too high for an FG anneal of the Al_2O_3/MoS_2 interface.

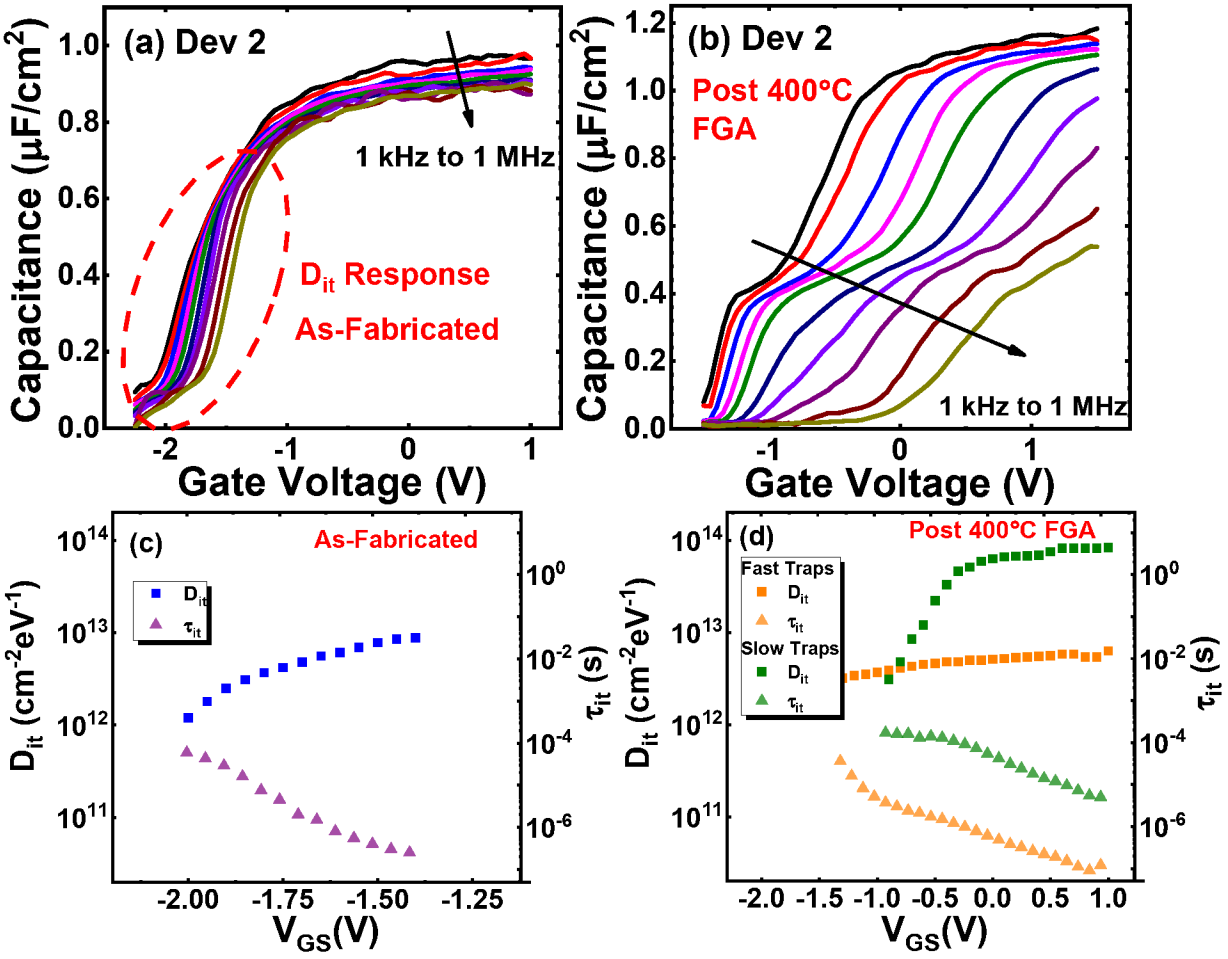


Figure 3. 400˚C FGA effects on a device showing interface trap response. (a) C-V characterization before 400˚C FG anneal. (b) C-V characterization after 400˚C FG anneal for an hour. The large frequency dispersion indicates a significantly higher D_{it} due to the anneal. (c) D_{it} and τ_{it} extraction by using the multiple-frequency method before the anneal. (d) D_{it} and τ_{it} extraction after the anneal.

Additional devices demonstrate a device-to-device variability of the C-V frequency dependence in the depletion region. Results of two devices are shown in Fig. 4, where a moderate D_{it} response is observed in (a) and a low D_{it} response is observed in (b). Similar variation has been reported in the literature.[13,14,16] Meanwhile, all the devices exhibit a similar border trap response[14] in the accumulation region. These suggest that the physical origins of the interface traps and border traps may be different. The interface traps are likely related to some pre-existing non-uniform defects[26,27] on the MoS_2 surface prior to ALD, which causes the device-to-device variation. The dangling bonds, that are generated during the exfoliation process on both the MoS_2 surface and edges, can be one of the possible sources of this variation. In contrast, the border traps are likely a consequence of the low ALD temperature and the deposition rate of the gate dielectric on MoS_2,[14] which has much less variation since the same deposition process occurred on these devices.

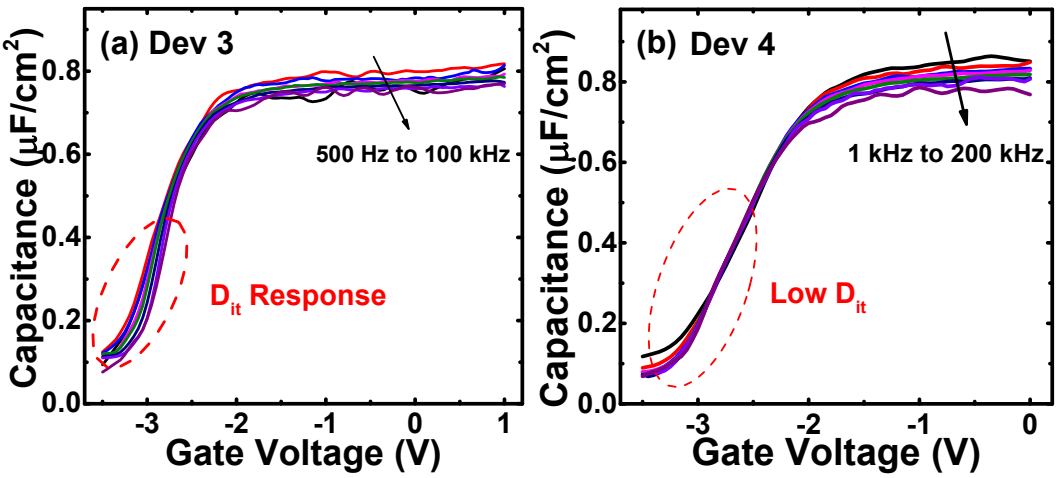


Figure 4. Another two devices showing lower D_{it} response, indicating the device-to-device variability.

Comparing with previous studies on HfO_2/MoS_2 interfaces,[14,19] annealing with the same conditions have noticeably different effects on the electrical behavior of the devices with Al_2O_3/MoS_2 interfaces. The 300˚C FGA introduces more positive charges in HfO_2/MoS_2 stacks,[19] but reduces positive charges and interface traps in $HfO_2/Al_2O_3/MoS_2$ stacks. The 400˚C FGA

reduces positive charges in HfO_2/MoS_2 stacks and may slight degrade the devices.[19] However, the 400˚C FGA largely degrades the interfaces and performance of devices with $HfO_2/Al_2O_3/MoS_2$ stacks. Confirmation of this is observed in device #4, which shows no appreciable D_{it}, but was annealed at 400˚C. The results are included in the supplemental information (Fig. S4) and clearly demonstrate degraded C-V results. If 400˚C was a viable FGA temperature for the Al_2O_3/MoS_2 interface, then the C-V data should have simply reproduced the pre-annealed results for device #4. It seems that the Al_2O_3/MoS_2 interface is more "sensitive" to the anneal temperature, which requires a lower annealing temperature to enhance the device performance, compared to HfO_2/MoS_2.

Simulation and Discussion

In order to quantify the energetic and spatial distributions of these interface traps and border traps observed in the C-V characterization, models of defects[20–22] are used to simulate the C-V response of electrically active traps in the gate stack. The C-V characterization for the sample annealed at 300˚C is fitted by the simulation software. Both experimental and simulated C-V characteristics are shown in Fig. 5 – experimental data as symbols and simulated data as lines. The inset figures show schematic device structures with interface traps in blue and border traps in red. Schematic energy band diagrams are show in Fig. 6, with the interface and border traps that affect the C-V behavior in our experiments. The traps are determined to be uniformly distributed within a certain energy range. Before the anneal, the energy distribution of the D_{it} is continuous from the MoS_2 conduction band edge (E_{CB}) to 0.35eV below the band edge, with a value of $1.3\times10^{13}cm^{-2}$ eV^{-1}. The simulation result shows that the 300˚C FGA decreases D_{it} from $1.3\times10^{13}cm^{-2}$ eV^{-1} to an ultra-low value (D_{it} removed in the simulation after the anneal). A border trap concentration of N_{bt} = 1.0×10^{19} cm^{-3} in the Al_2O_3/MoS_2 interfacial region is found before and after the anneal,

consistent with the intrinsic defect densities reported in the literature for alumina. The traps in HfO_2 are not considered here due to the relative distance from the MoS_2 interface, although the fixed positive charges in HfO_2 [28] are included. The D_{it} value before the anneal is slightly higher than the extracted D_{it} from H-L frequency method, probably because the frequency range of the experiments cannot reach the ideal limits for the H-L method, which can result in an underestimation of the D_{it} (i.e., D_{it} can respond with the AC signal in a wider frequency range than measured). The positive charges in the Al_2O_3 dielectric decreases from 5.1×10^{13} cm^{-2} to 2.6×10^{13} cm^{-2} due to the anneal. Interestingly, the anneal activates unintentional n-type doping in MoS_2 (from 9.0×10^{18} cm^{-3} to 1.7×10^{19} cm^{-3}), which was also reported previously for the HfO_2/MoS_2 interface.[19] These unintentional doping sites may come from the impurities[29] in the MoS_2 layers.

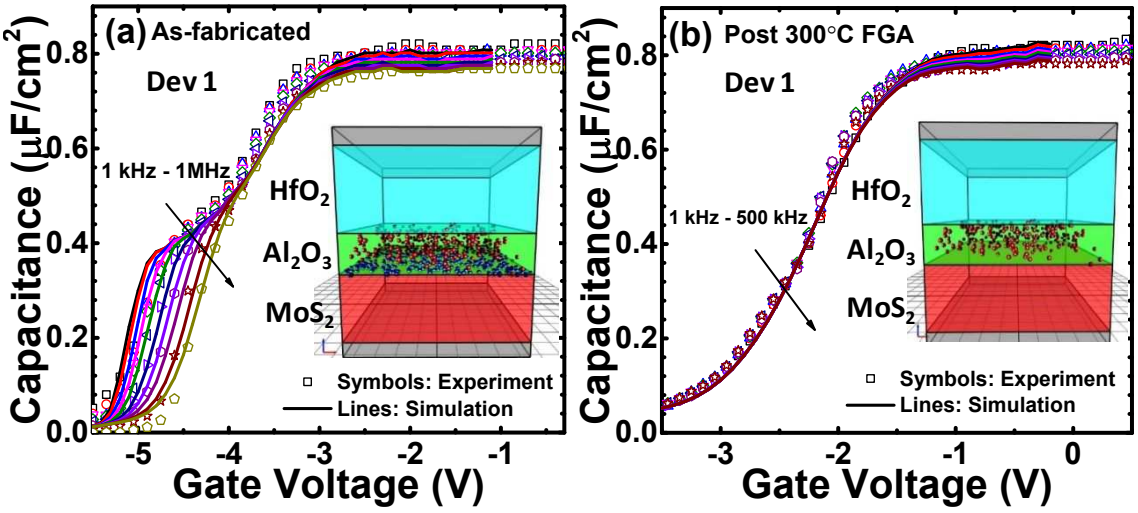


Figure 5. Simulation fitting of C-V characterization results for (a) As-fabricated device. (b) Device after FGA 300 ˚C. Inset: Schematic device structure with interface traps (blue) and border traps (red).

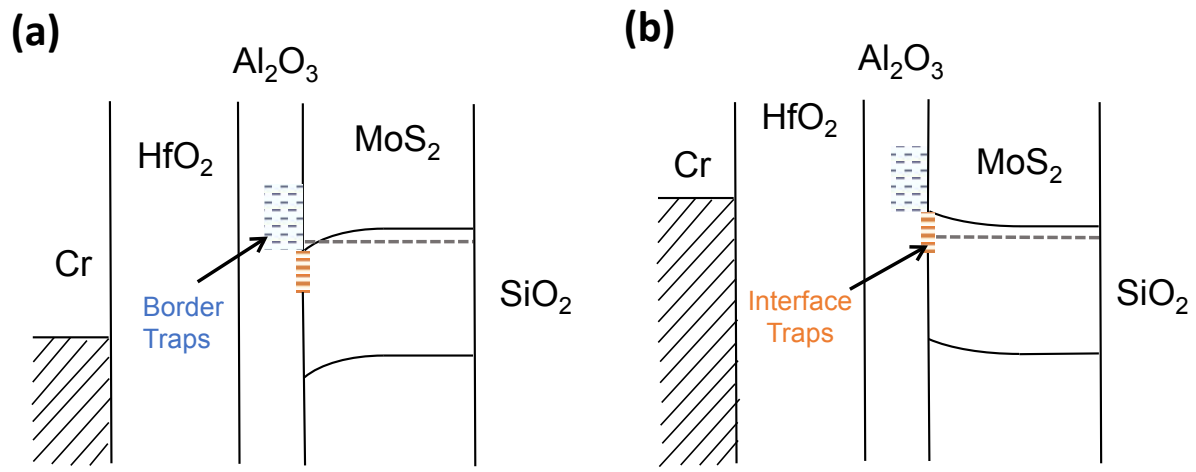


Figure 6. Schematic energy band diagrams of the distributions of interface traps (before anneal) and border traps (before/after anneal). (a) In accumulation, border traps in Al_2O_3 have an influence of the C-V characterization. (b) In depletion, interface traps in the MoS_2 band gap dominate the C-V response.

The other as-fabricated devices are also studied using the same defect models.[20–22] Figure 7 shows the C-V fitting results for three other devices which are fabricated with the same process but demonstrate slightly different electrical characteristics. All the devices show different C-V behavior in the depletion region due to different D_{it} distribution but similar behavior in the accumulation due to similar border traps densities. The D_{it} and its energy range, correlated subthreshold slope (SS) from Fig. S3, and N_{bt} values are summarized in Table 1. Device 4 has little C-V dispersion information, so it is hard to accurately estimate the D_{it} (about $6.2\times10^{11}cm^{-2}eV^{-1}$, extracted from the little dispersion in the depletion region) and energy range for this device. All other devices show a D_{it} energy ranging from the MoS_2 conduction band edge (E_{CB}) to 0.13-0.35 eV below in the band gap, and a range of D_{it} values.

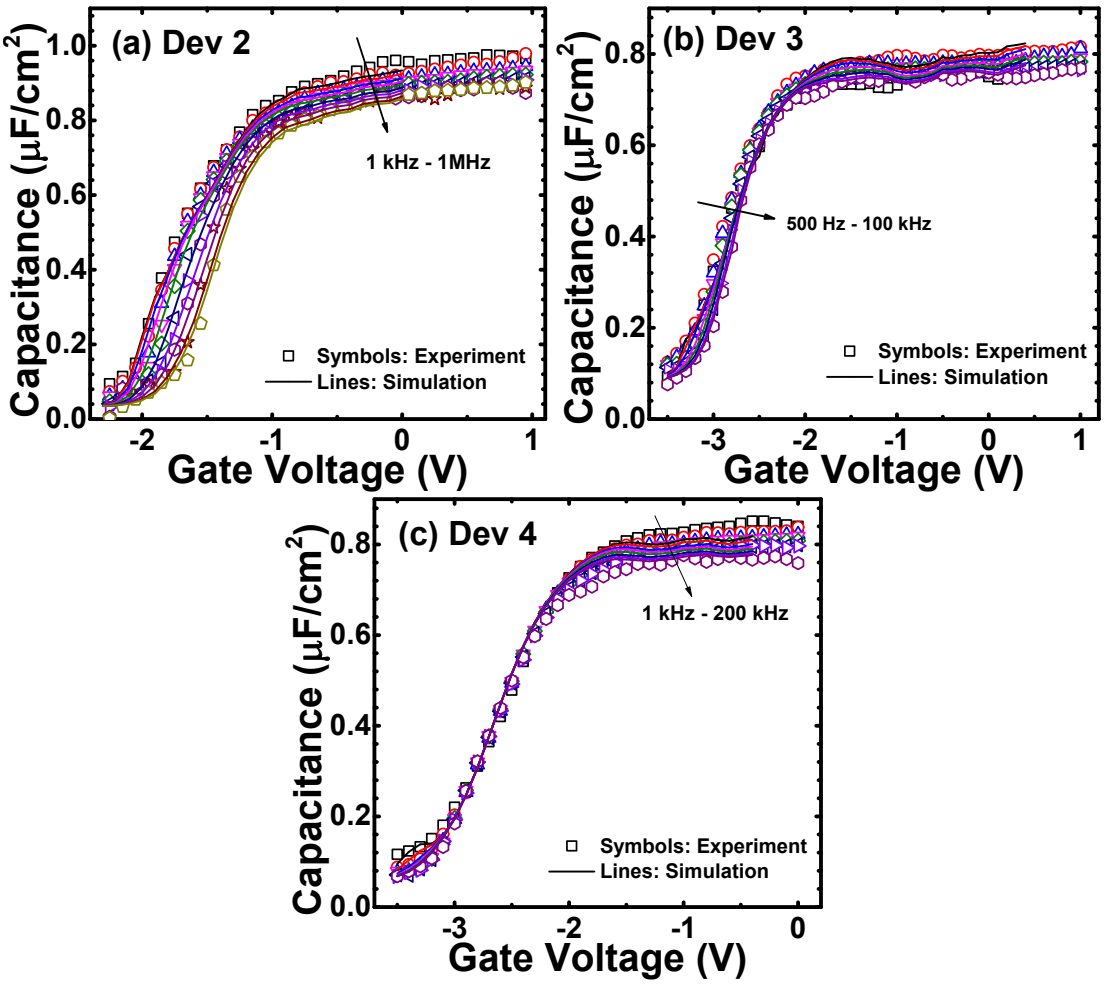


Figure 7. Defect model[20–22] fitting results of C-V characterizations on another three as-fabricated devices.

Table 1. Summary of D_{it} , SS, and N_{bt} of as-fabricated samples.

	Device 1	Device 2	Device 3	Device 4
D_{it} (10^{13} cm^{-2} eV^{-1})	1.3	1.6	0.27	Below detection
D_{it} Energy Range	E_{CB} to E_{CB}-0.35 eV	E_{CB} to E_{CB}-0.13 eV	E_{CB} to E_{CB}-0.30 eV	
Subthreshold Slope, SS (mV/dec)	~121	~131	~70	~67
N_{bt} (10^{19} cm^{-3})	1.0	2.3	1.5	2.0

Based on the analysis above, the D_{it} is highly likely related to defects which exist before surface treatment or ALD, due to the range of different values with similar D_{it} energy distributions. Sulfur vacancies (V_S)[26,27,30,31] are the defects that have been widely reported in the literature. The V_S can likely cover 0.1% -5% of the surface area after mechanical exfoliation,[26] which is well within the

range that electrical characterization can detect. However, the sulfur vacancies should have a peaked distribution and the energy level is relatively deep into the band gap,[32] while in our case, the defects levels are uniform, continuous, and are close to conduction band edge. Thus, the defects directly detected in the C-V measurements here are not peak-distributed V_S. Actually, considering the process of gate stack formation, especially the UV-O_3 treatment,[17] it can be safely assumed that most Vs are readily filled by oxygen during the treatment because of a lower formation energy needed for oxygen to fill the Vs than the energy of the O-S bonds formation.[17] The continuous defect levels close to conduction band edge are also in a good agreement with the simulation focusing on the oxidation of the MoS_2 surface.[33] In the simulation work by S. KC, et al.,[33] where oxygen filled the Vs, the density of states (DOS) are formed at both conduction band and valence band edges of MoS_2, and the DOS at conduction band are continuous and relatively uniform (Fig. 6 in reference[33]). Thus, a plausible origin of the D_{it} in our experiments are quite likely oxygen atoms that fill the Vs during the UV-O_3 treatment. Also, defects may be greatly reduced if V_S can be passivated before the UV-O_3 surface functionalization, using a sulfur treatment[34] that has been proposed in the literature. To further minimize the density of these defects, it is found that the 300˚C FGA works for reducing the D_{it} response, possibly by a H-passivation process.

Conclusion

In this work, top-gated, few-layer MoS_2 transistors with HfO_2 (6 nm) / Al_2O_3 (3 nm) gate dielectric stacks are fabricated and electrically characterized by C-V measurements to study electrically active defects in the interfacial region. Devices with low D_{it} and high D_{it} are observed in the C-V characterization. FG anneals at 300˚C or 400˚C are performed on devices having interface states present. A 300˚C FG anneal is able to reduce the D_{it} significantly while the 400˚C

FG anneal increases defects in the gate stack. Simulation results suggest a largely decreased D_{it}, reduced positive charge in the dielectric, but slightly increased unintentional doping in MoS_2 after the 300˚C FG anneal. For the as-fabricated devices having D_{it}, the energy distribution of the D_{it} is continuous from the conduction band edge of MoS_2 down to 0.13eV - 0.35eV into the band gap, at Al_2O_3/MoS_2 interface for all devices measured. A plausible D_{it} origin in our experiments is that unexpected oxygen atoms fill the sulfur vacancies during the UV-O_3 treatment. The border trap concentration in Al_2O_3 is not changed before and after the anneal, suggesting different origins of these traps, possibly due to the low-temperature ALD process. While the 300˚C FGA works for reducing the D_{it} response, it may also be greatly reduced if the sulfur vacancies can be passivated before the UV-O_3 surface functionalization.

Supporting Information

Optical photos of a representative device (Fig. S1); Parameters used/extracted in defect modeling (Table S-I); Typical (a) I_{DS}-V_{GS} (b) I_{DS}-V_{DS} characteristics for the as-fabricated MoS_2 transistors (Fig. S2); I_{DS}-V_{GS} data for the four devices used in C-V collection and analysis (Fig. S3); Multi-frequency C-V result for device #4 after a 400°C FGA (Fig. S4).

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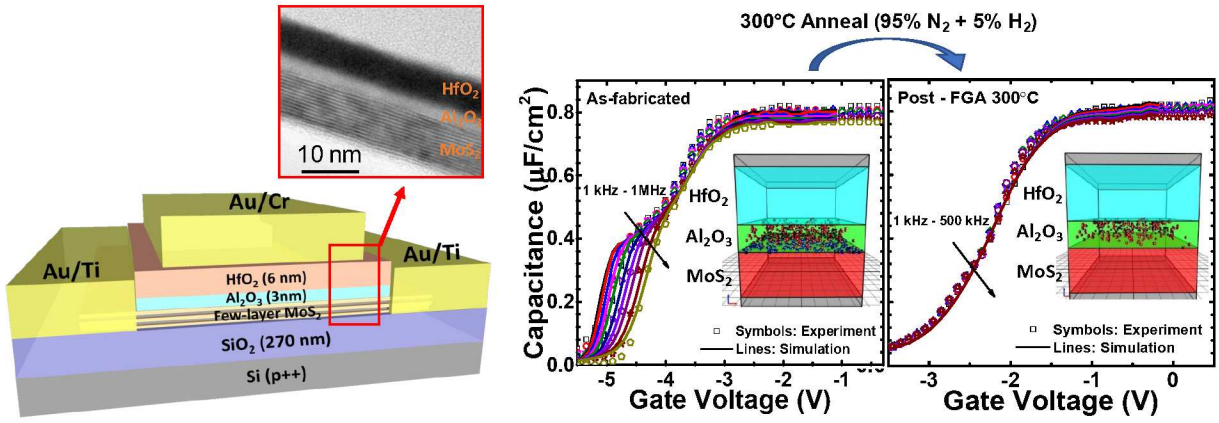
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TOC


10 nm
HfO2
Al2O3
MoS2
Au/Cr
Au/Ti
Au/Ti
HfO2 (6 nm)
Al2O3 (3nm)
Few-layer MoS2
SiO2 (270 nm)
Si (p++)
300°C Anneal (95% N2 + 5% H2)
As-fabricated
Post - FGA 300°C
Capacitance (μF/cm2)
1 kHz - 1MHz
1 kHz - 500 kHz
Symbols: Experiment
Lines: Simulation
Gate Voltage (V)