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# Fermi level de-pinning of aluminium contacts to n-type germanium using thin atomic layer deposited layers

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# Fermi level de-pinning of aluminium contacts to *n*-type germanium using thin atomic layer deposited layers

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Fermi-level pinning of aluminium on *n*-type germanium (*n*-Ge) was reduced by insertion of a thin interfacial dielectric by atomic layer deposition. The barrier height for aluminium contacts on *n*-Ge was reduced from 0.7 eV to a value of 0.28 eV for a thin $Al_2O_3$ interfacial layer (~2.8 nm). For diodes with an $Al_2O_3$ interfacial layer, the contact resistance started to increase for layer thicknesses above 2.8 nm. For diodes with a $HfO_2$ interfacial layer, the barrier height was also reduced but the contact resistance increased dramatically for layer thicknesses above 1.5 nm. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4858961]

Silicon-based MOSFETs (metal–oxide–semiconductor field-effect transistors) are reaching their physical scaling limits. Germanium has become a promising material for future CMOS (complementary metal–oxide–semiconductor) technology as it has high electron and hole mobility compared with silicon. Germanium also provides a higher saturation velocity which can eliminate the problem of drain current saturation in MOSFETs.[1] The instability of native oxide ($GeO_x$) on germanium[2] is the main obstacle for Ge-based MOSFETs, but high-$\kappa$ dielectrics on germanium have created renewed interest.[3] Significant progress has been achieved in *p*-MOSFETs,[4–7] while for *n*-MOSFETs there are still some hindrances.[6,8] The low solubility and high diffusion constants of *n*-type dopants make it difficult to produce ultra-shallow junctions in *n*-MOSFETs.[9]

Fermi level pinning of metal contacts on *n*-type germanium is a further issue and it makes the metal contact to $n^+$ source/drain regions rectifying, irrespective of metal work function. Fermi level pinning is caused by interface states between the metal and the semiconductor. Thus, to achieve ohmic contacts to *n*-type germanium, passivation of the germanium surface is needed. Kobayashi *et al.* de-pinned the Fermi level by growing an ultra-thin interfacial SiN layer.[10] Also, Thathachary *et al.* demonstrated Fermi level unpinning by sulphur passivation of the germanium surface prior to metal contact deposition.[11] Lieten *et al.*[12] fabricated ohmic contacts on germanium by producing a thin $Ge_3N_4$ layer with plasma nitridation of germanium prior to the metal deposition. However, this process needs high temperature annealing after the interfacial layer growth, which can increase the thermal budget of the fabrication. Zhou *et al.*[13] used a thin layer of aluminium oxide grown from oxidation of a thin layer of aluminium on germanium to un-pin the Fermi level of cobalt, nickel, and iron metal contacts on *n*-type germanium. In this process, the aluminium oxide was produced by oxidation of deposited aluminium. Researchers have also utilized sputtering techniques,[14] silicon passivation[15] at the metal-semiconductor interface to form an ideal metal-germanium contact without Fermi-level pinning and, therefore, obeying thermionic emission theory.

The mechanism of barrier height reduction by interfacial layer insertion is not always clear. It is often attributed to blocking of the electron wave function between metal and semiconductor and consequent reduction in the number of metal-induced gap states (MIGS).[16,17] More recently, several authors have argued that a dipole at the metal-semiconductor interface[18–21] or trapped charge in the interfacial layer will also alter the barrier height.[22] Roy *et al.*[19] showed that $TiO_2$ can be a good interface material as it has nearly zero conduction band offset. The materials with low electron barrier height and low dielectric constant would be the suitable interface material for low specific contact resistivity at the interface.[19] The materials, $Al_2O_3$ and $HfO_2$, fall in the low dielectric constant category compared with $TiO_2$. In this paper, atomic layer deposition (ALD) has been used to produce well-controlled interfacial layers of both $Al_2O_3$ and $HfO_2$. The influence of ALD interfacial layer thickness on the electrical characteristics of aluminium contacts on *n*-type germanium is studied. Thermionic emission theory has been applied to extract barrier height and the validity of this approach is discussed.

*N*-type germanium wafers of resistivity 0.34–035 Ωcm and 0.09–0.1 Ωcm were used for this work. All samples were degreased for 2 min in acetone and 2 min in methanol followed by a DI water rinse. Samples were then cleaned using 3 cycles of 1:10 HF solution and DI water, and dried in $N_2$ ambient. All samples were introduced to the load lock chamber of the ALD system with a minimum exposure to the atmosphere. On one set of wafers with 0.34–0.35 Ωcm resistivity, a thin alumina layer was deposited at 300 °C with $Al_2O_3$ thicknesses in the range of 1.4 nm to 3.1 nm along with a control sample without any interfacial layer. On the other set of wafers with 0.09-0.1 Ωcm resistivity, a thin hafnium dioxide layer was deposited at 250 °C with $HfO_2$ thicknesses in the range of 1.0 nm to 3.5 nm. Trimethylaluminum (TMA) and water ($H_2O$) were used as precursors for $Al_2O_3$ deposition and tetrakis (ethyl methyl amido) hafnium and water were used as precursors for $HfO_2$ deposition.

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The thicknesses of the $Al_2O_3$ and $HfO_2$ layers were measured using spectroscopic ellipsometry. The typical deposition rate for ALD alumina was measured as ~0.9 Å/cycle and the deposition rate of $HfO_2$ was ~0.8 Å/cycle. Aluminium of 100 nm thickness was deposited on these wafers by thermal evaporation and patterned into 1 mm diameter contacts.

Current-voltage measurements were carried out at different temperatures ranging from room temperature to 72 °C. It is accepted that the variation of current with temperature has to be studied to give an accurate value of barrier height, because of uncertainty in the value of the Richardson constant for germanium. Thermionic emission theory was used to find the Schottky barrier height. The relationship between current ($I$) and voltage ($V$) used for the calculations was[23]

$$I = I_s \exp\left(\frac{qV}{nkT}\right), \tag{1}$$

where $I_s$ is the reverse saturation current, defined as

$$I_s = AA^*\mathrm{T}^2 \exp\left(\frac{-q\varnothing_{Bn}}{kT}\right). \tag{2}$$

Here $A$ is the contact area, T is the measurement temperature, $A^*$ is the Richardson constant, $\varnothing_{Bn}$ is the Schottky barrier height for electrons, $n$ is the ideality factor, $k$ is the Boltzmann constant, and $q$ is the electron charge ($1.6 \times 10^{-19}$ coulombs). From Eq. (1), the intercepts from log $I$ vs $V$ plots at different measurement temperatures give the corresponding reverse saturation currents ($I_s$), the slope gives the ideality factor and the barrier height can be extracted from the slope of a $\ln(I_s/T^2)$ vs $1/T$ graph.

Figure 1 shows the $I$–$V$ characteristics of aluminium contacts on $n$-Ge wafers of resistivity 0.34–0.35 Ωcm and 0.09–0.1 Ωcm measured at room temperature. The inset diagram shows $I$-$V$ measurements at a range of temperatures for aluminium contacts on $n$-Ge with resistivity of 0.34–0.35 Ωcm. Aluminium contacts to $n$-Ge showed rectifying behaviour. The barrier height for electrons is ~0.7 eV for aluminium on $n$-type germanium irrespective of germanium resistivity, and the ideality factor is ~1.03. The ideal barrier height of aluminium contacts to germanium is ~0.28 eV for electrons and ~0.38 eV for holes, assuming an aluminium work function of 4.28 eV,[24] germanium electron affinity of 4 eV and germanium band-gap of 0.66 eV. The unusual barrier height of aluminium on $n$-type germanium in these experiments can be explained by Fermi-level pinning of aluminium on germanium.

In this case, the Fermi level of the semiconductor is pinned at the charge neutrality level surface states and the barrier height of the contact is no longer dependent on the metal work function, but on the position of the charge neutrality level of the semiconductor. In germanium, it is shown that the charge neutrality level is close to the valence band.[16,25] Irrespective of metal work function, all metals show a larger barrier height for electrons on $n$-type germanium[25] and for the same reason, all metals will form good ohmic contacts on $p$-type germanium. In these experiments, the barrier height for electrons (~0.7 eV) is higher than the band-gap energy of germanium (0.66 eV). Chi *et al.*[26] also observed a barrier height for nickel on $n$-type germanium larger than the band-gap of germanium. Walpole and Nill[27] and Chi *et al.*[26] proposed an inversion layer model, in which a very thin inversion layer on the surface causes the maximum electric field to be very high in the space charge region which increases the barrier height above the semiconductor band-gap.

When a thin interfacial layer is inserted between the aluminium and the $n$-type germanium, it is expected that the barrier height will be reduced. However, if the interfacial layer is too thick, the tunnelling resistance of the contact will increase. Connelly *et al.*[28] considered the optimum thickness of the interfacial layer to be a compromise between Fermi-level unpinning and tunnelling resistance of the metal contact. Figure 2 presents the model they used to define the optimum interfacial layer thickness.

Figure 3 shows a comparison of current-voltage measurements for $Al/Al_2O_3/n$-Ge diodes measured at room temperature with variation of the alumina interfacial layer thickness. The change from a rectifying aluminium contact to a more non-rectifying contact with insertion of an interfacial layer can be clearly seen in this figure. Figure 4 shows

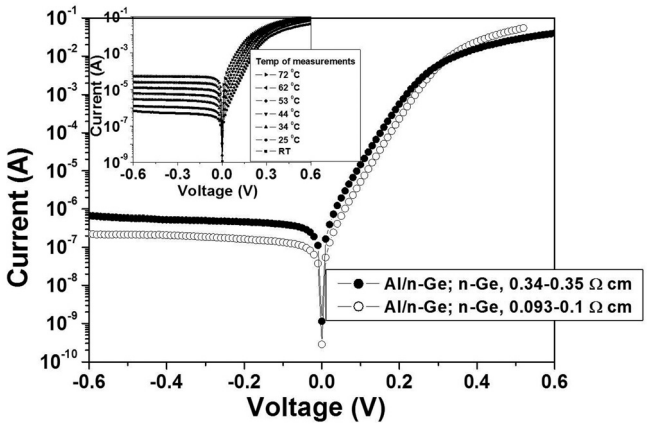



FIG. 1. Current-voltage measurements of aluminium contacts on $n$-type germanium. Aluminium contact formed a rectifying barrier on $n$-Ge irrespective of the germanium resistivity. Inset diagram shows $I$-$V$ measurements on Al/$n$-Ge (0.34–0.35 Ωcm) at a range of temperatures.

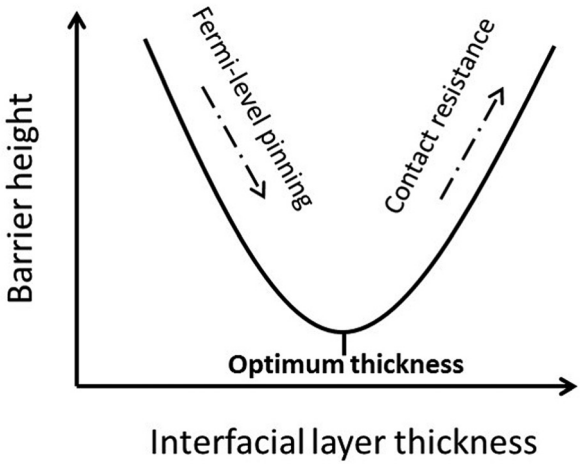



FIG. 2. The model for deciding the interfacial layer thickness between metal and semiconductor contact.

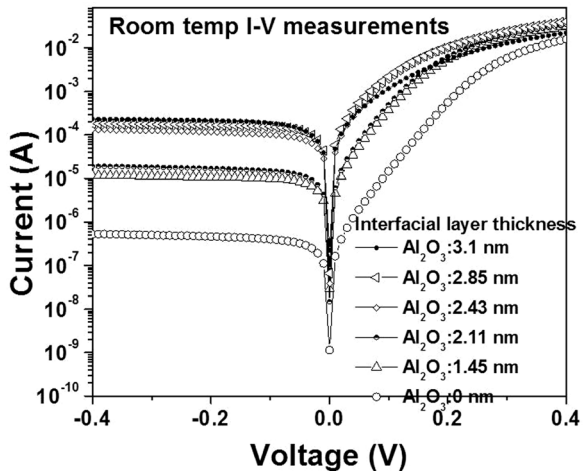



FIG. 3. The comparison of current-voltage measurements for Al/$Al_2O_3$/*n*-Ge diodes measured at room temperature.

the Richardson plots ($\ln(I_s/T^2)$ vs $1/T$) of all these diodes. The barrier height of Al/$Al_2O_3$/*n*-Ge diodes was calculated from the slopes of the Richardson plots and the corresponding barrier height of aluminium on *n*-germanium with interfacial layer thickness is plotted in Figure 5. It is observed that by insertion of a thin interfacial layer, the barrier height of aluminium contacts on *n*-type germanium reduced from 0.7 eV with no interfacial layer to 0.28 eV with an interfacial layer of thickness 3.1 nm. Thus the insertion of an ALD $Al_2O_3$ layer has almost completely de-pinned the Fermi level of aluminium contacts on *n*-type germanium.

The diode with a 3.1 nm thick interfacial layer yields the lowest $I_{on}/I_{off}$ ratio with an ideality factor of 1.4. However, the contact resistance starts to increase for $Al_2O_3$ thickness above 2.85 nm. This is due to the increase in the tunnel resistance caused by inserting an insulator between aluminium and *n*-type germanium. Therefore, the optimum interfacial layer thickness is approximately 2.8 nm. The increased ideality factor could be due to image force lowering[23] or barrier inhomogeneity[29] of the contact. However, the well-behaved Richardson plots of Figure 4 and the fact that the ideality factor remains less than 1.5 imply that thermionic emission theory satisfactorily describes the diode behaviour.

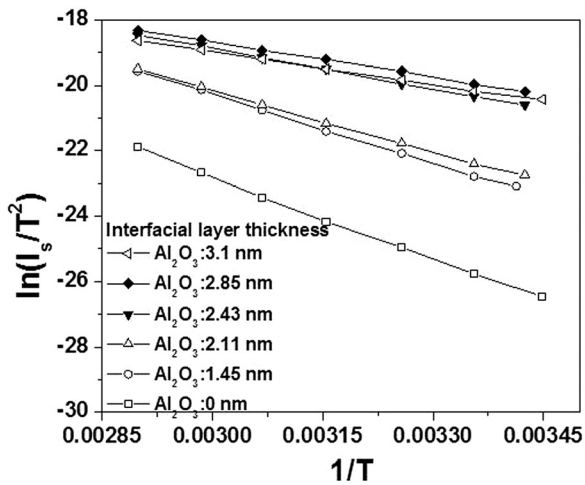



FIG. 4. Richardson plots for Al/$Al_2O_3$/*n*-Ge diodes. The corresponding interfacial layer thickness is mentioned on the diagram.

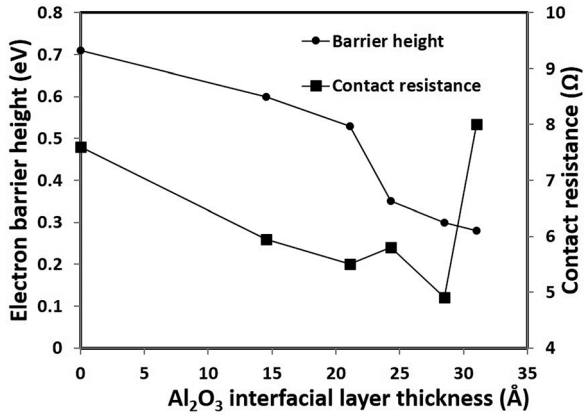



FIG. 5. Variation of barrier height and contact resistance of aluminium contact for Al/$Al_2O_3$/*n*-Ge diodes.

Figure 6 shows the variation of barrier height and contact resistance of aluminium contact with interfacial layer thickness for Al/$HfO_2$/*n*-Ge diodes. By the insertion of a $HfO_2$ interfacial layer, the barrier height dropped from 0.7 eV to a minimum value of 0.34 eV with an ideality factor of 1.5 for the diode with a $HfO_2$ thickness of ~2.7 nm. The ideal barrier height of aluminium contacts to *n*-type germanium is 0.26 eV. So, with a $HfO_2$ layer, the Fermi level is not completely unpinned, but a significant reduction in the barrier height has been achieved. With increasing $HfO_2$ thickness, the contact resistance of the Al/$HfO_2$/*n*-Ge diodes increases. This increase in contact resistance is due to the high dielectric constant value of $HfO_2$ and charge trapping in the $HfO_2$ layer.[30,31]

In conclusion, we report Fermi level de-pinning of aluminium contacts on n-type Ge with a thin ALD layer. As a compromise between series resistance and barrier height for aluminium contacts on *n*-type germanium, a thin ALD alumina layer with thickness of approximately 2.8 nm is recommended. For diodes with an alumina interfacial layer, the contact resistance started to increase for layer thicknesses above 2.8 nm, whereas for diodes with a hafnium dioxide interfacial layer, the contact resistance increased dramatically for layer thicknesses above 1.5 nm because of the high dielectric constant of $HfO_2$.

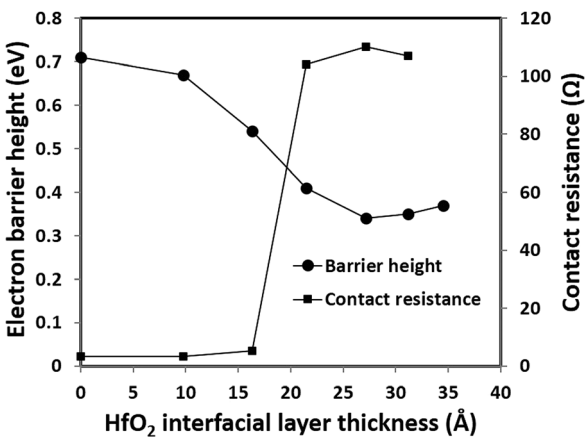



FIG. 6. Variation of barrier height and contact resistance of aluminium contact for Al/$HfO_2$/*n*-Ge diodes.

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