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Investigating positive oxide charge in the SiO_2/3C-SiC MOS system

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This paper investigates the origin of the fixed positive oxide charge often experimentally observed in Metal Oxide Semiconductor (MOS) structures of SiO_2 formed on cubic silicon carbide (3C-SiC). The electrical properties of MOS structures including either thermally grown SiO_2 or deposited SiO_2 by Plasma Enhanced Chemical Vapour Deposition (PECVD) on epitaxial 3C-SiC layers grown directly on Si are investigated. MOS structures with a range of oxide thickness values subjected to different thermal treatments were studied. It was found that both thermally grown and deposited SiO_2 on 3C-SiC exhibit similar positive charge levels indicating that the charge originates from interface states at the 3C-SiC surface and not from the oxide. The nature of this surface charge in the SiO_2/3C-SiC system is also discussed based on the current data and previously published results. © *2018 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).* https://doi.org/10.1063/1.5030636

INTRODUCTION

SiC presents a high electric breakdown field and a wide band gap which makes it a suitable semiconductor for power electronics.[1] The hexagonal SiC polytype (4H-SiC) is by far the most studied SiC polytype[2] and currently large bulk wafers of 4H-SiC are commercially available, albeit at a much larger cost than typical Si wafers used in the microelectronics industry.[3] 3C-SiC presents a significant cost advantage over 4H-SiC as it can be grown directly on Si by Chemical Vapour Epitaxy (CVD) at high temperature.[4] The availability of good quality 3C-SiC epitaxial layers on Si will enable the implementation of cost effective SiC power devices in the range 650V to 1200V.

SiC based power devices such as MOSFETs rely on a good quality gate oxide and a well-controlled oxide/SiC interface. The presence of oxide charge could shift the transistor characteristics or could affect the electric field profiles at the device edge terminations or in extreme cases could generate unwanted inversion layers at the oxide/SiC interface resulting in high levels of junction leakage currents. Furthermore, defects at the oxide/SiC interface create states which change occupancy with the modulation of the surface potential at the interface and this would also affect the switching of the device and cause instabilities.[5]

Thermally grown SiO_2 on 3C-SiC in pure O_2 very often shows the presence of a large density of positive oxide charge.[6] Significant levels of positive charge are also observed in oxides grown by dry oxidation at high temperature (1200°C-1400°C).[7] Some reports demonstrated that this positive charge can be reduced by thermal treatment in wet oxygen.[8,9]

This study combines a large number of thermal and deposited SiO_2 layers on 3C-SiC epitaxially grown on Si samples in order to investigate the electrical properties of the SiO_2/3C-SiC

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interface. In addition, a wide range of oxide thickness values and post oxidation treatments are also exploited in order to gain better understanding of the origin of the positive charge in the SiO_2/3C-SiC system. The work describes the characterisation of various gate oxide layers grown on the n-type drift layer, rather than a p-type body, to simplify and focus the problem on the SiO_2/SiC interface.

EXPERIMENTAL DETAILS

The 3C-SiC/Si epitaxial process uses a [100] n+ Si wafer (Sb doped), offset by 4° in the [110] direction to encourage step-flow epitaxial growth. The precursors are Silane and Ethylene, a conventional Carbonisation route is taken during the temperature ramp to the growth temperature of 1370°C. A Nitrogen doped buffer layer is produced at the Si/SiC interface and then the 6 to 7 micron drift layer is grown. The SiC layer is not intentionally doped, but yields an n type semiconductor with a doping of approximately $5x10^{15}cm^{-3}$. After growth a CMP step produces a smooth layer with a roughness of less than 0.5nm.

Gate oxides can be grown in a conventional Si oxidation furnace, but at higher temperatures compared to Si due to the lower oxidation rate of 3C-SiC. Alternatively PECVD can be used to deposit an oxide, but this requires a further densification step, either in Nitrogen, or dry or wet Oxygen.

Prior to thermal oxidation or oxide deposition, the wafers (both Si and SiC) were cleaned using an equivalent of the industry-standard RCA clean (DI-water/ozone/dilute NH_4OH/dilute HF). The oxide film was then either thermally grown (dry O_2 thermal oxidation at 1150°C) in an atmospheric tube-furnace or else deposited by PECVD (SiH_4/N_2O gas-chemistry at 300°C) in a low-frequency (380 kHz) PECVD tool. The PECVD SiO_2 process used in this study was optimised on bulk Si wafers and includes a densification thermal treatment in N_2 at 900°C for 120min resulting in near ideal SiO_2/Si MOS capacitors. The PECVD SiO_2 received post-deposition anneals in wet ambient in an atmospheric tube-furnace. For the wet annealing treatment H_2 and O_2 were introduced in the tube furnace (ratio 1.6) in order to generate steam. A pure Aluminium metal film was deposited in a sputter tool and lithographically patterned and wet-etched using a commercially-supplied Al wet-etch solution consisting-of orthophosphoric acid/nitric acid/acetic acid to define capacitor test structures. Finally, the wafers received a forming gas anneal $N_2(95\%)/H_2(5\%)$ at 425°C for 30min. The capacitance voltage (C-V) characteristics were recorded using an LCR meter. The on-wafer measurements were performed in a probe station at room temperature.

RESULTS AND DISCUSSION

An example of multi-frequency C-V characteristics measured on an Al/SiO_2/3C-SiC/Si MOS structure is shown in figure 1. The nominally 50nm thick SiO_2 layer was grown by thermal oxidation in dry O_2 at 1150°C. In addition to the experimental C-V, figure 1 includes a simulated 1MHz C-V characteristic obtained using a physics based commercial ac simulator. The theoretical C-V is simulated using standard drift diffusion transport models and Fermi-Dirac statistics. For the simulation, the n-type doping in SiC was assumed $5X10^{15}$ cm^{-3}, the 3C-SiC electron affinity and band gap were 3.8eV and 2.36eV, respectively, while the value used for the Al work function was 4.1eV. This resulted in a theoretical flat band voltage (Vfb) of approximately 0.1V. The SiO_2 thickness (56.6nm) used for the simulation was the value extracted from the experimental C-V. The most remarkable feature of the experimental C-V is the large negative Vfb (18.6V) recorded for this MOS structure. Such a voltage shift could be caused by a positive line charge at the SiO_2/SiC interface of approximately $7x10^{12}cm^{-2}$. The nature of this positive charge is main focus of this study.

In accumulation, the C-V curves are very well behaved and show no evidence of oxide charge trapping by oxide border traps communicating with carriers in the conduction band. This is also confirmed by the negligible C-V hysteresis measured on similar MOS structures. Figure 2 shows the level of hysteresis measured on MOS capacitor with a 21nm thick thermally grown SiO_2 layer.

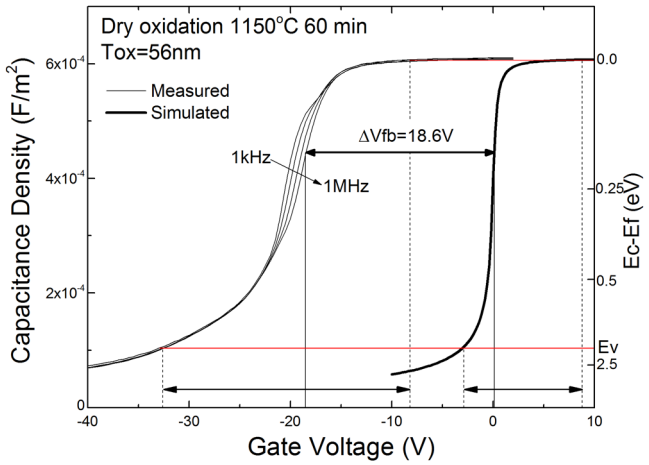


FIG. 1. Measured multi-frequency C-V characteristics of an Al/SiO_2/3C-SiC/Si MOS structure. The thickness of the thermally grown oxide extracted from the C-V was 56.6nm. The physics based 1MHz ac simulated CV is obtained assuming the same oxide thickness and 3C-SiC n-type doping $5x10^{15}$ cm^{-3}. The right axis indicates the surface Fermi level position for different gate voltage values.

The charge trapping estimated from the hysteresis amplitude (~20mV) is negligible ($2x10^{10}$ cm^{-2}) compared to the level of positive charge. In addition, the quality of the oxide is confirmed by the breakdown field values obtained on these MOS capacitors, which were close to those of thermal oxides grown on Si (10MV/cm).

A number of important physical parameters of the MOS capacitor are accessible at every bias through the physics based ac simulator. As the simulator computes the potential and charge carrier densities at every point of the physical structure, in particular the surface Fermi level at the 3C-SiC/SiO_2 interface is extracted. The right axis of figure 1 shows the excursion of the surface Fermi level between the conduction band (Ec) and the valence band (Ev) as extracted from the simulation data. The dashed vertical lines point to the voltage values at which Ec or Ev are reached. By projecting the theoretical capacitance value on the experimental curve we can estimate the surface Fermi level for a given gate voltage. This assumes the 1MHz CV is the true high frequency C-V, which is a reasonable assumption considering the wide band gap of 3C-SiC.

When comparing the ideal 1MHz C-V curve with the measured one it is evident the experimental C-V is stretched out. The noticeable dispersion with frequency in the C-V characteristic is due to interface states in the upper band gap of 3C-SiC. The total density of interface states can be roughly

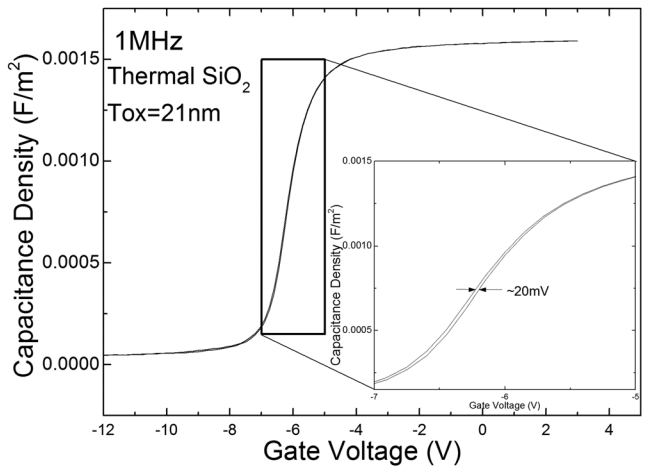


FIG. 2. C-V hysteresis measured on an SiO_2/3C-SiC MOS capacitor with 21.1 nm SiO_2 thermally grown on 3C-SiC.

estimated from the stretch-out magnitude measured on the highest frequency C-V characteristic. At high frequency, as the surface Fermi level is modified by the gate voltage, the charge occupancy of interface states is also changing which results in the C-V stretch out. Using the ideal C-V, the experimental C-V stretch out between Vfb and the gate voltage corresponding to the Fermi level at the valence band can be estimated. This method provides a rough estimate of the density of states but suffers from a limitation; it is the net charge density not the total interface defect density that is extracted. The extracted Dit value ~$4x10^{12}cm^{-2}$ is comparable to the level of positive fixed oxide charge. It is interesting to note that for both experimental and theoretical C-Vs the capacitance is decreasing past the voltage where the surface Fermi level reaches Ev, this deep depletion behaviour is to be expected in wide band gap materials where the generation of holes is insufficient to form an inversion charge counterbalancing the charges at the gate.

The extraction of fixed positive charge from the Vfb shift used in the example of figure 1 was implemented on a number of SiO_2/3C-SiC MOS structures, the Vfb shift values recorded for thermal oxides are presented as a function of oxide thickness in figure 3. The general trend for dry thermal oxide is a linear increase of Vfb shift with increasing oxide thickness which indicates that the shift is caused by a fixed positive line charge located at the SiO_2/3C-SiC interface. This positive charge could be generated as a result of the 3C-SiC thermal oxidation process. However, comparing the electrical properties of 3C-SiC MOS capacitors using deposited oxides with the results obtained using thermal oxides would help clarify this issue. Figure 4 shows the extracted oxide charge density as function of oxide thickness for the thermal and the PECVD SiO_2 3C-SiC MOS structures. It must be emphasised that the PECVD SiO_2 process was assessed on Si and resulted in very low Vfb shift (0.4V) equivalent to an apparent fixed charge ~$2x10^{11}$ cm^{-2} (see inset of figure 4). We can assume that the possibility of the two types of SiO_2 generating similar levels of positive charge but through different mechanisms as highly unlikely; meaning that in both cases the positive charge has the same origin. This result is significant as it indicates that the positive charge doesn't originate from the oxide but from the SiO_2/3C-SiC interface.

Origin of the positive charge

Could this positive charge be induced by interface states? And what could be the origin of these interface states?

It has been suggested in previous reports that interface states could be the cause of the positive charge at the interface of thermally grown SiO_2 on 3C-SiC.[7,8] The charge was attributed to donor states generated by carbon clusters or dangling bonds.[7,8] Our current results (figure 1) show a density of states $4x10^{12}cm^{-2}$ in the band gap as extracted by comparing the high frequency C-V

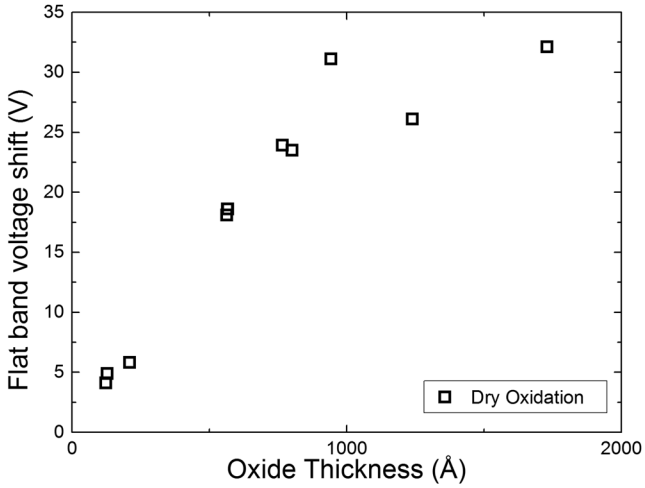


FIG. 3. Extracted flat band shift as function of oxide thickness for a range of Al/SiO_2/3C-SiC/Si MOS structures including thermal SiO_2 (grown at 1150°C). The flat band shift is measured with respect to a theoretical flat band value of 0.1V for an ideal Al/SiO_2/3C-SiC/Si MOS structure.

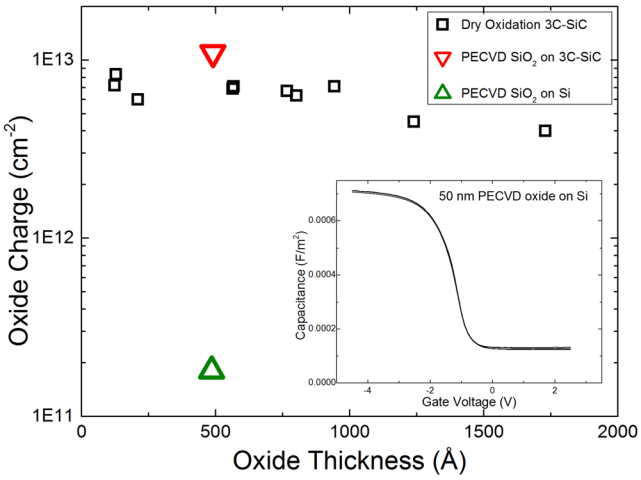


FIG. 4. Positive oxide charge density as function of oxide thickness extracted using the model of a line charge located at the SiO_2/3C-SiC interface. The inset shows C-V characteristics of the PECVD SiO_2/Si MOS structures where the measured oxide charge was almost two orders of magnitude lower than in the 3C-SiC MOS structures with either thermal or PECVD SiO_2.

with the ideal simulated C-V and $7x10^{12}cm^{-2}$ positive charge due to donor interface states energetically above the conduction band minimum. These donor interface states above the conduction band generated positive charge density ranging from $4x10^{12}$ up to $1x10^{13}$ cm^{-2} for the SiO_2/3C-SiC MOS structures with thermal SiO_2 and deposited PECVD (Figure 4). The occupancy of the donor states in the conduction band is unlikely to change as the surface Fermi level is restricted to energy close to the band edge. These donor states, as a result, manifest themselves as a 'fixed' positive charge.

A widely accepted interface states energy profile at the SiO_2/SiC interface was published by Afanasev et al. where the energy profile was extracted for the 3C, 6H and 4H-SiC polytypes using admittance spectroscopy.[10] The interface density was found very high (10^{12}-$10^{13}cm^{-2}$ eV^{-1}) in the lower band gap and near the 4H conduction band. For the 6H and 3C polytypes the density was lower near the edge of their respective conduction bands. A carbon cluster model was developed to explain the observed interface state energy profile. In this model, carbon clusters at SiO_2/SiC interface introduce energy states originating from the π bonds of sp2-hybridized carbon. The resulting energy profile consists of a donor band located in the lower band gap of different SiC polytypes (including 3C) and an acceptor band in the upper band gap of 4H-SiC and the conduction band of 3C-SiC (See figure 5). In case of small C clusters, the top of the donor band is located 1.4eV above the SiC valence band and a large gap (~3eV) separates it from acceptor band.[10] As the C clusters increase in size the resulting energy profile of interface states covers the full SiC band gap.

In order for the carbon cluster model to account for the observed Vfb shift in the C-V characteristics of the studied SiO_2/3C-SiC MOS structures, the SiC Fermi level must lie below the C clusters neutrality level, the donors above the Fermi level will then emit an electron and will be positively charged. The level of positive charge detected in this study suggests that the acceptor band possibly extends more than 1.4eV above the valence band edge and/or large C clusters are present at the interface and generate a band of acceptor levels higher in the band gap which is intersected by the surface Fermi level.

Figure 5 shows a simplified sketch of the carbon cluster model described in Ref. 10, the figure shows the donor and acceptor bands with respect to the 3C and 4H-SiC band gaps and illustrates how the donor band could be the origin of the positive charge at the interface. In figure 5, the broadening of the donor and acceptor bands is represented by the grey shaded regions which result in a continuum of states. In this simplified drawing, the surface charge neutrality level is well inside the conduction band of 3C-SiC resulting in permanently ionised donors (red region in figure 5). It is important to notice that for 4H-SiC, the neutrality level is within the band gap in this case; therefore the donors in this case should be fully occupied and neutral.

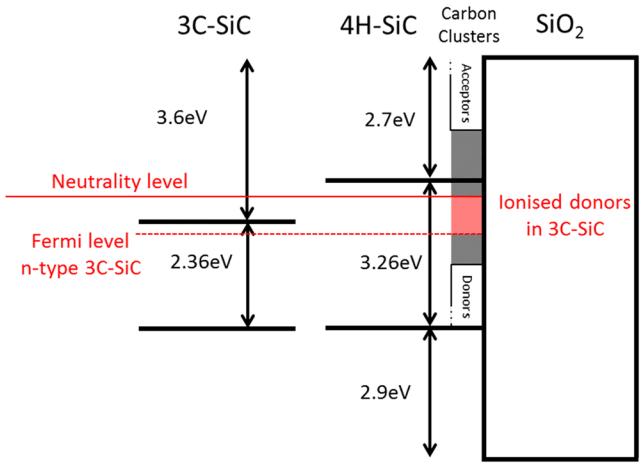


FIG. 5. Simplified band diagram showing the interface states energy profile according to the carbon cluster model.[10] The resulting Dit profile is presented with respect to the 4H and the 3C-SiC band gaps. The grey shaded region represents the broadening of donor and acceptor energy states predicted by the cluster model. The experimentally observed fixed positive charge could originate from the ionised donors energetically situated above the surface Fermi level and below the neutrality level.

It has been reported earlier that the presence of carbon on the SiC surface generate more Dit post oxidation and that certain surface treatments which remove excess carbon from the SiC surface prior to oxidation reduce the Dit levels.[11,12] For the structures investigated in this study, pre-existing carbon clusters on the SiC free surface could explain the high positive charge detected in MOS structures with PECVD oxides studied in this paper.

Thermal treatments

Figure 6 includes Vfb shifts pre and post oxidation thermal treatments in wet ambient for the PECVD SiO_2 structures. The wet post oxidation anneals show significant and consistent positive charge reduction. It has been shown that wet oxidation or post oxidation annealing treatment in wet O_2 improves the oxide charge and interface states in 6H SiC.[13] Large negative Vfb shifts were observed in p-type 4H-SiC and 6H-SiC MOS structures with thermal oxide which, by using CV under UV illumination, were indisputably attributed to deep donor interface states.[14] The latter study showed that a wet post-oxidation anneal reduces the level of the positive charge in p-type

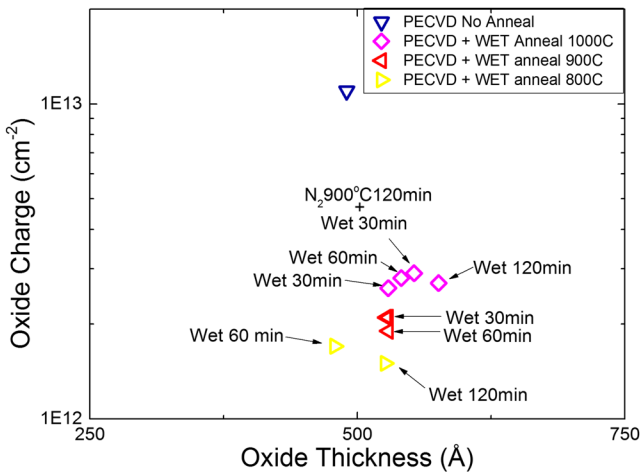


FIG. 6. Positive oxide charge density for the 3C-SiC MOS structures with PECVD SiO_2 pre and post deposition thermal annealing in wet ambient.

4H and 6H SiC but on n-type SiC this reduction is accompanied with an increase of negative charge.

In ref. 14, the large negative shift in p-type 4H-SiC reported together with a smaller negative shift in the n-type 4H-SiC fits very well with the Dit energy profile simply described in figure 5. The large negative shift seen in p-type 4H-SiC is due to empty deep donor states while for n-type 4H-SiC, a minimal level of donors or possibly even some acceptors are ionised due to the wider band gap of 4H-SiC. The observed Vfb shifts in p and n type 4H-SiC MOS structures in combination with their reduction by thermal treatment in wet oxygen ambient points towards interfaces states of similar nature in both 3C and 4H polytypes.

In more recent studies, wet post oxidation annealing treatments were shown to reduce the oxide positive charge in oxides thermally grown[8] and deposited by PECVD on 3C-SiC.[9] In Ref. 9, very low fixed positive charge density ($1.7x10^{11}$ cm^{-2}) was measured on free standing 3C-SiC with PECVD SiO_2 as opposed to $\sim 1x10^{12}$ cm^{-2} measured in 3C-SiC epitaxially grown on Si in the current study. In references 8, 9, the positive charge detected in SiO_2/3C-SiC MOS capacitors was considered independently from the interface states. The results reported in this paper seem to point to an ionised interface donor as the main origin of the fixed positive charge detected in these SiO_2/3C-SiC structures.

A closer look at the wet annealed samples (figure 6) shows that as the annealing temperature and duration increases a re-oxidation occurs which is associated with a more negative Vfb. Figure 7 shows the shift in Vfb as the annealing duration is increased for the samples annealed at 1000°C, a negative Vfb shift occurs along with an increase in oxide thickness. It must be pointed out that a constant positive charge level at the interface would also result in more negative Vfb shift if the oxide thickness increases. From the extracted density of charge (inset of figure 7), the positive charge variation is small and further annealing experiments (using more annealing durations) are needed to clarify whether the shift is caused solely by oxide thickness increase due to re-oxidation or more positive charges are generated and also contributing to the more negative Vfb. If the latter effect is the mechanism causing the observed Vfb shifts after long wet anneals, this means that during this anneal two competing effects are simultaneously occurring: the mechanism by which carbon is eliminated from the interface and the SiC oxidation which generates more carbon clusters. A successful strategy requires favouring the former over the latter.

The role of the wet post oxidation annealing treatment is still not very clear. The passivation of interface states using annealing in hydrogen even at high temperature didn't produce similar results to the SiO_2/Si system.[10] This suggests that the 3C-SiC interface states are not dominated by dangling bonds defects as it is the case for the SiO_2/Si system. The apparent reduction of the positive charge

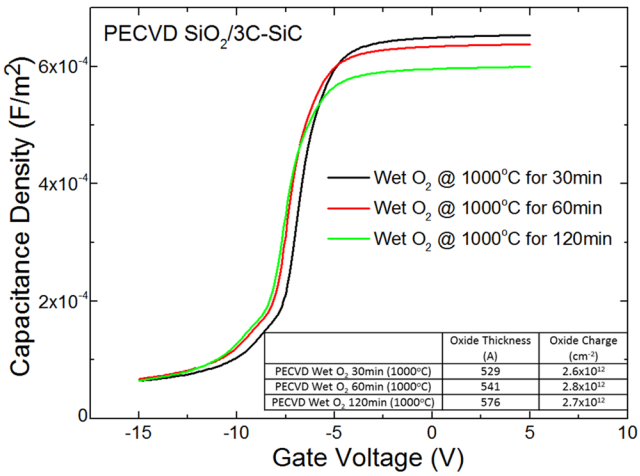


FIG. 7. Measured C-V characteristics of PECVD SiO_2/3C-SiC MOS structures after wet O_2 anneal @ 1000°C for different durations. The capacitance measurement frequency was 1MHz. The table shows the oxide thickness and oxide charge density extracted from the 1MHz C-V for each annealing condition.

at the interface could be either caused by a reduction in carbon clusters or a reconfiguration of these clusters which shifts their neutrality level downwards close to or below the Fermi level. If similar experiments were carried out on n-type and p-type 3C-SiC carbide structures with very different surface Fermi levels, it would first confirm the findings on n-type 3C-SiC MOS structures as the p-type C-V would see a Vfb shift corresponding to all ionised donors both in the band gap and conduction band, and more importantly, if a reconfiguration of C clusters after post thermal treatment is occurring with the interface states energy profile changing across the band gap and the conduction band, the n-type and p-type Vfb comparison would help to confirm this point. Unfortunately, this comparison is currently not possible due to the unavailability of p-type 3C-SiC/Si substrates.

It is important to note that previous studies reported significant improvements in carrier mobility after re-oxidation anneal in a wet ambient of 4H and 6H-SiC.[13–15] These mobility enhancements occurred in combination with a decrease in oxide charge and interface states density.[13,14] A more recent study investigated the effect of high temperature diluted-H_2 annealing on 6H and 4H-SiC interfaces and showed improvements in effective mobility of 6H-SiC MOSFETs and a reduction of interface traps in 4H-SiC.[16] However, the effects of the post oxidation anneals (wet or in diluted H_2) on the oxide and on the SiO_2/SiC interface are not fully understood.

The acceptor band predicted by the cluster model, and which could be responsible for the presence of negative charge at SiO2/4H-SiC interface, is neutral and located well above the conduction band minimum in 3C-SiC and therefore cannot be detected using the techniques employed in this study. Nevertheless, its effect on charge transport in 3C-SiC could be significant.

It must be emphasised that the level of oxide charge achieved in this work is still relatively high ($\sim 1 \times 10^{12}$ cm^{-2}) for MOS applications, especially compared to what has been previously published on free standing 3C-SiC.[9] More optimisation effort is required regarding the post oxidation annealing duration, temperature and ambient (e.g. partial pressures) and possibly more attention is needed towards surface preparation prior to the oxide deposition (oxidation) and the subsequent thermal treatments.

CONCLUSION

This study demonstrates by using a combination of thermal and deposited oxides that the positive charge observed in SiO_2/3C-SiC MOS structures mainly originates from positively charged donor interface state levels above the conduction band at the 3C-SiC surface. This work also shows that the density of positive charge could be reduced by post oxidation (or post deposition) wet annealing treatments in agreement with previous studies. The origin of the interface states and implications for other SiC polytypes was also discussed.

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