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Analysis and Design of Low Phase Noise CMOS Oscillator Circuit Topologies

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National University of Ireland, Cork

A thesis submitted for the degree of

DOCTOR OF PHILOSOPHY

Department of Electrical and Electronics Engineering

University College Cork

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Declaration

The submitted thesis is the candidate's own work and has not been submitted for another degree, either at University College Cork or elsewhere.

Ilias Chlis

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Last, I am thankful to Zuzanna Łojek, as well as to my family, for their patience and support.

Abstract

The research activity carried out during the PhD is focused on the study, analysis and design of millimeter-wave integrated oscillator circuits for high-speed wireless communications.

In Chapter 1 comparative analyses of phase noise (PN) in Hartley, Colpitts and common-source cross-coupled differential pair LC oscillator topologies are carried out under common conditions in 28 nm CMOS technology. The impulse sensitivity function (ISF) is used to carry out both qualitative and quantitative analyses of the phase noise exhibited by each circuit component in each circuit topology with oscillation frequency ranging from 1 to 100 GHz. The comparative analyses show the existence of four distinct frequency regions in which the three oscillator topologies rank unevenly in terms of best phase noise performance, due to the combined effects of device noise and circuit node sensitivity. Moreover, the analyses show that there is no superior oscillator topology in the absolute sense, but that the identification of the best circuit topology with respect to phase noise is strictly related to the operating frequency range.

In Chapter 2 comparative phase noise analyses of common-source cross-coupled pair, Colpitts, Hartley and Armstrong differential oscillator circuit topologies, designed in 28 nm bulk CMOS technology in a set of common conditions for operating frequencies in the range from 1 to 100 GHz, are carried out in order to identify their relative performance. The impulse sensitivity function is used to carry out qualitative and quantitative analyses of the noise contributions exhibited by each circuit component in each topology, allowing an understanding of their impact on phase noise. The comparative analyses show the existence of five distinct frequency regions in which the four topologies rank unevenly in terms of best phase noise performance. Moreover, the results obtained from the impulse sensitivity function show the impact of flicker noise contribution as the major effect leading to phase noise degradation in nano-scale CMOS LC oscillators.

Chapter 3 reports a phase noise analysis in a differential Armstrong oscillator circuit topology in CMOS technology. The analytical expressions of phase noise due to flicker and thermal noise sources are derived and validated by the results obtained through SpectreRF simulations for oscillation frequencies of 1, 10 and 100 GHz. The analysis captures well the phase noise of the oscillator topology and shows the impact of flicker noise contribution as the major effect leading to phase noise degradation in nano-scale CMOS LC oscillators.

Chapter 4 reports the analyses of three techniques for phase noise reduction in the CMOS Colpitts oscillator circuit topology. Namely, the three techniques are: inductive degeneration, noise filter, and optimum current density. The design of the circuit topology is carried out in 28 nm bulk CMOS technology. The analytical expression of the oscillation frequency is derived and validated through circuit simulations. Moreover, the theoretical analyses of the three techniques are carried out and verified by means of circuit simulations within a commercial design environment. The results obtained for the inductive degeneration and noise filter show the

existence of an optimum inductance for minimum phase noise. The results obtained for the optimum bias current density technique applied to a Colpitts oscillator circuit topology incorporating either inductive degeneration or noise filter, show the existence of an optimum bias current density for minimum phase noise. Overall, the analyses show that, with respect to the reference values obtained in Chapter 2, the adoption of these techniques may lead to a potential phase noise reduction up to 19 dB and 17 dB at a 1 MHz frequency offset for the oscillation frequencies of 10 GHz and 100 GHz respectively.

Chapter 5 reports the analyses of the three techniques discussed in Chapter 4, applied to the CMOS Hartley oscillator circuit topology. The design of the circuit topology is carried out in 28 nm bulk CMOS technology. The analytical expression of the oscillation frequency is derived and validated through circuit simulations. Moreover, the theoretical analyses of the three techniques are carried out and verified by means of circuit simulations. As in the case of the Colpitts topology, the results obtained for the inductive degeneration and noise filter show the existence of an optimum inductance for minimum phase noise. The results obtained for the optimum bias current density technique applied to a Hartley oscillator circuit topology incorporating either inductive degeneration or noise filter, show the existence of an optimum bias current density for minimum phase noise. Overall, wih respect to the reference values obtained in Chapter 2, the analyses show that the adoption of these techniques may lead to a potential phase noise reduction up to 17 dB and 16 dB at a 1 MHz frequency offset for the oscillation frequencies of 10 GHz and 100 GHz respectively, with respect to the traditional Hartley topology.

Finally, Chapter 6 reports the design of an advanced solution, adopting the techniques discussed in Chapters 4 and 5. The voltage-controlled oscillator (VCO) topology can be tuned from 58.1 GHz to 63.3 GHz. From periodic steady state (PSS) and periodic noise (Pnoise) SpectreRF simulations the best phase noise performance is observed for f_0=63.3 GHz, and amounts to -100.2 dBc/Hz at a 1 MHz frequency offset from the oscillation frequency, for a power consumption of 13.6 mW. This corresponds to a figure of merit (FOM) of 185 dB.

Preface

The recent advances in silicon technologies allow us to implement integrated transceivers operating at the millimeter-waves, enabling the realization of a new class of mass-market devices for very high data rate wireless communications, such as 60 GHz uncompressed wireless video communications. In spite of some encouraging results in transceiver integration, system-level studies reported in the literature have emphasized the need of building-blocks with superior performance in order to overcome the main limitations for an efficient system-on-chip implementation of the overall transceivers.

In particular, oscillator phase noise (PN) is one of the main bottlenecks for the information capacity of communication systems, leading to severe challenges in the design of local oscillators, especially at very high frequencies. However, no complete comparative studies have been carried out on how to choose the oscillator circuit topology that could potentially offer the best performance in terms of phase noise for the range of operating frequencies of modern telecommunication systems. Usually, thanks to its reliable start-up, the common-source cross-coupled differential pair topology is chosen a priori without any further considerations.

On the basis of the above motivations, the research activity carried out during the PhD dealt with this open question not addressed by the literature. The investigations could allow us to extend the range of possibilities beyond the common practice of choosing the common-source cross-coupled differential pair topology, traditionally selected for its reliable start-up, but without further topological considerations.

The PhD thesis is organized in six chapters. The presentation order follows the thesis schedule.

Chapter 1 reports a comparative analysis in terms of phase noise performance of the single-ended Colpitts, single-ended Hartley and common-source cross-coupled topogogies, under common conditions, for a discrete set of operating frequencies from 1 to 100 GHz.

Chapter 2 extends the comparative analysis of phase noise carried out in Chapter 1 to the Colpitts, Hartley and Armstrong differential oscillator topologies.

Chapter 3 addresses a complete analytical study of phase noise in the differential Armstrong topology, with the objective of providing a closed-form symbolic expression for the phase noise in both the $1/f^3$ and $1/f^2$ regions, by using the impulse sensitivity function (ISF).

Chapter 4 reports the analysis and design of three techniques for phase noise reduction in a single-ended Colpitts oscillator circuit topology. In particular, the techniques of inductive degeneration, noise filter and optimum current density.

In Chapter 5 the techniques discussed in Chapter 4 are applied and analysed for the design of a single-ended Hartley oscillator circuit topology.

Finally, Chapter 6 presents a novel differential Colpitts voltage-controlled oscillator (VCO) topology adopting the techniques of phase noise reduction discussed in Chapters 4 and 5.

The original contributions of this PhD thesis to the state of the art are referred with the label OP (e.g. [OP1]), and reported in the List of Publications.

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Chapter 1

Colpitts, Hartley and Common-Source Cross-Coupled Topologies

1.1 Introduction

Oscillator phase noise (PN) is one of the main bottlenecks for the information capacity of communication systems, leading to severe challenges in the design of local oscillators in silicon technologies, especially at very high frequency [1-5]. In particular, the main difficulties are to achieve a high quality factor LC tank [6-11] and consume a reasonable power [12-13].

Oscillator phase noise has been studied extensively over the last decades [14-17]. Most of these studies are based on linear time-invariant (LTI) oscillator models, which provide important qualitative design insights, but are limited in the quantitative prediction of the power spectral density levels [18], in some cases addressed by adopting nonlinear approaches [19].

The linear time-variant (LTV) oscillator model allows a quantitative understanding of oscillator phase noise through the Impulse Sensitivity Function (ISF), represented as $\Gamma(x)$ [18]. Since the oscillator is assumed as a linear time-varying circuit, the phase sensitivity to noise perturbations can be described in terms of its (time-varying) impulse response.

The evaluation of the ISF involves a significant amount of transient simulations and data extractions, resulting in time consuming calculations, potentially prone to inaccuracy. Recently, new efficient frequency-domain methods operating directly in the steady-state were proposed [20, 21], allowing a consistent reduction of the simulation workload. Regardless of the methods, the analysis of the phase sensitivity can contribute significantly to a better understanding of the impact of noise sources to the oscillator phase noise in the most widespread circuit topologies.

A comparative analysis of common-source cross-coupled differential pair and differential Colpitts LC oscillators in 0.35 μm CMOS technology at 2.9 GHz was carried in [22], showing the superior performance of the cross-coupled differential topology. In this perspective, it could be interesting to extend the comparison also to other topologies, technology nodes and oscillation frequencies.

This chapter reports a comparative study of phase noise for the three oscillator topologies: Hartley, Colpitts and common-source cross-coupled differential pair circuit topologies in 28 nm CMOS technology. The results of the analyses show interesting aspects not addressed by the literature. In detail, all the steps for an accurate derivation of the ISF are summarized and the phase noise predictions for a wide set of amplitudes of the injected current pulse are compared with the results obtained by the direct plots obtained by means of SpectreRF-Cadence Periodic Steady State (PSS) analysis. The contributions from each noise source to the overall phase noise are evaluated qualitatively and quantitatively through the ISF for each topology operating in a discrete set of frequencies from 1 to 100 GHz.

The chapter is organized as follows. Section 1.2 reports the design of the three oscillator topologies in 28 nm CMOS technology. Section 1.3 summarizes the key analytical expressions for phase noise predictions through the ISF, the key steps and settings for accurate evaluations, and finally reports the results for the oscillation frequency of 10 GHz. In Section 1.4, qualitative and quantitative analyses of the phase noise contributed by each circuit component are carried out for each topology for a discrete set of oscillation frequencies ranging from 1 to 100 GHz. Section 1.5 reports the results that reveal the existence of four different frequency regions in which the best phase noise performance is given case by case by a different topology. In Section 1.6, the conclusions are drawn.

The key contents of this chapter have been reported in original contributions published in an international peer-reviewed journal and in conference proceedings [OP1, OP6].

1.2 Circuit Topologies

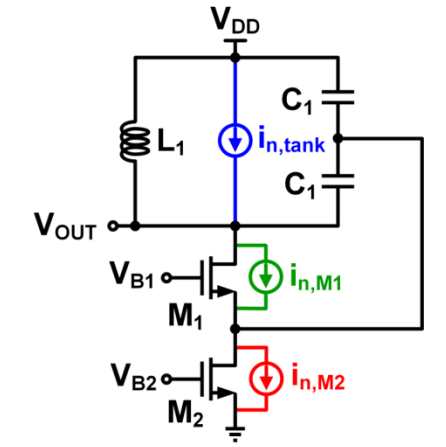
Three LC oscillator topologies have been analysed: single-ended Colpitts, single-ended Hartley and top-biased common-source cross-coupled differential pair oscillator topologies, as shown in Fig. 1.1. The three oscillator circuit topologies have been implemented in 28 nm bulk CMOS technology by ST-Microelectronics by adopting the same criteria for a fair comparison as follows. The frequency of operation is 10 GHz. The sizes of the transistors and the value of the inductors and capacitors used are reported in Table 1.1. Despite this work is addressed to the investigations of the circuit topologies as such, rather than the circuit design and implementation, i.e. regardless of the effects of parasitic components, we considered a reasonable quality factor for the LC tank in order to carry out the comparative study of the properties of each circuit topology under the same typical conditions. Thereby, a quality factor (Q) equal to 10 has been assumed for the inductors, considering a parasitic resistance in series with the inductor, whereas the capacitors have been considered as ideal devices. In all cases the power consumption is 6.3 mW.

A small signal noise analysis by SpectreRF was used for the derivation of the flicker noise corner of each transistor. Assuming that the power spectral density (PSD) of the thermal and flicker noise currents generated by the transistor in the saturation region are given by equations (1.1) and (1.2) respectively, the flicker noise corner is given by equation (1.3) [23].

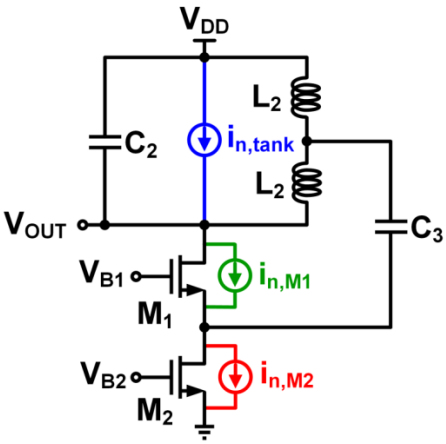
$$S_{iw} = 4kT\gamma g_m \tag{1.1}$$

$$S_{if} = g_m{}^2 \frac{k_f}{WLC_{ox}} \frac{1}{f^c} \tag{1.2}$$

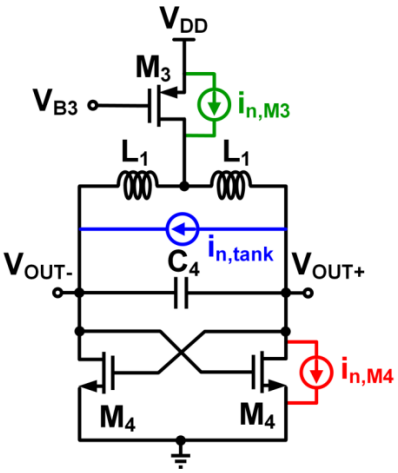
$$f_{1/f} = \sqrt[c]{\frac{k_f}{WLC_{ox}} \frac{g_m}{4kT\gamma}} \tag{1.3}$$



(a)



(b)



(c)

Fig. 1.1. Schematic of the oscillator circuit topologies: (a) single-ended Colpitts; (b) single-ended Hartley; (c) top-biased common-source cross-coupled differential pair. V_{B1}, V_{B2} and V_{B3} are DC bias voltages.

Table 1.1. Device Sizing.

Transistor Width [μm]				Capacitor value [pF]				Inductor value [pH]	
M_1	M_2	M_3	M_4	C_1	C_2	C_3	C_4	L_1	L_2
30	30	30	15	0.97	0.495	0.8	0.229	500	250

where k_f is a bias-dependent constant, c is a constant with typical values ranging from 0.7 to 1.2, C_{ox} is the oxide capacitance per unit area and γ is the excess noise coefficient. For the 28 nm bulk CMOS technology adopted, the thickness of the oxide t_{ox} is about 1.4 nm for the n-MOSFET and 1.7 nm for the p-MOSFET, from which we can derive that C_{ox} is about 0.026 and 0.02 F/m^2, respectively. The values of k_f, $f_{1/f}$ and c have been derived by means of noise simulation of each single stand-alone transistor of Table 1.1. They are reported in Table 1.2.

Table 1.2. Impulse Sensitivity Function.

Transistor	k_f (V^{2}F)	$f_{1/f}$ (MHz)	c
M_1	1.09×10^{-22}	1390	0.9
M_2	2.26×10^{-23}	870	0.9
M_3	1.88×10^{-23}	1100	0.93
M_4	1.25×10^{-22}	1430	0.9

1.3 Impulse Sensitivity Function

In order to get an insight of the noise contribution of each circuit component in each circuit topology, hereinafter we make use of the ISF as a predictive tool for quantitative and qualitative phase noise evaluations.

A detailed procedure for computation of the ISF and phase noise prediction in a linear time-varying system in the case of a source-coupled CMOS multi-vibrator with operating frequency up to 2 MHz was presented in [24]. All the results were achieved only for a single amplitude value of the injected pulse. However, the time-domain evaluation of the ISF involves a number of transient simulations, resulting potentially prone to inaccuracy. Thereby, it is worth consolidating all the steps in order to achieve accurate results.

The impulse response from each current noise source to the oscillator output phase can be written as [18]:

$$h_\phi(t,\tau)=\frac{\Gamma(\omega_0\tau)}{q_{\max}}u(t-\tau) \tag{1.4}$$

where q_{max} is the charge injected into a specific circuit node of the oscillator at time t=τ, u(t) is the unity step function and $\Gamma(\omega_0\tau)$ is a dimensionless periodic function that can be expressed as a Fourier series [18]:

$$\Gamma(\omega_0\tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos\left(n\omega_0\tau + \theta_n\right) \tag{1.5}$$

The DC and root mean square (rms) values of $\Gamma(\omega_0\tau)$ are given by the following two equations [18]:

$$\Gamma_{DC} = \frac{c_0}{2} \tag{1.6}$$

$$\Gamma_{rms} = \sqrt{\frac{1}{2}\sum_{n=0}^{\infty} c_n^2} \tag{1.7}$$

The thermal noise contribution to the phase noise spectrum for any oscillator, this last traditionally indicated with $\mathcal{L}$, from each given noise source with a white power spectral density, can be expressed as [18]

$$\mathcal{L}\{\Delta\omega\}\Big|_{flicker} = \frac{\Gamma_{rms}^2}{q_{max}^2}\frac{\left(\frac{\overline{i_n^2}}{\Delta f}\right)}{2\Delta\omega^2} \tag{1.8}$$

where q_{max} is the charge injected into a circuit node by the noise source insisting in that node and $\Delta\omega$ is the offset from the oscillation angular frequency. Therein [18], it is tacitly assumed that c in equation (1.2) is equal to 1, regardless of the technology node. This assumption leads to the above relatively rough but simple equation (1.8).

The flicker noise contribution to the phase noise spectrum for any oscillator, from each given noise source with a 1/f spectrum can be expressed as follows [18], where $\omega_{1/f}$ is the flicker noise corner of the device

$$\mathcal{L}\{\Delta\omega\}\Big|_{thermal} = \frac{c_0^2}{q_{max}^2}\frac{\left(\frac{\overline{i_n^2}}{\Delta f}\right)}{8\Delta\omega^2}\frac{\omega_{1/f}}{\Delta\omega} \tag{1.9}$$

1.3.1 Simulation Steps and Settings

All the simulations have been carried out by using the SpectreRF simulator in the Cadence design environment. The ISF of the oscillator topologies has been evaluated for an oscillation frequency of 10 GHz, which will be considered hereinafter as a reference for all the other cases. First we run a transient simulation in order to observe and record when the amplitude of the oscillation waveform reaches the steady state regime. In our case, this occurs with large margins after 5 ns. Afterwards, we perform other transient simulations applying current impulsive sources acting in parallel with the actual inherent current noise sources of the LC tank and transistors, by

activating only one noise source at one time. The current impulses are set to occur in the steady state regime starting from a given time reference for the unperturbed solution. The pulse width of each current source has been chosen equal to 1 ps (i.e. one hundredth of the oscillation period) with 0.1 ps rise and fall time, as shown in Fig. 1.2.

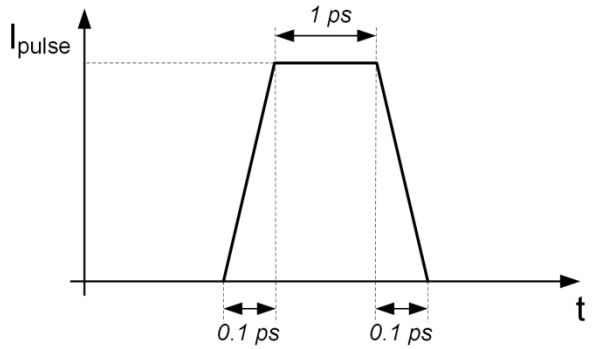


Fig. 1.2. The injected current pulse.

The simulation has been repeated for amplitudes of the injected current of 1, 10, 100 μA and 1, 10 mA. Each transient analysis is performed using the conservative mode and a maximum time step of 10 fs (i.e. one 10-thousandth of the oscillation period), in order to have a good accuracy even in the case of the smallest injected current pulse (i.e. 1 μA). The charge q_{max} injected in each node corresponds to the area under each pulse, i.e. the area of the trapezoid, of Fig. 1.2.

$$q_{\max} = I_{pulse} \times 1.1 \times 10^{-12} \text{ Coulombs} \tag{1.10}$$

where I_{pulse} is the amplitude value of each source pulse. This is repeated for all the N noise sources connected in parallel, for all the M instants of time over one period of oscillation, where N=3 and M=40, in our case. The time instants have been chosen to be equally spaced in an oscillation period. The time shift caused by the impulse injection can be extracted by comparing the perturbed and unperturbed waveforms. This means that when the oscillation has reached the steady state regime, the time shift Δt_i of the zero-crossing instant of the perturbed oscillation with respect to the unperturbed one, i.e. when no impulse is applied, is calculated as shown in Fig. 1.3.

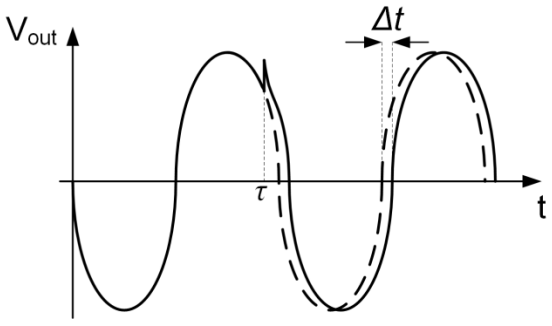


Fig. 1.3. Time shift Δt caused by the impulse injection occurring at the time τ.

Then, these time shifts are converted into phase shifts by using the following relation

$$\Gamma\left(x=\omega_0 t\right)=2\pi\frac{\Delta t_i\left(t\right)}{T} \tag{1.11}$$

In order to take into account the cyclostationary nature of the active device noise sources, Γ(x) is multiplied with α(x), where α(x) is the absolute value of the unperturbed current flowing in the respective node in which the impulses are injected, and at the same time instant in which they are injected, normalized to its maximum value in the period. Then, the DC and root mean square (rms) components of the product Γ(x)×α(x) can be calculated as follows

$$\Gamma_{DC}=\frac{\sum_{i=1}^{40}\left[\Gamma\left(x\right)\alpha(x)\right]}{40} \tag{1.12}$$

$$\Gamma_{rms}=\sqrt{\frac{\sum_{i=1}^{40}\left\{\left[\Gamma\left(x\right)\alpha(x)\right]^2\right\}}{40}} \tag{1.13}$$

Finally, the total phase noise of the oscillator is computed by adding the contributions from all the noise sources acting in the circuit, according to (1.8) and (1.9). In particular, the active devices inject noise to the terms responsible for both flicker and thermal noise contributions to the oscillator phase noise, whereas the LC tank participates only to the thermal noise contribution to phase noise. Equation (1.14) gives the total phase noise for each of the three oscillators, where m is the number of transistors of the oscillator circuit. The first sum in (1.14) describes the phase noise contribution from the thermal noise. As a result, it contains an additional term (m+1), due to thermal noise coming from the LC tank.

$$\mathcal{L}\left\{\Delta\omega\right\}\Big|_{total}=10\log\left\{\sum_{i=1}^{m+1}\left[\frac{\Gamma_{rms}{}^2}{q_{\max}{}^2}\frac{\left(\frac{\overline{i_n^{\,2}}}{\Delta f}\right)_i}{2\Delta\omega^2}\right]+\sum_{i=1}^{m}\left[\frac{\Gamma_{DC}{}^2}{q_{\max}{}^2}\frac{\left(\frac{\overline{i_n^{\,2}}}{\Delta f}\right)_i}{8\Delta\omega^2}\frac{\left(\omega_{1/f}\right)_i}{\Delta\omega}\right]\right\} \tag{14}$$

1.3.2 Results

Fig. 1.4 reports Γ(x)×α(x) for an injected current pulse amplitude of 1 μA versus the phase for the injected noise sources, during one oscillation period, for the three oscillator circuit topologies.

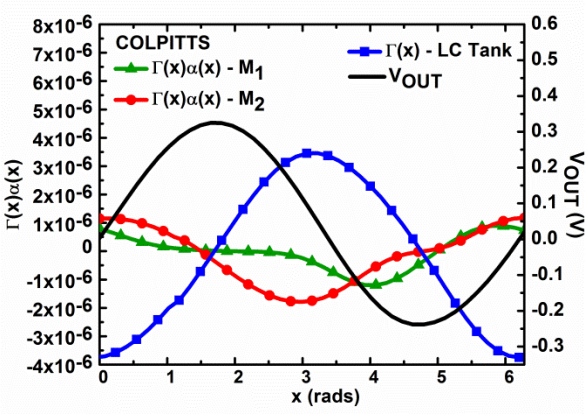
Fig. 1.5 reports the comparison between the phase noise obtained through the ISF and the phase noise obtained by direct plots from PSS and periodic noise simulations, for the three

oscillator circuit topologies. Note that the phase noise predicted by the ISF is very close to the values obtained by means of SpectreRF simulations. Table 1.3 provides the phase noise results for all the current impulse amplitude values, for a 1 MHz frequency offset from the carrier.

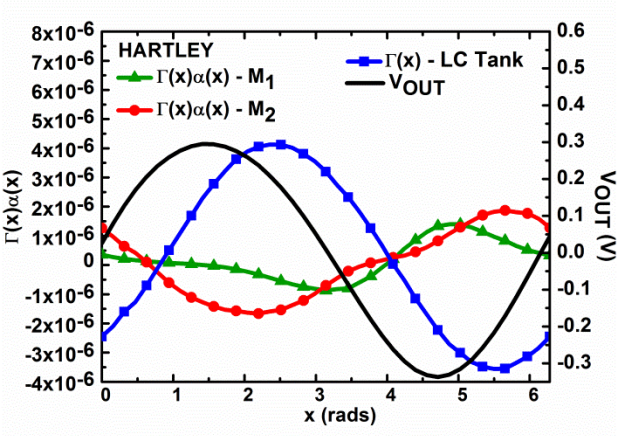
Table 1.3. Summary of the PN results obtained by SpectreRF and ISF.

PN [dBc/Hz] @ 1 MHz frequency offset						
Topology	**SpectreRF**	**ISF**				
		1 μA	10 μA	100 μA	1 mA	10 mA
Colpitts	-96.25	-96.20	-98.33	-98.49	-98.50	-98.45
Hartley	-92.75	-92.79	-95.18	-94.36	-94.85	-95.29
Cross-coupled	-102.66	-102.69	-102.84	-102.83	-102.84	-102.94

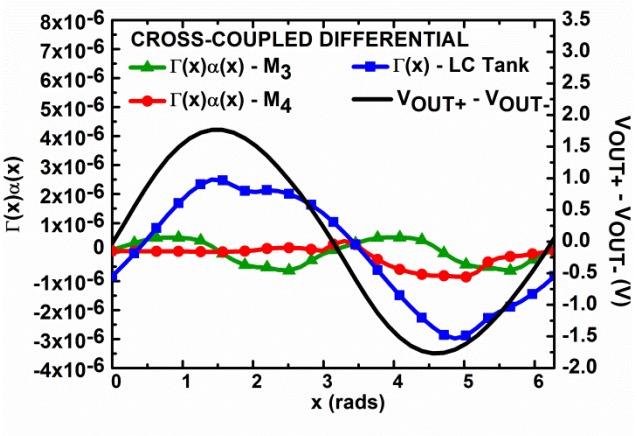
Note that for this oscillation frequency (10 GHz) the phase noise of the common-source cross-coupled differential pair topology is lower to the phase noise of the Colpitts topology, in agreement with [22], and that the phase noise of Colpitts is lower to the phase noise exhibited by the Hartley topology. Moreover, note that the agreement degrades for higher pulse amplitudes, when the current-to-phase transfer function starts becoming nonlinear. The amplitude in which this occurs is slightly different for each oscillator topology, but for the injected current impulse of 1 μA, the difference between the phase noise predicted by the ISF method and the one given by PSS and periodic noise (Pnoise) analysis is lower than 1 % at a 1 MHz frequency offset.



(a)

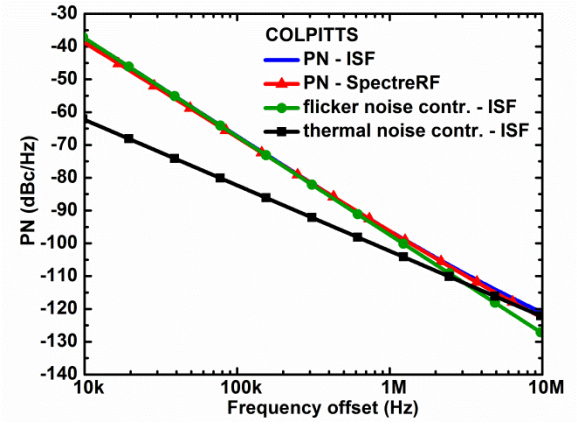


(b)

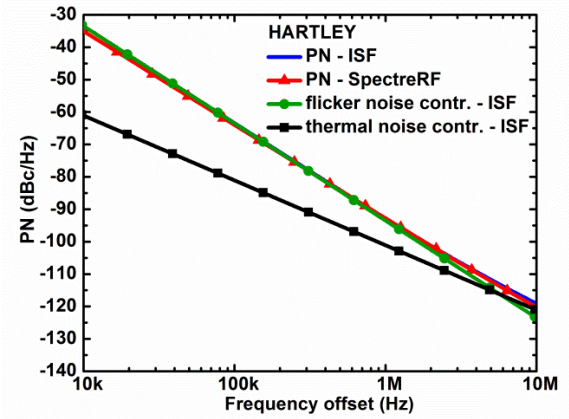


(c)

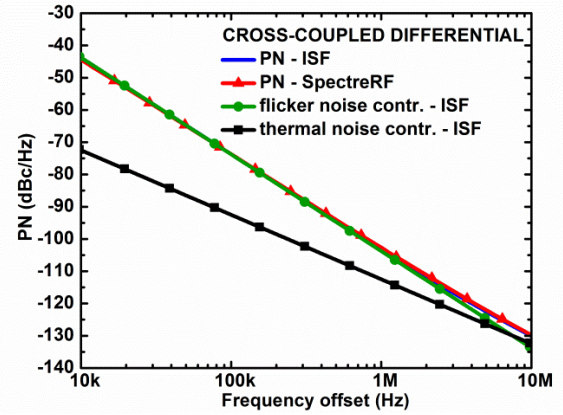
Fig. 1.4. Γ(x)×α(x) of the MOSFETs and Γ(x) of the LC tank vs. phase for a 1 μA amplitude current impulse, for the oscillation frequency of 10 GHz: (a) Colpitts topology; (b) Hartley topology; (c) Common-source cross-coupled differential pair topology.



(a)



(b)



(c)

Fig. 1.5. PN vs. frequency offset for the three oscillator circuit topologies, obtained through the ISF for a 1 μA current impulse and direct plot from PSS and periodic noise (PN) SpectreRF simulations, for the oscillation frequency of 10 GHz. The flicker and thermal noise contributions to the overall PN are also plotted in order to identify the $1/f^3$ PN frequency corner. (a) Colpitts. The $1/f^3$ PN corner is at the frequency offset of 3.1 MHz. (b) Hartley. The $1/f^3$ PN corner is at the frequency offset of 5.7 MHz. (c) Common-source cross-coupled differential pair. The $1/f^3$ PN corner is at the frequency offset of 7.5 MHz.

1.4 Analyses and Comparison versus Oscillation Frequency

The investigations through the ISF can provide a better understanding of the phase noise in each oscillator topology. In order to be able to extract further useful considerations about the devices and topologies, the previous analyses have been reiterated also for other oscillation frequencies. In detail, the three oscillator topologies have been implemented also for 1 and 100 GHz operations, by keeping the quality factor of 10 for the LC tank and preserving the same power consumption of 6.3 mW as in the case of the 10 GHz oscillation frequency. The transistor sizes were also kept the same as in the previous case. As a consequence of the results reported in the previous section, we injected noise current impulses with amplitude of 1 μA.

Table 1.4 reports the values of the individual circuit components for the topologies of Fig. 1.1, used for the oscillation frequencies of 1 and 100 GHz.

Table 1.4. Device Sizing for Oscillation Frequencies of 1 and 100 GHz.

	Transistor Width [μm]				**Capacitor value [pF]**					**Inductor value [pH]**	
Frequency [GHz]	M_1	M_2	M_3	M_4	C_1	C_2	C_3	C_4	C_5	L_1	L_2
1	30	30	30	15	10	10^5	5	10	2.5	5×10^3	2.5×10^3
100	30	30	30	15	0.0515	10^5	0.023	0.1	0.0057	50	25

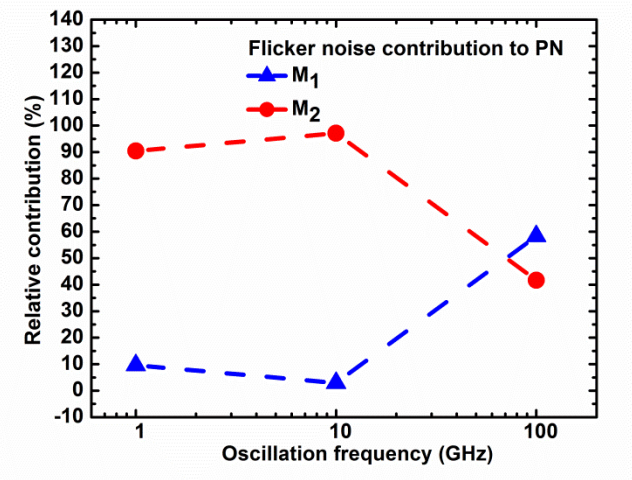
Table 1.5 reports the phase noise values at a 1 MHz offset predicted by the ISF along with the values obtained by means of SpectreRF simulations for the oscillation frequencies of 1 and 100 GHz.

Table 1.5. Summary of the PN Results Obtained by SpectreRF and ISF.

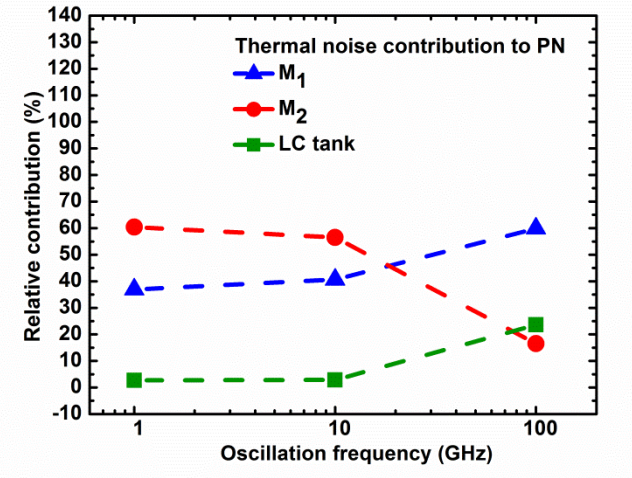
PN [dBc/Hz] @ 1 MHz frequency offset				
Topology	**1 GHz**		**100 GHz**	
	Spectre RF	ISF (1 μA)	Spectre RF	ISF (1 μA)
Colpitts	-115.31	-116	-77.06	-77.69
Hartley	-114.52	-114.85	-81.18	-81.38
Cross-coupled	-123.7	-124.06	-74.78	-75.59

Fig. 1.6 reports the relative contributions of M_1, M_2 and LC tank to the overall phase noise versus the oscillation frequency for the Colpitts topology, in both the flicker and thermal noise contributions to phase noise.

Figs. 1.7 and 1.8 report the results for the Hartley and common-source cross-coupled differential pair topologies, respectively.

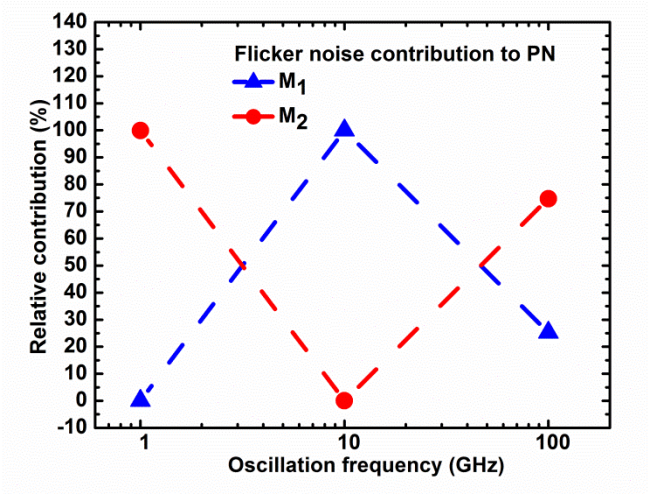


(a)

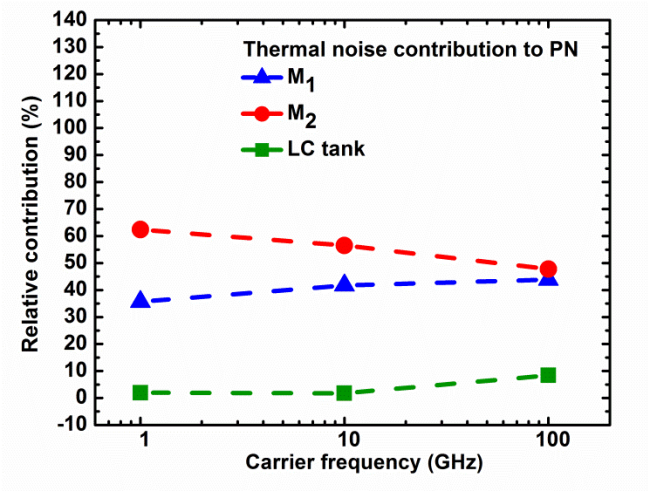


(b)

Fig. 1.6. Relative contributions of M_1, M_2 and the LC tank for the Colpitts topology vs. oscillation frequency @ 1 MHz offset. (a) flicker noise contribution to PN. (b) thermal noise contribution to PN.

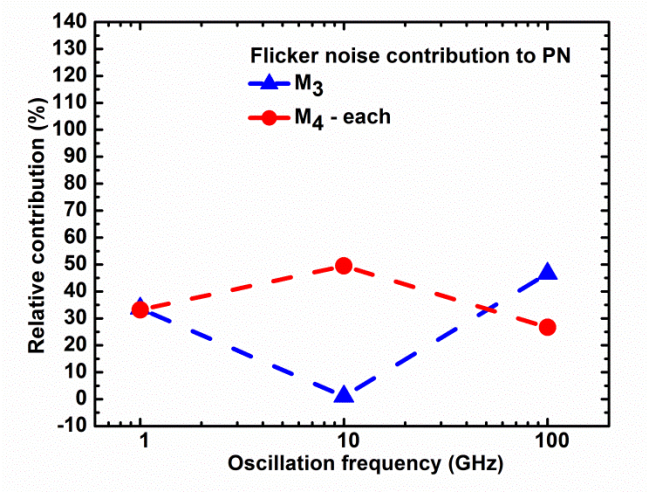


(a)

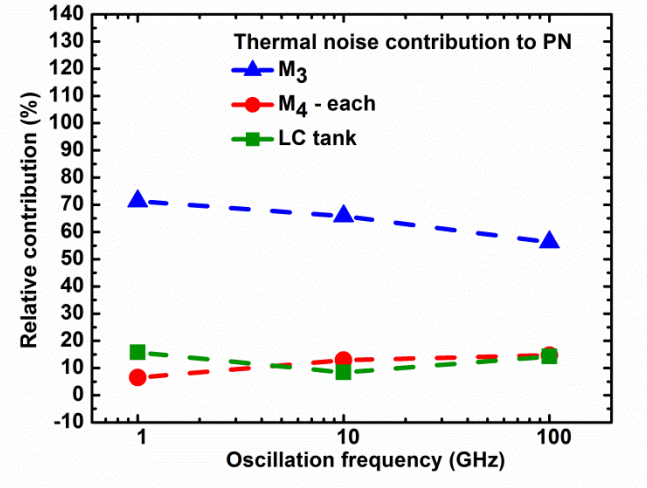


(b)

Fig. 1.7. Relative contributions of M_1, M_2 and the LC tank for the Hartley topology vs. oscillation frequency @ 1 MHz offset. (a) flicker noise contribution to PN. (b) thermal noise contribution to PN.



(a)



(b)

Fig. 1.8. Relative contributions of M_3, M_4 and the LC tank for the common-source cross-coupled differential pair topology vs. frequency of oscillation @ 1 MHz offset. (a) flicker noise contribution to PN. (b) thermal noise contribution to PN.

1.4.1 Comparative Analysis between Devices

The relative contributions to the overall current flicker and thermal noise from MOSFETs and LC tank of the three oscillator topologies are summarized in Table 1.6, as well as the values of Γ_{DC} and Γ_{rms} calculated for the 1 μA injected noise source.

Table 1.6. Γ_{DC}, Γ_{rms} and Relative Noise Contributions for a 1 μA Injected Noise Source @ 1 MHz offset.

Colpitts	Contribution to total flicker noise (%)	Contribution to total thermal noise (%)	Γ_{DC}			Γ_{rms}		
Oscillation freq.			1 GHz	10 GHz	100 GHz	1 GHz	10 GHz	100GHz
M_1	76.88	67.18	3.8×10^{-8}	-2.0×10^{-8}	5.4×10^{-7}	5.9×10^{-7}	5.9×10^{-7}	1.1×10^{-6}
M_2	23.1	32.27	-2.0×10^{-7}	-2.0×10^{-7}	9.9×10^{-8}	1.1×10^{-6}	1.0×10^{-6}	7.9×10^{-7}
LC tank		0.55				2.6×10^{-6}	1.8×10^{-6}	6.9×10^{-6}
Hartley	Contribution to total flicker noise (%)	Contribution to total thermal noise (%)	Γ_{DC}			Γ_{rms}		
Oscillation freq.			1 GHz	10 GHz	100 GHz	1 GHz	10 GHz	100GHz
M_1	76.88	67.18	-4.3×10^{-9}	1.9×10^{-7}	1.5×10^{-7}	6.1×10^{-7}	7.0×10^{-7}	5.4×10^{-7}
M_2	23.1	32.27	-3.0×10^{-7}	-4.1×10^{-9}	-3.0×10^{-7}	1.1×10^{-6}	1.2×10^{-6}	6.4×10^{-7}
LC tank		0.55				2.5×10^{-6}	2.7×10^{-6}	2.0×10^{-6}
Cross-coupled	Contribution to total flicker noise (%)	Contribution to total thermal noise (%)	Γ_{DC}			Γ_{rms}		
Oscillation freq.			1 GHz	10 GHz	100 GHz	1 GHz	10 GHz	100 GHz
M_3	20.60	26.47	-3.3×10^{-8}	-1.5×10^{-8}	3.3×10^{-7}	4.5×10^{-7}	4.1×10^{-7}	6.7×10^{-7}
M_4	39.7 - each	30.70 - each	4.6×10^{-8}	-1.5×10^{-7}	2.0×10^{-7}	2.7×10^{-7}	3.7×10^{-7}	6.7×10^{-7}
LC tank		12.13				1.8×10^{-6}	1.8×10^{-6}	2.9×10^{-6}

These results stimulate some careful evaluations about the noise contributions of each device in each oscillator topology at different oscillation frequencies.

To do this, we could refer again to equations (1.8), (1.9) and (1.14) and consider preliminarily that the amount of flicker or thermal noise of the transistor in a certain region of operation does not determine exclusively the flicker or thermal noise contribution to the oscillator phase noise, as reported in [18]. In particular, we can observe that for a given q_{max} (1.10) and a given frequency offset $\Delta\omega=2\pi\times10^6$, the amount of flicker noise contribution to phase noise is proportional to the product of the transistor flicker noise and Γ_{DC}^2

$$\mathcal{L}\{\Delta\omega\}\Big|_{flicker} \propto \sum_{i=1}^{m}\left\{\Gamma_{DC}^2\left[\left(\frac{\overline{i_n^2}}{\Delta f}\right)\frac{\omega_{1/f}}{\Delta\omega}\right]\right\} \tag{1.15}$$

whereas, the amount of thermal noise contribution to phase noise is proportional to the product of the thermal noise of the transistor and LC tank, and their respective Γ_{rms}^2

$$\mathcal{L}\{\Delta\omega\}\Big|_{thermal} \propto \sum_{i=1}^{m+1}\left\{\Gamma_{rms}^2\left(\frac{\overline{i_n^2}}{\Delta f}\right)\right\} \tag{1.16}$$

In other words, the flicker noise is weighted by Γ_{DC}^2 whereas the thermal noise is weighted by Γ_{rms}^2, as mentioned in [18]. On the other hand, Γ_{DC} and Γ_{rms} do not depend on the device noise sources, but on the node in which the noise current is injected in a circuit topology.

Considering these aspects it is worth highlighting the following observations on the above results.

In the Colpitts topology, we observe from Fig. 1.6 (a) and Table 1.6 that for oscillation frequencies higher than about 70 GHz, transistor M_1 dominates the flicker noise contribution to PN. However, M_2 dominates at frequencies lower than 70 GHz, despite M_2 generates a lower flicker noise than M_1. This is due to the fact that, according to Table 1.6, the absolute value of Γ_{DC} for M_2 is larger than Γ_{DC} for M_1 at low frequencies of oscillation. In other terms, this means that the oscillation waveform at the node (drain node of M_2) into which the noise current is injected is less symmetrical with respect to the rise and fall times [18]. Regarding the thermal noise contribution to phase noise, shown in Fig. 1.6 (b), at oscillation frequencies above 20 GHz, M_1 has the major phase noise contribution. However, below 20 GHz, M_2 has a higher Γ_{rms} than M_1, as shown in Table 1.6. As a result, despite according to Table 1.6 the thermal noise contribution of M_2 is half that of M_1, it takes a larger portion of the thermal noise contribution to PN at oscillation frequencies below 20 GHz.

As for the Hartley oscillator topology, we observe from Fig. 1.7 (a) that at oscillation frequencies between 3 and 50 GHz, transistor M_1 dominates the flicker noise contribution to phase noise. Nonetheless, in lower and higher oscillation frequencies, M_2 dominates, despite its lower flicker noise with respect to M_1 as shown in Table 1.6, since its contribution is characterized by a higher absolute value of Γ_{DC}, as again shown in Table 1.6. In the thermal noise contribution to phase noise reported in Fig. 1.7 (b), M_2 presents the major contribution, because, from Table 1.6 M_2 has a higher Γ_{rms} than M_1. As a result, despite according to Table 1.6 the thermal noise contribution of M_2 is half that of M_1, it takes a larger portion of the thermal noise contribution to phase noise.

As for the common-source cross-coupled differential pair oscillator topology, we see in Fig. 1.8 (a), that the pair of n-MOSFETs M_4, at frequencies lower than 50 GHz, is responsible for most of the flicker noise contribution to phase noise, as not only generates more flicker noise, but also has a higher absolute value of Γ_{DC} than M_3 (see Table 1.6). After 50 GHz, the contribution of M_3 increases due to its higher Γ_{DC} value and surpasses that of M_4, even though M_4 generates a higher flicker noise. With respect to the behavior of the thermal noise contribution to phase noise seen in Fig. 1.8 (b), the relative contribution from the current source M_3 gradually drops with increasing oscillation frequencies, whereas M_4 follows an opposite trend.

Moreover, from Figs. 1.6 (b) and 1.7 (b), we note that in the Colpitts and Hartley topologies, the LC tank occupies at lower oscillation frequencies a small portion of the contribution of thermal noise to phase noise graph, because, as Table 1.6 indicates, the thermal noise generated

by the LC tank is at least one order of magnitude below the thermal noise generated by the transistors in each case. However, both in Colpitts and Hartley, the contribution of the LC tank increases at higher oscillation frequencies where Table 1.6 indicates that Γ_{rms} of the tank is notably larger than Γ_{rms} of both devices.

On the other hand, from Figs. 1.6 (b), 1.7 (b) and 1.8 (b) we note that in all three oscillator topologies, the relative contribution of the current sources M_2 and M_3 to the thermal noise contribution to phase noise drops at higher oscillation frequencies. According to Table 1.6, this is due to the reduction of the Γ_{rms} for the current sources relative to the Γ_{rms} values for the other oscillator components.

1.4.2 Comparative Analysis between Topologies

By using the values in Table 1.6 along with the equations (1.15) and (1.16), we can determine the flicker and thermal noise contributions obtained by the ISF for a 1 μA injected current source, as reported in Table 1.7.

Table 1.7. Noise Contributions @ 1 MHz Frequency Offset for a 1 μA Injected Noise Current.

Colpitts	$\Gamma_{DC}^2\left[\left(\frac{\overline{i_n^2}}{\Delta f}\right)\frac{\omega_{1/f}}{\Delta\omega}\right]$			$\Gamma_{rms}^2\left(\frac{\overline{i_n^2}}{\Delta f}\right)$		
Oscillation freq.	1 GHz	10 GHz	100 GHz	1 GHz	10 GHz	100 GHz
M_1	6.8×10^{-33}	2.0×10^{-33}	4.2×10^{-32}	2.2×10^{-33}	2.3×10^{-33}	3.3×10^{-33}
M_2	6.4×10^{-32}	6.7×10^{-32}	3.0×10^{-32}	3.6×10^{-33}	3.2×10^{-33}	9.1×10^{-34}
LC tank				1.6×10^{-34}	1.6×10^{-34}	1.3×10^{-33}
Total (Σ)	7.1×10^{-32}	6.9×10^{-32}	7.2×10^{-32}	6.0×10^{-33}	5.6×10^{-33}	5.5×10^{-33}
Hartley	$\Gamma_{DC}^2\left[\left(\frac{\overline{i_n^2}}{\Delta f}\right)\frac{\omega_{1/f}}{\Delta\omega}\right]$			$\Gamma_{rms}^2\left(\frac{\overline{i_n^2}}{\Delta f}\right)$		
Oscillation freq.	1 GHz	10 GHz	100 GHz	1 GHz	10 GHz	100 GHz
M_1	6.2×10^{-35}	1.7×10^{-31}	4.4×10^{-33}	2.4×10^{-33}	3.1×10^{-33}	1.1×10^{-33}
M_2	9.8×10^{-32}	2.7×10^{-35}	1.3×10^{-32}	4.2×10^{-33}	4.2×10^{-33}	1.2×10^{-33}
LC tank				1.3×10^{-34}	1.3×10^{-34}	2.1×10^{-34}
Total (Σ)	9.8×10^{-32}	1.7×10^{-31}	1.8×10^{-32}	6.8×10^{-33}	7.4×10^{-33}	2.5×10^{-33}
Cross-coupled	$\Gamma_{DC}^2\left[\left(\frac{\overline{i_n^2}}{\Delta f}\right)\frac{\omega_{1/f}}{\Delta\omega}\right]$			$\Gamma_{rms}^2\left(\frac{\overline{i_n^2}}{\Delta f}\right)$		
Oscillation freq.	1 GHz	10 GHz	100 GHz	1 GHz	10 GHz	100 GHz
M_3	3.4×10^{-33}	1.3×10^{-34}	4.2×10^{-32}	7.7×10^{-34}	5.1×10^{-34}	1.7×10^{-33}
M_4	6.7×10^{-33}	1.3×10^{-32}	4.8×10^{-32}	1.4×10^{-34}	2.0×10^{-34}	8.9×10^{-34}
LC tank				1.7×10^{-34}	6.5×10^{-35}	4.3×10^{-34}
Total (Σ)	1.0×10^{-32}	1.3×10^{-32}	9.0×10^{-32}	1.1×10^{-33}	7.8×10^{-34}	3.0×10^{-33}

In order to provide them in a more intuitive form, the results in Table 1.7 are plotted in Figs. 1.9 and 1.10.

As in the previous subsection, by considering a given q_{max} (1.10) and a given frequency offset $\Delta\omega=2\pi\times10^6$, equations (1.15) and (1.16) can be used in order to compare the flicker and

thermal noise contributions respectively, to the phase noise of various oscillator topologies. In this perspective, Figs. 1.9 and 1.10 show the variation of the flicker and thermal noise contributions to phase noise respectively, for the three oscillator topologies under investigation with respect to changes in the oscillation frequency, at a frequency offset of 1 MHz.

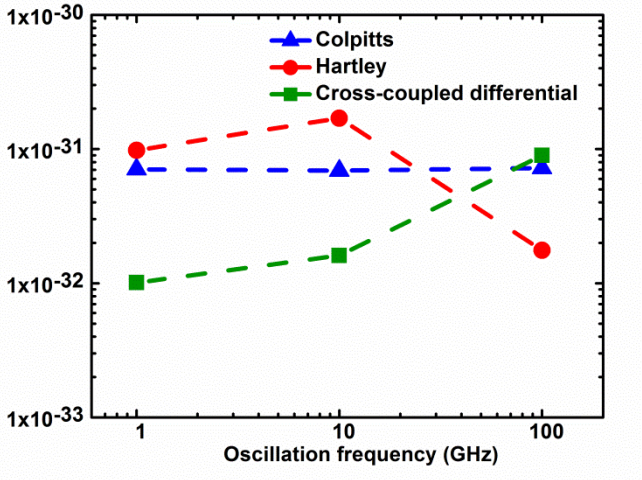


Fig. 1.9. Sum of $\Gamma_{DC}^2\left[\left(\frac{\overline{i_n^2}}{\Delta f}\right)\frac{\omega_{1/f}}{\Delta\omega}\right]$ for all flicker noise sources in each oscillator topology @ 1 MHz offset vs. oscillation frequency for Colpitts, Hartley and common-source cross-coupled differential pair topologies.

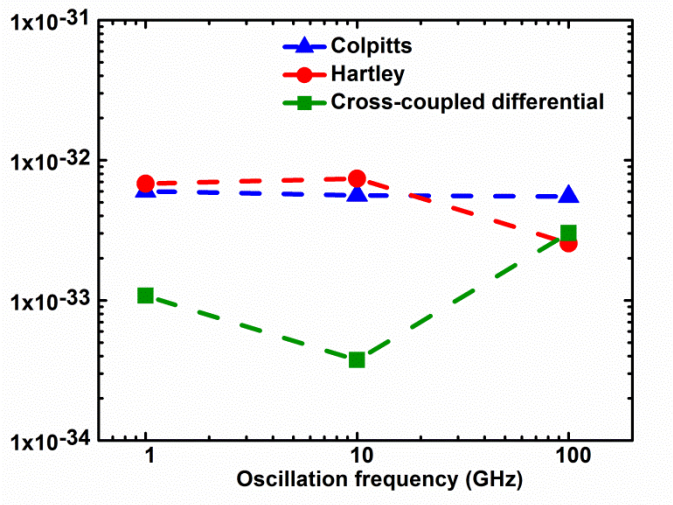


Fig. 1.10. Sum of $\Gamma_{rms}^2\left(\frac{\overline{i_n^2}}{\Delta f}\right)$ for all thermal noise sources in each oscillator topology @ 1 MHz offset vs. oscillation frequency for Colpitts, Hartley and common-source cross-coupled differential pair topologies.

1.5 Topology Performances versus Oscillation Frequency Regions

In the previous section we reported the results of the effective ISF for every active device of the three oscillator topologies according to equations (1.12) and (1.13). Here we try to explain the different phase noise behavior achieved for the three oscillator topologies over the frequency range from 1 to 100 GHz. The results of the previous section suggest considering additional oscillation frequencies. For this reason, the three topologies have been designed also for the additional oscillation frequencies of 30, 50 and 70 GHz, according to the same criteria of Sections 1.2 and 1.4.

Table 1.8 reports the values of the circuit components for each topology for the oscillation frequencies of 30, 50 and 70 GHz.

Table 1.8. Device sizing for oscillation frequencies of 30, 50 and 70 GHz.

	Transistor Width [µm]				**Capacitor value [pF]**					**Inductor value [pH]**	
frequency [GHz]	M_1	M_2	M_3	M_4	C_1	C_2	C_3	C_4	C_5	L_1	L_2
30	30	30	30	15	0.286	10^5	0.1385	0.4	0.0627	166.7	83.35
50	30	30	30	15	0.15	10^5	0.071	0.25	0.0297	100	50
70	30	30	30	15	0.0928	10^5	0.0439	0.15	0.0158	71.4	35.7

Fig. 1.11 reports the phase noise results obtained by SpectreRF for 1, 10, 30, 50, 70 and 100 GHz at a 1 MHz frequency offset from the carrier.

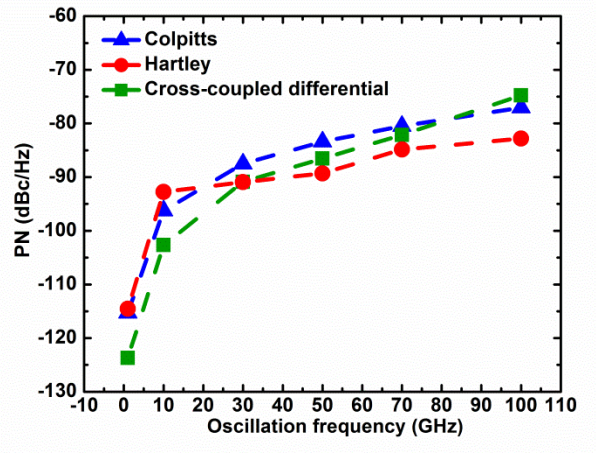


Fig. 1.11. PN at a 1 MHz frequency offset from carrier vs. oscillation frequency for Colpitts, Hartley and common-source cross-coupled differential pair topologies by SpectreRF.

These results allow us to identify the following four main frequency regions: 1-20, 20-30, 30-80 and 80-100 GHz. They offer the opportunity to carry out further comparative analyses and derive a number of observations.

Comparing the total (i.e. sum) contributions of the flicker and thermal noise sources in Table 1.7 and Figs. 1.9 and 1.10, we can note that the flicker noise contribution dominates at the frequency offset of 1 MHz at the oscillation frequencies of 1, 10 and 100 GHz. We can also note

that the term (1.15) determining the flicker noise contribution derived from ISF, as in Fig. 1.9, shows an agreement with the phase noise derived by SpectreRF-Cadence, as in Fig. 1.11.

This is because, as already mentioned in Section 1.4, from equations (1.8), (1.9) and (1.14), it can be concluded that the flicker noise contribution to phase noise is defined by the product of the transistor flicker noise with Γ_{DC}^2, as expressed in (1.15) and quantified in Table 1.7.

Region 1 (1-20 GHz): According to Fig. 1.11, the common-source cross-coupled differential pair topology exhibits the lowest phase noise with respect to the other two topologies. The highest phase noise is exhibited by the Hartley topology. This is in agreement with the trend reported in Fig. 1.9. Delving into the separate noise sources as addressed in Section 1.4 and shown in Figs. 1.6 (a), 1.7 (a) and 1.8 (a), the nodes mostly prone to the current noise injection are: the drain of M_2 in the Colpitts topology; the drain of M_2 from 1 to 3 GHz and the drain of M_1 from 3 to 20 GHz in the Hartley topology; and the drain of both M_3 and M_4 in the common-source cross-coupled differential pair topology.

Region 2 (20-30 GHz): In this region, we note from Fig. 1.11 that the common-source cross-coupled differential pair topology still maintains the best phase noise performance, but unlike the above case, we can observe an inversion between the Hartley and Colpitts topologies. The latter exhibits the worst phase noise at 30 GHz. Fig. 1.9 follows approximately the same results. From Figs. 1.6 (a), 1.7 (a) and 1.8 (a) we can see that the nodes mostly sensitive to noise injections are: the drain of M_2 in the Colpitts topology; the drain of M_1 in the Hartley topology; and the drain of M_4 in the common-source cross-coupled differential pair topology.

Region 3 (30-80 GHz): In Fig. 1.11, we register an inversion for the best phase noise performance, given now by the Hartley topology, whereas the Colpitts topology still exhibits the worst phase noise as in the previous case. A similar behavior is exhibited in Fig. 1.9. In this region the nodes mostly sensitive to noise injection according to Figs. 1.6 (a), 1.7 (a) and 1.8 (a) are: the drain of M_2 in the Colpitts topology; the drain of M_1 up to 50 GHz and the drain of M_2 at higher frequencies in the Hartley topology; the drain of both M_3 and M_4 until 50 GHz and of M_3 above 50 GHz in the common-source cross-coupled differential pair topology.

Region 4 (80-100 GHz): Fig. 1.11 indicates that Hartley continues to exhibiting the lowest phase noise. However, with respect to the previous case, here we can observe an inversion of performance between the Colpitts topology and the common-source cross-coupled differential pair topology, which now exhibits the highest phase noise. We can also derive the same conclusions from Fig. 1.9. The operation in the triode region for some part of the oscillation period is the main reason for this noise performance degradation at the highest frequencies in the common-source cross-coupled differential pair topology according to the notes in [25]. Indeed, our design operates in the voltage-limited regime, thus causing the active devices to enter in the triode region at the peaks of the differential output node voltage. We notice from Figs. 1.6 (a), 1.7 (a) and 1.8 (a) that the most sensitive nodes in this frequency range are: the drain of M_1 in the

Colpitts topology; the drain of M_2 in the Hartley topology; the drain of M_3 in the common-source cross-coupled differential pair topology.

At least up to a 1 MHz frequency offset from the carrier, the flicker noise contribution is dominant according to Figs. 1.5 (a) – (c) and Table 1.7. Therefore, the proportional increase of the flicker noise contribution to phase noise due to M_3 at the highest oscillation frequencies in the common-source cross-coupled differential pair topology, as observed in Table 1.6 and Fig. 1.8 (a), is the main cause of the overall phase noise increase. Actually, this is an effect of the losses through the p-MOSFET tail current source that become part of the tank circuit, thus impairing its Q [26, 27]. Note that the superior phase noise performance of the Hartley topology at high frequencies noted in Regions 3 and 4 is in agreement with the observations in [25, 28].

1.6 Conclusions

Phase noise comparative analyses have been carried out for Colpitts, Hartley and common-source cross-coupled differential pair LC oscillator topologies in the frequency range from 1 to 100 GHz. The circuit topologies have been implemented in 28 nm bulk CMOS technology for operation at 1, 10, 30, 50, 70 and 100 GHz, maintaining equal power consumption, quality factor and transistor sizes for a fair comparison among all the circuit topologies. All the steps and settings for accurate evaluations of the impulse sensitivity function have been discussed and clarified in depth. Phase noise performances have also been evaluated directly through periodic steady-state simulations in the SpectreRF-Cadence environment. These last results have been compared with the results obtained through the ISF for a wide set of amplitudes of injected current pulses. The phase noise predicted by the ISF is in a good agreement with the results obtained by SpectreRF under the given simulation settings, especially for the pulse amplitude of 1 μA.

Moreover, the investigations on the phase noise contributions from each component of the investigated oscillator circuit topologies have been reported and discussed in detail. The results show that, under the adopted design conditions, the three oscillator topologies rank unevenly in terms of the best phase noise performance rating scale for oscillation frequencies from 1 to 100 GHz. This comes as a result of the frequency dependence of both contributions from each circuit component and the sensitivity to noise injections in the circuit nodes. Recent studies refer to the common-source cross-coupled differential pair topology as the one with the best phase noise as a consequence of the circuit designs carried out at lower frequencies. Our comparative analyses reported here show that there is no superior topology in the absolute sense, but that the identification of the best circuit topology with respect to phase noise is strictly related to the operating frequency range. Nowadays, the most popular topology used is the common-source cross-coupled differential mainly due to its reliable start-up. However, the results presented here, suggest the opportunity to invest additional studies and efforts in exploring the circuit design implementations also of other topologies, whose potential may have been perhaps underestimated up to date, especially at very high frequencies for which, thanks to the recent

advances in the nano-scale technology process, MOSFETs with cut-off and max frequencies in excess of 280 and 350 GHz [29], respectively, are available nowadays for a potential use in a number of emerging wireless applications in the millimeter-wave frequency range.

Chapter 2

Colpitts, Hartley, Common-Source Cross-Coupled and Armstrong Differential topologies

2.1 Introduction

Advances in wireless communications have a great impact on our societal and economic challenges [30-34]. One of the most critical circuits of modern radiofrequency transceivers is the local oscillator, i.e. an autonomous circuit operating as the "pulsing heart" of such systems, in an analogy with the human body. As any other solid-state circuits, oscillators are affected by the inherent noise of the electronic devices. One of the major negative effects of noise in oscillators is given by the induced variations on the instantaneous oscillation frequency, leading to the degradation of the spectral purity of the output voltage, referred as phase noise (PN) [5, 8]. Oscillator phase noise performance directly affects the bit-error rate (BER) of the overall communication system [2].

Understanding the generation mechanisms of phase noise has been a very intriguing challenge and consequently most of the efforts have been made in this direction for a number of circuit topologies [35]. However, no complete comparative studies have been carried out on how to choose the oscillator circuit topology that could potentially offer the best performance in terms of phase noise for the range of operating frequencies of modern telecommunication systems. Usually, thanks to its reliable start-up, the common-source cross-coupled differential pair topology is chosen a priori without any further considerations. Thereby, from a designer perspective, such a comparative analysis could be very helpful in focusing the design efforts toward specific directions.

On the basis of the above motivations, in Chapter 1 and in our recent works [OP1, OP6] we dealt with this open question not addressed by the literature. In particular, we carried out a comparative analysis of phase noise of the common-source cross-coupled differential pair topology with Colpitts and Hartley single-ended topologies in 28 nm bulk CMOS technology for oscillation frequencies ranging from 1 to 100 GHz. In that study we made use of the impulse sensitivity function (ISF), $\Gamma(x)$ [36], which allowed us to quantify the noise contributions to the overall phase noise for each device in each oscillator circuit topology and identify the dominant noise sources and their impact versus the operating frequency [OP1]. Interestingly, the results showed that there is not a superior topology in the absolute sense, but that the identification of the best circuit topology is related to the operating frequency range. In particular, the Hartley topology exhibited the best performance at higher frequency [OP1].

Despite these results provide a first interesting perspective, this is limited by the comparison between a differential topology, i.e. cross-coupled common-source differential pair, and two single-ended topologies, Colpitts and Hartley. In fact, assuming a perfect symmetry, common-

mode noise sources (e.g. noise coming from the common bias circuitry) do not produce effects in a differential topology; thereby, in principle, this aspect may play a significant role in determining the phase noise performance, then leading to a less effective comparison. Moreover, despite Colpitts and Hartley single-ended topologies have long been used in discrete circuit design, the advances in silicon integration have led to the implementation of differential versions as well [37], which have shown the potential for superior performance, typically at the expenses of larger area occupancy on silicon.

Consequently, extending the comparative analyses of phase noise carried out in Chapter 1 and therein [OP1, OP6] to the Colpitts and Hartley differential topologies is in order for a comparison under common conditions. Moreover, on the basis of the advances in integration and intrigued by the interesting results revealed by our previous analyses reported in Chapter 1 and therein [OP1, OP6], it would be useful to extend the study to other oscillator topologies which may deserve our attention, such as the Armstrong topology. A recent implementation of this circuit topology shows potential for very low power operation, while achieving high spectral purity [38]. This solution exploits integrated transformers [6, 39] in order to implement magnetic coupling between gate and drain terminals, as well as source and drain terminals of the transistor pair in the oscillator.

Driven by the above motivations, in this chapter we report a comparative investigation of phase noise in the common-source cross-coupled pair, Colpitts, Hartley and Armstrong differential oscillator topologies, with the main objective of bringing to the light the contributions of the inherent noise sources in the most widespread oscillator topologies reported in the literature. This comparative analysis extends and complements the previous analysis reported in Chapter 1 and therein [OP1, OP6], which was limited to Colpitts and Hartley single-ended topologies and common-source cross-coupled differential pair. Here, the comparative analysis is extended to differential topologies for a fair comparison with the common-source cross-coupled differential pair and extended also to the Armstrong topology (in addition to Colpitts and Hartley). The oscillator circuit topologies are investigated under the common design conditions, such as (a) power consumption, (b) supply voltage, (c) transistor current density and (d) sizing (area, aspect ratio, finger width), (e) inductance and (f) quality factor of the integrated spiral inductors, (g) coupling factor of the integrated transformers, and (h) considering the full models of the transistors available within the process design kit, including all their parasitic components related to their actual size, but excluding the layout interconnections, since the additional parasitic components introduced by the layout implementation could mask the results of the topological investigations which are the objective of our study. The common conditions adopted in this comparative analysis are the same as those adopted for the comparative analysis between Colpitts and Hartley single-ended topologies and common-source cross-coupled differential pair reported in Chapter 1 and published therein [OP1, OP6], thereby they represent the natural sequel from the previous results, which assures the continuity with them. As in the previous work [OP1, OP6], the ISF is used to quantify the impact of each noise source on the

overall phase noise in each oscillator circuit topology, allowing the identification of the major contributions to the phase noise degradation versus the oscillation frequency. The results could drive the designer through the choice of the oscillator circuit topology that could potentially offer the best phase noise.

The chapter is organized as follows. Section 2.2 describes the oscillator circuit topologies and their common design conditions. Section 2.3 reports the comparative analyses of phase noise. Section 2.4 reports the investigation on the contributions of each noise source to the overall phase noise. Finally, in Section 2.5 the conclusions are drawn.

The key contents of this chapter have been reported in original contributions published in an international peer-reviewed journal and in conference proceedings [OP2, OP7, OP8].

2.2 Circuit Topologies

Fig. 2.1 shows the oscillator circuit topologies designed in 28 nm bulk CMOS technology, operating from a 1 V supply voltage. All the circuit topologies operate in the voltage-limited regime. The same figure shows the current impulsive sources acting in parallel to the inherent current noise sources and used for the evaluation of the ISF. Based on the findings reported in Chapter 1 and therein [OP1, OP6], transient simulations were performed for an injected current amplitude of 1 μA. The workload for the circuit simulations was significantly reduced by using OCEAN scripts [21].

The sizes of the active and passive devices are reported in Table 2.1. Capacitors are considered ideal, whereas a quality factor (Q) of 10 is assumed for the spiral inductors, i.e. a feasible value for the oscillation frequencies in the range of interest from 1 to 100 GHz [7, 40]. A coupling factor k of 0.85 is assumed for the transformers [37]. For all the investigated differential circuit topologies the total power consumption is 6.3 mW, as in Chapter 1 and therein [OP1, OP6].

In particular, the comparative analysis takes into account the common-source cross-coupled differential pair, Colpitts, Hartley and Armstrong differential circuit topologies shown in Figs. 2.1 (a)-(d), which have shown the best phase noise performances with respect to other design variations. Thereby, these topologies allow an effective comparison based on the actual needs and opportunities, rather than a comparison between basic topologies and their variations which are known from the literature to provide worse phase noise performance with respect to those considered in this comparative analysis. In other words, the investigated topologies are the most promising in their category. The common-source cross-coupled pair in Fig. 2.1 (a) provides the negative resistance needed for the oscillation start-up. A p-MOSFET is chosen as a current source since it exhibits lower flicker noise. The transformer coupling in the Colpitts topology of Fig. 2.1 (b) contributes to the suppression of common-mode oscillations [22]. Moreover, for lower phase noise, two separate tail current transistors are used for biasing, as in [41]. As for the Hartley topology in Fig. 2.1 (c), the transformer coupling is used in order to reduce the area

occupied by the inductors [42]. Finally, in the Armstrong topology of Fig. 2.1 (d), the transformer coupling between gate and drain is considered for the same reasons. Also, in the latter topology, the inductor of the LC tank is given by the overall equivalent inductance offered by the self-inductance of the spiral inductors of the transformer and the mutual inductance between the two spirals on the gate and drain terminals of M_1.

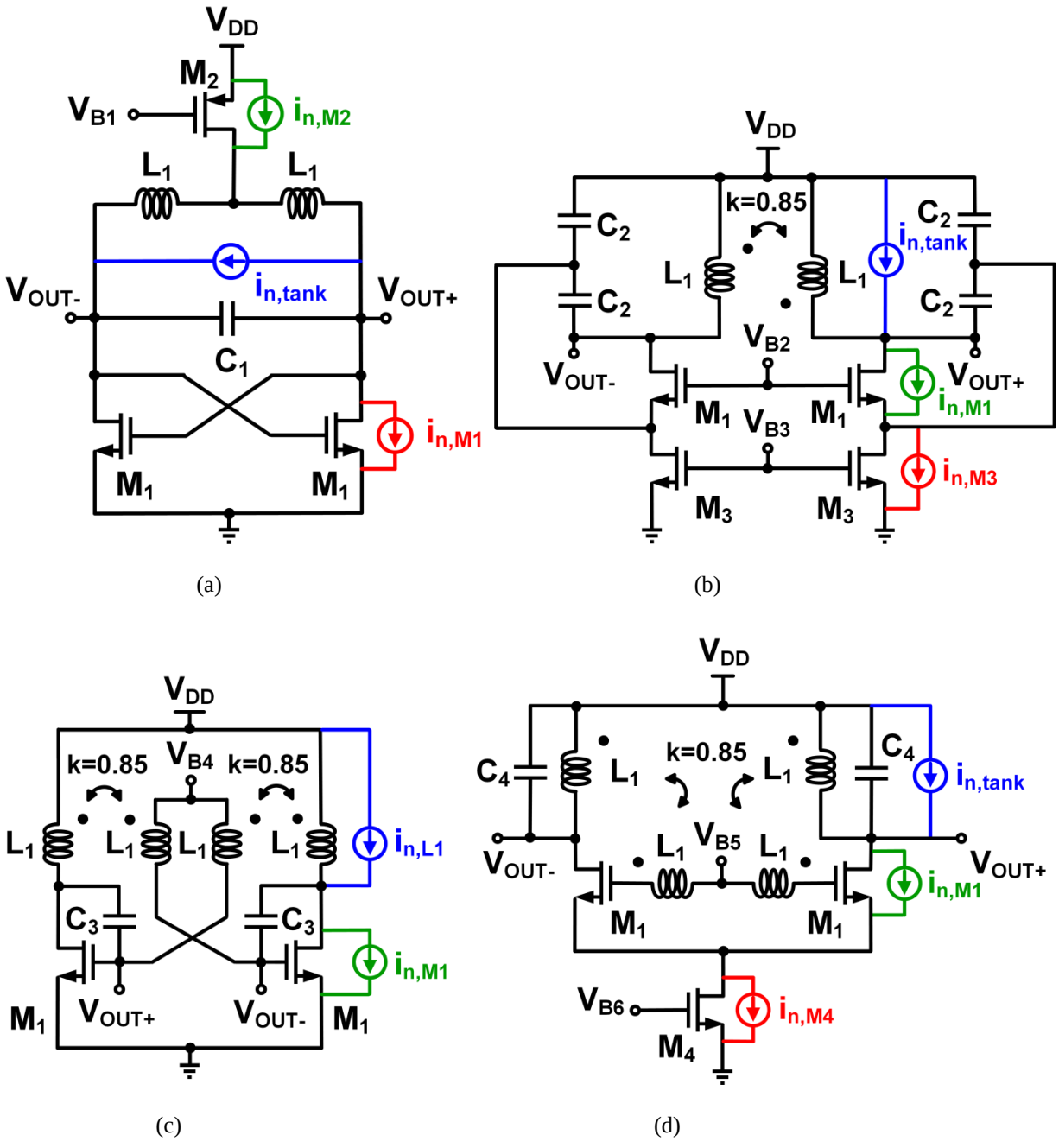


Fig. 2.1. Schematic of the oscillator circuit topologies: a) common-source cross-coupled differential pair; b) differential Colpitts; c) differential Hartley; d) differential Armstrong. V_{B1}, V_{B2}, V_{B3}, V_{B4}, V_{B5}, and V_{B6} are DC bias voltages.

Table 2.1. Device Sizing

Osc. freq. [GHz]	Transistor Width [µm]				Capacitor value [fF]				Inductor value [pH]
	M_1	M_2	M_3	M_4	C_1	C_2	C_3	C_4	L_1
1	15	30	15	30	2500	5550	1410	5000	5000
10	15	30	15	30	229	527	132.5	469	500
100	15	30	15	30	5.7	29	4.72	15	50

2.3 Comparison of Phase Noise Performance

Figs. 2.2-2.4 report the results in terms of phase noise obtained through the ISF and direct plots from periodic steady state (PSS) and periodic noise (Pnoise) simulations by SpectreRF in Cadence.

The ISF allows us to determine the flicker and thermal noise contributions to the overall phase noise, as reported in Figs. 2.2-2.4 [OP6]. Consequently, the $1/f^3$ corner of the phase noise can be identified in each case. Table 2.2 provides the results for a 1 MHz frequency offset from the carrier. The results show that the phase noise predicted by ISF matches well (within 1.7 dB) with the values obtained directly by means of SpectreRF simulations.

From Table 2.2, it can be observed that under the adopted design conditions, common to all topologies, differential Armstrong topology reported here exhibits the lowest phase noise at an oscillation frequency of 1 GHz. The second best phase noise performance is exhibited by the common-source cross-coupled topology, whereas Hartley follows closely and then Colpitts.

Table 2.2. Summary of PN Performance

Topology	PN [dBc/Hz] @ 1 MHz frequency offset					
	1 GHz		10 GHz		100 GHz	
	SpectreRF	ISF	SpectreRF	ISF	SpectreRF	ISF
Cross-coupled	-123.7	-124.06	-102.66	-102.69	-74.78	-75.79
Colpitts	-118.34	-119.71	-99.56	-100.26	-78.45	-78.27
Hartley	-121.69	-123.38	-102.59	-104.15	-89.78	-89.00
Armstrong	-127.51	-128.22	-106.12	-106.57	-72.34	-73.74

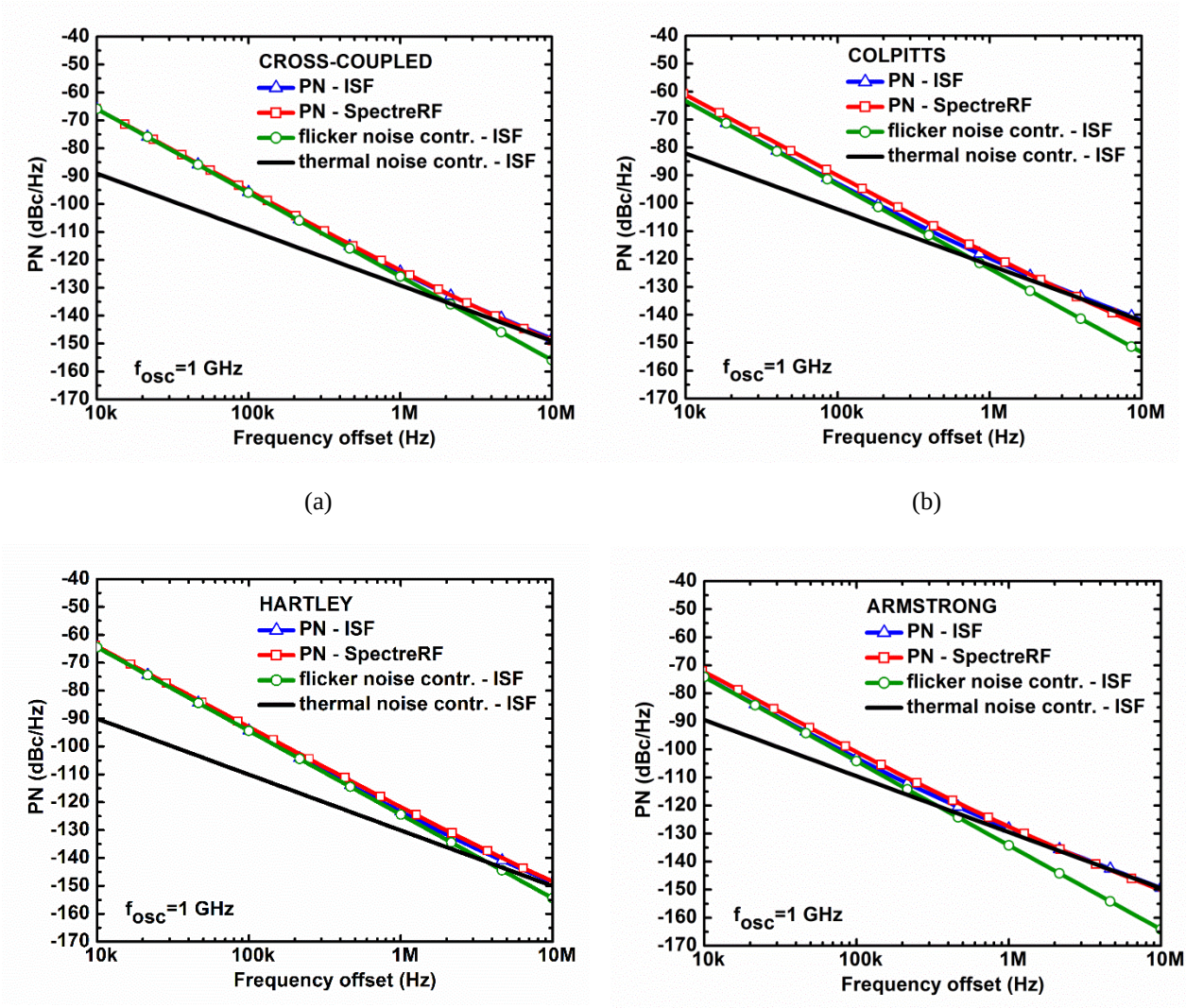


Fig. 2.2. PN vs. frequency offset obtained through the ISF for a 1 μA current impulse, and direct plot from PSS and Pnoise SpectreRF simulations, for the oscillation frequency of 1 GHz for: a) common-source cross-coupled differential pair. The $1/f^3$ PN corner is at the frequency offset of 2 MHz; b) differential Colpitts. The $1/f^3$ PN corner is at the frequency offset of 0.74 MHz; c) differential Hartley. The $1/f^3$ PN corner is at the frequency offset of 3.7 MHz; d) differential Armstrong. The $1/f^3$ PN corner is at the frequency offset of 0.34 MHz.

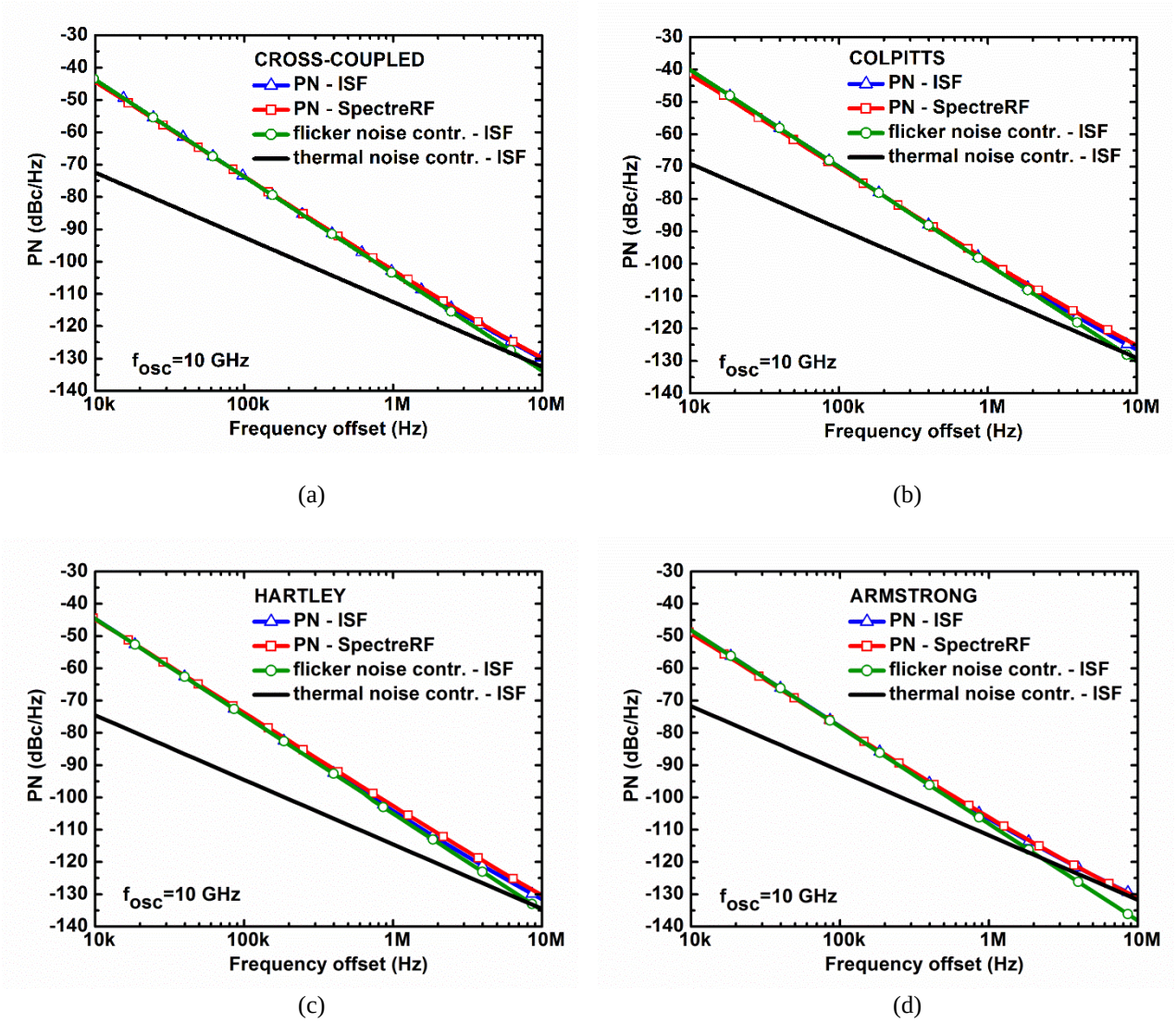


Fig. 2.3. PN vs. frequency offset obtained through the ISF for a 1 μA current impulse and direct plot from PSS and Pnoise SpectreRF simulations, for the oscillation frequency of 10 GHz for: a) common-source cross-coupled differential pair. The $1/f^3$ PN corner is at the frequency offset of 7.5 MHz; b) differential Colpitts. The $1/f^3$ PN corner is at the frequency offset of 8 MHz; c) differential Hartley. The $1/f^3$ PN corner is at the frequency offset of 10 MHz; d) differential Armstrong. The $1/f^3$ PN corner is at the frequency offset of 2.1 MHz.

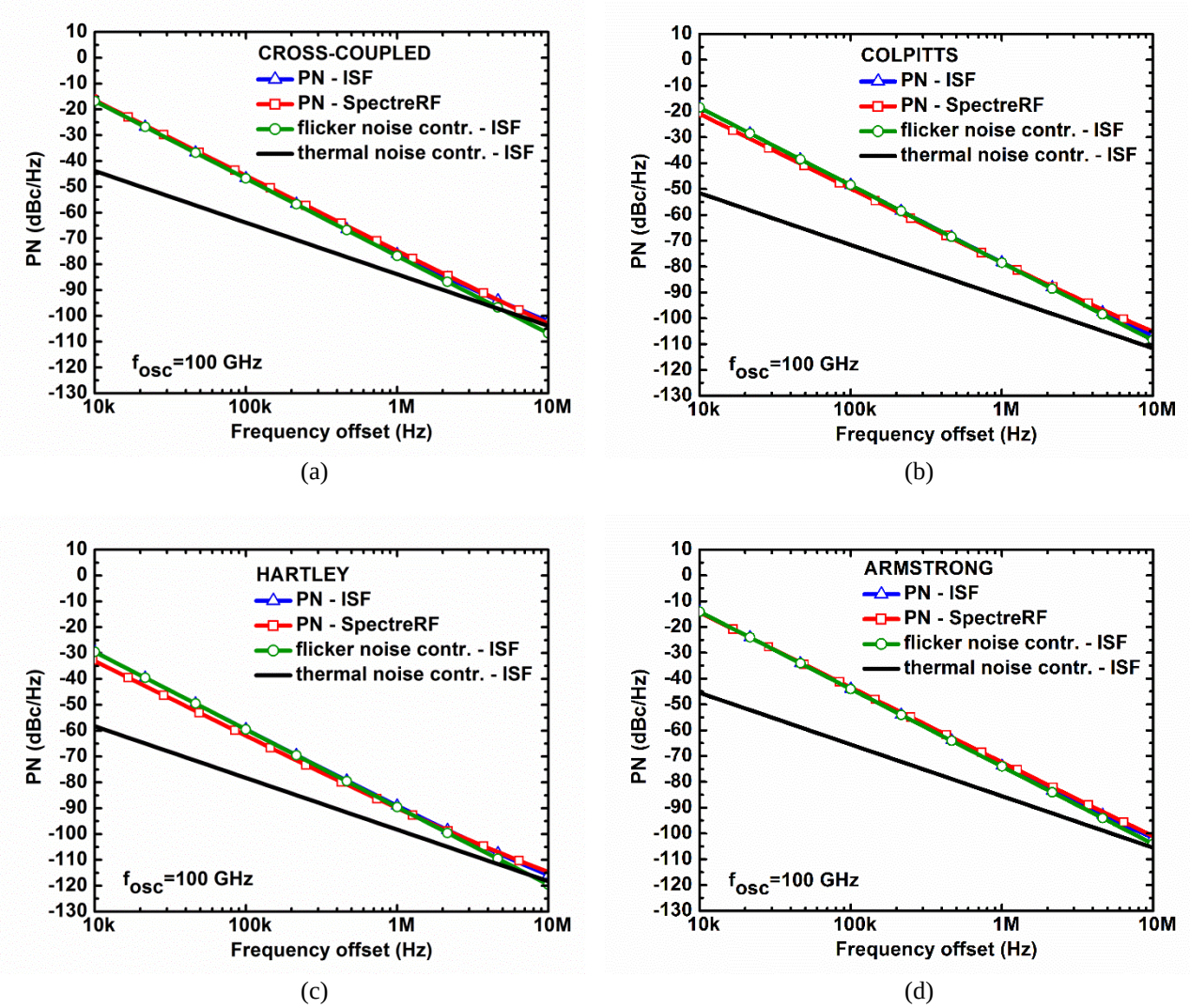


Fig. 2.4. PN vs. frequency offset obtained through the ISF for a 1 μA current impulse and direct plot from PSS and Pnoise SpectreRF simulations, for the oscillation frequency of 100 GHz for: a) common-source cross-coupled differential pair. The $1/f^3$ PN corner is at the frequency offset of 5.5 MHz; b) differential Colpitts. The $1/f^3$ PN corner is at the frequency offset of 20 MHz; c) differential Hartley. The $1/f^3$ PN corner is at the frequency offset of 7.4 MHz; d) differential Armstrong. The $1/f^3$ PN corner is at the frequency offset of 14 MHz.

At the oscillation frequency of 10 GHz, the Armstrong topology considered in this study is superior in terms of phase noise performance to the other topologies under investigation. From the results obtained by SpectreRF, the cross-coupled and Hartley topologies are characterized by similar phase noise performance, whereas Colpitts shows the worst one.

Finally, at 100 GHz, the Hartley topology shows the best phase noise compared to the others. The Colpitts topology exhibits a phase noise higher than 10 dB with respect to Hartley. Then follows the common-source cross-coupled topology and last ranks Armstrong, which exhibits the worst phase noise.

In order to gain a better understanding of the performances in between the initial discrete set of frequencies, the topologies have been designed also for the additional operating frequencies of 30, 50 and 70 GHz. The phase noise at a 1 MHz offset from the carrier frequency obtained by direct plots from PSS and Pnoise simulations is shown in Fig. 2.5. By inspection, Fig. 2.5 reveals five distinct regions in which the topologies rank unevenly in terms of best phase noise performance.

Region 1 (1-10 GHz): The Armstrong topology exhibits the lowest phase noise, whereas the Colpitts topology exhibits the worst one. In between, the common-source cross-coupled topology shows phase noise performance very close to that given by the Hartley topology.

Region 2 (10-20 GHz): The Armstrong still exhibits the best phase noise and Colpitts the worst one. On the other hand, Hartley gradually improves with respect to the other topologies. On an average, the common-source cross-coupled pair is characterized by a phase noise 2.5 dB lower than Colpitts.

Region 3 (20-40 GHz): The Hartley topology exhibits the lowest phase noise. The comparison with the others improves as the oscillation frequency increases. Here, Armstrong exhibits the second best phase noise performance, whereas the Colpitts topology still exhibits the worst one. On an average, the common-source cross-coupled pair shows a phase noise 1.2 dB lower than Colpitts.

Region 4 (40-70 GHz): The differential Armstrong topology shows the worst performance, and the cross-coupled and Colpitts do not show better performance. The Hartley topology keeps increasing its superior performance with respect to the others. In particular, at 70 GHz, the differential Hartley topology shows a phase noise about 10 dB lower with respect to the others.

Region 5 (70-100 GHz): The differential Hartley is still characterized by the best phase noise, whereas Armstrong continues to exhibit the most degraded output signal spectrum. Here the Colpitts topology exhibits a better phase noise with respect to the common-source cross-coupled topology. In particular, their phase noise is on an average 3.5 dB and 2 dB, respectively, lower than differential Armstrong.

Thereby, it can be concluded that for oscillation frequencies between 1 and 20 GHz, the Armstrong oscillator circuit topology considered here could be potentially the best choice. Outside this range, between 20 and 100 GHz, its performance dramatically deteriorates. For this oscillation frequency range, the differential Hartley topology considered in this study appears to be potentially the best choice. It is worth observing that the superior phase noise performance of the differential Hartley topology at high frequencies conforms with the results emerged from Chapter 1 and [OP1, OP6] for the single-ended Hartley topology.

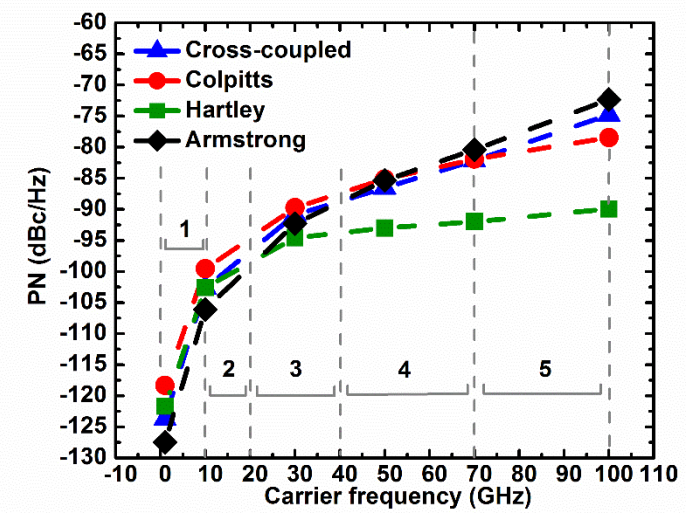


Fig. 2.5. PN at a 1 MHz frequency offset from the carrier frequency obtained by direct plots from PSS and Pnoise simulations, vs. oscillation frequency for the common-source cross-coupled differential pair, as well as for the differential Colpitts, Hartley and Armstrong oscillator circuit topologies.

2.4 Contributions of the Device Noise to Phase Noise

In order to get insight into the above results, in this section we report the evaluations of the contributions from each noise source in each oscillator circuit topology for a discrete set of oscillation frequencies from 1 to 100 GHz, carried out by means of the ISF. The total thermal noise contribution to the phase noise, the latter traditionally indicated with $\mathcal{L}$, from all m noise sources with a white power spectral density, can be expressed as [36]

$$\mathcal{L}\{\Delta\omega\}\big|_{white} = \sum_{i=1}^{m}\left[\left(\frac{\Gamma_{rms}^2}{q_{max}^2}\right)_i \frac{\left(\frac{\overline{i_n^2}}{\Delta f}\right)_i}{2\Delta\omega^2}\right] \tag{2.1}$$

where $\left(\frac{\overline{i_n^2}}{\Delta f}\right)_i$ is the thermal noise generated from the i^{th} noise source, q_{max} is the charge injected into a circuit node by the noise source insisting in that node, Γ_{rms} is the root mean square (rms) value of the ISF and $\Delta\omega$ is the offset from the oscillation angular frequency. The contribution of each noise source with white spectrum to the total thermal noise appearing at the output spectrum of the oscillator, the latter given by (2.1), is independent of the angular frequency offset $\Delta\omega$ as seen from (2.2).

$$\frac{\left[\mathcal{L}\{\Delta\omega\}\Big|_{white}\right]_i}{\mathcal{L}\{\Delta\omega\}\Big|_{white}} = \frac{\left(\frac{\Gamma_{rms}^2}{q_{max}^2}\right)_i \left(\frac{\overline{i_n^2}}{\Delta f}\right)_i}{\sum_{i=1}^{m}\left[\left(\frac{\Gamma_{rms}^2}{q_{max}^2}\right)_i \left(\frac{\overline{i_n^2}}{\Delta f}\right)_i\right]} \tag{2.2}$$

Moreover, the total flicker contribution to the phase noise, from all n noise sources with a 1/f (flicker) spectrum can be expressed as follows [36]

$$\mathcal{L}\{\Delta\omega\}\Big|_{flicker} = \sum_{i=1}^{n}\left[\left(\frac{4\Gamma_{DC}^2}{q_{\max}^{\ 2}}\right)_i \frac{\left(\frac{\overline{i_n^2}}{\Delta f}\right)_i}{8\Delta\omega^2} \frac{\left(\omega_{1/f}\right)_i}{\Delta\omega}\right] \tag{2.3}$$

where $\left(\frac{\overline{i_n^2}}{\Delta f}\right)_i \times \frac{\left(\omega_{1/f}\right)_i}{\Delta\omega}$ is the flicker noise generated from the ith noise source, Γ_{DC} is the DC value of the ISF and $\left(\omega_{1/f}\right)_i$ is the flicker noise corner of the ith active device. From (2.3) it can be concluded that larger oscillation amplitude leads to lower flicker noise contribution to phase noise, since $q_{max}=C\times V_{max}$, where C is the total tank capacitance and V_{max} is the maximum voltage swing across the tank [36]. The contribution of each flicker noise source to the total flicker noise appearing at the output spectrum of the oscillator, the latter given by (2.3), is independent of the angular frequency offset Δω as noted from (2.4).

$$\frac{\left[\mathcal{L}\{\Delta\omega\}\Big|_{1/f}\right]_i}{\mathcal{L}\{\Delta\omega\}\Big|_{1/f}} = \frac{\left(\frac{\Gamma_{DC}^2}{q_{max}^2}\right)_i \left(\frac{\overline{i_n^2}}{\Delta f}\right)_i \left(\omega_{1/f}\right)_i}{\sum_{i=1}^{n}\left[\left(\frac{\Gamma_{DC}^2}{q_{max}^2}\right)_i \left(\frac{\overline{i_n^2}}{\Delta f}\right)_i \left(\omega_{1/f}\right)_i\right]} \tag{2.4}$$

Figs. 2.6-2.8 report the percent contributions of the active and passive device noise sources to the flicker and thermal noise components of the phase noise. They show also the total contributions of each device to phase noise at a frequency offset of 1 MHz from the oscillation frequency. These results allow us to derive several important observations.

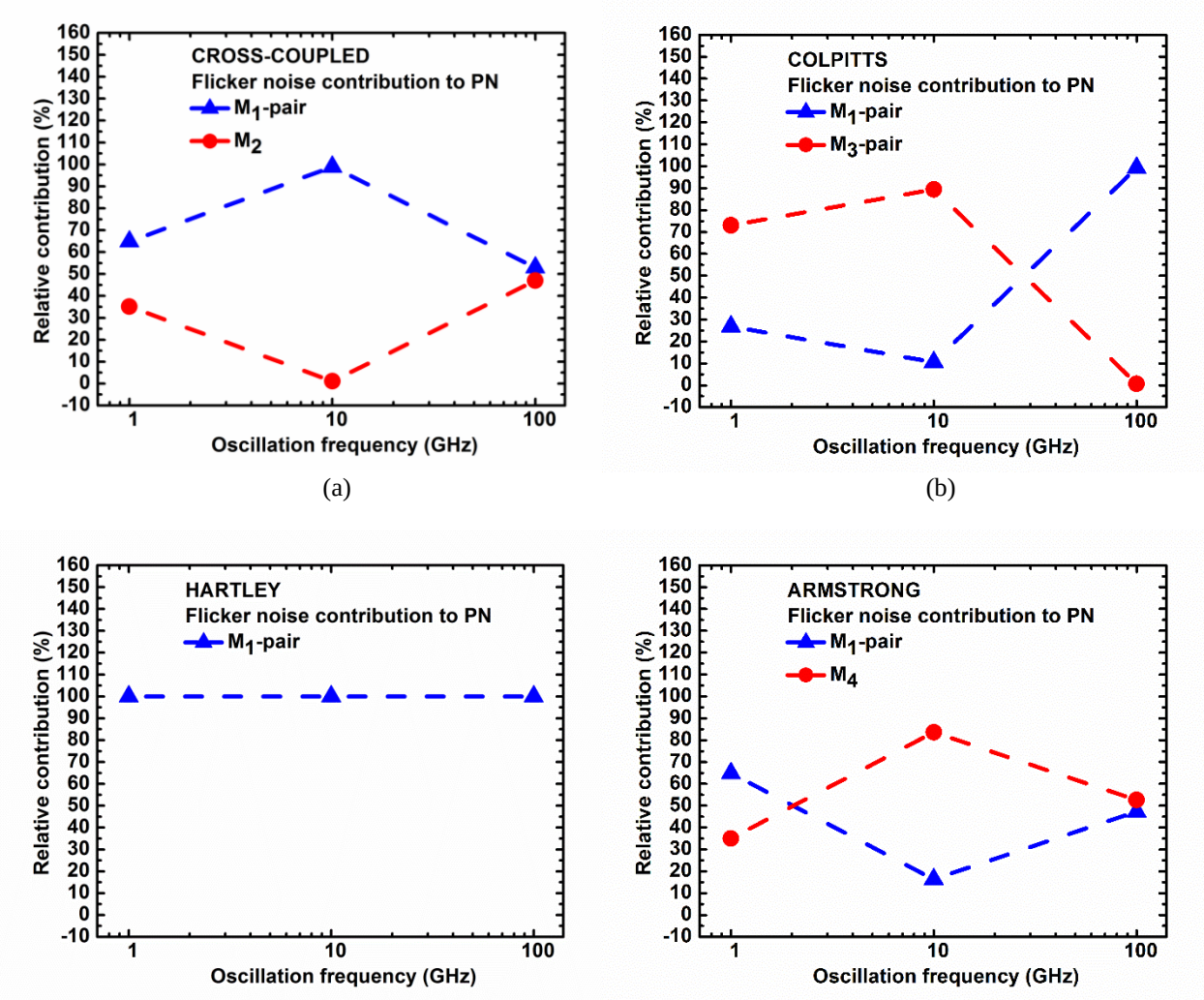


Fig. 2.6. Relative flicker noise contributions to PN from active devices in the oscillator circuit topologies for: a) common-source cross-coupled differential pair; b) differential Colpitts; c) differential Hartley; d) differential Armstrong. The contribution of each noise source to the flicker noise appearing at the output spectrum of the oscillator, is independent of the angular frequency offset $\Delta\omega$ as seen from (2.4).

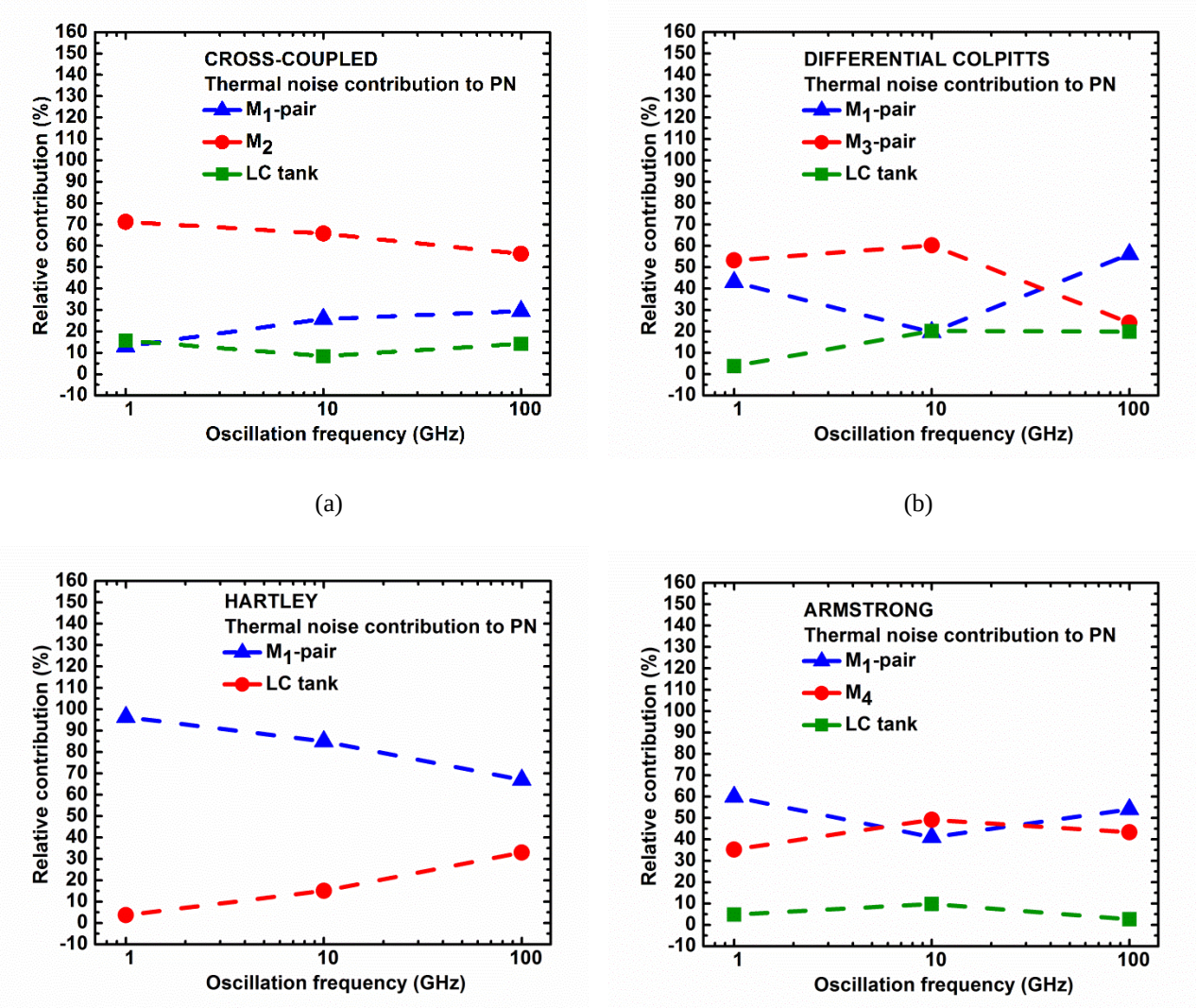


Fig. 2.7. Relative thermal noise contributions to PN from active and passive devices in the oscillator circuit topologies for: a) common-source cross-coupled differential pair; b) differential Colpitts; c) differential Hartley; d) differential Armstrong. The contribution of each noise source to the thermal noise appearing at the output spectrum of the oscillator, is independent of the angular frequency offset $\Delta\omega$ as seen from (2.2).

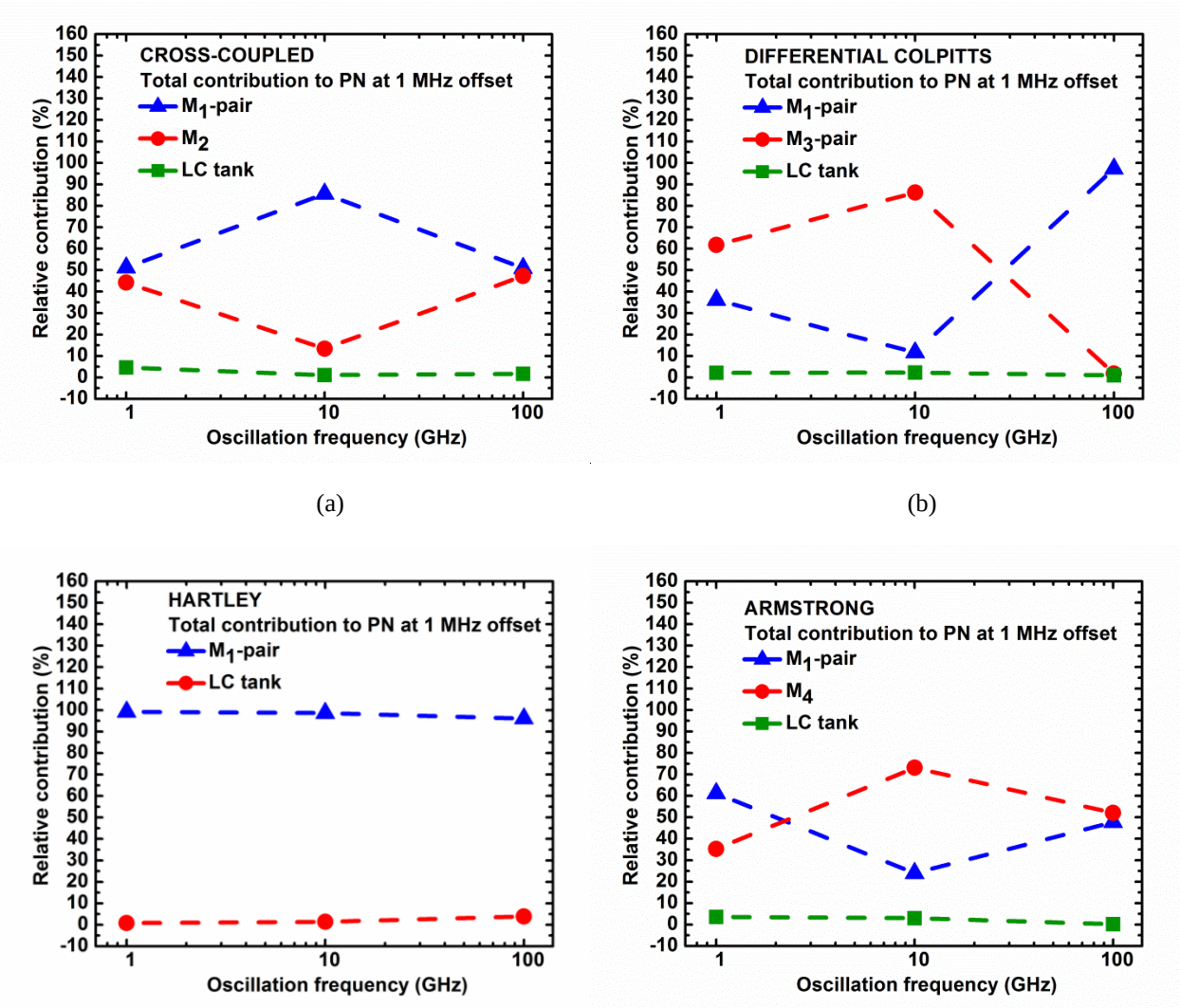


Fig. 2.8. Relative total noise contributions to PN, from active and passive devices in the oscillator circuit topologies at a 1 MHz offset from the carrier frequency for: a) common-source cross-coupled differential pair; b) differential Colpitts; c) differential Hartley; d) differential Armstrong.

For the 1 GHz oscillation frequency, in the common-source cross-coupled pair topology, the flicker noise sources of the cross-coupled pair contribute for about 65 % to the flicker noise component of the phase noise, as shown in Fig. 2.6 (a). From Fig. 2.7 (a), it can be observed that only 13% of the thermal noise component of phase noise comes from the thermal noise of the cross-coupled pair. In spite of all, Fig. 2.8 (a) shows that the total noise from the cross-coupled pair is the major contribution to the phase noise at a 1 MHz frequency offset. This can be explained by noticing from Fig. 2.2 (a) that the $1/f^3$ corner of the phase noise is at the frequency offset of 2 MHz.

In the Colpitts topology, from Figs. 2.6 (b) and 2.7 (b) both the flicker noise and thermal noise components of the phase noise are mainly due to the tail current transistor pair M_3. This explains why at a 1 MHz frequency offset, the tail current transistor pair M_3 takes the largest portion of the total phase noise as reported in Fig. 2.8 (b). With respect to the differential Hartley, the active device pair M_1 is the only source of flicker noise. In addition, the thermal noise generated by M_1 pair is mainly responsible for the white noise affecting the phase noise. This is why at a 1 MHz frequency offset, the total noise contribution to phase noise is dominated by the M_1 common-source crossed-coupled pair.

Last, from Figs. 2.6 (d) and 2.7 (d) M_1 transistor pair in the Armstrong topology is responsible for about 65 % and 60 % of the phase noise components due to flicker noise and thermal noise, respectively. Thereby, it is also responsible for most of the total phase noise (62 %) as shown in Fig. 2.8 (d).

For the oscillation frequency of 10 GHz, in the common-source cross-coupled pair topology, from Fig. 2.6 (a) the cross-coupled pair M_1 is the major contributor to the flicker noise component of phase noise. Also, at a 1 MHz offset the phase noise spectrum is still at the $1/f^3$ region according to Fig. 2.3 (a). Thereby, the cross-coupled pair M_1 is expected to be the dominant source of the overall phase noise as confirmed from Fig. 2.8 (a).

As for the Colpitts topology, the flicker contribution of the tail current transistor pair M_3 is predominant. Thereby, for the same reason as above, the tail current noise is the major contributor to phase noise at a 1 MHz frequency offset.

The pair of transistors M_1 in differential Hartley is almost the sole source of noise. This is because the noise generated by the parasitic resistance of the inductors is at least one order of magnitude lower than the flicker and thermal noise of the active device pair M_1.

Finally, the tail current transistor M_4 in the Armstrong topology is mostly responsible for the flicker component of phase noise. Moreover, the $1/f^3$ phase noise corner is at 2.1 MHz, as depicted in Fig. 2.3 (d). Therefore, at a 1 MHz offset the tail current transistor M_4 presents the main contribution to the overall phase noise.

For the oscillation frequency of 100 GHz, the $1/f^3$ frequency corners of phase noise in the four topologies under investigation are beyond 5 MHz, according to Figs. 2.4 (a)-(d). Consequently, at a 1 MHz frequency offset the phase noise is mostly due to the flicker noise. In particular, in the common-source cross-coupled topology, the cross-coupled pair M_1 and the p-MOSFET current source M_2 show similar contributions to the flicker noise component of phase noise and to the overall phase noise. This happens in spite of the higher thermal noise component of phase noise from the tail current transistor M_2.

In the Colpitts topology, flicker and thermal noise contributions to phase noise are mainly due to M_1 transistor pair. Thereby, the pair of transistors M_1 represents the noise source which is mainly responsible for the phase noise at a 1 MHz frequency offset.

In the Hartley topology, the active device pair M_1 is the only flicker noise source, which dominates the phase noise at a 1 MHz frequency offset.

In the Armstrong topology, almost equal contribution to the flicker and thermal noise components of phase noise from the M_1 transistor pair and the tail current transistor M_4, also means equal contribution to the overall phase noise at a 1 MHz frequency offset.

From all above, we can conclude that, for all four topologies and for the oscillation frequencies of 10 and 100 GHz, the $1/f^3$ region of the phase noise extends above 1 MHz. At an oscillation frequency of 1 GHz, this is true for the common-source cross-coupled pair and for the Hartley topologies. This is a consequence of the adoption of nano-scale CMOS technologies characterized by flicker noise corners of several tens or hundreds of MHz, which lead to flicker noise up-conversion being responsible for most of phase noise [43, 44] even at large offsets from the carrier frequency. This means that the devices with the highest contribution to the flicker noise present at the output spectrum will also dominate phase noise. Hence, design efforts should be made in minimizing as much as possible the flicker noise sources, as well as flicker noise up-conversion characteristic mechanisms in each topology. For example, increasing the width of the cross-coupled devices of Fig. 2.1 (a) would reduce the flicker noise produced by the transistor pair M_1. On the other hand, flicker noise up-conversion gain would be increased. This is due to the increased small-signal loop gain which would in turn cause a higher distortion of the voltage output [44, 45]. As another example, a filtering technique adopting a resonant filter could also be adopted for reducing flicker noise up-conversion [46].

For the oscillation frequency of 1 GHz, in the Colpitts and Armstrong topologies the $1/f^3$ phase noise corners are below the 1 MHz frequency offset. In this case, the active or passive devices with the highest contribution to the thermal noise component of the phase noise will be dominant. Short channel effects such as velocity saturation and channel length modulation are responsible for the significant increase in the thermal noise excess factor γ in deep submicron CMOS technologies [47, 48]. Thus, thermal noise from the active devices is usually the principal source of white noise in the output spectrum as already observed from Figs. 2.6-2.8.

Theoretical analysis of flicker noise up-conversion is outside the scope of this Chapter, for which we refer to the existing literature [44, 49, 50]. However, it is worth observing that due to the absence of varactor, flicker noise up-conversion is caused mainly by (a) amplitude to phase noise conversion due to nonlinear transconductor parasitic capacitance, as well as by (b) modulation of the harmonic content of the output voltage waveform, i.e., Groszkowski effect [44]. [49] reports an analysis which is based on the ideal quadratic I-V MOS characteristic, and, as such, quantitatively valid only for long-channel transistors. Thereby, the conclusion reported

therein [49] that there is no up-conversion of 1/f noise into phase noise from the core MOS transistors (M_1) does not apply to the oscillator circuit topologies investigated in this Chapter since they adopt short channel MOSFETs of the 28 nm bulk CMOS technology.

2.5 Conclusions

Comparative analyses of phase noise were carried out for four differential oscillator circuit topologies: common-source cross-coupled pair, Colpitts, Hartley and Armstrong. The oscillator circuit topologies were designed in a 28 nm bulk CMOS technology, for a set of operating frequencies in the range of 1 to 100 GHz. All the topologies were investigated under the same common design conditions, such as power consumption, supply voltage, transistor current density and sizing, inductance and quality factor of the integrated spiral inductors, coupling factor of the integrated transformers, and considering the full models of the transistors available within the process design kit, including all their parasitic components related to their actual size. Furthermore, the phase noise results from PSS and Pnoise simulations were compared with phase noise predictions obtained by the impulse sensitivity function. Finally, the noise contributions from each active or passive device in the circuit topologies to the flicker and thermal phase noise components and to the overall phase noise at a 1 MHz frequency offset from carrier frequency were evaluated and discussed.

The results show that, under the adopted design conditions, the phase noise of the four topologies degrades unevenly over the considered oscillation frequency range. In particular, the comparative analyses show the existence of five distinct frequency regions. Thereby, the results presented here suggest that the identification of the best oscillator circuit topology in terms of phase noise is related to the operating frequency range. Consequently, these results suggest the opportunity to address further investigations on the Armstrong and Hartley topologies considered in this study. The investigations could allow us to extend the range of possibilities beyond the common practice of choosing the common-source cross-coupled differential pair topology, traditionally selected for its reliable start-up, but without further topological considerations.

Finally, the investigations through the impulse sensitivity function allowed the identification of the dominant noise contributions for each oscillator circuit topology. Despite a few exceptions, the results showed that the flicker noise from the active devices is the component with the most significant effect on the oscillator phase noise at a 1 MHz frequency offset from the carrier frequency, confirming the rising role of flicker noise in nano-scale CMOS technology.

Chapter 3

Phase Noise Analysis of a Differential Armstrong Topology

3.1 Introduction

The phase noise (PN) performance of the local oscillator is one of the most critical bottlenecks in modern radio transceivers. Despite significant advances in recent years, achieving low phase noise is still a significant challenge [OP3, 8, 51-53].

Numerical methods for predicting accurately phase noise are not always available. However, even when such methods exist, in design environments such as Cadence, they may not provide the necessary insights to the designer. Thereby, relatively simple and intuitive analytical expressions are desirable in order to provide a first-order yet accurate prediction of phase noise in oscillator circuit topologies.

In this regard, a linear time-variant model based on the impulse sensitivity function (ISF) was introduced in [36], which describes the phase sensitivity to noise perturbations. The ISF approach was found very helpful for getting critical insights about oscillator phase noise and was used widespread over the past years. As examples, in [22] it was adopted to derive phase noise expressions for differential Colpitts and common-source cross-coupled oscillators. Its application on the Tuned-Input-Tuned-Output (TITO) and injection-locked oscillators was presented in [54] and [20] respectively.

Another approach for deriving accurate expressions of the phase noise is based on phasor analysis. In particular, expressions for the noise of the output spectrum of common-source single and double cross-coupled oscillator circuit topologies were derived in [55, 56].

As examples, analytical derivations of phase noise in multiphase and quadrature voltage controlled oscillators (QVCOs) have been reported in [57, 58]; phase noise analyses in ring oscillators have been addressed in [17, 59-61]; moreover, phase noise in relaxation oscillators has been studied in [17, 62, 63].

In our previous studies reported in Chapter 2 and therein [OP2, OP7, OP8], the differential Armstrong oscillator circuit topology was compared in terms of phase noise performance with common-source cross-coupled, Colpitts, and Hartley differential circuit topologies at operating frequencies in the range from 1 to 100 GHz. The differential Armstrong topology proposed therein exploits integrated transformers [6, 31, 64] in order to implement magnetic coupling between the gate and drain terminals of the transistor pair in the oscillator. Under the adopted design conditions, common to all topologies, the Armstrong topology showed a good potential for superior phase noise performance in the oscillation frequency range from 1 to 20 GHz. As a consequence of our previous studies, an in-depth investigation of phase noise is in order, since it may allow us to get useful insights.

To date, to the best of our knowledge, an in-depth study of phase noise in Armstrong oscillator circuit topology, either differential or not, through analytical investigations of phase noise has not been addressed yet in the literature.

In this chapter we address a complete analytical study of phase noise in the differential Armstrong topology shown in Fig. 3.1, with the objective of providing a closed-form symbolic expression for the phase noise by using the ISF. In detail, in this chapter we report a theoretical analysis of the phase noise exhibited by the differential Armstrong oscillator topology shown in Fig. 3.1, in both the $1/f^3$ and $1/f^2$ regions. The analytical expressions derived by our theoretical study are then validated through the comparison with the results of the circuit simulations carried out within the Cadence design environment, which takes into account the full models of the transistors of a process design kit commercially available, including all their parasitic components. In compliance with the expectations from the theoretical study, in our analyses we will exclude the effects of the layout interconnections; moreover, it is worth considering that the additional parasitic components introduced by the layout could lead to an unjustified increase of complexity and cumbersome expressions that could mask the topological properties that we would like bringing to the light in our study. Capacitors will be considered as ideal components, whereas a typical quality factor (Q) of 10 is considered for all the spiral inductors. The assumptions made above are reasonable in a first-order approximation and in line with the common practice adopted by other theoretical studies reported in the literature. From the comparison with the simulation results we will see that the results of our study are characterized by a good accuracy.

The chapter is organized as follows. In Section 3.1 an expression for the oscillation frequency is derived. Section 3.2 reports the analysis of phase noise for the differential Armstrong topology of Fig. 3.1. In Section 3.3 the theoretical results are validated by the results obtained from SpectreRF simulations for the oscillation frequencies of 1, 10, 100 GHz. Finally, conclusions are drawn in Section 3.4.

The key contents of this chapter have been reported in original contributions published in an international peer-reviewed journal [OP4]. Moreover, the phase noise analysis method reported in this chapter has also been applied to a 67 GHz LC oscillator exploiting a three-spiral transformer. The results have been published therein [OP5].

3.2 Oscillation Frequency

Fig. 3.1 shows the differential Armstrong oscillator circuit topology designed in 28 nm bulk CMOS technology with 1 V supply voltage. In order to make the results directly comparable with those reported in the previous chapters, the oscillator circuit design has been carried out with the same transistor size, power and current consumptions, inductance of the tanks and their quality factors, as in Chapters 1, 2 and therein [OP2, OP7, OP8]. In particular, the width and length of transistor pair M_1 is 15 μm and 28 nm, respectively. The dc bias voltage and current

sources V_{B1} and I_{B1}, respectively, in Fig. 3.1 are chosen such that the total power consumption is 6.3 mW for all oscillation frequencies. In addition, a typical coupling factor k of 0.85 is assumed for the transformers. In order to exclude noise from the bias circuitry being converted to phase noise, V_{B1} and I_{B1} are chosen to be ideal and noiseless. This will allow a direct verification of the theoretical analysis carried out in Section 3.3 with the SpectreRF simulation results reported in Section 3.4.

Fig. 3.2 (a) shows the equivalent half-circuit of Fig. 3.1. The small-signal equivalent of the half-circuit of Fig. 3.1 is reported in Fig. 3.2 (b). The oscillator loop is broken at the gate of M_1 and a voltage source V_{in} is inserted at this point. This equivalent circuit is obtained by considering the simplified transistor model with the small-signal transconductance (g_m), gate-to-source capacitance (C_{gs}), gate-to-drain capacitance (C_{gd}), source-to-bulk capacitance (C_{sb}) and drain-to-bulk capacitance (C_{db}). In the interest of a low complexity of the derived equations, the small-signal output resistance r_o of M_1 is neglected. For the same reason, C_{gd} will be broken into two equivalent capacitances according to the Miller effect. An effective capacitance C_a equal to $(1+g_m r_o)\times C_{gd}$ appears at the gate of M_1 and an effective capacitance C_b equal to $(1+1/(g_m r_o))\times C_{gd}$ appears at the drain of M_1. Moreover, R_1 and R_2 can be neglected assuming a high Q for L_1 and L_2. Later, we will see that this working hypothesis is acceptable.

C_1 appears in parallel with C_{db} and C_b, and C_2 appears in parallel with C_{gs} and C_a. Their sum can be represented as an equivalent capacitance C_1' and C_2' respectively.

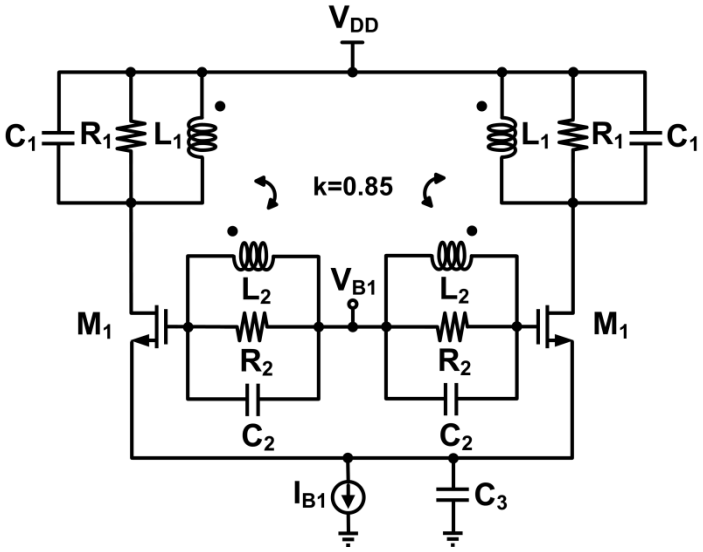
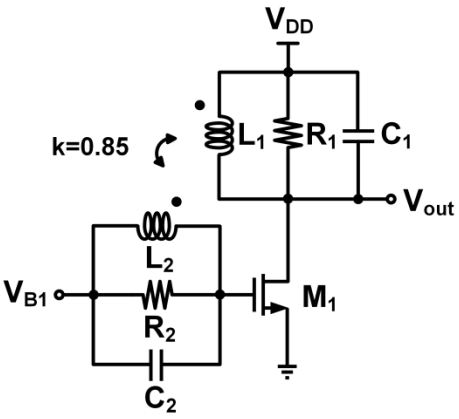
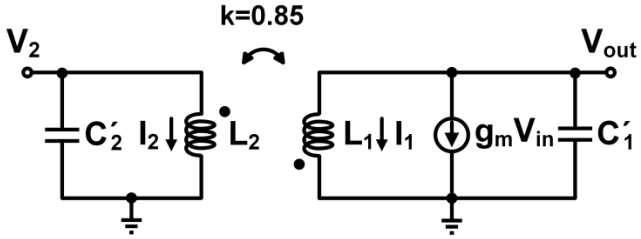


Fig. 3.1. Schematic of the differential Armstrong oscillator circuit topology. V_{B1} and I_{B1} are dc bias voltage and current sources respectively.



(a)



(b)

Fig. 3.2. (a) Equivalent half-circuit of the differential Armstrong topology shown in Fig. 3.1. (b) Small-signal equivalent circuit of Fig. 3.2 (a).

From Fig. 3.2 (b) we yield

$$V_{out} = I_1 sL_1 + I_2 Ms \tag{3.1}$$

$$V_2 = I_2 sL_2 + I_1 Ms \tag{3.2}$$

$$-I_2 = V_2 sC_2' \tag{3.3}$$

$$g_m V_{in} + I_1 + V_{out} sC_1' = 0 \tag{3.4}$$

From (3.2) and (3.3) we derive

$$I_2 = -\frac{Ms}{\frac{1}{sC_2'} + sL_2} I_1 \tag{3.5}$$

From (3.1) and (3.5) we can write

$$I_1 = -\frac{1}{sL_1 - \dfrac{M^2 s^2}{\dfrac{1}{sC_2'} + sL_2}} V_{out} \tag{3.6}$$

Finally, from (3.4) and (3.6) we derive the open-loop transfer function V_{out}/V_{in}

$$\frac{V_{out}}{V_{in}} = \frac{L_1 g_m (C_2' L_2 - C_2' L_2 k^2)\omega^2 - L_1 g_m}{(C_1' C_2' L_1 L_2 - C_1' C_2' L_1 L_2 k^2)\omega^4 + (-C_1' L_1 - C_2' L_2)\omega^2 + 1} \omega j \tag{3.7}$$

Equivalently, V_{out}/V_{in} can be written as

$$\frac{V_{out}}{V_{in}} = \frac{X_1 + jY_1}{X_2 + jY_2} \tag{3.8}$$

where $X_{1,2}$ and $Y_{1,2}$ are the real and imaginary parts of the numerator and denominator of V_{out}/V_{in}, respectively.

The Barkhausen criterion for oscillation leads to $\angle H(j\omega)=0^o$ at the oscillation frequency f_0. Thereby, at f_0 we have that

$$X_2 Y_1 - X_1 Y_2 = 0 \tag{3.9}$$

By solving this equation, we derive the following expression for f_0

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{1}{2} \frac{C_1' L_1 + C_2' L_2 - \sqrt{(C_1' L_1 - C_2' L_2)^2 + 4 C_1' C_2' L_1 L_2 k^2}}{C_1' C_2' L_1 L_2 (1 - k^2)}} \tag{3.10}$$

Fig. 3.3 shows the results obtained by the theoretical expression of the oscillation frequency provided by (3.10), as a function of C_1. Note that the oscillation frequency predicted by (3.10) closely follows the simulation results obtained by SpectreRF. In particular, the maximum difference amounts to about 80 MHz, observed for C_1=380 fF. Thereby, the aforementioned simplifications in the derivation of (3.10) are justified for an accurate first-order prediction of the oscillation frequency f_0.

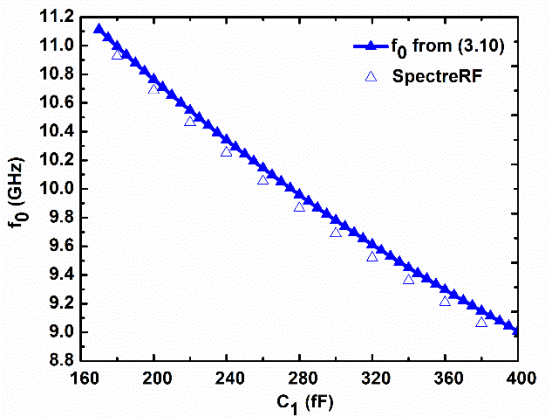


Fig. 3.3. Oscillation frequency values vs. C_1 for the circuit of Fig. 3.1, predicted by (3.10), and simulated in SpectreRF for an oscillation frequency in the vicinity of 10 GHz.

3.3 Phase Noise Analysis

In our study we aim at extending the analysis to the $1/f^3$ phase noise region, not addressed yet in the literature, since such an analysis would be essential in order to achieve a good phase noise prediction in oscillator topologies designed in deep submicron (nano-scale) technologies. Indeed, flicker noise in the output spectrum of an integrated CMOS oscillator is particularly important since the $1/f^3$ phase noise region usually extends beyond 1 MHz offset from the oscillation frequency, as a consequence of nano-scale devices featuring 1/f corner frequencies of several tens or hundreds of megahertz.

In order to have expressions in a more manageable form, in an analogy with [54] it is convenient to change the ground reference as shown in Fig. 3.4. By using the describing function approach [65], we achieve the single-ended large-signal equivalent circuit shown in Fig. 3.5.

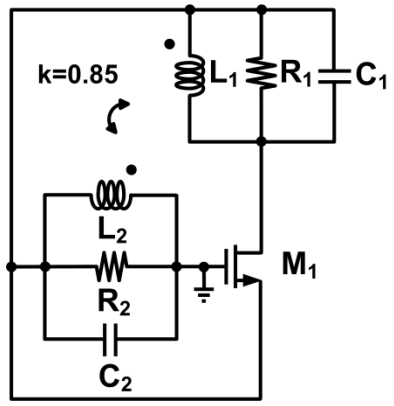


Fig. 3.4. Single-ended large-signal equivalent circuit of the differential Armstrong oscillator circuit topology of Fig. 3.1, with changed ground reference.

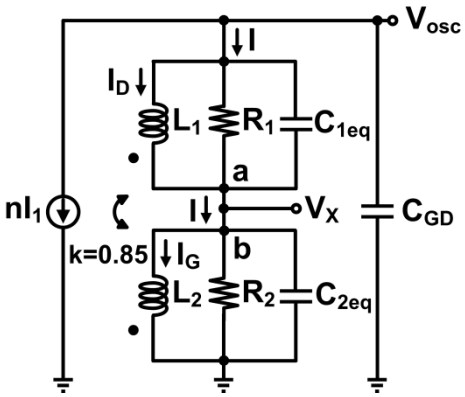


Fig. 3.5. Single-ended large-signal equivalent circuit of the differential Armstrong oscillator circuit topology of Fig. 3.1, based on the describing-function approach.

I_1 is the amplitude of the fundamental harmonic of the drain current of M_1. Denoting the drain and gate resonator impedances as Z_D and Z_G respectively, n is defined as the ratio $Z_G/(Z_D+Z_G)$. C_{GD} is the large-signal capacitance between gate and drain of M_1, which can be either a parasitic component or external to the transistor itself. C_{1eq} represents the parallel combination of C_1 with the large signal drain-to-bulk capacitance C_{DB} of M_1, whereas C_{2eq} is the parallel combination of C_2 with the large-signal gate-to-source capacitance C_{GS} of M_1.

Defining M as $k\sqrt{L_1L_2}$ and Z_1, Z_2 as the impedances given by the parallel combination of R_1, C_{1eq} and R_2, C_{2eq} respectively

$$Z_1 = \frac{R_1}{1+sR_1C_{1eq}} \tag{3.11}$$

$$Z_2 = \frac{R_2}{1+sR_2C_{2eq}} \tag{3.12}$$

we can write

$$V_{osc} - V_X = L_1 s I_D + I_G M s \tag{3.13}$$

$$V_X = L_2 s I_G + I_D M s \tag{3.14}$$

From Kirchhoff current law (KCL) at the output node

$$I = -nI_1 - V_{osc} s C_{GD} \tag{3.15}$$

Moreover, from KCL at nodes a and b, respectively

$$I_D = I - \frac{V_{osc} - V_X}{Z_1} \tag{3.16}$$

$$I_G = I - \frac{V_X}{Z_2} \tag{3.17}$$

Then we use (3.15) into (3.16) and (3.17) in order to write I_D and I_G as function of V_{osc} and V_X, respectively, as follows

$$I_D = -nI_1 - V_{osc} s C_{GD} - \frac{V_{osc} - V_X}{Z_1} \tag{3.18}$$

$$I_G = -nI - V_{osc} s C_{GD} - \frac{V_X}{Z_2} \tag{3.19}$$

Using (3.18) and (3.19) into (3.13) and (3.14), we can express V_{osc} and V_X as a function of circuit components with known values. Afterwards, expressing Z_D and Z_G as $(V_{osc}-V_X)/I$ and V_X/I respectively, and then summing, we yield

$$Z_D + Z_G = \frac{\left(L_1 L_2 - M^2\right)\left(Z_1 + Z_2\right)s^2 + Z_1 Z_2 \left(L_1 + L_2 + 2M\right)s}{\left(L_1 L_2 - M_2\right)s^2 + \left(L_1 Z_2 + L_2 Z_1\right)s + Z_1 Z_2} \tag{3.20}$$

Z_D+Z_G can be interpreted as a parallel RLC resonator made of an inductance $L_T=L_1+L_2+2M$, a resistance $R_T=R_1+R_2$, and a capacitance $C_p=C_{GD}+C_{1eq}C_{2eq}/(C_{1eq}+C_{2eq})$ [54].

We now define $\Gamma_{eff,rms}$ and $\Gamma_{eff,dc}$ as the rms and dc values of the effective impulse sensitivity function (ISF) for the noise current of M_1 [22, 36]. Using $\Gamma^2_{eff,rms}$ in (31) and $\Gamma^2_{eff,dc}$ in (33) from [36], as corrected in [66], and equating we find

$$\Gamma^2_{eff,dc} = \frac{\omega_{1/f^3}}{\omega_{1/f}} \Gamma^2_{eff,rms} \tag{3.21}$$

where ω_{1/f^3} is the frequency where the sideband power due to thermal noise is equal to the sideband power due to flicker noise, and $\omega_{1/f}$ is the corner frequency of the flicker noise generated by M_1. From [22] $\Gamma^2_{eff,rms}$ is given by

$$\Gamma^2_{eff,rms} = \frac{(1-n)^2}{N^2} \frac{I_1}{2\left(\mu_n C_{ox} \frac{W}{L}\right)V_1^2} \tag{3.22}$$

where C_{ox} is the gate oxide capacitance per unit area approximately equal to 0.026 F/m^2, W and L are the width and length of M_1 respectively, and V_1 is the amplitude of the fundamental harmonic of the source voltage of M_1.

The phase noise due to flicker noise from M_1 can be written as

$$\mathcal{L}(\Delta\omega)\Big|_{flicker} = N\frac{1}{2q_{max}^2\Delta\omega^2}\Gamma_{eff,dc}^2\frac{\overline{i_n^2}}{\Delta f}\frac{1}{(\cos\phi-\cos\Phi)^2} \tag{3.23}$$

where N=2 for the differential Armstrong, q_{max} is the maximum charge displacement across the tank capacitance equal to $V_{tank}\times C_p$, V_{tank} being the amplitude of the fundamental harmonic of the tank voltage. $\Delta\omega$ is the angular frequency offset from the oscillation frequency, and Φ is half the conduction angle defined by

$$\Phi = cos^{-1}\left(\frac{V_{GS}-V_T}{V_1}\right) \tag{3.24}$$

where ϕ is equal to $\omega_0 t$, V_{GS} is the direct current (dc) gate-to-source voltage of M_1 and V_T is the threshold voltage of M_1. Also, $\overline{i_n^2}/\Delta f$ is the power spectral density of the flicker noise current of M_1 reported in [67, 68]

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{Kg_{m1}^2}{C_{ox}WL}\frac{1}{f} \tag{3.25}$$

where K is a process-dependent constant approximately equal to 10^{-23} V^{2}F, f is the frequency, and g_{m1} is the small-signal transconductance of M_1 given by

$$g_{m1} = \left(\mu_n C_{ox}\frac{W}{L}\right)V_1(\cos\phi-\cos\Phi) \tag{3.26}$$

where μ_n is the electron mobility approximately equal to 0.06 m^2/(V×s).

Moreover, from [65] we can write

$$V_1 = I_1\frac{R_T n}{n^2 G_{m1}R_T+1} \tag{3.27}$$

$$V_{tank} = \frac{V_1}{n} \tag{3.28}$$

where G_{m1} is the large-signal transconductance of M_1 equal to I_1/V_1.

Also, from [22] g_{m1} is proportional to G_{m1}

$$G_{m1} = \frac{2}{15\pi}\Phi^5\left(1-\frac{11}{42}\Phi^2\right)\frac{1}{\left(\cos\Phi-\cos\phi\right)}g_{m1} \tag{3.29}$$

The phase noise given by (3.23) can now be rewritten as

$$\mathcal{L}(\Delta\omega)\Big|_{flicker} = \frac{\pi(1-n)^2 K\mu_n}{2N}\frac{\omega_{1/f^3}}{\omega_{1/f}}\frac{1}{\Delta\omega^3}\frac{n^2 G_{m1}R_T+1}{V_{tank}R_T C_p^2 L^2} \tag{3.30}$$

It is worth noting that, as it could be expected intuitively, a higher V_{tank} will result in lower flicker noise from M_1 being up-converted into phase noise. Moreover, (3.29)-(3.30) suggest that the larger the excess gain $g_{m1}R_T$, the more pronounced is the flicker noise up-conversion. This can be attributed to the increase of the harmonic distortion of the output voltage, due to noise current tones modulating the amplitude of the voltage harmonics. In turn, this effect causes changes in the oscillation frequency, thereby producing phase noise as explained in [44].

Phase noise due to thermal noise can be expressed as [22, 54]

$$\mathcal{L}(\Delta\omega)\Big|_{thermal} = \frac{K_B T\left(1+\gamma\frac{1-n}{n}\right)}{V_{tank}^2 C_p^2 \Delta\omega^2 R_T} \tag{3.31}$$

where K_B is the Boltzmann constant, T is the absolute temperature, and γ is the excess noise coefficient.

The overall phase noise is given by

$$\mathcal{L}(\Delta\omega)\Big|_{total} = 10\log_{10}\left[\mathcal{L}(\Delta\omega)\Big|_{flicker} + \mathcal{L}(\Delta\omega)\Big|_{thermal}\right] \tag{3.32}$$

In the next section, the phase noise predicted by (3.30)-(3.32) will be compared with the results from circuit simulations carried out within the Cadence design environment.

3.4 Numerical Evaluations and Circuit Simulations

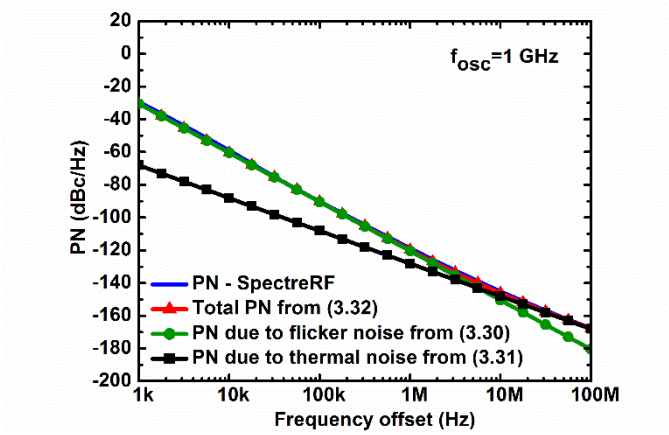
For simplicity we assume that the drain and gate resonators are identical, neglecting the possible slight difference in parasitic capacitance in the resonators. This means that n is a real number and equal to 0.5. As in Chapter 2 and therein [OP2, OP7, OP8], L_1 and L_2 are chosen equal to 5 nH, 500 pH and 50 pH for the oscillation frequencies of 1, 10 and 100 GHz, respectively.

Assuming that the losses due to the parasitic resistance of the inductors L_1 and L_2 dominate the losses in the drain and gate resonators, the parasitic resistors R_1 and R_2 are equal to $QL_1\omega$ and $QL_2\omega$, respectively. Q is equal to 10 and ω is the angular frequency of operation. C_1 and C_2 are equal to 2.5 pF, 231 fF and 8 fF for the operating frequencies of 1, 10 and 100 GHz, respectively. C_3 is equal to 1 μF, in order to exhibit small impedance toward ground at the frequency of oscillation.

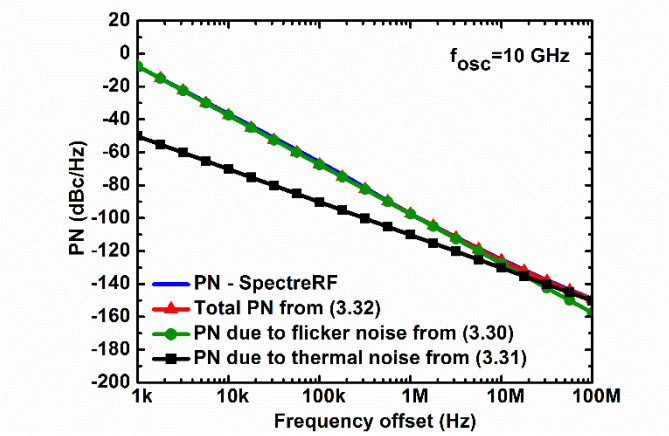
Figs. 3.6 (a)-(c) show the phase noise obtained by direct plots from periodic steady state (PSS) and periodic noise (Pnoise) circuit simulations in SpectreRF, for oscillation frequencies of 1, 10 and 100 GHz. Phase noise is reported over a wide frequency offset from the carrier frequency, in order to include the regions in which the noise at the output spectrum is dominated by either flicker or thermal noise.

Figs. 3.6 (a)-(c) report also the numerical evaluations of the theoretical expressions of phase noise due to flicker and thermal noise from (3.30) and (3.31) respectively, as well as the total phase noise from (3.32). Note that the theoretical phase noise predicted by (3.30)-(3.32) matches well with the results obtained by means of SpectreRF simulations. Even for the oscillation frequency of 100 GHz, where the worst match is observed, the theoretical phase noise predicted by (3.32) is within 3 dB difference from the simulation results.

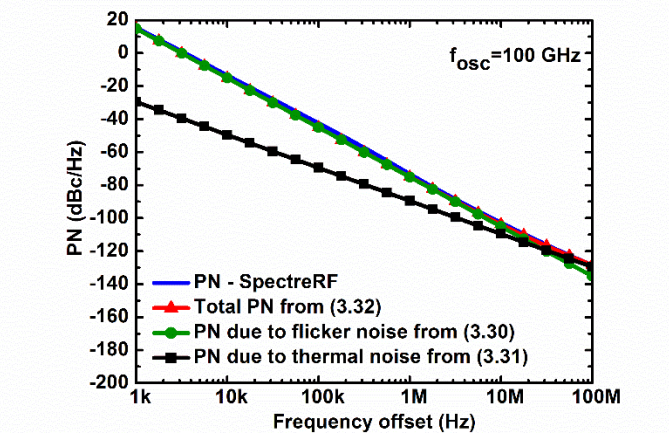
In all cases considered here, the $1/f^3$ frequency corner is beyond 1 MHz frequency offset. In particular it is at the frequency offset of 5.8, 18, and 28 MHz from the oscillation frequencies of 1, 10 and 100 GHz, respectively. These last results confirm the rising role of flicker noise in oscillators designed in a nano-scale CMOS technology, as already shown in Chapter 2 and therein [OP2, OP7, OP8]. This means that the devices with the largest contribution to the flicker noise component of phase noise will also dominate phase noise.



(a)



(b)



(c)

Fig. 3.6. Phase noise vs. frequency offset obtained from direct plots through PSS and Pnoise SpectreRF simulations, as well as from the theoretical expressions of (3.30)-(3.32) for an oscillation frequency of: (a) 1 GHz; (b) 10 GHz; (c) 100 GHz.

3.5 Conclusions

The analytical expression of the oscillation frequency for a differential Armstrong oscillator circuit topology was derived by means of circuit theory and validated by means of the results provided by SpectreRF simulations in Cadence.

Moreover, this chapter reports for the first time, a theoretical analysis of the phase noise in a differential Armstrong oscillator circuit topology, both in the $1/f^3$ and $1/f^2$ regions, in order to allow accurate predictions.

Flicker noise up-conversion has resulted explicitly linked to the excess gain of the oscillator circuit topology. Specifically, due to the non-linear nature of the topology, larger excess gain causes more flicker noise from the active devices in the circuit being up-converted near the oscillation frequency.

The derived analytical expressions of the phase noise have been validated through a direct comparison with the results obtained by SpectreRF simulations for a discrete set of oscillation frequencies spanning over two decades from 1 to 100 GHz. Under the adopted design conditions, the theoretical and simulation results are in a good agreement, with a maximum deviation of about 3 dB at 100 GHz.

Finally, the analysis of the results obtained by the theoretical derivations allowed us to identify the dominant noise contributions. It can be observed that in all cases, the flicker noise from the active devices is the component with the most significant effect in terms of phase noise on the oscillator output spectrum at 1 MHz offset from the carrier frequency.

Chapter 4

Phase Noise Reduction Techniques in the Colpitts Topology

4.1 Introduction

Modern wireless and wireline data communication systems impose severe requirements on phase noise (PN) at a given frequency offset from the carrier [2, 5, 8].

Recently, accurate analysis of the behavior of oscillator circuits has been the subject of intense investigation. An effective method for providing qualitative and quantitative predictions of phase noise in integrated oscillators is based on the Impulse Sensitivity Function (ISF) [36].

In Chapter 1 and therein [OP1, OP6], the derivation of accurate evaluations of the ISF in relation to simulation settings was addressed. Moreover, the topological investigations, carried out in Chapter 1 and therein [OP1, OP6] under common design conditions in 28 nm CMOS technology for an oscillation frequency of 10 GHz, showed that the common-source cross-coupled differential pair oscillator circuit topology exhibited better phase noise performance with respect to Colpitts and Hartley topologies. In Chapter 1 and therein [OP1], the comparison was extended also to a range of frequencies between 1 and 100 GHz, under the same design conditions, taking into account both flicker and thermal noise contributions to phase noise. The results showed for the first time that there is no best topology in the absolute sense as it may have appeared from previous studies reported in the literature limited to oscillators operating at a few gigahertz, but the opportunity of identifying the topology exhibiting the lowest phase noise depends on the operating frequency range. Moreover, the use of the ISF allowed the separation of the total phase noise in its two components due to flicker and thermal noise from each device in the oscillator circuit. In particular, it was observed how the tail transistor plays a significant role in the phase noise degradation occurring in the Colpitts oscillator circuit topology, here shown in Fig. 4.1.

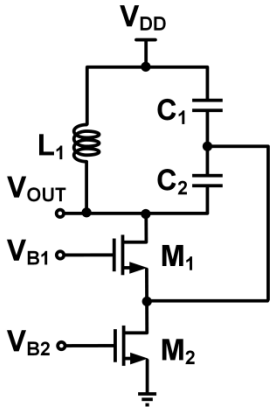


Fig. 4.1. Single-ended Colpitts oscillator circuit topology. V_{B1} and V_{B2} are dc bias voltages.

In the past years, an effective technique for the reduction of phase noise due to the tail transistor in CMOS LC oscillators was proposed. Namely, the inductive degeneration of the tail transistor.

This technique was proposed in [69, 70]. It consists of introducing an off-chip inductance of 100 μH as a degeneration impedance to the source node of the tail transistor in a common-source cross-coupled differential pair oscillator circuit topology operating around 2 GHz and implemented in 0.35 μm CMOS technology.

Moreover, the technique of noise filter was proposed in [46, 71, 72] for the reduction of phase noise due to the tail transistor in CMOS LC oscillators. In particular, it was shown to reduce the up-conversion of low-frequency noise. It consists of replacing the tail transistor with a band-stop filter, referred therein [46, 71, 72] as noise filter, in a common-source cross-coupled differential pair oscillator operating close to 1.1 GHz and fabricated in 0.35 μm CMOS technology.

These techniques for the reduction of phase noise due to the tail transistor are here applied to the Colpitts oscillator circuit topology of Fig. 4.1. In particular, these techniques will be adopted and analyzed for a single-ended Colpitts topology designed in a 28 nm bulk CMOS process.

Our analyses will allow us to show mathematically and prove by means of simulations that there is a specific degeneration inductance value for M_2 in Fig. 4.1, for which the phase noise of the Colpitts oscillator reaches a minimum. Furthermore, that there is a specific inductance value which tunes the resonance frequency of the noise filter to the oscillation frequency and for which the phase noise reaches a minimum, confirming the discussion in [71], as well as to derive the dependence of the oscillation frequency on the filter components. Minimizing the flicker noise in the output spectrum is particularly important since the $1/f^3$ phase noise region of integrated CMOS oscillators usually extends beyond 1 MHz offset from the oscillation frequency [OP1, 44], as a consequence of the deep sub-micrometer devices featuring 1/f corner frequencies of several tens or hundreds of megahertz.

Moreover, a third technique, namely optimum current density, for phase noise reduction will be proposed and analyzed in detail. It consists of biasing an oscillator circuit topology with the optimum bias current density for minimum phase noise. This technique of the optimum bias current density applied to specific metrics of interest has been extensively used for the design of low noise amplifiers (LNAs) with minimum noise figure and the design of power amplifiers (PAs) with a maximum linearity range [73-75]. In a few cases it has been also mentioned in achieving low phase noise in differential Colpitts and common-source cross-coupled differential pair oscillators [76-78]. Here, it will be applied to a single-ended Colpitts oscillator circuit topology with the objective of providing adequate theoretical proofs of the benefits for its extensive use in oscillators as well. Our analyses will allow for the first time to gain insight into the theoretical details of this technique and its effective applications.

Overall, the primary objective of this study reported here is to analyze by circuit theory and verify by circuit simulations, compare the results and highlight the benefits emerging from the aforementioned phase noise reduction techniques applied to the Colpitts oscillator circuit topology. In particular, in our theoretical analyses we will consider the equivalent circuit of the transistors with the typical parameters of a typical 28 nm bulk CMOS technology commercially available. The details of the equivalent circuits will be given in the related sections. Whereas, circuit simulations will be carried out within the Cadence design environment which takes into account the full models of the transistors of a process design kit commercially available, including all their parasitic components related to their actual size. In our analyses we will exclude the effects of the layout interconnections, since the additional parasitic components introduced by the layout could mask the results of the topological properties that we would like bringing to the light in this chapter. Capacitors will be considered as ideal components, whereas a typical quality factor (Q) of 10 will be considered for all the spiral inductors. Since the quality factor of the LC tank has a heavy impact on the phase noise, this common condition will assure that all the oscillator circuits will be compared under common conditions [7, 40, 79].

The chapter is organized as follows. Section 4.2 addresses the inductive degeneration of the tail current transistor in a Colpitts oscillator. The analytical expressions of the oscillation frequency and the optimum inductance are derived by means of circuit theory and validated by means of the results provided by SpectreRF simulations in Cadence. Section 4.3 addresses the noise filter technique where the tail current transistor is replaced by a passive band-stop filter, i.e. noise filter. The analytical expressions of the oscillation frequency and the optimum inductance are also derived by means of circuit theory and compared with the results obtained by means of SpectreRF simulations. Section 4.4 addresses the optimum current density for minimum phase noise for the Colpitts oscillator circuit topology under examination. The theoretical results are validated by the results obtained from SpectreRF simulations for the oscillation frequencies of 10 and 100 GHz. Finally, conclusions are drawn in Section 4.5.

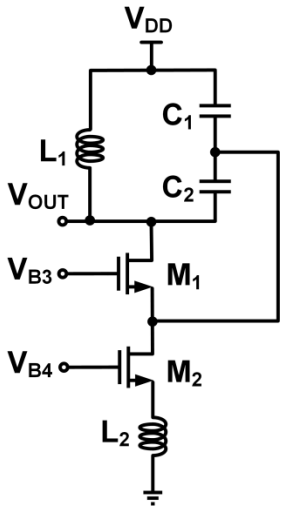
The key contents of this chapter have been reported in original contributions published in an international peer-reviewed journal and in conference proceedings [OP3, OP9, OP11].

4.2 Inductive Degeneration

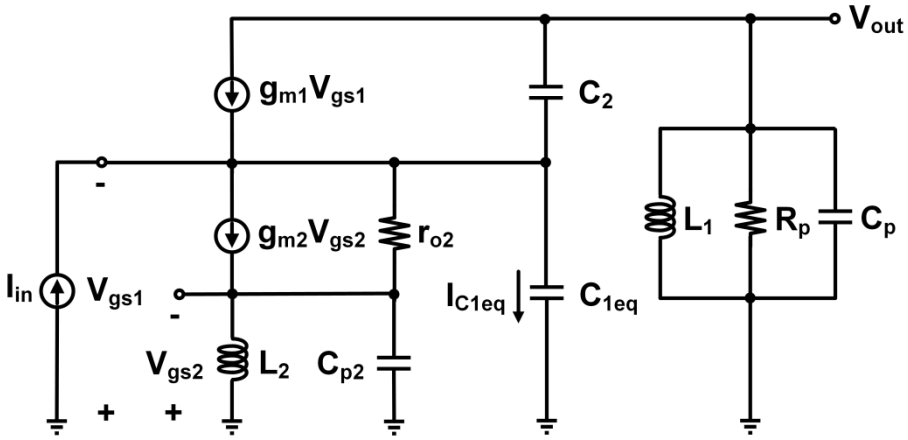
In this section we will derive an analytical expression for the oscillation frequency (f_0) of the Colpitts oscillator circuit topology in which we introduced an inductive degeneration (L_2) to the source node of the tail current transistor (M_2), as shown in Fig. 4.2 (a). Moreover, we will observe that there is an optimum inductance value for which the oscillator circuit topology exhibits a minimum phase noise and will calculate such an optimum inductance.

In order to extract appropriate evaluations about the improvement of performance with respect to the traditional topology of Fig. 4.1, the oscillator circuit design will be carried out under the same transistor size, power and current consumptions, inductance of the tanks and their

quality factors, as in Chapters 1, 2 and therein [OP1, OP2, OP6-OP8]. Specifically, the transistor width is 30 μm, whereas the power consumed is 6.3 mW. The tank inductance is equal to 500 pH for operation at 10 GHz and 50 pH for operation at 100 GHz.



(a)



(b)

Fig. 4.2. (a) Colpitts oscillator circuit topology incorporating an inductive degeneration (L_2) to the source node of the tail current transistor (M_2). V_{B3} and V_{B4} are dc bias voltages. (b) Small-signal equivalent circuit. I_{in} is the input current stimulus used for the calculation of the closed-loop gain V_{out}/I_{in}.

4.2.1 Oscillation Frequency

The Colpitts oscillator circuit topology with an inductively degenerated tail current transistor (M_2) is shown in Fig. 4.2 (a). Its small-signal equivalent circuit is shown in Fig. 4.2 (b). This equivalent circuit is obtained by considering the simplified transistor model with the small-signal transconductance (g_m), gate-to-source capacitance (C_{gs}), gate-to-drain capacitance (C_{gd}), source-to-bulk capacitance (C_{sb}), drain-to-bulk capacitance (C_{db}) and output resistance (r_{o2}). In the

interest of a low complexity of the derived equations, the small-signal output resistance r_{o1} of M_1 as well as the polysilicon gate resistance r_g of M_1 and M_2, are neglected. Later, we will see that this working hypothesis is acceptable. If the small-signal output resistance r_{o2} of M_2 is also neglected, it can be proved that the oscillation frequency f_0 does not depend on L_2. Thereby, in order to take into account the effect of L_2 in f_0, r_{o2} is considered in the equivalent circuit. R_p represents the total load resistance of the LC tank, including the effect of the finite Q and the resistance seen from the source of M_1 scaled by the capacitive divide factor. C_p is the parasitic capacitance at the drain node of M_1, equal to the sum of C_{db1} and C_{gd1}. C_{p2} is the parasitic capacitance at the source node of M_2, equal to the sum of C_{gs2} and C_{sb2}. C_1 appears in parallel with C_{gs1}, C_{sb1}, C_{gd2} and C_{db2}. Their sum can be represented as an equivalent capacitance C_{1eq}.

In order to excite the circuit into oscillation we insert a current stimulus I_{in} at the source of M_1. We can now write that

$$C_p = C_{db1} + C_{gd1} \tag{4.1}$$

$$C_{p2} = C_{gs2} + C_{sb2} \tag{4.2}$$

$$C_{1eq} = C_1 + C_{gs1} + C_{sb1} + C_{gd2} + C_{db2} \tag{4.3}$$

From Kirchhoff current law (KCL) at the source of M_2 it derives that

$$g_{m2}V_{gs2} + \frac{-V_{gs1} + V_{gs2}}{r_{o2}} + \frac{V_{gs2}}{sL_2} + V_{gs2}sC_{p2} = 0 \tag{4.4}$$

By applying the KCL at the source of M_1, we can write

$$g_{m2}V_{gs2} - I_{in} + \frac{-V_{gs1} + V_{gs2}}{r_{o2}} + I_{C_{1eq}} + \frac{V_{out}}{sL_1} + \frac{V_{out}}{R_p} + V_{out}sC_p = 0 \tag{4.5}$$

Solving (4.4) with respect to V_{gs2} and combining with (4.5), we obtain

$$I_{C_{1eq}} = I_{in} - \left[\frac{1}{g_{m2} + \frac{1}{r_{o2}} + \frac{1}{sL_2} + sC_{p2}} \frac{1}{r_{o2}} \left(g_{m2} + \frac{1}{r_{o2}} \right) - \frac{1}{r_{o2}} \right] \times V_{gs1} - \left(\frac{1}{sL_1} + \frac{1}{R_p} + sC_p \right) V_{out} \tag{4.6}$$

Additionally, V_{gs1} is given by

$$V_{gs1} = -I_{C_{1eq}} \frac{1}{sC_{1eq}} \tag{4.7}$$

Moreover, from KCL at the output node

$$g_{m1}V_{gs1} + \left(V_{out} + V_{gs1}\right)sC_2 + \frac{V_{out}}{sL_1} + \frac{V_{out}}{R_p} + V_{out}sC_p = 0 \tag{4.8}$$

which can be expressed as a function of V_{gs1} as follows

$$V_{gs1} = -\frac{1}{g_{m1} + sC_2}\left(sC_2 + \frac{1}{sL_1} + \frac{1}{R_p} + sC_p\right)V_{out} \tag{4.9}$$

Using (4.6) in (4.7), expressing the result as a function of V_{gs1}, and equating to (4.9), we can express the closed-loop transfer function V_{out}/I_{in} as a ratio. By equating the imaginary part of the denominator of V_{out}/I_{in} to zero, we find that the oscillation frequency is given by (4.10)-(4.13). To reduce the complexity of the expression, C_{p2} is neglected in the equation for f_0 reported hereinafter.

$$f_o = \frac{1}{2\pi}\omega_0 \tag{4.10}$$

$$\omega_o = \sqrt{\frac{N_1}{D_1}} \tag{4.11}$$

where

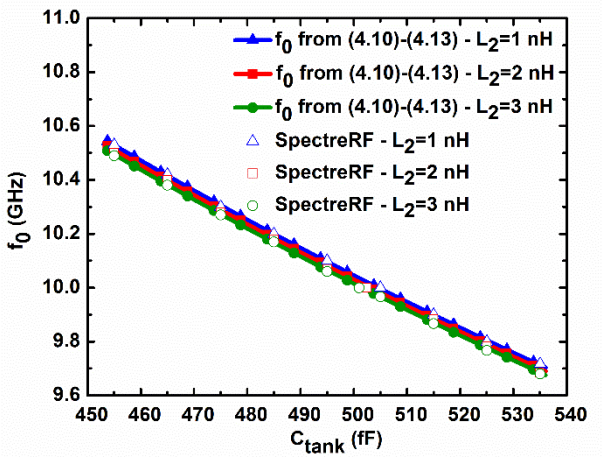
$$N_1 = \left(L_1 g_{m1} + C_{1eq}R_p + C_2R_p + L_2R_p g_{m1}g_{m2}\right)r_{o2} + L_1 + L_2R_p g_{m1} \tag{4.12}$$

$$\begin{aligned} D_1 = {} & \left(C_{1eq}C_2R_p + C_{1eq}C_pR_p + C_2C_pR_p + C_{1eq}L_2g_{m2} + C_2L_2g_{m2} + C_pL_2R_pg_{m1}g_{m2}\right)L_1r_{o2} + \\ & \left(C_{1eq} + C_2 + C_pR_pg_{m1}\right)L_1L_2 \end{aligned} \tag{4.13}$$

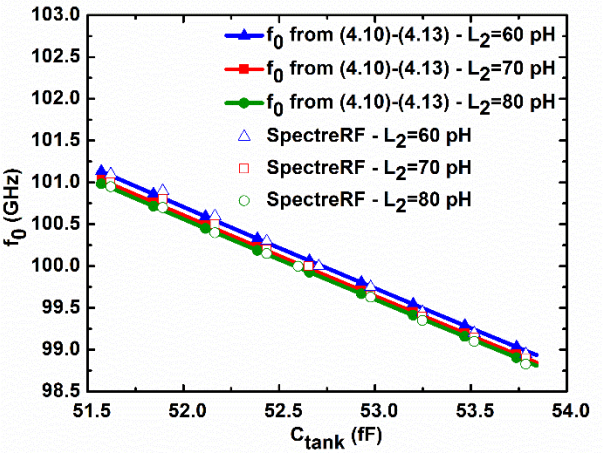
Figs. 4.3 (a)-(b) show the results obtained by theoretical expressions of the oscillation frequency provided by (4.10)-(4.13), as a function of the LC tank capacitance C_{tank} expressed as

$$C_{tank} = \frac{C_{1eq}C_2}{C_{1eq} + C_2} + C_p \tag{4.14}$$

The simulations are repeated for three values of L_2 in order to demonstrate the dependence of the oscillation frequency f_0 on L_2, which is shown being relatively weak. Note that the oscillation frequency predicted by (4.10)-(4.13) closely follows the simulation results obtained by SpectreRF. Thereby, the aforementioned simplifications in the derivation of (4.10)-(4.13) are justified for an accurate first-order prediction of the oscillation frequency f_0.



(a)



(b)

Fig. 4.3. Oscillation frequency values vs. C_{tank} for the circuit of Fig. 4.2 (a), predicted by (4.10)-(4.13), and simulated in SpectreRF for oscillation frequencies in the vicinity of (a) 10 GHz; (b) 100 GHz.

4.2.2 Optimum Inductance for Minimum Phase Noise

Here, our aim is to derive the value of L_2, for which the phase noise in the output spectrum of the Colpitts oscillator circuit topology of Fig. 4.2 (a) reaches a minimum. The theoretical results will be compared with respect to the simulation results obtained by means of SpectreRF.

From [65] we can write

$$C_{tank} = \frac{C_{1eq}C_2}{C_{1eq}+C_2} + C_p \tag{4.15}$$

$$V_1 = I_1 R_p (1-n) n \tag{4.16}$$

$$V_{tank} = \frac{V_1}{n} \tag{4.17}$$

where V_1 and I_1 are the amplitudes of the fundamental harmonics of the source voltage and drain current of M_1, respectively. V_{tank} is the amplitude of the fundamental harmonic of the tank voltage. G_{m1} is the large-signal transconductance of M_1 and n is the capacitive divide factor equal to $C_2/(C_{1eq}+C_2)$.

The power spectral density of the flicker noise current of M_1 can be written as follows [80]

$$\frac{\overline{i_d^2}}{\Delta f} = \frac{Kg_{m1}^2}{2\left(\mu_n C_{ox}\frac{W}{L}\right)C_{ox}L^2 f} \tag{4.18}$$

where K is a process dependent parameter, μ_n is the electron mobility, C_{ox} is the gate oxide capacitance per unit area, W and L are the width and length of M_1, respectively, and f is the frequency.

Moreover, the small-signal transconductance g_{m1} of M_1 and the phase noise for the Colpitts oscillator due to flicker or thermal noise from M_1 can be expressed as [22, 66, 81, 82]

$$g_{m1} = \left(\mu_n C_{ox}\frac{W}{L}\right)V_1\left(cos\phi - cos\Phi\right) \tag{4.19}$$

$$\mathcal{L}\left(\Delta\omega\right)\Big|_{flicker} = N\frac{1}{2q_{\max}^2\Delta\omega^2}\Gamma_{id,dc}^2\frac{\overline{i_d'^2}}{\Delta f} \tag{4.20}$$

where ϕ is equal to $\omega_0 t$, Φ is half the conduction angle defined by

$$\Phi = cos^{-1}\left(\frac{V_{GS}-V_T}{V_1}\right) \tag{4.21}$$

with V_{GS} and V_T being the dc gate-to-source voltage and the threshold voltage of M_1 respectively. Moreover, N=1 for the single-ended Colpitts, q_{max} is the maximum charge displacement across the tank capacitance, $\Delta\omega$ is the angular frequency offset from the oscillation frequency, $\frac{\overline{i_d'^2}}{\Delta f}$ is equal to $\frac{\overline{i_d^2}}{\Delta f}\times\frac{1}{cos\phi - cos\Phi}$ and $\Gamma_{id,dc}^2$ is the square dc value of the ISF given by [66, 81, 82]

$$\Gamma_{id,dc}^2 = \frac{\omega_{1/f^3}}{\omega_{1/f}}\Gamma_{id,rms}^2 \tag{4.22}$$

where $\Gamma_{id,rms}^2$ can be derived from [22]

$$\Gamma_{id,rms}^2 = \frac{1}{2\pi}\frac{(1-n)^2}{N^2}\left[\Phi - \frac{1}{2}sin(\Phi)\right] \tag{4.23}$$

Thereby, (4.20) now becomes

$$\mathcal{L}(\Delta\omega)\Big|_{flicker} = N\frac{1}{2q_{max}^2\Delta\omega^2}\frac{\omega_{1/f^3}}{\omega_{1/f}}\Gamma_{id,rms}^2\frac{\overline{i_d'^2}}{\Delta f} \tag{4.24}$$

In order to take into account the cyclostationarity of the noise from M_1, we replace $\Gamma_{id,rms}^2$ in (4.24) with $\Gamma_{id,eff,rms}^2$, that is the square rms value of the effective ISF [22, 36]

$$\Gamma_{id,eff,rms}^2 = \frac{(1-n)^2}{N^2}\frac{I_1}{2\left(\mu_n C_{ox}\frac{W}{L}\right)V_1^2} \tag{4.25}$$

Combining (4.18) and (4.19), the flicker noise current can be rewritten as follows

$$\frac{\overline{i_d^2}}{\Delta f} = \frac{K\left(\mu_n C_{ox}\frac{W}{L}\right)}{2C_{ox}L^2 f}V_1^2\left(cos\phi - cos\Phi\right)^2 = \frac{\overline{i_d'^2}}{\Delta f}\left(cos\phi - cos\Phi\right)^2 \tag{4.26}$$

Thereby, using (4.26) into (4.24) we yield

$$\mathcal{L}(\Delta\omega)\Big|_{flicker} = N\frac{1}{2q_{max}^2\Delta\omega^2}\frac{\omega_{1/f^3}}{\omega_{1/f}}\Gamma_{id,eff,rms}^2\frac{\overline{i_d^2}}{\Delta f}\frac{1}{\left(cos\phi - cos\Phi\right)^2} \tag{4.27}$$

Then we substitute $\frac{\overline{i_d^2}}{\Delta f}$ and $\Gamma_{id,eff,rms}^2$ in (4.27) as expressed by (4.18) and (4.25), respectively. Rearranging the result by using (4.15)-(4.17), we arrive in the following expression

$$\mathcal{L}(\Delta\omega)\Big|_{flicker} = \left|\frac{\pi(1-n)^2 K}{4N}\frac{\omega_{1/f^3}}{\omega_{1/f}}\frac{n^2 G_{m1}R_p + 1}{V_{tank}R_p C_{tank}^2\Delta\omega^3 C_{ox}L^2}\right| \tag{4.28}$$

In order to excite the Colpitts oscillator circuit topology of Fig. 4.2 (a) a stimulus can be applied to different nodes. The type of stimulus (voltage or current) must be chosen such that when it is set to zero, the circuit returns to its original topology [68]. The large-signal equivalent circuit of the Colpitts oscillator of Fig. 4.2 (a) is shown in Fig. 4.4.

V_{in} is a voltage stimulus applied to the gate of M_1. Transistor M_1 is represented as a transconductance amplifier according to the describing function analysis [65]. G_{m1} is the large-signal transconductance of M_1, equal to the ratio of the fundamental harmonic of the drain current of M_1 to the fundamental harmonic of the gate-source voltage of M_1. For transistor M_2 a simplified large-signal equivalent circuit is used [83, 84]. This equivalent circuit is obtained by considering the simplified transistor model with the large-signal transconductance (G_m), gate-to-source capacitance (C_{GS}), gate-to-drain capacitance (C_{GD}), source-to-bulk capacitance (C_{SB}), drain-to-bulk capacitance (C_{DB}) and output resistance (R_{DS}). G_{m2} is approximated by the average value of g_{m2} during the oscillation period. C_1 appears in parallel with C_{GD2} and C_{DB2}. Their sum can be represented as an equivalent large-signal capacitance C_{1EQ}. C_{P2} is the parasitic capacitance at the source node of M_2, equal to the sum of C_{GS2} and C_{SB2}. R_{DS2} is approximated by the average value of r_{o2} during the oscillation period. For simplicity of our analysis, it is assumed that, at the oscillation frequency of 10 GHz, extrinsic components as well as the gate and substrate resistances have a negligible effect to phase noise [85, 86]. Later we will verify that this assumption is acceptable.

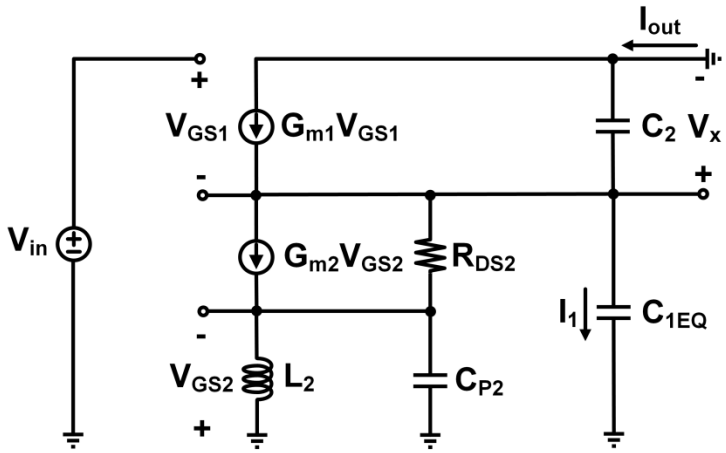


Fig. 4.4. Large-signal equivalent circuit of the Colpitts oscillator circuit of Fig. 4.2 (a). G_{m1} and G_{m2} are the large-signal transconductance of M_1 and M_2 respectively. V_{in} is a voltage stimulus applied to the gate of M_1.

We can now write

$$C_{1EQ} = C_1 + C_{GD2} + C_{DB2} \tag{4.29}$$

$$C_{P2} = C_{GS2} + C_{SB2} \tag{4.30}$$

We will now calculate the equivalent transconductance for the circuit of Fig. 4.4 with respect to the voltage stimulus V_{in}, i.e. $G_{m,eq1}=I_{out}/V_{in}$. Next, we will calculate the value of L_2, for which the flicker and thermal phase noise components at the output of the Colpitts oscillator circuit topology of Fig. 4.2 (a) reach the minimum values. For simplicity of the derived equations C_{P2} will be neglected.

From Kirchhoff voltage law (KVL)

$$V_{GS1} = V_{in} - V_x \tag{4.31}$$

then, from KCL at the source of M_2

$$I_{C_{1EQ}} - \frac{V_{GS2}}{sL_2} - I_{out} = 0 \tag{4.32}$$

which can be rewritten as

$$V_{GS2} = -I_{out} sL_2 + V_x s^2 L_2 C_{1EQ} \tag{4.33}$$

Moreover, from KCL at the source of M_1

$$V_x sC_2 - G_{m1} V_{GS1} + G_{m2} V_{GS2} + V_x sC_{1EQ} + \frac{V_x + V_{GS2}}{R_{DS2}} = 0 \tag{4.34}$$

Finally, from KCL at the drain of M_1

$$G_{m1} V_{GS1} - I_{out} - V_x sC_2 = 0 \tag{4.35}$$

Moreover, we can substitute V_{GS1} in (4.35) with its value given by (4.31). Using (4.31) and (4.33) into (4.34), solving with respect to V_x and substituting for V_x in (4.35), $G_{m,eq1}$ can be written as

$$G_{m,eq1} = \frac{N_2}{D_2} \tag{4.36}$$

$$N_2 = G_{m1}\left(C_{1EQ}L_2 + C_{1EQ}L_2 G_{m2} R_{DS2}\right)s^2 + C_{1EQ} G_{m1} R_{DS2} s + G_{m1} \tag{4.37}$$

$$\begin{aligned} D_2 = {} & \left(C_{1EQ}L_2 + C_2 L_2 + C_{1EQ}L_2 G_{m2} R_{DS2} + C_2 L_2 G_{m2} R_{DS2}\right)s^2 + \\ & \left(L_2 G_{m1} + C_{1EQ} R_{DS2} + C_2 R_{DS2} + L_2 G_{m1} G_{m2} R_{DS2}\right)s + G_{m1} R_{DS2} + 1 \end{aligned} \tag{4.38}$$

By replacing G_{m1} with $G_{m,eq1}$ in (4.28), taking the derivative with respect to L_2 and equating to zero, we find the value of L_2 for which the flicker noise present at the output of the Colpitts oscillator circuit topology of Fig. 4.2 (a) reaches a minimum, i.e.

$$L_2 = \left|\frac{N_3}{D_3}\right| \tag{4.39}$$

where

$$N_3 = \left(-C_{1EQ}R_pG_{m1}R_{DS2}n^2 - C_{1EQ}R_{DS2} - C_2R_{DS2}\right)s - R_pG_{m1}n^2 - G_{m1}R_{DS2} - 1 \tag{4.40}$$

$$D_3 = \left(C_{1EQ} + C_2 + C_{1EQ}G_{m2}R_{DS2} + C_2G_{m2}R_{DS2} + C_{1EQ}R_pG_{m1}n^2 + C_{1EQ}R_pG_{m1}G_{m2}n^2R_{DS2}\right)s^2 + \left(G_{m1} + G_{m1}G_{m2}R_{DS2}\right)s \tag{4.41}$$

A similar derivation can also be performed for the phase noise component due to the thermal noise of M_1, M_2, L_2 and the LC tank. From [22, 65] we have

$$G_{m1} = \frac{-I_1}{V_1} \tag{4.42}$$

$$I_1 = 2I_B\left(1 - \frac{\Phi^2}{14}\right) \tag{4.43}$$

where

$$I_B = \frac{\left(\mu_nC_{ox}\frac{W}{L}\right)V_1^2}{15\pi}\Phi^5\left(1 - \frac{4}{21}\Phi^2\right) \tag{4.44}$$

The phase noise expression due to the thermal noise is

$$\mathcal{L}(\Delta\omega)\Big|_{thermal} = \left|\frac{K_BT}{4NI_B^2R_p^3C_{tank}^2\Delta\omega^2}\left(1 - \frac{\Phi^2}{14}\right)^{-2} \times \left(\frac{\gamma}{n(1-n)} + \frac{1}{(1-n)^2} + \frac{n^2R_p\gamma G_{m2}}{(1-n)^2}\right)\right| \tag{4.45}$$

where K_B=1.38×10^{-23} V×C/K is the Boltzmann constant and T is the absolute temperature.

Combining (4.42) and (4.43), we get

$$V_1 = -\frac{1}{G_{m1}}2I_B\left(1 - \frac{\Phi^2}{14}\right) \tag{4.46}$$

Moreover, (4.44) can be rewritten as

$$V_1 = \left|\frac{15\pi}{\left(\mu_nC_{ox}\frac{W}{L}\right)}I_B\Phi^{-5}\left(1 - \frac{4}{21}\Phi^2\right)^{-1}\right|^{1/2} \tag{4.47}$$

Taking the absolute value of (4.46), equating to (4.47), and then solving with respect to I_B

$$I_B = \frac{15\pi}{\left(\mu_n C_{ox}\frac{W}{L}\right)}\frac{1}{4}G_{m1}^2\left(1-\frac{\Phi^2}{14}\right)^{-2}\Phi^{-5}\left(1-\frac{4}{21}\Phi^2\right)^{-1} \tag{4.48}$$

Afterwards, we substitute G_{m1} in (4.48) with the expression of $G_{m,eq1}$ given by (4.36)-(4.38), and then use the calculated value of I_B in (4.45). After taking the derivative of the resulting equation with respect to L_2 and equate to zero, we find that the value of L_2, for which the thermal noise at the output of the Colpitts oscillator circuit topology of Fig. 4.2 (a) reaches a minimum is

$$L_2 = \left|\frac{N_4}{D_4}\right| \tag{4.49}$$

where

$$N_4 = \left(-C_{1EQ}R_{DS2} - C_2R_{DS2}\right)s - G_{m1}R_{DS2} - 1 \tag{4.50}$$

$$D_4 = \left(C_{1EQ} + C_2 + C_{1EQ}G_{m2}R_{DS2} + C_2G_{m2}R_{DS2}\right)s^2 + \left(G_{m1} + G_{m1}G_{m2}R_{DS2}\right)s \tag{4.51}$$

The total phase noise expression is found by adding the flicker and thermal phase noise components given by (4.28) and (4.45) respectively as follows

$$\mathcal{L}(\Delta\omega)\Big|_{total} = 10log_{10}\left[\mathcal{L}(\Delta\omega)\Big|_{flicker} + \mathcal{L}(\Delta\omega)\Big|_{thermal}\right] \tag{4.52}$$

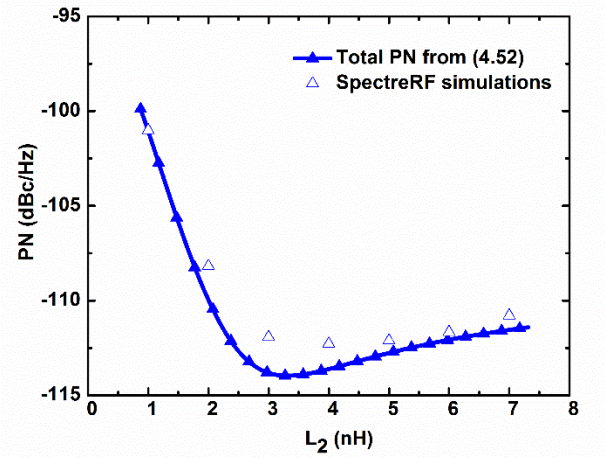
The total phase noise given by (4.52) is plotted in Figs. 4.5 (a)-(b) versus L_2, at an average bias current of 6.3 mA, for an oscillation frequency of 10 GHz, at a 1 MHz frequency offset. Note the agreement between the theoretical derivations and the SpectreRF simulations.

Thereby, the aforementioned simplifications in the derivation of (4.39)-(4.41) and (4.49)-(4.51) are acceptable for a first-order and lead to a relatively accurate derivation of the optimum inductance value (L_2) for which the Colpitts oscillator circuit topology of Fig. 4.2 (a) exhibits a minimum phase noise.

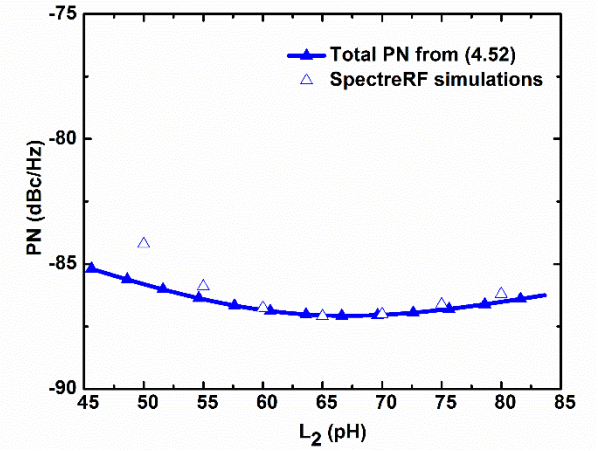
From SpectreRF simulations, for an oscillation frequency of 10 GHz, a minimum phase noise is achieved for L_2 equal to about 3 nH. This value of inductance can be obtained by means of integrated inductors. Note that these results are achieved by considering a typical quality factor of 10 as reported in Section 4.1.

The existence of an optimum value for L_2 for minimum noise from M_2 reaching the output can be explained as follows. Assuming the tail transistor M_2 generates a flicker and thermal noise current with power equal to $\overline{I_n^2}$, then the power of the noise current at the drain of M_2, $\overline{I_{n,out}^2}$, is

equal to $\overline{I_n^2}/\left(Z_S g_{m2}+1\right)^2$, where Z_S is the impedance of the parallel combination of L_2 with the capacitance present at the source node of M_2, which is C_{p2} shown in Fig. 4.2 (b).



(a)



(b)

Fig. 4.5. Total PN at a 1 MHz frequency offset from the carrier vs. the degeneration inductance L_2 at an average bias current of 6.3 mA, for the circuit of Fig. 4.2 (a), predicted by (4.52) and obtained by SpectreRF simulations for the oscillation frequencies of (a) 10 GHz; (b) 100 GHz.

$\overline{I_{n,out}^2}$ is plotted vs. frequency in Fig. 4.6. R_{p2} is the parallel resistance representing the losses of L_2. It can be observed that $\overline{I_{n,out}^2}$ shows a minimum at the resonance frequency of the bandpass filter formed by L_2 and C_{p2}. At that frequency, Z_S takes its maximum value, which means that the impedance looking down from the drain of M_2, Z_{out}, which is equal to $\left[1+\left(g_{m2}+g_{mb2}\right)r_{o2}\right]Z_S+r_{o2}$ will also be maximized. According to [46, 71], for single-ended Colpitts the impedance (magnitude) seen at the source of M_1 should be maximum at the oscillation frequency of the

oscillator topology. Thereby, here for Z_{out} to be maximum at the oscillation frequency, the resonance frequency f_{filter} of the bandpass filter at the source of M_2 should be equal to the oscillation frequency.

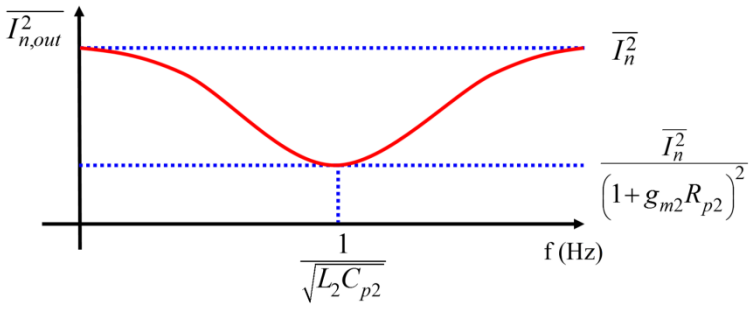


Fig. 4.6. Power of the noise current at the drain of M_2 in Fig 4.2 (a) vs. frequency.

In regard of the upconversion of the flicker noise from M_1 and M_2, it is reduced as follows. The inductive degeneration acts in a similar way to the noise filter, since at f_{filter}, the nonlinear capacitance present at the source node of M_2 is cancelled by L_2. Thereby, the modulation of the current flowing through the nonlinear junction capacitance present at the source node of M_2 and then through M_1 to the output, is minimized.

At this stage, it is worth also comparing these results obtained from the Colpitts topology with the inductive degeneration with those obtained for the traditional Colpitts oscillator circuit topology of Fig. 4.1, previously reported in Chapter 1 and therein [OP1, OP6]. In particular, from Chapter 1 and therein [OP1, OP6] the phase noise obtained under the same design conditions amounts to -96.25 dBc/Hz and -77.06 dBc/Hz for the oscillation frequencies of 10 GHz and 100 GHz respectively. Comparing these phase noise performances with the results obtained here and reported in Figs. 4.5 (a)-(b), we can observe that the Colpitts topology with inductive degeneration can lead potentially to a phase noise reduction up to 16 dB and 11 dB at the oscillation frequencies of 10 GHz and 100 GHz respectively.

The $1/f^3$ region of the phase noise extends above 1 MHz as observed in Chapter 1 and therein [OP1, OP6]. This is a consequence of the adoption of nano-scale CMOS technologies characterized by flicker noise corners of several tens or hundreds of MHz, which lead to flicker noise up-conversion being responsible for most of phase noise [44] even at large offsets from the carrier frequency. Thereby, the optimum inductance value for the total phase noise shown in Figs. 4.5 (a)-(b) is very close to that given by (4.39)-(4.41), since at a 1 MHz offset, thermal noise has a negligible effect on phase noise.

4.3 Noise Filter

In this section we will derive the analytical expression for the oscillation frequency (f_0) of a Colpitts oscillator circuit topology in which we introduced a band-stop filter (L_3, C_3) to the source node of M_1 as shown in Fig. 4.7 (a). Due to its noise filtering action, it is referred therein

[46, 71, 72] as noise filter. Moreover, we will observe that there is an optimum inductance value (L_3) for which the oscillator circuit topology exhibits a minimum phase noise and will calculate such an optimum inductance which leads the noise filter to resonate at the oscillation frequency, as aforementioned.

In order to extract appropriate evaluations about the improvement of phase noise performance with respect to the traditional topology of Fig. 4.1, the oscillator circuit design will be carried out under the same transistor size, power and current consumption, inductance of the tank and its quality factor, as in Chapters 1, 2 and therein [OP1, OP2, OP6-OP8].

4.3.1 Oscillation Frequency

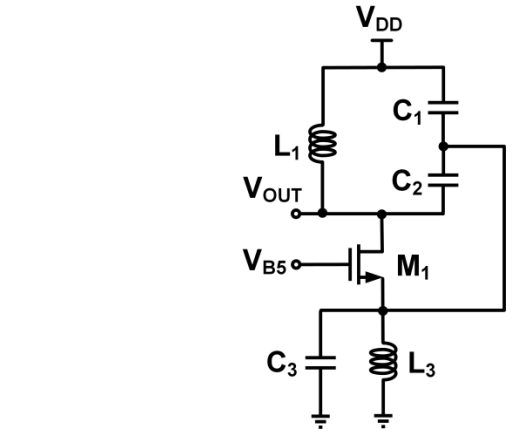
The Colpitts oscillator circuit topology incorporating a noise filter is shown in Fig. 4.7 (a). Its small-signal equivalent circuit is shown in Fig. 4.7 (b). This equivalent circuit is obtained by considering the simplified transistor model with the small-signal transconductance (g_m), gate-to-source capacitance (C_{gs}), gate-to-drain capacitance (C_{gd}), source-to-bulk capacitance (C_{sb}) and drain-to-bulk capacitance (C_{db}). In the interest of a low complexity of the derived equations, the small-signal output resistance r_{o1} as well as the polysilicon gate resistance r_g of M_1 are neglected. Later, we will verify that this hypothesis is acceptable. R_p represents the total load resistance of the LC tank, including the effect of the finite Q of the tank and the resistance seen from the source of M_1 scaled by the capacitive divide factor.

The junction capacitances of transistors M_1 and M_2 in Fig. 4.1 behave nonlinearly during the oscillation period. One of the major upconversion mechanisms of flicker noise is the modulation of the current flowing through the capacitance at the source node of M_1 [44]. By removing M_2, the modulation of the current flowing through this capacitance is significantly reduced, due to the decrease of the nonlinear parasitic capacitance.

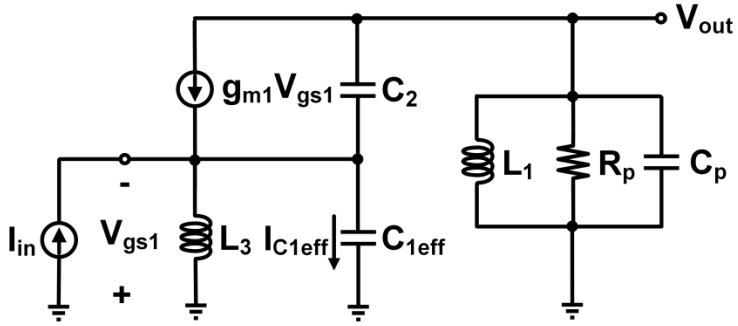
The presence of an optimum L_3 for minimum phase noise is due to L_3 resonating with the capacitance present at the source node of M_1, thereby acting as an ideal high impedance node at the resonance frequency of the noise filter. This results in further decrease of the modulation current, since this capacitance is effectively tuned out by L_3.

C_3 can be varied in order to tune the oscillation frequency, so avoiding changes in the tank capacitance. Moreover, the amplitude of the tank voltage can be larger than in the topology of Fig. 4.1, since there is no tail transistor consuming voltage headroom.

It is worth noting that since no varactor was used in the circuit of Fig. 4.7 (a), there are only two major up-conversion mechanisms: the modulation of the current flowing through the capacitance present at the source node of M_1, and the modulation of the harmonic content of the output voltage waveform (i.e. Groszkowski effect). The adoption of the noise filter can minimize the first cause of flicker noise up-conversion [44].



(a)



(b)

Fig. 4.7. (a) Colpitts oscillator circuit topology incorporating a noise filter. V_{B5} is the dc bias voltage. (b) Small-signal equivalent circuit. I_{in} is the input current stimulus used for the calculation of the closed-loop gain V_{out}/I_{in}.

C_{gs1}, C_{sb1} and C_3 appear in parallel with C_1, and their sum can be expressed as an effective capacitance

$$C_{1eff} = C_1 + C_{gs1} + C_{sb1} + C_3 \tag{4.53}$$

C_p is the parasitic capacitance present at the drain node of M_1, given by

$$C_p = C_{db1} + C_{gd1} \tag{4.54}$$

In order to excite the circuit into oscillation we insert a current stimulus I_{in} at the source of M_1. From KCL at the source of M_1, we obtain

$$I_{C1eff} - I_{in} - \frac{V_{gs1}}{sL_3} + \frac{V_{out}}{sL_1} + \frac{V_{out}}{R_p} + V_{out}sC_p = 0 \tag{4.55}$$

and also

$$V_{gs1} = -I_{C1eff}\frac{1}{sC_{1eff}} \tag{4.56}$$

Solving (4.55) for I_{C1eff} and using the result in (4.56) we find

$$V_{gs1} = \frac{1}{1+\dfrac{1}{s^2 L_3 C_{1eff}}}\frac{1}{sC_{1eff}}\left(-I_{in} + \frac{V_{out}}{sL_1} + \frac{V_{out}}{R_p} + V_{out}sC_p\right) \tag{4.57}$$

and from KCL at the output

$$g_{m1}V_{gs1} + \left(V_{out} + V_{gs1}\right)sC_2 + \frac{V_{out}}{sL_1} + \frac{V_{out}}{R_p} + V_{out}sC_p = 0 \tag{4.58}$$

Expressing (4.58) as a function of V_{gs1} and equating to (4.57), we can derive the closed-loop transfer function V_{out}/I_{in} as a ratio. By equating the real part of the denominator of this ratio to zero, we find that the oscillation frequency is given by

$$f_o = \frac{1}{2\pi}\omega_0 \tag{4.59}$$

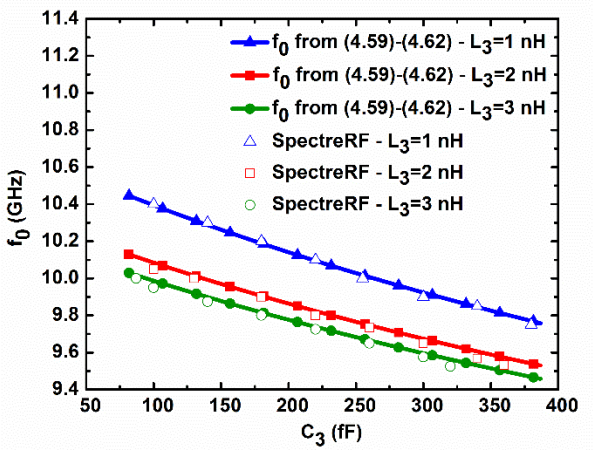
$$\omega_o = \sqrt{\frac{N_5}{D_5}} \tag{4.60}$$

where

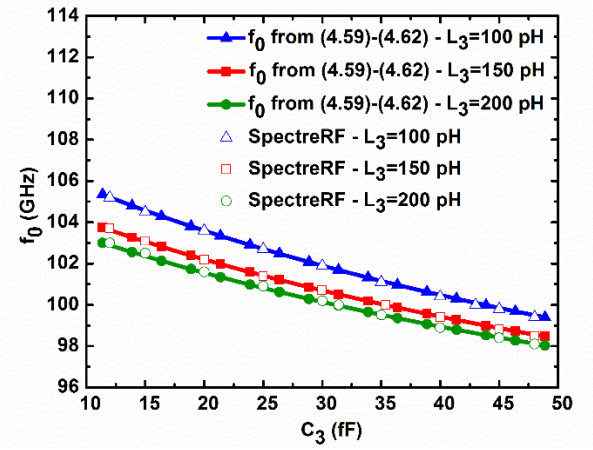
$$N_5 = C_{1eff}L_3R_p + C_2L_3R_p + C_2L_1R_p + C_pL_1R_p + L_1L_3g_{m1} + \left(C_{1eff}^2L_3^2R_p^2 + 2C_{1eff}C_2L_3^2R_p^2 - 2C_{1eff}C_2L_1L_3R_p^2 - 2C_{1eff}C_pL_1L_3R_p^2 + 2C_{1eff}L_1L_3^2R_pg_{m1} + C_2^2L_3^2R_p^2 + 2C_2^2L_1L_3R_p^2 + C_2^2L_1^2R_p^2 - 2C_2C_pL_1L_3R_p^2 + 2C_2C_pL_1^2R_p^2 + 2C_2L_1L_3^2R_pg_{m1} + 2C_2L_1^2L_3R_pg_{m1} + C_p^2L_1^2R_p^2 + 2C_pL_1^2L_3R_pg_{m1} + L_1^2L_3^2g_{m1}^2\right)^{1/2} \approx C_{1eff}L_3R_p + C_2L_3R_p + C_2L_1R_p + C_pL_1R_p + \left(C_{1eff}^2L_3^2R_p^2 + 2C_{1eff}C_2L_3^2R_p^2 - 2C_{1eff}C_2L_1L_3R_p^2 + C_2^2L_3^2R_p^2 + 2C_2^2L_1L_3R_p^2 + C_2^2L_1^2R_p^2\right)^{1/2} \tag{4.61}$$

$$D_5 = 2L_1L_3R_p\left(C_{1eff}C_2 + C_{1eff}C_p + C_2C_p\right) \approx 2L_1L_3R_pC_{1eff}C_2 \tag{4.62}$$

Figs. 4.8 (a)-(b) show the theoretical estimation of the oscillation frequency provided by (4.59)-(4.62), as a function of C_3. Simulations are repeated for three different values of L_3 in order to show the dependence of f_0 on L_3, which turns out being significant. Note that the oscillation frequency predicted by (4.59)-(4.62) closely follows the results obtained by simulations.



(a)



(b)

Fig. 4.8. Oscillation frequency vs. C_3 for the circuit of Fig. 4.7 (a) as predicted by (4.59)-(4.62) and SpectreRF simulations for oscillation frequencies in the vicinity of (a) 10 GHz; (b) 100 GHz.

Thereby, the aforementioned simplifications in the derivation of (4.59)-(4.62) are justified and lead to an accurate first-order prediction of the oscillation frequency f_0.

4.3.2 Optimum Inductance for Minimum Phase Noise

Here, our objective is to derive the value of L_3 for which the phase noise at the output of the Colpitts oscillator circuit topology of Fig. 4.7 (a) reaches a minimum. The theoretical results will be compared with those obtained by means of SpectreRF simulations.

The large-signal equivalent circuit of the Colpitts oscillator of Fig. 4.7 (a) is shown in Fig. 4.9. V_{in} is a voltage stimulus applied to the gate of M_1. Transistor M_1 is represented as a transconductance amplifier according to the describing function analysis [65]. G_{m1} is the large-signal transconductance of M_1, equal to the ratio of the fundamental harmonic of the drain current of M_1 to the fundamental harmonic of the gate-source voltage of M_1.

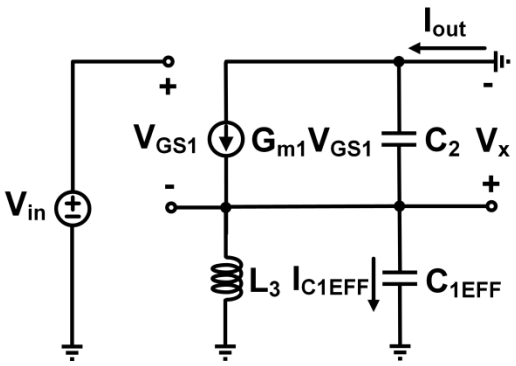


Fig. 4.9. Large-signal equivalent circuit of the Colpitts oscillator circuit topology of Fig. 4.7 (a). G_{m1} is the large-signal transconductance of M_1. V_{in} is a voltage stimulus applied to the gate of M_1.

G_{m1} does not take into account the degeneration effect due to the non-ideal bias provided by L_3. For this reason, first, we calculate the equivalent transconductance for the describing function model of Fig. 4.9 with respect to the voltage stimulus V_{in}, i.e. $G_{m,eq2}=I_{out}/V_{in}$. Next, we will calculate the value of L_3 for which the flicker and thermal phase noise components at the output of the Colpitts oscillator circuit topology of Fig. 4.7 (a) reach the minimum values.

We can write

$$C_{1EFF} = C_1 + C_3 \tag{4.63}$$

$$Z_p = sL_3 // \frac{1}{sC_{1EFF}} = \frac{sL_3}{s^2 L_3 C_{1EFF} + 1} \tag{4.64}$$

$$V_{in} = V_{GS1} + I_{out} Z_p \tag{4.65}$$

Using (4.64) into (4.65) and rewriting

$$V_{GS1} = V_{in} - I_{out} \frac{sL_3}{s^2 L_3 C_{1EFF} + 1} \tag{4.66}$$

moreover,

$$V_x = I_{out} Z_p = I_{out} \frac{sL_3}{s^2 L_3 C_{1EFF} + 1} \tag{4.67}$$

From KCL at the drain of M_1, it derives

$$G_{m1} V_{GS1} - I_{out} - V_x s C_2 = 0 \tag{4.68}$$

Finally, replacing V_{GS1} and V_x into (4.68) with their values given by (4.66) and (4.67), respectively, we find $G_{m,eq2}$ as follows

$$G_{m,eq2} = \frac{G_{m1}}{1 + G_{m1}\dfrac{sL_3}{s^2 L_3 C_{1EFF} + 1} + \dfrac{s^2 L_3 C_2}{s^2 L_3 C_{1EFF} + 1}} \tag{4.69}$$

By replacing G_{m1} in (4.28) with $G_{m,eq2}$ given by (4.69), taking the derivative with respect to L_3 and equating to zero, we find that the value of L_3 for which the flicker phase noise component at the output of the Colpitts oscillator circuit topology of Fig. 4.7 (a) reaches the minimum is given by

$$L_3 = \left| \frac{R_p G_{m1} n^2 + 1}{\left(C_{1EFF} R_p G_{m1} n^2 + C_{1EFF} + C_2\right) s^2 + G_{m1} s} \right| \tag{4.70}$$

A similar derivation can also be performed for the phase noise component due to the thermal noise of M_1, L_3 and the LC tank.

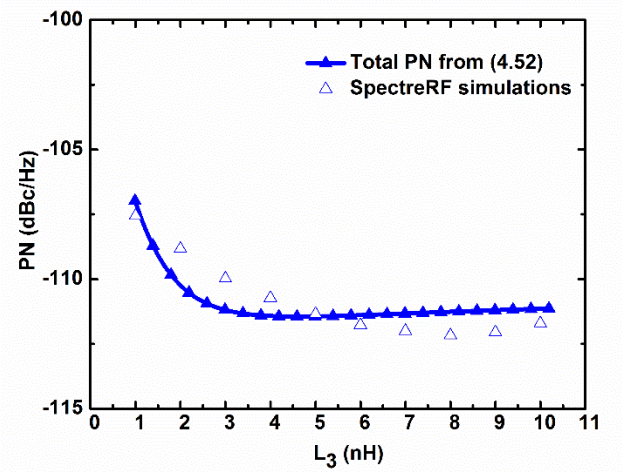
The phase noise expression due to the thermal noise is

$$\mathcal{L}(\Delta\omega)\Big|_{thermal} = \left| \frac{K_B T}{4 N I_B^2 R_p^3 C_{tank}^2 \Delta\omega^2} \left(1 - \frac{\Phi^2}{14}\right)^{-2} \times \left(\frac{\gamma}{n(1-n)} + \frac{1}{(1-n)^2} + \frac{n^2 R_p}{(1-n)^2} \frac{1}{Q\omega L_3} \right) \right| \tag{4.71}$$

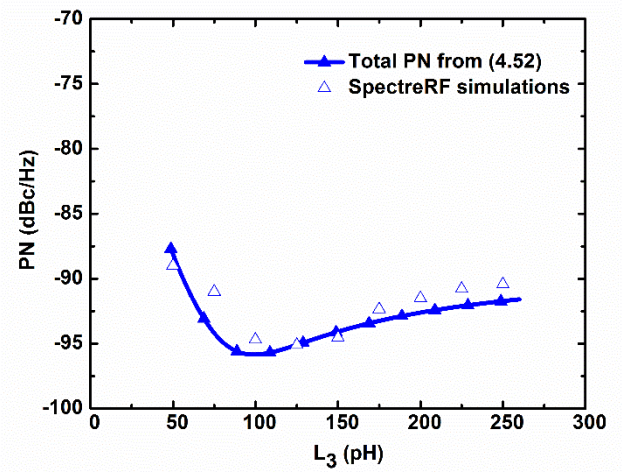
We then substitute G_{m1} in (4.48) with the expression of $G_{m,eq2}$ given by (4.69) and then use the calculated value of I_B in (4.71). After taking the derivative of the result with respect to L_3 and equate to zero, we find that the value of L_3 for which the thermal phase noise component at the output of the Colpitts oscillator circuit topology of Fig. 4.7 (a) reaches the minimum is

$$L_3 = \left| \frac{1}{\left(C_{1EFF} + C_2\right) s^2 + G_{m1} s} \right| \tag{4.72}$$

The total phase noise is plotted in Figs. 4.10 (a)-(b) versus L_3, for an average current of 6.3 mA, for an oscillation frequency of 10 GHz, at a 1 MHz frequency offset. Note the relatively good agreement between the theoretical derivations and the SpectreRF simulations.



(a)



(b)

Fig. 4.10. Total PN at a 1 MHz frequency offset from the carrier vs. L_3, for the circuit of Fig. 4.7 (a) with an average bias current of 6.3 mA, as predicted by (4.52) and obtained by SpectreRF simulations for the oscillation frequencies of (a) 10 GHz; (b) 100 GHz.

From SpectreRF simulations, the minimum phase noise is achieved for L_3 approximately equal to 8 nH. Thereby, this result confirms the discussion in [46], according to which the optimum inductance value in terms of phase noise is expected to be the value which tunes the resonance frequency of the noise filter (L_3, C_3) to the oscillation frequency. This value of inductance can be obtained by means of integrated inductors. Note that this result is achieved by considering a typical quality factor of 10 as reported in Section 4.1.

At this stage, it is worth also comparing these results obtained from the Colpitts topology with noise filter of Fig. 4.7 (a) with those obtained for the traditional Colpitts oscillator circuit topology of Fig. 4.1, previously reported in Chapter 1 and therein [OP1, OP6]. In particular, from Chapter 1 and [OP1, OP6] the phase noise obtained under the same design conditions

amounts to -96.25 dBc/Hz and -77.06 dBc/Hz for the oscillation frequencies of 10 GHz and 100 GHz respectively. Comparing these phase noise performances with the results obtained here and reported in Figs. 4.10 (a)-(b), we can observe that the Colpitts oscillator circuit topology with noise filter can potentially allow a phase noise reduction up to 16 dB and 17 dB for the oscillation frequencies of 10 GHz and 100 GHz respectively.

Last, coherently with that fact that the $1/f^3$ region of the phase noise extends above 1 MHz, as observed in Chapter 1 and therein [OP1, OP6], we can also observe that the optimum inductance value for the total phase noise shown in Figs. 4.10 (a)-(b) is very close to that given by (4.71), since at a 1 MHz offset, thermal noise has a negligible effect.

4.4 Optimum Current Density

In this section, we will examine the technique of biasing an oscillator topology with the optimum current density for the minimum phase noise. The efficiency of this technique for oscillators was shown in [76-78] where the transistors were biased at or close to the current density for minimum noise figure.

It is worth observing that from the phase noise analysis point of view, an oscillator can be treated as a low noise amplifier, needed to be noise matched to the signal source impedance, represented in this case by the tank impedance at resonance [74]. In low noise amplifiers the transistors should be biased at the current density minimizing their noise figure. On the other hand, in oscillators the bias point changes during the oscillation period and the optimum current density for minimum phase noise may significantly deviate from the current density for minimum noise figure for the transistors.

We will analyze and apply this third technique for further reduction of phase noise to the Colpitts oscillator incorporating either inductive degeneration or noise filter investigated above. Combining the benefits of this third technique with those of inductive degeneration or of the noise filter, could lead to maximize the potential reduction of phase noise achievable for the oscillator circuit topology under common design conditions.

First, in our analysis the phase noise components due to flicker and thermal noise will be expressed as a function of the bias current. Next, the resulting equations will be plotted versus the bias current density and validated by means of the results provided by SpectreRF simulations in Cadence.

4.4.1 Inductive Degeneration

Combining (4.17), (4.42) and (4.43) we yield

$$G_{m1} = -\frac{2I_B\left(1-\frac{\Phi^2}{14}\right)}{nV_{tank}} \tag{4.73}$$

With reference to the Colpitts oscillator circuit topology with the inductive degeneration (L_2) at the source node of the tail current transistor (M_2) shown in Fig. 4.2 (a), we use G_{m1} given by (4.73) into (4.36)-(4.38) in order to express $G_{m,eq1}$ in terms of I_B. Then, for the flicker component of the phase noise, we use (4.28) where G_{m1} is substituted by the value of $G_{m,eq1}$ calculated above. After taking the derivative of the resulting equation with respect to I_B and equating to zero, we find

$$I_B = \left|\frac{N_6}{D_6}\right| \tag{4.74}$$

where

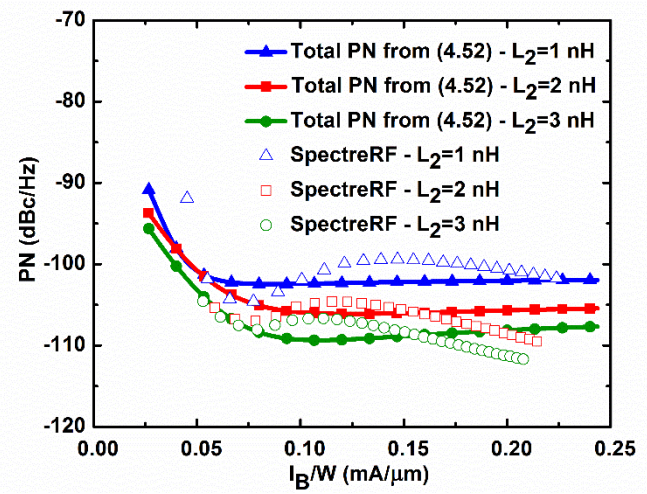
$$N_6 = 7V_{tank}n\left[\left(C_{1EQ}L_2 + C_2L_2 + C_{1EQ}L_2G_{m2}R_{DS2} + C_2L_2G_{m2}R_{DS2}\right)s^2 + \left(C_{1EQ}R_{DS2} + C_2R_{DS2}\right)s + 1\right] \tag{4.75}$$

$$\begin{aligned} D_6 = {} & \left(14C_{1EQ}L_2R_pn^2 - C_{1EQ}\Phi^2L_2R_pn^2 + 14C_{1EQ}L_2R_pG_{m2}n^2R_{DS2} - C_{1EQ}\Phi^2L_2R_pG_{m2}n^2R_{DS2}\right)s^2 + \\ & \left(14L_2 - \Phi^2L_2 + 14L_2G_{m2}R_{DS2} - \Phi^2L_2G_{m2}R_{DS2} + 14C_{1EQ}R_pn^2R_{DS2} - C_{1EQ}\Phi^2R_pn^2R_{DS2}\right)s - \\ & R_p\Phi^2n^2 - R_{DS2}\Phi^2 + 14R_pn^2 + 14R_{DS2} \end{aligned} \tag{4.76}$$

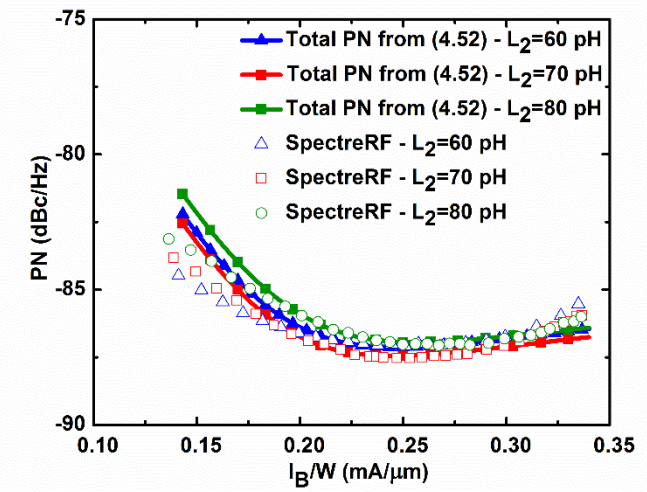
The thermal noise contribution to phase noise does not exhibit a minimum. By examining (4.45), it can be observed that the phase noise due to the thermal noise decreases for higher values of I_B.

The total phase noise is given by (4.52) where the flicker and thermal phase noise components have been replaced by the new derivations. The total phase noise is plotted in Figs. 11 (a)-(b) versus the bias current density I_B/W and validated by means of the results provided by SpectreRF simulations in Cadence, for a 1 MHz frequency offset from the carrier. In order to demonstrate the dependence of phase noise on L_2, the total phase noise is plotted for three different values of L_2. V_{B3} in Fig. 4.2 (a) is connected to V_{DD} which is equal to 1 V, whereas V_{B4} has been swept from the value required to start up the oscillations to V_{DD}.

At 10 GHz, both theory and simulations predict a current density of about 0.075 mA/μm for which phase noise reaches a minimum. This value is independent from L_2 according to SpectreRF simulation results. However, from simulations it appears that beyond the local minimum and a certain bias current density, further increases may offer a further slight reduction in phase noise for inductances of 2 and 3 nH. Thereby, in this case it may be worth investing additional bias current in order to achieve improved phase noise performance.



(a)



(b)

Fig. 4.11. Total PN at a 1 MHz frequency offset from the carrier vs. the bias current density I_B/W for the circuit of Fig. 4.2 (a), predicted by (4.52) and obtained by SpectreRF simulations for the oscillation frequencies of (a) 10 GHz; (b) 100 GHz.

From Fig. 4.11 (a) we can calculate the difference in phase noise between the values obtained for the bias current of 6.3 mA considered in Section 4.2, corresponding to a bias current density of 0.21 mA/μm, and the optimum bias current density of 0.075 mA/μm. SpectreRF simulation results for 10 GHz show a reduction of phase noise of about 3 dB for L_2 equal to 1 nH and optimum bias current density of 0.075 mA/μm.

By summing up the phase noise reduction provided for 10 GHz by the inductive degeneration of 3 nH and optimum bias current density of 0.075 mA/μm, a potential overall reduction up to 14 dB can be achieved. Despite the current density of 0.075 mA/μm may lead to

a better figure of merit, as mentioned above, it could be worth increasing the current consumption to 0.23 mA/μm in order to reach an overall potential reduction up to 16 dB.

Regarding the operation at 100 GHz, from Fig. 4.11 (b), the potential overall reduction provided by combining the inductive degeneration of 70 pH and optimum bias current density of 0.23 mA/μm amounts to 11 dB. Note that this improvement is limited by the proximity of the current density used in Chapters 1, 2 and therein [OP1, OP2, OP6-OP8] to the optimum current density identified here, and thereby, in principle, it could be potentially even larger in case the current density was significantly far away from the optimum value.

4.4.2 Noise Filter

With reference to the Colpitts oscillator circuit topology of Fig. 4.7 (a), where a noise filter (L_3, C_3) has been introduced to the source node of M_1, for the phase noise component contributed by flicker noise, we use G_{m1} given by (4.73) into (4.69) in order to express $G_{m,eq2}$ in terms of I_B.

The value of G_{m1} in (4.28) is then substituted by the value of $G_{m,eq2}$ calculated before. After taking the derivative of the resulting equation with respect to the bias current I_B and equate to zero, we obtain the following expression

$$I_B = \left| \frac{N_7}{D_7} \right| \tag{4.77}$$

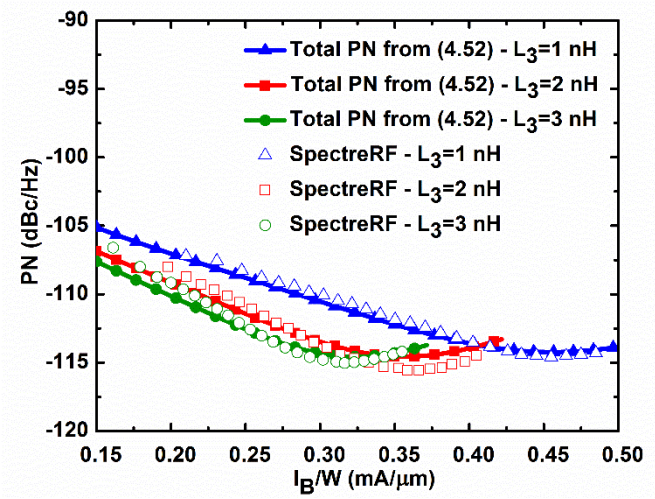
where

$$N_7 = 7V_{tank}\left[L_3 n \left(C_{1EFF} + C_2 \right) s^2 + n \right] \tag{4.78}$$

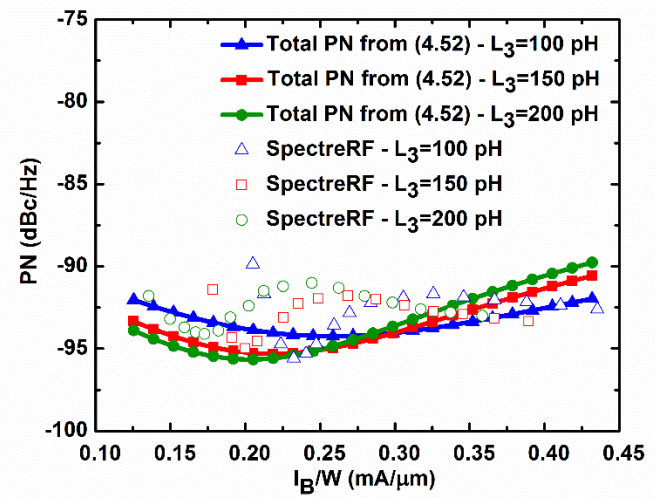
$$D_7 = \left(-C_{1EFF} L_3 R_p \Phi^2 n^2 + 14 C_{1EFF} L_3 R_p n^2 \right) s^2 + \left(-L_3 \Phi^2 + 14 L_3 \right) s - R_p \Phi^2 n^2 + 14 R_p n^2 \tag{4.79}$$

Again the thermal noise contribution to phase noise does not exhibit a minimum. By examining (4.71), it can be observed that the phase noise due to the thermal noise decreases as I_B increases.

The total phase noise is given by (4.52) where the flicker and thermal phase noise components have been replaced by the new derivations. It is plotted in Figs. 4.12 (a)-(b) vs. the bias current density I_B/W and validated by means of the results provided by SpectreRF simulations in Cadence, at a 1 MHz frequency offset from the carrier. In order to demonstrate the dependence of phase noise on L_3, the total phase noise is plotted for three values of L_3. V_{B5} has been swept from the value required to start up the oscillation to V_{DD}.



(a)



(b)

Fig. 4.12. Total PN at a 1 MHz frequency offset from the carrier vs. the bias current density I_B/W for the circuit of Fig. 4.7 (a), predicted by (4.52) and obtained by SpectreRF simulations for the oscillation frequencies of (a) 10 GHz; (b) 100 GHz.

Fig. 4.12 (a) shows that for L_3=2 nH both theory and simulations predict a bias current density of around 0.375 for which phase noise is minimized. Moreover, we can calculate the difference of phase noise between the results obtained for the bias current of 6.3 mA adopted in Section 4.3, corresponding to a current density of 0.21 mA/μm, and the optimum current density. From SpectreRF simulations, for instance, a phase noise reduction of about 6 dB can be achieved for L_3 of 2 nH and a current density of 0.36 mA/μm.

Overall, by summing up the phase noise reduction provided by the Colpitts topology with the noise filter for 3 nH and optimum bias current density of about 0.31 mA/μm, a potential overall reduction up to 19 dB can be achieved with respect to the traditional Colpitts topology.

Note that due to the very close phase noise performance, the case of 3 nH and 0.31 mA/μm lead to a lower current consumption and, thereby, potentially to a better figure of merit of the oscillator with respect to the case of 2 nH with a current density of 0.36 mA/μm.

Regarding operation at 100 GHz, Fig. 4.12 (b) shows that, overall, the potential reduction provided by L_3 of 200 pH and optimum bias current density of 0.17 mA/μm amounts to about 17 dB. Note that this improvement is limited by the proximity of the current density used in Chapters 1, 2 and therein [OP1, OP2, OP6-OP8] to the optimum current density identified here, and thereby, in principle, it could be potentially even larger in case the current density was significantly far away from the optimum value.

4.5 Conclusions

The techniques of inductive degeneration and noise filter for the reduction of phase noise due to the tail transistor in CMOS LC oscillators have been applied for the first time to a single-ended Colpitts oscillator circuit topology. These techniques have been analysed in detail by means of circuit theory and simulations.

The analyses allow us to gain insight in a few interesting aspects not addressed yet in the literature. In particular, an analytical expression of the oscillation frequency has been derived in order to allow an accurate prediction and show the dependence on the degeneration inductance and the noise filter components. In addition, an analytical expression of the phase noise has been derived in order to allow a good prediction and identify design opportunity for phase noise reduction in the above techniques. The theoretical results, supported by circuit simulations, show that it is possible to integrate a degeneration or noise filter inductance for the oscillation frequencies of 10 GHz and 100 GHz. Also, that there is an optimum degeneration inductance which resonates at the oscillation frequency with the parasitic capacitance present at the source of the tail current transistor. In addition, that for a given typical capacitance there is an optimum inductance for which the noise filter resonates at the oscillation frequency. Furthermore, that the phase noise of the Colpitts oscillator topology modified with the introduction of either the inductive degeneration or the noise filter reaches a minimum, leading to considerable potential benefits.

Moreover, a third technique, namely optimum current density, for the phase noise reduction has been applied to the Colpitts topology with either the inductive degeneration or noise filter and analyzed in detail by means of circuit theory and simulations. It consists of biasing the oscillator circuit with the optimum current density for the minimum phase noise. The proposed analyses allow us for the first time to gain insight in the theoretical details of this technique and its applications, identifying additional opportunities for the reduction of phase noise in the examined circuit topologies.

The results of the analyses presented above show that, under the adopted common design conditions in a 28 nm CMOS technology, the above techniques may potentially lead to phase

noise reduction up to about 19 dB and 17 dB at a 1 MHz offset from the oscillation frequencies of 10 GHz and 100 GHz respectively, with respect to the traditional Colpitts topology.

Chapter 5

Phase Noise Reduction Techniques in the Hartley Topology

5.1 Introduction

In this Chapter, the techniques for phase noise reduction reported in Chapter 4 and therein [OP3, OP9-OP12] will be applied to the traditional single-ended Hartley oscillator circuit topology reported in Fig. 5.1 with the objective of providing adequate theoretical proofs of the potential benefits. Our analyses will allow, for the first time, to gain insight into some theoretical details. Exploring these techniques for phase noise reduction to a Hartley oscillator topology operating at 10 and 100 GHz, could provide useful insight regarding their effectiveness over a wide frequency range. Moreover, it could also provide a useful comparison in terms of phase noise performance with respect to the most widespread topologies. Indeed, in Chapter 1 and therein [OP1, OP6] we analyzed Colpitts, Hartley and cross-coupled differential pair topologies across two decades, from 1 to 100 GHz, and we showed that the opportunity of identifying the topology exhibiting the lowest phase noise depends also on the operating frequency range. In addition, we showed that under the adopted common conditions, Hartley topology exhibits superior phase noise performance at high frequencies with respect to the other topologies examined in Chapter 1 and therein [OP1, OP6]. Furthermore, such an investigation could be helpful in understanding the application boundaries of these techniques and gaining useful insights about the potential opportunities and benefits in the mm-wave frequency range, expected to play a pivoting role for research and developments of next-generation (i.e. 5^{th} generation and beyond) communication systems [2, 30].

The key contents of this chapter have been reported in original contributions published in conference proceedings [OP10, OP12].

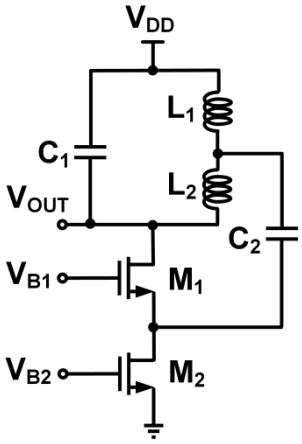


Fig. 5.1. Single-ended Hartley oscillator circuit topology. V_{B1} and V_{B2} are dc bias voltages.

5.2 Inductive Degeneration

In this section we will derive an analytical expression for the oscillation frequency (f_0) of the Hartley oscillator circuit topology in which we introduced an inductive degeneration (L_3) to the source node of the tail current transistor (M_2), as shown in Fig.5.2 (a).

In order to extract appropriate evaluations about the improvement of performance with respect to the traditional topology of Fig. 5.1, the oscillator circuit design will be carried out under the same transistor size, power and current consumptions, inductance of the tanks and their quality factors, as in Chapters 1, 2 and therein [OP1, OP2, OP6-OP8]. Specifically, the transistor width is 30 μm, whereas the power consumed is 6.3 mW. V_{DD} is equal to 1 V. The tank inductance is equal to 500 pH and 50 pH for operation at 10 GHz and 100 GHz respectively.

5.2.1 Oscillation Frequency

The Hartley oscillator circuit topology with an inductively degenerated tail current transistor (M_2) is shown in Fig. 5.2 (a). Its small-signal equivalent circuit is shown in Fig. 5.2 (b). This equivalent circuit is obtained by considering the simplified transistor model with the small-signal transconductance (g_m), gate-to-source capacitance (C_{gs}), gate-to-drain capacitance (C_{gd}), source-to-bulk capacitance (C_{sb}), drain-to-bulk capacitance (C_{db}) and output resistance (r_{o2}). For simplicity of the derived equations, the small-signal output resistance r_{o1} of M_1 as well as the polysilicon gate resistance r_g of M_1 and M_2, are neglected. Later, we will see that this working hypothesis is acceptable. If the small-signal output resistance r_{o2} of M_2 is also neglected, it can be proved that the oscillation frequency f_0 does not depend on L_3. Thereby, in order to take into account the effect of L_3 in f_0, r_{o2} is considered in the equivalent circuit. R_p represents the total load resistance of the LC tank, including the effect of the finite Q and the resistance seen from the source of M_1 scaled by the inductive divide factor. C_p is the parasitic capacitance at the source node of M_1, equal to the sum of C_{gs1}, C_{sb1}, C_{gd2} and C_{db2}. C_{p2} is the parasitic capacitance at the source node of M_2, equal to the sum of C_{gs2} and C_{sb2}. C_1 appears in parallel with C_{gd1}, and C_{db1}. Their sum can be represented as an equivalent capacitance C_{1eq}.

In order to excite the circuit into oscillation we insert a current stimulus I_{in} at the source of M_1. We can now write that

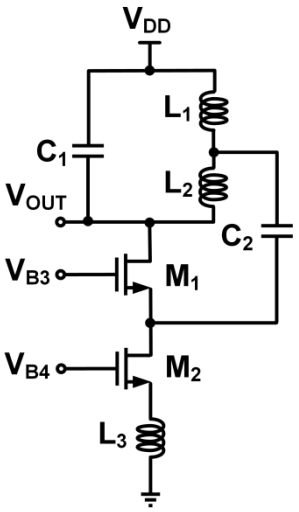
$$C_p = C_{gs1} + C_{sb1} + C_{gd2} + C_{db2} \tag{5.1}$$

$$C_{p2} = C_{gs2} + C_{sb2} \tag{5.2}$$

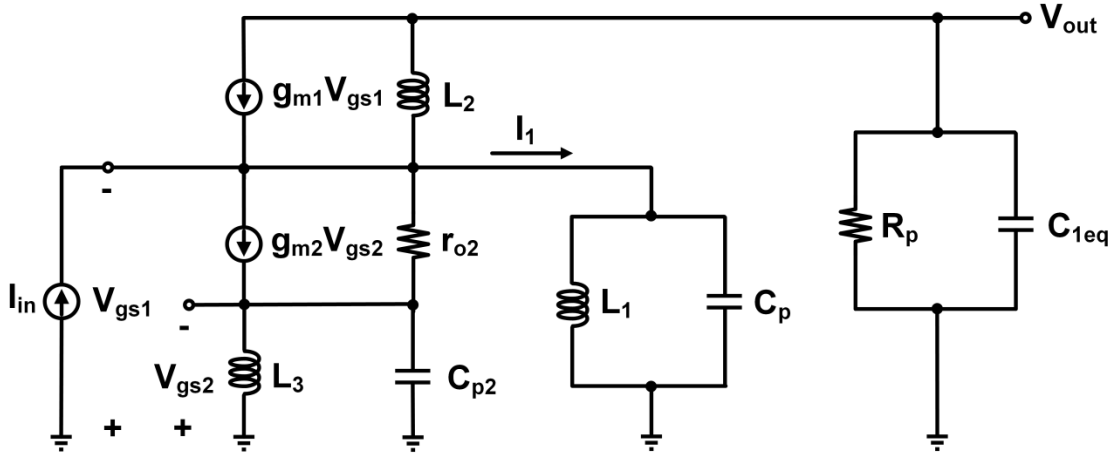
$$C_{1eq} = C_1 + C_{gd1} + C_{db1} \tag{5.3}$$

From Kirchhoff Current Law (KCL) at the source of M_2

$$g_{m2}V_{gs2}+\frac{-V_{gs1}+V_{gs2}}{r_{o2}}+\frac{V_{gs2}}{sL_3}+V_{gs2}sC_{p2}=0 \tag{5.4}$$



(a)



(b)

Fig. 5.2. (a) Hartley oscillator circuit topology incorporating an inductive degeneration (L_3) to the source node of the tail current transistor (M_2). V_{B3} and V_{B4} are dc bias voltages. (b) Small-signal equivalent circuit. I_{in} is the input current stimulus used for the calculation of the closed-loop gain V_{out}/I_{in}.

Thereby

$$V_{gs2}=\frac{1}{g_{m2}+\frac{1}{r_{o2}}+\frac{1}{sL_3}+sC_{p2}}\frac{1}{r_{o2}}V_{gs1} \tag{5.5}$$

From KCL at the source of M_1 and the output node

$$g_{m2}V_{gs2} - I_{in} + \frac{-V_{gs1} + V_{gs2}}{r_{o2}} + I_1 + \frac{V_{out}}{R_p} + V_{out}sC_{1eq} = 0 \tag{5.6}$$

Combining (5.5) and (5.6)

$$I_1 = I_{in} - \left[\frac{1}{g_{m2} + \frac{1}{r_{o2}} + \frac{1}{sL_3} + sC_{p2}} \frac{1}{r_{o2}} \left(g_{m2} + \frac{1}{r_{o2}} \right) - \frac{1}{r_{o2}} \right] \times V_{gs1} - \left(\frac{1}{R_p} + sC_{1eq} \right) V_{out} \tag{5.7}$$

Also, V_{gs1} is given by (5.8)

$$V_{gs1} = -I_1 \frac{sL_1}{s^2 L_1 C_p + 1} \tag{5.8}$$

Moreover, from KCL at the output

$$g_{m1}V_{gs1} + \frac{\left(V_{out} + V_{gs1}\right)}{sL_2} + \frac{V_{out}}{R_p} + V_{out}sC_{1eq} = 0 \tag{5.9}$$

which can be expressed as a function of V_{gs1}

$$V_{gs1} = -\frac{1}{g_{m1} + \frac{1}{sL_2}} \left(\frac{1}{sL_2} + \frac{1}{R_p} + sC_{1eq} \right) V_{out} \tag{5.10}$$

Using (5.7) in (5.8), expressing the result as a function of V_{gs1}, and equating to (5.10), we can express the closed-loop transfer function V_{out}/I_{in} as a ratio. By equating the imaginary part of the denominator of V_{out}/I_{in} to zero, we find that the oscillation frequency is given by (5.11)-(5.14). To reduce the complexity of the expression, C_p and C_{p2} are neglected in the equation for f_0 reported hereinafter.

$$f_o = \frac{1}{2\pi} \omega_0 \tag{5.11}$$

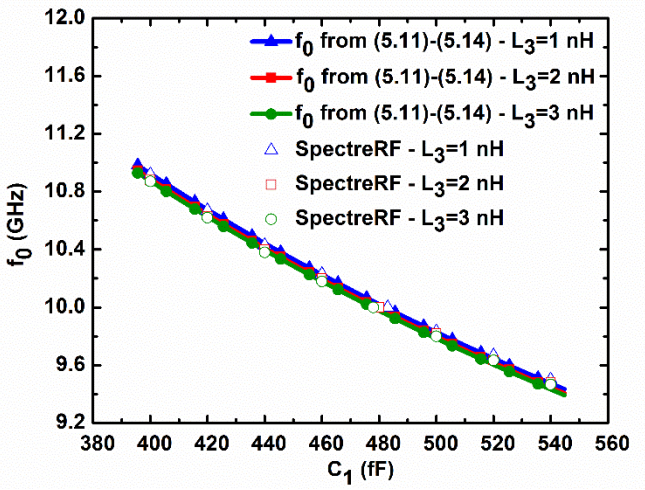
where

$$\omega_o \approx \sqrt{\frac{N_1}{D_1}} \tag{5.12}$$

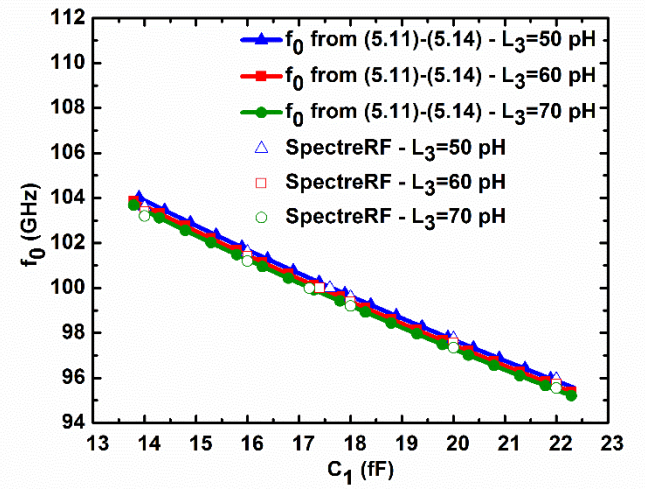
$$N_1 = L_1 r_{o2} + L_2 r_{o2} + L_1 R_p + L_3 R_p + L_3 R_p g_{m2} r_{o2} \tag{5.13}$$

$$D_1 = C_{1eq}L_1L_2R_p + C_{1eq}L_1L_3R_p + C_{1eq}L_2L_3R_p + L_1L_2L_3g_{m1} + C_{1eq}L_1L_2R_pg_{m1}r_{o2} + g_{m2}r_{o2}L_3\left(C_{1eq}L_1R_p + C_{1eq}L_2R_p + L_1L_2g_{m1}\right) \quad (5.14)$$

Figs. 5.3 (a)-(b) show the results obtained by theoretical expressions of the oscillation frequency provided by (5.11)-(5.14), as a function of the LC tank capacitance C_1.



(a)



(b)

Fig. 5.3. Oscillation frequency values vs. C_1 for the circuit of Fig. 5.2 (a), predicted by (5.11)-(5.14), and simulated in SpectreRF for oscillation frequencies in the vicinity of (a) 10 GHz; (b) 100 GHz.

The simulations are repeated for three values of L_3 in order to demonstrate the weak dependence of the oscillation frequency f_0 on L_3. This means that L_3 can be sized to satisfy other design requirements, with limited effects on the oscillation frequency. This result will be exploited in the next subsection. Moreover, note that the oscillation frequency predicted by

(5.11)-(5.14) closely follows the simulation results obtained by SpectreRF. Thereby, the aforementioned simplifications in the derivation of (5.11)-(5.14) are justified for an accurate first-order prediction of the oscillation frequency f_0.

5.2.2 Optimum Inductance for Minimum Phase Noise

Here, our aim is to explore the dependence of phase noise on L_3, and to derive under which condition the phase noise in the output spectrum of the Hartley oscillator circuit topology of Fig. 5.2 (a) could be minimized. The theoretical results will be compared with respect to the simulation results obtained by means of SpectreRF.

Adopting the analysis presented in [22] and following the derivations reported in Chapter 4 and therein [OP3, OP9-OP12] based on the same considerations, we can write

$$\mathcal{L}(\Delta\omega)\Big|_{flicker} = \left| \frac{\pi(1-n)^2 K}{4N} \frac{\omega_{1/f^3}}{\omega_{1/f}} \frac{n^2 G_{m1} R_p + 1}{V_{tank} R_p C_{1eq}^2 \Delta\omega^3 C_{ox} L^2} \right| \tag{5.15}$$

where L and G_{m1} are the length and the large-signal transconductance of M_1 respectively, n is the inductive divide factor equal to $L_1/(L_1+L_2)$, K is a process dependent parameter, C_{ox} is the gate oxide capacitance per unit area, N=1 for the single-ended Hartley, and $\Delta\omega$ is the angular frequency offset from the oscillation frequency. Moreover, ω_{1/f^3} is the frequency where the sideband power due to thermal noise is equal to the sideband power due to flicker noise, and $\omega_{1/f}$ is the corner frequency of the flicker noise generated by M_1.

In order to excite the Hartley oscillator circuit topology of Fig. 5.2 (a) a stimulus can be applied at different points. The type of stimulus (voltage or current) must be chosen such that when it is set to zero, the circuit returns to its original topology [68]. The large-signal equivalent circuit of the Hartley oscillator topology of Fig. 5.2 (a) is shown in Fig. 5.4.

V_{in} is a voltage stimulus applied to the gate of M_1. Transistor M_1 is represented as a transconductance amplifier according to the describing function analysis [65]. G_{m1} is the large-signal transconductance of M_1, equal to the ratio of the fundamental harmonic of the drain current of M_1 to the fundamental harmonic of the gate-source voltage of M_1. For transistor M_2 a simplified large-signal equivalent circuit is used [83, 84]. This equivalent circuit is obtained by considering the simplified transistor model with the large-signal transconductance (G_m), gate-to-source capacitance (C_{GS}), gate-to-drain capacitance (C_{GD}), source-to-bulk capacitance (C_{SB}), drain-to-bulk capacitance (C_{DB}) and output resistance (R_{DS}). G_{m2} is approximated by the average value of g_{m2} during the oscillation period. C_{P2} is the parasitic capacitance at the source node of M_2, equal to the sum of C_{GS2} and C_{SB2}. R_{DS2} is approximated by the average value of r_{o2} during the oscillation period. For simplicity of our analysis, it is assumed that, at the oscillation frequencies of 10 GHz and 100 GHz, extrinsic components as well as the gate and substrate

resistances have a negligible effect to phase noise [85, 86]. Later we will verify that this assumption is acceptable.

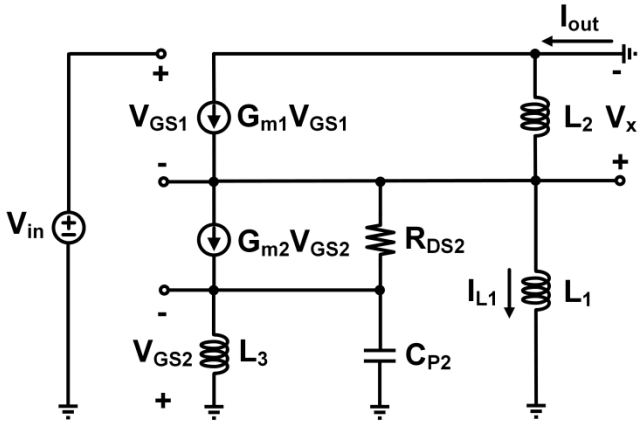


Fig. 5.4. Large-signal equivalent circuit of the Hartley oscillator circuit topology of Fig. 5.2 (a). G_{m1} and G_{m2} are the large-signal transconductance of M_1 and M_2 respectively. V_{in} is a voltage stimulus applied to the gate of M_1.

We can now write

$$C_{P2} = C_{GS2} + C_{SB2} \tag{5.16}$$

We will now calculate the equivalent transconductance for the circuit of Fig. 5.4 with respect to the voltage stimulus V_{in}, i.e. $G_{m,eq1}=I_{out}/V_{in}$. Next, we will determine L_3, for which the flicker and thermal phase noise components at the output of the Hartley oscillator circuit topology of Fig. 5.2 (a) reach the minimum values. For simplicity of the derived equations C_{P2} will be neglected.

From Kirchhoff Voltage Law (KVL)

$$V_{GS1} = V_{in} - V_x \tag{5.17}$$

Then, from KCL at the source of M_2

$$I_{L1} - \frac{V_{GS2}}{sL_3} - I_{out} = 0 \tag{5.18}$$

which can be rewritten as

$$V_{GS2} = -I_{out} sL_3 + V_x \frac{L_3}{L_1} \tag{5.19}$$

Moreover, from KCL at the source of M_1

$$\frac{V_x}{sL_2} - G_{m1}V_{GS1} + G_{m2}V_{GS2} + \frac{V_x}{sL_1} + \frac{V_x + V_{GS2}}{R_{DS2}} = 0 \tag{5.20}$$

Using now (5.17) and (5.19) into (5.20), we calculate

$$V_x = \frac{G_{m1}V_{in}}{G_{m1} + \frac{1}{sL_1} + \frac{1}{sL_2} + \left(G_{m2} + \frac{1}{R_{DS2}}\right)\frac{L_3}{L_1} + \frac{1}{R_{DS2}}} + \frac{\left(G_{m2} + \frac{1}{R_{DS2}}\right)I_{out}sL_3}{G_{m1} + \frac{1}{sL_1} + \frac{1}{sL_2} + \left(G_{m2} + \frac{1}{R_{DS2}}\right)\frac{L_3}{L_1} + \frac{1}{R_{DS2}}} \tag{5.21}$$

Finally, from KCL at the drain of M_1

$$G_{m1}V_{GS1} - I_{out} - \frac{V_x}{sL_2} = 0 \tag{5.22}$$

We can now substitute V_{GS1} and V_x in (5.22), with (5.17) and (5.21) respectively. $G_{m,eq1}$ can be written as

$$G_{m,eq1} = \frac{N_2}{D_2} \tag{5.23}$$

$$N_2 = \left(L_2G_{m1}\left(L_1 + L_3 + L_3G_{m2}R_{DS2}\right)\right)s + L_2G_{m1}R_{DS2} \tag{5.24}$$

$$\begin{aligned} D_2 = {} & \left(L_1L_2L_3G_{m1} + L_1L_2L_3G_{m1}G_{m2}R_{DS2}\right)s^2 + \left(L_1L_3 + L_2L_3 + L_1L_2 + L_1L_3G_{m2}R_{DS2} + \right. \\ & \left. L_2L_3G_{m2}R_{DS2} + L_1L_2G_{m1}R_{DS2}\right)s + R_{DS2}\left(L_1 + L_2\right) \end{aligned} \tag{5.25}$$

By replacing G_{m1} with $G_{m,eq1}$ in (5.15), take the derivative with respect to L_3 and equate to zero, we find that the value of L_3 which gives the minimum phase noise due to flicker noise is

$$L_3 = \left|\frac{N_3}{D_3}\right| \tag{5.26}$$

where

$$N_3 = \left(-L_1L_2R_pG_{m1}n^2 - L_1L_2 - L_1L_2G_{m1}R_{DS2}\right)s - L_2R_pG_{m1}R_{DS2}n^2 - L_1R_{DS2} - L_2R_{DS2} \tag{5.27}$$

$$D_3 = L_1L_2G_{m1}\left(G_{m2}R_{DS2} + 1\right)s^2 + \left(G_{m2}R_{DS2} + 1\right)\left(L_2R_pG_{m1}n^2 + L_1 + L_2\right)s \tag{5.28}$$

An equivalent derivation can also be done for the phase noise component due to the thermal noise of M_1, M_2 and the LC tank. From Chapter 4 and therein [OP3, 22] we have that the phase noise expression due to the thermal noise is

$$\mathcal{L}(\Delta\omega)\Big|_{thermal} = \left|\frac{K_B T}{4NI_B^2 R_p^3 C_{1eq}^2 \Delta\omega^2}\left(1-\frac{\Phi^2}{14}\right)^{-2} \times \left(\frac{\gamma}{n(1-n)}+\frac{1}{(1-n)^2}+\frac{n^2 R_p \gamma G_{m2}}{(1-n)^2}\right)\right| \tag{5.29}$$

where Φ is half the conduction angle defined by $\cos^{-1}[(V_{GS}-V_T)/V_1]$, with V_{GS} and V_T being the dc gate-to-source voltage and the threshold voltage of M_1 respectively. γ is the excess noise coefficient for the transistors M_1 and M_2.

Moreover that the bias current for transistor M_1 is given by

$$I_B = \frac{15\pi}{\left(\mu_n C_{ox}\frac{W}{L}\right)}\frac{1}{4}G_{m1}^2\left(1-\frac{\Phi^2}{14}\right)^{-2}\Phi^{-5}\left(1-\frac{4}{21}\Phi^2\right)^{-1} \tag{5.30}$$

Afterwards, we substitute G_{m1} in (5.30) with the expression of $G_{m,eq1}$ given by (5.23)-(5.25), and then use the calculated value of I_B in (5.29). The derived equation for phase noise can be minimized versus L_3. The value of L_3 which gives the minimum phase noise due to thermal noise is

$$L_3 = \left|\frac{N_4}{D_4}\right| \tag{5.31}$$

where

$$N_4 = (-L_1L_2 - L_1L_2G_{m1}R_{DS2})s - L_1R_{DS2} - L_2R_{DS2} \tag{5.32}$$

$$D_4 = (L_1L_2G_{m1} + L_1L_2G_{m1}G_{m2}R_{DS2})s^2 + (L_1 + L_2 + L_1G_{m2}R_{DS2} + L_2G_{m2}R_{DS2})s \tag{5.33}$$

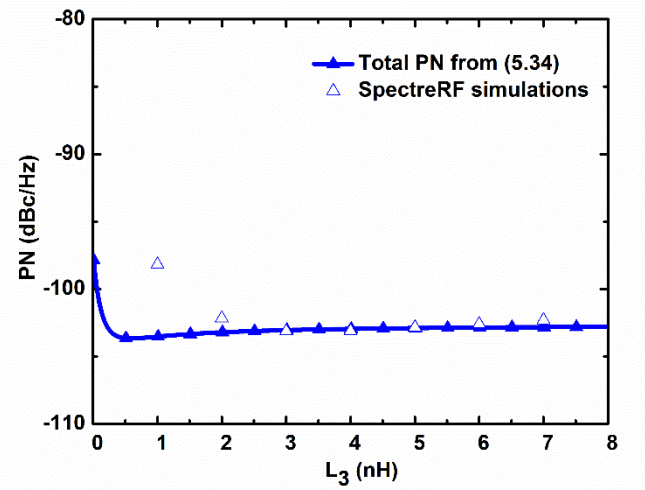
The total phase noise expression is found by adding the flicker and thermal phase noise components given by (5.15) and (5.29) respectively as follows

$$\mathcal{L}(\Delta\omega)\Big|_{total} = 10log_{10}\left[\mathcal{L}(\Delta\omega)\Big|_{flicker} + \mathcal{L}(\Delta\omega)\Big|_{thermal}\right] \tag{5.34}$$

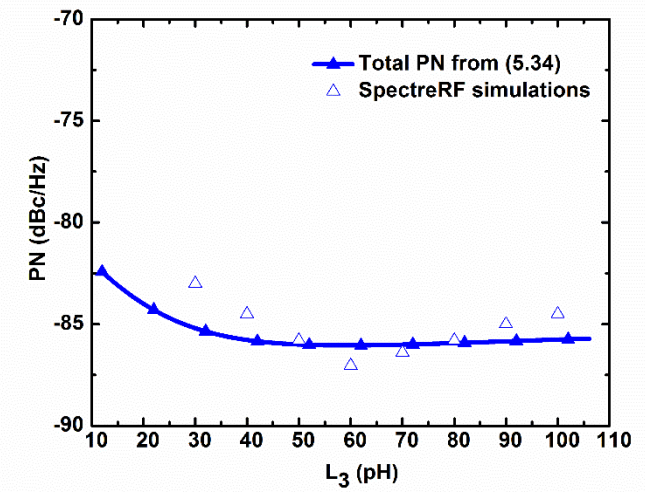
The total phase noise given by (5.34) is plotted in Figs. 5.5 (a)-(b) versus L_3, at an average bias current of 6.3 mA, for the oscillation frequencies of 10 GHz and 100 GHz, at a 1 MHz frequency offset.

From SpectreRF simulations, a minimum phase noise is achieved for L_3 equal to about 3 nH and 60 pH for the oscillation frequencies of 10 GHz and 100 GHz respectively. These values of inductance can be obtained by means of integrated inductors.

It is interesting observing that the optimum inductance value corresponds to the inductance value resonating, at or close to the oscillation frequency f_0, with the overall capacitance at the source node of M_2, given by the sum of C_{GS2} and C_{SB2}, equal to 23.5 and 31.7 fF, respectively, leading to an increase of the overall impedance at the drain node of M_2.



(a)



(b)

Fig. 5.5. Total phase noise at a 1 MHz frequency offset from the carrier vs. the degeneration inductance L_3 at an average bias current of 6.3 mA, for the circuit of Fig. 5.2 (a), predicted by (5.34) and obtained by SpectreRF simulations for the oscillation frequencies of (a) 10 GHz; (b) 100 GHz.

In regard of the upconversion of the flicker noise from M_1 and M_2, it is reduced as follows. The inductive degeneration acts in a similar way to the noise filter, since at the resonance frequency f_{filter} of the bandpass filter formed by L_3 and C_{P2}, the nonlinear capacitance present at the source node of M_2 is cancelled by L_3. Thereby, the modulation of the current flowing through the nonlinear junction capacitance present at the source node of M_2 and then through M_1 to the output, is minimized, as reported in Chapter 4 and therein [OP3].

At this stage, it is worth also comparing these results obtained from the Hartley topology with the inductive degeneration shown in Fig. 5.2 (a) with those obtained for the traditional Hartley oscillator circuit topology of Fig. 5.1, previously reported in Chapter 1 and therein [OP1, OP6]. In particular, from Chapter 1 and [OP1, OP6] the phase noise obtained under the same design conditions amounts to -92.75 dBc/Hz and -81.18 dBc/Hz for the oscillation frequencies of 10 GHz and 100 GHz respectively. Comparing these phase noise performances, we can observe that the Hartley topology with inductive degeneration can lead potentially to a phase noise reduction up to 10 dB and 6 dB for oscillation at 10 GHz and 100 GHz respectively.

Last, the results presented in Chapter 1 and therein [OP1, OP6] show that the $1/f^3$ region of the phase noise extends above a 1-MHz frequency offset for the Hartley oscillator circuit topology under study. This is a consequence of the adoption of nano-scale CMOS technologies characterized by flicker noise corners of several tens or hundreds of MHz, which lead to flicker noise up-conversion being responsible for most of phase noise even at large offsets from the carrier frequency. Thereby, the optimum inductance value for the total phase noise shown in Figs. 5.5 (a)-(b) is very close to that given by (5.26)-(5.28), since at a 1 MHz offset, thermal noise has a negligible effect on phase noise.

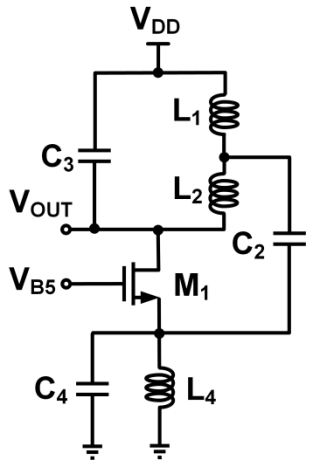
5.3 Noise Filter

In this section we will derive the analytical expression for the oscillation frequency (f_0) of a Hartley oscillator circuit topology in which we introduced a band-stop filter (L_4, C_4) to the source node of M_1 as shown in Fig. 5.6 (a). Due to its noise filtering action, it is referred therein [46, 71, 72] as noise filter. Moreover, we will observe that there is an optimum inductance value (L_4) for which the oscillator circuit topology exhibits a minimum phase noise and we will calculate such an optimum inductance which leads the noise filter to resonate at the oscillation frequency.

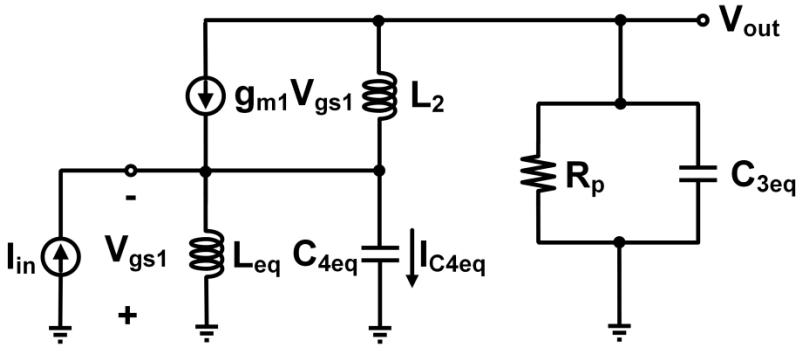
Again, in order to extract appropriate evaluations about the improvement of phase noise performance with respect to the traditional topology of Fig. 5.1, the oscillator circuit design will be carried out under the same transistor size, power and current consumption, inductance of the tank and its quality factor, as in Chapters 1, 2 and therein [OP1, OP2, OP6-OP8].

5.3.1 Oscillation Frequency

The Hartley oscillator circuit topology incorporating a noise filter is shown in Fig. 5.6 (a). Its small-signal equivalent circuit is shown in Fig. 5.6 (b). This equivalent circuit is obtained by considering the simplified transistor model with the small-signal transconductance (g_m), gate-to-source capacitance (C_{gs}), gate-to-drain capacitance (C_{gd}), source-to-bulk capacitance (C_{sb}) and drain-to-bulk capacitance (C_{db}). For simplicity of the derived equations, the small-signal output resistance r_{o1} as well as the polysilicon gate resistance r_g of M_1 are neglected. Later, we will verify that this hypothesis is acceptable. R_p represents the total load resistance of the LC tank, including the effect of the finite Q of the tank and the resistance seen from the source of M_1 scaled by the inductive divide factor.



(a)



(b)

Fig. 5.6. (a) Hartley oscillator circuit topology incorporating a noise filter. V_{B5} is the dc bias voltage. (b) Small-signal equivalent circuit. I_{in} is the input current stimulus used for the calculation of the closed-loop gain V_{out}/I_{in}.

The junction capacitances of transistors M_1 and M_2 in Fig. 5.1 behave nonlinearly during the oscillation period. Thereby, one of the major upconversion mechanisms of flicker noise is the modulation of the current flowing through the capacitance at the source node of M_1 [44]. By

removing M_2, the modulation of the current flowing through this capacitance is significantly reduced, due to the decrease of the nonlinear parasitic capacitance.

The presence of an optimum L_4 for minimum phase noise is due to L_4 resonating with the capacitance present at the source node of M_1, thereby acting as an ideal high impedance node at the resonance frequency of the noise filter. This results in further decrease of the modulation current, since this capacitance is effectively tuned out by L_4.

In order not to change the tank capacitance, the oscillation frequency can be tuned by changing the value of C_4. The amplitude of the tank voltage can be larger than in the topology of Fig. 5.1 since there is no tail transistor consuming voltage headroom. C_4, C_{gs1} and C_{sb1} appear in parallel. Their sum can be represented as an equivalent capacitance

$$C_{4eq} = C_4 + C_{gs1} + C_{sb1} \tag{5.35}$$

C_{3eq} is the parasitic capacitance present at the drain node of M_1, given by

$$C_{3eq} = C_3 + C_{db1} + C_{gd1} \tag{5.36}$$

L_{eq} is the parallel combination of L_1 and L_4 expressed as

$$L_{eq} = \frac{L_1 L_4}{L_1 + L_4} \tag{5.37}$$

In order to excite the circuit into oscillation we insert a current stimulus I_{in} at the source of M_1. From KCL at the source of M_1, we obtain

$$I_{C4eq} - I_{in} - \frac{V_{gs1}}{sL_{eq}} + \frac{V_{out}}{R_p} + V_{out} sC_{3eq} = 0 \tag{5.38}$$

also,

$$V_{gs1} = -I_{C4eq} \frac{1}{sC_{4eq}} \tag{5.39}$$

Solving (5.38) for I_{C4eq} and using the result in (5.39) we find

$$V_{gs1} = \frac{1}{1 + \dfrac{1}{s^2 L_{eq} C_{4eq}}} \frac{1}{sC_{4eq}} \left(-I_{in} + \frac{V_{out}}{R_p} + V_{out} sC_{3eq} \right) \tag{5.40}$$

and from KCL at the output

$$g_{m1}V_{gs1} + \frac{V_{out} + V_{gs1}}{sL_2} + \frac{V_{out}}{R_p} + V_{out}sC_{3eq} = 0 \tag{5.41}$$

Expressing (5.41) as a function of V_{gs1} and equating to (5.40), we can derive the closed-loop transfer function V_{out}/I_{in} as a ratio. By equating the real part of the denominator of this ratio to zero, we find that the oscillation frequency is given by

$$f_o = \frac{1}{2\pi}\omega_0 \tag{5.42}$$

where

$$\omega_o = \sqrt{\frac{N_5}{D_5}} \tag{5.43}$$

$$\begin{aligned} N_5 = {} & C_{4eq}L_{eq}R_p - \left(C_{4eq}^2L_{eq}^2R_p^2 - 2C_{4eq}C_{3eq}L_2L_{eq}R_p^2 + 2C_{4eq}C_{3eq}L_{eq}^2R_p^2 + 2C_{4eq}L_2L_{eq}^2R_pg_{m1} + C_{3eq}^2L_2^2R_p^2 + \right. \\ & \left. 2C_{3eq}^2L_2L_{eq}R_p^2 + C_{3eq}^2L_{eq}^2R_p^2 + 2C_{3eq}L_2^2L_{eq}R_pg_{m1} + 2C_{3eq}L_2L_{eq}^2R_pg_{m1} + L_2^2L_{eq}^2g_{m1}^2\right)^{1/2} + \\ & C_{3eq}L_2R_p + C_{3eq}L_{eq}R_p + L_2L_{eq}g_{m1} \end{aligned} \tag{5.44}$$

$$D_5 = 2C_{4eq}C_{3eq}L_2L_{eq}R_p \tag{5.45}$$

Figs. 5.7 (a)-(b) show the theoretical estimation of the oscillation frequency provided by (5.42)-(5.45), as a function of C_4. Simulations are repeated for three different values of L_4 in order to show the dependence of f_0 on L_4, which turns out being significant. Note that the oscillation frequency predicted by (5.42)-(5.45) closely follows the results obtained by circuit simulations.

Thereby, the aforementioned simplifications in the derivation of (5.42)-(5.45) are justified and lead to an accurate first-order prediction of the oscillation frequency f_0.

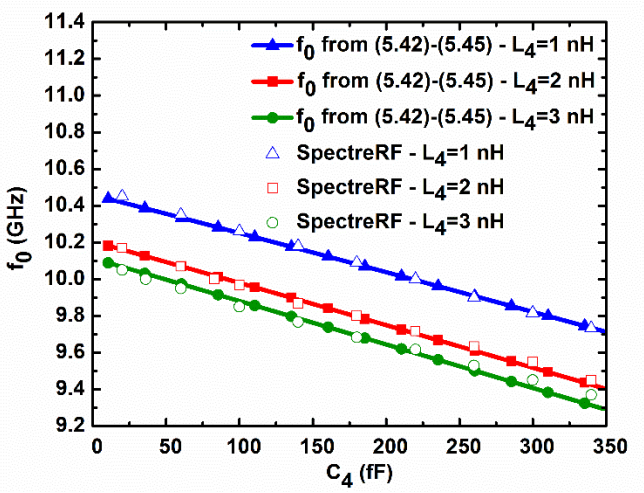
5.3.2 Optimum Inductance for Minimum Phase Noise

Here, our objective is to explore the dependence of phase noise on L_4 and to derive the condition for which the phase noise at the output of the Hartley oscillator circuit topology of Fig. 5.6 (a) can be reduced. The theoretical results will be compared with those obtained by means of SpectreRF simulations.

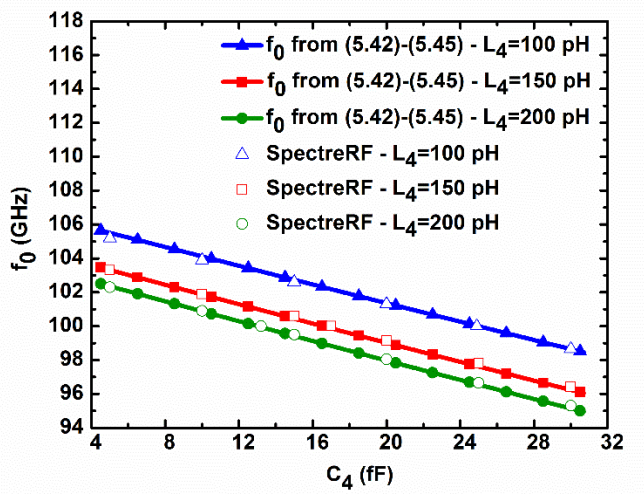
The large-signal equivalent circuit of the Hartley oscillator topology reported in Fig. 5.6 (a) is shown in Fig. 5.8. V_{in} is a voltage stimulus applied to the gate of M_1. Transistor M_1 is represented by a transconductance amplifier according to the describing function analysis [65]. G_{m1} is the large-signal transconductance of M_1, equal to the ratio of the fundamental harmonic of

the drain current of M_1 to the fundamental harmonic of the gate-source voltage of M_1. C_4 and the large-signal gate-to-source and source-to-bulk capacitances, C_{GS1} and C_{SB1} respectively, appear in parallel. Their sum can be represented as an equivalent capacitance

$$C_{4EQ} = C_4 + C_{GS1} + C_{SB1} \tag{5.46}$$



(a)



(b)

Fig. 5.7. Oscillation frequency vs. C_4 for the circuit of Fig. 5.6 (a) as predicted by (5.42)-(5.45) and SpectreRF simulations for oscillation frequencies in the vicinity of (a) 10 GHz; (b) 100 GHz.

First, we calculate the equivalent transconductance for the describing function model of Fig. 5.8 with respect to the voltage stimulus V_{in}, i.e. $G_{m,eq2}=I_{out}/V_{in}$. Next, we will derive the condition

on L_4 for which the flicker and thermal components of the phase noise at the output of the Hartley oscillator circuit topology of Fig. 5.6 (a) can be minimized.

We can write

$$Z_p = \frac{1}{sC_{4EQ}} // sL_1 // sL_4 = \frac{sL_1L_4}{L_1 + L_4 + s^2L_1L_4C_{4EQ}} \tag{5.47}$$

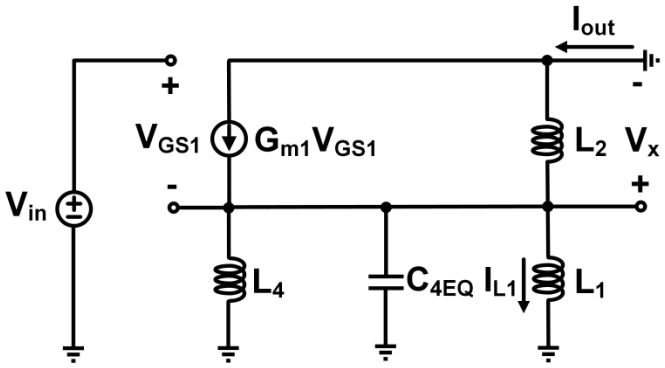


Fig. 5.8. Large-signal equivalent circuit of the Hartley oscillator circuit of Fig. 5.6 (a). G_{m1} is the large-signal transconductance of M_1. V_{in} is a voltage stimulus applied to the gate of M_1.

$$V_{in} = V_{GS1} + I_{out}Z_p \tag{5.48}$$

Using (5.47) into (5.48) and rewriting

$$V_{GS1} = V_{in} - I_{out}\frac{sL_1L_4}{L_1 + L_4 + s^2L_1L_4C_{4EQ}} \tag{5.49}$$

moreover

$$V_x = I_{out}Z_p = I_{out}\frac{sL_1L_4}{L_1 + L_4 + s^2L_1L_4C_{4EQ}} \tag{5.50}$$

also, from KCL at the drain of M_1

$$G_{m1}V_{GS1} - I_{out} - \frac{V_x}{sL_2} = 0 \tag{5.51}$$

Finally, replacing V_{GS1} and V_x into (5.51) with their values given by (5.49) and (5.50) respectively, we find $G_{m,eq2}$ as follows

$$G_{m,eq2} = \frac{G_{m1}}{1 + \frac{sL_1L_4}{L_1 + L_4 + s^2L_1L_4C_{4EQ}}\left(G_{m1} + \frac{1}{sL_2}\right)} \tag{5.52}$$

In order to calculate the value of L_4, for which the flicker noise present at the output of the Hartley oscillator circuit topology of Fig. 5.6 (a) reaches a minimum, we substitute G_{m1} in (5.15) with $G_{m,eq2}$ given by (5.52). Then, we take the derivative of the resulting equation with respect to L_4 and equate to zero to find

$$L_4 = \left|\frac{N_6}{D_6}\right| \tag{5.53}$$

where

$$N_6 = -\left(L_1L_2R_pG_{m1}n^2 + L_1L_2\right) \tag{5.54}$$

$$D_6 = \left(C_{4EQ}L_1L_2R_pG_{m1}n^2 + C_{4EQ}L_1L_2\right)s^2 + L_1L_2G_{m1}s + L_2R_pG_{m1}n^2 + L_1 + L_2 \tag{5.55}$$

A similar derivation can also be performed for the phase noise component due to the thermal noise of M_1, L_4 and the LC tank.

The phase noise expression due to the thermal noise is

$$\mathcal{L}(\Delta\omega)\Big|_{thermal} = \left|\frac{K_BT}{4NI_B^2R_p^3C_{1eq}^2\Delta\omega^2}\left(1 - \frac{\Phi^2}{14}\right)^{-2} \times \left(\frac{\gamma}{n(1-n)} + \frac{1}{(1-n)^2} + \frac{n^2R_p}{(1-n)^2}\frac{1}{Q\omega L_4}\right)\right| \tag{5.56}$$

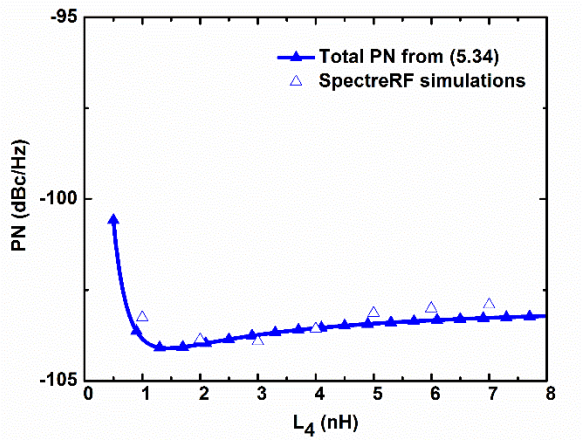
where K_B=1.38×10-23 V×C/K is the Boltzmann constant and T is the absolute temperature.

Afterwards, we substitute G_{m1} in (5.30) with the expression of $G_{m,eq2}$ given by (5.52) and use the calculated value of I_B in (5.56). After taking the derivative with respect to L_4 and equate to zero, we find that the value of L_4 for which the thermal phase noise component at the output of the Hartley oscillator circuit topology of Fig. 5.6 (a) reaches the minimum is given by

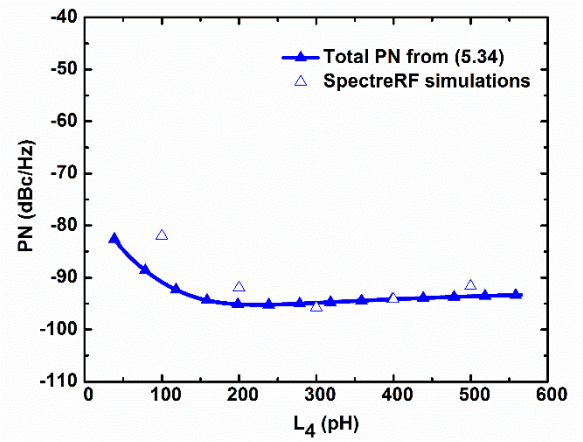
$$L_4 = \left|-\frac{L_1L_2}{C_{4EQ}L_1L_2s^2 + L_1L_2G_{m1}s + L_1 + L_2}\right| \tag{5.57}$$

The total phase noise is plotted in Figs. 5.9 (a)-(b) versus L_4, for an average current of 6.3 mA, for the oscillation frequencies of 10 GHz and 100 GHz, at a 1 MHz frequency offset. Note the relatively good agreement between the theoretical derivations and the SpectreRF simulations.

From SpectreRF simulations, the minimum phase noise is achieved for L_4 approximately equal to 3 nH and 300 pH for oscillation frequencies of 10 GHz and 100 GHz respectively. C_4 is here set to zero, and the inductance present at the source node of transistor M_1, resonates with the capacitance present at that node, given by the sum of C_{GS1} and C_{SB1}, equal to 21 and 7 fF respectively.



(a)



(b)

Fig. 5.9. Total phase noise at a 1 MHz frequency offset from the carrier vs. L_4, for the circuit of Fig. 5.6 (a) with an average bias current of 6.3 mA, as predicted by (5.34) and obtained by SpectreRF simulations for oscillation frequencies of (a) 10 GHz; (b) 100 GHz.

At this stage, it is worth also comparing these results obtained from the Hartley topology with noise filter of Fig. 5.6 (a) with those obtained for the traditional Hartley oscillator circuit topology of Fig. 5.1, previously reported in Chapter 1 and therein [OP1, OP6]. In particular, from Chapter 1 and [OP1, OP6] the phase noise obtained under the same design conditions amounts to -92.75 dBc/Hz and -81.18 for oscillation frequencies of 10 GHz and 100 GHz respectively. Comparing these phase noise performances, we can observe that the Hartley

oscillator circuit topology with noise filter can potentially allow a phase noise reduction up to 11 dB and 14 dB respectively.

As reported in Section 5.2, at a 1 MHz offset, thermal noise has a negligible effect. Thereby, the optimum inductance value for the total phase noise shown in Fig. 5.9 is very close to that given by (5.53)-(5.55).

5.4 Optimum Current Density

In this section, we will examine the method of minimizing the phase noise of the oscillator topology under study, through the choice of the bias current density. First, the phase noise components due to flicker and thermal noise will be expressed as a function of the bias current. Next, the resulting equations will be plotted versus the average current density and validated against SpectreRF simulations.

5.4.1 Inductive Degeneration

From Chapter 4 and [OP3] we can write

$$G_{m1} = -\frac{2I_B\left(1-\frac{\Phi^2}{14}\right)}{nV_{tank}} \tag{5.60}$$

where V_{tank} is the amplitude of the fundamental harmonic of the tank voltage, equal to V_1/n.

With reference to the Hartley oscillator circuit topology with the inductive degeneration (L_3) at the source node of the tail current transistor (M_2) shown in Fig. 5.2 (a), we use G_{m1} given by (5.60) into (5.23)-(5.25) in order to express $G_{m,eq1}$ in terms of I_B. Then, for the flicker component of the phase noise, we use (5.15) where G_{m1} is substituted by the value of $G_{m,eq1}$ calculated above. After taking the derivative of the resulting equation with respect to I_B and equating to zero, we find

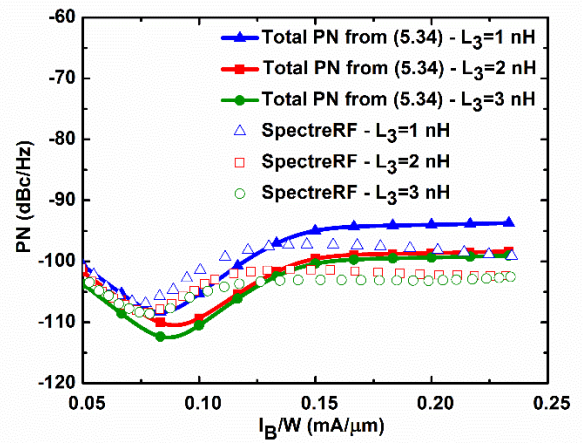
$$I_B = \left|\frac{N_7}{D_7}\right| \tag{5.61}$$

where

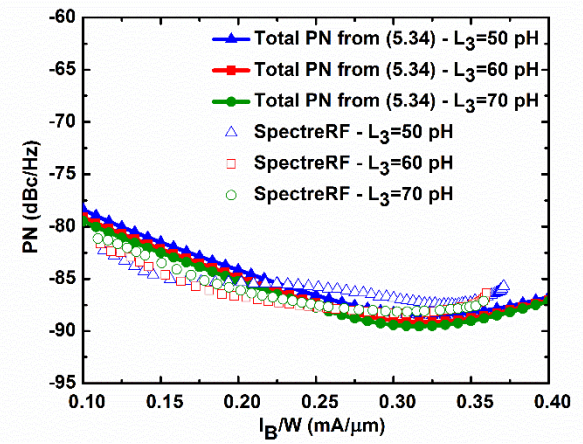
$$N_7 = 7V_{tank}\left[\left(L_1L_3n + L_2L_3n + 7L_1L_2n + L_1L_3G_{m2}nR_{DS2} + L_2L_3G_{m2}nR_{DS2}\right)s + L_1nR_{DS2} + L_2nR_{DS2}\right] \tag{5.62}$$

$$\begin{aligned} D_7 = {} & \left(14-\Phi^2+14G_{m2}R_{DS2}-\Phi^2G_{m2}R_{DS2}\right)L_1L_2L_3s^2+\left(14L_1L_2R_{DS2}-\Phi^2L_1L_2R_{DS2}+14L_2L_3R_pn^2+\right. \\ & 14L_1L_2R_pn^2-\Phi^2L_2L_3R_pn^2-\Phi^2L_1L_2R_pn^2+14L_2L_3R_pG_{m2}n^2R_{DS2}-\Phi^2L_2L_3R_pG_{m2}n^2R_{DS2}\left.\right)s- \\ & L_2R_pR_{DS2}\Phi^2n^2+14L_2R_pR_{DS2}n^2 \end{aligned} \tag{5.63}$$

As for the thermal noise contribution to phase noise, there is no optimum bias current density. By examining (5.29), it can be observed that the phase noise due to the thermal noise decreases for higher values of I_B.



(a)



(b)

Fig. 5.10. Total phase noise at a 1 MHz frequency offset from the carrier vs. the bias current density I_B/W for the circuit of Fig. 5.2 (a), predicted by (5.34) and obtained by SpectreRF simulations for oscillation frequencies of (a) 10 GHz; (b) 100 GHz.

The total phase noise is given by (5.34) where the flicker and thermal components of the phase noise have been replaced by the new derivations. The total phase noise is plotted in Figs. 5.10 (a)-(b) versus the bias current per unit of width I_B/W and validated by means of the results provided by SpectreRF simulations in Cadence, for a 1 MHz frequency offset from the carrier. In order to demonstrate the dependence of phase noise on L_3, the total phase noise is plotted for three different values of L_3. V_{B3} in Fig. 5.2 (a) is connected to V_{DD}, whereas V_{B4} has been swept from the value required to start up the oscillations to V_{DD}.

At 10 GHz, both theory and simulations predict a current density of about 0.075 mA/μm for which phase noise reaches a minimum. This value is weakly dependent on L_3, despite slightly increasing for higher values of L_3.

On the other hand, at 100 GHz, both theory and simulations predict a bias current density of around 0.325 mA/μm for which phase noise is minimized.

From Figs. 5.10 (a)-(b) we can calculate the difference in phase noise between the values obtained for the bias current of 6.3 mA considered in Section 5.2, corresponding to a bias current density of 0.21 mA/μm, and the optimum bias current density of 0.075 mA/μm. SpectreRF simulation results for 10 GHz show a reduction of phase noise of about 6 dB for L_3 equal to 3 nH and optimum bias current density of 0.075 mA/μm. At 100 GHz the phase noise reduction appears limited to 2 dB for L_3 equal to 70 pH and bias current density of 0.325 mA/μm. However, it is worth noting that the phase noise reduction depends on the proximity of phase noise performance between the optimum bias current density and the current density of 0.21 mA/μm considered in Section 5.2, but potentially could be larger (i.e. depends on the term of reference for the comparison).

Anyway, by summing up the phase noise reduction provided for 10 GHz by the inductive degeneration of 3 nH and optimum bias current density of 0.125 mA/μm, a potential overall reduction up to 13 dB can be achieved. For 100 GHz, a potential overall reduction provided by the inductive degeneration of 70 pH and optimum bias current density of 0.325 mA/μm amounts to 7 dB.

5.4.2 Noise Filter

With reference to the Hartley oscillator circuit topology of Fig. 5.6 (a), where a noise filter (L_4, C_4) has been introduced to the source node of M_1, for the phase noise component contributed by flicker noise, we use G_{m1} given by (5.60) into (5.52) in order to express $G_{m,eq2}$ in terms of I_B.

The value of G_{m1} in (5.15) is then substituted by the value of $G_{m,eq2}$ calculated before. After taking the derivative of the resulting equation with respect to the bias current I_B and equate to zero, we obtain the following expression

$$I_B = \left| \frac{N_8}{D_8} \right| \tag{5.64}$$

where

$$N_8 = 7V_{tank}\left(C_{4EQ}L_1L_2L_4ns^2 + L_1L_4n + L_2L_4n + L_1L_2n\right) \tag{5.65}$$

$$D_8 = C_{4EQ}L_1L_2L_4R_pn^2\left(14-\Phi^2\right)s^2 + L_1L_2L_4\left(14-\Phi^2\right)s + R_pn^2\left(14L_1L_2 + 14L_2L_4 - \Phi^2L_1L_2 - \Phi^2L_2L_4\right) \tag{5.66}$$

As for the thermal noise contribution to phase noise there is no optimum bias current density. By examining (5.56), it can be observed that the phase noise due to the thermal noise decreases as I_B increases.

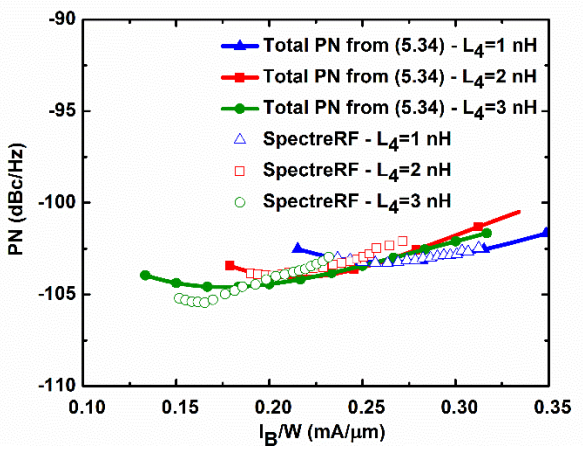
The total phase noise is given by (5.34) where the flicker and thermal phase noise components have been replaced by the new derivations. It is plotted in Figs. 5.11 (a)-(b) versus the bias current per unit of width I_B/W and validated by means of the results provided by SpectreRF simulations in Cadence, at a 1 MHz frequency offset from the carrier. In order to demonstrate the dependence of phase noise on L_4, the total phase noise is plotted for three values of L_4. C_4 is set equal to zero. V_{B5} has been swept from the value required to start up the oscillation to V_{DD}.

At 10 and 100 GHz, for L_4=3 nH and L_4=200 pH respectively, both theory and simulations predict a bias current density of around 0.17 and 0.26 mA/μm respectively for which phase noise is minimized.

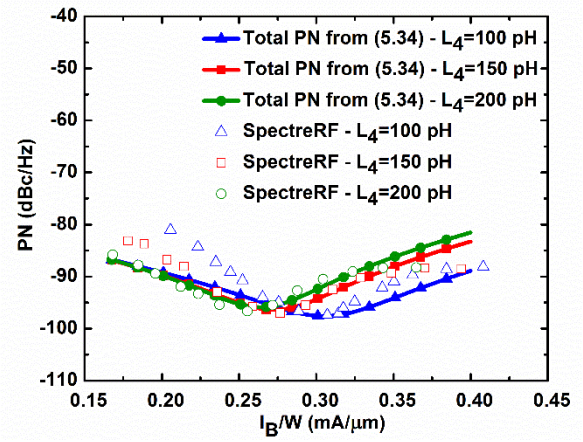
From Figs. 5.11 (a)-(b) we can calculate the difference of phase noise between the results obtained for the bias current of 6.3 mA adopted in Section 5.3, corresponding to a current density of 0.21 mA/μm, and the optimum current density. From SpectreRF simulations at 10 GHz, for instance, a phase noise reduction of about 2 dB can be achieved for L_4 of 3 nH and a current density of 0.17 mA/μm. For the oscillation frequency of 100 GHz, the improvement is around 5 dB for L_4 equal to 200 pH and a current density of about 0.26 mA/μm.

It is worth noting that the phase noise reduction depends on the proximity of phase noise performance between the optimum bias current density and the current density of 0.21 mA/μm considered in Section 5.3, but potentially could be larger (i.e. depends on the term of reference for the comparison).

By summing up the phase noise reduction provided for 10 GHz by the Hartley topology with the noise filter for 3 nH and optimum bias current density of about 0.17 mA/μm, a potential overall reduction up to 18 dB can be achieved with respect to the traditional Hartley topology shown in Fig. 5.1. For 100 GHz, the potential overall reduction provided by L_4 of 200 pH and optimum current density of 0.26 mA/μm amounts to 16 dB. Note that due to the very close phase noise performance, the case of 200 pH and 0.26 mA/μm lead to a lower current consumption and, thereby, potentially to a better figure of merit of the oscillator with respect to the case of 100 pH with a current consumption of 0.31 mA/μm.



(a)



(b)

Fig. 5.11. Total phase noise at a 1 MHz frequency offset from the carrier vs. the bias current density I_B/W for the circuit of Fig. 5.6 (a), predicted by (5.34) and obtained by SpectreRF simulations for the oscillation frequencies of (a) 10 GHz; (b) 100 GHz.

The contents of this chapter are being submitted for publication in the International Journal on Circuit Theory and Applications.

5.5 Conclusions

The techniques of inductive degeneration and noise filter for the reduction of phase noise due to the tail transistor in CMOS LC oscillators have been applied for the first time to a single-ended Hartley oscillator circuit topology. These techniques have been analyzed in detail by means of circuit theory and simulations.

The analyses have allowed us to bring to the light a few interesting aspects not identified yet by the literature. In particular, an analytical expression of the oscillation frequency has been derived in order to allow a good prediction and show the dependence on the degeneration

inductance. In addition, an analytical expression of the phase noise has been derived in order to allow a good prediction and identify design opportunity for phase noise reduction in the above techniques. The theoretical results, confirmed by means of circuit simulations, demonstrate that the phase noise of the Hartley oscillator topology modified with the introduction of either the inductive degeneration or the noise filter reaches a minimum, leading to considerable potential benefits. In particular, there is an optimum degeneration inductance which resonates at the oscillation frequency with the parasitic capacitance at the source of the tail current transistor. In addition, that for a given typical capacitance there is an optimum inductance for which the noise filter resonates at the oscillation frequency. Last, that it is possible to integrate a degeneration or noise filter inductor, in particular for oscillation frequencies of 10 and 100 GHz.

Moreover, a third technique for the phase noise reduction, namely optimum current density, has been applied to the Hartley topology with either the inductive degeneration or the noise filter and analyzed in detail by means of circuit theory and simulations. It consists of biasing the oscillator circuit with the optimum bias current density for the minimum phase noise. The proposed analyses allow us for the first time to get an understanding of the theoretical details of this technique and its applications, identifying additional opportunities for the reduction of phase noise in the examined circuit topology.

Overall, the analyses carried out for multiple degeneration inductances, noise filter inductances and current density variations allow also some evaluations about the sensitivity of the respective phase noise reduction techniques.

The results of the analyses presented show that, under the adopted common design conditions, the above techniques may potentially lead to phase noise reduction up to 18 dB and 16 dB at a 1 MHz frequency offset from the oscillation frequencies of 10 GHz and 100 GHz respectively, with respect to the traditional Hartley topology.

Chapter 6

Design of a Low Phase Noise Differential Colpitts VCO Topology

6.1 Introduction

Oscillator phase noise is very critical for the CMOS implementation of emerging high data rates wireless communication systems at the millimeter-waves, e.g. 60 GHz, [87], especially considering the rising role of flicker noise in latest nano-scale technology nodes [OP1, OP2, OP6-OP8] and the high-frequency losses associated to the parasitic components. Over the past years, the phase noise of oscillators operating at a few gigahertz achieved performance better than -130 dB/Hz at a 1 MHz frequency offset [87]. These performances are far from those currently achievable in the millimeter-wave (mm-wave) frequency range, where the oscillator design is still a severe challenge. Thereby, investigating phase noise reduction techniques at the mm-waves is in order.

The results of the analyses of the phase noise reduction techniques reported in Chapters 4, 5 and therein [OP3, OP9-OP12], in particular inductive degeneration, noise filter, and optimum current density, show that these design techniques when combined may offer a phase noise reduction of up to 20 dB. In Chapters 4, 5 and therein [OP3, OP9-OP12] we investigated these techniques for single-ended Colpitts and Hartley topologies. Assuming a perfect symmetry, common-mode noise sources (e.g. noise coming from the common bias circuitry) do not produce effects in a differential topology; thereby, leading potentially to lower phase noise. Consequently, it is worth considering applying these techniques to differential Colpitts and Hartley topologies as well.

Moreover, in Chapter 2 and therein [OP2, OP7, OP8], we carried out comparative analyses of phase noise for four oscillator circuit topologies: common-source cross-coupled pair, Colpitts, Hartley and Armstrong, under common conditions. The investigations allowed us to extend the range of design possibilities beyond the common practice of choosing the common-source cross-coupled differential pair topology, traditionally selected for its reliable start-up, but without further topological considerations. The results presented in Chapter 2 and therein [OP2, OP7, OP8], suggest the opportunity to invest additional studies and efforts in exploring the circuit design implementations also of other topologies, whose potential may have been perhaps underestimated up to date, especially at very high frequencies.

Based on the above motivations, in this chapter, we present a novel differential Colpitts voltage-controlled oscillator (VCO) topology using the techniques of noise filter, optimum current density and transformer coupling for phase noise reduction.

In Section 6.2 the analytical expressions of the oscillation frequency f_0, the startup condition, and the output voltage are derived by means of circuit theory. In Section 6.3, the post-

layout simulation results are reported and compared with the state of the art. Finally, conclusions are drawn in Section 6.4.

6.2 Oscillation Frequency and Output Voltage

Fig. 6.1 shows the novel differential Colpitts LC oscillator circuit topology designed in 28 nm fully-depleted silicon-on-insulator (FDSOI) CMOS technology with 1 V supply voltage. The amplitude of the tank voltage can be larger than in the traditional differential Colpitts oscillator circuit topology, since there is no tail transistor consuming voltage headroom. Moreover, the magnetic coupling between L_1 and L_2 pairs leads to an enhancement of the equivalent quality factor of the LC tank.

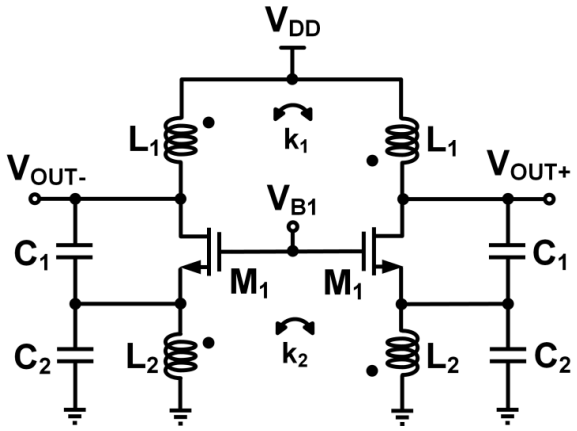


Fig. 6.1. Schematic of the differential Colpitts oscillator circuit topology. V_{B1} is a dc bias voltage.

In this section we will derive closed-form expressions for the oscillation frequency, the startup condition, and the output voltage, for the circuit of Fig. 6.1.

6.2.1 Oscillation Frequency

The small-signal single-ended equivalent circuit of Fig. 6.1 for derivation of the closed-loop transfer function is reported in Fig. 6.2. This equivalent circuit is obtained by considering the simplified transistor model with the small-signal transconductance (g_m), gate-to-source capacitance (C_{gs}), gate-to-drain capacitance (C_{gd}), source-to-bulk capacitance (C_{sb}) and drain-to-bulk capacitance (C_{db}). In the interest of a low complexity of the derived equations, the small-signal output resistance r_o, as well as the polysilicon gate resistance r_g of M_1, are neglected. C_p is the parasitic capacitance at the drain node of M_1, equal to the sum of C_{db} and C_{gd}. C_2' is the sum of C_2 with C_{gs} and C_{sb}. The parasitic resistors R_1 and R_2 are the parasitic resistance in series with L_1 and L_2 respectively. L_1' and L_2' are equal to $(1+k_1)\times L_1$ and $(1+k_2)\times L_2$ respectively. Q_1 and Q_2 are the quality factor of L_1 and L_2 respectively.

In order to excite the circuit into oscillation we insert a current stimulus I_{in} at the source of M_1. We can now write that

$$Z_1 = \frac{L_1' s + R_1}{C_p L_1' s^2 + C_p R_1 s + 1} \tag{6.1}$$

$$Z_2 = \frac{L_2' s + R_2}{C_2' L_2' s^2 + C_2 R_2 s + 1} \tag{6.2}$$

$$V_{gs} = -V_X \tag{6.3}$$

$$g_m V_{gs} + (V_{out} - V_X) s C_1 + \frac{V_{out}}{Z_1} = 0 \tag{6.4}$$

$$\frac{V_X}{Z_2} - g_m V_{gs} - I_{in} - (V_{out} - V_X) s C_1 = 0 \tag{6.5}$$

From (6.1)-(6.5), we derive the closed-loop transfer function as follows

$$\frac{V_{out}(s)}{I_{in}(s)} = \frac{C_1 L_1' L_2' s^3 + \left[C_1 (L_1' R_2 + L_2' R_1) + L_1' L_2' g_m\right] s^2 + \left[g_m (L_1' R_2 + L_2' R_1) + C_1 R_1 R_2\right] s + R_1 R_2 g_m}{L_1' L_2' (C_1 C_2' + C_1 C_p + C_2' C_p) s^4 + A s^3 + B s^2 + \left[L_2' g_m + C_1 R_1 + R_2 (C_1 + C_2' + C_p R_1 g_m) + C_p R_1\right] s + R_2 g_m + 1} \tag{6.6}$$

where

$$A = (L_1' R_2 + L_2' R_1)(C_1 C_2' + C_1 C_p + C_2' C_p) + C_p L_1' L_2' g_m \tag{6.7}$$

$$B = L_1' (C_1 + C_p) + L_2' (C_1 + C_2') + R_1 R_2 (C_1 C_2' + C_1 C_p + C_2' C_p) + C_p g_m (L_1' R_2 + L_2' R_1) \tag{6.8}$$

By equating the denominator of the closed-loop transfer function to zero, we derive the oscillation frequency f_0 and the condition for oscillation. If $L_1'=L_2'= L'$ and $R_1=R_2=R$, then

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{L'(2C_1 + C_2' + C_p) + C_1 C_2' R^2 + C_p R^2 (C_1 + C_2') + 2C_p L' R g_m + \sqrt{C}}{2L'^2 (C_1 C_2' + C_1 C_p + C_2' C_p)}} \tag{6.9}$$

where

$$C = 4L'^2 R g_m \left[(C_1 C_p - C_1 C_2') + C_p^2 (R g_m + 1)\right] + 2L' R^2 \left[2C_1^2 (C_2' + C_p) + C_2'^2 (C_1 + C_p) + C_p^2 (C_1 + C_p)\right] +$$
$$L'^2 \left[4C_1^2 + (C_2' - C_p)^2\right] + 4C_1 C_2' C_p L' R^2 (R g_m + 2) + 4L' R^3 g_m C_p^2 (C_1 + C_2') + R^4 (C_1 C_2' + C_1 C_p + C_2' C_p)^2 \tag{6.10}$$

and the necessary condition for oscillation is

$$g_m R \geq \frac{\left[2C_1 + C_2' + C_p - 2L'\omega^2\left(C_1C_2' + C_1C_p + C_2'C_p\right)\right]}{Q_{1,2}^2\left(C_p - \frac{1}{L'\omega^2}\right) - C_p} \tag{6.11}$$

At f_0=60 GHz, (6.11) yields that $g_m(Q^2R)\geq 1.12$ for oscillations to start.

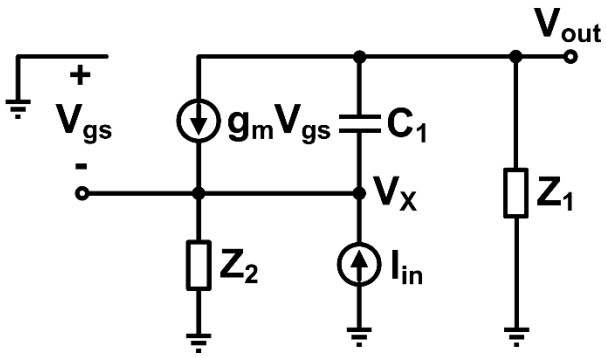


Fig. 6.2. Small-signal single-ended equivalent circuit of Fig. 6.1 for derivation of the closed-loop transfer function.

6.2.2 Output Voltage

In order to derive an analytical expression for the output voltage at the drain node of M_1, the drain current is approximated by its fundamental component $I_{\omega o}$. The single-ended large-signal equivalent circuit of the differential Colpitts oscillator circuit topology reported in Fig. 6.1 is shown in Fig. 6.3.

Z_3 and Z_4 are given by

$$Z_3 = \frac{L_1's + R_1}{C_7L_1's^2 + C_7R_1s + 1} \tag{6.12}$$

$$Z_4 = \frac{L_2's + R_2}{C_6L_2's^2 + C_6R_2s + 1} \tag{6.13}$$

where C_6 is the sum of C_2 with the large-signal gate-to-source and source-to-bulk capacitances, C_{GS} and C_{SB} respectively, and C_7 is the sum of the large-signal drain-to-bulk and gate-to-drain capacitances C_{DB} and C_{GD} respectively. C_{GS}, C_{SB}, C_{DB}, and C_{GD}, are set equal to the average value of C_{gs}, C_{sb}, C_{db}, and C_{gd}, respectively, during the oscillation period.

From Fig. 6.3 we can derive the following expression for the output voltage.

$$V_{out2} = \frac{C_6L_1'L_2's^3 + C_6L_1'R_2C_6L_2'R_1s^2 + \left(L_1' + C_6R_1R_2\right)s + R_1}{L_1'L_2'\left(C_1C_6 + C_1C_7 + C_6C_7\right)s^4 + Ks^3 + Ls^2 + \left(C_1R_1 + C_1R_2 + C_6R_2 + C_7R_1\right)s + 1} I_{\omega o} \tag{6.14}$$

where

$$K = \left(L_1' R_2 + L_2' R_1\right)\left(C_1 C_6 + C_1 C_7 + C_6 C_7\right) \tag{6.15}$$

$$L = C_1 L_1' + C_1 L_2' + C_6 L_2' + C_7 L_1' + R_1 R_2 \left(C_1 C_6 + C_1 C_7 + C_6 C_7\right) \tag{6.16}$$

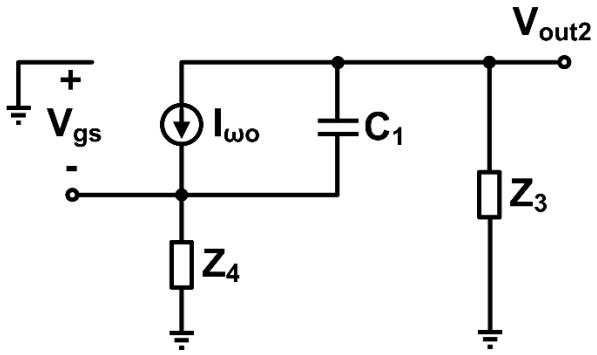


Fig. 6.3. Single-ended large-signal equivalent circuit for derivation of an analytical expression for the output voltage at the drain node of M_1, for the differential Colpitts oscillator circuit topology reported in Fig. 1.

6.3 Post-Layout Simulation Results

Fig. 6.4 reports the schematic of the proposed differential Colpitts VCO circuit topology including the tuning network and the buffers. The tuning network uses a bank of capacitors for coarse tuning, and varactors for fine tuning. The buffers are implemented by means of source followers. The VCO has been designed and implemented in 28 nm fully-depleted silicon-on-insulator (FDSOI) CMOS technology with 1 V supply voltage. V_{ctrl} is the control dc voltage for biasing the varactors. $V_{DD,buffer}$ is equal to 1 V. The VCO is biased at the current density optimum for minimum phase noise, using the technique reported in Chapters 4, 5 and therein [OP3, OP7-OP8].

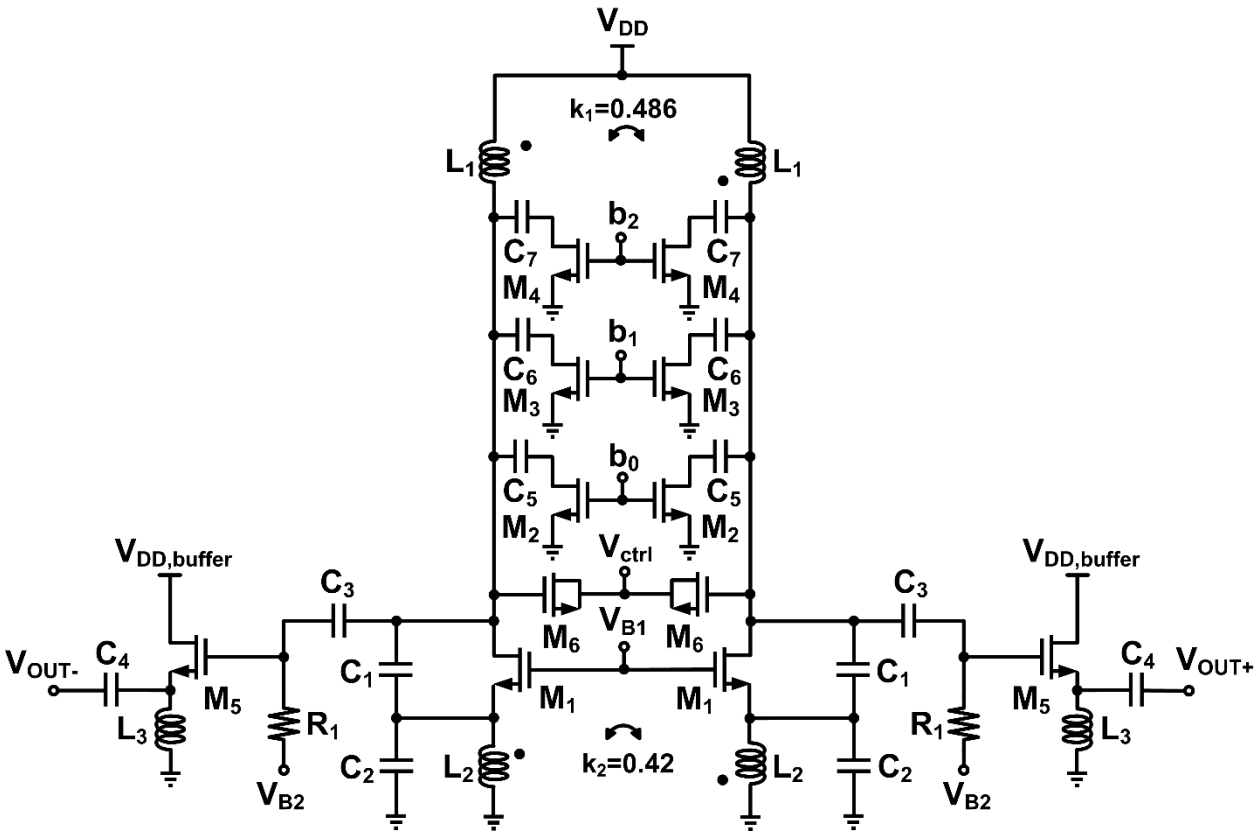


Fig. 6.4. Schematic of the differential Colpitts VCO. V_{B1} and V_{B2} are dc bias voltages.

The VCO topology can be tuned from 58.1 GHz to 63.3 GHz. From post-layout PSS and Pnoise SpectreRF simulations, the best phase noise performance is observed for f_0=63.3 GHz, and amounts to -100.2 dBc/Hz at a 1 MHz frequency offset from the oscillation frequency, for a power consumption of 13.6 mW, excluding the buffers. This corresponds to a figure of merit (FOM) of 185 dB [27].

Fig. 6.5 reports the phase noise obtained by direct plots from post-layout PSS and Pnoise circuit simulations in SpectreRF, for an oscillation frequency of 60 GHz.

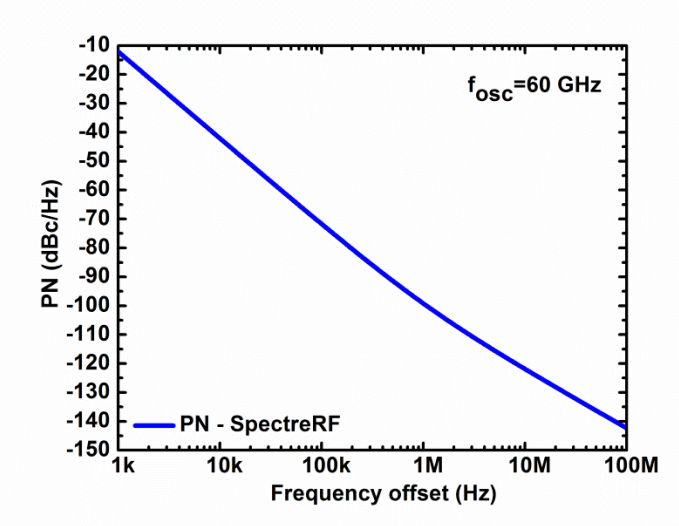


Fig. 6.5. Phase noise vs. frequency offset obtained from direct plots through post-layout PSS and Pnoise SpectreRF simulations for the oscillation frequency of 60 GHz.

A summary of the performance achieved by the proposed differential Colpitts VCO circuit topology and a comparison with the state-of-the-art solutions for 60 GHz CMOS VCOs are reported in Table 6.1.

Table 6.1 . Summary of Performance and Comparison with the State of the Art.

Ref.	Technology	Freq. [GHz]	PN @ 1 MHz freq. offset [dBc/Hz]	Power [mW]	FOM
[89]*	0.18 µm BiCMOS	55.7-66	-93.5	19.1	181
[90]*	65 nm CMOS	48.8-62.3	-96	15.6	176
[91]*	90 nm CMOS	56.2-62.2	-93	12	181
[92]*	65 nm CMOS	55.1-70.4	-92.2	21.5	182.6
[93]*	90 nm CMOS	58.76-63.94	-90.9	7.2	178.1
This work**	28 nm CMOS	58.1-63.3	-100.2	13.6	185

* measurements
** simulations

Assuming that the simulation results reported here will be confirmed by on-chip measurements, this VCO exhibits the lowest phase noise, the highest FOM and one of the lowest power consumptions with respect to the state of the art.

The contents of this chapter are being reported in an invention disclosure and patent, and will be submitted to high-quality peer-reviewed international conference and journal after patent filing.

6.4 Conclusions

In this chapter a novel differential Colpitts voltage-controlled oscillator (VCO) topology is reported. Assuming that the simulation results will be confirmed by on-chip measurements, this VCO circuit topology exhibits the lowest phase noise, the highest FOM and one of the lowest power consumptions with respect to the state of the art.

Recent studies refer to the common-source cross-coupled differential pair topology as the one with the best phase noise as a consequence of the circuit designs carried out at lower frequencies. The results reported in this chapter suggest that it is worth investing additional studies and efforts in exploring the circuit design implementations also of other topologies, whose potential might have been underestimated until today, especially at very high frequencies. In particular, the differential Colpitts topology presented in this chapter using the techniques of noise filter, transformer coupling and optimum current density, shows a potential for low phase noise at the 60 GHz band. Our investigations could allow us to extend the range of possibilities beyond the common practice of choosing the common-source cross-coupled differential pair topology, especially at the millimeter-wave frequency range where the quality factor of passive devices limits the obtained phase noise performance.

Conclusions

In Chapter 1 phase noise comparative analyses were carried out for Colpitts, Hartley and common-source cross-coupled differential pair LC oscillator topologies in the frequency range from 1 to 100 GHz. The investigations on the phase noise contributions from each component of these oscillator circuit topologies were reported and discussed in detail. The results show that, under the adopted design conditions, the three oscillator topologies rank unevenly in terms of the best phase noise performance rating scale for oscillation frequencies from 1 to 100 GHz. Moreover, the comparative analyses show that there is no superior topology in the absolute sense, but that the identification of the best circuit topology with respect to phase noise is strictly related to the operating frequency range.

In Chapter 2 comparative analyses of phase noise were carried out for four differential oscillator circuit topologies: common-source cross-coupled pair, Colpitts, Hartley and Armstrong. The oscillator circuit topologies were designed in a 28 nm bulk CMOS technology, for a set of operating frequencies in the range of 1 to 100 GHz. The results show that, under the adopted design conditions, the phase noise of the four topologies degrades unevenly over the considered oscillation frequency range. In particular, the comparative analyses show the existence of five distinct frequency regions. Moreover, the investigations through the impulse sensitivity function allowed the identification of the dominant noise contributions for each oscillator circuit topology. Despite a few exceptions, the results showed that the flicker noise from the active devices is the component with the most significant effect on the oscillator phase noise at a 1 MHz frequency offset from the carrier frequency, confirming the rising role of flicker noise in nano-scale CMOS technology.

Chapter 3 reports a theoretical analysis of the phase noise in a differential Armstrong oscillator circuit topology, both in the $1/f^3$ and $1/f^2$ regions, in order to allow accurate predictions. The derived analytical expressions of the phase noise have been validated through a direct comparison with the results obtained by SpectreRF simulations for a discrete set of oscillation frequencies spanning over two decades from 1 to 100 GHz. Under the adopted design conditions, the theoretical and simulation results are in a good agreement, with a maximum deviation of about 3 dB at 100 GHz.

In Chapter 4 the techniques of inductive degeneration, noise filter and optimum current density for the reduction of phase noise in CMOS LC oscillators were applied to a single-ended Colpitts oscillator circuit topology. These techniques have been analysed in detail for the first time by means of circuit theory and simulations. Unlike reported in previous works, the theoretical results, supported by circuit simulations, show for the first time that there is an optimum degeneration inductance which resonates at the oscillation frequency with the parasitic capacitance present at the source of the tail current transistor. Also that it is possible to integrate a degeneration or noise filter inductance for the oscillation frequencies of 10 and 100 GHz. The results show that, under the adopted common design conditions in a 28 nm CMOS technology,

these techniques may potentially lead to phase noise reduction up to about 19 dB and 17 dB at a 1 MHz offset from the oscillation frequencies of 10 GHz and 100 GHz respectively, with respect to the traditional Colpitts topology.

In Chapter 5 the techniques for phase noise reduction reported in Chapter 4 have been applied and studied for the first time to a single-ended Hartley oscillator circuit topology. The results of the analyses presented show that, under the adopted common design conditions, these techniques may potentially lead to phase noise reduction up to 18 and 16 dB at a 1 MHz frequency offset from the oscillation frequencies of 10 and 100 GHz respectively, with respect to the traditional Hartley topology.

Chapter 6 reports the design of a novel differential Colpitts voltage-controlled oscillator (VCO) topology adopting the techniques for phase noise reduction reported in Chapters 4 and 5. The VCO topology can be tuned from 58.1 GHz to 63.3 GHz. From PSS and Pnoise SpectreRF simulations the best phase noise performance is observed for f_0=63.3 GHz, and amounts to -100.2 dBc/Hz at a 1 MHz frequency offset from the oscillation frequency, for a power consumption of 13.6 mW. This corresponds to a figure-of-merit (FOM) of 185 dB.

In conclusion, nowadays, the most popular oscillator topology used is the common-source cross-coupled differential traditionally selected for its reliable start-up, but without further topological considerations. The investigations reported in this thesis could allow us to extend the range of possibilities beyond the common practice of choosing a priori the common-source cross-coupled differential pair topology. In particular, the results reported here show that there is no superior topology in the absolute sense, but that the identification of the best circuit topology with respect to phase noise is strictly related to the operating frequency range. Moreover, the results presented here, suggest the opportunity to invest additional studies and efforts in exploring the circuit design implementations also of other topologies, whose potential may have been perhaps underestimated up to date, especially at very high frequencies for which, thanks to the recent advances in the nano-scale technology process, MOSFETs with cut-off and max frequencies in excess of 280 and 350 GHz [29], respectively, are available for a potential use in a number of emerging wireless applications in the millimeter-wave frequency range.

List of Publications

International peer-reviewed journals

[OP1] I. Chlis, D. Pepe, and D. Zito, "Comparative analyses of phase noise in 28 nm CMOS LC oscillator circuit topologies: Hartley, Colpitts, and common-source cross-coupled differential pair," The Scientific World Journal, vol. 2014, article ID 421321, 13 pages, 2014.

[OP2] I. Chlis, D. Pepe, and D. Zito, "Analysis of Phase Noise in 28 nm CMOS LC Oscillator Differential Topologies: Armstrong, Colpitts, Hartley and Common-Source Cross-Coupled Pair," Journal of Circuits, Systems, and Computers, vol. 24, issue 4, pp. 1-18, 2015.

[OP3] I. Chlis, D. Pepe, and D. Zito, "Analyses and techniques for phase noise reduction in CMOS Colpitts oscillator topology," International Journal of Circuit Theory and Applications, John Wiley & Sons, 23 pages, 27 May 2015.

[OP4] I. Chlis, D. Pepe, and D. Zito, "Phase Noise Analysis in CMOS Differential Armstrong Oscillator Topology," International Journal of Circuit Theory and Applications, John Wiley & Sons, January 2016.

[OP5] D. Pepe, I. Chlis, and D. Zito, "67 GHz Three-Spiral Transformer CMOS Oscillator," International Journal of Circuit Theory and Applications, John Wiley & Sons, January 2016.

International peer-reviewed conferences

[OP6] I. Chlis, D. Pepe, and D. Zito, "Phase noise comparative analysis of LC oscillators in 28 nm CMOS through the impulse sensitivity function," in IEEE Proc. of the 9th Conf. on Ph.D. Research in Microelectronics and Electronics (PRIME '13), pp. 85-88, Villach, Austria, 2013.

[OP7] I. Chlis, D. Pepe, and D. Zito, "Comparative analyses of phase noise in differential oscillator topologies in 28 nm CMOS technology," IEEE Proc. of the 10th Conf. on Ph.D. Research in Microelectronics and Electronics (PRIME '14), pp. 1-4, 30 June-3 July, Grenoble, France, 2014.

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[OP9] I. Chlis, D. Pepe, and D. Zito, "Analyses of phase noise reduction techniques in CMOS Colpitts oscillator topology at the mm-waves: Inductive degeneration and optimum current density," IEEE Proc. of 26th Irish Signals & Systems Conference, Carlow, pp. 1-4, Ireland, 24-25 June 2015.

[OP10]I. Chlis, D. Pepe, and D. Zito, “Analyses of phase noise reduction techniques in CMOS Hartley oscillator topology at the mm-waves: Inductive degeneration and optimum current density,” IEEE Proc. of 26th Irish Signals & Systems Conference, Carlow, Ireland, pp. 1-4, 24-25 June 2015.

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[OP13]I. Chlis, D. Pepe, and D. Zito, “Analyses of phase noise in LC oscillator topologies,” 17th Wireless Research Colloquium, Dublin, Ireland, 2014.

Book Chapter

[OP14]I. Chlis, D. Pepe, and D. Zito, “Topological investigations and phase noise analyses in CMOS LC oscillator circuits,” in Mixed-Signal Circuits, chapter 6, CRC press, pp. 143-170, 2015.

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List of Symbols and Abbreviations

Transistor Width [μm]		
Abbreviation	Description	Definition
PN	phase noise	page iii
ISF	impulse sensitivity function	page iii
VCO	voltage-controlled oscillator	page iv
Q	quality factor	page iv
FOM	figure-of-merit	page iv
PSS	periodic steady state	page iv
Pnoise	periodic noise	page iv
LTI	linear time-invariant	page 1
Linear Time variant	linear time-variant	page 1
PSD	power spectral density	page 2
rms	root mean square	page 3
dc	direct current	page 41
LNA	low noise amplifier	page 54
PA	power amplifier	page 54
FDSOI	fully-depleted silicon-on-insulator	page107

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