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Microwave design of multi-layer interposers for the packaging of photonic integrated circuits

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113220311

Thesis submitted for the degree of
Doctor of Philosophy



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Declaration

I, Moises A. Jezzini, certify that this work is my own and has not been submitted for another degree, either at University College Cork or elsewhere. All external references and sources are clearly acknowledged and identified within the contents. I have read and understood the regulations of University College Cork concerning plagiarism.

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Moises A. Jezzini

Abstract

The increasing growth of data traffic on the Internet is supported by innovations in high-speed photonic devices. Some of this novel photonic devices are photonic integrated circuits (PICs) that use higher speeds, have higher circuit density and integrate more heterogeneous devices. A new generation of photonic packaging is also required to handle the increasing device density and data rate of the PICs. An important element to package the PICs is the carrier board which also serves as an interposer between the PIC and the package. The usual interposer material for PICs is a single-layer aluminium nitride (AlN) substrate due to its high thermal conductivity and good microwave performance. In contrast, other high-speed and high-density applications use multi-layer substrates as carrier boards. The typical multi-layer technologies for high-speed interposers is low-temperature co-fired ceramic (LTCC). The motivation of this research is the need of multi-layer interposers suitable for the packaging of high-speed and high-density PICs. A key element to enable this multi-layer interposer is the high-speed channels. The task of this research was the microwave design of these high-speed channels for a multi-layer interposer and carrier board suitable for PICs.

The main findings of this research can be divided into three areas. First, improvements to the microwave theory. A novel impedance profile reconstruction algorithm based on time-domain reflectometry (TDR) was developed. Additionally, a novel set of equations to calculate the characteristic impedance and the complex propagation constant from the vector network analyser (VNA) measurements of long lines was found and tested with positive results. Also, a novel single impedance thru-only de-embedding algorithm was completed. Second, the design of a novel rotatable vertical transition. The vertical transition has a 3 dB bandwidth around 35 GHz and small penalties on the eye diagram at 40 Gbit s^{-1}. Third, positive measured results of these designs in co-fired AlN. The measurements of the co-fired AlN board show similar results than in an LTCC board proving that co-fired AlN is an attractive option for PICs where the thermal management is important. The main conclusion from these findings is that the designed transmission lines and vertical transitions are suitable for the use of LTCC or of co-fired AlN as multi-layer interposers for the packaging of high-speed PICs Future work include improvements to the novel microwave algorithms, the development of equation-based models for the transmission lines. Also, the vertical transition has a resonance around 35 GHz that could be compensated using stubs or other elements. Finally, the transmission line designs and vertical transition designs need to be used for real applications of high-speed PICs using LTCC or co-fired AlN.

Software and instruments used in this thesis

Commercial software

- ANSYS HFSS for 3D full-wave simulations (2.5.2)
- ANSYS 2D Extractor for 2D waveguide simulations (2.5.1)
- ANSYS Circuit for simulating effect of frequency domain response in the eye diagram (2.5.3)
- MATLAB with the RF toolbox to plot the vector network analyser (VNA) results and for other transformations (2.3)
- WinCal (https://www.formfactor.com/) for the VNA short-open-load-thru (SOLT) calibration.
- PICDraw is used to create the layouts. PICDraw is a C++ software developed by Prof Frank H. Peters to draw and simulate photonic integrated circuits (PICs).

Open-source software

- R programming language (https://www.r-project.org/) using R-studio (https://www.rstudio.com/) and the packages: DoE.base, lhs and rsm (6.3.2).
- Vector fitting toolbox (https://www.sintef.no/projectweb/vectfit/)
- Inkscape (https://inkscape.org/)
- LaTeX (https://www.latex-project.org/)
- Vim (https://www.vim.org/)
- Gimp (https://www.gimp.org/)

Developed software

- Time-domain reflectometry (TDR) impedance profile reconstruction (A.1)
- Thru-only de-embedding algorithm (A.2.1)
- Characteristic impedance from long lines measurements (A.2.2)
- Importing layouts to ANSYS HFSS (A.3)
- PICDraw functions to draw high-speed lines in multi-layer technologies. The code is not provided in the thesis to reserve the code for future commercialization.

Measurement instruments

- Agilent digital communication analyser (DCA) DCA-J-86100C with modules 86118A abd 86107A
- Anritsu VNA 37397D
- Picoprobe calibration substrate CS-9
- Picoprobe probes 40A-GSG-150

Author's publications

[1] M. A. Jezzini, P. J. Marraccini, and F. H. Peters, "Design of a high-speed vertical transition in LTCC for interposers suitable for packaging photonic integrated circuits," in *SPIE Photonics Eur.*, L. Vivien, L. Pavesi, and S. Pelli, Eds., International Society for Optics and Photonics, May 2016, 98911R. DOI: 10.1117/12.2227628. URL: .

[2] P. J. Marraccini, M. A. Jezzini, and F. H. Peters, "Conductor backed and shielded multi-layer coplanar waveguide designs on LTCC for RF carrier boards for packaging PICs," in *SPIE Photonics Eur.*, L. Vivien, L. Pavesi, and S. Pelli, Eds., International Society for Optics and Photonics, May 2016, 98911Q. DOI: 10.1117/12.2225962. URL: .

[3] P. E. Morrissey, P. J. Marraccini, M. A. Jezzini, and F. H. Peters, "Shallow etch electrical isolation in capacitively loaded Mach-Zehnder modulators," in *SPIE Photonics Eur.*, F. Wyrowski, J. T. Sheridan, and Y. Meuret, Eds., International Society for Optics and Photonics, Apr. 2016, p. 988 903. DOI: 10.1117/12.2224583. URL: .

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[5] ——, "Multilevel transmission lines for photonics packaging," in *Photonics Irel.*, Cork, Ireland, 2015.

[6] Yanbo Li, Hua Yang, M. Jezzini, P. Morrissey, B. Corbett, N. Kelly, M. Sadiq, F. Peters, M. Crowley, P. Marraccini, and Lei Gao, "Phase matched transmission line design for high-speed optical modulators," in *25th IET Irish Signals Syst. Conf. 2014 2014 China-irel. Int. Conf. Inf. Communities Technol. (ISSC 2014/CIICT 2014)*, IET, Institution of Engineering and Technology, 2014, pp. 135–140. DOI: 10.1049/cp.2014.0673. URL: .

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Glossary and acronyms

The definitions in this section are taken from *Wikipedia*.

Acronyms

AlN aluminium nitride

BER bit error rate

CB-CPW conductor backed co-planar waveguide

CB-SL conductor backed slotline

CPW co-planar waveguide

CTE coefficient of thermal expansion

DCA digital communication analyser

DSP digital signal processing

DUT device under test

FWHM full width at half maximum

HSE high-speed electronics

HTCC high-temperature co-fired ceramic

IoT Internet of things

LCP liquid crystal polymer

LED light-emitting diode

LTCC low-temperature co-fired ceramic

NRZ non-return-to-zero

OTN optical transport network

PCB printed circuit board

PIC photonic integrated circuit

PM-QPSK polarization multiplexed quadrature phase-shift keying

PRBS pseudorandom binary sequence

PRBSG pseudorandom binary sequence generator

SiP system-in-a-package

SM-CPW shielded multi-layer co-planar waveguide

SOLT short-open-load-thru

TDR time-domain reflectometry

TEC thermoelectric cooling

VNA vector network analyser

Symbols

Z_0 characteristic impedance

$f_{3\,\mathrm{dB}}$ 3 dB bandwidth

ϵ_r relative permittivity

$\tan\delta$ loss tangent

Glossary

3 dB bandwidth ($f_{3\,\mathrm{dB}}$) The 3 dB bandwidth ($f_{3\,\mathrm{dB}}$) of an electronic filter or communication channel is the part of the system's frequency response that lies within 3 dB of the response at its peak, which in the passband filter case is typically at or near its centre frequency, and in the low-pass filter is near 0 Hz. If the maximum gain is 0 dB, the 3 dB bandwidth is the frequency range where the gain is more than −3 dB, or the attenuation is less than 3 dB. This is also the range of frequencies where the amplitude gain is above 70.7 % of the maximum amplitude gain, and the power gain is above half the maximum power gain.

BER power penalty The BER power penalty is the additional power needed at the input of a receiver to compensate for the introduction of a device under test (DUT) and maintain the same BER.

Bit error rate (BER) In digital transmission, the number of bit errors is the number of received bits of a data stream over a communication channel that have been altered due to noise, interference, distortion or bit synchronization errors. The bit error rate (BER) is the number of bit errors per unit time. The bit error ratio (also BER) is the number of bit errors divided by the total number of transferred bits during a studied time interval. Bit error ratio is a unit-less performance measure, often expressed as a percentage.

Carrier board A board in which the circuit module usually needs to be mounted. It usually contains the electrical connections to the peripheral interfaces.

Co-Planar Waveguide (CPW) Co-Planar Waveguide (CPW) has the return conductors on top of the substrate in the same plane as the main line, unlike stripline and microstrip where the return conductors are ground planes above or below the substrate. The return conductors are placed either side of the main line and made wide enough that they can be considered to extend to infinity.

Die-bonding Also referred to as eutectic-bonding, describes a wafer bonding technique with an intermediate metal layer.

Digital signal processing (DSP) Digital signal processing (DSP) is the use of digital processing, such as by computers, to perform a wide variety of signal processing operations. The signals processed in this manner are a sequence of numbers that represent samples of a continuous variable in a domain such as time, space, or frequency.

Eye diagram In telecommunication an eye diagram is an oscilloscope display in which a digital signal from a receiver is repetitively sampled and applied to the vertical input, while the data rate is used to trigger the horizontal sweep. It is so called because, for several types of coding, the pattern looks like a series of eyes between a pair of rails. It is a tool for the evaluation of the combined effects of channel noise and inter-symbol interference on the performance of a baseband pulse-transmission system. It is the synchronised superposition of all possible realisations of the signal of interest viewed within a particular signalling interval.

Flip-chip Describes a method for interconnecting semiconductor devices to external circuitry with solder bumps that have been deposited onto the chip pads. The solder bumps are deposited on the chip pads on the top side of the wafer during

the final wafer processing step. In order to mount the chip to external circuitry, it is flipped over so that its top side faces down, and aligned so that its pads align with matching pads on the external circuit, and then the solder is re-flowed to complete the interconnect. This is in contrast to wire bonding, in which the component is upright.

III-V semiconductor compound A III-V compound semiconductor is composed of elements of of elements from group III (i.e. boron, aluminium, gallium, indium) and from group V (nitrogen, phosphorus, arsenic, antimony, bismuth). The most common compositions are InP and GaAs. These two groups have direct band-gap making it useful for optoelectronics devices like laser diodes.

Internet of things (IoT) Internet of things (IoT) is the inter-networking of physical devices, vehicles, buildings, and other items embedded with electronics, software, sensors, actuators, and network connectivity which enable these objects to collect and exchange data.

Interposer An electrical interface between modules. The purpose of an interposer is to spread a connection to a wider pitch or to reroute a connection to a different connection. Interposer comes from the Latin word *interponere* meaning: to put up between.

Light-Emitting Diode (LED) A light-emitting diode (LED) is a two-lead semiconductor light source. It is a p-n junction diode that emits light when activated.

Loss tangent ($\tan\delta$) The loss tangent ($\tan\delta$) is defined as the ratio (or angle in a complex plane) of the lossy reaction to the electric field in the Maxwell's curl equation to the lossless reaction, more details provides in Chapter 2. It turns out that the power decays with propagation distance $z \propto \exp(-\delta k z)$ where k is the angular wavenumber.

Microstrip Microstrip consists of a strip conductor on the top surface of a dielectric layer and a ground plane on the bottom surface of the dielectric. Microstrip is often favoured for its easy compatibility with printed circuits.

Non-return-to-zero (NRZ) In telecommunication, a non-return-to-zero (NRZ) line code is a binary code in which ones are represented by one significant condition, usually a positive voltage, while zeros are represented by some other significant condition, usually a negative voltage, with no other neutral or rest condition.

Optical transport network (OTN) Optical transport network (OTN) as a set of elements connected by optical fibre links, able to provide functionality of transport, multiplexing, switching, management, supervision and survivability of optical channels carrying client signals.

Profilometer Profilometer is a measuring instrument used to measure a surface's profile, in order to quantify its roughness. Critical dimensions as step, curvature, flatness are computed from the surface topography.

Pseudorandom binary sequence (PRBS) A pseudorandom binary sequence (PRBS) is a binary sequence that, while generated with a deterministic algorithm, is difficult to predict and exhibits statistical behaviour similar to a truly random sequence. PRBS are used in telecommunication, encryption, simulation, correlation technique and time of flight spectroscopy.

Relative permittivity (ϵ_r) The relative permittivity of a material (ϵ_r) is its absolute permittivity expressed as a ratio relative to the permittivity of vacuum. Permittivity is a material property that affects the Coulomb force between two point charges in the material. Relative permittivity is the factor by which the electric field between the charges is decreased relative to vacuum.

Scattering parameters (S-parameters) Scattering parameters (S-parameters) describe the electrical behaviour of linear electrical networks when undergoing steady state stimuli of various frequencies by electrical signals.

Slotline A slotline is a slot cut in the metallisation on top of the substrate. It is the dual of stripline, a dielectric line surrounded by conductor instead of a conducting line surrounded by dielectric.

Stripline Stripline is a strip conductor embedded in a dielectric between two ground planes. It is usually constructed as two sheets of dielectric clamped together with the stripline pattern on one side of one sheet.

Thermoelectric cooler (TEC) Thermoelectric cooler (TEC) uses the Peltier effect to create a heat flux between the junction of two different types of materials. A Peltier cooler, heater, or thermoelectric heat pump is a solid-state active heat pump which transfers heat from one side of the device to the other, with consumption of electrical energy, depending on the direction of the current. It can be used as a temperature controller that either heats or cools.

Time-domain reflectometry (TDR) Time-domain reflectometry or TDR is a measurement technique used to determine the characteristics of electrical lines by observing reflected waveforms.

Wire-bonding Describes a method of making electrical interconnections between electronic components using gold wire in microwave applications, although aluminium or copper wires are also possible. The electrical component has to be mounted upright in order to place the wires.

Young's modulus Young's modulus, also known as the elastic modulus, is a measure of the stiffness of a solid material. It is a mechanical property of linear elastic solid materials. It defines the relationship between stress (force per unit area) and strain (proportional deformation) in a material.

Acknowledgements

I will always be grateful to Prof Frank H. Peters for supervising the work presented in this thesis. The best thing that I get from my PhD studies was having him as a model, both professionally and as a person.

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Para Magaly, Matías y Malena, ustedes también han puesto mucho esfuerzo en esta tesis que es una prueba más de que nos especializamos en lo difícil.

Para mis padres y mis hermanos, gracias por todo su amor.

However absurd it may seem, I do in all seriousness hereby declare that I am animated mainly by philanthropic motives.

Oliver Heaviside
Electrical Papers (1882), Vol. I;

Chapter 1
Introduction

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1.1 Context: The packaging of high-speed Photonic Integrated Circuits

1.1.1 The Internet traffic growth forecast

The Internet is very useful for our societies and has been growing since its creation. The Internet traffic forecast predicts a continued strong growth into the future. This

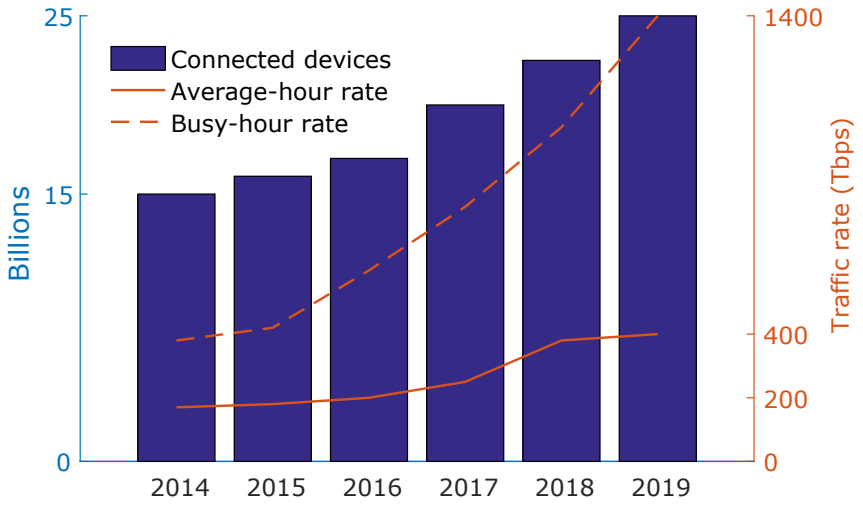


Figure 1.1: The Internet traffic is projected to keep growing. Both the number of connected devices and the traffic rates have strong growth. Data taken from [1].

section presents a short discussion on the impact of the Internet in our societies, summarises the latest Internet growth forecast and discusses the evolution of the technologies that support the Internet.

The Internet is so beneficial for societies that there are proposals to make it a human right, see for details [2]–[5].

In [1], the Internet is projected to keep growing both in traffic rate and in the number of connected devices. The Internet annual global traffic reached 1 ZB per year in 2016 (1 ZB is 10×10^{21} B), starting what has been called the zettabyte era, and it is projected to be 2 ZB per year by 2019. That is high growth, five times in the past five years, and a projection of a threefold growth over the next five years. The busy-hour traffic rate is growing even faster than the average-hour rate, see Figure 1.1. The number of connected devices will be around 25 billion by 2019, that is more than three times the global population. There are several trends that could sustain the Internet traffic growth. One of these trends is the Internet of things (IoT), which is the term that describes machines that are connected to the Internet and that communicate to other machines (e.g. a sensor connected to a computer). The IoT trend means that more devices will be connected to the Internet. Another trend is that people are watching more and more videos through the Internet and the definition or resolution of these videos is getting higher, requiring more bandwidth. Another trend is that home connection speeds are increasing and when the connection speed in a home increases the number of minutes watched per viewer also increases. Overall, many conditions to sustain the Internet traffic growth exist.

In [1], the broadband speed has been projected to more than double by 2019 so the supporting technologies need to evolve accordingly. For example, the *Ethernet Alliance*

recently introduced the new standard for 400 Gbit s^{-1} in [6]. This new standard and any other standard above 40 Gbit s^{-1} are supported only by optical fibre since the metal cable solutions have too much loss. This increase in the data traffic has created the necessity to escalate tenfold the optical transport network (OTN) from 2010 to 2020, see [7]. The network traffic is growing faster than the system capability, so new technologies are needed to satisfy the demand. Thus, there is a need for research, as presented in this document, to create these new technologies.

In summary, the Internet is very beneficial for our societies and has been growing since its creation. The Internet traffic forecasts show strong growth in the next years. Thus, the components that support the Internet need to evolve. Some of these components are the photonic integrated circuits (PICs) that are discussed in the next section.

1.1.2 The history of the Photonic Integrated Circuits

The Internet traffic growth, summarised in the previous section, has motivated an evolution of its components. That is certainly the case for the photonic devices. The reader needs to understand the characteristics of the current photonic devices to appreciate the motivation of this research and this section describes the characteristics of the newest photonic devices by summarising their history. The photonic devices have evolved from the simple visible light-emitting diode (LED) to large-scale PICs. These large-scale PICs have high circuit-density, high channel-speeds, and use hybrid integration to fully package the PICs.

In the last 55 years, the photonic devices have evolved from the simple LED to complex devices that integrate hundreds of functions. A good account of this evolution can be found in [8]: the first visible-light LED was demonstrated in 1962. This demonstration was important because it showed the viability of using III-V semiconductor compounds, which have direct bandgaps that can be adjusted through material design. This property of III-V semiconductor compounds makes them useful to create photonic devices that generate, amplify, modulate or detect light. Today (2018), PICs include hundreds of photonic devices per chip and thus integrate many of the required functions for the most sophisticated optical transmitters and receivers. For example, 500 Gbit s^{-1} transmitters and receivers have been developed by the integration concept as showed in [8]. The transmitter integrates over 440 functions per device and the receiver over 150 functions per device.

Currently, PICs use higher than ever circuit-density and interface-rate; and integrate more heterogeneous devices. The circuit-density (i.e. the number of components per chip) has been increasing exponentially from a single device in 1987 to hundreds of devices in 2015; see Figure 1.2 plotted with data from [9]. Similarly, the interface-rate has grown from 100 Mbit s^{-1} in 1994 to 100 Gbit s^{-1} in 2015; see Figure 1.2 plotted with data from [10]. In [11], the rates have been projected to reach 1 Tbit s^{-1} in 2020. PICs are not only made of III-V semiconductor compounds, silicon is also a promising material for high sales-volume and integration with electronics, as discussed in [12]–[15]. So even when the III-V semiconductor compound PICs are able to integrate more

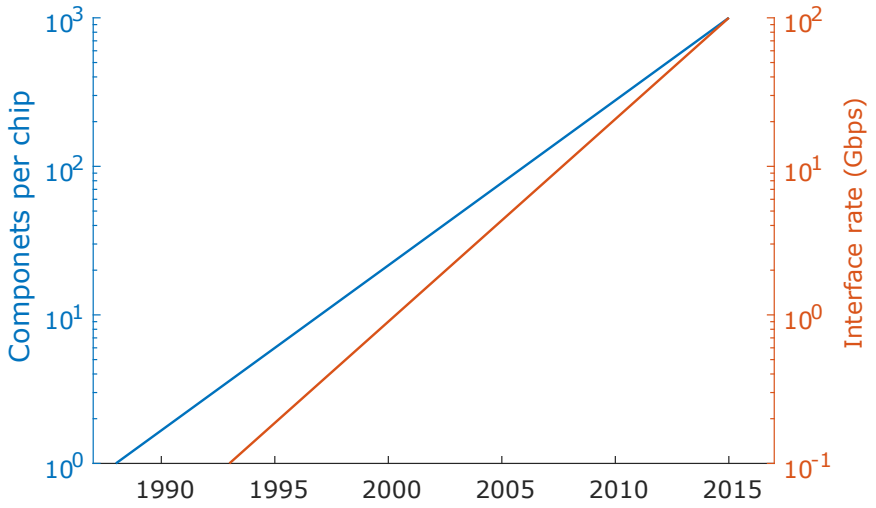


Figure 1.2: The circuit-density and interface speeds are increasing in PICs. Data from [9], [10].

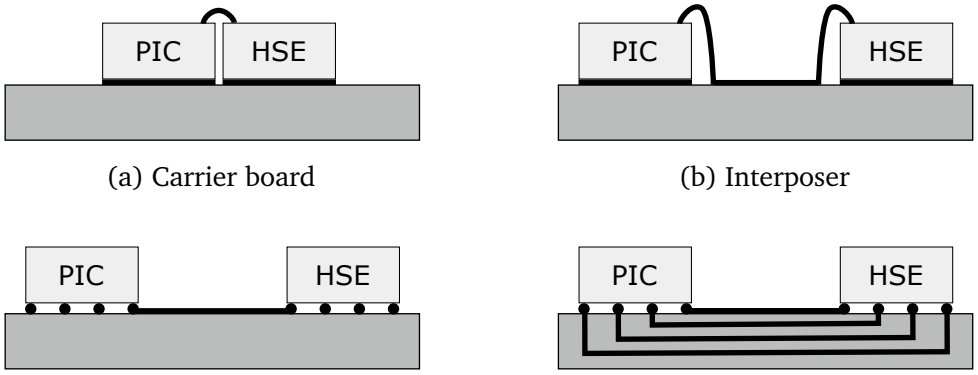
and more devices monolithically, they still need to integrate with other platforms like silicon photonics, high-speed electronics, thermal management devices, digital signal processors and optical elements. Some examples of the hybrid integration can be found in [16]–[23]. One field where the need for hybrid integration is clear is microwave photonics; for examples see [24]–[26]. The hybrid integration occurs while the devices are being packaged and assembled and is a necessary step in the manufacture of PICs.

The latest photonic devices are large-scale PICs that use higher circuit-density, higher channel-speeds and integrate the most heterogeneous devices. These PICs need specialised packaging. To understand the available packaging options, the state of the art for high-speed packaging is discussed in the next section.

1.1.3 The state of the art for high-speed packaging

The evolution of PICs creates the need for an evolution of their packaging, including the high-speed part. The reader needs to be familiar with the state of the art of the current high-speed packaging technologies to understand the motivation of this research. This section discusses some recent examples of high-speed packages used with both photonic devices and microwave devices, and argues that the use of flip-chip and a multi-layer interposer is a better option than using die-bonding, wire-bonding and a single-layer interposer.

Several recent examples, from 2016 to 2017, of a high-speed packaging methodology have been found in the literature and are discussed next. In [27], a packaging that operates at 56 Gbit s^{-1} based on wire-bonding, more specifically ribbon bonds, and die-bonding is presented. The package uses short wire-bonds and a board in-



(a) Carrier board (b) Interposer

(c) Interposer (d) Multi-layer interposer

Figure 1.3: Illustration of some common packaging scenarios to integrate a PIC to a high-speed electronics (HSE) device. The use of a multi-layer interposer facilitates the connections and maintains the signal integrity.

terposer to route the signal. In [28], an antenna working at 60 GHz is made on a printed circuit board (PCB) and connected by wire-bonds. The wire-bonds need compensating structures to provide the required performance. In [29], the packaging of a 36 Gbit s^{-1} transmitter is based on a combination of flip-chip and wire-bonds and uses a high-speed interposer. In [30], [31], flip-chip bonding is used to create low-cost assemblies operating at speeds from 300 GHz to 500 GHz. In [32], the high-speed electronics and the photonic devices are placed together using die-bonding and connected by wire-bonding, a board with thermal vias is used, and the devices operate at 25 Gbit s^{-1}. In [14], multiple examples of packaging are discussed using combinations of die-bonding, wire-bonding and flip-chip. In [33], five active chips including a mixer, driver amplifier, power amplifier, two frequency multipliers, and passive circuits such as filters and antennas were integrated using a low-temperature co-fired ceramic (LTCC) package substrate working at 60 GHz. In [34], a PIC is integrated to the corresponding electronics by using die-bonding and wire-bonding working at 28 Gbit s^{-1}. In [23], a package substrate is used to integrate a digital signal processing (DSP) unit, high-speed electronics and a PIC by using flip-chip with data rates as high as 25 Gbit s^{-1}. In [35], a multi-layer interposer is used to package a 100 Gbit s^{-1} transmitter by flip-chip, based on four 25 Gbit s^{-1} channels and achieving a very small and energy efficient module. In [15], flip-chip is used to integrate a PIC with high-speed electronics and a DSP unit. Multiple channels at 25 Gbit s^{-1} are used to generate a total of 1 Tbit s^{-1}. The conclusion from these examples is that there are three main processes used for the packaging of high-speed devices: Die-bonding, wire-bonding and flip-chip.

Using die-bonding and wire-bonding in a single-layer interposer is the standard practice for high-speed packaging, but using flip-chip in a multi-layer interposer is being adopted. Figure 1.3 illustrates some common scenarios for these practices. Figure 1.3a shows a concept using a carrier board to mount a PIC and a HSE device, by

die-bonding, where the connection between them is done by wire-bonding. The PIC and the HSE are placed close together to minimize the length of the wires, but there might be reasons to separate them, such as avoiding thermal crosstalk and giving space for other components. If the PIC and the HSE are separated, an interposer is used as shown in Figure 1.3b where die-bonding and wire-bonding are used on a single-layer interposer. The components are connected to the metal traces on the top of the interposer. Those metal traces route the signals between the PIC and the HSE. In this case, as in the previous one, the high-speed signals are routed from the perimeter of the components to shorten the wires. Instead of die-bonding and wire-bonding, flip-chip can be used together with an interposer, as illustrated in Figure 1.3c. By using flip-chip, the connection between the components and the interposer is minimised, thus improving the microwave performance. The benefits of flip-chip are better harnessed by using a multi-layer interposer as illustrated in Figure 1.3d. The use of the multi-layer interposer facilitates the routing of the signals by adding more space and facilitating the crossing of channels. This concept of integrating heterogeneous components along with passive components using multi-layer technologies (sometimes referred as 3-D packaging technologies) is called system-in-a-package (SiP), see for reference [19], [33], [36]–[39]. The SiP concept provides a package with optimized cost, size and performance.

Thus, high-speed packaging uses several approaches but its future is probably in SiP using mostly flip-chip. There are several multi-layer packaging technologies available to support the SiP concept; the next section discusses those multi-layer technologies in detail.

1.1.4 The state of the art for multi-layer technologies

Several multi-layer technologies are available to support the SiP concept: PCB, co-fired ceramics (i.e. LTCC and high-temperature co-fired ceramic (HTCC)), liquid crystal polymer (LCP), silicon and glass. This section summarises the state of the art for these multi-layer technologies. The selection of the technology is a trade-off between three different characteristics: electrical, thermal and mechanical. Therefore, Figure 1.4, Figure 1.5 and Figure 1.6 present the most important characteristics of the most common materials used in these multi-layer technologies ([39]–[42]).

PCB is very mature and thus inexpensive but it has the worst electrical performance of the multi-layer technologies. Therefore, PCB is a good option when the electrical performance is not critical. The most common material for PCB is FR4 which has a low relative permittivity (ϵ_r) and a high loss tangent ($\tan\delta$) (Figure 1.4). The low ϵ_r means that the metal widths need to be large or the substrate thickness small. The high $\tan\delta$ means that the lines will be lossy. There are some new substrates for PCB that are much better electrically but more expensive than FR4 and thus not as competitive as other multi-layer technologies. Thermally, FR4 has a high coefficient of thermal expansion (CTE) and a low thermal conductivity (Figure 1.5). The high CTE means that it is incompatible with gold, so copper is used for the metal traces. But copper has an undesired CTE mismatch with III-V semiconductor compounds,

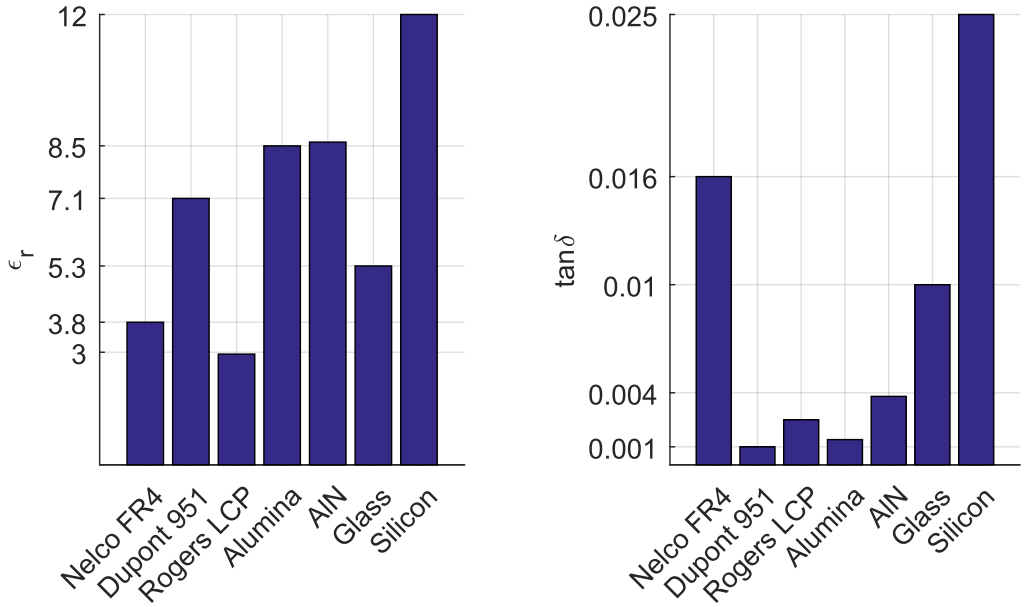


Figure 1.4: Electrical properties of the most common materials of each multi-layer technology at 10 GHz. LTCC material Dupont 951 and HTCC material Alumina excel in their electrical properties [39]–[42].

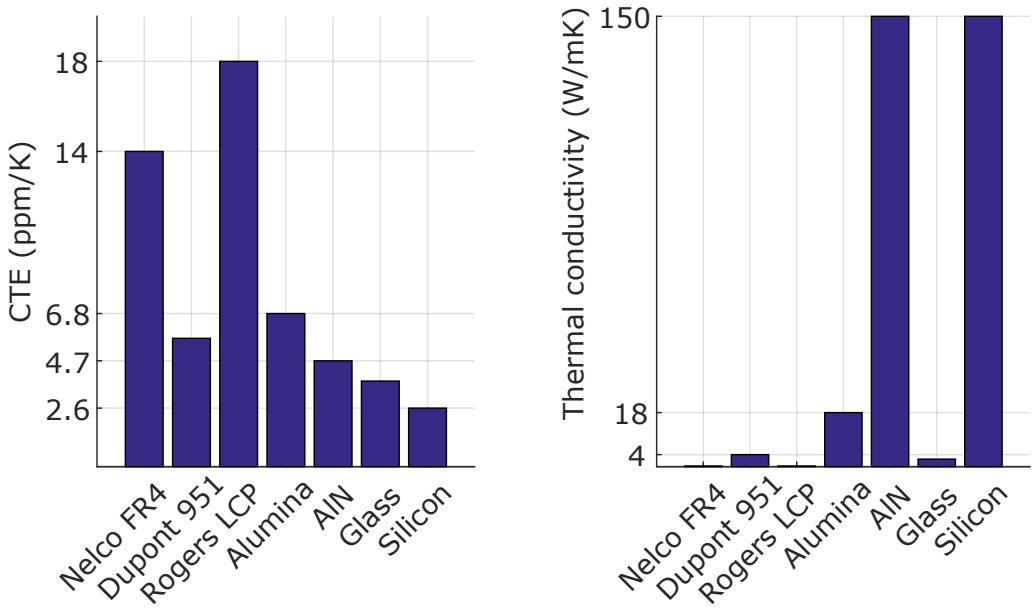


Figure 1.5: Thermal properties of the most common materials of each multi-layer technology. Aluminium nitride (AlN) and silicon excel in their thermal properties [39]–[42].

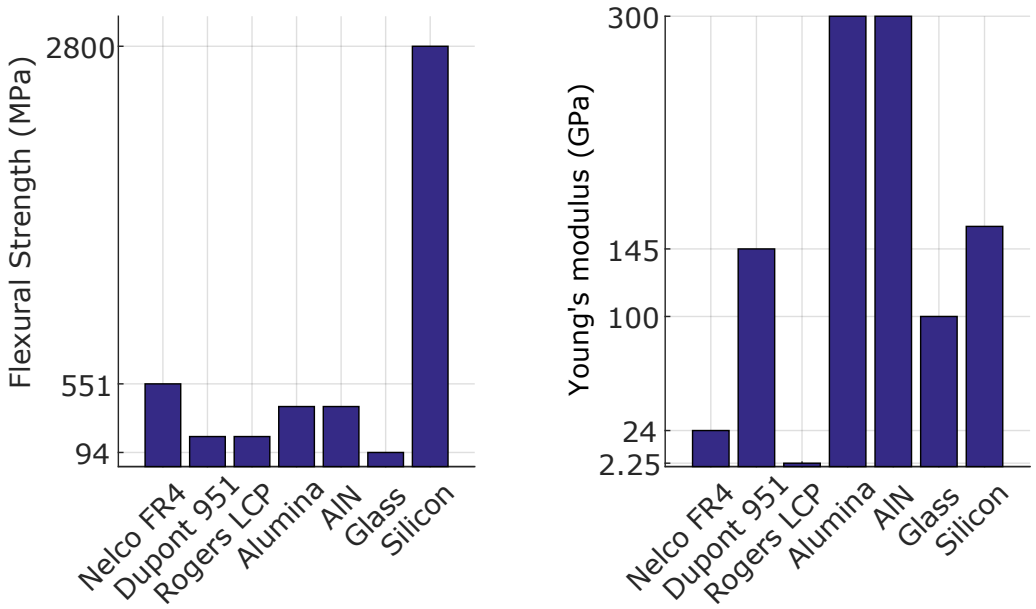


Figure 1.6: Mechanical properties of the most common materials of each multi-layer technology. PCB material Nelco FR4 and LCP from Rogers are too flexible to be used as carrier boards [39]–[42].

which is a potential mechanical problem. Also, the low thermal conductivity of FR4 forces the use of metal vias to remove heat from the system. Mechanically, FR4 has a relatively low Young's modulus (see Figure 1.6), so thick substrates are needed to get rigid boards as needed for a carrier board.

LCP has excellent electrical performance (Figure 1.4) but is too flexible (Figure 1.6). For example, Rogers LCP material has the lowest $\tan\delta$, which means low losses, but it also has the lowest ϵ_r which means that the substrate thickness must be very small to get small metal traces and that it will be difficult to design passive circuits on it. Thermally, LCP has a high CTE and a low thermal conductivity (Figure 1.5). The high CTE means that LCP is not compatible with gold so copper must be used and therefore there will be additional mechanical stresses when coupled with III-V semiconductor compounds. The low thermal conductivity creates the necessity for metal traces to manage the heat. LCP is the most flexible of the materials (i.e. has the lowest Young's modulus) (Figure 1.6). LCP flexibility makes it suitable for flexible connections but not as a carrier board.

Silicon and glass are being developed but are not yet widely available commercially. The main advantage of silicon and glass is the ease of integration with PICs. Electrically, silicon is very lossy (i.e. has high $\tan\delta$) but, that is compensated by the high ϵ_r which allows for miniaturisation; glass has a medium $\tan\delta$ and ϵ_r (Figure 1.4). Thermally, both have low CTE making them the best for mounting integrated circuits. Glass has very low thermal conductivity and in contrast, silicon has very high thermal conductivity (Figure 1.5). Mechanically, both have low flexibility but glass is brittle,

that is, it has a low flexural strength (Figure 1.6). Silicon and glass are the least mature options.

The co-fired ceramics, LTCC and HTCC, are the most used multi-layer technologies. The most common substrate for LTCC is Dupont 951 and for HTCC is Alumina. Electrically, both materials have high ϵ_r and low $\tan\delta$ (Figure 1.4) which are ideal. Thermally, both have medium CTE (Figure 1.5) which means that both are compatible with gold. The thermal conductivity is also low which means that additional metal traces are required to drain the heat. Mechanically, both are somewhat brittle but rigid enough to be used as carrier boards (Figure 1.6). Both technologies have been extensively used for high-speed packaging.

AlN has a high thermal conductivity and good electrical performance so it is widely used as a single-layer substrate but it is not widely available as multi-layer. Electrically, AlN has a high ϵ_r and a low $\tan\delta$ (Figure 1.4). The electrical performance of AlN is similar to the performance of the substrate Dupont 951 for LTCC. Thermally, AlN has a good CTE and a high thermal conductivity (Figure 1.5). The CTE allows for the integration with gold and III-V semiconductor compounds and the high thermal conductivity is very useful when heat must be removed from the circuit which usually the case for PICs. Mechanically, AlN is strong and rigid (see Figure 1.6), making it a good option for carrier boards. AlN is also offered as an HTCC material but is not as widely available as Alumina.

In summary, the selection of the multi-layer technology requires analysing the trade-off between several characteristics. In this research, I decided to use LTCC and co-fired AlN. LTCC is chosen because it is a mature option with proven performance in high-speed applications including photonic applications. Co-fired AlN is chosen because of the important advantage of high thermal conductivity.

1.1.5 The state of the art for microwave design

The design of high-speed packaging (Section 1.1.3) is performed using microwave engineering theory. This section summarises, in general, the state of the art of the design of microwave devices. This summary provides the context to understand the motivation outlined in Section 1.2 and the objectives in Section 1.3. Chapter 2 is dedicated to explaining the specific research methodology based on the microwave engineering theory.

The term microwave refers to alternating signals with frequencies between 3 GHz and 300 GHz, and thus the wavelength of the signal at these frequencies is similar to the dimensions of the circuits (Figure 1.7 from [43]). Therefore, circuit theory can not be used directly; instead the electromagnetic theory, as described by Maxwell's equations, is required. The goal of the microwave design is to reduce the results of the electromagnetic theory into the more practical terms of the standard circuit theory.

The electromagnetic theory is often used through electromagnetic simulators, and a good discussion about the state of these simulators can be found in [44]. The electromagnetic simulators can be categorised into three types: 2D cross-sectional solvers,

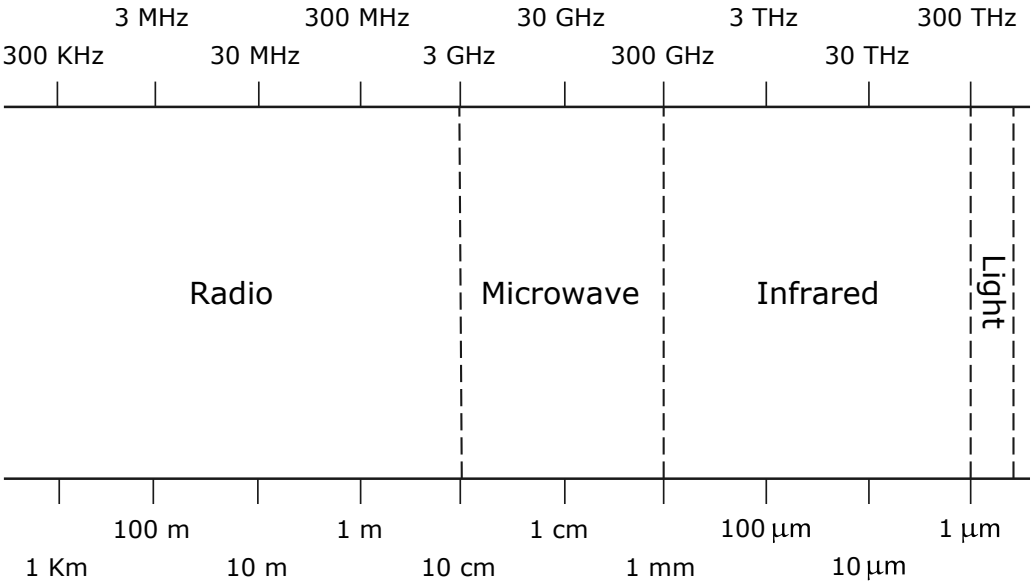


Figure 1.7: Frequency (top) and wavelength (bottom) in free space for different regimes of electromagnetic waves. In the microwave regime, the wavelength is similar to the dimensions of the device [43].

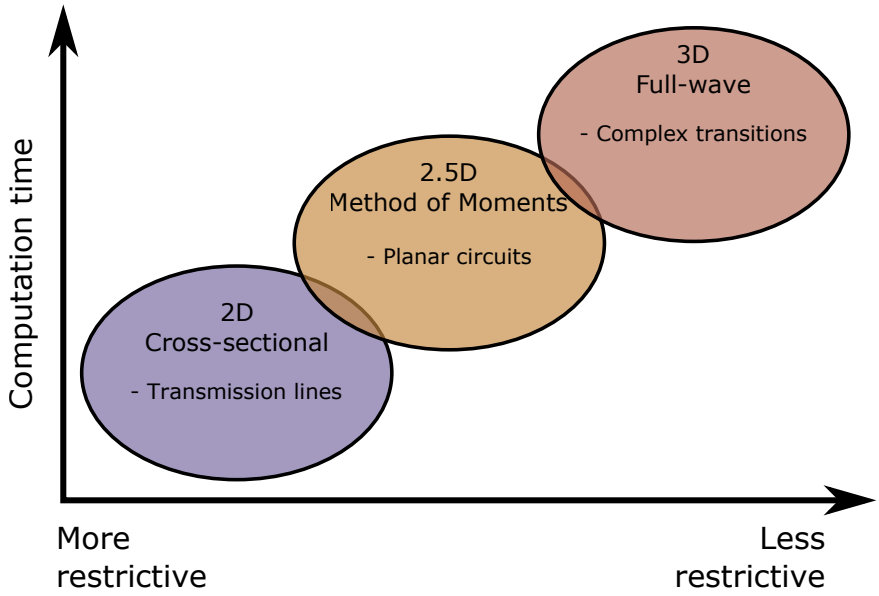


Figure 1.8: The main categories of electromagnetic solvers. The type must be chosen for the application [44].

2.5D Method of Moments (MoM) solvers, and 3D full-wave solvers (Figure 1.8). The 2D cross-sectional solvers find the charge and current per unit length. The resulting solution is then used to calculate the resistance, inductance, capacitance, and conductance per unit length. These type of simulations have the shortest computation times but are also the most restrictive, since this type of simulation can be only used to design transmission lines. The 2.5D solvers, based on the Method of Moments are numerical computational methods of solving the integral Maxwell's equations. These calculations only require the boundary values, rather than values throughout the volume, and thus they need less computation time than the full-wave solvers for problems with a small surface to volume ratio. However, many problems have a large surface to volume ratio, and the 2.5D solvers use more memory and have longer computational times than the 3D full-wave solvers. The 3D full-wave simulators are the least restrictive, since they can solve for arbitrary 3D geometries by solving Maxwell's equations completely, but they also use the most computation time and memory. The electromagnetic simulation results are usually embedded in the circuit simulator to simulate the system behaviour. But the microwave design is not only based on simulations. Once the simulations are performed to design a microwave device, the fabricated device must be characterised.

Vector network analysers (VNAs) and digital communication analysers (DCAs) are two of the most useful instruments used to characterise the microwave performance of a device. The VNA is capable of creating an incident signal at different frequencies and then measuring the reflected and transmitted signals. Then it calculates the ratio of the reflected wave to the incident wave and the ratio of the transmitted wave to the incident wave. These ratios are complex numbers since they contain information about the phase of the signals. These ratios are the scattering parameters (S-parameters) which contain information of the measured system such as the gain and the return loss. The DCA is a sampling oscilloscope with advanced trigger and pattern locking capabilities. It allows the measurement of the eye diagrams, which gets its name from its shape (Figure 2.20). The eye diagrams are a synchronised superposition of all possible three bit combinations. The eye diagrams provide a visual way to judge the quality of the signal; easily showing if the signal is too low compared to the noise or any timing synchronisation problems or jitter problems. More details about the eye diagram are presented in Chapter 2.

Section 1.1.5 only provides some context needed for the rest of this chapter, but more detail of the microwave theory and tools used in this research is given in Chapter 2.

Section 1.1 argues that the Internet traffic will continue growing strongly. To meet this growth, the photonic devices have evolved from single lasers to complex PICs that integrate hundreds of devices and work faster than ever. The packaging of the PICs is moving towards the SiP concept, preferring flip-chip over die-bonding with wire-bonding. The SiP requires multi-layer technologies from which LTCC is the most used and co-fired AlN has been identified as a promising technology due to its higher thermal conductivity. The SiP concept needs multi-layer interposers as discussed in

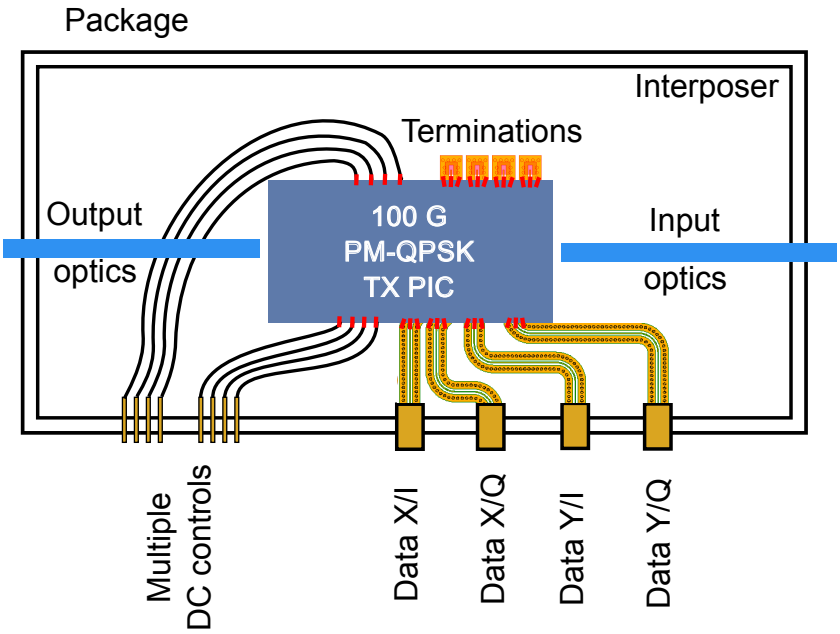
Section 1.2. The microwave design of the elements of a multi-layer interposer is done using electromagnetic simulations and their characterisation through microwave measurements. The objectives of this research, as explained in Section 1.3, are to use these electromagnetic simulations and microwave measurements to design and characterise high-speed multi-layer interposers for both LTCC and co-fired AlN.

1.2 Motivation: The need for multi-layer interposers for the packaging of high-speed PICs

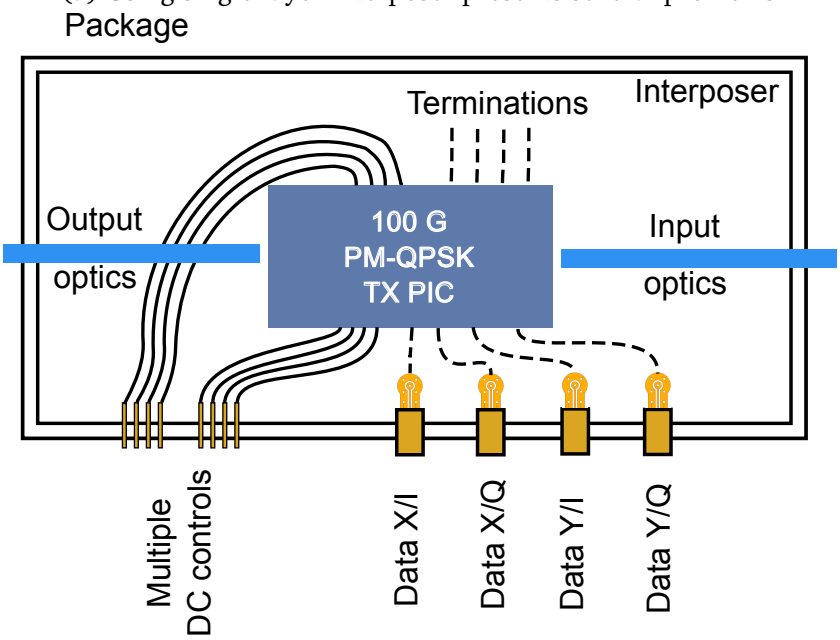
In this section, I argue that multi-layer high-speed interposers are needed to provide more space, better microwave performance, more flexible thermal management and less expensive manufacturability. The new generation of high-speed PICs integrates more and faster devices, as was discussed in Section 1.1.2. One example of this new generation of PICs is the 100 Gbit s^{-1} polarization multiplexed quadrature phase-shift keying (PM-QPSK) transmitter; this transmitter is a good example because there is a public implementation agreement [45] about its packaging. Inspired loosely on this public agreement, a packaging concept using a single-layer high-speed interposer is compared to another using multi-layer interposers in Figure 1.9. The concept is based on a single-layer interposer, where wire-bonding and die-bonding is required to implement the packaging concept as discussed in Section 1.1.3 and shown in Figure 1.9a. In contrast, the newer concept using multi-layer interposers is shown in Figure 1.9b. The 100 Gbit s^{-1} PM-QPSK transmitter example shows the problems of the single-layer interposers and demonstrates the importance of using multi-layer interposers thus clarifying the importance of this research. Section 1.2.1 argues that the microwave performance of using a multi-layer interposer coupled with flip-chip bonding to route the channels is better than the performance of using single-layer interposers with wire-bonding. Section 1.2.2 discusses how the single-layer interposers restrict the space and how multi-layer interposers could remove this restriction. Section 1.2.3 argues that the single-layer carrier boards restrict the thermal management and that multi-layer carrier boards provide more flexibility. Section 1.2.4 finishes Section 1.2 arguing that multi-layer interposers decrease the cost of manufacture for high density PIC applications.

1.2.1 The need for microwave performance

As discussed in Section 1.1.2, the PICs typical channel speed is increasing as is the circuit density. Therefore, the packaging of these PICs requires excellent microwave performance; that is a high 3 dB bandwidth ($f_{3\,\mathrm{dB}}$) and low crosstalk. This section argues that flip-chip provides better microwave performance than wire-bonding, and that multi-layer interposers decrease crosstalk between channels.



(a) Using single-layer interposer presents several problems



(b) Using multi-layer interposer has several advantages over a single-layer inteposer

Figure 1.9: A high-speed PIC packaging concept based on a single-layer interposer (Figure 1.9a) is compared to another based on a multi-layer interposer (Figure 1.9b). The single-layer interposer restricts the space; degrades the microwave and thermal performances, and complicates the manufacture. The use of multi-layer interposer alleviates these problems.

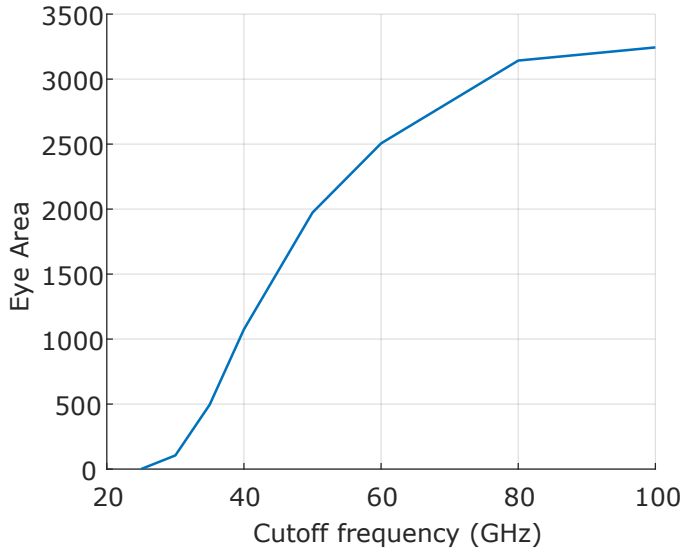


Figure 1.10: Eye area versus the $f_{3\,\mathrm{dB}}$ of a filter. The signal quality, measured by the eye area (i.e. eye height times eye width), decreases with the $f_{3\,\mathrm{dB}}$ of a fourth-order low-pass Chebyshev filter for a 100 Gbit s^{-1} non-return-to-zero (NRZ) signal. Calculation from theory in Section 2.5.3.

The packaging of high-speed PICs requires excellent microwave performance. One way to measure this microwave performance of a transmission system is by measuring the frequency response ($f_{3\,\mathrm{dB}}$) which must be as high as possible to maintain the signal integrity. The signal integrity can be visualised using the eye diagram; the more open an eye diagram, the better signal integrity it has. The openness of an eye diagram can be quantified by the eye area, that is the eye height times the eye width (more details in Chapter 2). The eye area of a 40 Gbit s^{-1} NRZ signal passing through a low-pass first-order filter is plotted against the filter's $f_{3\,\mathrm{dB}}$ in Figure 1.10. That figure shows that the eye area reduces if the $f_{3\,\mathrm{dB}}$ is not high enough. This reduction is not exclusive to the low-pass first-order filter but there is a general need for higher $f_{3\,\mathrm{dB}}$ of all the components of a high-speed system.

Flip-chip provides better microwave performance than wire-bonding. The reasons for the better microwave performance is that flip-chip creates a shorter discontinuity since the usual solder ball is only 50 µm diameter; in contrast, the typical wire length is several times longer. Comparisons between flip-chip and wire-bonding can be found in [30], [31], [46]–[50]. Flip-chip has been successfully used with signals in the millimetre-wave regime. The wire-bonds can give a comparable microwave performance to flip-chip if compensating structures are used [51], but these compensating structures use additional space and are difficult to design. The better performance of flip-chip over wire-bonding is one of the reasons why the concept in Figure 1.9b is an improvement over the concept in Figure 1.9a. The other reason is crosstalk.

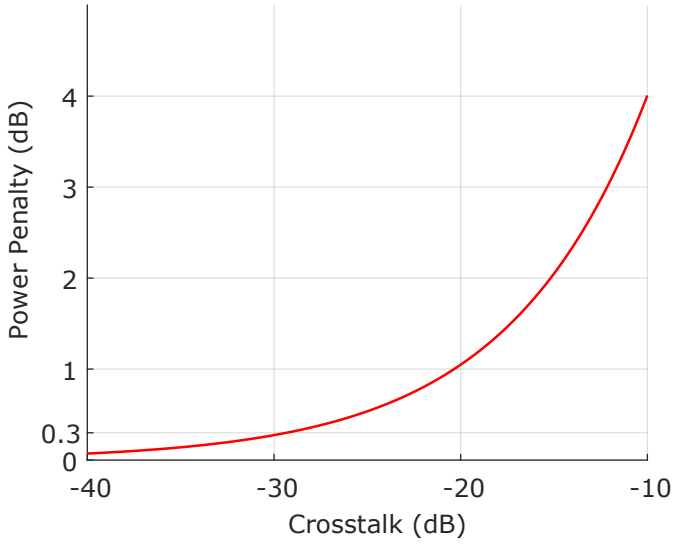


Figure 1.11: The signal quality, quantified by the power penalty, decreases with the crosstalk so the objective is to have crosstalk below −30 dB. Data from [52].

The multi-layer interposers decrease the crosstalk between channels as we will show in Chapter 3. Decreasing the crosstalk is important to maintain the signal integrity. For example, in [52] the effect of the crosstalk in the bit error rate (BER) is analysed showing that the BER power penalty has an exponential relation to the crosstalk (Figure 1.11). The BER power penalty is below 0.3 dB for crosstalk below −30 dB which is considered in this research as acceptable performance.

Multi-layer interposers not only improve microwave performance and reduce crosstalk but are also more space efficient, as discussed in the next section.

1.2.2 The need for space

The PICs circuit density is increasing, as discussed in Section 1.1.2. This increase in circuit density constrains the available space in the packaging since each circuit requires multiple electrical connections. This section argues that the multi-layer interposer adds space that can be used to route the signals and to integrate more devices, and is therefore more space efficient.

The multi-layer interposer simplifies the routing of the signals, as for example, the 100 Gbit s^{-1} PM-QPSK transmitter shown in Figure 1.9. The single-layer interposers using die-bonding and wire-bonding (Figure 1.9a) force the position of the high-speed connections between the devices and the interposer to the perimeter of the device, since wires must be short to ensure sufficient microwave performance (Section 1.2.1). The use of flip-chip instead of die-bonding plus wire-bonding on a single-layer interposer enables the electrical connections between the devices and

the interposer to be positioned at any location on the surface of the devices as the routing of the signals to the perimeter of the device can be done within the multi-layer interposer. In the case of the single layer interposer, the high-speed channel crossing is done by wire-bonding, however, the introduction of wires decreases the performance. By using a multi-layer interposer and flip-chip (Figure 1.9b) the routing is not constrained to the perimeter of the devices since the crossing of channels is done easily by routing in multiple layers. A good example of this approach can be found in [35].

The multi-layer interposer adds space not only for routing the signals but also for hybrid integration and the use of passive circuits. As discussed in Section 1.1.2, the PICs are used in packages that integrate circuits based on different technologies. The SiP uses the multi-layer technologies to do the hybrid integrations and the packaging of these types of systems. The SiP concept adds effective space by allowing the circuits to be placed in several different layers. A good example of this concept is found in [33]. The additional layers also open the opportunity to add passive circuits, such as impedance matching networks, junctions or filters, to the package. The passive circuits can perform multiple functions efficiently, but usually require too much space. Some examples of these passive circuits can be found in [33], [53]–[58].

Multi-layer interposers not only add space for fitting the PICs and other devices but also help with the thermal management as will be explained in the next section.

1.2.3 The need for thermal management

This section discusses the need for thermal management in the packaging of PICs and how the multi-layer interposer provides more flexibility for thermal management compared to single-layer interposers.

The PICs need thermal management because the operating wavelength and optical power of any laser sources on the PICs are sensitive to the temperature (Figure 1.12). For example, in [59] the ratio $(\mathrm{d}\lambda/\mathrm{d}P)$ between the peak wavelength (λ) and the thermal power dissipated by the substrate (P) is calculated to be $9.98\,\mathrm{nm\,W^{-1}}$ for a hybrid III-V semiconductor compound on silicon laser emitting around 1550 nm. The wavelength of any laser in the PICs must be constant at all times because it represents a specific channel in the network. The wavelength drift is not the only parasitic effect, the optical power decreases with temperature too. Therefore the temperature of the PIC must be kept constant, which is usually done by using a thermoelectric cooling (TEC) in a control loop. This temperature control is expensive due to its constant use of energy and use of additional electronics for the implementation of the control loop.

A multi-layer interposer provides more flexibility for the thermal management than a single-layer interposer. For example, in [60] and in [61], cavities are added in a carrier board fabricated with LTCC to circulate some liquid coolant. Another example is the use of complex metallic structures, in [19] and in [32], where metallic planar channels and vias are used to route the heat taking advantage of the low thermal conductivity of the LTCC substrate. Co-fired AlN could be used together with air

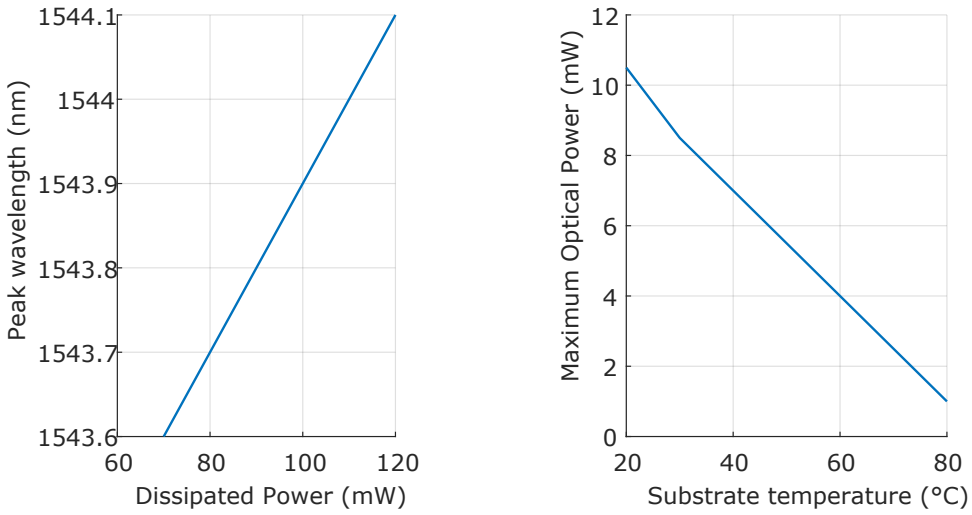


Figure 1.12: The performance of a laser is affected by the substrate temperature and the thermal power dissipated by the substrate. Data from [59].

cavities in a similar approach and AlN is much better for typical applications that require removing the heat from the system. These examples show that the multi-layer technologies can be very useful for the thermal management of the system, which is important in systems that include PICs.

Multi-layer interposers help to provide the thermal management needed by the PICs. This research explores two multi-layer technologies: LTCC and co-fired AlN see Sections 1.3.3 and 1.3.4. The reason for exploring co-fired AlN is the higher thermal conductivity that is useful for the thermal management discussed in this section. One more issue for the packaging of PICs is the cost of manufacture that is discussed in the next section.

1.2.4 The need for manufacturability

This section explains the need for manufacturability of the PICs. The section starts by discussing the typical cost of a photonic module, showing that the packaging is usually the most expensive part. Then the section discusses how multi-layer technologies can decrease this cost by enabling cost-effective situations for flip-chip bonding.

The PIC package is usually the most expensive part in a photonic module. For example, in [62] the cost breakdown by processes of a monolithically fabricated PIC is calculated (Figure 1.13) at a fabrication rate of 30 000 units annually. The cost breakdown shows that the largest cost is the package. The high cost of the packaging is the reason for the high benefit for moving from separately packaged devices to a single package (hybrid integration). Therefore, research to improve the hybrid integration techniques will be key to the long-term growth of PIC system sales.

The use of multi-layer technologies can make flip-chip more cost-effective. For example, in [50] a cost analysis comparison between flip-chip and wire-bonding

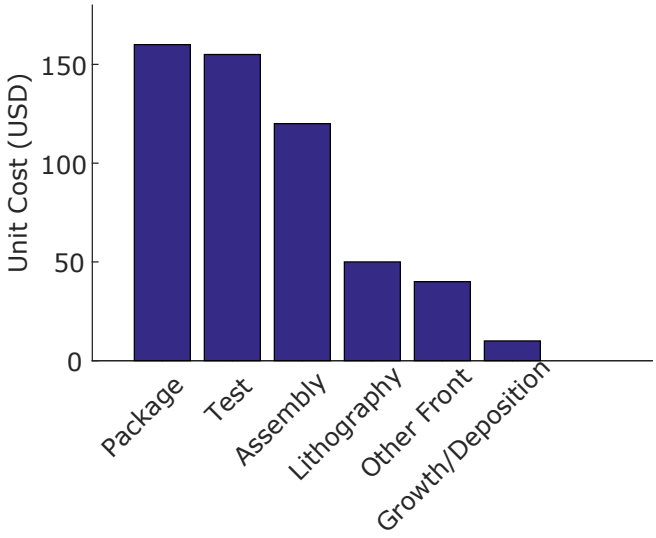


Figure 1.13: The cost breakdown by processes of a monolithically fabricated device at 30 000 units annually. The PIC packaging is the most expensive part of the module. Data from [62].

was completed. The conclusion from [50] showed that the equipment cost of wire-bonding is higher than the equipment cost of flip-chip. Also, the floor space occupied by wire-bonding is larger than for flip-chip. The study also concludes that the cost per good die is cheaper for larger devices if the flip-chip yield is very high, especially for high-cost good dies. Moreover, in the cases where the cost of flip-chip is higher, it might be compensated by the better performance, density, and form-factor. A more recent analysis [48] had the same conclusion - that flip-chip has a lower cost than wire-bonding for larger devices and also shows that the main cost of the flip-chip assembly is the substrate cost.

Section 1.2.4 shows that the package is the main cost of a PIC module and that the use of multi-layer technologies could reduce this cost by enabling a more effective use of flip-chip bonding.

Section 1.2 explains that the modules using PICs need high microwave performance, space for more devices, thermal management and manufacturability. Also, Section 1.2 shows how the use of multi-layer technologies could meet these needs. The objective of this research, presented in the next section, is to enable the use of these multi-layer technologies.

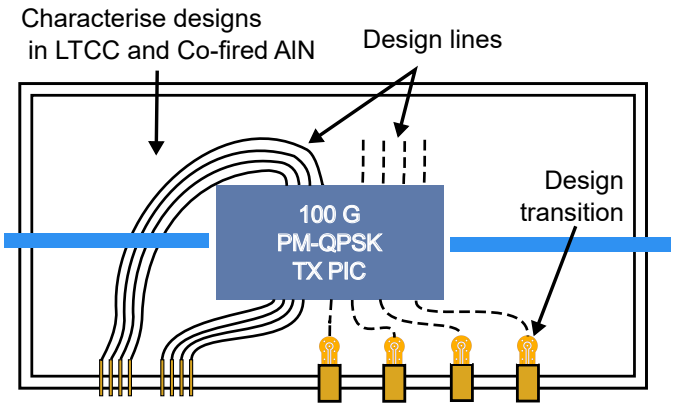


Figure 1.14: There are four objectives in this research. First, the design of multi-layer transmission lines. Second, the design of microwave vertical transitions for those transmission lines. Third the characterisation of an interposer fabricated from LTCC. Fourth, the characterisation of an interposer fabricated from co-fired AlN.

1.3 Objectives: Microwave design of multi-layer interposers for the packaging of PICs

This section discusses the objectives of this research. The general objective is to complete the microwave design of a multi-layer interposer for the packaging of PICs. This general objective is divided in four specific objectives (Figure 1.14). The first specific objective, explained in Section 1.3.1, is the design of transmission lines for the different layers that have low loss and low crosstalk. Those transmission lines need vertical transitions between them. Therefore, the second specific objective, explained in Section 1.3.2, is the design of those microwave vertical transitions. The first and the second objectives are achieved using theoretical work and electromagnetic simulations. In contrast, the third and fourth objectives are experimental. The third objective, explained in Section 1.3.3, is the characterisation of the designed transmission lines and the vertical transitions in LTCC. The fourth objective, explained in Section 1.3.4, is similar to the third one but in the fourth objective the material is co-fired AlN. The last two objectives aim to assess the feasibility of these designs and technologies for a high-speed interposer.

1.3.1 Designing transmission lines for multi-layer interposers

The first objective is to design transmission lines for multi-layer interposers. The transmission lines must have excellent microwave performance and minimise their

layout footprint. Electromagnetic simulations are used to achieve this objective.

The transmission lines must have excellent microwave performance; that is, low microwave-loss and low crosstalk. The microwave-loss objective is set to have loss below 1 dB cm^{-1} at 40 GHz. This objective is lower than the typical loss of 2.5 dB cm^{-1} for FR4, the typical material used to fabricate PCBs. The crosstalk objective is set to a maximum of −30 dB based on Figure 1.11 in Section 1.2.1 to have a BER power penalty below 0.3 dB. The crosstalk is higher for lines closer together so the crosstalk limits the minimal separation between adjacent lines.

The multi-layer transmission lines must be as small as possible. The restrictions to the miniaturisation of the lines are the crosstalk, the loss and the design rules. Electromagnetic simulations are used to design the transmission lines that fit these restrictions (Chapter 3).

Section 1.3.1 presented the first objective of this research which is the design of transmission lines suitable for a multi-layer interposer by using electromagnetic simulations. These transmission lines need to be connected through a vertical transition and the design of those transitions is the second objective presented in the next section.

1.3.2 Designing microwave vertical transitions

The second objective is to design microwave vertical transitions for the transmission lines designed in the first objective. The transition is critical for enabling the multi-layer interposer. Since the transition is a discontinuity, it cannot be simulated by a cross-section, so full-wave electromagnetic simulations are used.

The transition must have good transmission to support high-speed signals. This transmission is characterised by measuring the $f_{3\,\mathrm{dB}}$ so the objective is to design the vertical transition with $f_{3\,\mathrm{dB}} > 28\,\mathrm{GHz}$. This limit ensures the integrity of 40 Gbit s^{-1} NRZ signals.

The transition must have low complexity, must be simple enough to comply with standard commercial design rulesand and must use the smallest possible number of layers to facilitate the thermal management. The transition must also avoid using air cavities for the same reason.

Electromagnetic simulations are used to design the transitions that meet all the previous requirements. There are many variables that affect the performance of the transition, such as resonances, impedance mismatch and radiation. Therefore, finding the right design that minimizes the parasitic effects and optimises the performance cannot be done using simpler approaches and electromagnetic simulations are used.

In summary, Section 1.3.2 explains the second objective which is to design transitions with good microwave performance and low complexity. Electromagnetic simulations are used to design these transitions. However, simulations are not enough to assess the feasibility of the transmission lines and the vertical transitions; fabricated devices must be characterised which is the next objective.

1.3.3 Measuring an LTCC interposer

The third objective is to measure a board fabricated in LTCC with the elements designed in the first and second objectives. The full layout that was designed for this purpose is shown in Figure 1.15. Measurements are needed to assess the fabrication, to determine the real performance of the designed structures and to validate the electromagnetic simulations.

The measurement of the LTCC board is needed to assess the fabrication. The measurement of the LTCC interposer must provide two important fabrication characteristics: the material microwave performance and the fabrication dimensional variability. These characteristics are important to understand the differences between the simulated performance and the measurements.

The measurement of the LTCC board is needed to determine the real performance of the simulated structures. The structures have been designed using electromagnetic simulations that have not been validated. The characterisation of the board provides the actual performance of the circuits. The most important characteristics of the transmission line are the loss and the crosstalk and, for the vertical transition, the $f_{3\,\mathrm{dB}}$ and the eye diagram.

The measurement of the LTCC board is needed to validate the electromagnetic simulations. We need to guarantee the accuracy of the simulation results [63]. The simulation accuracy is diminished due to de-embedding errors, modelling errors and physical variability. De-embedding, explained in Chapter 2, is necessary for the microwave characterisation of the device under test (DUT). This de-embedding is usually done during the VNA calibration and is a source of errors. Another source of errors are the modelling errors that include: Algorithmic rounding errors, numerical truncation errors and port discontinuity errors (Chapter 2). Finally, the physical variability of the fabricated devices create variation compared with the exact physical models of our simulations. These are the reasons why the simulations models must be validated with actual microwave measurements.

Section 1.3.3 presented the third objective which is the measurement of a board fabricated in LTCC. The board's layout shown in Figure 1.15 has been designed and fabricated to be characterised. The details of the design, fabrication and characterisation of this layout are given in Chapter 5. This is done in order to assess the feasibility of the microwave design and to validate the electromagnetic simulations. The next objective is similar to that presented in this section but using co-fired AlN instead of LTCC.

1.3.4 Measuring a Co-fired AlN interposer

The fourth objective is to measure a board fabricated in co-fired AlN. The fourth objective is very similar to the third one in the last section but the measured interposer is now fabricated in co-fired AlN. The full layout that was designed for this purpose is shown in Figure 1.16. Just as in the third objective, the characterisation is needed to assess the fabrication technology, the designed structures and to validate the

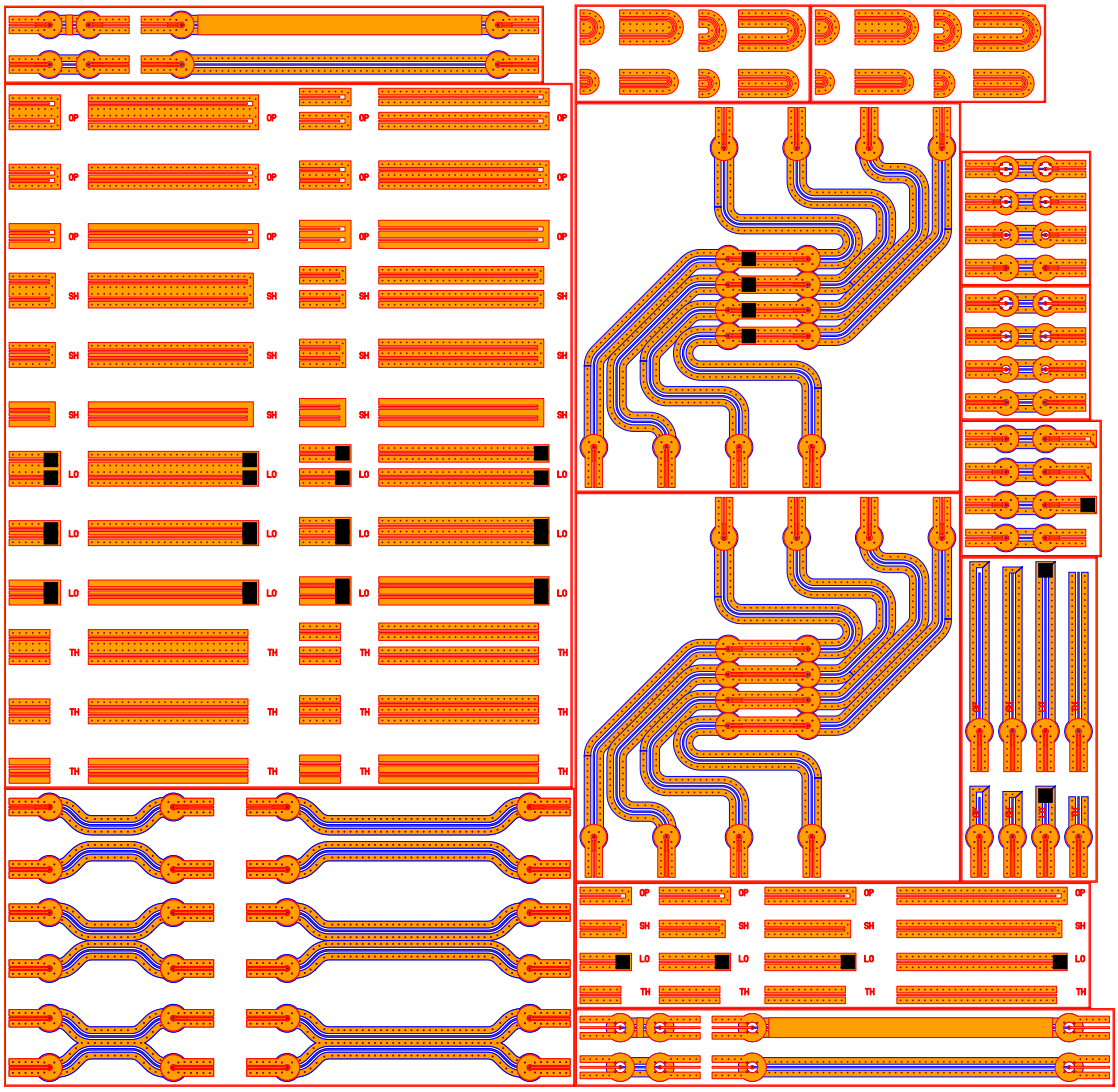


Figure 1.15: The layout fabricated in LTCC. The third objective is to characterise this fabricated board. The objects with red lines are top layer metals and the blue line is the buried layer metal. The ground backside metal is removed to allow for visibility.

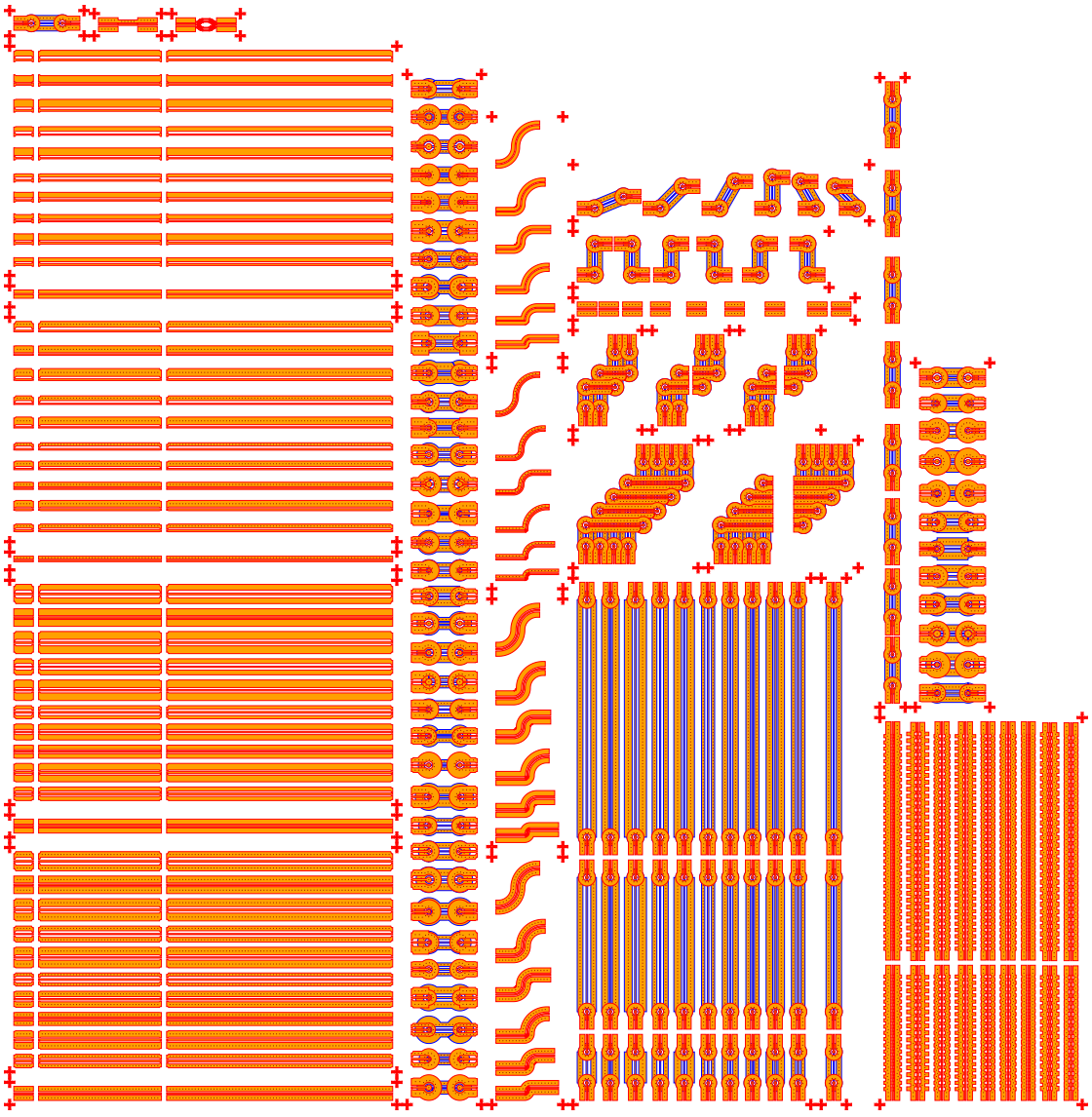


Figure 1.16: The layout fabricated in co-fired AlN. The fourth objective is to characterise this fabricated board. New structure that expand over the first desings are added in this layout. The objects with red lines are top layer metals and the blue line is the buried layer metal. The ground backside metal is removed to allow for visibility.

electromagnetic simulations but also serves as a comparison between LTCC, the typical multi-layer microwave technology, and co-fired AlN that is not typical for high-speed applications but rather for high-power applications due to its higher thermal conductivity.

The measurement of a co-fired AlN board is important to assess the fabrication technology and the designed structures and to validate the electromagnetic simulations. These are the same objectives discussed for LTCC in the previous section.

The measurement of the co-fired AlN also serves as a comparison to LTCC. The standard multi-layer microwave technology is LTCC and AlN as a single-layer substrate is popular in high-power electronics and PICs because of the high thermal conductivity. This characterisation serves as an assessment of the viability of co-fired AlN as a replacement for LTCC for the packaging of PICs.

Section 1.3.4 presented the fourth and last objective which is very similar to the third one but for a board fabricated using co-fired AlN. The results serve as an assessment of co-fired AlN as a replacement for the standard LTCC.

In summary, Section 1.3 presents the four objectives of this research. These four objectives are key to enable the use of high-speed multi-layer interposers for PICs. This document's chapters map these four objectives as explained in Section 1.4.

1.4 In this document

The rest of the document is divided into six chapters. The document starts from the most theoretical work in Chapter 2, move to analysis based on electromagnetic simulation in Chapters 3 and 4 and finishes with the experimental work in Chapters 5 and 6. Chapter 2 presents the microwave design methodology, that is the theory and methods used in this research including some developed by the author. Therefore, Chapter 2 has information that is needed to understand the results in the other chapters. Chapters 3 to 6 map the four objectives in Section 1.3: Chapter 3 presents the electromagnetic simulations completed to design the transmission lines discussed in Section 1.3.1; Chapter 4 presents the electromagnetic simulations and optimisations used to design the vertical transitions in Section 1.3.2; Chapter 5 presents the characterisation results of a board fabricated in LTCC as discussed in Section 1.3.3 and, Chapter 6 does the same as Section 1.3.3 but for co-fired AlN, as discussed in Section 1.3.4. Finally, Chapter 7 concludes the document presenting a summary of the findings, the main conclusions and the future work.

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Chapter 2
The microwave design methodology

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This chapter presents the microwave design methodology, that is the theory and methods used in this research including some developed by the author. Section 2.1 summarises the electromagnetic theory in which microwave theory and the electromagnetic simulators are based. Section 2.2 summarises the most important concepts

of the circuit theory used to represent a transmission line. Section 2.3 discusses the more general circuit concept of the microwave network used to represent complex three-dimensional devices like transitions. Section 2.4 explains the measurements used to obtain these microwave networks for our devices and, finally, Section 2.5 explains the functioning of the electromagnetic simulators used in this research.

> Electric and magnetic forces. May they live for ever, and never be forgot, ...
>
> *Oliver Heaviside*
> *Electromagnetic Theory (1912), Volume III;*

2.1 Electromagnetic theory

This section presents the electromagnetic theory on which the simulators and this research are based. Section 2.1.1 presents Maxwell's equations in the way the electromagnetic simulators use them. Section 2.1.2 discussed how conductors absorb electromagnetic power and the implications of this fact.

2.1.1 Maxwell's equations and plane waves

This section presents a summary of Maxwell's equations and the plane wave concept used by the electromagnetic simulators. Maxwell's equations are explained in detail in several well-known sources, for example [1] and here only a short discussion on some important considerations is presented.

The electromagnetic state of a system is completely represented by two vectorial fields, the electric field ($\vec{\mathbf{E}}$ in $\mathrm{V\,m^{-1}}$) and the magnetic field ($\vec{\mathbf{H}}$ in $\mathrm{A\,m^{-1}}$). Maxwell's equations describe the characteristics that these fields must have. The four equations that constitute Maxwell's equations are:

$$\boldsymbol{\nabla} \times \vec{\mathbf{E}} = -j\omega\mu\vec{\mathbf{H}} - \vec{\mathbf{M}}_{\text{ext}} \tag{2.1a}$$

$$\boldsymbol{\nabla} \times \vec{\mathbf{H}} = (j\omega\epsilon + \sigma)\vec{\mathbf{E}} + \vec{\mathbf{J}}_{\text{ext}} \tag{2.1b}$$

$$\boldsymbol{\nabla} \cdot \left(\epsilon\vec{\mathbf{E}}\right) = \rho \tag{2.1c}$$

$$\boldsymbol{\nabla} \cdot \left(\frac{\vec{\mathbf{H}}}{\mu}\right) = 0 \tag{2.1d}$$

where j is the imaginary unit. In these equations the time (t) dependency is $e^{j\omega t}$ and ω is the angular frequency, related to the frequency (f) by $\omega = 2\pi f$. The system geometry is defined by the three material microwave-parameters: the complex

permittivity ($\epsilon = \epsilon' + j\epsilon''$ in $\mathrm{F\,m^{-1}}$), the complex permeability ($\mu = \mu' + j\mu''$ in $\mathrm{H\,m^{-1}}$) and the conductivity (σ in $\mathrm{S\,m^{-1}}$). The sources of electromagnetic energy in the systems are threefold: an electric current density ($\vec{\mathbf{J}}_{\mathrm{ext}}$ in $\mathrm{V\,m^{-2}}$), a magnetic current density ($\vec{\mathbf{M}}_{\mathrm{ext}}$ in $\mathrm{A\,m^{-2}}$) and a electrical charge density (ρ in $\mathrm{C\,m^{-3}}$).

In all our simulations, all the sources are assumed to be outside our system. In this case, Maxwell's equations are reduced to:

$$\nabla \times \vec{\mathbf{E}} = -j\omega\mu\vec{\mathbf{H}} \tag{2.2a}$$

$$\nabla \times \vec{\mathbf{H}} = (j\omega\epsilon + \sigma)\vec{\mathbf{E}} \tag{2.2b}$$

$$\nabla \cdot \left(\epsilon\vec{\mathbf{E}}\right) = 0 \tag{2.2c}$$

$$\nabla \cdot \left(\frac{\vec{\mathbf{H}}}{\mu}\right) = 0 \tag{2.2d}$$

The last four equations depending on $\vec{\mathbf{E}}$ and $\vec{\mathbf{H}}$ can be reduced to only three depending only on $\vec{\mathbf{E}}$ by solving for $\vec{\mathbf{H}}$ in Equation 2.2a and substituting this into Equations 2.2b and 2.2d. After the substitutions the following three equations remain:

$$\nabla \times \left(\frac{\nabla \times \vec{\mathbf{E}}}{\mu}\right) = \left(\omega^2\epsilon - j\omega\sigma\right)\vec{\mathbf{E}} \tag{2.3a}$$

$$\nabla \cdot \left(\epsilon\vec{\mathbf{E}}\right) = 0 \tag{2.3b}$$

$$\nabla \cdot \left(\frac{\nabla \times \vec{\mathbf{E}}}{\mu^2}\right) = 0 \tag{2.3c}$$

After solving these last three equations for $\vec{\mathbf{E}}$, $\vec{\mathbf{H}}$ can be recovered by Equation 2.2a. If ϵ and μ are constant in the region of interest, Equation 2.3 can be reduced to a single equation called the wave equation:

$$\nabla^2\vec{\mathbf{E}} - \gamma^2\vec{\mathbf{E}} = 0 \tag{2.4a}$$

$$\gamma = \alpha + j\beta = j\omega\sqrt{\mu\epsilon}\sqrt{1 - j\frac{\sigma}{\omega\epsilon}} \tag{2.4b}$$

Where γ is the complex propagation constant, α is the attenuation constant and β is the phase constant. The plane wave is the solution to the wave equation described by the next three equations:

$$\vec{\mathbf{E}} = \vec{\mathbf{E}}_0 e^{-\vec{\mathbf{k}}\cdot\vec{\mathbf{r}}} \tag{2.5a}$$

$$\vec{\mathbf{k}} \cdot \vec{\mathbf{E}}_0 = 0 \tag{2.5b}$$

$$\left|\vec{\mathbf{k}}\right| = \gamma \tag{2.5c}$$

Table 2.1: The conductivity and skin depth at 10 GHz for several common conductors. The skin depth is small compared with the usual circuit dimensions.

	σ [S m^{-1}]	δ_s [µm]
Aluminium	3.816×10^7	0.814
Copper	5.813×10^7	0.660
Gold	4.098×10^7	0.786
Silver	6.173×10^7	0.640

Being a fundamental solution to the wave equation, any solution of the wave equation can be expanded to a superposition of plane waves. An important case for the microwave engineering field is the propagation of a plane wave in a good conductor which is the topic of the next section.

2.1.2 Power absorbed by a good conductor

For a plane wave propagating with $\vec{\mathbf{k}} = \gamma \hat{\boldsymbol{z}}$. The plane wave is

$$\vec{\mathbf{E}} = \vec{\mathbf{E}}_0 e^{-\alpha z} e^{-j\beta z} \tag{2.6}$$

which shows that α is an exponential decay constant. Therefore, the skin depth (δ_s) is defined as the mean travel length ($\delta_s = \frac{1}{\alpha}$). If the material is a good conductor then $\frac{\sigma}{\omega\epsilon} \gg 1$ and Equation 2.4b becomes

$$\gamma = \alpha + j\beta = \sqrt{\frac{\omega\mu\sigma}{2}} + j\sqrt{\frac{\omega\mu\sigma}{2}} \tag{2.7}$$

and the skin depth becomes

$$\delta_s = \sqrt{\frac{2}{\omega\mu\sigma}} \tag{2.8}$$

At high frequencies and for a high σ, the skin depth is very short as can be seen in Table 2.1. This result is important because it means that only a thin plating of a good conductor is necessary for low-loss microwave components.

The power dissipated by the conductor (R_s) in a surface S is for this case

$$P_{\text{avg}} = \frac{R_s}{2} \int_S \left\| \vec{\mathbf{H}} \right\|^2 \mathrm{d}s \tag{2.9a}$$

$$R_s = \sqrt{\frac{\omega\mu}{2\sigma}} = \frac{1}{\sigma\delta_s} \tag{2.9b}$$

where R_s is the surface resistance of the conductor. Equation 2.9b shows that the dissipated power by the good conductor will increase with frequency and with the intensity of the fields in the surface. The equation also shows that the dissipated power is lower with metals with higher conductivity.

Section 2.1 presented some important concepts from the Electromagnetic Theory used in this research. Maxwell's equations summarise the Electromagnetic Theory that describes microwave phenomena and microwave engineering translates this description of the phenomena into practical terms of circuit theory. The microwave transmission lines use metals to guide the electromagnetic fields, and the implications of the metal conductivity on the loss was discussed.

2.2 Transmission lines

A transmission line is modelled as a distributed circuit. The goal of microwave engineering is to translate electromagnetic theory to electronic circuit theory. The concept of a transmission line is a good example of this translation. Section 2.2.1 presents the Telegrapher's equation that describe the distributed circuit of a general transmission line. Section 2.2.2 discusses the solution to the Telegrapher's equation when the transmission line is uniform in z, which is the simplest case. The more general case of a non-uniform transmission line is discussed in Section 2.2.3. Finally, Section 2.2.4 presents the time-domain reflectometry (TDR) concept that is very useful to understand the sources of unwanted reflections in a system.

2.2.1 Telegrapher's equations

The transmission line theory presented in this section was developed by Oliver Heaviside, whose first employment was as a telegraph operator. Heaviside formulated the main equations that describe transmission line theory, which are called the Telegrapher's equations. An analysis of the Telegrapher's equations show that if one could distribute inductance in a telegraph line uniformly, this would cut down on the attenuation and distortion of the signal. Based on this equation, he proposed that inductance loading a line by using induction coils could greatly decrease the amount of distortion of signals transmitted along the lines. Years later, AT&T built upon Heaviside's work and obtained a patent in 1904. AT&T offered part of the proceeds to Heaviside, who refused unless AT&T also gave him full recognition for the idea. Heaviside was very poor at this point and the proceeds would have solved all his financial problems [2].

The RLGC distributed-parameter lumped-element circuit shown in Figure 2.1 is the circuit representation of a transmission line. The series inductance (L) represents the total self-inductance of the two conductors in $\mathrm{H\,m^{-1}}$. The shunt capacitance (C) is the capacitance between the two conductors in $\mathrm{F\,m^{-1}}$. The series resistance

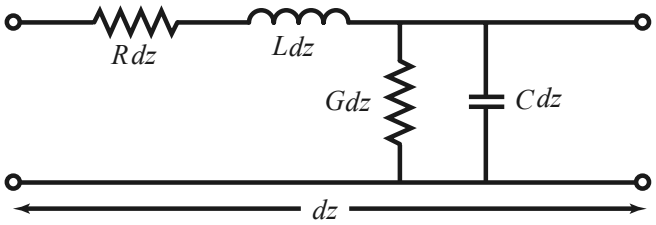


Figure 2.1: The distributed-parameter lumped-element circuit model ($RLGC$) of a transmission line [1].

(R) represents the resistance due to the conductivity of the individual conductors in $\Omega\,\mathrm{m}^{-1}$. Finally, the shunt conductance (G) is related to the dielectric loss in the material between the conductors and given in $\mathrm{S\,m}^{-1}$. The resistive element R and G create the loss in the transmission lines. Therefore, a transmission line where $R = G = 0$ is called a lossless transmission line. A transmission line is thus modelled as a cascade of sections similar to Figure 2.1.

The analysis of a cascade of circuits similar to Figure 2.1 using standard circuit theory gives the next two equations

$$\frac{\mathrm{d}V(z)}{\mathrm{d}z} = -(R(z) + j\omega L(z))I(z) = -Z(z)I(z) \tag{2.10a}$$

$$\frac{\mathrm{d}I(z)}{\mathrm{d}z} = -(G(z) + j\omega C(z))V(z) = -Y(z)V(z) \tag{2.10b}$$

where the sinusoidal steady-state condition ($e^{j\omega t}$) is assumed. These two equations are the Telegrapher's equations and describe completely the propagation of a signal through the full length of the transmission line.

The transmission line parameters (R, L, G, C) can be related to the electric field ($\vec{\mathbf{E}}$) and magnetic field ($\vec{\mathbf{H}}$) introduced in Section 2.1.1. This relation is given by the next four equations:

$$L = \frac{\mu'}{|I_0|^2} \int_S \vec{\mathbf{H}} \cdot \vec{\mathbf{H}}^* \,\mathrm{d}s \tag{2.11a}$$

$$C = \frac{\epsilon'}{|V_0|^2} \int_S \vec{\mathbf{E}} \cdot \vec{\mathbf{E}}^* \,\mathrm{d}s \tag{2.11b}$$

$$R = \frac{R_S}{2} \int_{C_1+C_2} \vec{\mathbf{H}} \cdot \vec{\mathbf{H}}^* \,\mathrm{d}l \tag{2.11c}$$

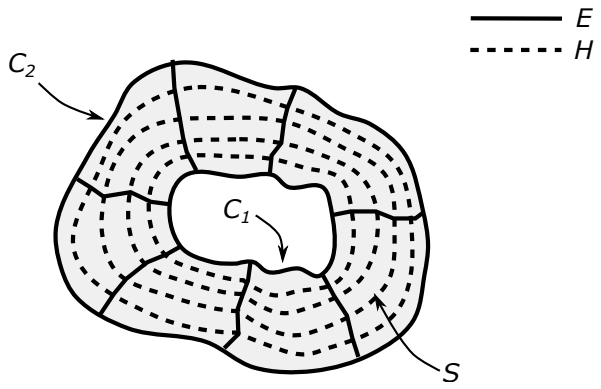


Figure 2.2: Field lines of an arbitrary transmission line [1]

$$G = \frac{\omega\epsilon''}{|V_0|^2}\int_S \vec{\mathbf{E}}\cdot\vec{\mathbf{E}}^*\,\mathrm{d}s \tag{2.11d}$$

where the surface (S) is the dielectric between two metals, signal and ground, placed at the contours C_1 and C_2 as shown in Figure 2.2. The parameters ϵ', ϵ'' and μ' describe the dielectric in the surface S and the surface resistance R_S describes the conductors in the line contours C_1 and C_2.

The response at any point of the transmission line to an input is given by the solution to the Telegrapher's equations. The simplest solution to these equations is the case of an uniform transmission line which is discussed in the next section.

2.2.2 Uniform transmission lines

This section presents the solution to the Telegrapher's equations for the case of a uniform transmission line, which is the simplest case and its solution provides important insight to understand the propagation of high-speed signals.

For a uniform line the four real functions $R(z)$, $L(z)$, $G(z)$ and $C(z)$ become four real constants and the telegrapher equations can be separated into two wave equations

$$\frac{\mathrm{d}^2V(z)}{\mathrm{d}z^2} - \gamma^2 V(z) = 0 \tag{2.12a}$$

$$\frac{\mathrm{d}^2I(z)}{\mathrm{d}z^2} - \gamma^2 I(z) = 0 \tag{2.12b}$$

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} = \sqrt{ZY} \tag{2.12c}$$

where γ is again called the complex propagation constant, as in Equation 2.4; α is called the attenuation constant and β is called phase constant. The analogy between

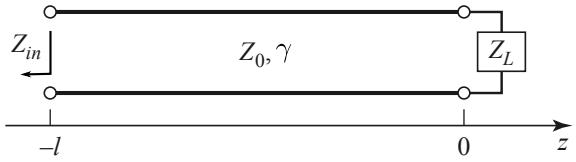


Figure 2.3: A transmission line terminated by an impedance Z_L. Based in [1].

the propagation of a sinusoidal signal in a transmission line and a plane wave is evident.

The solutions to these equations are given by

$$V(z) = V_0^+ e^{-\gamma z} + V_0^- e^{+\gamma z} \tag{2.13a}$$

$$I(z) = \frac{V_0^+}{Z_0} e^{-\gamma z} + \frac{V_0^-}{Z_0} e^{+\gamma z} \tag{2.13b}$$

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} = \sqrt{\frac{Z}{Y}} \tag{2.13c}$$

where V_0^+ is the amplitude of the sinusoidal signal travelling in the z direction and V_0^- the amplitude of the signal in the $-z$ direction. Z_0 is called the characteristic impedance of the transmission line.

A uniform transmission line can be fully described by four real numbers (R, L, G and C), the two complex impedances (Z and Y), or by the characteristic impedance and complex propagation constant (Z_0 and γ). The transformation between these representations are given by Equations 2.12c and 2.13c or by

$$Z = R + j\omega L = Z_0 \gamma \tag{2.14a}$$

$$Y = G + j\omega C = \frac{\gamma}{Z_0} \tag{2.14b}$$

The quality of a transmission line is measured by a Quality factor (Q) which is defined in terms of the attenuation constant (α) and the phase constant (β), from Equation 2.12c, by [3]

$$Q = \frac{\beta}{2\alpha} \tag{2.15}$$

In the case where the transmission line is terminated (Figure 2.3), the reflection (Γ) is given by

$$\Gamma = \frac{Z_{\text{in}} - Z_g}{Z_{\text{in}} + Z_g} \tag{2.16a}$$

$$Z_{\text{in}} = Z_0 \frac{Z_L + Z_0 \tanh \gamma l}{Z_0 + Z_L \tanh \gamma l} \tag{2.16b}$$

where Z_g is the source impedance, Z_{in} is the effective impedance at the end of the transmission line that is not terminated by the load, the load impedance (Z_L) is the effective impedance of the termination (Figure 2.3). If we assume that $Z_g = Z_L$ as is usually the case for the measurements (Section 2.4) the reflection is then

$$\Gamma = \frac{Z_0^2 - Z_L^2}{2Z_0 Z_L \coth \gamma l + Z_0^2 + Z_L^2} \tag{2.17}$$

which shows that matching the load and the characteristic impedance of the line ($Z_L = Z_0$) gives zero reflection and that the reflection will be also dependant on the length of the line. The model of the uniform transmission line is very useful but there are situations where the transmission line must contain non-uniform segments. That is the case discussed in the next section.

2.2.3 Non-uniform transmission lines

This section discusses the case of non-uniform transmission lines, that is transmission lines with segments of distinct characteristics. Getting the response to a signal of a non-uniform transmission line involves solving the Telegrapher's equations (Equation 2.10). There are multiple approaches to solve the non-uniform transmission lines: some based on semi-discrete methods [4], [5], power-series approximations [6]), ABCD matrices ([7], closed form approximations [8], [9], and bounce diagrams [4], [10]–[15]. In this research, an algorithm based on the bounce diagram was chosen due to its simplicity.

The implemented algorithm, from [13], is based on the bounce diagram shown in Figure 2.4. The non-uniform transmission line is represented as a chain of segments of uniform transmission lines. Each segment in the chain has a characteristic impedance Z_{0i} where i is an integer that represents the position of the segment in the chain. The non-uniform transmission line is terminated with an impedance Z_L. In each time step (Δt), depicted by the index j, the boundary between each segment creates a reflected and transmitted wave as depicted in Figure 2.4.

From Figure 2.4, the basic lattice is shown in Figure 2.5. In this basic lattice, $V^R(i,j)$ represents the voltage amplitude of the wave travelling out of node (i,j) to the right and $V^L(i,j)$ the same but for the wave travelling to the left. From the basic lattice, the next relations arise

$$V^R(i,j) = V^R(i-1,j-1)(1+\Gamma(i)) - V^L(i+1,j-1)\Gamma(i) \tag{2.18a}$$
$$V^L(i,j) = V^R(i-1,j-1)\Gamma(i) + V^L(i+1,j-1)(1-\Gamma(i)) \tag{2.18b}$$

where the reflection coefficient $\Gamma(i)$ is defined by

$$\Gamma(i) = \frac{Z_0(i+1) - Z_0(i)}{Z_0(i+1) + Z_0(i)} \tag{2.19}$$

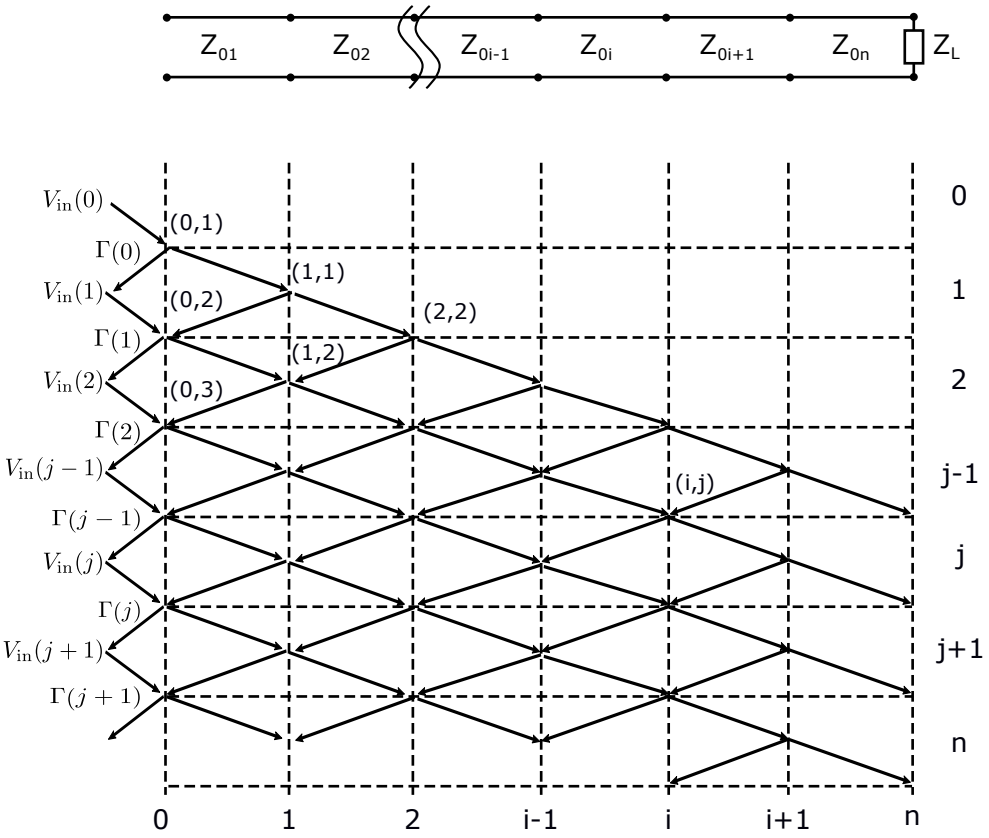


Figure 2.4: A bounce diagram that illustrates the multiple reflections in a discrete non-uniform transmission line. Based on [13].

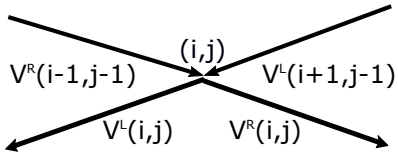
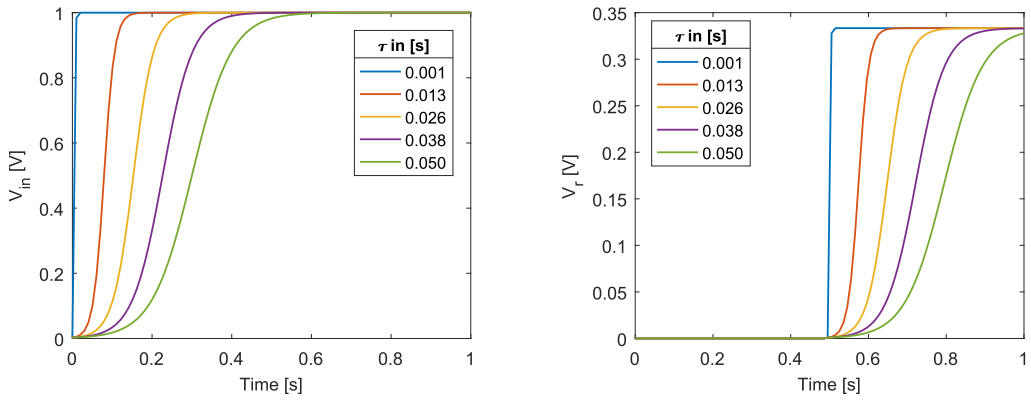


Figure 2.5: The basic lattice of our non uniform transmission line modelled as a chain of uniform transmission lines.



(a) Input (b) Reflection

Figure 2.6: Several non-ideal step inputs (Figure 2.6a) and the corresponding calculated reflection (Figure 2.6b).

where $Z_0(i)$ is the characteristic impedance of the i segment in the chain.

Therefore, three things are needed to calculate the next time step state and reflection of a chain. First, the array of characteristic impedances in the chain (Z_{0i}) including the termination load (Z_L) and the input impedance (Z_{00}). Second, the arrays of the current propagating voltages, that is V^R, V^L. Finally, the input voltage at the time step (V_{in}). The algorithm to propagate a step implemented in Matlab is given in Appendix A.1.1.

The propagation algorithm is used to calculate the reflection on a simple 50 Ω to 100 Ω transition for different input profiles. The input voltage is defined as:

$$V_{\text{in}}(t) = \frac{1}{1 + e^{-t/(\tau+6)}} \tag{2.20}$$

where the constant τ in s defines how sharp the step is (Figure 2.6a). This function tends to the Heaviside function when $\tau \to 0$. The reflection results show that the shape of the input step together with the impedance profile defines the shape of the reflection (Figure 2.6b). These reflections can be used to reconstruct the non-uniform transmission line as explained in the next section.

2.2.4 Time-domain reflectometry

Time-domain reflectometry (TDR) is a technique used to determine the characteristics of long devices by observing the reflected waveforms (Figure 2.7). The impedance at the discontinuity can be determined from the amplitude of the reflected signal. The distance to the reflecting impedance can also be determined from the time that a pulse takes to return. Therefore, TDR has been used to locate faults in electrical connections and optimize circuits [16]–[22].

The reflection used in TDR can be obtained in the time-domain or in the frequency-domain. Moreover, the reflection can be obtained using electromagnetic simulations

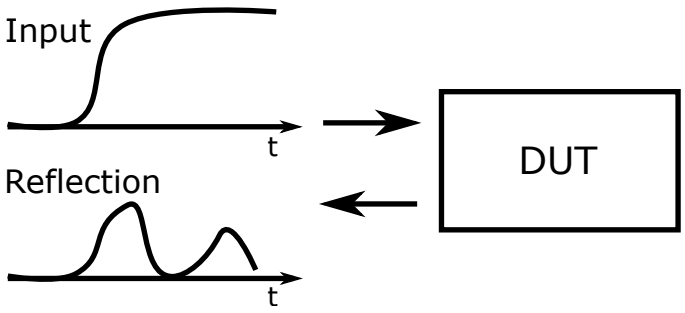


Figure 2.7: The TDR uses the reflected signal to imagine a non-uniform transmission line.

or by measurement. The theory behind the time-domain and the frequency-domain simulations is explained in Section 2.5. Experimentally, the time-domain reflection is obtained using Time-domain reflectometres and the frequency-domain reflection is obtained from a vector network analyser (VNA), see Section 2.4. The time domain reflection $\Gamma(t)$ can be calculated from the frequency-domain reflection $\Gamma(f)$ by [13]

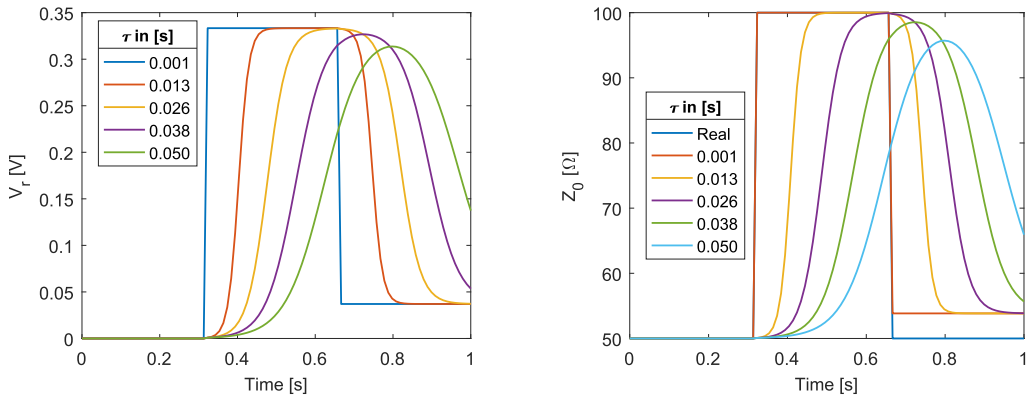
$$\Gamma(t) = \text{ICZT}\left[\frac{\Gamma(f)}{1-e^{-j\frac{2\pi f}{N+1}}}\right] \tag{2.21}$$

where ICZT is the inverse Chirp-Z transform and N is the total number of points in $\Gamma(f)$.

After the reflection has been obtained, the impedance profile has to be reconstructed [11]–[15], [23]. The simplest way to reconstruct the impedance is the relation:

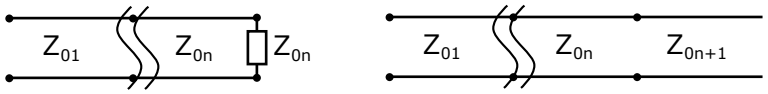
$$Z_0(n) = Z_{00}\frac{1+\Gamma(n)}{1-\Gamma(n)} \tag{2.22}$$

but this equation does not take into account either the multiple reflections inside a non-uniform transmission line or the input voltage profile and therefore the reconstructed impedance profile is wrong. For example, the reflection from a double impedance discontinuity is calculated using the algorithm in Appendix A.1.1 and shown in Figure 2.8a and the recovered impedance by Equation 2.22 is shown in Figure 2.8b. Clearly, the reconstructed impedance profile is shaped by the input voltage profile and thus a sharp input step is needed. In Figure 2.8b, only the input signal with $\tau = 0.001\,\text{s}$ predicts the square shape of the real impedance profile. However, even



(a) Reflection (b) Impedance

Figure 2.8: The reflection and impedance reconstruction of a impedance discontinuity by Equation 2.22. The reconstruction fails to recover the real impedance after the second discontinuity even for close to ideal inputs ($\tau \approx 0$).



Perfect match load with next segment

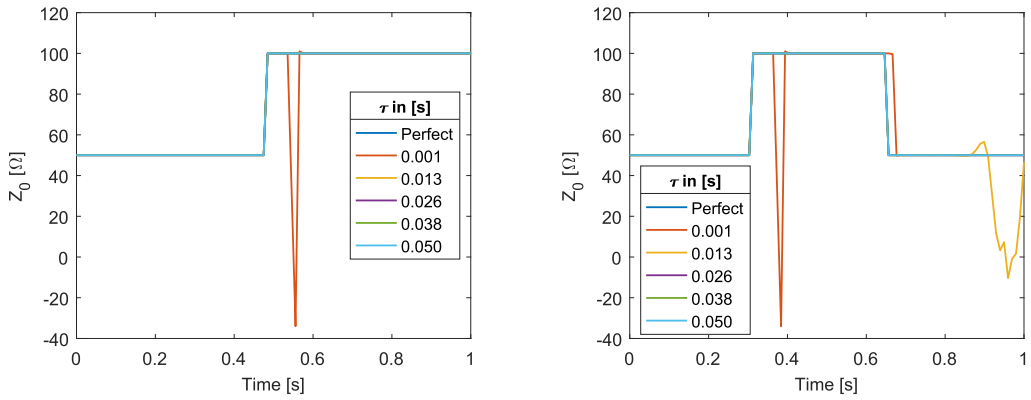
Figure 2.9: The cascaded uniform transmission line reconstruction is based on the comparison of these two models.

for a sharp input step, the reflection in the last third of Figure 2.8a is not zero even when the impedance is 50 Ω in that section. This reflection comes from the non-wave-front signal reflecting at previous discontinuities located times 0.33 s and 0.66 s and this creates the discrepancy of impedance in Figure 2.8b since Equation 2.22 does not take into account multiple reflections. This problem can become critical when more complex impedance profiles are being characterised and thus highlights the importance of using a reconstruction algorithm.

A novel impedance profile reconstruction algorithm has been created. The algorithm is a generalization of the algorithm in [13]. The ideas is to compare the actual reflection with the known reflection from the model of the known impedances terminated with a perfect matched load, as illustrated in Figure 2.9. The comparison of both models gives the next relationship

$$\Gamma(n) = \frac{V_{\mathrm{r}}(n) - V_{\mathrm{rm}}(n)}{V_{\mathrm{fw}} \prod_{i=0}^{n-1} (1 - \Gamma(i)^2)} \tag{2.23}$$

where $V_r(n)$ is the measured or simulated reflection at time n, $V_{\mathrm{rm}(n)}$ is the expected reflection from the known impedance chain assuming a perfectly matched load at time n (left circuit in Figure 2.9). V_{fw} is the amplitude of the front-wave, that is the $V_{\mathrm{in}}(0)$. The denominator of Equation 2.23 represents the voltage of part of the



(a) Step (b) Discontinuity

Figure 2.10: The results of the impedance reconstruction algorithm generalized to used arbitrary input.

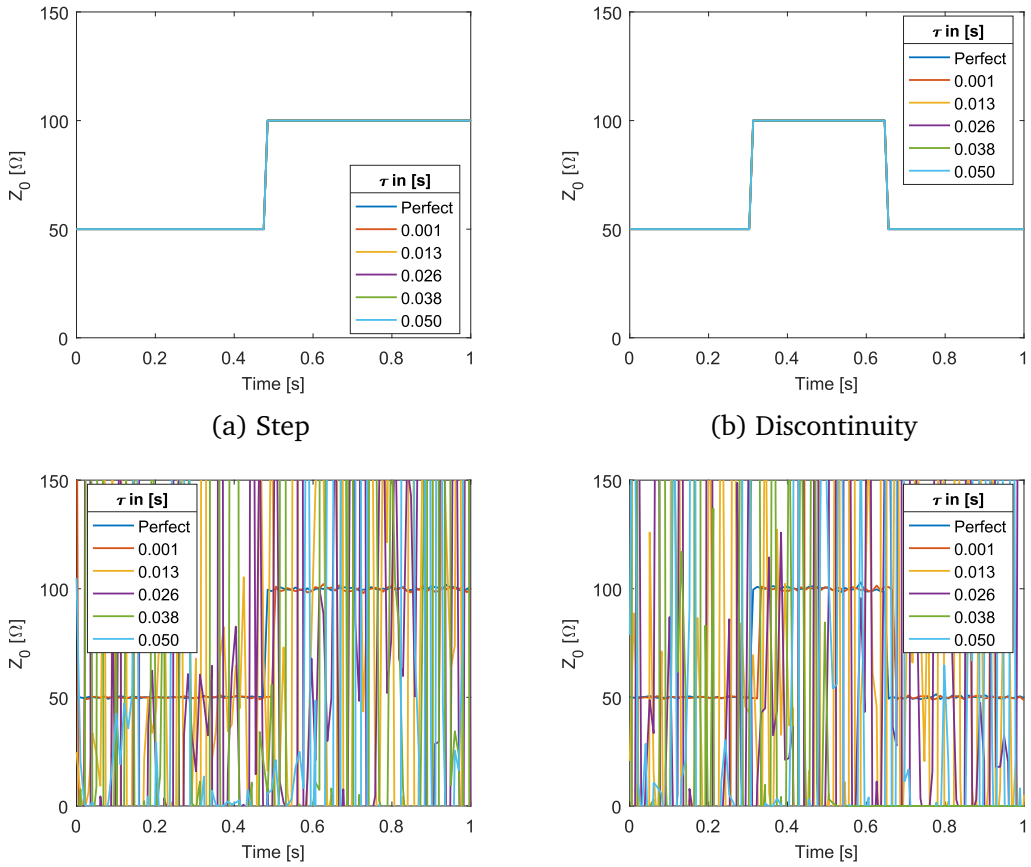
wave-front that travels to the input to the discontinuity n, reflects completely there, and comes back to the input side without any further reflection. Therefore, the algorithm works by calculating the reflection of the known segments of the chain with a perfect match to calculate $V_r(n)$. Then Equation 2.23 is used to calculate the reflection of the next interface, and finally Equation 2.22 is used to obtain the characteristic impedance of the next section. This procedure is repeated iteratively and the code is provided in Appendix A.1.2.

The results for this generalized algorithm in the step and in the discontinuity are shown in Figure 2.10. This algorithm is able to recover, in general, the correct impedance profile. The algorithm is able to remove the input voltage profile, a clear example of this is in the comparison between Figure 2.8b and Figure 2.10b. The problem with this algorithm is that it is unstable. Small numerical errors oscillate non-linearly and create chaotic behaviours as illustrated in the peaks in Figure 2.10.

To solve the oscillation problem, a second algorithm has been created. This algorithm uses a minimum impedance change to remove the small oscillations (Appendix A.1.3). The results of the new algorithm are able to recover the impedance (Figures 2.11a and 2.11b). However, if noise is added in the form of a standard normal distribution with peak at 0.01 V the algorithm fails to recover the impedance profile (Figures 2.11c and 2.11d) for all the cases except when the input profile is a perfect step. The reason is that since the input profile monolithically increases, the front-wave voltage is very small and thus the denominator of Equation 2.23 is almost zero. Then the noise creates small errors in the impedance that then are compensated in the following steps creating a non-linear oscillation.

This algorithm works well for reflections created by the full-wave time-domain electromagnetic solver (Section 2.5.2) since it contains only small numerical errors.

Section 2.2 presented the theory behind the concept of a transmission line. The transmission lines are modelled as a distributed circuit with a state that is described



(a) Step

(b) Discontinuity

(c) Step using noisy signals

(d) Discontinuity using noisy signals

Figure 2.11: The results of the impedance reconstruction algorithm generalized with stabilisation. The algorithm is able to recover the impedance profile for slow input voltage profiles for low noise signals (a-b). However, It stops working for noisy signals (c-d).

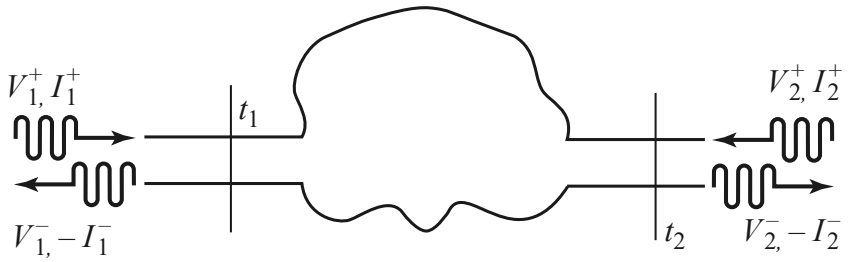


Figure 2.12: An arbitrary two-port microwave network. Based on [1].

by the Telegrapher's equation. The simplest case is the uniform transmission line. A uniform transmission line can be described by four real variables R, L, G and C or two complex numbers Z_0 and γ. The case of non-uniform transmission lines do not have a simple general solution but there are a few algorithms to solve these systems. Based on the idea of the non-uniform transmission lines, the TDR idea uses the reflection of a system to obtain an equivalent transmission line. The TDR is then very useful to get an idea of the source of reflection in the system.

2.3 Microwave Networks

A microwave network is a circuit representation of a microwave device (Figure 2.12). A microwave circuit is governed by Maxwell's equations and therefore the functioning of any device can be described by electromagnetic fields. However, the electromagnetic fields provide significantly more information than what is usually needed. To avoid this, a microwave network represents the device by its response to voltages and currents which are more common in circuit theory. The input and output voltages are fed into the microwave network through ports. A port in a microwave network is defined as a transmission line of a single propagation mode that connects the microwave network to other circuits.There are a few different types of microwave networks that can describe a microwave device. First, Section 2.3.1 describes the scattering matrix that relates the wave amplitudes of the reflected and transmitted waves travelling through the microwave device. The problem with the matrices generated by this approache is that they do not cascade, so Section 2.3.2 presents the ABCD matrix that is used to cascade multiple microwave circuits. Finally, Section 2.3.3 discusses how to use these networks to describe an arbitrary passive circuit.

2.3.1 Scattering matrix

The scattering matrix represents a microwave network in a way that it is easy to relate with direct measurements. The scattering matrix relates the incident, reflected, and transmitted waves instead of the voltages and currents. Thus, the reflected and transmitted waves can be measured directly using a VNA (Section 2.4).

The scattering matrix ($[S]$) relates the voltage waves incident on the ports to those

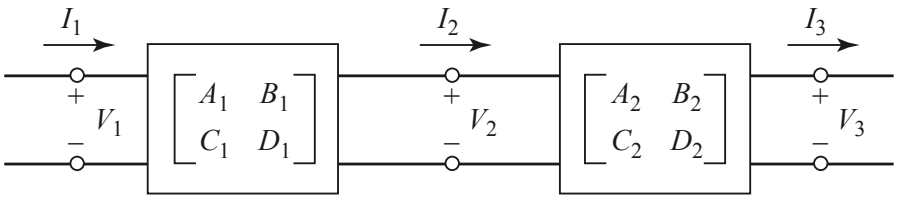


Figure 2.13: A cascade connection of two-port arbitrary microwave networks. Based on [1].

reflected from the ports as:

$$\left[V^-\right] = [S]\left[V^+\right] \tag{2.24a}$$

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix} \tag{2.24b}$$

The next terminology is used in this document

$$\text{Transmission in dB} = 20\log|S_{21}| \tag{2.25a}$$

$$\text{Reflection in dB} = -20\log|S_{11}| \tag{2.25b}$$

$$\text{Cross-talk in dB} = 20\log|S_{31}| \tag{2.25c}$$

where port 1 and port 2 are directly connected to the device under test and port 3 is the end of another device where the cross talk is measured.

2.3.2 ABCD matrix

The ABCD matrix is useful for calculating a microwave network of cascaded networks. The cascaded network is easily found by multiplying the ABCD matrices of the individual networks. The impedance and the scattering matrices can represent single microwave devices but they do not cascade. However, in practice many microwave networks consist of a cascaded connection of several networks.

The ABCD matrix is defined for a two-port network as:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \tag{2.26}$$

and the cascading of two networks (Figure 2.13) is given by

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \begin{bmatrix} V_3 \\ I_3 \end{bmatrix} \tag{2.27}$$

There other ways to define this ABCD matrices by changing the sign of the currents, I am following the convention presented in [1].

The ABCD matrix representation of some elementary two-port networks that are useful in this research are shown in Figure 2.14. A uniform transmission line (Section 2.2.2) can be represented with a ABCD matrix. This make it easy to model

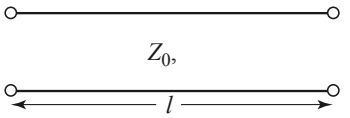
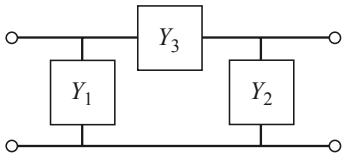
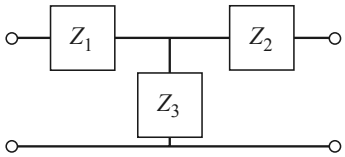
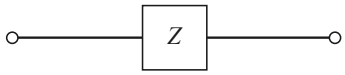
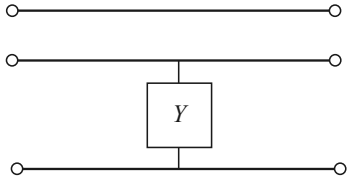
Circuit	*ABCD* Parameters	
	$A = \cosh \gamma l$ $C = \frac{1}{Z_0} \sinh \gamma l$	$B = Z_0 \sinh \gamma l$ $D = A$
	$A = 1 + \frac{Y_2}{Y_3}$ $C = Y_1 + Y_2 + \frac{Y_1 Y_2}{Y_3}$	$B = \frac{1}{Y_3}$ $D = 1 + \frac{Y_1}{Y_3}$
	$A = 1 + \frac{Z_1}{Z_3}$ $C = \frac{1}{Z_3}$	$B = Z_1 + Z_2 + \frac{Z_1 Z_2}{Z_3}$ $D = 1 + \frac{Z_2}{Z_3}$
	$A = 1$ $C = 0$	$B = Z$ $D = 1$
	$A = 1$ $C = Y$	$B = 0$ $D = 1$

Figure 2.14: ABCD Parameters of some circuits used in this research. Based on [1].

a non-uniform transmission line as a cascading of uniform transmission lines by multiplying their corresponding ABCD matrices. The π-network and the T-network also have straightforward representations as ABCD matrices. This is useful since both of these networks can represent a general reciprocal network. The ABCD matrices of a single series impedance or singe shunt admittance are used in the thru-only de-embedding procedure used and developed in this research (Section 2.4.1).

The ABCD parameters and the scattering parameters are related by

$$S_{11} = \frac{A + B/Z_0 - CZ_0 - D}{A + B/Z_0 + CZ_0 + D} \tag{2.28a}$$

$$S_{12} = \frac{2(AD - BC)}{A + B/Z_0 + CZ_0 + D} \tag{2.28b}$$

$$S_{21} = \frac{2}{A + B/Z_0 + CZ_0 + D} \tag{2.28c}$$

$$S_{22} = \frac{-A + B/Z_0 - CZ_0 + D}{A + B/Z_0 + CZ_0 + D} \tag{2.28d}$$

and the inversion gives

$$A = \frac{(1 + S_{11})(1 - S_{22}) + S_{21}S_{12}}{2S_{21}} \tag{2.29a}$$

$$B = Z_0 \frac{(1 + S_{11})(1 + S_{22}) - S_{21}S_{12}}{2S_{21}} \tag{2.29b}$$

$$C = \frac{1}{Z_0} \frac{(1 - S_{11})(1 - S_{22}) - S_{21}S_{12}}{2S_{21}} \tag{2.29c}$$

$$D = \frac{(1 - S_{11})(1 + S_{22}) + S_{21}S_{12}}{2S_{21}} \tag{2.29d}$$

These microwave networks will next be used to describe an arbitrary microwave discontinuity.

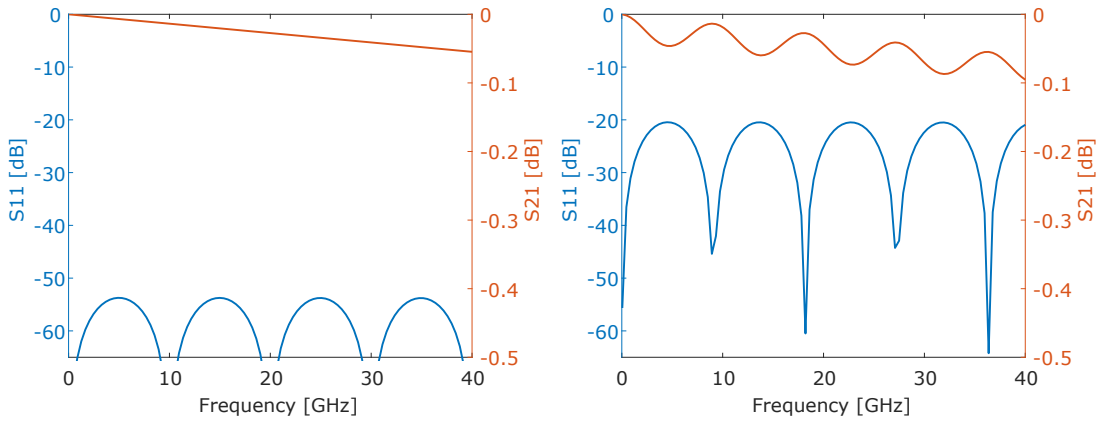
2.3.3 Discontinuities

A microwave discontinuity is a circuit that does not have a uniform cross-section like a transmission line. Another important assumption is that the discontinuity is reciprocal. That is, the discontinuity is a circuit that does not contain any active devices, ferrites or plasmas. The reciprocity of the microwave networks discussed previously is expressed as:

$$S_{ij} = S_{ji} \tag{2.30a}$$

$$AD - BC = 1 \tag{2.30b}$$

The π-network and the T-network shown in Figure 2.14 have the property of being unconditionally reciprocal (i.e. they always comply with Equation 2.30b). This



(a) Almost matched (b) Mismatched

Figure 2.15: The effect of a mismatch in a frequency sweep of S_{21} and S_{11}.

property means that a π-network and the T-network can be always recovered from any reciprocal scattering matrix. But of course the values of Z_1, Z_2 and Z_3, or Y_1, Y_2 and Y_3, are in general frequency dependant and thus not always easily representable by standard resistive, inductive and capacitive circuit elements.

The vector fitting algorithm is a useful way to represent these frequency dependant elements [24]–[26]. This algorithm is available through the *Matrix fitting toolbox*. The idea of the vector fitting algorithm is to represent the impedance by a summation of poles in the Laplace space. That means the algorithm calculates the complex coefficients c_{xyn} and a_n that best represent the impedance $Z(s)$ by:

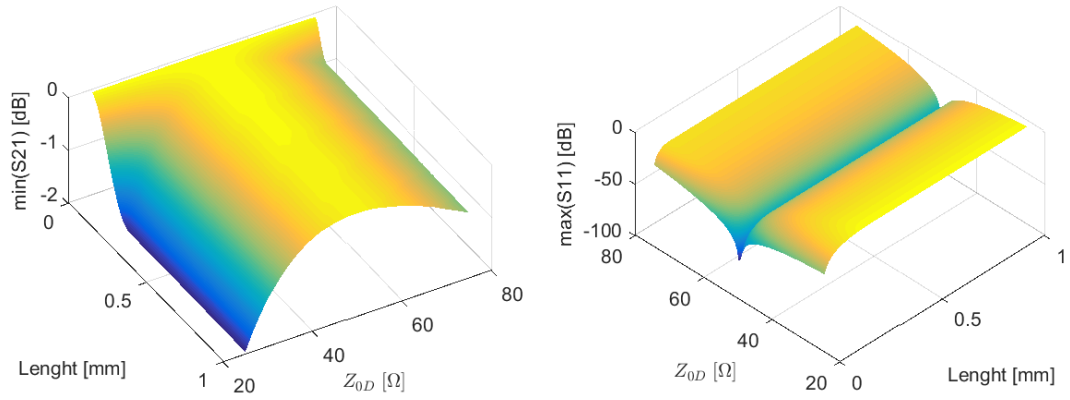
$$Z(s) = \sum_{n \in N} \frac{c_{xyn}}{s - a_n} \tag{2.31}$$

where $s = \sigma + j2\pi f$. Thus the frequency dependency can be reconstructed by setting $\sigma = 0$. The coefficient c_{xyn} and a_n are then represented by standard circuit elements by using the procedures explained in [27]–[29]. The circuit elements calculated this way can be used in standard circuit simulators but are not physically realizable since they include negative resistances and reactances, even when the representation is generally passive.

As an example, the simplest discontinuity is a piece of transmission line with impedance Z_{0D} and length l. In this case, we can use the model of the transmission lines in Figure 2.14 and substitute in Equations 2.28a and 2.28c to obtain

$$S_{11} = \frac{\frac{1}{2}\left(\frac{Z_0}{Z_{0D}} - \frac{Z_{0D}}{Z_0}\right)\sinh(\gamma l)}{\cosh(\gamma l) + \frac{1}{2}\left(\frac{Z_0}{Z_{0D}} + \frac{Z_{0D}}{Z_0}\right)\sinh(\gamma l)} \tag{2.32a}$$

$$S_{21} = \frac{1}{\cosh(\gamma l) + \frac{1}{2}\left(\frac{Z_0}{Z_{0D}} + \frac{Z_{0D}}{Z_0}\right)\sinh(\gamma l)} \tag{2.32b}$$



(a) (b)

Figure 2.16: The effect of a mismatch in a frequency sweep of S_{21} and S_{11}.

where Z_0 is the termination impedance at both ends and Equation 2.32a is equivalent to Equation 2.17 as expected. The graphs in Figure 2.15 were calculated with these equations for a matched line ($Z_0 \approx Z_{0D}$) shown in Figure 2.15a and for a mismatched line ($Z_0 = 50\,\Omega$ and $Z_{0D} \approx 55\,\Omega$) shown in Figure 2.15b. The comparison shown in Figure 2.15 illustrates that the effect of a mismatch is to increase S_{11} (also called return loss) and decrease periodically the S_{21} (Transmission). Figure 2.16 shows the effect of the discontinuity's length l and impedance Z_{0D} in the minimum S_{21} and the maximum S_{11}. The impedance mismatch clearly deteriorates the transmission and increases the return loss. A short discontinuity has almost no effect in the transmission thus highlighting the importance of shortening any discontinuity.

In summary, Section 2.3 described the concept of a microwave network and several matrices that can be used to characterise the function of arbitrary microwave devices. These matrices are used to describe the transmission lines and vertical transitions described in the next chapters.

2.4 Microwave measurements

This section discusses the techniques used for making measurements in this research. First, Section 2.4.1 discusses the VNA, which is the instrument used to get the frequency-domain measurements. Section 2.4.2 discusses the digital communication analyser (DCA), which is the instrument used to get the time-domain measurements. Finally, Section 2.4.3 discusses an algorithm used in this research to extract the material microwave properties from the frequency-domain measurements.

2.4.1 Vector Network Analyser (VNA)

The VNA measures the scattering matrix of a microwave network. A VNA is a microwave transceiver designed to process the magnitude and phase of the transmitted and reflected waves from the device under test (DUT) coming from a known incident wave. The incident wave is swept over a frequency range and thus the response of the devices in that frequency range is obtained. The incident, the reflected, and the transmitted waves are sampled and distinguished using directional couplers. Standard switches allow the VNA to drive the DUT from any port. Super-heterodyne receivers are used to lock the reflected and transmitted frequency with the incident (source) signal. An internal computer is used to calculate and display the magnitude and phase of the scattering parameters.

An important feature of the VNA is the ability to remove errors caused by mismatches, imperfect directivity, loss, and other parasitic phenomena. The procedure to remove these parasitic responses is called a calibration. The calibrations used to characterize planar microwave devices are usually performed in two steps [30]. These steps are often referred to as "tiers" of the calibration.

The first-tier calibration is usually an off-wafer probe-tip calibration. That means that the first-tier calibration is performed on a commercial calibration substrate that contains standards. These commercial calibration standards are usually fabricated by plating gold contacts and conductors on an alumina substrate, which ensures robust calibration standards and good contact repeatability. This first-tier calibration moves the measurement reference plane to the probe tips. The first-tier calibration used in this research is the short-open-load-thru (SOLT) calibration. The SOLT calibration is the default in the software used to control the VNA (WinCal), but has two problems: First, it is based on a standard circuit model of the calibration structures that do not hold at high frequencies [30], [31]. Second, the SOLT calibration does not account for the probe pads in our real device. In order to compensate for these two problems, a second-tier calibration is performed.

The second-tier aims to extract the parasitic phenomena left from the first-tier calibration. These two-tier parasitic-extraction calibrations are intended to move the calibration reference plane from the probe tips to the DUT. The most frequently used algorithm for this case is the thru-reflect-line (TRL). A few useful techniques around the TRL calibration can be found in [30], [32], [33]. In this research, a novel calibration called the thru-only method is used.

Thru-only calibration. The thru-only calibration is a de-embedding technique similar to the TRL calibration [34]–[39]. The thru-only calibration is less complex than TRL but also less general. It is less complex than the TRL since it only needs a thru standard and thus does not need a reflection standard or a line. The thru-only calibration is less general than the TRL calibration since it is only valid if the pads or fixture on the left are an identical, inverted version of the pads in the right (Figure 2.17).

There are multiple possible representation of the pads in the thru element (Fig-

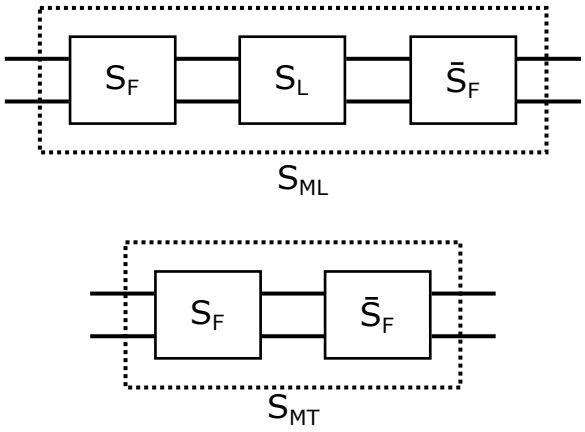
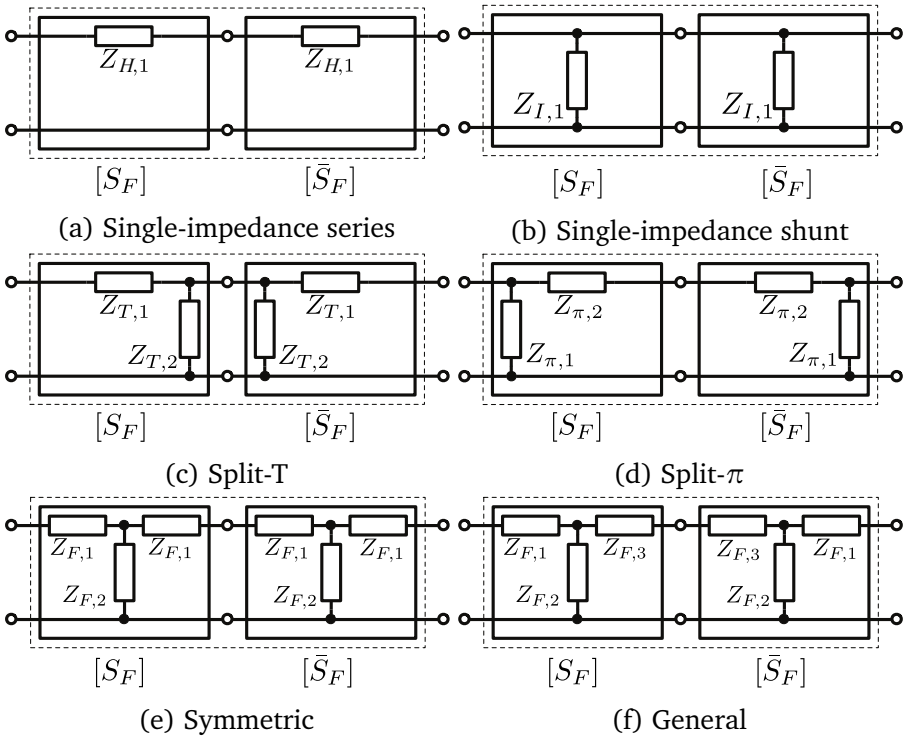


Figure 2.17: The measurements that are needed in the thru-only calibration and the model to be extracted.



(a) Single-impedance series (b) Single-impedance shunt

(c) Split-T (d) Split-π

(e) Symmetric (f) General

Figure 2.18: The possible representations of the thru element.

ure 2.18). The general representation uses three impedances in a T-network (Figure 2.18f) or could also use a *pi*-network configuration. This model can represent any reciprocal network, however, it is not possible to calculate the three impedances with only the thru measurement. It is not possible because there are three unknown complex numbers and only two equations since the thru measurement is symmetric and reciprocal, and thus only provides two uncorrelated complex numbers of information. That is why three models that consist of only two impedances have been used [34]–[38]. Three options are available using two impedances: assuming the pad is symmetric (Figure 2.18e), assuming a split-π network (Figure 2.18d) or assuming a split-T network (Figure 2.18c). These three representations have mathematical solutions, however, they might not represent the pad correctly. Also, it is not possible to know which of the three representations is closer to the real pad with only the thru measurement. In this research, a novel algorithm that uses the single-impedance representations has been developed.

The new single-impedance thru-only de-embedding (Appendix A.2.1) is based on the fact that the measurement of a thru element that is formed by single-impedance circuits (i.e. Figures 2.18a and 2.18b) can be distinguished from any other of the representations in Figure 2.18. In the case of the single-impedance as a series impedance ($Z_{H,1}$)

$$[A_{MT}] = \begin{bmatrix} 1 & 2Z_{H,1} \\ 0 & 1 \end{bmatrix} \tag{2.33}$$

and in the case of the single-impedance as a shunt admitance

$$[A_{MT}] = \begin{bmatrix} 1 & 0 \\ 2Y_{I,1} & 1 \end{bmatrix} \tag{2.34}$$

where $Y_{I,1}$ is the admittance that corresponds to the impedance $Z_{I,1}$ in Figure 2.18b and $[A_{MT}]$ is the ABCD matrix of the measured thru element. Based on these matrices, if $A_{MT} = D_{MT} \approx 1$ and $C_{MT} \approx 0$ for the measured thru then the single-impedance as a series impedance is valid and if $A_{MT} = D_{MT} \approx 1$ and $B_{MT} \approx 0$ then the single-impedance as a shunt impedance is valid, and the ABCD matrix for the pad is straightforward to calculate. This idea has been implemented in an algorithm programmed in MATLAB (Appendix A.2.1) together an implementation of the symmetric pad representation based on the sqrtm function in MATLAB.

A short pad can be represented as a single-impedance as the results in Section 5.2.1 will show. This explains the counter intuitive results found in [37] where a thru-line procedure based on the assumption of a single-impedance as a shunt impedance ([39]) presents better results than assuming a more complex split-π or split-T representation. However, measuring a very short pad is a challenge since having the probes too close will capacitively couple the signal through the air. However, using a line ($[A_L]$), and a second line that has exactly double the length of the first one ($[A_{2L}]$), both including the short pads; the measured thru ($[A_{MT}]$) can be calculated by [40]

$$[A_{MT}] = [A_L][A_{2L}]^{-1}[A_L] \tag{2.35}$$

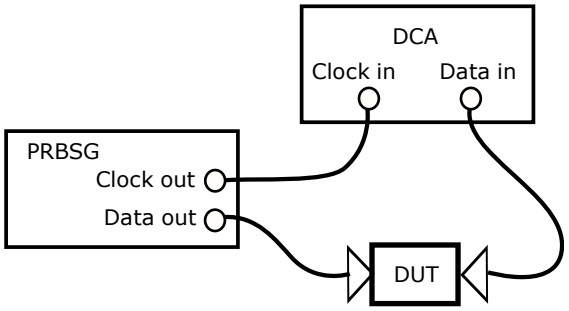


Figure 2.19: The time-domain test set-up. A pseudorandom binary sequence generator (PRBSG) and a DCA are used to obtain the eye pattern. The triangle represents high-speed probes.

2.4.2 Digital communication analyser

A DCA and a PRBSG was used to measure the time-domain response of our devices (Figure 2.19). The PRBSG is used to generate a pseudorandom binary sequence (PRBS). Our PRBSG is able to work at a maximum data rate of 44 Gbit s^{-1}. A clock signal with the same frequency of the sequence is also sent to the DCA. This clock signal is used by the DCA to lock the pattern and superpose multiple traces to generate the eye diagram.

An eye diagram is a tool for the evaluation of the combined effects of channel noise and the general characteristics of the communication channel. An eye diagram is the visual representation of the superposition of multiple traces of a bit pattern. By superposing enough bits, the eye diagram represents visually the quality of all possible three-bit patterns of the signal of interest. It is called eye diagram because, for several types of coding, the pattern looks like a series of eyes between a pair of rails (Figure 2.20).

The DCA measurement is a test that is closer to a real communication channel, and thus to a functional test, than the VNA. For that reason, the effect of a frequency-domain feature from the scattering parameters (S-parameters) of a device in the eye diagram is of interest [41]. In order to calculate the effect of given measured or simulated scattering parameters (S-parameters) in the eye diagram, an eye diagram simulator is used, which is explained in Section 2.5.3.

2.4.3 Transmission line performance extraction

This section presents a novel algorithm (Appendix A.2.2) that is a based on a new set of equations that calculate the characteristic impedance (Z_0) and the complex propagation constant (γ) from VNA measurements of long lines.

There are several ways that the Z_0 and the complex propagation constant (γ) can be calculated from VNA measurements [39], [42]–[52]. The most used algorithm starts by calculating the $ABCD$ matrix from the scattering matrix by Equation 2.29. Based on the model in Figure 2.14 the characteristic impedance Z_0 and the complex

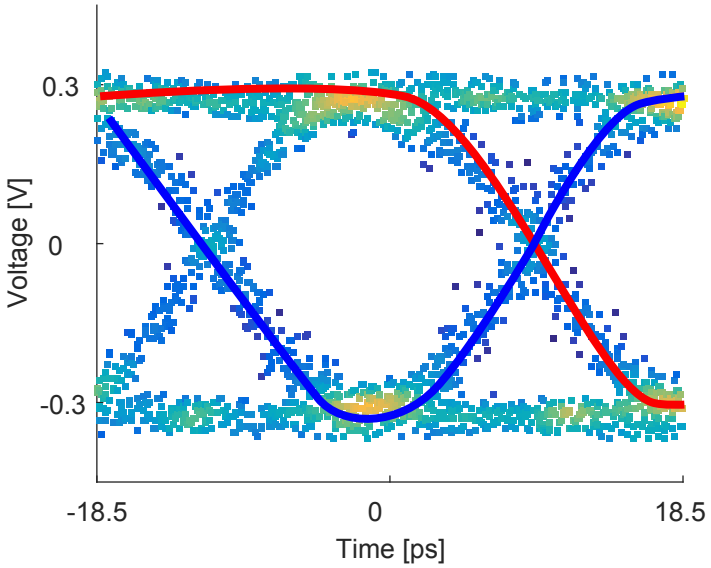


Figure 2.20: An example of an eye diagram. The red line shows a "110" pattern and the blue line a "101".

propagation constant γ are obtained by:

$$Z_0 = \sqrt{\frac{B}{C}} = \sqrt{\frac{Z_0 \sinh \gamma l}{\frac{1}{Z_0} \sinh \gamma l}} \tag{2.36a}$$

$$\gamma = \frac{\operatorname{acosh} A}{l} = \frac{\operatorname{acosh} (\cosh \gamma l)}{l} \tag{2.36b}$$

However, these equations have two problems. The first problem is that Equation 2.36a is the division of two small numbers when $\sinh \gamma l \approx 0$ and this creates periodic parasitic features as can be seen in [48], [52] and in the results presented in Chapters 5 and 6 if the line is long. This problem is avoided if the measured or de-embedded line is short, but by mistake that was not our case. The second problem is that $\operatorname{acosh} z$, used in Equation 2.36b, is a multivalued function. Numerically, $\operatorname{acosh} z$ is calculated by $\operatorname{acosh} z = \log\left(z + \sqrt{z^2 - 1}\right)$ but the negative square is also a solution. This creates problems like the ones discussed in [45].

In order to deal with these two problems, a novel algorithm (Appendix A.2.2) has been completed based on the next set of equations

$$\gamma = \frac{1}{l} \ln\left(A + \left|\sqrt{BC}\right| \exp(i(\arg BC)/2)\right) \tag{2.37a}$$

$$Z_0 \approx \left(B + \frac{\partial B}{\partial \gamma l}\right) \exp(-\gamma l) \tag{2.37b}$$

based on the idea that

$$\ln\left(A + \left|\sqrt{BC}\right| \exp(i(\arg BC)/2)\right) = \ln(\sinh \gamma l + \cosh \gamma l) = \ln(\exp(\gamma l)) \tag{2.38a}$$

$$\frac{\partial B}{\partial \gamma l} = \frac{\partial Z_0}{\partial \gamma l}\sinh\gamma l + Z_0\cosh\gamma l \approx Z_0\cosh\gamma l \tag{2.38b}$$

since for our lines $(\partial Z_0/\partial \gamma l)\sinh\gamma l \approx 0$.

Once Z_0 and γ have been calculated, the $RLGC$ are obtained by stating Equations 2.12c and 2.13c as:

$$R = \mathrm{Re}\{Z_0\gamma\} \tag{2.39a}$$

$$L = \frac{1}{\omega}\mathrm{Im}\{Z_0\gamma\} \tag{2.39b}$$

$$G = \mathrm{Re}\left\{\frac{\gamma}{Z_0}\right\} \tag{2.39c}$$

$$C = \frac{1}{\omega}\mathrm{Im}\left\{\frac{\gamma}{Z_0}\right\} \tag{2.39d}$$

Summarising, Section 2.4 presented the VNA and the DCA that are used to measure the devices designed and fabricated in this thesis. Also, this section presented the thru-only calibration which is the second-tier calibration used in the measurements of the devices designed in this thesis. Finally, the algorithm to extract the material microwave properties of the fabricated boards was presented.

2.5 Electromagnetic simulators

This section presents information needed to understand the electromagnetic simulators used in this research. Section 2.5.1 discusses the 2D cross-sectional simulator used to design the transmission lines from Chapter 3. Section 2.5.2 discusses the 3D full-wave electromagnetic simulator used to design the vertical transition as discussed in Chapter 4.

2.5.1 2D cross-sectional simulator

The 2D cross-sectional simulator (ANSYS 2D Extractor) computes $RLGC$ circuit parameter matrices for any arbitrary multi-conductor transmission line. Once computed, these circuit parameters can then be transformed into a SPICE circuit that can be incorporated into a system to analyse its impact on signal integrity. This section outlines the technical aspects of the general procedure used by 2D Extractor to generate an equivalent circuit for a transmission line.

The 2D cross-sectional simulator is based on two assumptions: First, the transmission line is quasi-TEM. Second, the transmission line has a uniform cross-section along its length. The software requires the user to draw the cross section, identify which objects are signal lines, ground lines, and floating conductors, specify object materials and specify boundary conditions. The simulation procedure is simplified in the next steps:

1. Solve the fields
2. Refine the mesh iteratively with the first point
3. Calculate the $RLGC$ parameters
4. Calculate the modal solution

There are two field solvers used by the 2D cross-sectional simulator. The first calculates the electric field $\vec{\mathbf{E}}$ by taking the divergence of Equation 2.2b and solving that equation for $\vec{\mathbf{E}}$. The magnetic field $\vec{\mathbf{H}}$ is then solved by using a procedure based on [53].

The mesh refinement is done iteratively with the field solver. An initial mesh is assumed and, after the first field solutions are completed, the simulator refines the mesh and solves the field again. The simulator calculates the error between the original mesh and the refined mesh in each triangle. The triangles with the highest error are divided into smaller triangles in order to produce a more accurate solution.

The $RLGC$ parameters are calculated in two parts, first, the G and C parameters are calculated and then the R and L parameters. The G and C parameters are calculated by applying sequentially 1 V to each conductor in the model while setting the rest of the conductors to 0 V. The R and L parameters are calculated by applying 1 A sequentially through each conductor in the model while setting the current through the rest of the conductors to 0 A. As each conductor is excited, the field solution is used to compute the $RLGC$ parameters for that conductor relative to the reference ground and to the other conductors by Equation 2.11. The results are entered in matrix format.

A modal solution of voltage and current modes are computed from the $RLGC$ matrices. It is convenient to define per-unit-length impedance $[Z(j\omega)]$ and admittance matrices $[Y(j\omega)]$ as

$$[Z(j\omega)] = [R(j\omega)] + j\omega[L(j\omega)] \tag{2.40a}$$
$$[Y(j\omega)] = [G(j\omega)] + j\omega[C(j\omega)] \tag{2.40b}$$

then Equation 2.12a becomes

$$\frac{\mathrm{d}^2[v(z)]}{\mathrm{d}z^2} - [Z][Y][v(z)] = 0 \tag{2.41}$$

where $[v]$ represents a vector with the voltage at each of the conductor terminals in our transmission line. It can be demonstrated that the eigenvalues of $[Z][Y]$ represent the complex propagation constants of the modes propagating in the transmission lines. The characteristic impedance vector $[Z_0]$ is then obtained by

$$[Z_0] = [Z][T][\Gamma]^{-1}[T]^{-1} \tag{2.42}$$

where the calculation of $[T]$ and $[\Gamma]$ is explained in [54], [55].

2.5.2 3D Full-wave simulator

The 3D full-wave simulator used in this research is *ANSYS HFSS*, which is able to solve both in the frequency-domain and in the time-domain. First, the frequency-domain simulator is explained. The time-domain models and the frequency-domain model share the boundary conditions and the excitation field (port) definitions.

Boundary conditions. Boundary conditions specify the field behaviour on the surfaces of the problem region and the object interfaces. The boundary types available are perfect E boundaries, impedance boundaries, radiation boundaries, and perfectly matched layers (PML) boundaries. The perfect E boundary represent perfectly conducting surfaces in a structure. Impedance boundaries represent surfaces of known impedance. The radiation boundary condition should be a "transparent" condition. In other words, it should not produce any unphysical reflection as a result of the artificial truncation. Radiation boundaries only absorb normal or near normal incident waves. Thus in order to produce accurate results, they must be placed sufficiently far away from any structure. The typical recommendation is at least a quarter wavelength from the radiating source. PML boundaries absorbs all outgoing waves by adding artificial material layers that are designed such that all of the incident waves impinging upon them are completely transmitted or absorbed with minimal reflections. Thus, PML boundaries can be placed closer than radiation boundaries. Furthermore, the PML boundary absorb a much wider range of waves in terms of frequency and direction whereas the radiation boundary absorbs only normally incident waves accurately. However, using PML boundaries, in general, makes it more difficult for the iterative solver to reach convergence compared to radiation boundaries.

Excitations. The excitations in the simulation model specify the sources of electromagnetic fields in the model. Two types of excitations are used in this research: wave ports and lumped ports. Wave ports are placed on the edge of the model to provide a window that couples the model device to the external world. The simulation assumes that each wave port is connected to a waveguide that has the same cross-section and material properties as the port. The simulator calculats the modes of these transmission lines. The 2D modes are used as boundary conditions for the 3D problem. A wave port is restricted to reside at an external boundary of a 3D problem. In contrast, lumped ports should be used when defining ports in the interior of a 3D domain. Lumped ports are restricted to single-mode ports and the scattering parameters are always based on the user-defined reference impedance. This is because the lumped port is interpreted as a measurement probe being connected to the surface of the lumped port with the reference impedance specified by the user. Lumped ports are very similar to high-speed probes and there is usually a need to de-embed parasitic couplings from the port to the desired measured device.

The frequency-domain simulations. The 3D full-wave simulator is based on the *Finite Element Method* (FEM). In general, the FEM divides the full problem space into thousands of smaller elements. This collection of tetrahedra is referred to as the mesh. The frequency-domain simulations used to calculate the scattering matrix associated with a structure is done following the next general steps:

1. Generate the mesh
2. Calculate ports' modes
3. Solve the fields
4. Compute the scattering matrix

The mesh generation follows the following procedure. First, an initial mesh is generated at the frequency of interest, usually the highest frequency but can also be a resonance frequency. Second, the simulator iteratively refines the 2D mesh at the ports. Third, the simulator computes the electromagnetic fields when the port is excited at the solution frequency. Fourth, the simulator estimates the regions of the problem domain where the exact solution has a large error and the mesh in these regions is refined. The simulator generates another solution using the refined mesh and recomputes the error. This procedure is repeated iteratively until the error converges. Finally, the simulator solves the problem at the other frequency points without further refining the mesh.

The excitation field pattern at each port must be calculated before the field inside a structure is calculated. The simulator calculates the modes that can exist inside a transmission line with the same cross-section as the port. The resulting 2D field patterns serve as boundary conditions for the full-wave 3D problem. A waveguide could support an infinite number of modes, however, the simulator uses a single mode. Any linear combination of these modes can exist in the waveguide so the user needs to specify the number of modes to be included in a wave port. In general, in order to obtain accurate scattering-parameters the number of modes defined for a given port should be the same or greater than the number of propagating modes at the highest frequency of interest. The modes included in a port are based on a sorting criteria to extract the dominant set of modes out of the infinite set of possible modes. If there is no prior knowledge to the number of propagating modes, the user can do a ports-only solution while specifying a reasonably large number of modes and view the γ values to determine what modes are propagating. The field pattern of a travelling wave inside a waveguide can be determined by solving Maxwell's equations. The excitation field pattern computed by the port solver is valid only at a given frequency. A different excitation field pattern is computed for each frequency of interest. The port solver performs an iterative refinement of the triangular mesh. This procedure to calculate the excitation fields in the ports is based on [56]. This procedure is distinct from the 2D cross-sectional simulator discussed in Section 2.5.1. A problem with the port-solver in the 3D full-wave simulator is that it forces the boundaries conditions to be Perfect-E at 0 V which means that the boundaries of the port are grounded.

The simulator solves for $\vec{\mathbf{E}}$ using Equation 2.3a, subject to excitations and boundary conditions and then $\vec{\mathbf{H}}$ is calculated using Equation 2.2a. The solver uses the procedure explained in [57] to convert Equation 2.3a into a matrix of the form:

$$[A][x] = [b] \tag{2.43}$$

where $[A]$ is a known matrix that has the information of the boundary conditions and $[b]$ contains the information of the port excitations. Solving for $[x]$ gives $\vec{\mathbf{E}}$. The matrix is solved by using Gaussian elimination, which uses elementary matrix operations to compute the solution but the solver includes an iterative method based on [58].

The scattering matrix is obtained from the solved electric and magnetic fields. *ANSYS HFSS* uses the next equation

$$E(x,y) = \sum_{m=1}^{M} (a_m + b_m) e_m(x,y) \tag{2.44}$$

where $E(x,y)$ is the field that resulted from the FEM and e_m is the field obtained with the port solver. The simulator calculates the complex amplitudes a_m and b_m with an undisclosed algorithm. The scattering parameter S_{ij}, specifies the multiplication factor to be applied to the incident modal amplitude a_j to get the reflected/transmitted modal amplitude b_i given that all the other input modes are turned off. This can be described mathematically as:

$$S_{ij} = \left. \frac{b_i}{a_j} \right|_{a_k=0, k\neq j} \tag{2.45}$$

where the recovered scattering parameter is not normalized. To re-normalise a generalised scattering matrix to a specific impedance, a unique impedance matrix $[Z]$ is calculated by:

$$[Z] = \sqrt{[Z_0]}([I]-[S])^{-1}([I]+[S])\sqrt{[Z_0]} \tag{2.46}$$

where $[S]$ is the calculated scattering matrix, $[I]$ is the identity matrix. $[Z_0]$ is a diagonal matrix having the characteristic impedance (Z_0) of each port as a diagonal value. The renormalized scattering matrix is then calculated from the unique impedance matrix using this relationship:

$$[S_\Omega] = \sqrt{[Y_\Omega]}([Z]-[Z_\Omega])^{-1}([Z]+[Z_\Omega])\sqrt{[Z_\Omega]} \tag{2.47}$$

where $[Z]$ is the structure's unique impedance matrix. Z_Ω and Y_Ω are diagonal matrices with the desired impedance and admittance as diagonal values.

The time-domain simulations. The time-domain simulator is a Discontinuous Galerkin Time Domain (DGTD) type, based on the Discontinuous Galerkin [59] family of numerical methods. For the DGTD the modal port solution is provided by the same 2D port solver as is used in the frequency-domain solver. However, if a lossy dielectric or a non-perfectly conducting metal is part of the port, the port impedance will be frequency dependent and the simulation cannot be completed. In the desings in this thesis, this means that a lumped port must be used.

2.5.3 Eye diagram simulator

This section explains the time-domain simulations used to calculate the eye diagrams from a frequency-domain response, which is usually the scattering parameters (S-parameters) for a frequency sweep obtained by measurement or simulations. These simulations are done by the *QuickEye* package in the circuit simulator in *ANSYS Electronics Desktop*. This eye diagram simulations are very useful to assess the effect of the features of the scattering parameters (S-parameters) in the eye diagram.

The fundamental assumption in *QuickEye* is that the channel is a linear time-invariant (LTI) system. Therefore, the system can be characterized by its response, called the transfer function ($h(t)$), to a Dirac delta function input or by its response ($u(t)$) to a Heaviside step function. The transfer function in the Laplace domain $H(s)$ corresponding to $h(t)$ can be calculated from the scattering parameters (S-parameters) by [60]

$$H(s) = \frac{S_{21}(1-\Gamma_l\Gamma_s)}{1-\Gamma_s S_{11}-\Gamma_l S_{22}+\Gamma_l\Gamma_s|[S]|} \tag{2.48}$$

$$\Gamma_l = \frac{Z_l - Z_0}{Z_l + Z_0} \tag{2.49}$$

$$\Gamma_s = \frac{Z_s - Z_0}{Z_s + Z_0} \tag{2.50}$$

where Z_s is the input source impedance and Z_l is the output load impedance.

QuickEye uses the principle of superposition which allows solving the time domain problem by convolution. The eye diagram simulator has three main stages. First, the rising and falling step responses are calculated. Second, these responses are super-positioned to reconstruct a PRBS. Third, the eye diagram is constructed by overlaying pieces of the reconstructed PRBS.

In the first stage, *QuickEye* convolutes a linearly raising input ($x(t)$) to the system transfer function to calculate the step responses for rising and falling edges ($y(t)$) with the time derivative of the input waveform.

$$y(t) = x(t) * h(t) = x(t) * \frac{\mathrm{d}u(t)}{\mathrm{d}t} \tag{2.51}$$

with inputs defined by

$$x_{\text{rise}}(t) = \begin{cases} 0 & t \leq 0 \\ \frac{1}{t_{\text{rise}}} t & 0 \leq t \leq t_{rise} \\ 1 & t \geq t_{rise} \end{cases} \tag{2.52}$$

$$x_{\text{fall}}(t) = \begin{cases} 1 & t \leq 0 \\ 1 - \frac{1}{t_{\text{fall}}} t & 0 \leq t \leq t_{fall} \\ 0 & t \geq t_{fall} \end{cases} \tag{2.53}$$

In the second stage, *QuickEye* creates the PRBS waveform by superposing the calculated rising and falling step responses. *QuickEye* superposes one response for each transition in the corresponding transitions of a perfectly squared PRBS with each response located in the position of the corresponding transitions of a perfectly squared PRBS. In this way, a waveform as long as the requested PRBS is created.

Finally, in the third stage, *QuickEye* overlays the bits from the calculated long waveform to generate the eye diagram. For a given set of data, the *QuickEye* convolution algorithm is faster than full transient analysis.

In conclusion, Section 2.5 presented information on the 2D and 3D electromagnetic simulations used in the next chapters. The simulation models, explained in this section, consist of the geometry, the mesh, the boundaries condition and the excitations. These are the elements that are needed to understand the next chapters.

Chapter 2 presented the methodology used for the microwave design of the structures in this research. The theoretical basis for the electromagnetic simulators used in this research is Maxwell's equations. The electromagnetic simulators were described in detail; each part of the simulation has been discussed so the simulations presented in the next chapters can be understood. The *RLGC* model is used to describe the transmission lines and an improved TDR algorithm has been created to represent transitions as non-uniform lossless transmission lines. The general microwave network concept is presented including the improved Thru-only de-embedding algorithm. Finally, the microwave measurements used to measure the fabricated boards are discussed.

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Chapter 3
The design of the transmission lines

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This chapter presents the work done to design the multi-layer transmission lines to be used as interposers for the packaging of photonic integrated circuits (PICs). The general theory behind transmission lines has been presented in Chapter 2 and this chapter focuses on the results of the simulations from the electromagnetic solvers. The chapter starts in Section 3.1 with a discussion about the different planar waveguides and the reasoning in choosing conductor backed co-planar waveguide (CB-CPW)

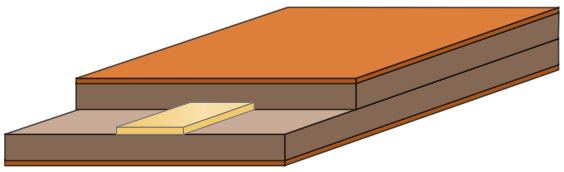


Figure 3.1: A schematic of the stripline. The stripline is a metal strip between two ground metals surrounded by a dielectric material. Courtesy Spinningspark at Wikipedia.

and shielded multi-layer co-planar waveguide (SM-CPW). Then, Section 3.2 presents the work done to design CB-CPWs and SM-CPWs that have low-loss and a 50 Ω characteristic impedance. Both CB-CPWs and SM-CPWs use ground vias to connect the grounds at the different levels and Section 3.3 discusses the effect of these ground vias on the signal integrity. The ground vias also help to reduce the crosstalk between channels. Finally, Section 3.4 presents other transmission lines that were developed during this research.

3.1 Planar waveguides

Planar waveguides are transmission lines with conductors that are flat. They are used to interconnect components at microwave frequencies because the planar format fits in well with the manufacturing methods for these components. There are several options for planar waveguides. The most common options are stripline, microstrip, slotline and co-planar waveguide (CPW). This section discusses and compares the main characteristics of these options.

3.1.1 Stripline

Stripline is a strip conductor embedded in a dielectric between two ground planes, shown in Figure 3.1. It is usually constructed as two sheets of dielectric clamped together with the stripline pattern on one side of one sheet. The characteristic impedance can be tuned by changing the substrate thickness or the width of the signal line giving a typical range of 40 Ω to 130 Ω. The quality factor for the stripline is high because the effective dielectric constant is high since there is no air. The main advantage of stripline is that transmission is purely in the TEM mode and is free of dispersion at least for frequencies below the cut-off for the substrate modes. The main disadvantage is that it is not as easy as microstrip to mount components. For any that are incorporated, cut-outs have to be provided in the dielectric and they are not accessible once assembled.

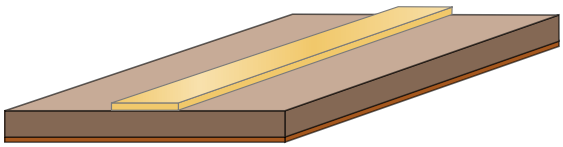


Figure 3.2: A schematic of the microstrip. The microstrip is a strip conductor on the top surface of a dielectric substrate and a ground plane on the bottom surface. Courtesy Spinningspark at Wikipedia.

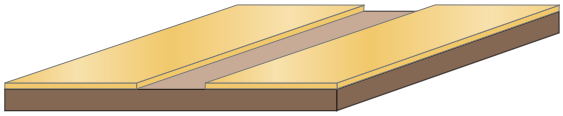


Figure 3.3: A schematic of the slotline. The slotline is a slot cut in the metallization on top of the substrate. Courtesy Spinningspark at Wikipedia.

3.1.2 Microstrip

Microstrip is a strip conductor on the top surface of a dielectric substrate and a ground plane on the bottom surface, as shown in Figure 3.2. The characteristic impedance can be tuned by changing the substrate thickness or the width of the sigal line giving a typical range of 25 Ω to 95 Ω. The quality factor is around 250 where most of the field is between the signal metal and the backside ground. The electromagnetic wave travels partly in the dielectric and partly in the air above the conductor resulting in quasi-TEM transmission. Thus, the dispersion of the high-order modes is usually not a problem in the microwave range and the dispersion is low. It is easy to integrate microstrip in series with other components, but making a shunt connection is hard because vias are needed to connect to the backside ground.

3.1.3 Slotline

A slotline is a gap in the metallization on top of the substrate, shown in Figure 3.3. The characteristic impedance can be tuned by changing the gap width or the signal width giving a range of 40 Ω to 130 Ω. The quality factor is around 100, the lowest of the planar waveguides because most of the field is in the air between the metals. The electromagnetic wave travels partly in the dielectric and partly in the air above the conductor resulting in quasi-TEM transmission. One of the disadvantages of the slotline is that both the characteristic impedance and the group velocity vary strongly with frequency, resulting in the slotline being more dispersive than the other options. The slotline makes it particularly easy to connect components to the line in shunt; surface mount components can be mounted bridging across the line. However, mounting in series is difficult because the line is unbalanced.

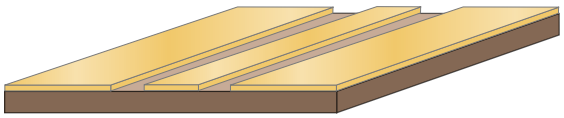


Figure 3.4: A schematic of the CPW. The CPW consists of a single signal metal on top of a dielectric substrate, together with a pair of ground conductors, one to either side of the track. Courtesy Spinningspark at Wikipedia.

3.1.4 Co-Planar waveguides (CPW)

A CPW consists of a single signal metal on top of a dielectric substrate, together with a pair of ground conductors, one to either side of the track (Figure 3.4). The characteristic impedance can be tuned by changing the signal width or the gap between the ground and the signal. This gives an impedance tuning range of typically 30 Ω to 140 Ω. The quality factor is around 150. The electromagnetic wave travels partly in the dielectric and partly in the air above the conductor resulting in quasi-TEM transmission. There is a second mode that has a zero frequency cut-off called the odd-mode. The odd-mode can be suppressed by bonding the two return conductors together. This can be achieved with a bottom ground plane and periodic ground vias, or periodic air bridges on the top of the board. CPW makes it particularly easy to connect components both in shunt or in series because the line is balanced.

The CPW offer several advantages over microstrip or stripline including ease of fabrication, reduced radiation losses, additional design room provided by the gap between the co-planar ground and signal metals, and ease of integration with mounted components. For example, CPWs have shown better performance than the microstrip lines at higher frequencies, when the radiation losses start to dominate [1]. Another example shows that CPW has better performance than microstrip lines for millimetre waves and that different usual discontinuities show less radiation in the CPW lines [2]. Furthermore, the size of the overall CPW lines are larger than the microstrip but the signal line width is smaller.

However, the use of CPW lines also presents additional challenges that are not present for microstrip or stripline. The CPW lines can support additional parasitic modes [3], [4]. For example, CPW allows for the excitation of the odd mode due to unequal ground metal widths [5]. Bends also excite this parasitic odd mode and thus air-bridges, ground vias or defected grounds are needed [6]. If the ground vias are used, the transmission line is called a CB-CPW. Recently the impact of the ground via placement on CB-CPW lines in the suppression of substrate and patch antenna modes has been presented [3]. But the effect of the ground via placement on the characteristic impedance of the line, the inter-channel crosstalk and the excitation of parasitic modes needs to be investigated. In this document, full wave simulations are used to study these effects not only on CB-CPW but also in SM-CPW lines, see Section 3.3.

Section 3.1 discussed the advantages and disadvantages of the most common planar waveguides. A summary of these advantages and disadvantages is provided

Table 3.1: Comparison of planar waveguides [7]

Type	Z_0 [Ω]	Q-factor	Dispersion	Component mount
Stripline	40 to 130	400	None	Hard for shunt, hard for series
Microstrip	25 to 95	250	Low	Hard for shunt, easy for series
Slotline	40 to 130	100	High	Easy for shunt, hard for series
CPW	30 to 140	150	Low	Easy for shunt, easy for series

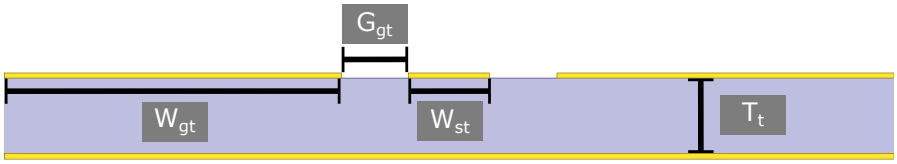


Figure 3.5: The CB-CPW geometry. The effect of five dimensions are studied; the ground width (W_{gt}), the gap width (G_{gt}), the signal width (W_{st}), the substrate thickness (T_t) and the metal thickness (T_{mt}).

in Table 3.1. The transmission lines chosen for our multi-layer interposers are CPWs because CPWs have a lower footprint (in an equal crosstalk situation) and better performance at higher frequencies and are therefore best for integration.

3.2 Design of the co-planar waveguides

This section presents the result of the simulations done to design the CPW lines for our multi-layer interposer. Two transmission lines are studied in detail; the CB-CPW and the SM-CPW (Figures 3.5 and 3.6). The materials are assumed to have frequency independen properties with values as shown in Table 3.2. The values for gold and air are the default values in *ANSYS EM Suite* and the low-temperature co-fired ceramic (LTCC) is based on the data sheet for Dupont™ 9K7, which provides the measured information at 10 GHz. The simulation frequency, whenever it is

Table 3.2: The materials properties used for the electromagnetic simulations. The values for gold and air are the defaults in the software. LTCC based on datasheet provided by supplier.

Material	ϵ_r	μ_r	σ [S m^{-1}]	$\tan\delta$
Gold	1.0	1.0	41×10^6	–
Air	1.0	1.0	–	0.0
LTCC	7.1	1.0	–	0.0015

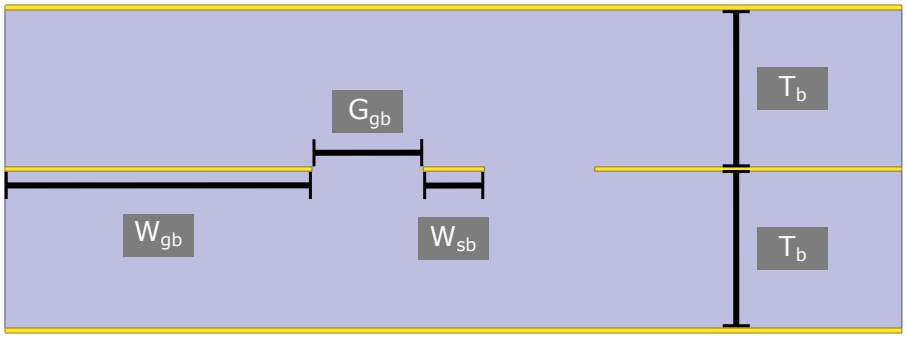


Figure 3.6: The SM-CPW geometry. The effect of five dimensions are studied; the ground width (W_{gb}), the gap width (G_{gb}), the signal width (W_{sb}), the substrate thickness (T_b) and the metal thickness (T_{mb}, not labelled).

Table 3.3: The starting point for the transmission line simulations.

(a) CB-CPW

	W_{gt}	G_{gt}	W_{st}	T_t	T_{mt}
[µm]	500	100	120	127	8

(b) SM-CPW

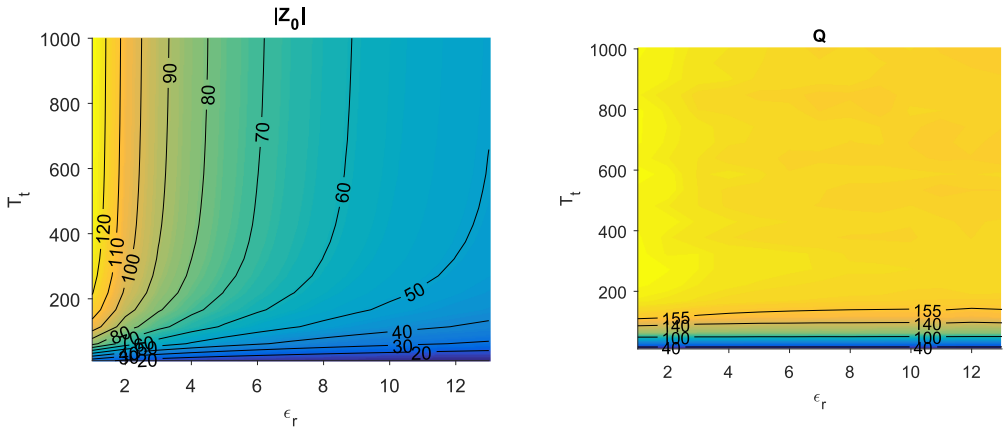
	W_{gb}	G_{gb}	W_{sb}	T_b	T_{mb}
[µm]	500	180	100	254	8

not specified, is 40 GHz. The effect of the substrate thickness and the substrate permittivity is discussed first in Section 3.2.1. Then, the effect of the signal and gap width are discussed in Section 3.2.2. Similarly, Section 3.2.3 discusses the effect of the metal width. Finally, the effect of the finite ground width is discussed in Section 3.2.4 These are the main parameters used to tune the transmission lines. The results are presented in two dimensional colormaps created by simulating 2000 designs, that is the equivalent to 22 h of computational time.

3.2.1 Substrate thickness and permittivity

In this section, the substrate thickness (T_t and T_b) and the permittivity are varied to calculate their effect on the characteristic impedance and the Q-factor. The geometric parameters are set initially to the values in Table 3.3 that are the values of the smallest 50 Ω transmission lines that can be fabricated. The substrate thickness is varied from 10 µm to 1000 µm and the permittivity from 1 to 13.

The characteristic impedance and the Q factor of the CB-CPW for several combinations of substrate width and permittivity are shown in Figure 3.7. For small substrate thickness (T_t) the characteristic impedance is insensitive to the substrate



(a) Characteristic impedance

(b) Q factor

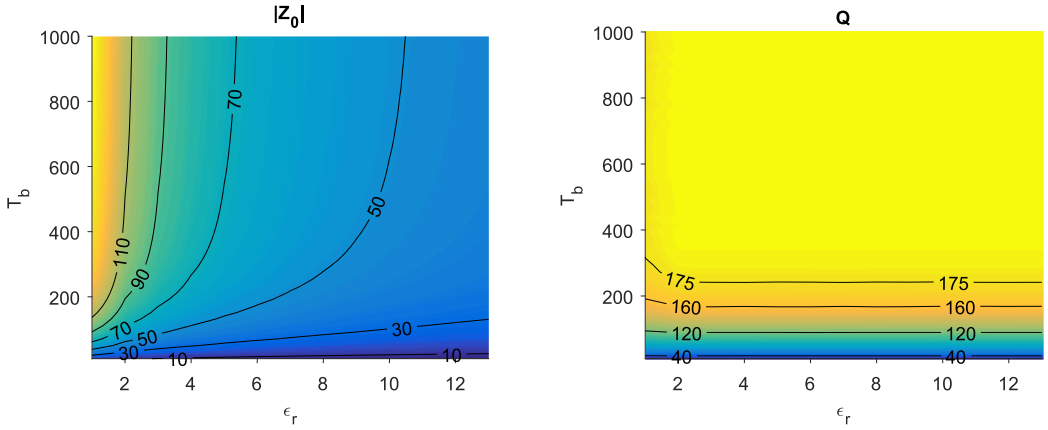
Figure 3.7: The characteristic impedance and the Q factor of the CB-CPW for several combinations of substrate width and permittivity. For small substrate thickness (T_t) the characteristic impedance is insensitive to the substrate permittivity. Above 200 µm thickness; the impedance does not change and is only affected by the permittivity. The Q factor is only affected by the thickness and reaches a maximum for thicknesses larger than 100 µm.

permittivity. In contrast, when T_t is larger than 200 µm the impedance does not change by increasing the thickness and it is only affected by the permittivity. This is because for substrates that are thick enough, the coupling to the backside ground is weak. Therefore, when the substrate thickness is high enough the mode converges to a standard CPW mode. The Q factor is only affected by the thickness and reaches a maximum for thicknesses larger than 100 µm. If the thickness is small the fields become concentrated around the metals and the loss is higher.

The characteristic impedance and the Q factor of the SM-CPW for several combinations of substrate width and permittivity are shown in Figure 3.8. For a small substrate thickness (T_b) the characteristic impedance is insensitive to the substrate permittivity. In contrast, when T_b is larger than 200 µm the impedance does not change by increasing the thickness and it is only affected by the permittivity. This is because for substrates that are thick enough, the coupling to the topside and backside grounds is weak. Therefore, when the substrate thickness is high enough the mode converges to an embedded CPW mode. The Q factor is only affected by the thickness and gets to a maximum for thicknesses larger than 300 µm. If the thickness is small the fields get concentrated around the metals and the loss is higher.

3.2.2 Gap and signal width

In this section, the gap width and the signal width are varied (G_{gt} and W_{st}, or G_{gb} and W_{sb}). These two variables are the main design parameters of our transmission lines. Since these are the main design parameters, additional results are given providing



(a) Characteristic impedance (b) Q factor

Figure 3.8: The characteristic impedance and the Q factor of the SM-CPW for several combinations of substrate width and permittivity. For small substrate thickness (T_b) the characteristic impedance is insensitive to the substrate permittivity; Above 200 µm thickness the impedance does not change and is only affected by the permittivity. The Q factor is only affected by the thickness and gets to a maximum for thicknesses larger than 300 µm.

four quantities that completely define the transmission line: $|Z_0|$, $\angle Z_0$, α and $\lambda_{\text{eff.}}$, where $\lambda_{\text{eff.}} = 2\pi/\beta$. The final design point is shown with a white dot in all the figures.

The results for the CB-CPW are shown in Figure 3.9. Figure 3.9a shows that $|Z_0|$ has a tuning range from 40 Ω to 90 Ω. Figure 3.9a also shows that the characteristic impedance becomes insensitive to the gap width for gap widths greater than the substrate thickness, due to the mode becoming very similar to the microstrip mode. Figure 3.9b shows that $\angle Z_0$ is very small, showing that Z_0 is mostly real. Figure 3.9c shows how the attenuation increases when the dimensions of the transmission line decrease, and this is due to the higher fields around metals while using smaller dimensions. Figure 3.9c also shows that the final design is away from the higher attenuation range. Figure 3.9d shows that λ_{eff} can be tuned from 3.9 mm to 3.4 mm. The final design point has the signal width equal to 125 µm and a gap width equal to 100 µm, and is shown with a white dot in the results. The final design has a characteristic impedance of 50 Ω and has low attenuation. The field shows that the mode is a mix of a microstrip and a CPW.

The simulation model and the results for the SM-CPW are shown in Figure 3.10. Figure 3.10a shows that $|Z_0|$ has a tuning range from 30 Ω to 70 Ω. Figure 3.10a also shows that the characteristic impedance becomes insensitive to the gap width for a gap width greater than the substrate thickness, due to the mode becoming very similar to the stripline mode. Figure 3.10b shows that $\angle Z_0$ is very small, and that Z_0 is mostly real. Figure 3.10c shows how the attenuation increases when the dimensions of the transmission line decrease. Figure 3.10c also shows that the final design is away from the higher attenuation range. Figure 3.10d shows that λ_{eff} is constant around

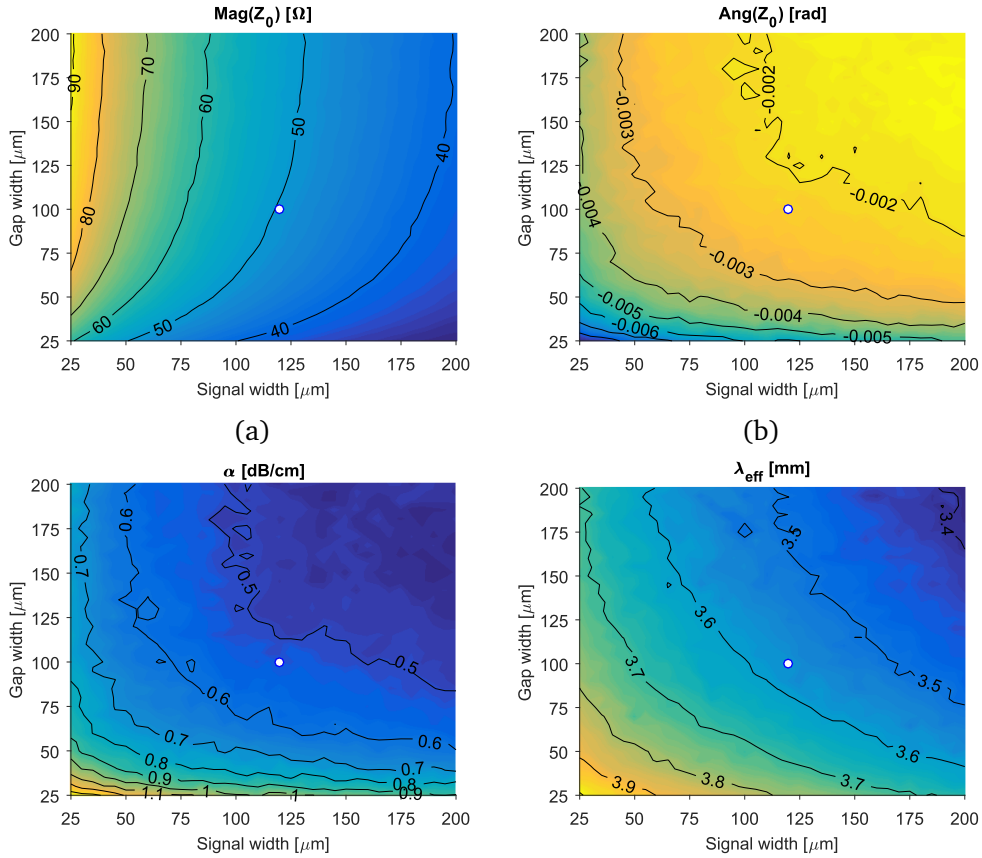


Figure 3.9: The transmission line parameters of the CB-CPW for several combinations of gap width and signal width. These simulations are performed at 40 GHz. The final design point is shown with a white dot in all the following subfigures. (a) shows that $|Z_0|$ has a tuning range from 40 Ω to 90 Ω. (b) shows that $\angle Z_0$ is very small and that Z_0 is mostly real. (c) shows that the designed point is away from the higher attenuation range (d) shows that λ_{eff} can be tuned from 3.9 mm to 3.4 mm.

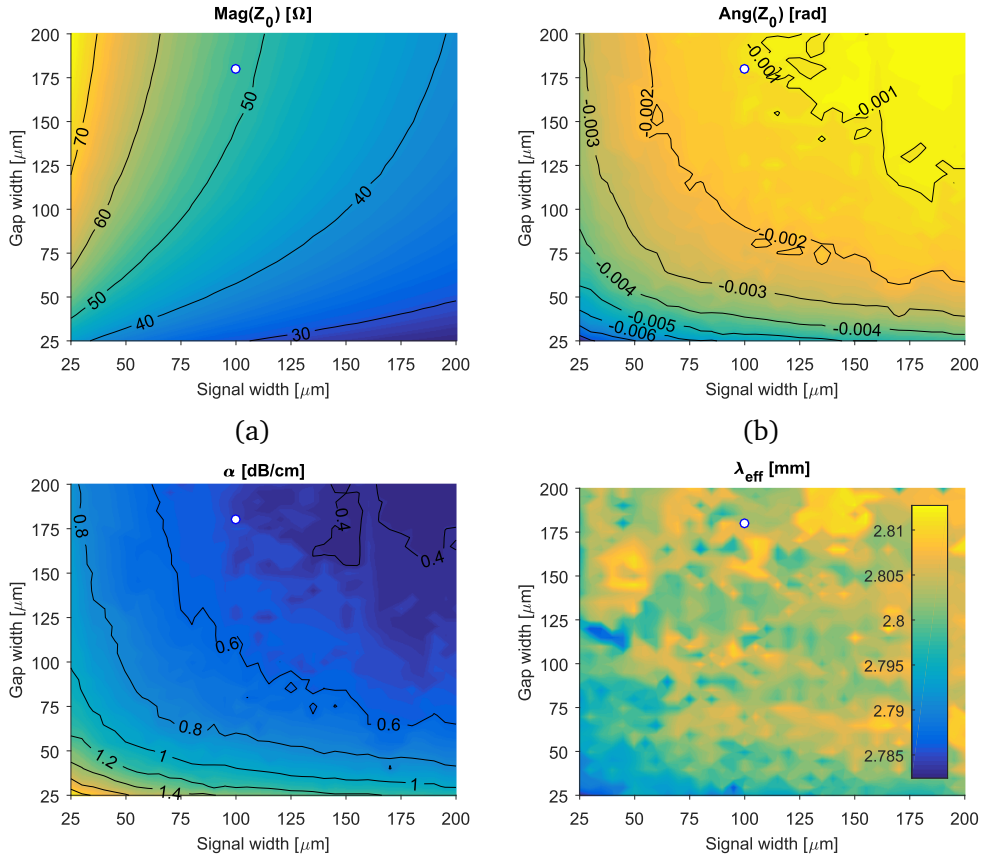
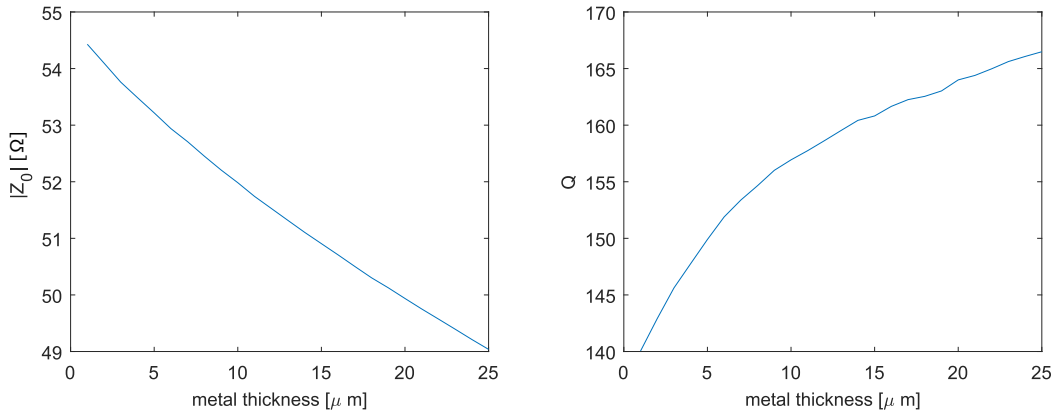


Figure 3.10: The transmission line parameters of the SM-CPW for several combinations of gap width and signal width. These simulations are performed at 40 GHz. The final design point is shown with a white dot. (a) shows that $|Z_0|$ has a tuning range from 30 Ω to 70 Ω. (b) shows that $\angle Z_0$ is very small, and that Z_0 is mostly real. (c) shows that the designed point is away from the higher attenuation range (d) shows that λ_{eff} is almost constant around 2.8 mm in this range.



(a) Characteristic impedance (b) Q factor

Figure 3.11: The characteristic impedance and the Q factor of the CB-CPW for several metal thickness. The impedance is inversely proportional to the thickness and proportional to the quality factor.

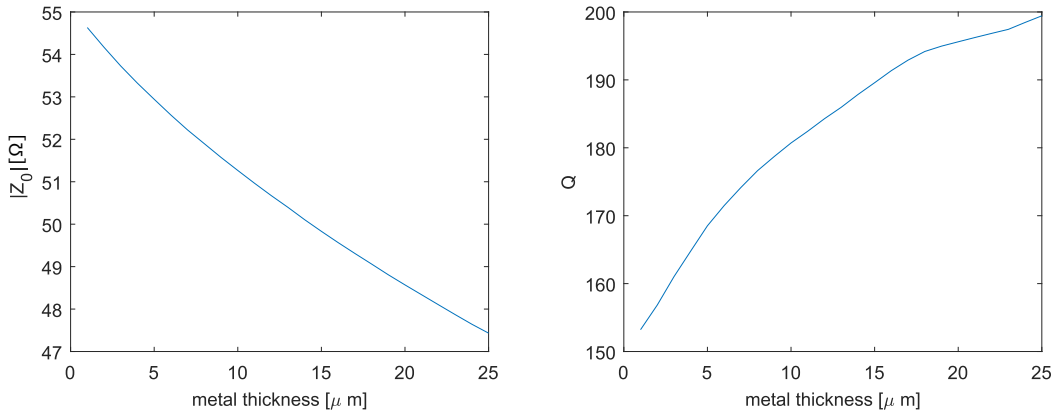
2.8 mm in this range. The constant λ_{eff} is expected as the SM-CPW has only one dielectric, the ceramic, in contrast to the CB-CPW where the electromagnetic fields exist in both the dielectric and the surrounding air. The final design point, which has a signal line width equal to 100 µm and a gap width equal to 180 µm, is shown with a white dot in Figure 3.10. The final design has a characteristic impedance of 53 Ω, not 50 Ω due to a mistake but close, and has low attenuation.

3.2.3 Metal thickness

In this section, the metal thickness of the co-planar metals is varied to explore its effect on the transmission line parameters. The starting point is given in Table 3.3, and the metal thickness is varied from 1 µm to 25 µm. This range was chosen to represent the actual thickness that might be fabricated by electroplating. The usual metal thickness offered in LTCC and aluminium nitride (AlN) is 8 µm.

The characteristic impedance and the Q factor of the CB-CPW for several metal thickness are shown in Figure 3.11. The impedance decreases with the thickness but only by a few Ω for the range of thickness simulated. The quality factor improves with the thickness meaning that thicker metal lines have lower loss.

The characteristic impedance and the Q factor of the SM-CPW for several metal thickness and frequencies are shown in Figure 3.12. The impedance decreases with the thickness but only by a few Ω. The quality factor improves with the thickness meaning that thicker metal creates lines that have lower loss.



(a) Characteristic impedance (b) Q factor

Figure 3.12: The characteristic impedance and the Q-factor of the SM-CPW for several metal thickness. The impedance is inversely proportional to the thickness and proportional to the quality factor.

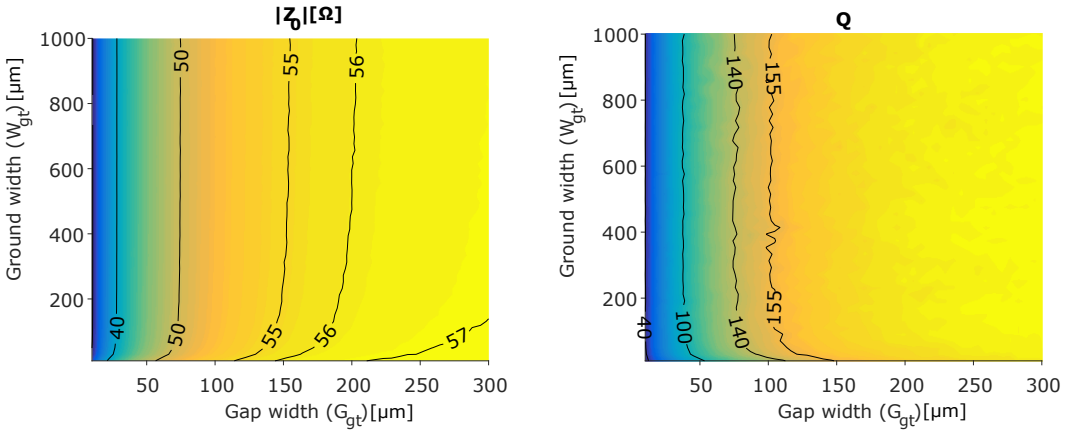
3.2.4 Ground width

In this section, the effect of the ground width is studied. The CB-CPW ground width (W_{gt}) is varied from 10 µm to 1000 µm in the two-dimensional simulation and the characteristic impedance and the Q-factor is calculated. The ground width of the SM-CPW (W_{gb}) is varied the same way.

The characteristic impedance and the Q-factor of the CB-CPW for several combinations of ground and gap widths are shown in Figure 3.13. The characteristic impedance is not affected by the ground width if it is larger than the gap width. The reason for this is that the field coupled between the signal and the coplanar ground decreases with the distance. A ground width smaller than 200 µm decreases the Q-factor. This is because when the ground width is small enough the field around the metal is distributed in less metal and the conductor losses increase. After the ground is increased to near the gap width, the field does not couple to the end of the ground and both the characteristic impedance and the Q-factor become insensitive.

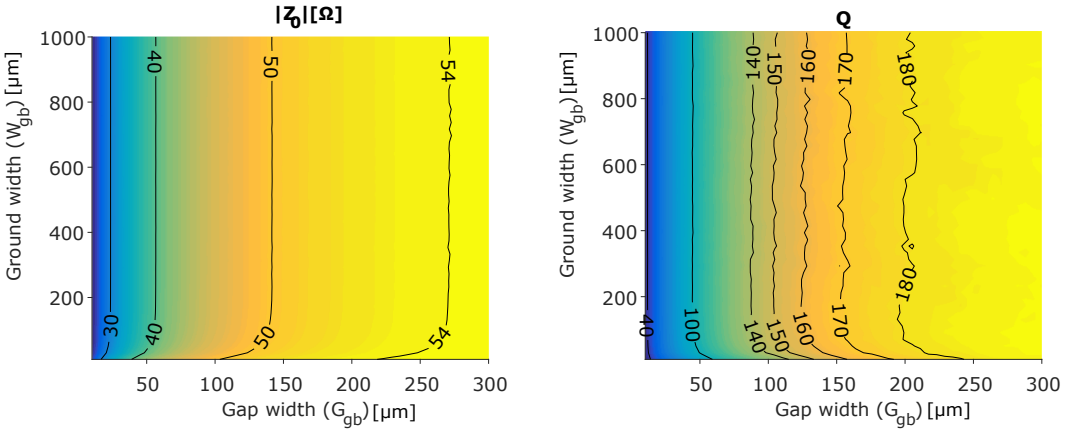
The characteristic impedance and the Q-factor of the SM-CPW are shown in Figure 3.14 for several combinations of ground and gap widths. The characteristic impedance is not affected by the ground width if the ground width is larger than the gap width. A ground width smaller than 200 µm decreases the Q-factor but not as much as changing the gap width. The same mechanism discussed for the CB-CPW act in this case. The fact that the effective dielectric constant is higher for SM-CPW than for CB-CPW since there is no air layer involved makes the electrical field around the metals lower. Therefore, the transmission line characteristics are less sensitive to the ground width.

Section 3.2 showed that the substrate thickness has to be chosen based on the dielectric constant. If the dielectric constant is small, the thickness has to be small to



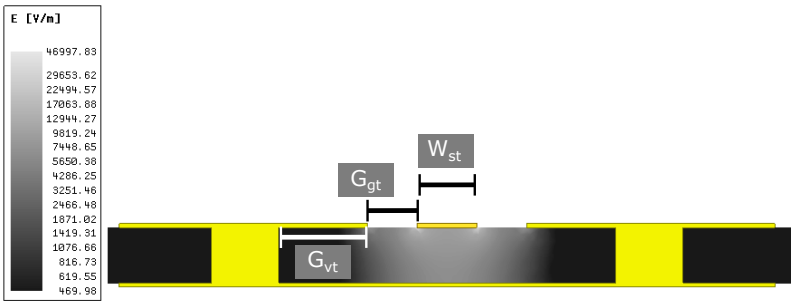
(a) Characteristic impedance (b) Q factor

Figure 3.13: The characteristic impedance and the Q-factor of the CB-CPW for several combinations of ground and gap widths. The characteristic impedance is not affected by the ground width if it is larger than the gap width. A ground width smaller than 200 µm decreases the Q factor.

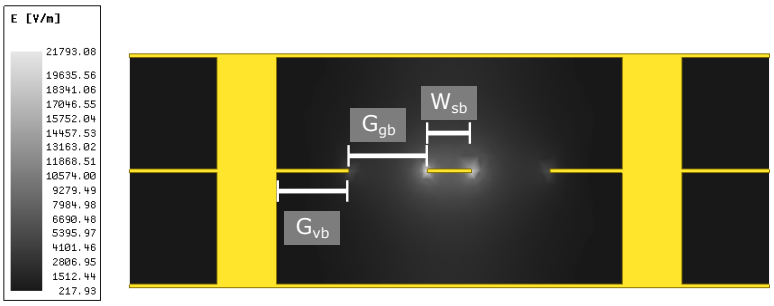


(a) Characteristic impedance (b) Q factor

Figure 3.14: The characteristic impedance and the Q-factor of the SM-CPW for several combinations of ground and gap widths. The characteristic impedance is not affected by the ground width if the ground width is larger than the gap width. A ground width smaller than 200 µm decreases the Q-factor but not as much as changing the gap width.



(a) CB-CPW



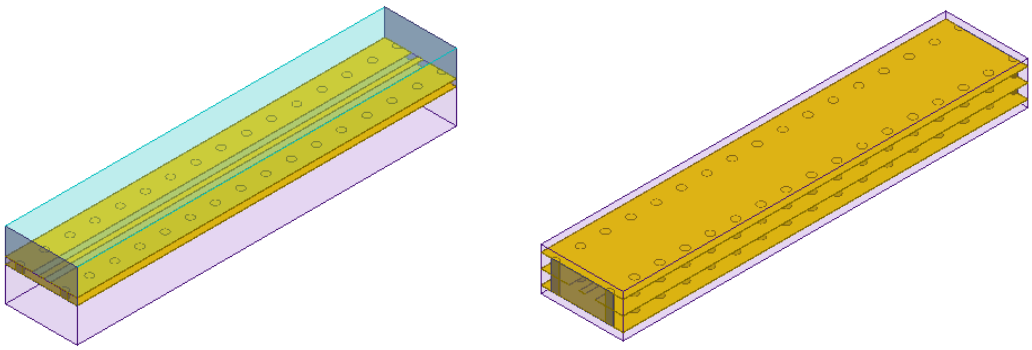
(b) SM-CPW

Figure 3.15: The geometry of the CB-CPW and the SM-CPW with the ground via. The effect of the ground position (G_{vt} and G_{vb}) is studied.

decrease the characteristic impedance. Anyway, decreasing the thickness decreases the quality of the signal for thicknesses below 150 µm. The ground width stops affecting the transmission line characteristics after it is larger than two times the gap. Finally, this section provides the transmission line characteristics for several combinations of gap and signal widths. The next section explores the effect of the ground vias in these designs.

3.3 Effect of the ground vias

This section discusses the effect of the position of the ground vias on the transmission line. In order to do so, models for the 2D electromagnetic simulator of the CB-CPW and the SM-CPW that include the ground vias were created (Figures 3.15a and 3.15b). These geometries differ from the previous geometries (Figures 3.5 and 3.6) in that they include vias connecting the grounds at the different levels. This section discusses the effect of the position of the ground vias in the performance of the transmission line. In this section, the 3D full-wave electromagnetic simulator is used for the first time in this document and Section 3.3.1 shows the comparison to the 2D simulator and to actual measurements as validation. Following, Section 3.3.2 discusses the effect of the ground via position on the characteristic impedance. Section 3.3.3 discusses the effect of the vias on the inter-channel crosstalk. Finally, Section 3.3.4



(a) CB-CPW (b) SM-CPW

Figure 3.16: The full-wave models of straight lines used in the simulations.

shows how the ground vias are used to realise bends.

3.3.1 Validation of the simulation models

First, the two-dimensional models shown in Figures 3.15a and 3.15b are validated by comparing them to a three-dimensional full-wave simulation and measurements of simple straight lines. For the CB-CPW used for this validation, the planar ground width is 500 µm and the via diameter is 136 µm in all the simulations. For the CB-CPW, the signal width (W_{st}) is 120 µm and the gap width (G_{gt}) is equal to 100 µm. For the SM-CPW, the signal width (W_{sb}) is 100 µm and the gap width (G_{gb}) is equal to 180 µm. The substrate thickness for the CB-CPW is 127 µm and the SM-CPW is surrounded by two substrates with thicknesses of 254 µm.

The 2D electromagnetic models (Figures 3.15a and 3.15b) were used to calculate the distributed RLGC model of the transmission lines, then the equivalent S-parameters were calculated for a length of 136 µm with via and 335 µm without via. Then the two scattering parameters (S-parameters) were concatenated by use of ABCD matrices [8]. Several segments are concatenated until a total length of 7.5 mm is obtained. The electric field is shown in Figure 3.15a, and the S_{21} simulation result is shown in Figure 3.17 with the label 2D.

The full-wave model consists of the material models, the geometry, the signal feed ports and the boundary conditions, as shown in Figure 3.16. The material models are the same as in the 2D case (Table 3.2). The CPW dimensions are the same as discussed in the 2D model. The via to via spacing is set to 450 µm. The 3D model contains an air layer on the top with a modelled thickness of 200 µm. The excitation ports used in the model are rectangular wave ports centred in the signal metal, with only the main mode being excited. The outer boundary condition is set to radiation. The electric field is shown in Figure 3.15b. The S_{21} simulation result is shown in Figure 3.17 with the label 3D.

Two CB-CPW lines were fabricated and characterised. The board was fabricated at

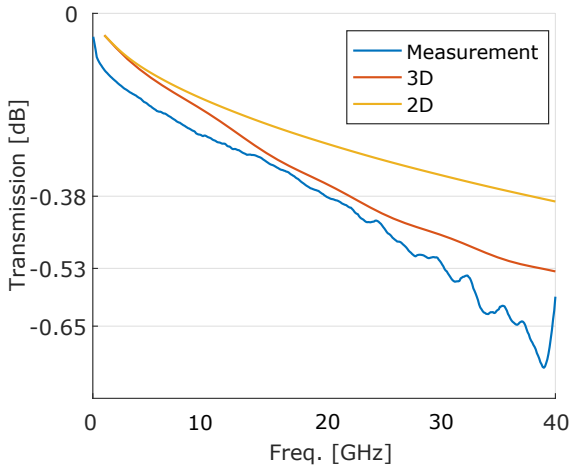


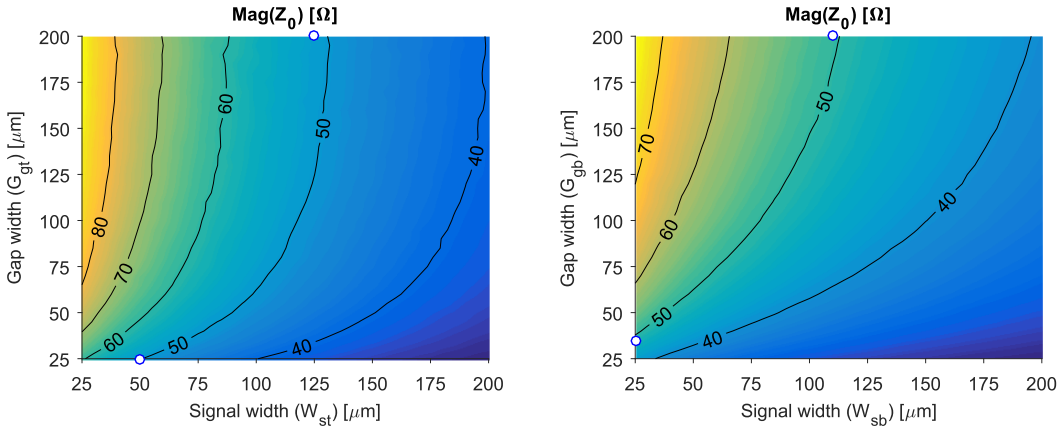
Figure 3.17: The simulations and the measurements show good agreement.

the École de Technologie Supérieure (ÉTS), and the material used for the fabrication was Dupont™ 9K7. Once the board was fabricated, a Vector Network Analyser (VNA) was used to measure the ten copies of two lines with different lengths. The average of the ten measurements for the two lines with different lengths was used to de-embed a 7.5 mm line using the thru-only algorithm [9] and the result is shown in Figure 3.17 with the label Measurement. The measurements are discussed in detail in Chapter 5.

The simulation and the measurements have a good agreement, as can be seen in Figure 3.17. The measurements show a higher loss than the transmission line simulation or the full-wave simulation. The reason might be related to the material models used since they do not account for any frequency dependency or the metal roughness. The result for a similar exercise using SM-CPW lines also showed a good general agreement but with differences as high as 1.5 dB at two frequencies, probably related to the effect of the manufacturing variations of the vertical transition in the de-embedding procedure. Also, the full-wave model of a transition between a CB-CPW to an SM-CPW showed good agreement with the measurements (Chapter 5).

3.3.2 Effect on the characteristic impedance

The CB-CPW and the SM-CPW structures have two operational modes. If the gap between the signal and the ground (G_{gt} or G_{gb}) is large enough, the characteristic impedance becomes insensitive to the gap distance. This case is referred to as the microstrip or stripline mode because the field is mostly coupled between the signal trace and the backside grounds. If the gap is small then most of the field is coupled between the signal trace and the coplanar ground traces, thus the mode is very similar to a simple CPW. This behaviour can be seen in Figure 3.18 where the characteristic impedance calculated by the 2D simulation model is plotted versus the signal width (W_{st} or W_{sb}) and the gap width (G_{gt} or G_{gb}) at 40 GHz. Two operation points for the CB-CPW and two for the SM-CPW have been chosen to reflect these operation modes.



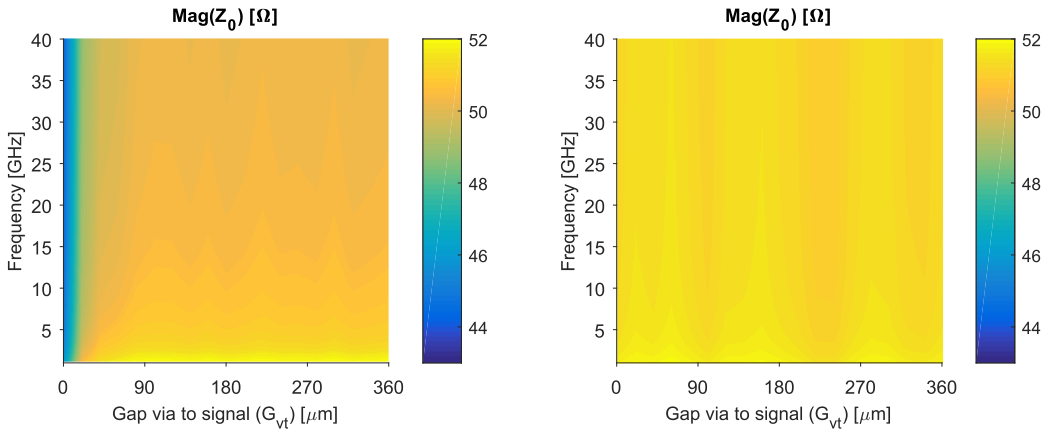
(a) CB-CPW (b) SM-CPW

Figure 3.18: The characteristic impedance versus G_{gt} and G_{gb}. If the gap widths (G_{gt} or G_{gb}) are large enough, the characteristic impedance becomes insensitive to the gap width because the mode becomes like a microstrip or a stripline. If they are small the characteristic impedance is that of a simple CPW. Two different operation points have been chosen for the experiments around the ground via position.

The CB-CPW CPW-like operation point is chosen by setting the signal width (W_{st}) to 50 µm and the gap width (G_{gt}) to 25 µm. The CB-CPW microstrip-like operation point is chosen by setting $W_{st} = 125\,\mu m$ and $G_{gt} = 200\,\mu m$. The SM-CPW CPW-like operation point is chosen by setting $W_{sb} = 25\,\mu m$ and $G_{gb} = 30\,\mu m$. The SM-CPW stripline-like operation point is chosen by setting $W_{sb} = 100\,\mu m$ and $G_{gb} = 200\,\mu m$. Those four operation points are shown in Figure 3.18.

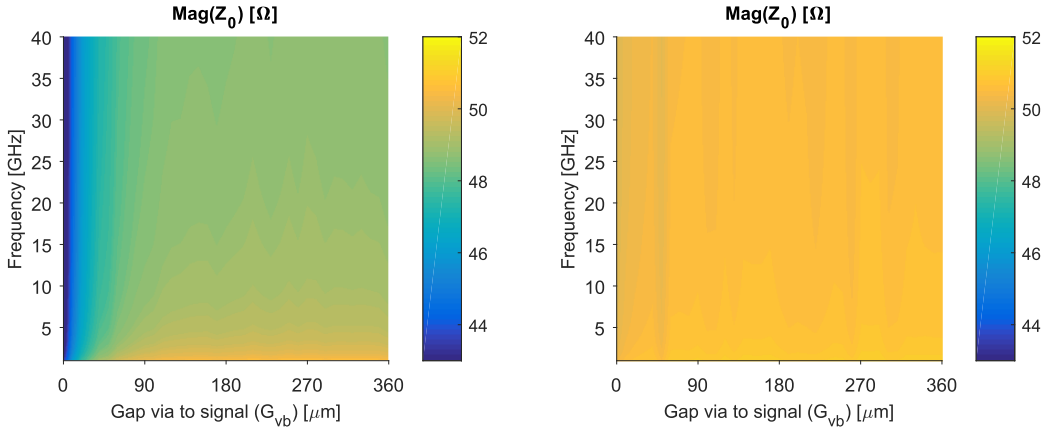
The characteristic impedance is influenced by the position of the via fence if the CB-CPW or SM-CPW is in a strong CPW-like mode. This is clearly seen in the colour-map range in Figure 3.19a and Figure 3.20a. For small gap widths between the via and the signal trace (G_{vt} or G_{vb}), the characteristic impedance is 43 Ω. The impedance becomes insensitive to G_{vt} or G_{vb} for widths sufficiently large to a value close to 50 Ω. The characteristic impedance does not change much with frequency after a few GHz. This behaviour is due to the vias being too far away to have any field coupled to them. The disturbance of the characteristic impedance by the via position is problematic because the transmission line will be made of sections with and without ground vias thus having sections with different characteristic impedances, which create additional reflections and potentially filters certain frequencies [10].

The characteristic impedance is not disturbed due to the position of the via fence if the CB-CPW, or SM-CPW, is in a strong microstrip-like or stripline-like mode. This is clearly seen in the colour map range in Figure 3.19b and Figure 3.20b. The range of the impedance for the variations of the G_{vt} or G_{vb} is only 1 Ω contrasting with the almost 10 Ω range in Figure 3.19a and Figure 3.20a. The reason for this behaviour is that for this mode the field is mostly coupled between the signal trace and backside



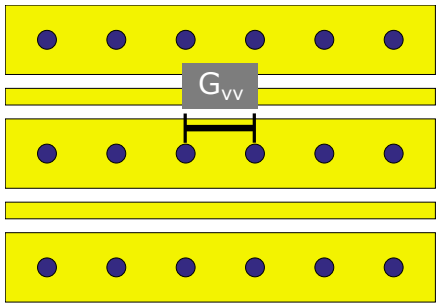
(a) CB-CPW CPW-like mode (b) CB-CPW microstrip-like mode

Figure 3.19: The impedance disturbance by the ground via position in the CB-CPW: (a) CPW-like mode, the impedance is sensitive to the gap between the via and the signal trace (G_{vt}). (b) microstrip-like mode: the characteristic impedance is not sensitive to G_{vt}.

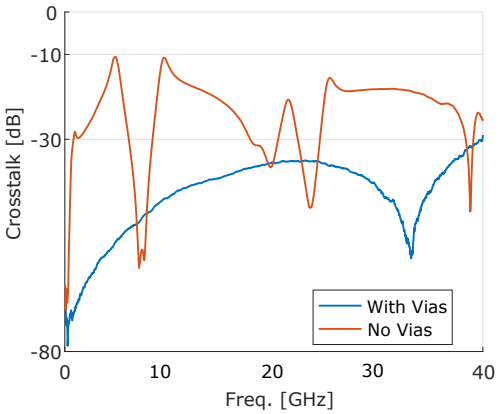


(a) SM-CPW CPW-like mode (b) SM-CPW stripline-like mode

Figure 3.20: The impedance disturbance by the ground via position in the SM-CPW. (a) In the CPW-like mode: the impedance is sensitive to the gap between the via and the signal trace (G_{vb}). (b) stripline-like mode: the characteristic impedance is not sensitive to G_{vb}.



(a) The measured device



(b) Measured results

Figure 3.21: An experiment into the effect of ground vias on crosstalk. The measured results of a fabricated board show that the via fences are necessary to avoid inter-channel crosstalk.

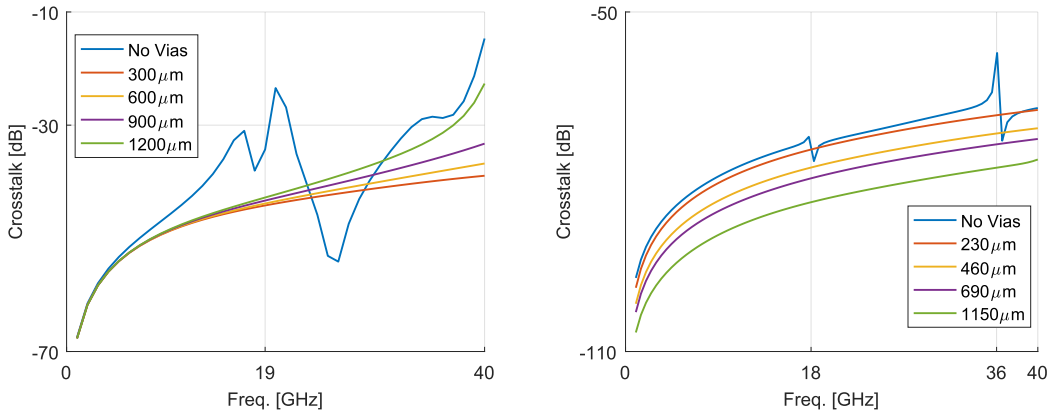
ground, thus no coupling to the via is obtained even with small G_{vt} or G_{vb}.

A good rule of thumb to avoid disturbing the designed characteristic impedance is to keep the space between the signal trace and the via fence to at least two times the gap between the signal trace and the planar ground traces. That is $G_{vt} > 2G_{gt}$ for CB-CPW or $G_{vb} > G_{gb}$ for SM-CPW. In addition, if the mode is very microstrip-like or stripline-like, then the position of the ground via will have a negligible effect on the transmission line.

3.3.3 Crosstalk

In the case of a CB-CPW, the via fence is very important to reduce the inter-channel crosstalk. The device shown in Figure 3.21a has been fabricated and measured to study the effect the ground via has on the crosstalk. The signal to signal pitch is 620 µm, the via to via gap (G_{vv}) is 450 µm and the line length is 3.1 mm. Another device was fabricated but without the ground vias. The devices were measured using a *Vector Network Analyser* (VNA) from 0.5 GHz to 40 GHz by placing one probe at the left end of the bottom line and the other probe in the right end of the top line, leaving the other two ends open. The results of this measurement for the device with and without vias are shown in Figure 3.21b. The results show that the maximum crosstalk without the ground vias is −10 dB and with the ground vias −30 dB; thus the ground vias are needed to shield the lines against crosstalk. Other lines with a larger signal to signal pitch were fabricated and measured showing that the signal to signal pitch had little impact on the crosstalk if the ground vias were present.

For a CB-CPW, the via fence will shield inter-channel crosstalk for signals with wavelength larger than four times the spacing between adjacent fence via, that is $G_{vv} < \lambda_{\text{eff}}/4$. This conclusion was obtained from the simulation of a full-wave model



(a) CB-CPW (b) SM-CPW

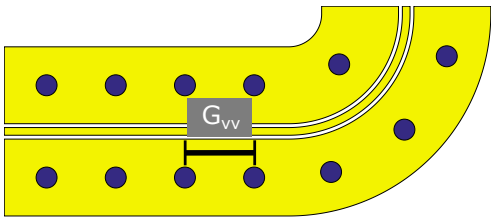
Figure 3.22: Simulation of the effect of the ground via spacing on crosstalk. (a) For a CB-CPW, the fence via will shield inter-channel crosstalk for signals with wavelength larger than four times the spacing between adjacent fence via, that is $G_{vv} < \lambda_{\text{eff}}/4$. (b) In the case of the SM-CPW, the fence via is not necessary to reduce the crosstalk, since the structure seems to be naturally protected against crosstalk.

that was created to characterise the effect of the via to via spacing (G_{vv}) in the crosstalk. The model uses the same materials, boundaries and ports that the simple line used for validation. The geometry is two adjacent lines with a length of 3.1 mm as shown in Figure 3.21a. Four ports were placed in each of the ends of the lines. The results for different via to via spacings (G_{vv}) are shown in Figure 3.22a. When there are no vias, the crosstalk gets above −30 dB after 15 GHz. If the $G_{vv} = 1200\,\mu$m the crosstalk is below −30 dB for frequencies below 35 GHz, exactly when the spacing is equal to $\lambda_{\text{eff}}/4$. For smaller values of G_{vv} the crosstalk is below −30 dB for the entire frequency range.

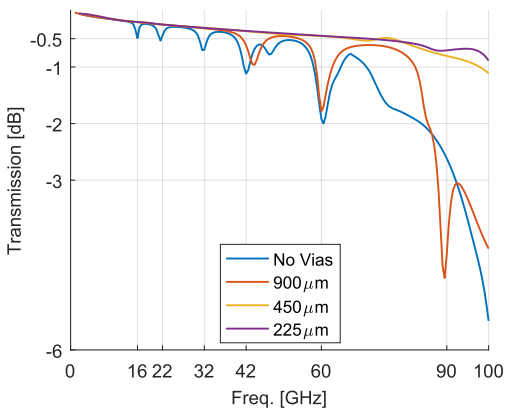
In the case of the SM-CPW, the fence vias are not necessary to reduce the crosstalk, since the structure seems to be naturally protected against crosstalk. The same simulations as for the CB-CPW were completed and the results are shown in Figure 3.22b. The crosstalk is below −50 dB for all the variations, including the case without vias. The reason seems to be that the higher effective dielectric constant (ϵ_{eff}) decreases the current densities on the metals, including the shared ground metal. In the case of without vias, two resonant kinks are obtained at 18 GHz and 36 GHz that are consistent with the coupled line theory [8].

3.3.4 Effect on parasitic modes due to bends

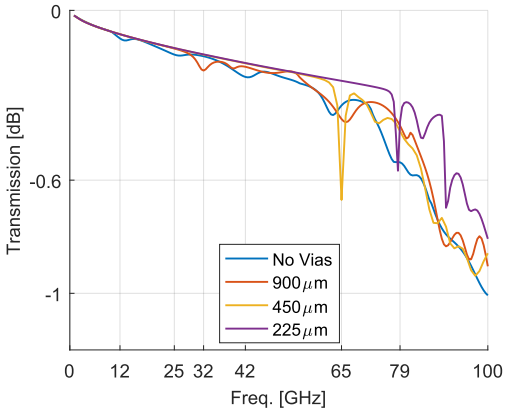
Bends have been shown to excite the propagation of the odd parasitic CPW mode, thus requiring special structures to avoid this excitation. For example, air-bridges [6], [11] or the use of velocity compensated CPW bends [12], [13]. Another parasitic mode is



(a)



(b) CB-CPW



(c) SM-CPW

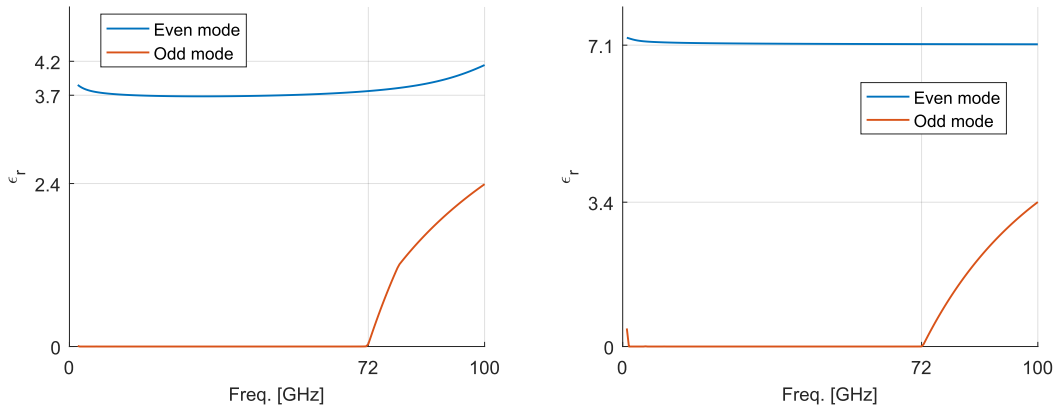
Figure 3.23: The effect of the ground via spacing in bends. The simulations results show that the ground vias protect against parasitic mode propagation up to wavelengths larger than four times the spacing between adjacent fence vias.

the patch antenna mode [3], [14], where the coplanar ground metals resonate as patch antennas at the resonant frequencies given for a straight CPW by

$$f_{mn} = \frac{c}{2\sqrt{\epsilon_r}}\left[\left(\frac{m}{w_g}\right)+\left(\frac{n}{l_g}\right)\right] \tag{3.1}$$

where c is the light velocity in a vacuum, ϵ_r is the relative effective dielectric constant, w_g is the ground pad width, l_g the ground pad length and both m and n are indices. The use of ground vias was shown to avoid the parasitic mode excitation for the case of liquid crystal polymer (LCP) [15].

The ground vias are effective at eliminating the propagation of the odd CPW mode for frequencies below the point where the wavelength is smaller than four times the spacing between ground vias (i.e. $G_{vv} < \lambda_{\text{eff}}/4$). A simulation of the bend that is shown in Figure 3.23a was completed. The material models, the boundary conditions and wave ports are the same as before. Several via to via gaps (G_{vv}) were simulated for both the CB-CPW and the SM-CPW. The dimensions of the CB-CPW were chosen as a signal width equal to 50 µm, the gap width equal to 25 µm, the ground width equal to 500 µm and the line length equal to 3.1 mm. Those dimensions were chosen



(a) CB-CPW (b) SM-CPW

Figure 3.24: Modal analysis of the CPW structures. The CPW odd mode is evanescent up to 72 GHz. The ϵ_r is higher for the SM-CPW since the SM-CPW does not contain air.

to select a design where the mode is CPW-like. The results of the simulations for the CB-CPW are presented in Figure 3.23b. Those results show that a bend without ground vias results in a degradation in the performance at frequencies 16 GHz, 22 GHz, 32 GHz, 42 GHz and 60 GHz, which are due to the patch antenna modes and described by Equation 3.1. After 72 GHz, the transmission has a roll-off due to inter-modal crosstalk with the parasitic odd mode, while before 72 GHz the odd mode is evanescent as shown in Figure 3.24a. Adding ground vias with separations of 900 µm removes the degradation at frequencies below 42 GHz, but the patch antenna modes are still excited at 42 GHz and 60 GHz. A via to via spacing below 450 µm removes both the patch antenna resonances and the roll-off due to the odd mode.

The simulation results for the SM-CPW are shown in Figure 3.23c. The dimensions of the SM-CPW were chosen to have a signal width equal to 180 µm, the gap width equal to 100 µm and the ground width 500 µm. The results show that the main degradation of a bend without ground vias is related to the excitation of the odd mode after 72 GHz, while before that frequency, the odd mode is evanescent as shown in Figure 3.24b. When $G_{vv} = 900\,\mu m$, the transmission does not improve. The use of $G_{vv} = 450\,\mu m$ improves the transmission up to 65 GHz, where a new resonance is introduced after which the roll-off restarts. When $G_v = 225\,\mu m$ the recently introduced resonance is moved to 79 GHz.

In summary, Section 3.3 presented a 2-D and a 3-D electromagnetic simulation model that showed good agreement with the measurements for an LTCC board. Using the 2-D model, an analysis of the effect of ground via placement on the characteristic impedance in SM-CPW and CB-CPW was presented. The 3-D model was used to study the effect of the ground via placement on the crosstalk and bends. Two modes have been identified for the SM-CPW and the CB-CPW - The stripline/microstrip

mode and the CPW mode. The placement of the fence vias does not disturb the impedance of the transmission line if in the stripline/microstrip mode, but it does in the CPW mode. If the transmission line is in the CPW mode, ensuring that the distance between the signal metal and the ground via is at least twice the CPW gap width is recommended to avoid a change in the designed impedance. For the CB-CPW, the shield vias are effective in reducing the inter-channel crosstalk as long as their separation is below a quarter wavelength of the operating frequency. The SM-CPW is less sensitive to inter-channel crosstalk. The via fences are effective in eliminating parasitic mode excitations, like the patch antenna mode or the CPW odd-mode, as long as the separation is kept below a quarter of the wavelength of the operating frequency.

3.4 Other transmission lines

This section presents two transmission lines for the cases when the multi-layer channels are not created by co-firing but rather by bonding or flip-chip. These designs were pursued when it seemed uncertain if I could get access to a multi-layer AlN process. Thus, the plan was to assemble our own multi-layer AlN board. Section 3.4.1 presents the case of bonding and Section 3.4.2 presents the case of flip-chip.

3.4.1 Layer stacking by bonding

In the case of the layer stacking by bonding, the top layer is a CB-CPW as in the co-fired case. However, the buried layer transmission line is different. The use of bonding adds an air layer over the signal trace that is not present in the co-firing case as seen in Figure 3.25. The top AlN substrate thickness is 127 µm and the bottom layer thickness is 254 µm. The top layer is smaller so that smaller via diameters can be used since the via diameter must be at least as large as the substrate thickness due to manufacturing limitations. A bonding line thickness of 25 µm is chosen to match the design rules. Additional simulations that vary the bonding layer thickness show that the design is tunable. The vertical transition for this case is similar to the transition for the co-firing case, except for the solder bond layer between the vias' catch pads and a corresponding air layer. The transition has not been optimised in this research and this is an opportunity for future work.

3.4.2 Layer stacking by flip-chip

In the case of the layer stacking realised by flip-chip, the top layer CPW is a CB-CPW as before. However, the buried layer CPW is different (Figure 3.26). The difference is that the solder balls add a layer of air between the AlN board layers. The buried layer is based in a shielded multi-layer CPW (SM-CPW) as in the Section 3.4.1, but the difference with using co-firing and bonding attachment is that a layer of air will be

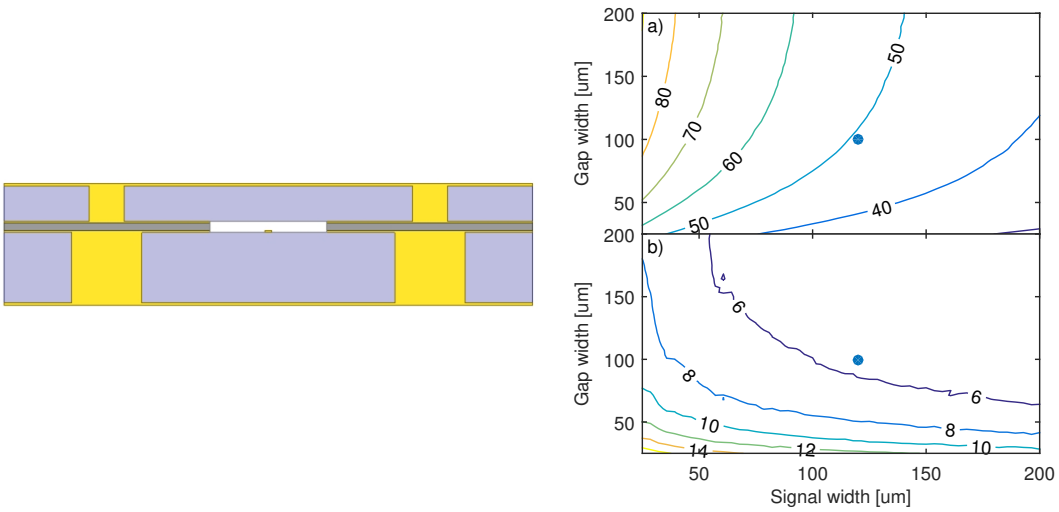


Figure 3.25: The buried CPW for a multilayer system based on bonding. The buried layer is based in a SM-CPW, an air layer will be present in this case. The design maps shows the final design point. The top plot shows the magnitude of the characteristic impedance in Ω and the bottom plot shows the attenuation in $\mathrm{Np\,mm^{-1}}$.

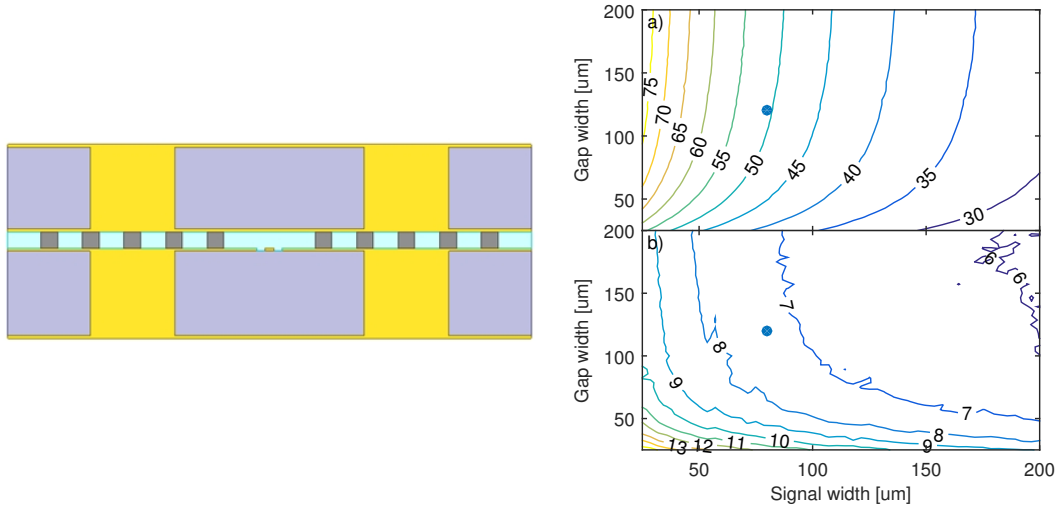


Figure 3.26: The buried CPW for a multilayer system based on flip-chip. The buried layer is based on a SM-CPW. The solder balls are 50 µm long, leaving an air gap. The ground is covering the signal trace in this case. The design maps shows the final design point. The top plot shows the magnitude of the characteristic impedance in Ω and the bottom plot shows the attenuation in $\mathrm{Np\,mm^{-1}}$.

thicker, since the solder ball diameter is 50 µm. The top AlN substrate is not needed since the top ground is now covering the signal. The bottom layer thickness is 254 µm. This configuration allows for smaller transitions due to smaller via diameters. Five solder balls at each side were added, but only the closest to the signal is needed for microwave purposes; the rest will be added for mechanical or thermal reasons.

Section 3.4 presented two transmission lines that could be used to realise a multilayer board without using co-fired ceramics but instead using flip-chip or bonding. The designed transmission lines have 50 Ω characteristic impedance and low loss. A problem with using bonding or flip-chip to create multilayer boards is that the trapped air will decrease the thermal conductivity of the board.

Chapter 3 discussed why CB-CPWs and SM-CPWs have been chosen as our multilayer transmission lines. The CB-CPWs and SM-CPWs were designed using simulations that show how to acheive low-loss and the desired characteristic impedance. The chapter also showed that ground vias are able to remove parasitic modes and realise bends that have good performance while leaving the characteristic impedance undisturbed through the length of the line. The lines have shown low crosstalk, provided certain conditions are met. Finally, some other transmission lines have been presented that could be useful to realise multi-layer interposers without co-fired ceramics.

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Chapter 4
The design of the vertical transitions

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This chapter presents the work done to design two vertical transitions between the transmission lines described in the last chapter. In order to understand the novelty of these transitions, this chapter starts with Section 4.1 presenting the state of the art of microwave vertical transitions found in the literature. Then, Section 4.2 presents the first vertical transition designed for low-temperature co-fired ceramic (LTCC). Following this and based on this first transition, Section 4.3 explains a second vertical transition designed for co-fired aluminium nitride (AlN).

4.1 State of the art of vertical transitions

There are multiple microwave vertical transitions in the literature and Section 4.1 provides a discussion on the state of the art. Section 4.1 starts with Section 4.1.1

presenting a summary of the state of the art. Based on this summary, Section 4.1.1 continues by presenting and justifying the general concept of our vertical transitions. Also, Appendix B provides a more detailed review of each of the vertical transition found in the literature.

4.1.1 Summary of the literature review

Twenty one vertical transitions were found in the literature (Table 4.1). To facilitate the understanding of the state of the art, this sections provides a summary of the characteristics of these vertical transitions. This summary is then used to justify and explain the novelty of this transition.

The analysis of the vertical transitions in the literature is focused on a few characteristics that are key for our application, which are mapped into the columns of Table 4.1. The first important characteristic is the fabrication technology and this discussion focuses on vertical transitions fabricated using co-fired ceramics or liquid crystal polymer (LCP) since these are the two technologies with most of the publications. The LCP transitions are not usable in this case because of the low mechanical strength and the low thermal conductivity (Section 1.1.4) but some of the concepts described using these transitions are useful. The LTCC vertical transitions can use different substrates and the substrate used is important because a lower relative permittivity (ϵ_r) means that the transition is electrically shorter and thus the resonant effects occur at higher frequencies. Our transition uses Dupont 9K7 which has a high ϵ_r but the lowest loss tangent ($\tan\delta$). This means that our transition is more difficult to design but the transmission lines have higher quality. The second important characteristic is the type of transition. In this analysis, the focus is on vertical transitions between planar waveguides (Section 3.1). The third key characteristic is the number of metal layers, which is directly related to the price of fabrication, so the fewer metal layers the better (Section 1.2.4). The fourth key characteristic is the transition thickness, which is the distance between signal metals. This thickness is related to the microwave performance of the transition since smaller distances present fewer resonance effects. The fifth key characteristic is the overall thickness. The overall thickness is important because our carrier board needs to drain the heat from the devices through the package. Thus, the thinner the carrier board the better the board is able to drain the heat. The sixth key characteristic is the cross-level cross-talk shield. If there is no ground metal layer between the signal layers, the crosstalk between channels can be significant and thus the crossing of channels is not possible. Similarly, the seventh key characteristic is the shield against the mounting substrate. If the transition is between two transmission lines on the top, the performance of the connection will be affected by the characteristics of the substrate on which the board is mounted. The eighth key characteristic is the use of only standard commercially available features. Several of the transitions found in the literature have been designed by research groups that have research access to the fabrication facilities, and thus are able to use non-commercial features. In our case, it was important to comply with standard commercial design rules. The ninth and

Table 4.1: Summary of vertical transitions found in literature. RL refers to the lowest frequency at with the return loss is above −10 dB.

Source	Tech. (ϵ_r)	Type	Metal layers	Transition thick. µm	Overall thick. µm	Cross-level shield	Substrate shield	Standard	f_{3dB} GHz	RL GHz
[1]	LCP (2.98)	CB-CPW-CB-CPW	2	50	50	No	Yes	Yes	40	40
[2], [3]	LCP (2.98)	CPW-Microstrip	2	100	100	No	No	Yes	100	100
[4]	LCP (2.98)	CPW-Stripline	3	59	109	No	Yes	Yes	60	80
[5]	LCP (2.98)	CPW-Stripline	6	375	450	Yes	Yes	Yes	70	70
[6]	LTCC (5.90)	Board-Board	2	1000	1000	No	No	Yes	11	11
[7]	LTCC (5.90)	CB-CPW-CB-CPW	5	300	500	No	Yes	No	70	70
[8], [9]	LTCC (7.80)	CB-CPW-CB-CPW	4	600	600	No	Yes	Yes	45	45
[10]	LTCC (7.80)	CB-CPW-CB-CPW	3	420	840	No	Yes	Yes	10	10
[11]	LTCC (5.90)	CB-CPW-CB-CPW	4	800	800	Yes	No	Yes	50	50
[11]	LTCC (5.90)	CB-CPW-Microstrip	4	800	800	Yes	No	Yes	50	50
[12]	LTCC (5.90)	CB-CPW-Stripline	5	500	800	No	Yes	No	45	40
[13]	LTCC (7.10)	CB-CPW-Stripline	3	127	254	No	Yes	No	100	100
[14]	LTCC (7.10)	CB-CPW-Stripline	5	300	600	Yes	Yes	No	–	–
[15]	LTCC (5.90)	CB-CPW-Stripline	5	300	500	Yes	Yes	Yes	1	1
[11]	LTCC (5.90)	CB-CPW-Stripline	4	400	800	Yes	Yes	No	50	50
[16]	LTCC (5.90)	CB-CPW-Stripline	4	500	800	Yes	Yes	Yes	37	37
[17]	LTCC (5.90)	CPW-CPW	2	300	300	No	No	Yes	25	25
[18], [19]	LTCC (7.00)	CPW-SMT	9	700	700	Yes	Yes	No	20	20
[20]	LTCC (7.10)	CPW-Stripline	4	110	432	No	Yes	No	150	150
[21], [22]	LTCC (5.90)	CPW-Stripline	4	800	1120	Yes	Yes	Yes	30	10
[23]	LTCC (7.50)	Flipchip-Microstrip	5	400	560	Yes	Yes	Yes	35	45
[24]	LTCC (7.80)	Microstrip-Microstrip	11	550	550	Yes	No	Yes	40	35
[25]	LTCC (5.90)	Microstrip-Microstrip	7	600	600	Yes	No	Yes	60	40
[26]	LTCC (5.90)	Microstrip-Stripline	6	600	800	Yes	Yes	Yes	70	25
[16]	LTCC (5.90)	Microstrip-Stripline	4	500	800	Yes	Yes	Yes	35	50
[16]	LTCC (7.80)	Microstrip-Stripline	4	680	960	Yes	Yes	Yes	25	42
[27]	LTCC (–)	Microstrip-Stripline	5	500	750	Yes	Yes	Yes	–	30
[28]	LTCC (5.90)	Microstrip-Stripline	5	600	1200	Yes	Yes	Yes	30	40

tenth key characteristics are related to the microwave performance. The microwave performance of the transitions is summarised by the 3 dB bandwidth ($f_{3\,\mathrm{dB}}$) and by the shortest frequency at which the return loss (RL) is above −10 dB.

There are more microwave vertical transitions for LTCC than for LCP even though the vertical transitions fabricated in LCP show excellent performance. The reason for this is that the ϵ_r is small, as is the substrate thickness. This results in signal widths that are below 100 µm and shorter transitions thicknesses; thus the better performance. However, this is a problem because LCP becomes flexible (Figure 1.6) making the interposers not very suitable to be carrier boards. One exception to the small thickness trend is found in [5], where the overall thickness is 450 µm with good simulated results (but no fabricated device is reported). However, LCP also presents the problem of not being as commercially available as LTCC and having significantly lower thermal conductivity.

Even though there are plenty of vertical transition reported in the literature, just a few designs are able to provide the cross-level shielding, substrate shielding and use only standard features. The vertical transitions found in [21], [22], [26], [27] provide these desired characteristics but, to achieve these characteristics, the transitions are thicker than 500 µm. The transition in [15] provides the required shielding by using only standard features with a thickness of only 500 µm but the microwave performance is not good enough for our application with a $f_{3\,\mathrm{dB}}$ of only 1 GHz. The LTCC microwave vertical transition with the best microwave performance can be found in [13], [20]. The performance is high because the transition is short. However, to make it so short, the transitions go from the top of a substrate to the bottom of the same substrate. The problem with this approach is that, because of the lack of an intermediate ground layer, there is no shielding for crosstalk between the channels running on both layers.

In summary, none of the transitions found in the literature provides the characteristics needed by our application. The LCP transitions are not suitable as carrier boards for photonic integrated circuits (PICs). Few designs provide the cross-level cross-talk shield, the shield to the substrate and use only standard features. None of the transitions in Table 4.1 uses shielded multi-layer co-planar waveguide (SM-CPW) in the buried layer. Our application needs to have the co-planar grounds in order to have good terminations and reduce the overall footprint.

4.1.2 Overview of our vertical transition

From the LTCC vertical transitions, most of the transitions choose a conductor backed co-planar waveguide (CB-CPW), or co-planar waveguide (CPW), in the top and a buried stripline. In this research, the stripline is replaced by an SM-CPW. This decision was taken based on two reasons. The first reason is that it is easier to realise a thick film termination by having the coplanar grounds, and in the case of the stripline, the grounds are on different levels. The second reason is that having the coplanar grounds adds the gap as one additional design parameter. In the case of the stripline the only way to change the characteristic impedance is by changing

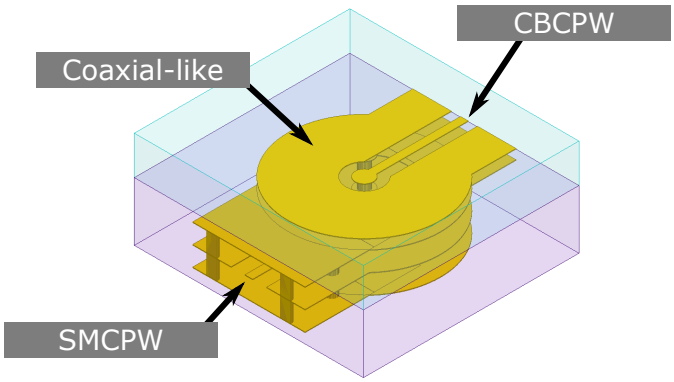


Figure 4.1: Our vertical transition concept. The transition is between a CB-CPW and an SM-CPW using a coaxial-like structure.

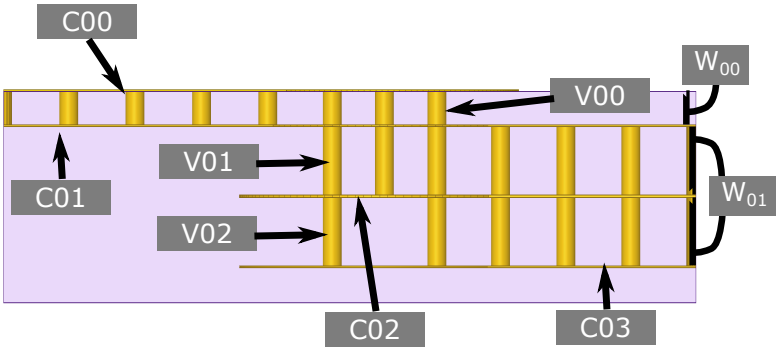


Figure 4.2: The different layers in the transition. The layout consists of three substrates, four conductor layers (CXX) and three via layers (VXX) and thus three substrate layers.

the signal width. The addition of the coplanar grounds does not increase the overall footprint because the stripline needs ground vias to avoid radiation and problems with crosstalk. These ground vias need to be placed at a distance larger than the substrate thickness to avoid characteristic impedance disturbances. In contrast, if the SM-CPW is in a CPW mode, the distance to the vias needs to be only around twice the gap width (Section 3.3.2). So the SM-CPW can realise a smaller footprint for the two adjacent channels. Additionally, the SM-CPW presents the advantage over a stripline of facilitating the inclusion of high-speed load terminations, like the one presented in Section 5.4.1, as a result of the existence of the coplanar grounds and its balanced nature (i.e. it is symmetric around the signal trace).

The vertical transition designed in this research is between a CB-CPW and an SM-CPW using a coaxial-like structure (Figure 4.1). The CB-CPW uses ground vias to connect the co-planar ground with the backside ground. The backside ground of the CB-CPW and the SM-CPW topside ground is shared (Figure 4.2). In this way, the board is shielded against cross-level cross-talk without the need for additional substrate layers. Some care has to be taken to merge the elements drawn in the

CB-CPW backside ground and the SM-CPW topside ground. Conveniently, PICDraw provides functions that allow for the correct merging of these elements. The SM-CPW also uses ground vias to connect the co-planar grounds with the topside and backside grounds. The ground vias also provide cross-talk shielding and enable bends (Section 3.3). The coaxial-like structure is realised by having a signal via surrounded by ground vias. The catch pads for the signal via and the ground vias of the coaxial-like structure are circular, with a gap shaped as a ring. The transition requires only 4 metal layers and 3 substrate layers (Figure 4.2) making it easy to manufacture. This concept provides the cross-level cross-talk shielding. Thus, the performance does not change based on the substrate where it is mounted, and the transition uses only standard features without the use of small features or air cavities.

Section 4.1 presented a summary of the multiple microwave vertical transitions found in the literature and a detailed can be found in Appendix B. In short, there are no transitions that provide cross-level crosstalk shield, shield to the substrate where the board is mounted and that can be fabricated using only standard fabrication rules with enough microwave performance for our application and that minimises the overall thickness. The transition showed in the next section uses only 4 metal layers and meets our goals.

4.2 LTCC vertical transition

The first vertical transition is designed for fabrication in LTCC. The transition was designed using the 2D cross-sectional electromagnetic simulator and then using the 3D full-wave electromagnetic solver to simulate the performance. Section 4.2.1 describes the general concept of the transition. Section 4.2.2 presents the 2D electromagnetic simulations used to define the radius of the transition. Using these results, the final dimensions of the fabricated LTCC board were completed as presented in Section 4.2.3. Finally, Section 4.2.4 presents the 3D full wave simulation used to simulate the performance of this transition.

4.2.1 General description

The vertical transition is between the CB-CPW on the top and a buried SM-CPW connected by a coaxial-like structure (Figure 4.1). The design consists of three ceramic layers (Figure 4.2). An optional layer, depending on whether the metal is needed on the backside of the board or not, can be added without disturbing the design. The design has four conductor layers (C00 to C03). C00 and C02 contain the co-planar circuits and C01 and C03 have the backside grounds that provide the cross-level crosstalk shield. All the parametric dimensions that define the transition are shown in Figure 4.3.

Figure 4.3a shows the dimensional variables that describe layers C00 and V00. W_{nt}, G_{gt} and W_{st} define the CB-CPW,; W_{nt} is the ground width, G_{gt} the gap width,

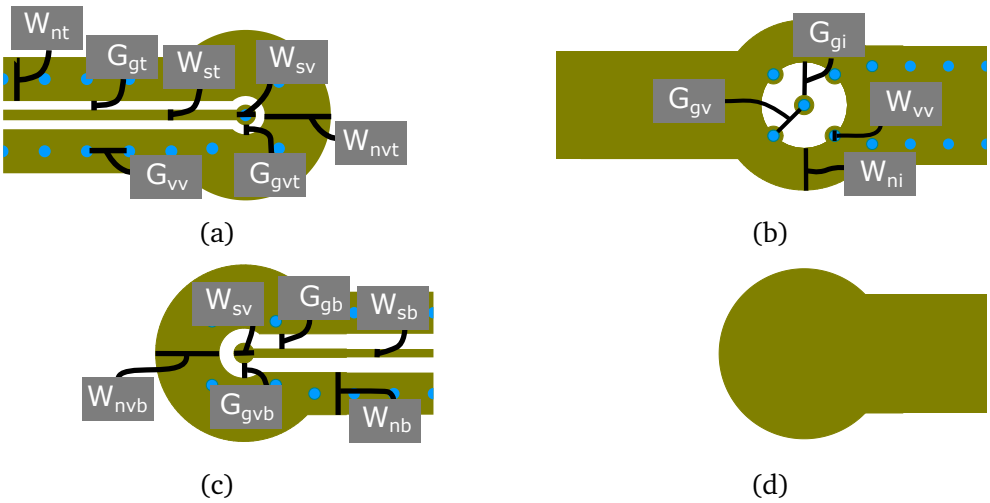


Figure 4.3: The vertical transition fabricated in LTCC. This figure shows all the dimensions that define the final design. The conductor layers are shown in dark yellow and the vias in dark cyan. (a) shows C00 and V00 and the parametric dimensions that define the transition. Similarly, (b) shows C01 and V01, (c) shows C02 and V02, and (d) shows C03.

and W_{st} the signal width. G_{vv} is the spacing between shield vias in both the CB-CPW and the SM-CPW. W_{sv} is the signal catch pad width and it has been chosen to be as small as the fabrication design rules allow . G_{gvt} is the gap between the signal catch pad and the ground via catch pads, and has been chosen to be equal to the gap in the CB-CPW (G_{gt}); in order to avoid adding an extra discontinuity. W_{nvt} is the ground catch pad width used to connect all the ground vias together in this layer, and is chosen to be large enough to catch the closest ground via in the CB-CPW.

Figure 4.3b shows the dimensional variables on layers C01 and V01. G_{gv} is the gap between the signal via and any of the four ground vias that comprise the coaxial-like structure. W_{vv} is the via width, which is the same for all the vias in the transition to reduce the fabrication complexity. G_{gi} is the gap between the signal via catch pad and the ground via catch pad in layer C01, and has been chosen to be equal to the radius of the coaxial-like structure with the idea of not adding a discontinuity. W_{ni} is the ground catch pad width used to connect all the ground vias together in this layer, and is chosen to be large enough to catch the closest ground via in the SM-CPW.

Figure 4.3c shows the dimensional variables on layers C02 and V02. The catch pad diameter is the same as in the layer C00. W_{nb}, G_{gb} and W_{sb} define the SM-CPW: W_{nb} is the ground width, G_{gb} the gap width and W_{sb} the signal width. G_{gvb} is the gap between the signal catch pad and the ground catch pad in this layer, and has been chosen to be equal to the gap in the SM-CPW (G_{gb}) to avoid adding an extra discontinuity. W_{nvb} is the ground catch pad width used to connect all the ground vias together in this layer and is chosen to be large enough to catch the closest ground via in the SM-CPW.

Figure 4.3d shows the layer C03; this is simply the back side ground of the SM-CPW. This layer is like a shadow that covers all the co-planar circuit above it. The geometry in this layer is calculated automatically using a function in PICDraw.

The next section explains how all these parametric dimensions that define the vertical transition were chosen by the use of the 2D cross-sectional electromagnetic solver.

4.2.2 Design procedure

In general, the LTCC vertical transition was designed using only 2D cross-sectional simulations and this section presents the design methodology and the simulation results. Finding a starting point using a 2D cross-sectional electromagnetic solver for a design that is going to be optimised by a 3D full-wave electromagnetic solver makes sense because the cross-sectional solver is much faster than the full-wave solver (Section 1.1.5). In this case, a first design was completed by using only the 2D cross-sectional electromagnetic solver and the performance was simulated using the 3D full-wave electromagnetic solver. The simulated performance of this first design was good enough for our application. The decision to fabricate this first design instead of proceeding to an optimisation by the full-wave simulations was taken based on two reasons. First, the full-wave model had not been validated by measurements. This model has multiple variables that change the simulated performance of the device and therefore using a model that has not been validated by measurements is a risk. The second reason is that the fabrication time is about six months and fabricating this first transition sooner rather than later allowed sufficient time to fabricate the second iteration in co-fired AlN.

Three structures were simulated using the 2D cross-sectional electromagnetic solver: the CB-CPW, the SM-CPW and the coaxial-like structure. The simulations of the CB-CPW and the SM-CPW were discussed in Chapter 3 and the simulations of the coaxial-like structure are explained next.

A coaxial-like transmission line (Figure 4.4a) was simulated using the 2D cross-sectional electromagnetic solver (Section 2.5.1). The material microwave parameters used in the simulations are shown in Table 3.2, as discussed in Section 3.2. The simulation frequency was 40 GHz for all the presented results. Figure 4.4a shows the geometry of the transmission line, which has four ground vias surrounding a single signal via for the coaxial-like vertical transition. Having more ground vias has been shown to be beneficial [26] but only four ground vias are used in our design to allow enough space for the signal metal and gaps, the CB-CPW, the SM-CPW, and to keeps the ground vias continuous through the three substrates. Figure 4.4a shows that the electric field is mostly confined between the signal and ground vias, as desired. This coaxial-like transmission line has two design parameters: the via diameter (W_{vv}) and the gap width (G_{gv}). Both the signal via and the ground vias have the same diameter. Figure 4.4b shows that the modulus of the characteristic impedance ($|Z_0|$) has a tuning range from 20 Ω to 100 Ω and that the impedance contour lines are straight lines with varying slope. Figure 4.4c shows that the argument of Z_0 ($\angle Z_0$) is very

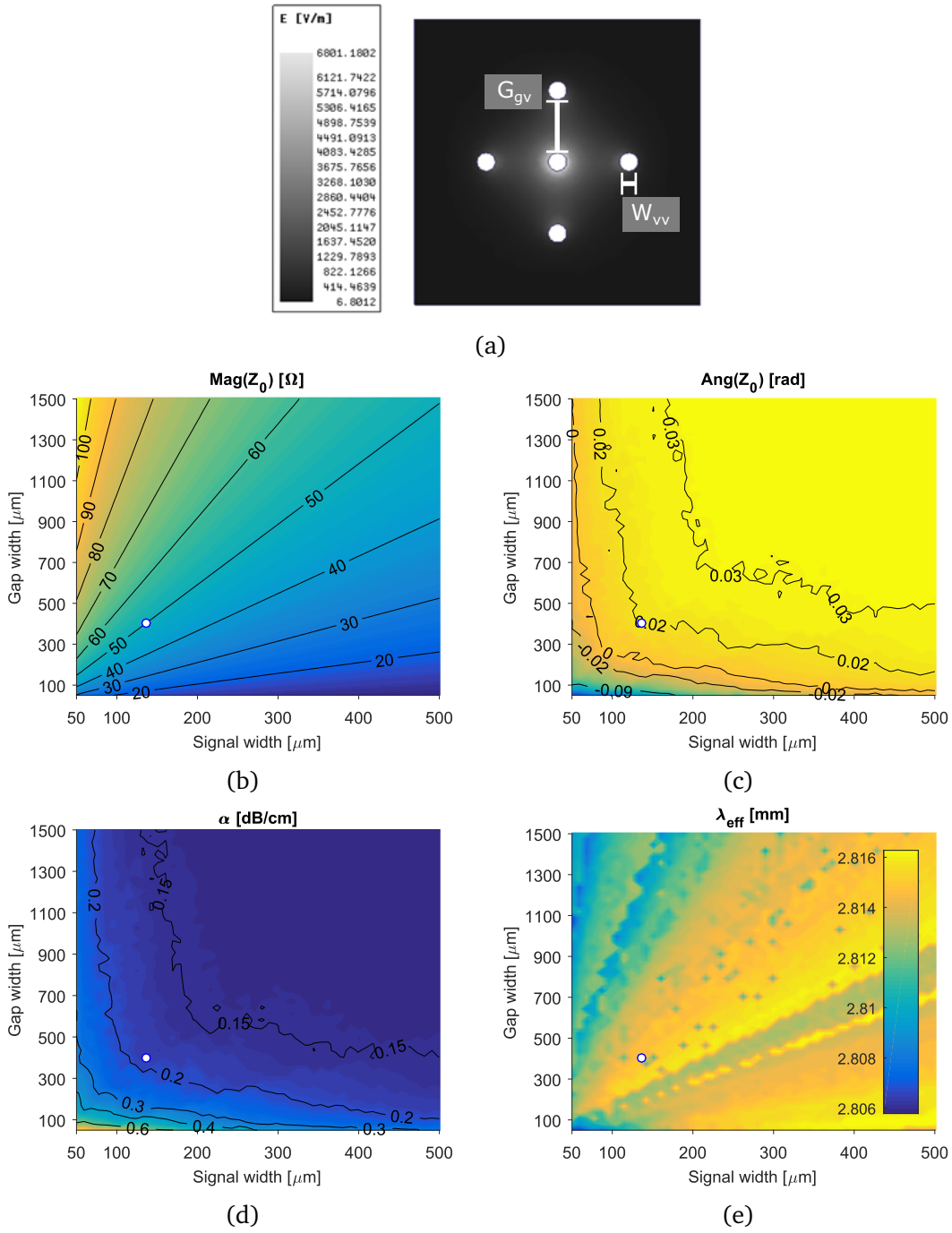


Figure 4.4: The coaxial-like transmission line. (a) shows the geometry and the two parameters swept. The signal width in this case is the via diameter for all the vias. The final design point is shown with a white dot. (b) shows that $|Z_0|$ has a tuning range from 20 Ω to 100 Ω. (c) shows that $\angle Z_0$ is very small. (d) shows that the designed point is away from the higher attenuation range (e) shows that λ_{eff} is almost constant around 2.81 mm.

Table 4.2: The dimensions of the fabricated design

(a) Defined from 2-D simulations

	W_{nt}	G_{gt}	W_{st}	W_{nb}	G_{gb}	W_{sb}	W_{vv}	G_{gv}	W_{00}	W_{01}
[µm]	500	100	120	500	180	100	136	400	127	254

(b) Other parameters

	G_{vv}	W_{sv}	G_{gvt}	W_{nvt}	G_{gi}	W_{ni}	G_{gvn}	W_{nvn}
[µm]	$\gtrapprox$ 450	236	100	750	417	500	180	750

small; that is, Z_0 is mostly real. This is especially true at larger dimensions where $\angle Z_0$ is constant at a maximum. Figure 4.4d shows the attenuation (α) of the transmission line. The attenuation decreases with the larger dimensions as expected. Figure 4.4d shows that λ_{eff} is almost constant around 2.81 mm in this range. The final design point, with a signal diameter equal to 136 µm and gap width equal to 400 µm, is shown with a white dot in the results. The final design has a characteristic impedance of 50 Ω with low attenuation. The final design point was chosen to minimise the footprint of the transition since a via diameter of 136 µm is the smallest that can be fabricated for this substrate thickness.

Once the 2D cross-sectional simulations were completed, a final design of the transition was also completed for fabrication. This final design is presented in the next section.

4.2.3 Final design

The fabrication design rules imposed several constraints. In our case, the board was fabricated at the École de Technologie Supérieure (ÉTS). The fabrication required gold metallization with a thickness of 8 µm for all metal layers. All the vias were made with stencils with 150 µm diameter. These holes were made before the co-firing and due to ceramic shrinkage during the co-firing, the resulting diameter of holes was 136 µm. Circular catch pads covering the metal vias were needed to ensure contact between the metal on the surface and the via fill. In addition, the catch pad diameter needed to be 100 µm bigger than the via diameter. The minimum feature size (metal line width or gap between metals) was 100 µm. The minimal spacing between adjacent vias is 450 µm from centre to centre. The substrate thickness could only be a multiple of 127 µm.

A final design was chosen using the previously discussed simulations and the final dimensions are summarized in Table 4.2. The 10 dimensions shown in Table 4.2a have been defined using the simulation results from the 2D cross-sectional simulator from Chapter 3 and Section 4.2.2, where the ground widths (W_{nt} and W_{nb}) have been fixed at 500 µm. The ground width must be large enough to fit the shield ground vias and can be extended without changing the CPW performance, but decreasing it could change the transmission line characteristics (Section 3.3). The shield ground

vias are placed in the middle of the ground width. The thickness of Layers 00 and 03 (W_{00}) is 127 µm, and the thickness of layers 01 and 02 (W_{01}) are 254 µm each. The thicker ceramics are needed to set the SM-CPW characteristic impedance (Z_0) to be 50 Ω and to be compliant with the design rules. The dimensions in Table 4.2b can not be calculated by 2D simulations since they are inherently 3D. The shield via spacing (G_{vv}) is chosen to allow the maximum number of vias while complying with the minimal separation fabrication requirement of 450 µm. All the via catch pads have a diameter (W_{sv}) of 236 µm, which is the minimum that the fabrication design rules allow. The gap between the signal and ground catch pads at the layer $C00$ (G_{gvt}) is chosen to be 100 µm, equal to the gap in the CPW. Similarly, in layer $C02$ the gap (G_{gvb}) is 180 µm. Both catch pad ground widths at $C00$ and $C01$ are 750 µm. At the layer $C01$, the iris gap (G_{gi}) is 417 µm; that is, the largest gap that can be dimensionally fitted. This is done to try to avoid perturbations of the coaxial-like environment.

The vertical transition layout for the metal layers was drawn using PICDraw. PICDraw is a tool in C++ developed by Dr Frank H. Peters to draw complex layouts for PICs. PICDraw was extended by the author to draw layouts for multilayer boards. Once the layout of the vertical transition was drawn in PICDraw, the 2D layouts are imported into our 3D full-wave simulator.

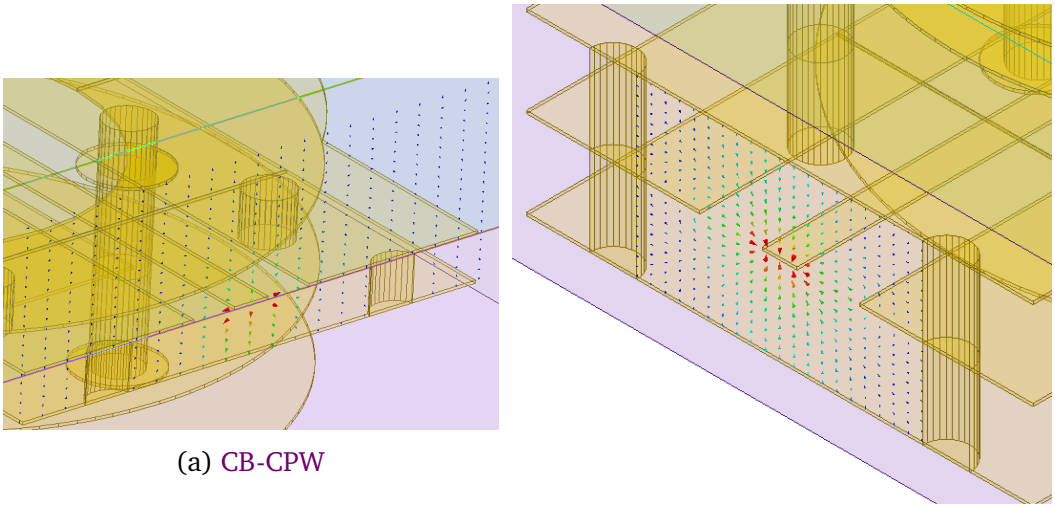
4.2.4 Simulated performance

The 3D model for the full-wave electromagnetic simulation of the transition is shown in Figure 4.1. In order to generate this 3D model, the 2D layouts of the metal layers and the vias positions generated by PICDraw (Figure 4.3) were imported to ANSYS HFSS using a Python script. The script was coded by the author and is presented in Appendix A.3. The material models used are shown in Table 3.2. The 3D model contains an air layer on the top of thickness 200 µm.

The excitation ports used in the model are wave ports. The ports are placed cutting a shield via (Figure 4.5). This is done to have a single mode port, since the shield vias eliminate the CPW odd mode. Figure 4.5 also shows the vector fields of the calculated modes. The vector field shows that the excitation modes that are being used are as expected from the cross-sectional simulation (Chapter 3), and as confirmed by the calculated characteristic impedance (Figure 4.6).

The solver was set up to perform the mesh refinement at 40 GHz and using a frequency sweep from 1 GHz to 40 GHz. The model is surrounded with the outer boundary condition set to radiation.

The performance of the full-wave simulations for the LTCC transition was sufficient for our application (Figure 4.7). The results in Figure 4.7 are normalized to the calculated port characteristic impedance (Figure 4.6) and therefore reduces the reflections due to the port. The transition has a $f_{3\,\mathrm{dB}}$ in excess of 40 GHz. The S_{21} shows a resonance at 38 GHz. The reflection is below −10 dB up to 30 GHz. This performance is good enough for channels working at 40 Gbit s^{-1} and thus it was decided to use this design for the fabricated board presented in Chapter 5.



(a) CB-CPW

(b) SM-CPW

Figure 4.5: The ports used for the full-wave simulation.

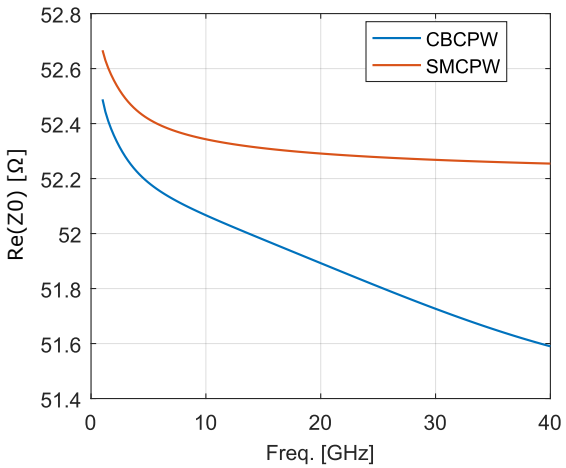
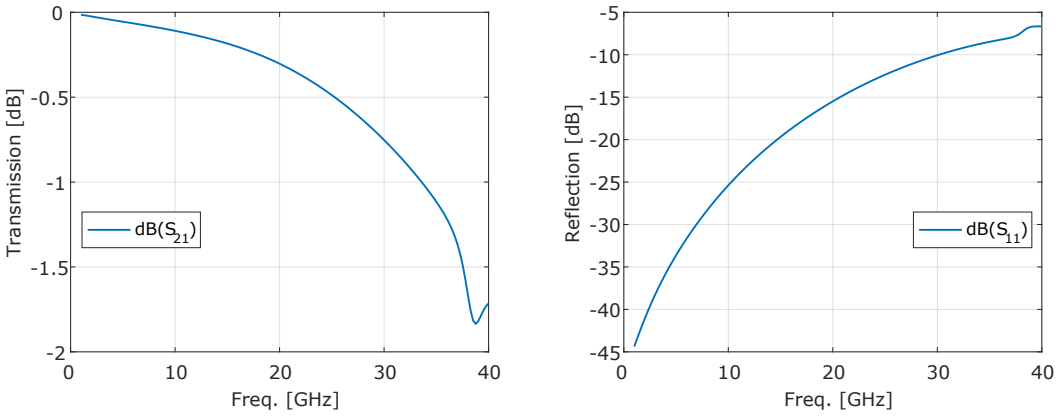
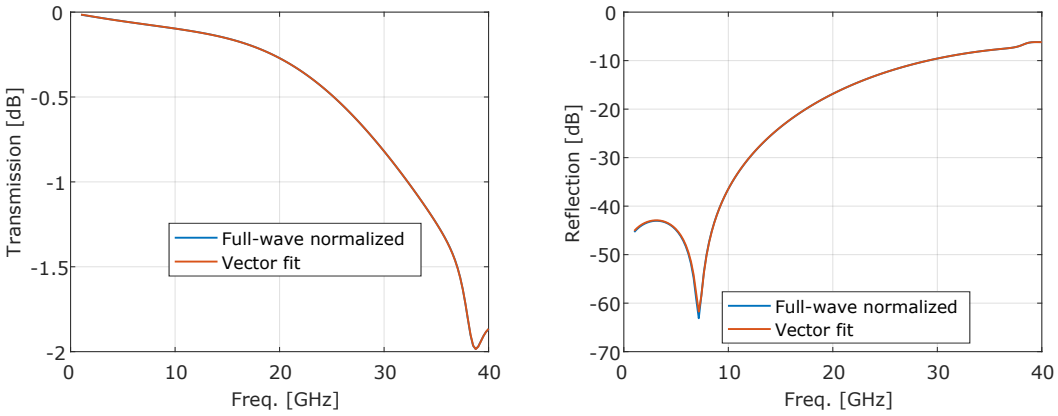


Figure 4.6: The characteristic impedance of the ports used for the full-wave simulation.



(a) (b)

Figure 4.7: The performance of the LTCC transition. The transition has a $f_{3\,\mathrm{dB}}$ in excess of 40 GHz and the reflection is below −10 dB up to 30 GHz.



(a) (b)

Figure 4.8: The performance of the LTCC transition normalized to 50 Ω ports and its vector fitting.

Table 4.3: A vector-fitting model of the CB-CPW to SM-CPW transition

(a) The poles

Re(a)	Im(a)
-9.11×10^{9}	0
-3.79×10^{10}	0
-1.53×10^{11}	0
-1.19×10^{12}	0
-1.55×10^{11}	$\pm 1.36 \times 10^{11}$
-6.84×10^{9}	$\pm 2.42 \times 10^{11}$
-1.45×10^{11}	$\pm 2.66 \times 10^{11}$
-6.07×10^{9}	$\pm 3.65 \times 10^{11}$

(b) The residues

Re(c_{11})	Im(c_{11})	Re(c_{22})	Im(c_{22})	Re(c_{21})	Im(c_{21})
-1.91×10^{7}	0	-9.65×10^{6}	0	1.86×10^{7}	0
-4.16×10^{8}	0	-7.19×10^{8}	0	5.07×10^{8}	0
-2.09×10^{11}	0	-3.86×10^{11}	0	3.34×10^{11}	0
1.1×10^{12}	0	1.27×10^{12}	0	1.83×10^{11}	0
-3.48×10^{11}	$\pm 1.56 \times 10^{11}$	-4.94×10^{11}	$\pm 3.29 \times 10^{11}$	-5.46×10^{11}	$\pm 2.65 \times 10^{11}$
1.59×10^{8}	$\pm 2.86 \times 10^{8}$	-2.12×10^{8}	$\pm 1.44 \times 10^{8}$	7.73×10^{7}	$\pm 3.04 \times 10^{8}$
1.47×10^{11}	$\pm 2.55 \times 10^{11}$	2.81×10^{11}	$\pm 3.67 \times 10^{11}$	3.15×10^{11}	$\pm 2.83 \times 10^{10}$
-1.18×10^{10}	$\pm 1.08 \times 10^{10}$	6.32×10^{7}	$\pm 6.36 \times 10^{9}$	-8.84×10^{9}	$\pm 1.95 \times 10^{10}$

The performance of the LTCC transition normalized to 50 Ω ports and its vector fitting is shown in Figure 4.8. Changing the impedance of the ports is done by using Equation 2.47. The resulting normalized scattering parameters (S-parameters) are then used to create a vector fitting model that can be used to reproduce this results. The vector-fitting algorithm is described in [29]–[31]. The fitting was completed using the publicly available *Matrix fitting toolbox*. The parameter values used in the resulting model are given in Table 4.3. The model uses 12 poles, 4 simple real poles, and 8 complex conjugate pairs. The reconstruction of elements of the S-parameter matrix is given by

$$S_{xy} = \sum_{n \in N} \frac{c_{xyn}}{s - a_n} \tag{4.1}$$

where the summation is done over all the 12 poles, $s = j2\pi f$, a_n is taken from Table 4.4a and c_{xyn} is taken from Table 4.4b, where the missing c_{12} parameters are obtained from $c_{12} = c_{21}$, since the circuit is reciprocal.

Section 4.2.4 presented the full-wave electromagnetic model used to predict the performance of the transition that was fabricated in LTCC. The simulation uses a wave-port whose modes agree with our 2D cross-sectional electromagnetic simulations. The simulated performance from 1 GHz to 40 GHz shows a performance good enough for 40 Gbit s^{-1} channels and a vector-fitting model is provided for the use in circuit simulators.

Section 4.2 presented the design procedure for the microwave vertical transition fabricated in LTCC. The transition was designed by using three 2D cross-sectional simulations, one for the CB-CPW, one for the SM-CPW and, finally, one for a coaxial-like structure. The final geometry of the transition was simulated using a 3D full-wave electromagnetic solver resulting in a simulated performance that is good enough for 40 Gbit s^{-1} channels. A second iteration for this transition was completed, but this time the fabrication technology was co-fired AlN.

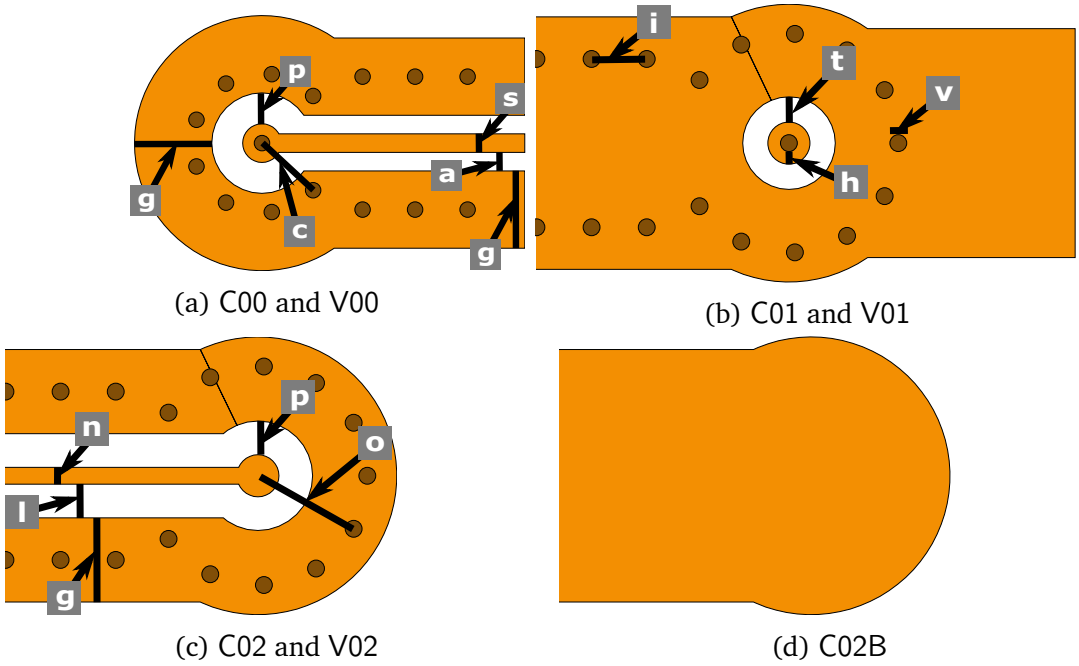
4.3 Co-fired AlN vertical transition

The second vertical transition was designed for fabrication in co-fired AlN. Even though AlN has a worse microwave performance than the LTCC substrate, the microwave performance is better than standard printed circuit board (PCB) substrates, and the high thermal conductivity of AlN makes it attractive for applications involving PICs. This second transition is based on the first transition presented in the previous section but with some improvements and adjustments. Section 4.3.1 describes the general concept of the transition including the improvements over the first version. Section 4.3.2 presents the procedure followed to design this second transition, which is based on an optimisation using time-domain reflectometry (TDR) simulations. Section 4.3.3 presents the final dimensions, that were fabricated, which were obtained from the design optimisation. Finally, Section 4.3.4 presents the 3D full-wave frequency-domain simulation used to simulate the performance of this transition.

4.3.1 General description

The vertical transition is, again, between the CB-CPW and a buried SM-CPW connected by a coaxial-like structure (Figure 4.1). As in the first vertical transition, the design consists of three ceramic layers and four conductor layers (Figure 4.2). Also unchanged, C00 and C02 contain the co-planar circuits and C01 and C03 have the backside grounds that provide the cross-level crosstalk shield. All the parametric dimensions that define the transition are shown in Figure 4.9.

The new geometry has three key differences compared to the first design. First, instead of using only four ground vias for the coaxial-like structure, the number of ground vias in the coaxial-like structure surrounding the signal via is maximised to keep the minimum spacing between vias required by the manufacturing design rules, the desired coaxial radius and to provide space for the signal and gap of the corresponding CB-CPW and SM-CPW. The calculation of the maximum number of vias that can be fitted is done using functions coded in PICDraw by the author. This minimises the radiation of the vertical transition. Second, two distinct coaxial-like structures for each of the first two substrates are used instead of a single one shared in all the layers as before. This provides an additional dimension (o) that is used for optimization purposes. Third and most important, since t is smaller than c and



(a) C00 and V00

(b) C01 and V01

(c) C02 and V02

(d) C02B

Figure 4.9: The geometry of the second iteration of the vertical transition. The new geometry includes some new elements that allow for rotation at any angle of the transition.

o, and the ground vias in the coaxial-like structure are no longer aligned in each substrate layer, the transition can now be rotated around the signal via.

Figure 4.9a shows the dimensional variables used on layers C00 and V00. The parametric dimensions s, a and g define the CB-CPW, where g is the ground width, a is the gap width and s is the signal width. The dimension p is the gap between the signal catch pad and the ground via catch pads. The dimension c is the gap between the signal via and any of the ground vias that form the coaxial-like structure in the top substrate. The dimension g is the ground catch pad width used to connect all the ground vias together in this layer.

Figure 4.9b shows the dimensional variable on layers C01 and V01. The dimension v is the via diameter, which is the same for all the vias in the transition to reduce the fabrication complexity. The dimension h is the signal catch-pad overlay distance. The dimension t is the gap between the signal via catch-pad and the ground via catch-pad in layer C01. The dimension i is the spacing (centre-to-centre) between the ground vias in both the CB-CPW and the SM-CPW.

Figure 4.9c shows the dimensional variables of layers C02 and V02. The catch pad diameter is the same as in the layers C00 and C01. The dimensions g, l and n define the SM-CPW; g the ground width (the same used in layer C00); l the gap width and n the signal width. The dimension p is the gap between the signal catch pad and the ground catch pad in this layer and has been chosen to be the same as the gap in the layer C00 for simplicity. The dimension o is the gap between the signal via and any

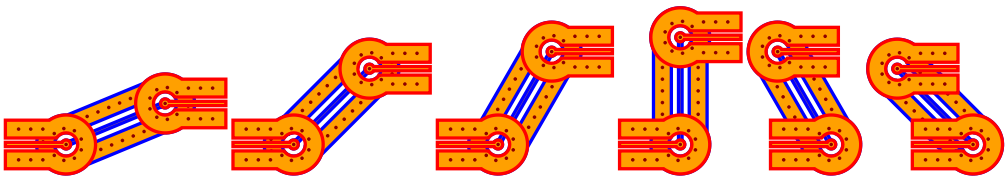


Figure 4.10: The second iteration of the transition allows for arbitrary rotations.

of the ground vias that form the coaxial-like structure in the two substrates that form the SM-CPW.

Figure 4.9d shows the layer C03, that is just the back side ground of the SM-CPW. This layer is like a shadow that covers all the co-planar circuits above it. The geometry in this layer is calculated automatically using a function in PICDraw.

The new geometry allows for the rotation at any angle of the transition. That means that the transition can be rotated around the signal via, thus having arbitrary directions for the CB-CPW and the SM-CPW as shown in Figure 4.10. This new property of this second transition helps to route the channels when complex routing schemes are needed, as is the case for some of the phase modulation devices where each channel must be phase matched. The performance under different rotation angles is explored in Chapter 6.

A function was created in PICDraw to create the 2D layouts of the transition for any combination of the parameters shown in Figure 4.9. The function calculates all the dimensions necessary to maintain the same length of the of the transition and to maximize the number of ground vias in both coaxial-like structures. The resulting layouts are used for both our electromagnetic simulations and fabrication.

4.3.2 Design procedure

The new transition was optimized by using the full-wave time-domain electromagnetic solver to perform a TDR, using the TDR results to locate the source of reflections and then manually modifying the parametric dimensions that form the vertical transitions to minimise the reflections. This follows a similar procedure to [32]. The reason for taking this approach is that the frequency-domain results given by the scattering parameters (S-parameters) give us information of the performance of the overall transition but does not point to the location of the source of reflections. In contrast, the time-domain information can be mapped to the position of the source of the reflection and thus give us more information for the optimization.

The 2D layouts created in PICDraw were imported into our full-wave simulator by using the script in Appendix A.3 (Figure 4.11). Layer D00 is 127 µm thick and layers D01 and D02 are 254 µm thick. The metal is gold with a thickness of 3 µm for all the layers, based on the fabrication design rules. The manufacturing design rules force the minimum metal width to be 100 µm, the spacing between vias (i) to be greater than 300 µm, and the via catch pad (h) to be greater than 75 µm. The co-planar ground width (g) must be large enough to fit the ground vias. The full-wave model

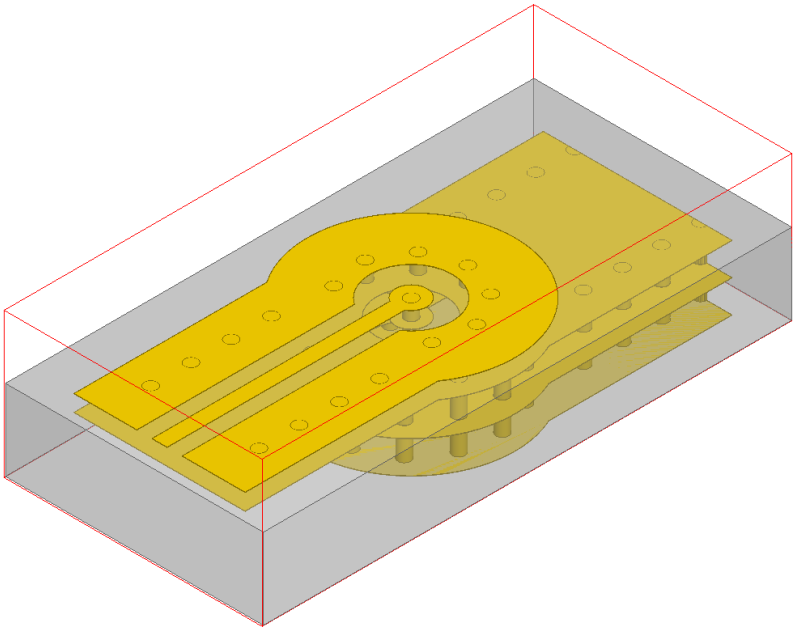
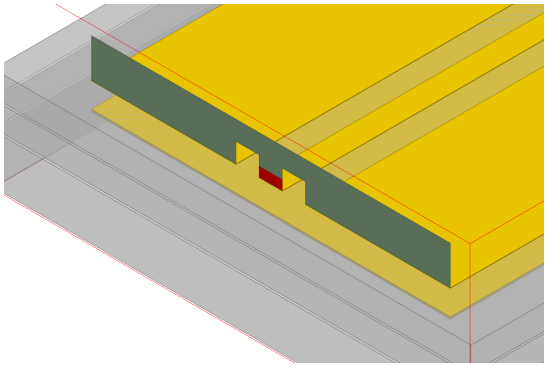


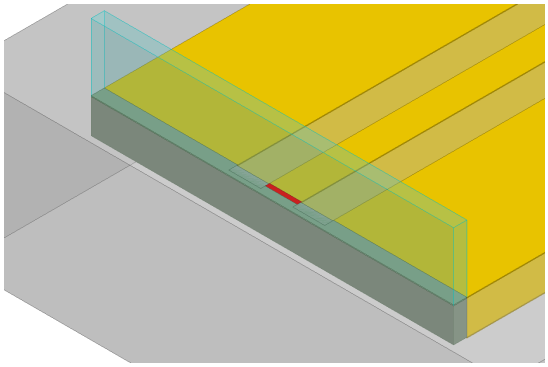
Figure 4.11: The geometry imported to the time-domain full-wave electromagnetic solver.

includes a top layer of air with a thickness of 500 µm. The material models used are given in Table 3.2.

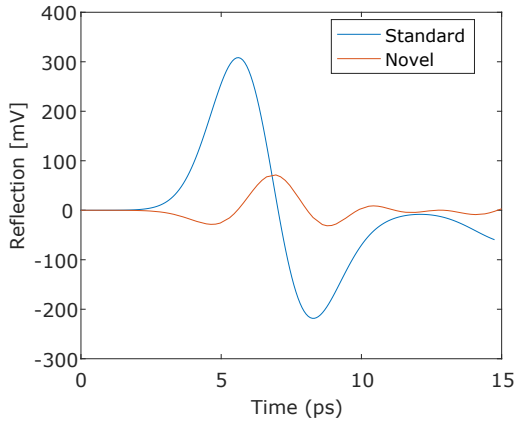
A novel port was created for the full-wave time-domain electromagnetic solver (Figure 4.12). The time-domain full-wave electromagnetic solver does not allow for wave-ports in the case of a CPW since the transmission line has multiple dielectrics and a lossy dielectric (Section 2.5.2). A standard lumped port was created (Figure 4.12a) based on the software documentation and on [33]–[38]. The standard lumped port results showed a notable reflection (Figure 4.12c). To reduce this reflection created by the port, a novel version (Figure 4.12b) was created in this research which reduces the reflections from the port compared to the standard lumped port (Figure 4.12c). The idea of the novel lumped port is to surround the three-leg standard lumped port by a box of Perfect E boundary conditions. The novel lumped port uses a standard three-leg lumped port but, in order to be able to surround it by the Perfect E boundary, it is placed horizontally on top of the substrate surface where the co-planar metals lie. Surrounding boxes of air and AlN are added. A Perfect E boundary condition is applied to the faces of this box except for the faces where the three-leg lumped port sits and the faces normal to the transmission line direction and touching the transmission line. Two of the dimensions of these boxes are chosen to match with the two dimensions of the three-leg lumped port. The height of the air box must be large enough to avoid coupling from the small square port to the top surface of the air box. The height of the AlN box is chosen as the distance between the coplanar metals and the backside ground metal. In this way, the grounds at the two levels



(a) Standard

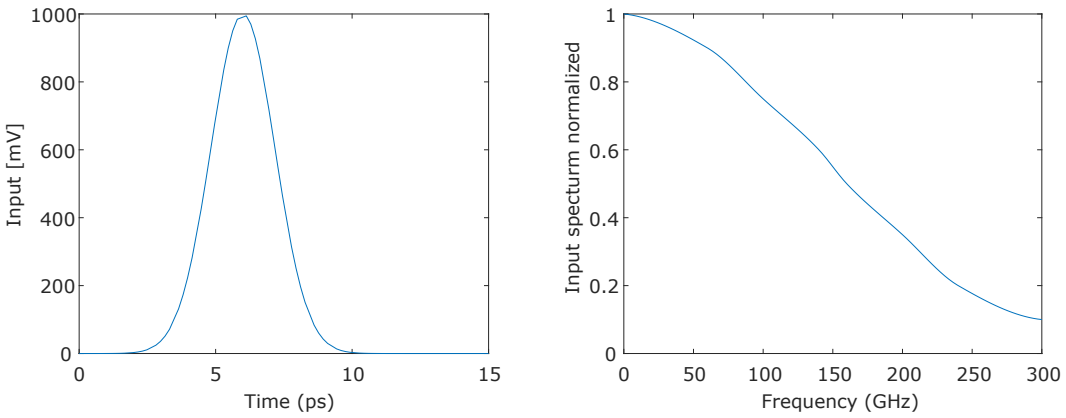


(b) Novel



(c) Reflections

Figure 4.12: The lumped ports created for the time-domain full-wave electromagnetic solver. The novel version, created in this research, reduces the reflections from the port compared to the standard lumped port. The input amplitude is 1 V.



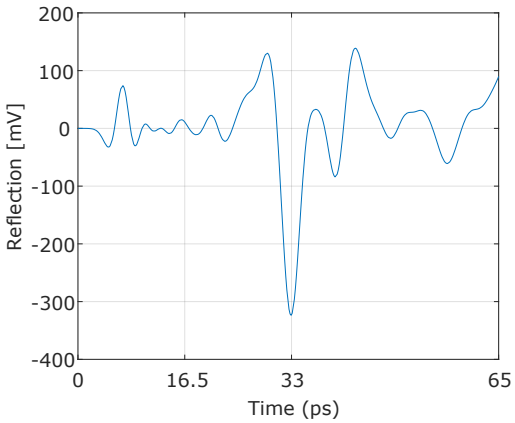
(a) (b)

Figure 4.13: The input voltage profile used in the time-domain simulations.

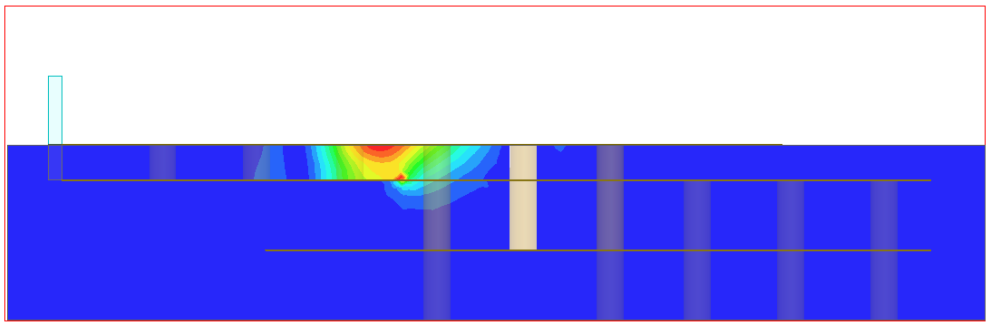
are shorted together by the Perfect E boundary conditions at the faces of the box. Finally, the dimension of the lumped port in the direction of the transmission line must be small enough to avoid resonances at frequencies contained by the input voltage profile but as large as possible to avoid increasing the number of points in the mesh around the port. A port that is too small consumes a lot more computer memory and computational time. In our case, the port is 20 µm for a Gaussian input profile with a full width at half maximum (FWHM) of 3 ps.

The solver was set up to use a Gaussian input profile with a FWHM of 3 ps (Figure 4.13a). The shorter the pulse the more detail that the reflections can resolve. However, the shorter the pulse the finer the meshing and thus the higher the memory and computer time. The 3 ps pulse is the shortest that the memory in the available computer was able to simulate. The time step is set to 0.1655 ps. The profile shown in Figure 4.13a is maintained as 0 V after 15 ps. The 3 ps pulse has a spectral content with frequencies up to 300 GHz (Figure 4.13b). The model is surrounded by the outer boundary condition set to radiation.

The results can be used to identify the regions that are creating the unwanted reflections. For example, the simulated reflection for the initial version of the AlN transition using the same design procedure as in Section 4.2 is presented in Figure 4.14a. The reflection has the highest reflection at time 33 ps. This is the reflection measured at the port, therefore, the event that created this reflection occurred at half this time (i.e. 16.5 ps). This is because the reflected signal has to travel back to the port and it takes exactly the same time for the pulse to get to the source of the reflection as it does to come back to the port. Once the timing of the event has been located, the fields can be inspected to translate this reflection to a location in the geometry of the transition. For example, Figure 4.14b shows the field at the cross-section at the centre of the transition at the closest time of the event that was solved by the simulator (16.6 ps). One question that remains is how much the reflected voltage is affected by the input voltage profile and the multiple reflections the pulse creates

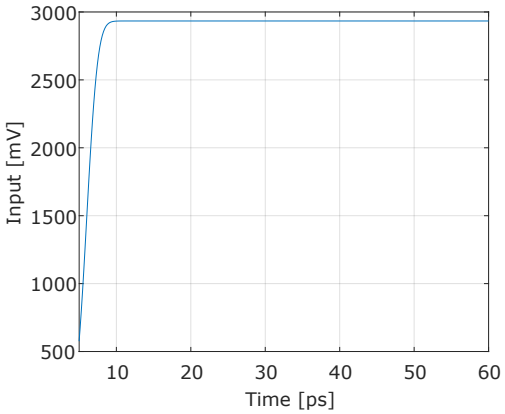


(a) Simulated reflection

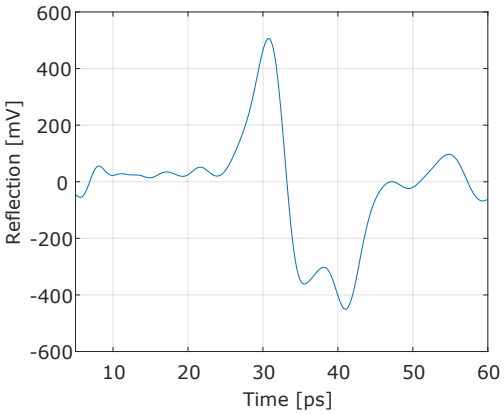


(b) The field cross-section at time 16.6 ps

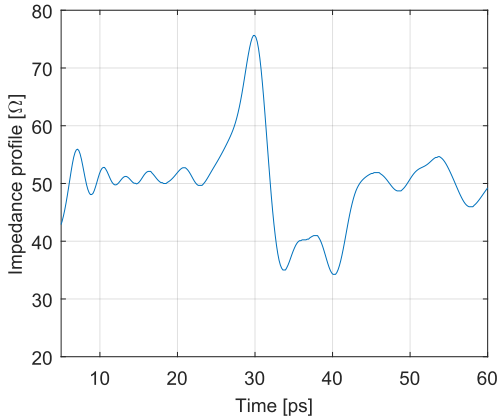
Figure 4.14: The reflection of the initial version of the transition and the field at the time that creates the maximum reflection. Input voltage showed in Figure 4.13a. The simulation can be used to locate the source of reflections.



(a) Integrated input voltage



(b) Integrated reflected voltage

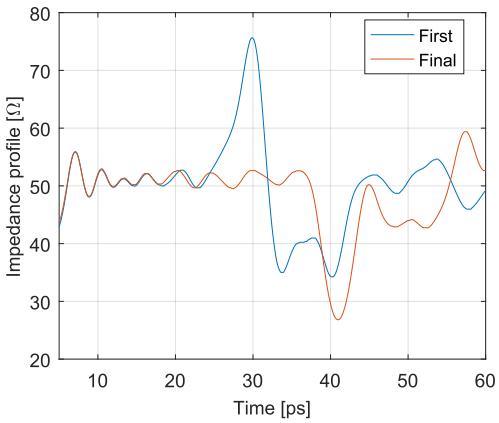


(c) Reconstructed impedance profile

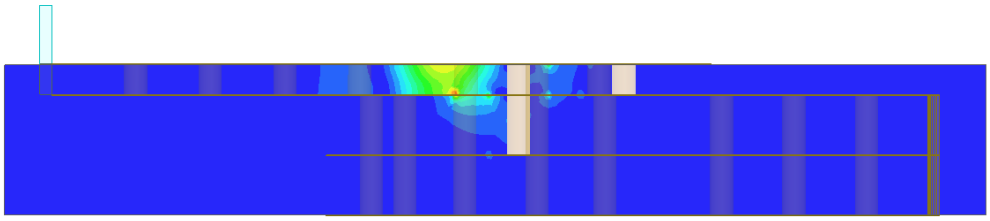
Figure 4.15: The reconstructed impedance (c) from the integrated input voltage (b) and reflected voltage (a).

before coming back to the port.

The multiple reflection TDR algorithm, described in Section 2.2.4, was used to recover an impedance profile that takes into account the shape of the input voltage waveform and the multiple reflections that occur in the transition. The reconstruction fails when using the Gaussian input profile. The algorithm presents non-linear oscillations that the stabilisation modification is not able to solve for the impedance profile. Based on the full-wave electromagnetic solver documentation, the input voltage profile and the reflection are integrated. After integration, the input profile is similar to the Heaviside's step function (Figure 4.15a). The reflected voltage is also integrated (Figure 4.15b). The integrated input voltage and integrated reflected voltage were used in the impedance reconstruction by a TDR algorithm. The input voltage starts at zero and thus the algorithm presents problems with division by zero and numerical errors. Therefore, the first 5 ps of the input voltage and the reflected voltage were removed, setting the front-wave voltage to 500 mV. The resulting



(a) Impedance reconstruction first version vs final version



(b) The field cross-section at time 21 ps

Figure 4.16: A comparison of the reconstructed impedance profile for the first version and the final version. The final version presents a single low impedance section at 42 ps which relates to the events at time 21 ps.

impedance profile (Figure 4.15c) takes into account the shape of the input profile and the multiple reflections in the device.

The vertical transition was manually optimised by using the time-domain full-wave simulation and the impedance recovery algorithm. The optimisation process consisted of performing the time-domain full-wave simulation, using the results in the impedance reconstruction algorithm by TDR, locating the regions that generate the maximum impedance mismatch and then manually changing design parameters related to the localised region. A total of 36 different versions were simulated. The variable that made the largest change in the simulated results was the radius of the coaxial iris in the CB-CPW backside ground metal (t). A optimization sweep in t showed that the design works better if t is smaller than the gap in the coaxial-like catch pads (p).The comparison between the starting design and the final design is shown in Figure 4.16a. The impedance profile of the final version shows a low characteristic impedance section centred at 42 ps. The author was not able to remove this feature by means of changing any of the variables shown in Figure 4.9. However, the impedance discontinuity is shorter than in the first design and all the high

Table 4.5: Dimensions in µm of the fabricated transition

s	a	g	c	p	i	t	h	v	l	n	o
120	120	500	450	200	$\gtrapprox$ 300	150	75	100	200	100	650

impedance discontinuities were removed. The examination of the electromagnetic fields at time 21 ps (Figure 4.16b) shows that the low impedance discontinuity is located at the start of the vertical transition.

4.3.3 Final design

The fabrication design rules imposed several constraints. In our case, the board was fabricated by Kyocera. The fabrication required gold metallization with a thickness of 3 µm for all metal layers. The vias diameters after co-firing are 100 µm (i.e. $v = 100\,\mu m$). Circular catch pads covering the metal vias were needed to ensure contact between the planar metal and the via fill, and the catch pad diameter needed to be 50 µm bigger than the via diameter (i.e. $h > 25\,\mu m$). The minimum feature size (metal line or gap between metals) was 100 µm. The minimal spacing between adjacent vias is 300 µm from centre to centre (i.e. $i > 300\,\mu m$). The substrate thickness could only be a multiple of 127 µm.

The final dimensions of the optimized design are given in Table 4.5. The CB-CPW dimensions (s and a) and the SM-CPW dimensions (n and l) were defined by simulating the transmission line in the 2D cross-sectional electromagnetic solver to get 50 Ω characteristic impedance and the smallest dimensions that could be fabricated. The ground width (g) is 500 µm; which is large enough to fit the ground vias in the middle of it without disturbing the characteristic impedance (Section 3.3). The dimensions c, p, t, h and o were optimised using the procedure described in Section 4.3.2. The space between vias is chosen to be the smallest allowed by the geometry that complies with the fabrication requirement of $i > 300\,\mu m$. In order to achieve a good arrangement of the vias, several functions for PICDraw were written to calculate the smallest dimensions that fit the geometry and the fabrication requirements. The via diameter (v) is 100 µm which is the smallest via diameter that the fabrication rules allow.

The vertical transition layout for the metal layers was drawn using PICDraw. Once the layout of the vertical transition was drawn in PICDraw, the 2D layouts were imported into our 3D full-wave simulator.

4.3.4 Simulated performance

The 3D model of the final design of the vertical transition for co-fired AlN was imported for the full-wave electromagnetic simulation of the transition and is shown in Figure 4.17. As before, the script in Appendix A.3 was used for this purpose. The

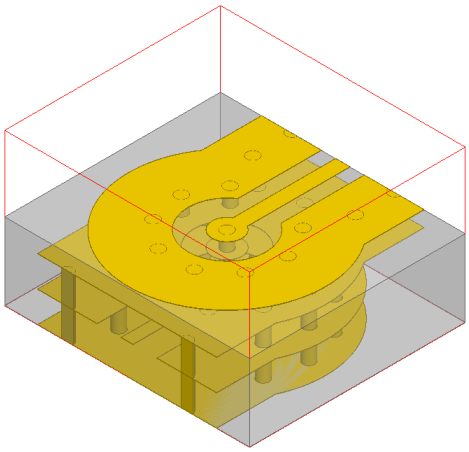


Figure 4.17: The AlN vertical transition geometry imported to the frequency-domain full-wave electromagnetic solver.

material properties used in the model are shown in Table 3.2. The 3D model contains an air layer on the top of thickness 200 µm.

The excitation ports used in the model are wave ports as in the previous case of the first vertical transition. The ports are placed so they cut the shield vias (Figure 4.17). This is done to have a single mode port, since the shield vias eliminate the CPW odd mode. The port fields show that the modes are as expected from the cross-sectional simulation (Chapter 3) and as confirmed by the calculated characteristic impedance (Figure 4.18).

The solver was set up to perform the mesh refinement at 40 GHz and a sweep from 1 GHz to 40 GHz. The model is surrounded by the outer boundary condition set to radiation.

The performance of the full-wave simulation for the co-fired AlN transition (Figure 4.19) is similar to the results obtained for LTCC. The results shown in Figure 4.19 are normalized to the calculated port characteristic impedance (Figure 4.18) and therefore eliminates the reflections due to the port. The transition has a $f_{3\,\mathrm{dB}}$ in excess of 40 GHz, while the reflection is below −10 dB up to 33 GHz. This performance is good enough for channels working at 40 Gbit s^{-1} and thus it was decided to use this design for the fabricated board presented in Chapter 6.

The performance of the co-fired AlN transition normalized to 50 Ω ports and its vector fitting is shown in Figure 4.20. Changing the impedance of the ports is done by using Equation 2.47. The resulting normalized scattering parameters (S-parameters) is then used to create a vector fitting model that can be used to reproduce this results. The fitting was completed using the publicly available *Matrix fitting toolbox*. The resulting model is given in Table 4.6, the model consists of 7 poles, 1 simple real pole and 6 complex conjugate pairs of poles. The reconstruction of elements of the S-parameter matrix is given by Equation 4.1 where the summation is done over all the 7 poles, $s = j2\pi f$, a_n is taken from Table 4.6a and c_{xyn} is taken from Table 4.6b,

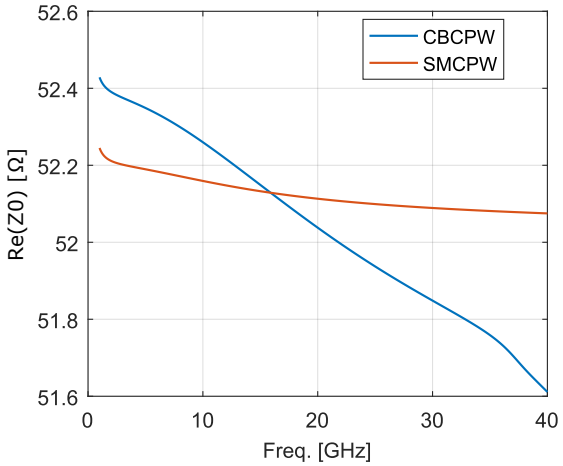
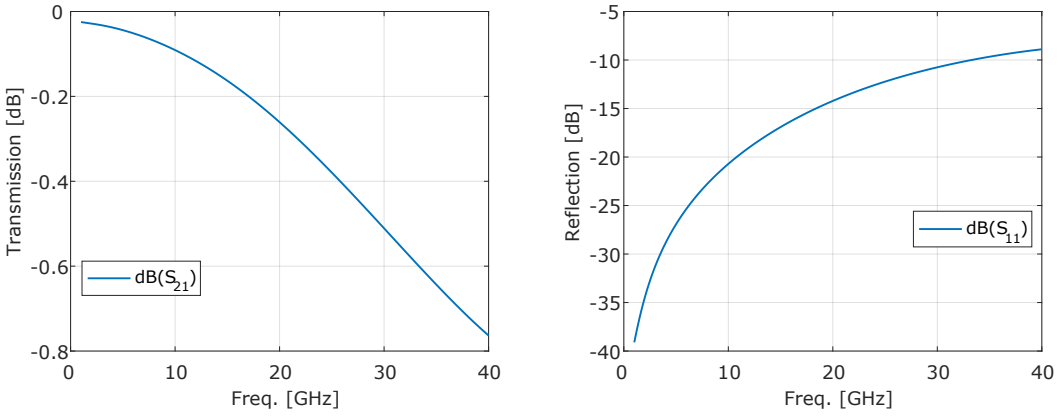
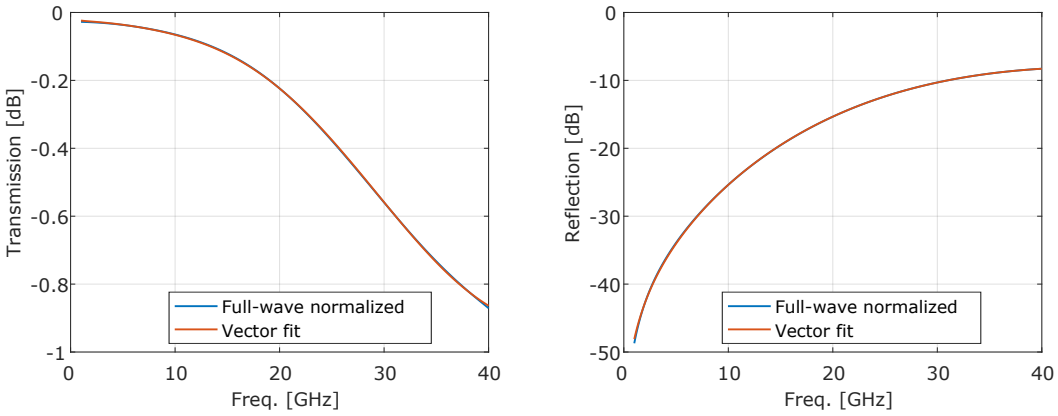


Figure 4.18: The characteristic impedance of the ports used for the full-wave simulation of the transition in co-fired AlN.



(a) (b)

Figure 4.19: The performance of the co-fired AlN transition. The transition has a $f_{3\,\mathrm{dB}}$ in excess of 40 GHz and the reflection is below −10 dB up to 33 GHz.



(a) (b)

Figure 4.20: The performance of the co-fired AlN transition normalized to 50 Ω ports and its vector fitting.

Table 4.6: A vector-fitting model of the CB-CPW to SM-CPW transition

(a) The poles

Re(a)	Im(a)
-1.52×10^{11}	0
-1.53×10^{11}	$\pm 1.12 \times 10^{11}$
-1.6×10^{11}	$\pm 2.16 \times 10^{11}$
-8.41×10^{10}	$\pm 3.35 \times 10^{11}$

(b) The residues

Re(c_{11})	Im(c_{11})	Re(c_{22})	Im(c_{22})	Re(c_{21})	Im(c_{21})
-2.23×10^{11}	0	-5.56×10^{10}	0	3.14×10^{11}	0
-8.46×10^{10}	$\pm 3.06 \times 10^{11}$	-1.18×10^{11}	$\pm 1.82 \times 10^{11}$	-2.02×10^{11}	$\pm 3.37 \times 10^{11}$
2.06×10^{11}	$\pm 1.32 \times 10^{11}$	2.98×10^{11}	$\pm 1.4 \times 10^{11}$	-3.51×10^{10}	$\pm 3.39 \times 10^{11}$
-1.77×10^{10}	$\pm 3.31 \times 10^{10}$	-1.1×10^{11}	$\pm 1.53 \times 10^{10}$	6.63×10^{10}	$\pm 1.16 \times 10^{11}$

where the missing c_{12} parameters are obtained by using $c_{12} = c_{21}$, since the circuit is reciprocal.

Section 4.3.4 presented the full-wave electromagnetic model used to predict the performance of the second transition that was fabricated in co-fired AlN. The simulation uses a wave-port, whose modes agree with our 2D cross-sectional electromagnetic simulations. The simulated performance from 1 GHz to 40 GHz shows a performance high enough for 40 Gbit s^{-1} channels and a vector-fitting model is provided for use in circuit simulators.

Section 4.3 presented the design procedure of the microwave vertical transition fabricated in co-fired AlN. The transition has the advantage that it can be rotated at an arbitrary angle. The vertical transition was optimised using a 3D full-wave time-domain electromagnetic solver and an impedance recovery TDR algorithm. The final design has a simulated performance in the frequency-domain that is good enough for 40 Gbit s^{-1} channels.

Chapter 4 presented the work done to design two vertical transitions between a CB-CPW and an SM-CPW (Chapter 3). An analysis of the state of the art on vertical transition was provided showing the need for a transition with crosstalk shielding, standard fabrication features, and good microwave performance. The first of the two transitions was designed using a 2D cross-sectional electromagnetic solver and the full-wave electromagnetic solver to check the frequency-domain performance. Starting from this first transition, the full-wave time-domain solver and the impedance reconstruction by TDR algorithm was used to optimise the second transition. The second vertical transition presents a better simulated-performance while also having the useful characteristics of allowing for arbitrary rotations. The transitions designed in this chapter compare positively in that they provide better performance than other vertical transitions that also provide shielding to the environment, cross-level crosstalk and that only use standard commercially available features. Both transitions were fabricated. The measured performance of the first vertical transition is presented in the next chapter (Chapter 5) and the measurements of the second transition are presented in Chapter 6.

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Chapter 5
The characterisation of an interposer in LTCC

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This chapter presents the characterisation of the transmission lines (Chapter 3), the first vertical transition (Chapter 4) and other structures fabricated in low-temperature co-fired ceramic (LTCC). First, Section 5.1 presents an analysis of the dimensional variations of the fabricated board. The analysis of the dimensional variations is needed to understand the deviations from the models used to design the structures. Following, Section 5.2 presents the measurements done to characterise the transmission lines, the conductor backed co-planar waveguide (CB-CPW) and the shielded multi-layer co-planar waveguide (SM-CPW). Next, Section 5.3 presents the measurements that characterise the performance of the first vertical transition (Section 4.2). Finally,

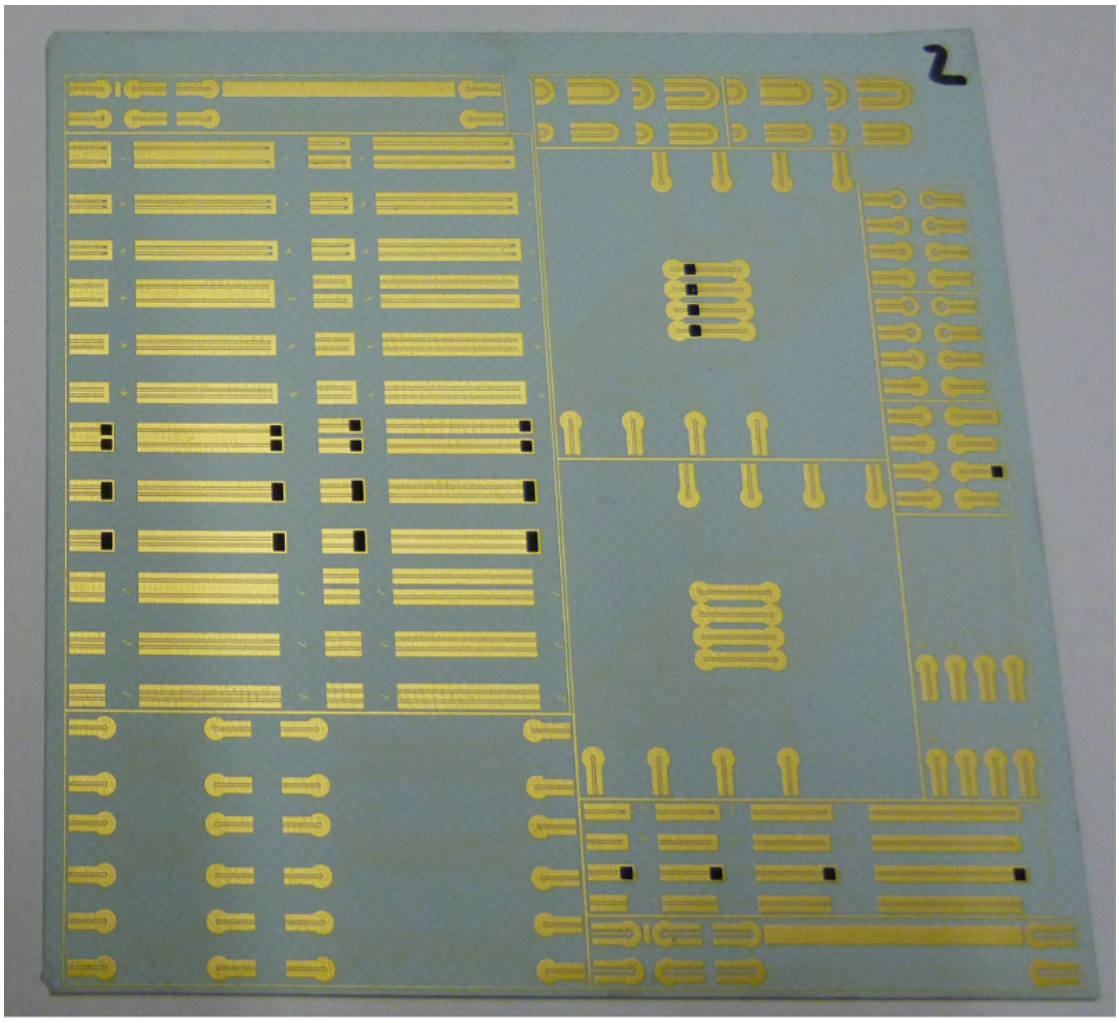


Figure 5.1: A picture of the board fabricated in LTCC.

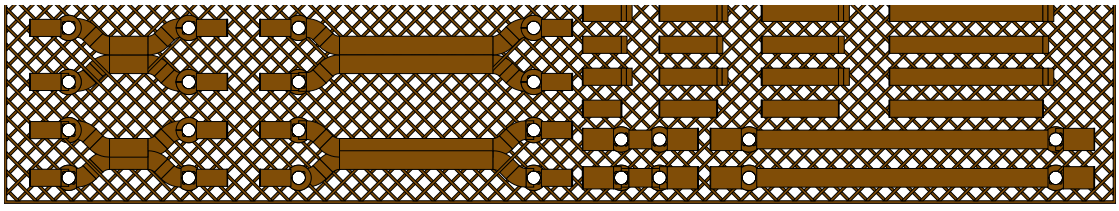


Figure 5.2: The mesh ground used in the LTCC board (C01).

Section 5.4 presents the measurements of some other structures fabricated to explore some complementary research ideas.

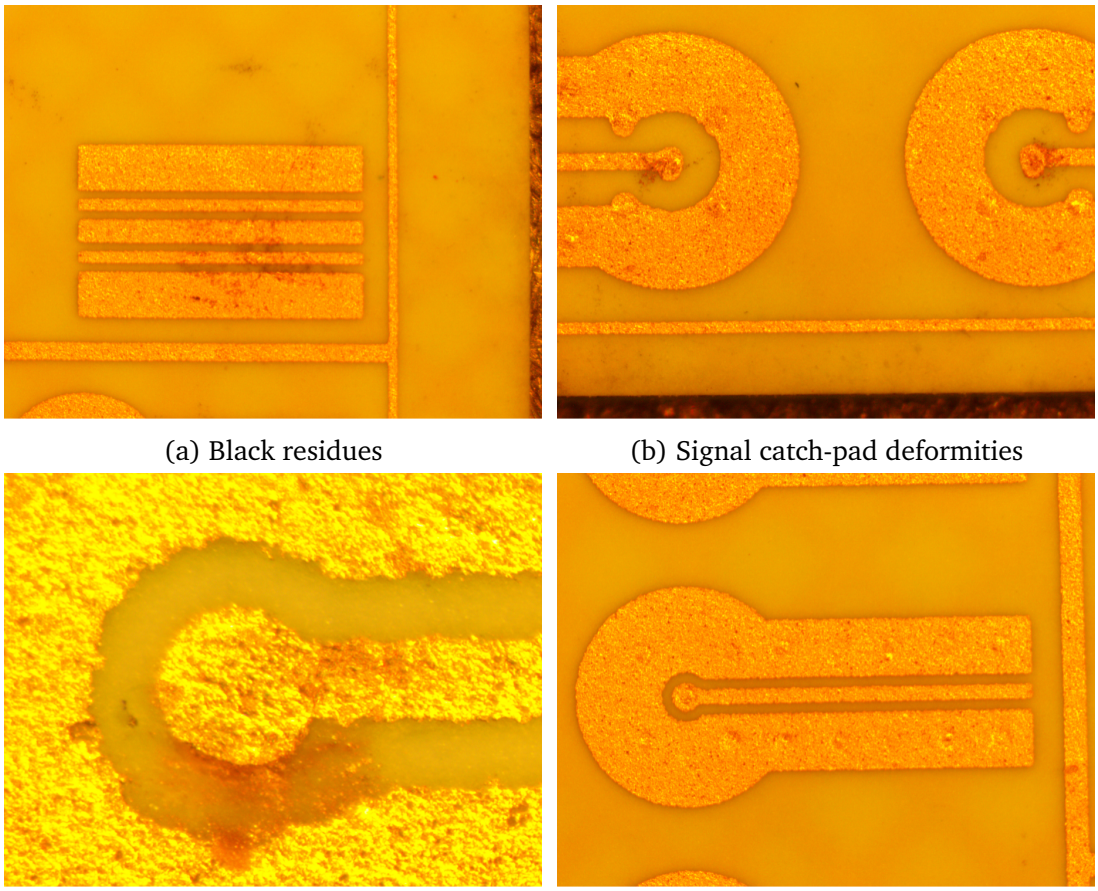
Three LTCC boards were fabricated at the École de Technologie Supérieure (ÉTS) using Dupont 9K7 substrates (Figure 5.1). The shape of the fabricated boards is a square with length equal to 8.7 cm. The gold metallization has a target thickness of 8 µm for all metal layers. The substrate thickness could only be a multiple of 127 µm. The thickness of the top dielectric substrate (W_{00} in Figure 4.3) is 127 µm, and the thickness of the two following layers (W_{01}) are both 254 µm . The thicker ceramics are needed to get the SM-CPW to be 50 Ω and to be compliant with the design rules. All the vias were made with stencils with 150 µm diameters; however, after co-firing and due to shrinking, the final diameter of holes is expected to be 136 µm. Circular catch pads covering the metal vias were needed to ensure contact between the planar metal and the via fill, and the catch pad diameter needed to be 100 µm bigger than the via diameter. The minimum feature size (metal line or gap between metals) is 100 µm. The minimal spacing between adjacent vias is 450 µm from centre to centre. The three boards have the same layout. The fabricated layout for the top circuits and the buried circuits is shown in Figure 1.15. The ground layers use a meshed structure (Figure 5.2) to interconnect all the ground structures. This ground layer cannot be a solid metal due to shrinkage problems that a solid ground can create while the ceramics are co-fired.

5.1 Dimensional characterisation

Several dimensions of the LTCC board were measured to characterise the fabrication. First, Section 5.1.1 discusses the findings of a visual inspection of the board. Then, Section 5.1.2 presents some measurements done to characterise the metal thickness and the metal roughness. After that, Section 5.1.3 present dimensional measurements to characterise the rectangular features.

5.1.1 Visual inspection

Three types of recurrent defects were found in the visual inspection (Figure 5.3). The first type of defect is black residues (Figure 5.3a). These residues probably come from the thick film resistor used to create terminations. These residues were both spread or localised on single spots; however, none of these defects short the metals. The second type of defect is deformities in the signal catch-pad (Figure 5.3b). The vias seem to create recesses that create a visual discontinuity in the metals. From these discontinuities, the position of the vias is distinguishable. These recesses also seem to be the reason of why several signal catch-pads are deformed. The third type of recurrent defect is metal splashes (Figure 5.3c). These metal splashes are more frequent in the coaxial-like structure signal catch-pads but also appear in the co-planar waveguide (CPW) structures. As in the case of the resistor residues, the



(a) Black residues

(b) Signal catch-pad deformities

(c) Metal splashes

(d) No defects

Figure 5.3: Recurrent visual defects found on the LTCC board.

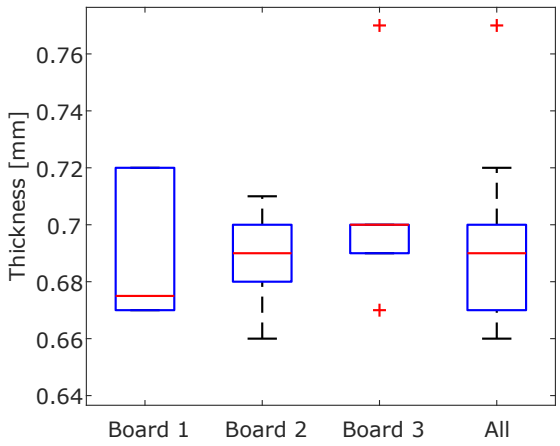


Figure 5.4: The measured overall thickness of the LTCC boards.

metal splashes do not short the metals. Despite these defects, the LTCC boards provided plenty of structures free of visual defects (Figure 5.3d).

The board thickness was measured using a Vernier calliper (Figure 5.4). Three boards were measured at six different locations, the same approximated relative locations were used in each board. The Vernier calliper's resolution is 0.01 mm. The measurements from each of the three boards have similar distributions. The overall thickness used for the design of the circuit is 762 µm, assuming that the metal gets embedded in the substrate, and that the metals do not contribute to the overall thickness. In comparison, the mean of all the measurements is 693.9 µm, which is thiner than the one used for the design. This smaller thickness indicates that the substrate has shrunken during the co-firing process and that the layers are multiples of 115 µm rather than 127 µm.

5.1.2 Metal characterisation

The metal thickness was measured using a contact profilometer with a 5 µm stylus. Three profiles were measured over the substrate, over the metal, and in a metal step (Figure 5.5). The substrate presents variations of around 3 µm. Furthermore, the metal presents similar variations probably caused by the substrate roughness while depositing the metal. The metal roughness creates additional losses at sufficiently high-frequencies. In order to measure the metal thickness, the profile of a step was measured. The measurement of the step shows that the metal increases linearly to a maximum thickness over a length of around 100 µm and that the maximum metal thickness is around 3 µm. This means that the thickness of the metal is comparable to the substrate roughness. This fact is especially clear when the signal metal (100 µm width) was measured. The metal was indistinguishable in the profile. This is an important deviation from the thickness used in the simulations, 8 µm, during the design.

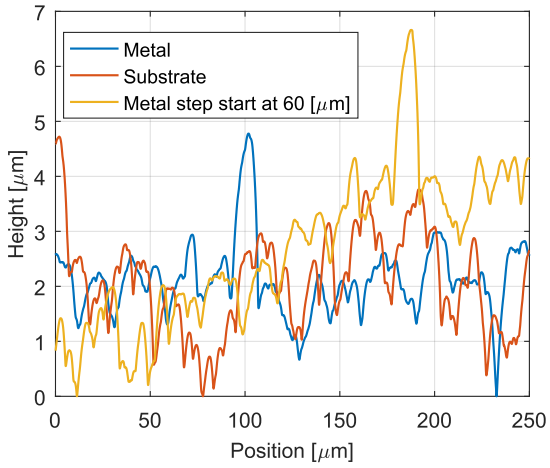


Figure 5.5: The surface profiles of the LTCC board. The substrate and the metal are rough. The metal is not a step but rather a linear increase to a maximum thickness of 3 µm.

5.1.3 Characterisation of rectangular features

The gap width and the signal width of the CB-CPW were measured as well as the corners of the rectangular features. The gap and the signal width were measured in order to verify the fabricated dimensions and to characterise the fabrication variation. The corners of the rectangular features were measured by fitting a circle and recording the diameter of that circle. The smaller the diameter means the sharper the corner. A total of 40 gap widths were measured, the mean value of these measurements is 96.25 µm (Figure 5.6). The layout specified a gap of 100 µm and thus, the gap is 3.75 µm smaller than expected. The interquartile range for the gap measurements is 5.75 µm. A total of 20 signal widths were measured, and the mean value of these measurements is 124.40 µm (Figure 5.6). The interquartile range for the gap measurements is 7 µm. The layout specified a gap of 120 µm so the signal width is 4.4 µm larger than expected. Thus, the gap is shorter than specified by a similar length as the signal is longer than specified. A total of 80 corners were measured; the mean value of the fitted circle diameter is 77 µm with an interquartile range of 34.82 µm (Figure 5.6). A corner that visually looks very square has a diameter of 35 µm. The distribution presents a long upper tail that corresponds to very rounded corners or defects.

In conclusion, Section 5.1 presented some recurrent defects, found by visual inspection that might account for variations in the electrical measurements. The measurement of the overall board thickness suggests that the substrate thickness is 115 µm rather than 127 µm. The substrate and the metal surfaces were found with significant roughness and the metal thickness is found to be around 3 µm, a significant deviation to the 8 µm used during the design. The measurement of several rectangular and circular geometries found that the fabricated dimensions are close

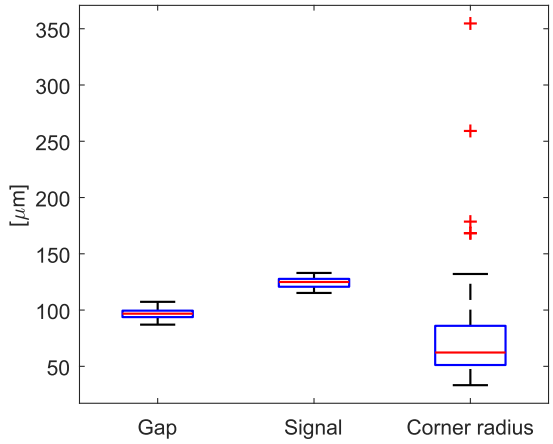


Figure 5.6: Measurements to characterise the rectangular structures in the LTCC board. The gap label refers to the gap width of the CB-CPW and the signal label refers to the signal width of the CB-CPW.



Figure 5.7: The structures used to characterise the CB-CPW. The four lengths are 3.1 mm, 4.6 mm, 6.1 mm and 12.1 mm.

to the designed dimensions and that some of the rectangular corners are defects. All these findings must be accounted for when comparing the simulated to measured results.

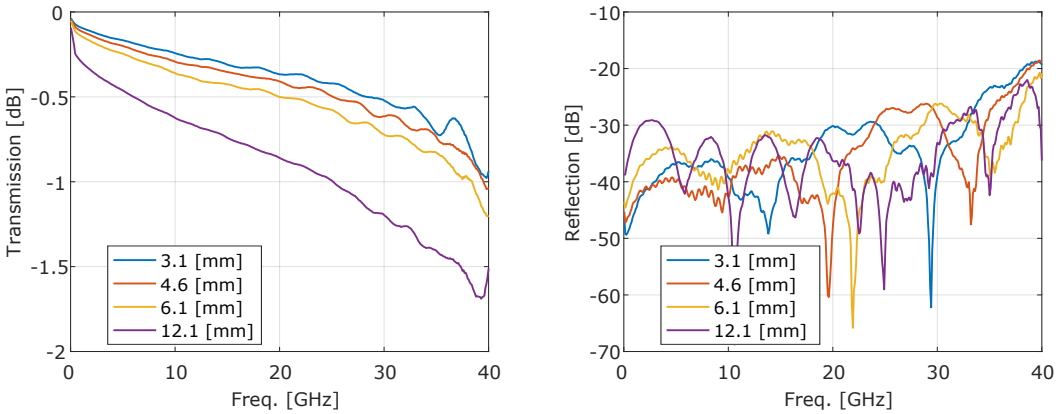
5.2 Transmission lines

The transmission lines were measured using a vector network analyser (VNA). First, Section 5.2.1 presents the measurements done to characterise the CB-CPW. Next, Section 5.2.2 does the same for the SM-CPW. Finally, Section 5.2.3 presents the measurements of some structures fabricated to explore the effect of the ground vias in the performance of the transmission lines.

5.2.1 CB-CPW

Four different lengths of CB-CPW lines were fabricated in the LTCC board (Figure 5.7). The lengths of the lines measured are 3.1 mm, 4.6 mm, 6.1 mm and 12.1 mm. A first-tier short-open-load-thru (SOLT) calibration was performed using a commercial calibration substrate. Three fabricated copies, one for each of the fabricated boards, were available for each length.

The scattering parameters (S-parameters) measured directly from with the VNA



(a) (b)

Figure 5.8: Transmission and reflection measured with the VNA for the CB-CPW structures on the LTCC board. The measurements show some deviations from a perfect transmission line model.

(Figure 5.8) show some deviations from the simple transmission line model (Figure 2.15). The plots shown in Figure 5.8 are the average of the three available measurements. The transmission (Figure 5.8a) shows some peaks around 38 GHz. The reflection (Figure 5.8b) increases with the frequency and the quarter wave-length minimums are not clearly defined.

Assuming that the measurements from the VNA represent only the transmission line, the transmission line parameters were calculated for each of the lines (Figure 5.9). The transmission line parameters were calculated by getting the ABCD matrix (Equation 2.29) and then using Equation 2.36. The calculated transmission lines parameters show multiple deviations from the expected results. The characteristic impedance (Z_0) shows errors (Figures 5.9a and 5.9b) related to the quarter-wavelength resonances. These type of errors are found in the literature ([1]–[5]) and are avoided by measuring short transmission lines. The attenuation (α) in Figure 5.9c shows that the attenuation for the different lines is not consistent; the shorter lines have the higher attenuation. This fact points to an additional loss due to the coupling between the VNA probe and the CB-CPW. The phase propagation constant (β) in Figure 5.9d follows the expected behaviour for all lines. In order to remove these parasitic features, a second-tier calibration was performed.

A thru-only calibration was performed as the second-tier calibration. The shortest element in the fabricated board is 3.1 mm long; however, this line is too long to comply with the single shunt impedance assumption (Section 2.4.1). In order to get a shorter thru, the transmission lines include 50 µm probe pads. Due to this fact, a short thru of 100 µm can be recovered by Equation 2.35 [1], [6], [7] where we have two pairs to calculate the 100 µm thru: the pair with 3.1 mm and 6.1 mm lines or the pair with 6.1 mm and 12.1 mm lines. The A, B and the C parameters of the calculated 100 µm thru show that $A \approx 1$ and $C \approx 0$ (Figure 5.10) and therefore, the

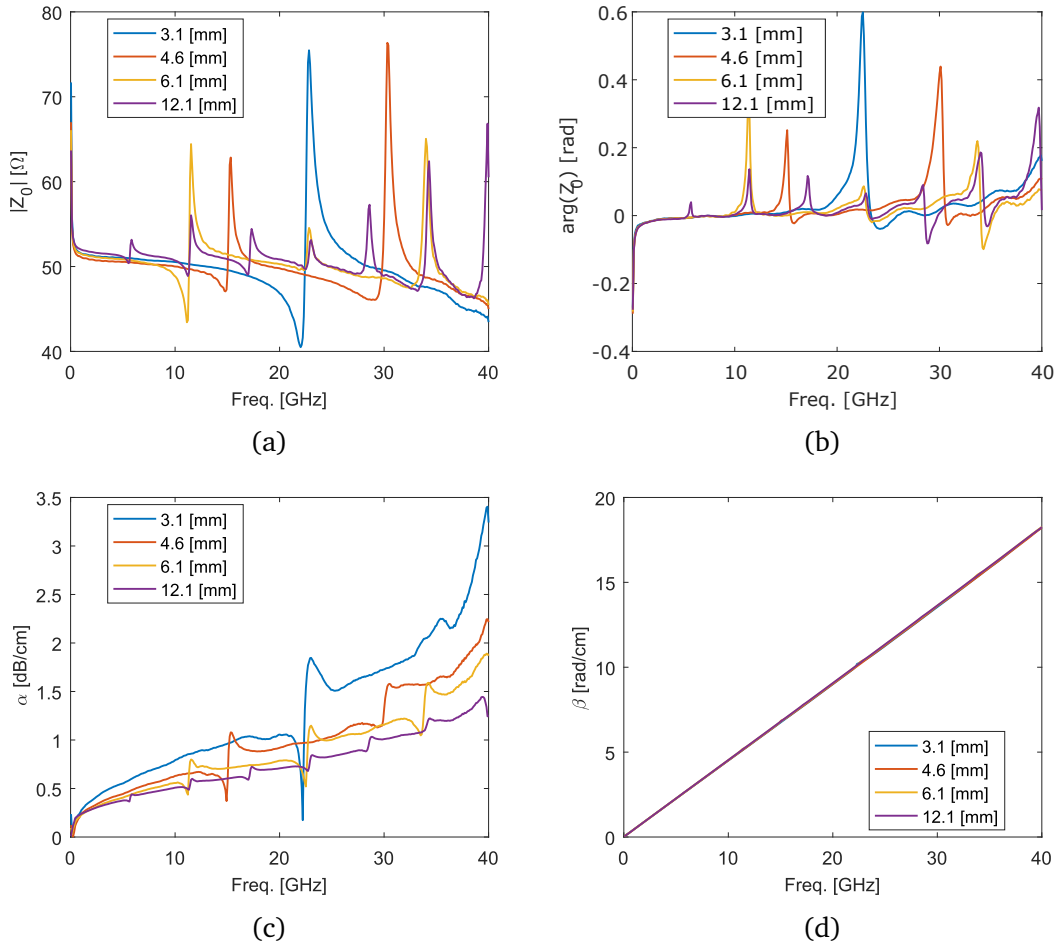


Figure 5.9: The transmission line parameters recovered directly from the VNA measurements. The results do not match the model of a transmission line due to parasitic effects on the measurements that need to be accounted for. Therefore, a second-tier calibration was performed.

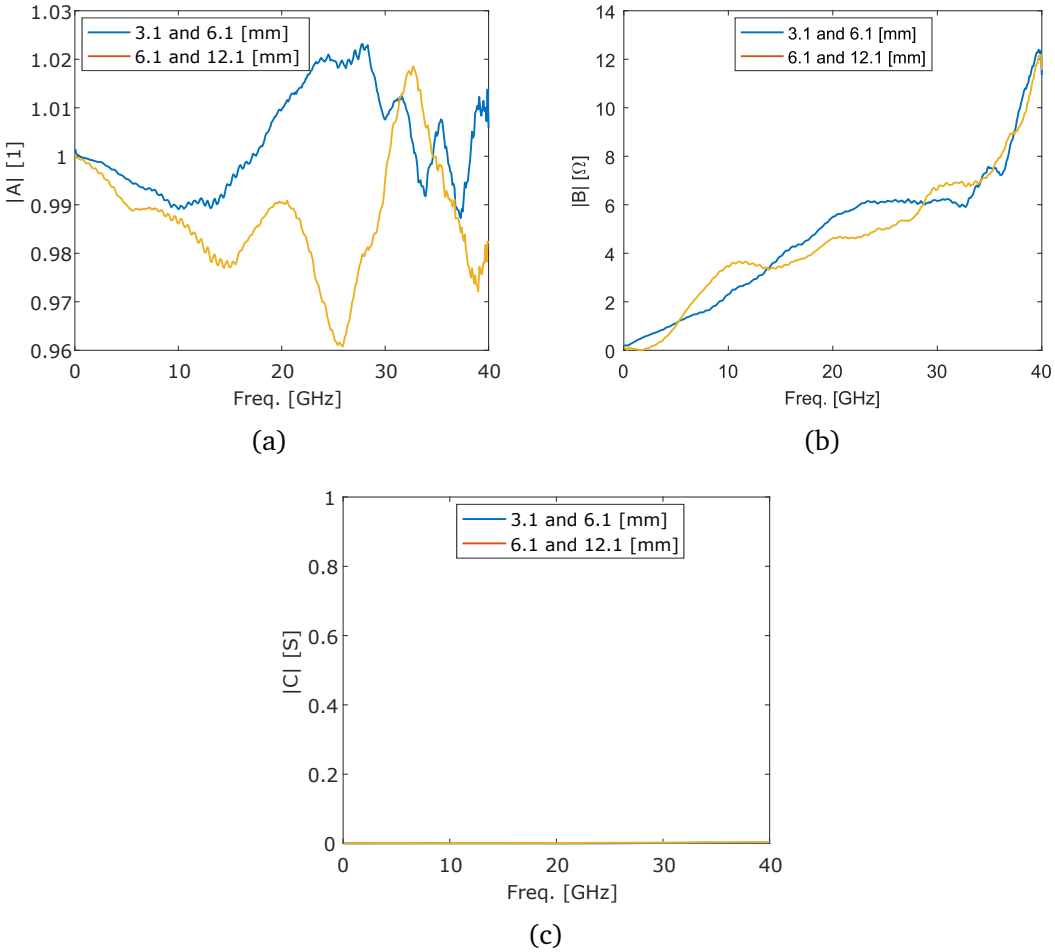


Figure 5.10: The A, B and C parameters of the calculated 100 µm thru for the CB-CPW thru on the LTCC board. Since $A \approx 1$ and $C \approx 0$ the thru can be approximated as a series impedance.

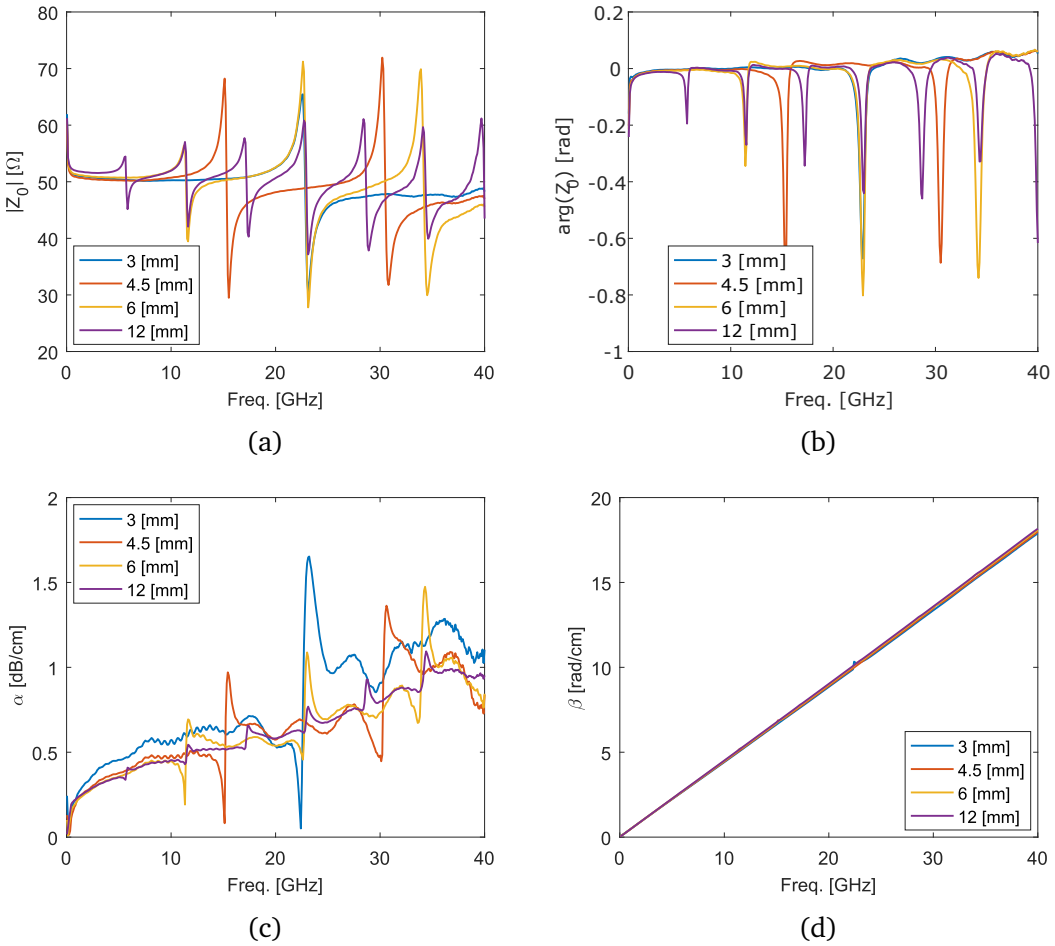


Figure 5.11: The transmission line parameters recovered after second-tier calibration. These results are an improvement over the results from the direct measurements but they still have some issues related to quarter-wavelength resonances.

thru can be approximated as a series impedance (Section 2.4.1). Based on this, the ABCD matrix for the 50 µm pad is calculated using the average of the two ABCD matrices (Figure 5.10) by the procedure discussed in Section 2.4.1. Once the ABCD matrix of the pad ($[A_P]$) is known, the ABCD matrix for the transmission lines can be de-embedded by

$$[A_L] = [A_P]^{-1}[A_{ML}][\bar{A}_P]^{-1} \tag{5.1}$$

where the bar means the swapping of the ports.

In this way, the pad was de-embedded from the measurements and the results show an improvement over the results from the direct measurements but they still have the problems related to the quarter-wavelength resonances (Figure 5.11). The attenuations (α) recovered from the different line lengths are more consistent; however,

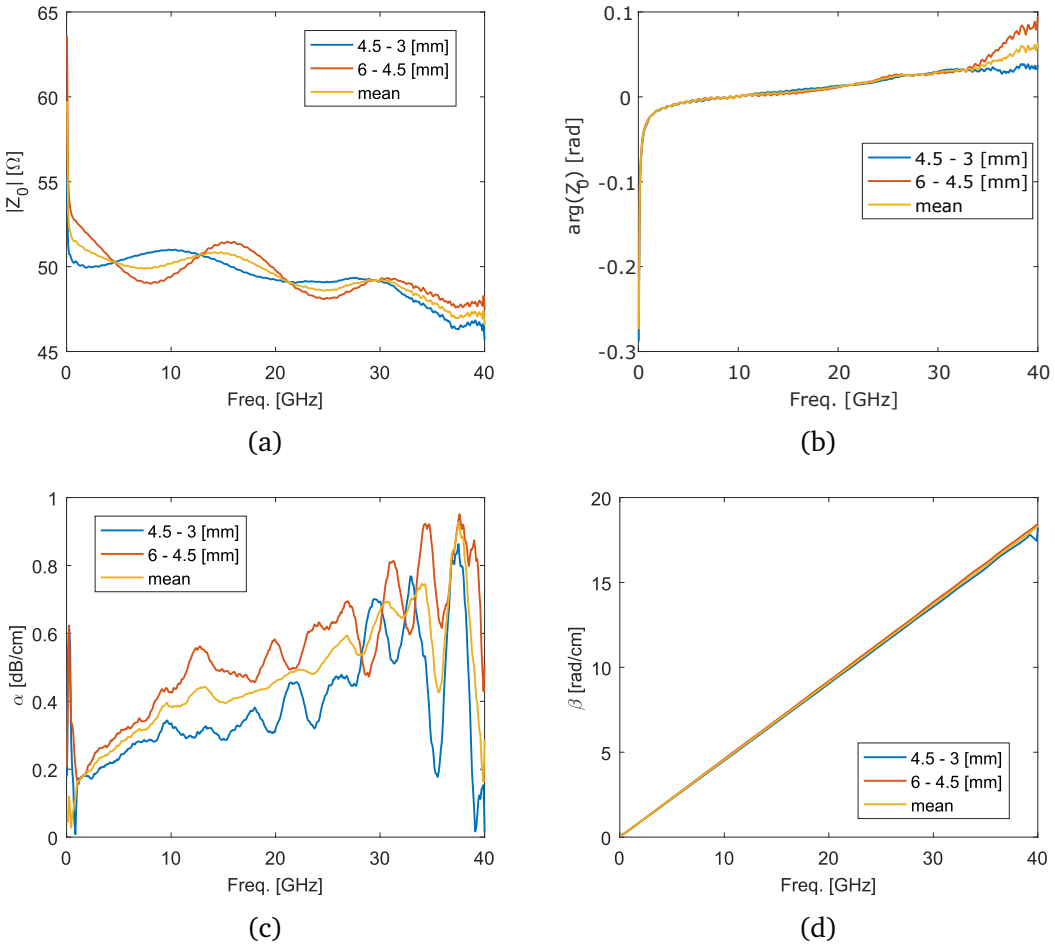


Figure 5.12: The transmission line parameters recovered from the 1.5 mm line. The CB-CPW has Z_0 of 50 Ω and has loss below 1 dB cm^{-1} at 40 GHz.

the parasitic features related to the quarter-wavelength resonances are still present. These parasitic features can be removed by measuring a shorter line but the shortest fabricated lines is 3 mm. However, the performance of shorter lines, with length equal to the difference between measured lines, can be calculated by de-embedding.

In order to get the performance of a line with length 1.5 mm, the 3 mm line is de-embedded from the 4.5 mm line or, similarly, the 4.5 mm line is de-embedded from the 6 mm line. The results show that CB-CPW has a Z_0 around 50 Ω and that the loss is below 1 dB cm^{-1} at 40 GHz (Figure 5.12). The Z_0 (Figures 5.12a and 5.12b) is around 50 Ω real (i.e. Arg $Z_0 \approx 0$) but it decreases to 47 Ω at 40 GHz. The Z_0 has some ripples that can be associated with the remaining parasitic features from the measurements and the de-embedding procedure.

In conclusion, the transmission line parameters were recovered from the measurement of several CB-CPW lines of different lengths. In order to calculate the transmission line parameters, a second-tier thru-only calibration was completed.

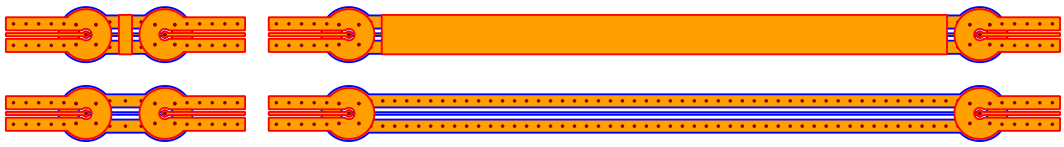


Figure 5.13: The structures used to characterise the SM-CPW on the LTCC board. The structures have two different lengths, 9.1 mm and 30.1 mm, where only the SM-CPW are different and a metal on the top layer is added on some structures to check if the performance is disturbed.

The CB-CPW was found to have a Z_0 around 50 Ω and low loss, accomplishing our objectives.

5.2.2 SM-CPW

Four different structures were created to characterise the SM-CPW (Figure 5.13). The structures have two different total lengths: 9.1 mm and 30.1 mm. The structure length is varied by changing the SM-CPW length. In two of the structures (top row in Figure 5.13), a square of metal above the CB-CPW is added to check if the SM-CPW is correctly shielded to the top layer. A two tier calibration was completed. The first-tier calibration is a standard SOLT calibration using a calibration substrate and the second-tier calibration was the single-impedance thru-only calibration explained in Section 2.4.1 as done in Section 5.2.1. Three copies, one for each fabricated board, were available for each structure. Additionally, the bottom left structure from Figure 5.13 had copies in other places of the layout, so 12 measurements were available for this structure.

As expected, the measurements from the VNA show that the top metal structure does not disturb the performance of the transmission lines. This is expected since the top ground layer of the SM-CPW is there to shield for inter-level cross-talk.

The measurements of the structures in Figure 5.13 include the performance of the two vertical transitions. In order to de-embed the SM-CPW characteristics from the measurements, the short structure in Figure 5.13 is used as a thru element. In order to check if the short structure satisfies the single shunt admittance, or series impedance assumption, The ABCD-matrix is calculated and the results show that $A \not\approx 1$, $B \not\approx 1$ and $C \not\approx 1$ (Figure 5.14). Since $A \not\approx 1$, the series impedance approximation, or shunt admittance approximation, is not valid.

Since the approximations needed for the thru-only series impedance or shunt admittance calibration are not valid, two other calibration procedures were tried. First, a full-wave de-embedding was performed [8]–[12] and, second, a symmetric thru-only calibration (Section 2.4.1) was completed. The full-wave de-embedding was done by simulating half of the short structure in Figure 5.13 and using the results to de-embed the transition from the long structure and, in that way, recover the SM-CPW portion. The half of the thru structure, without the probe pads, is simulated using the full-wave electromagnetic simulator. The full-wave electromagnetic model

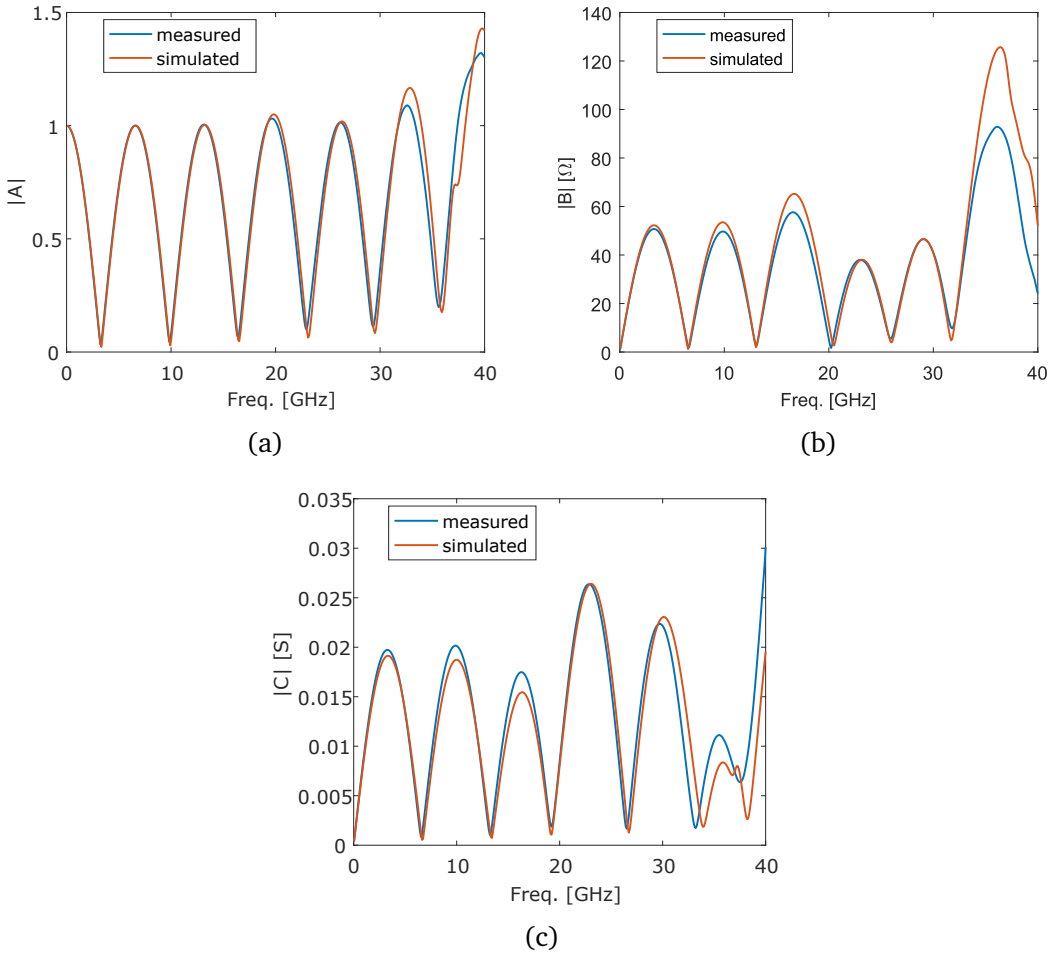


Figure 5.14: The A, B and C parameters, measured and simulated, for the short structure in Figure 5.13 on the LTCC board. $D = C$ since the structure is symetrical. Since $A \not\approx 1$ the series impedance or shunt admittance approximation is not valid.

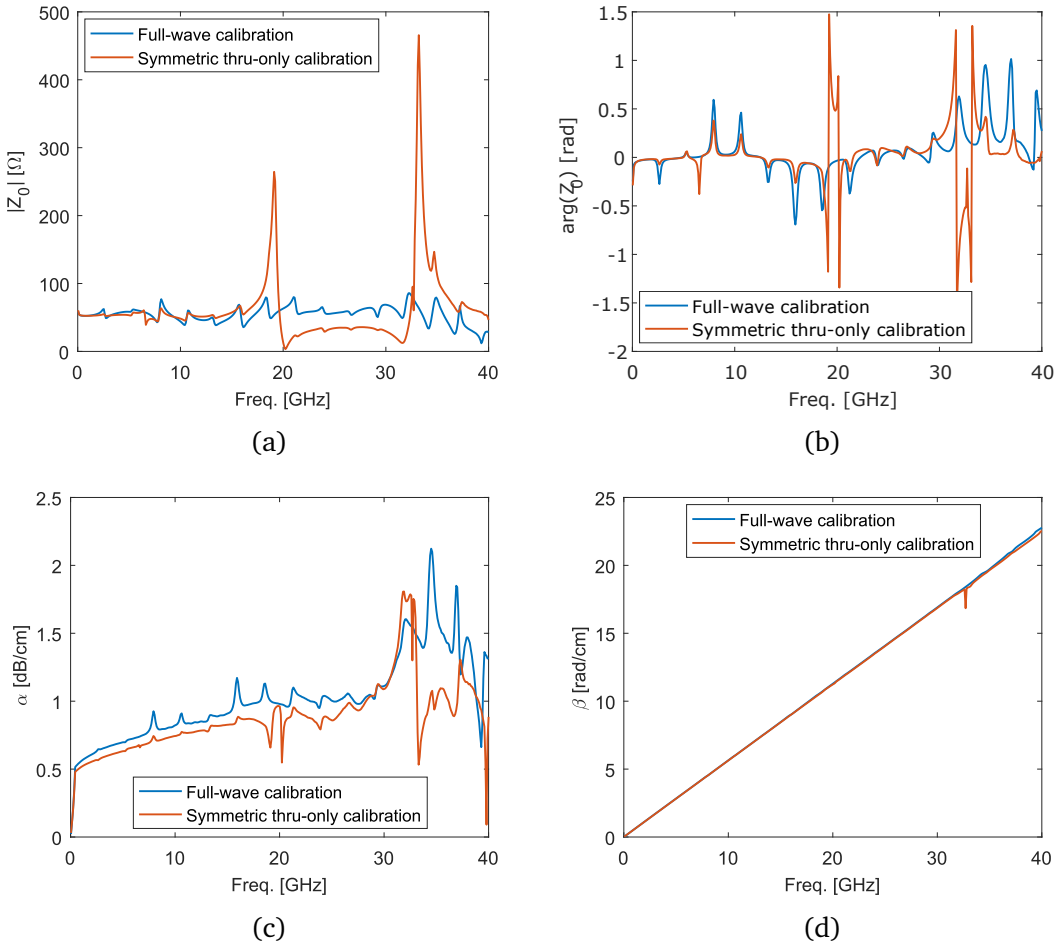


Figure 5.15: The transmission line parameters recovered from the 21 mm SM-CPW line on the LTCC board after two types of the second-tier calibration. The full-wave calibration looks better than the symmetric thru-only calibration.

uses the same set-up as discussed in Chapter 4, but the substrate and metal thicknesses are adjusted based on the measurements presented in Section 5.1.1. The ABCD-matrix is calculated from the simulated scattering parameters (S-parameters) of the half-thru. The calculated ABCD-matrix is then cascaded with its flipped version to get the simulated performance of the thru structure. The results of this simulated thru are compared to the measured thru in Figure 5.14. The matching for the A parameters is good but there are important differences between the simulated C and D parameters and the measurements. The simulated half-thru is then used to de-embed the vertical transitions from the average of the 6 measurements of the long structures in Figure 5.13, leaving only a 21 mm long SM-CPW. The transmission line parameters were recovered from the 21 mm SM-CPW line on the LTCC board using the two types of the second-tier calibration (Figure 5.15). The full-wave calibration looks better than the symmetric thru-only calibration. The symmetric thru-only calibration results present a much lower than expected Z_0 between 20 GHz to 33 GHz and two high Z_0 peaks. In contrast, the full-wave calibration has less extreme limits, however, the results still present a lot of features that seem to be related to the quarter-wavelength resonances of the long line.

Since in this case, no other structures that allow the de-embedding of a shorter line were added to the fabricated layout, the only option available to improve these results was to use the formulation for long lines presented in Section 2.4.3. The transmission line parameters recovered with the proposed equations suitable for long lines have a large variation in the Z_0 compared to the expected results (Figure 5.16). However, the results suggest that the Z_0 is around 50 Ω and that the SM-CPW line has loss below 2 dB cm^{-1} up to 40 GHz. The loss at 40 GHz is around 1.2 dB cm^{-1}.

In conclusion, the transmission line parameters were recovered from the measurement of two SM-CPW lines with different lengths. A long procedure was needed to calculate the SM-CPW transmission line parameters. First, a second-tier thru-only calibration was completed for the pads. Second, a full-wave de-embedding for the transition was used since the symmetric thru-only calibration gave worse results. Finally, a novel equation to obtain the Z_0 from long lines was used. The results present important deviation to the expected results from the simulations but still suggest that the Z_0 is around 50 Ω, and with loss below 2 dB cm^{-1}.

5.2.3 Effect of ground vias

Some structures were fabricated and measured to characterise the effect of the ground vias in the CB-CPW (Figure 5.17). Three separations (signal metal centre to centre) were fabricated: 820 µm, 1320 µm and 1820 µm. The structure with the shortest distance between lines was fabricated, with and without ground vias, to test the effect of these ground vias on the cross-talk and on the transmission.

The scattering parameters (S-parameters) were measured using the VNA for the CB-CPW structures (Figure 5.18). The transmission is similar between the 820 µm separation structure with and without vias. However, the crosstalk measurements show that the ground vias are important to shield against the crosstalk. The crosstalk

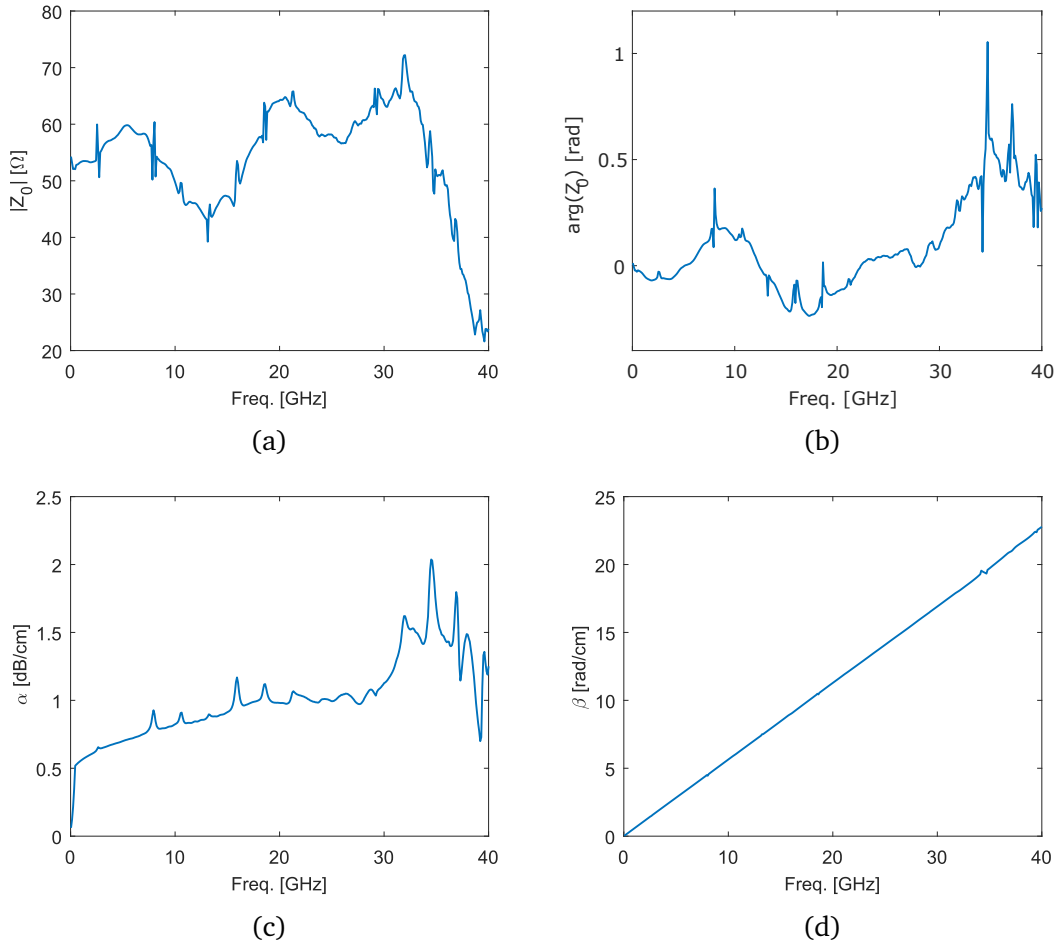


Figure 5.16: The transmission line parameters recovered from the 21 mm SM-CPW line on the LTCC board. The Z_0 is not correctly recovered but seems to be varying around 50 Ω and the loss is below 2 dB cm^{-1} up to 40 GHz.

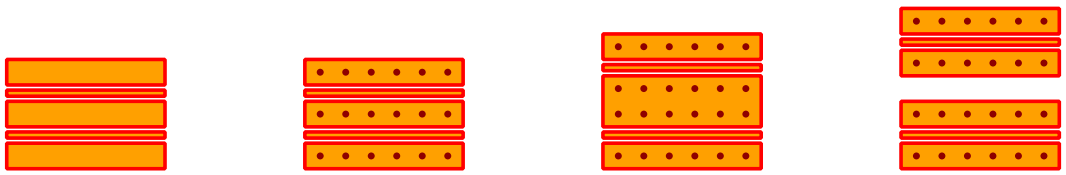


Figure 5.17: The structures used to characterise the effect of the ground vias in the CB-CPW.

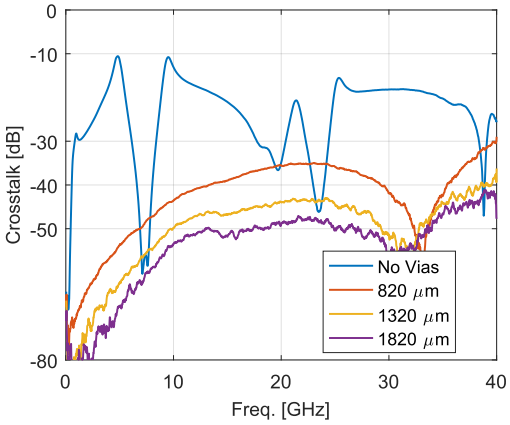


Figure 5.18: Measured results of the effect of the ground vias in the crosstalk. The ground vias have an important effect on reducing the crosstalk.

was measured by placing one probe at the bottom left end of one line and the other in the top right end of the adjacent line, leaving the other ends without termination. Using the vias, the crosstalk maximum is reduced from −10 dB to −30 dB. The crosstalk is reduced further by increasing the distance between the adjacent channels, which means that the ground vias do not completely shield the crosstalk . However, the ground vias reduce the crosstalk to levels that meet our objectives.

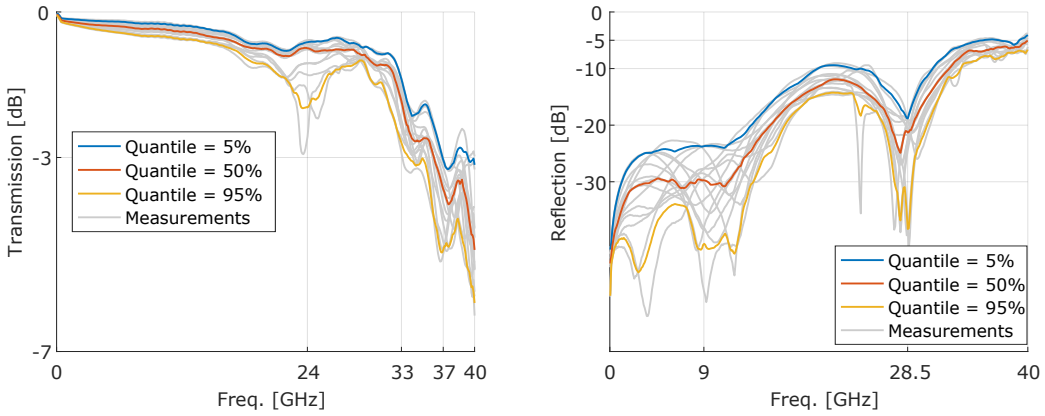
Section 5.2 presented the measurements that characterise the CB-CPW and the SM-CPW. The results show that the CB-CPW have a Z_0 around 50 Ω and a loss around 1 dB cm^{-1} at 40 GHz. In the case of the SM-CPW, the results show that the Z_0 is around 50 Ω and the loss is between 1 dB cm^{-1} and 2 dB cm^{-1} at 40 GHz. However, the SM-CPW results present some deviations from the expected results due to errors in the vertical transition de-embedding procedure and the long lines available. Finally, the measurement of some structures demonstrated the importance of having ground vias for decreasing the crosstalk.

5.3 Vertical transition

The vertical transition was measured using a VNA and a digital communication analyser (DCA). The performance of the design presented in Chapter 4 is presented in Section 5.3.1. Some other variations of the transition were fabricated and the measured results are presented in Section 5.3.2. Finally, Section 5.3.3 presents the fitting between the measurements and the electromagnetic full-wave model.

5.3.1 Measured performance

The transition showed good results with the VNA as can be seen in Figure 5.19. The devices under test are 9 mm lines with two transitions. A first-tier SOLT calibration,

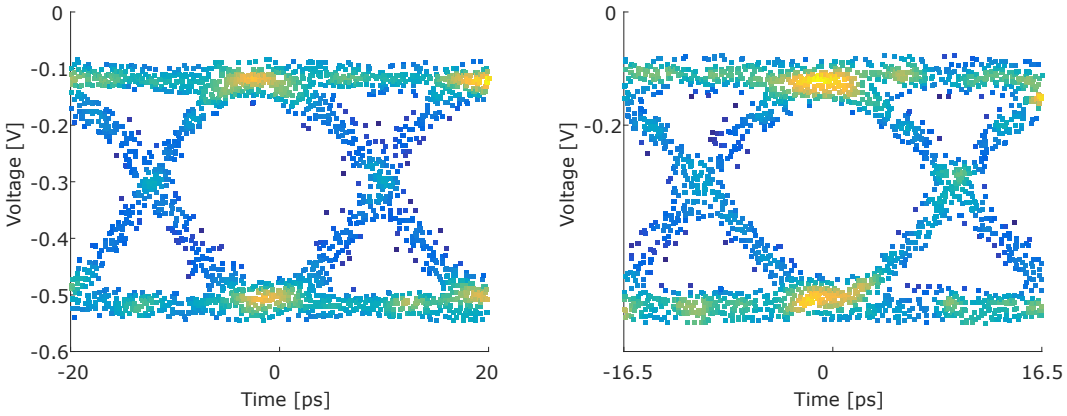


(a) (b)

Figure 5.19: The measured performance (VNA) of the vertical transition fabricated in LTCC. The devices under test are 9 mm lines with two transitions. Fourteen devices were fabricated and measured, plotted in grey. The 5 % and 95 % quantiles for all the measurements at each frequency were calculated. The transmission shows a 3 dB bandwidth between 33 GHz and 37 GHz. There is some manufacturing variability that is seen at 24 GHz for the transmission and at 9 GHz for the reflection.

using calibration substrates, was performed to remove the effect of the cables, probes, and the 50 µm probe pads, as calculated by a second-tier thru-only calibration. Fourteen devices were fabricated and measured, and the reflection and transmission measurements for the fourteen structures are plotted in grey in Figure 5.19. The 5 %, 50 % (i.e. median) and 95 % quantiles for all the measurements at each frequency are also plotted in Figure 5.19. The transmission, shown in Figure 5.19a, shows a 3 dB bandwidth ($f_{3\,\mathrm{dB}}$) between 33 GHz and 37 GHz. The manufacturing variability is below 0.5 dB for frequencies below 20 GHz. Some of the structures showed a degradation of the transmission at 24 GHz, and this degradation is probably caused by misalignments during the fabrication. After 30 GHz, the variability increases with frequency to a maximum of around 3 dB. This is likely due to the effective wavelength of the signal getting small enough to be comparable to the manufacturing process variability, but also due to the nature of the plot in the logarithmic scale. The reflection variability is shown in Figure 5.19b. The variability is larger at frequencies below 9 GHz, and the minimum at 28.5 GHz is due to some variability, both in location and depth.

The same double transition that was measured with the VNA shows good results on the DCA (Figure 5.20). The test setup, consisting of a DCA using a 44 Gbps PRBSG was connected to a double transition using probes. Figure 5.20a shows the measured eye pattern of a thru from the calibration substrate. Figure 5.20b shows the measured eye diagram of the double transition. The insertion insertion of the double transition creates a rather small penalty on the eye diagram.



(a) Calibration thru (b) Double vertical transition

Figure 5.20: The measured performance (DCA) of the vertical transition fabricated in LTCC. The eye diagram is measured with a 44 Gbps pseudorandom binary sequence generator (PRBSG). The double transition is the same at the measured with the VNA. The penalties for insertion of the double transition are small.

In conclusion, the VNA and DCA measurements show that the vertical transition meets the objectives defined for this research and can be used in channels working at data rates of 40 Gbit s^{-1}.

5.3.2 Vertical transition variations

Four variations of the main vertical transition (Figure 5.21) were measured in order to understand the affect of each variation on the performance of the transition. Three variations have different gaps between the signal catch pad metal and the ground catch pad metal in the coaxial-like structure. The gap between the signal catch pad and the ground catch pad in layers C00 and C02 are set to be equal ($G_{gvt} = G_{gvb}$ in Figure 4.3) and the three variations have gaps equal to 200 µm, 300 µm and 400 µm. The last variation uses a different CB-CPW design that has also a Z_0 equal to 50 Ω but in this case, the signal width is 140 µm and the gap width 300 µm.

The measurements from the VNA of the variations of the original vertical transition show that the coaxial-via catch pad gap changes the performance, but the wider CB-CPW does not (Figure 5.22). The gap in the coaxial-like catch pads has a noticeable effect. The results show that the variation of the catch pads gaps has an important effect since it can improve the $f_{3\,\mathrm{dB}}$ by 3 GHz. The variations with the highest $f_{3\,\mathrm{dB}}$ are for the gap equal to 300 µm, and the maximum 3 dB bandwidth is 38 GHz. However, the result with a gap equal to 300 µm shows higher losses at 25 GHz than the original variation. At 10 GHz all the variations show equivalent performance and loss below 0.5 dB. Figure 5.22b shows the reflection loss for the same variations, which is below −10 dB up to 37 GHz for the best variation. The variation with the gaps equal to

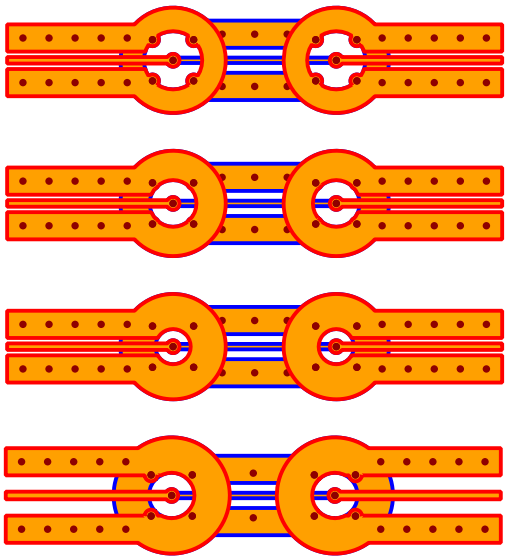
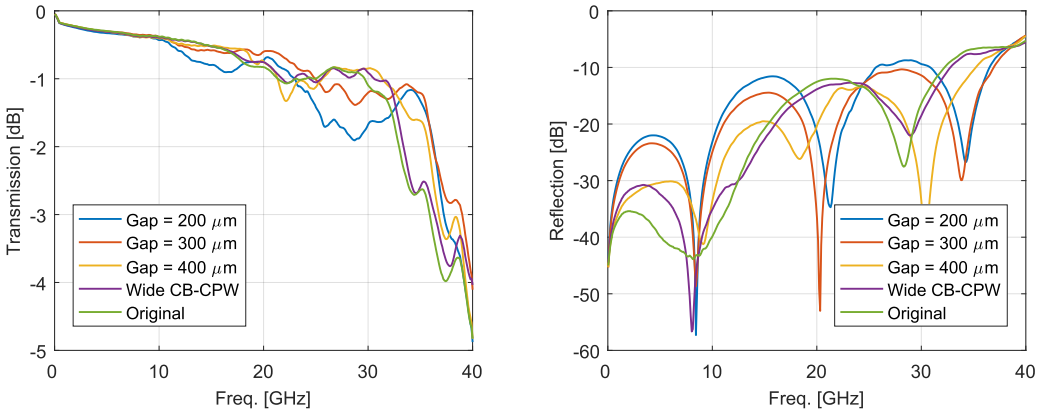


Figure 5.21: Variations of the main vertical transition that have been measured. These are 9 mm long.



(a) (b)

Figure 5.22: The measurements from the VNA of the variations of the original vertical transition. The gap in the coaxial-like catch pads has a noticeable effect.

300 µm has the best performance overall. The use of a second 50 Ω CB-CPW design had a very limited effect and the results are very similar to the original design.

These results show the possibility of further optimisation and thus point to the importance of the optimisation work done for the second version of the transition presented in Chapter 6.

5.3.3 Fitting to the simulation model

Two models of the transition have been constructed: a full-wave simulation and a circuit simulation. The full wave model can be used to simulate the performance of variations of this transition and the circuit model can be used to simulate the performance of the transition in a given system.

The full-wave model is shown in Figure 5.23a. The model is for a 9 mm line with the same dimensions measured in Section 5.3.1. The full-wave model is the same as used in Chapter 4 but with the thickness reduced based on the measurements of Section 5.1.

The circuit model is shown in Figure 5.23b and consists of two distinct elements: a transmission line model of a CB-CPW (Chapter 3) and the model of a CB-CPW to an SM-CPW vertical transition (Chapter 4). All the dimensions are the same as in the fabricated devices shown in the previous section and in the full-wave model. The CB-CPW model is based on the results presented in Chapter 3 with a length of 1.7 mm and the thicknesses measured in Section 5.1. The CB-CPW to SM-CPW vertical transition (similar to Figure 4.17) has a total length of 2.8 mm, the length from the start of the CB-CPW to the signal via centre is 1.3 mm and the length from the signal via centre to the end of the SM-CPW is 1.5 mm. Since a mirrored version is attached afterwards, the total length of the double transition is 9 mm. The scattering parameters (S-parameters) were calculated using the full-wave simulation. The simulated circuit is constructed with these two elements. First, the CB-CPW circuit is connected to the vertical transition model. Then the ports of the vertical transition model are swapped by reordering the scattering parameters (S-parameters) in the matrix. Finally, the last section of CB-CPW is added. An SM-CPW section can be added between the two vertical transition elements if needed, but in this case, the middle part was so short that the middle SM-CPW model was not needed.

The full-wave model and the circuit model agree with the VNA measurements (Figure 5.23). The measurement result shown is the average of the measurements of all the available devices (Section 5.3.1). Figure 5.23c shows excellent agreement on the transmission results. The most significant differences occur around 36 GHz. However, if we take into account the variability of the measurements (Figure 5.19) due to the manufacturing variability, the agreement is very good. Similarly, Figure 5.23d shows good agreement between the simulated and measured reflection for most of the frequency range, except for 7 GHz. However, around 7 GHz the variability between equal structures was higher.

Section 5.3 showed that the measurement results of the vertical transition meet our

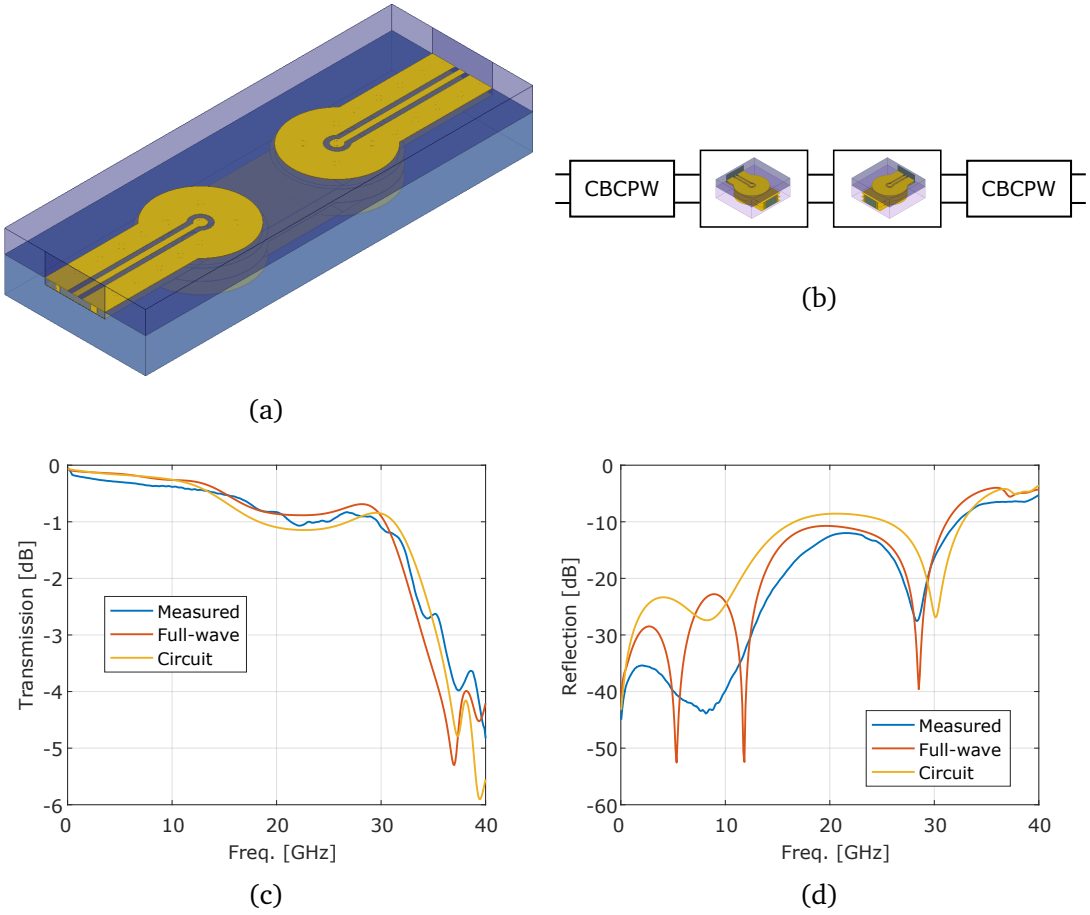


Figure 5.23: The comparison between the models used in the electromagnetic solvers and the measurements. (a) shows the 3D structure that is modelled using the full-wave electromagnetic simulator. (b) shows the model used in the circuit simulation. (c) shows the transmission agrees between the full-wave simulation, the circuit simulation and the VNA measurements. (d) shows the reflection agrees between the full-wave simulation, the circuit simulation and the VNA measurements.

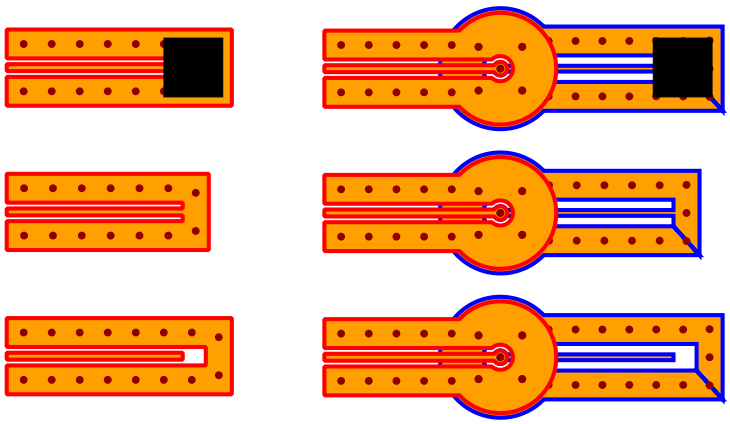


Figure 5.24: The terminations of the LTCC board for measurement.

objectives and can be used in channels working at 40 Gbit s^{-1}. Additionally, the measurement of some variations of the transition shows the possibility of improving the performance by optimizing the parameters of the design. Finally, the measurements were compared with our electromagnetic models resulting in good agreement.

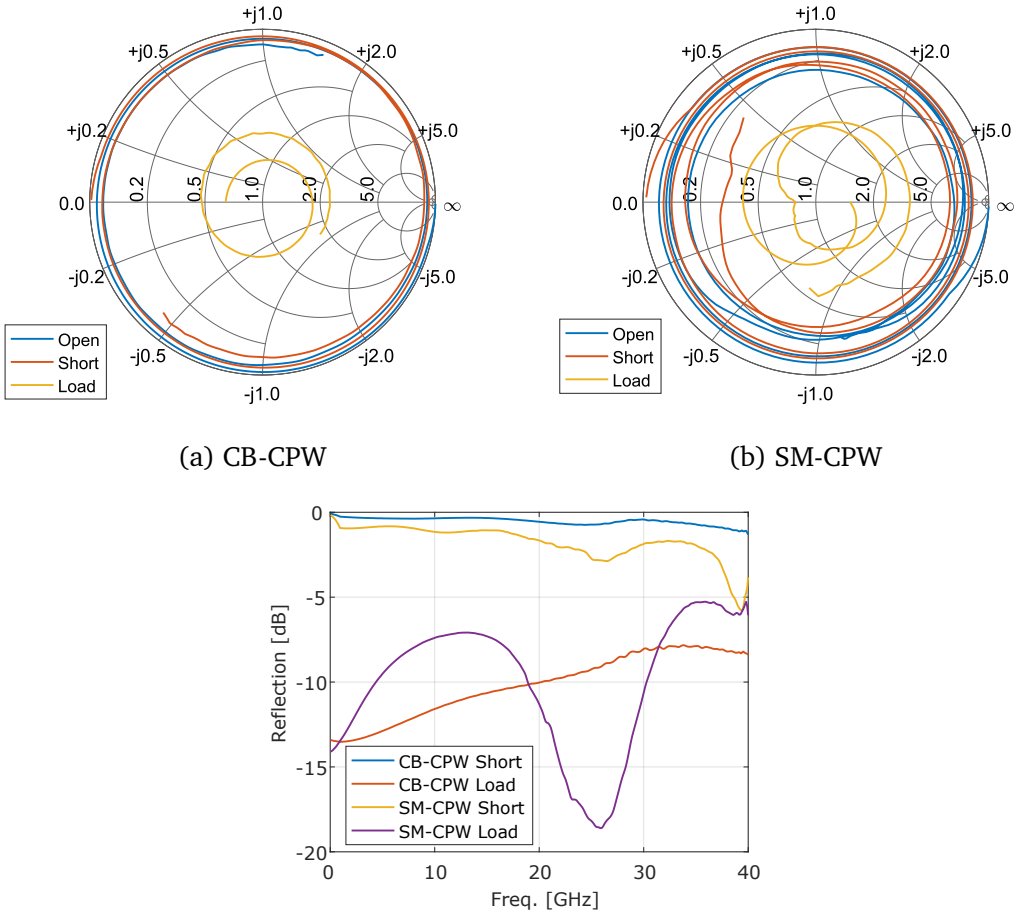
5.4 Other structures

Some other elements that are useful in carrier boards for photonic integrated circuits (PICs) were fabricated. Section 5.4.1 presents the measured results of several terminations and Section 5.4.2 presents the measured results of a four channels phase-matched arrays.

5.4.1 Terminations

Six terminations were fabricated in the LTCC board for measurement (Figure 5.24). Three types: open, short and a load, were fabricated for both the CB-CPW and the SM-CPW. All the terminations contain ground vias at the end intended to avoid unwanted radiation. The gap between the end of the signal metal and the ground pad is 400 µm. The 400 µm gap is also used below the thick film resistor (colour black in Figure 5.24). This gap was designed by using an electrostatic simulator (*COMSOL*) to get a 50 Ω resistance at direct current.

The VNA measurements of the terminations of the LTCC board show expected results for the open, short, and load (Figure 5.25). The load termination reduces the reflection significantly, as shown by the reflection being closer to the Smith chart centre or as shown by the reduction in the reflection. Both loads, in the CB-CPW and in the SM-CPW, decrease the reflection by around 14 dB at 1 GHz. At 40 GHz, the CB-CPW load adds 9 dB attenuation but the SM-CPW load measurement does not show any additional attenuation compared to the short termination. This lack of additional attenuation does not represent the performance of the load but rather the

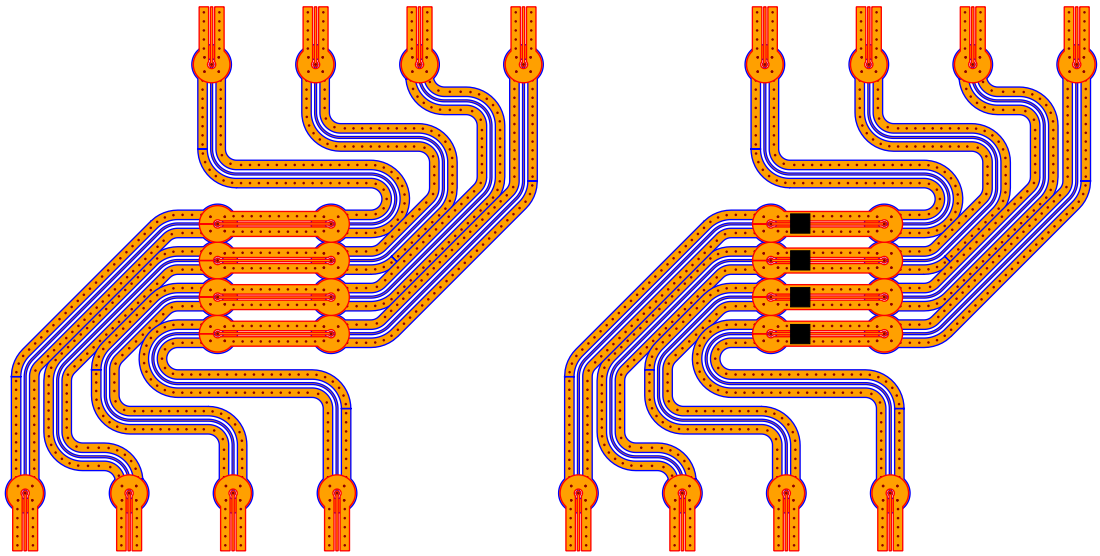


(a) CB-CPW

(b) SM-CPW

(c)

Figure 5.25: The measurements from the VNA of the terminations on the LTCC board.



(a) (b)

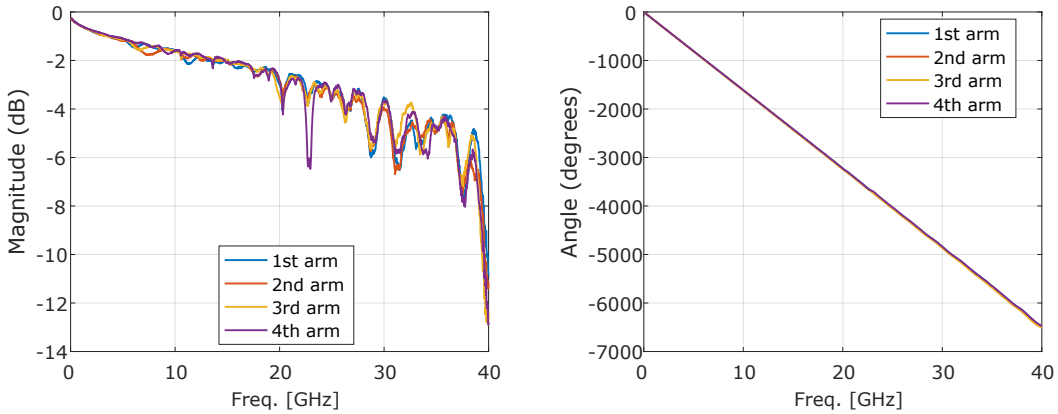
Figure 5.26: The four phase-matched channels that were fabricated: (a) without any load; (b) with a thick film resistor as a load.

large losses in the short termination. These losses in the short termination represent the microwave power that is attenuated by the metals and the power loss due to radiation.

These terminations are useful for travelling waveguide devices where the high-speed device in the PIC must be terminated with a load to avoid unwanted reflections back to the device.

5.4.2 Phase-matched array

A four channel phase-matched array was fabricated (Figure 5.24). This type of phase-matched array is useful for PICs used in phase modulation subsystems, using formats such as polarization multiplexed quadrature phase-shift keying (PM-QPSK). The design is based on a four channel array designed for high-speed PM-QPSK modulation based on travelling-wave Mach-Zehnder modulators [13]. The layout is for equally spaced channels. In that work, some mathematical relations to achieve phase matching between the lines was derived by making the path length difference zero. These mathematical relations were used to generate our array. The final design uses several bends to equalize the length of the channels and thus the length from top to bottom is 2.9 cm. The channels start and end in CB-CPW sections but after a vertical transition, the channel is routed in the buried SM-CPW emulating our target interposer (Figure 1.9b). After the routing in the SM-CPW, another transition is used to bring the channel to the top layer where our PIC would sit. To emulate a PIC, a thick-film resistor is deposited on a second version of the array. The structure is then mirrored to facilitate the testing.



(a) (b)

Figure 5.27: (a) The transmission and (b) phase (i.e. $\angle S_{21}$) of all channels measured with the VNA. The channels are correctly phase matched.

The transmission and phase ($\angle S_{21}$) of all channels were measured with the VNA (Figure 5.27). The channels are long and contain four vertical transitions. Therefore, the $f_{3\,\mathrm{dB}}$ is only around 20 GHz (Figure 5.27a). The phase shows that the channels have the same electrical length (Figure 5.27b), as desired.

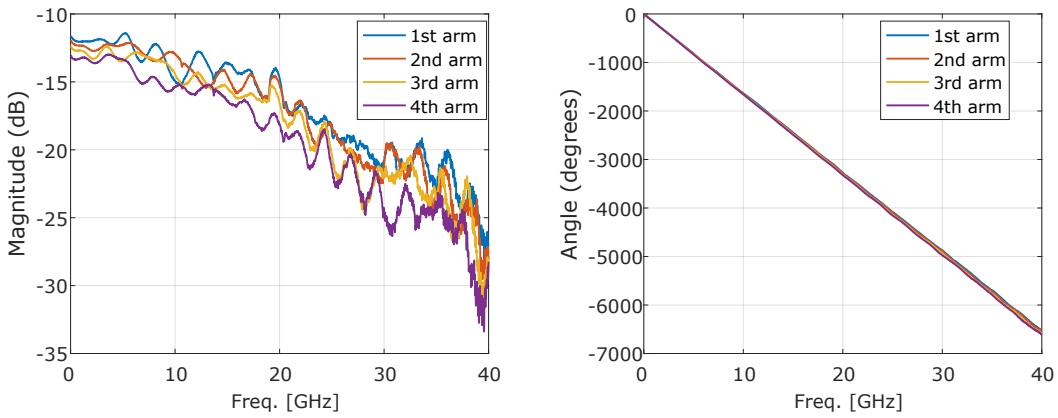
Similarly, the transmission and phase (i.e. $\angle S_{21}$) of all channels were measured with the VNA, but this time the channels included a resistive load realised by a thick film resistor (Figure 5.26b). The power is absorbed in the loads as can be noticed by the substantial reduction of the measured transmission (Figure 5.28a). The load does not disturb the phase matching (Figure 5.28b).

In order to understand the performance of the channels in the time domain, the eye diagram transmitted through one of the channels in the phase-matched array was measured using the DCA at 22 Gbit s^{-1} and 44 Gbit s^{-1} (Figure 5.29). In this way, we can evaluate the effect of the multiple features found in Figure 5.27a in the time-domain. The measured eye diagram is still open after the long channel and the four vertical transitions even at 44 Gbit s^{-1}. The comparison between the measurement of the short 500 µm thru load in the calibration substrate shows that the insertion penalties meet our objectives even for these long channels.

In conclusion, these structures have shown that the transmission lines and the vertical transition can be used to realise channels for the interposer that can achieve phase-matching, and work at 44 Gbit s^{-1}.

Section 5.4 presented the measurement results of some terminations and of a phase-matched channel array. These structures are often needed in applications that use PICs. The load terminations gave good attenuation and the phase-matched channels performed well for our objectives with good phase-matching and acceptable penalties at 45 Gbit s^{-1}.

Chapter 5 presented the measurements done to characterise the fabricated trans-

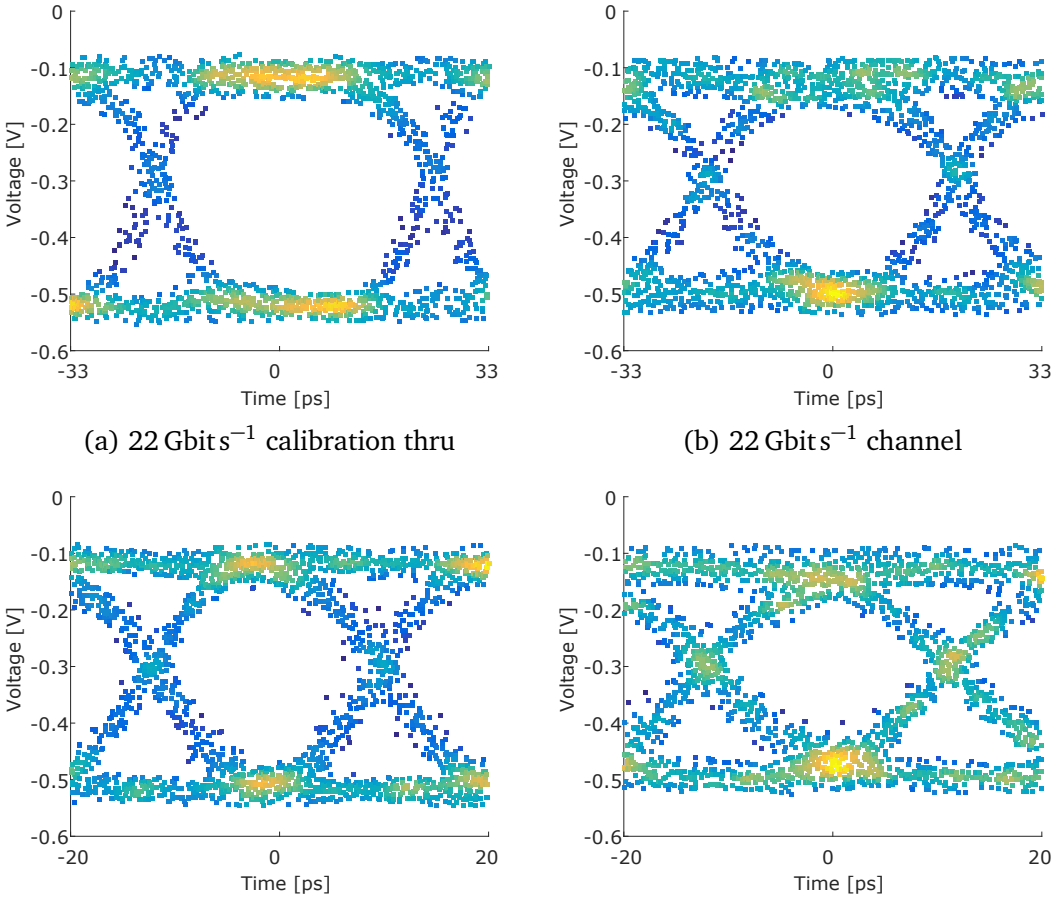


(a) (b)

Figure 5.28: (a) The transmission and (b) phase (i.e. $\angle S_{21}$) of all channels, including loads, measured with the VNA. The power is delivered to the loads and the phase matching is maintained.

mission lines and vertical transition designed in Chapters 3 and 4. The dimensional characterisation (Section 5.1) showed some recurrent defects, found by visual inspection, that might account for variations in the electrical measurements. The measurement of the overall board thickness suggests that the substrate thickness was 115 µm rather than 127 µm. The substrate and the metal roughness are found to be high, and the metal thickness was found to be around 3 µm which is a significant deviation from the 8 µm used in the design process. These findings must be accounted for when comparing the simulated to the measured results. This chapter also showed that the CB-CPW has a Z_0 close to 50 Ω and a loss around 1 dB cm^{-1} at 40 GHz (Section 5.2). In the case of the SM-CPW, the fabricated structures only allowed a full-wave de-embedding, and the measurement for a 21 mm line, thus including several quarter-wavelength resonances. Therefore, the results are noisy but still the Z_0 is around 50 Ω and the loss is between 1 dB cm^{-1} and 2 dB cm^{-1} at 40 GHz. Finally, the measurements of some structures that demonstrate the importance of having ground vias for decreasing the crosstalk were completed.

Additionally, this chapter showed that the measurement results of the vertical transitions meet our objectives and can be used in channels working at 44 Gbit s^{-1} (Section 5.3). The measurements of some variations of the transition design show the possibility of improving the performance by optimizing the parameters of the design, and the measurements were compared with our electromagnetic models resulting in good agreement. Finally, this chapter presented the measurement results of some terminations and of a phase-matched channel array (Section 5.4). These terminations and phase-matched arrays are often needed in applications that use PICs. The load termination presented good attenuation and the phase-matched channels performed well for our objectives with good phase-matching and acceptable penalties at 44 Gbit s^{-1}.



(a) 22 Gbit s^{-1} calibration thru

(b) 22 Gbit s^{-1} channel

(c) 44 Gbit s^{-1} calibration thru

(d) 44 Gbit s^{-1} channel

Figure 5.29: The eye diagram transmitted through one of the channels in the phase-matched array. The eye diagram is still open after the long channel and four vertical transitions.

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Chapter 6
The characterisation of an interposer in co-fired Aluminium Nitride

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In a similar manner to Chapter 5, this chapter presents the characterisation of the transmission lines (Chapter 3), the second vertical transition (Chapter 4) and other structures, but this time fabricated in co-fired aluminium nitride (AlN). Section 6.1 presents an analysis of the dimensional variations of the fabricated board. The analysis of the dimensional variations show deviations from the models used to design the structures. Then, Section 6.2 presents the measurements done to characterise the transmission lines, the conductor backed co-planar waveguide (CB-CPW) and the shielded multi-layer co-planar waveguide (SM-CPW). Next, Section 6.3 presents the

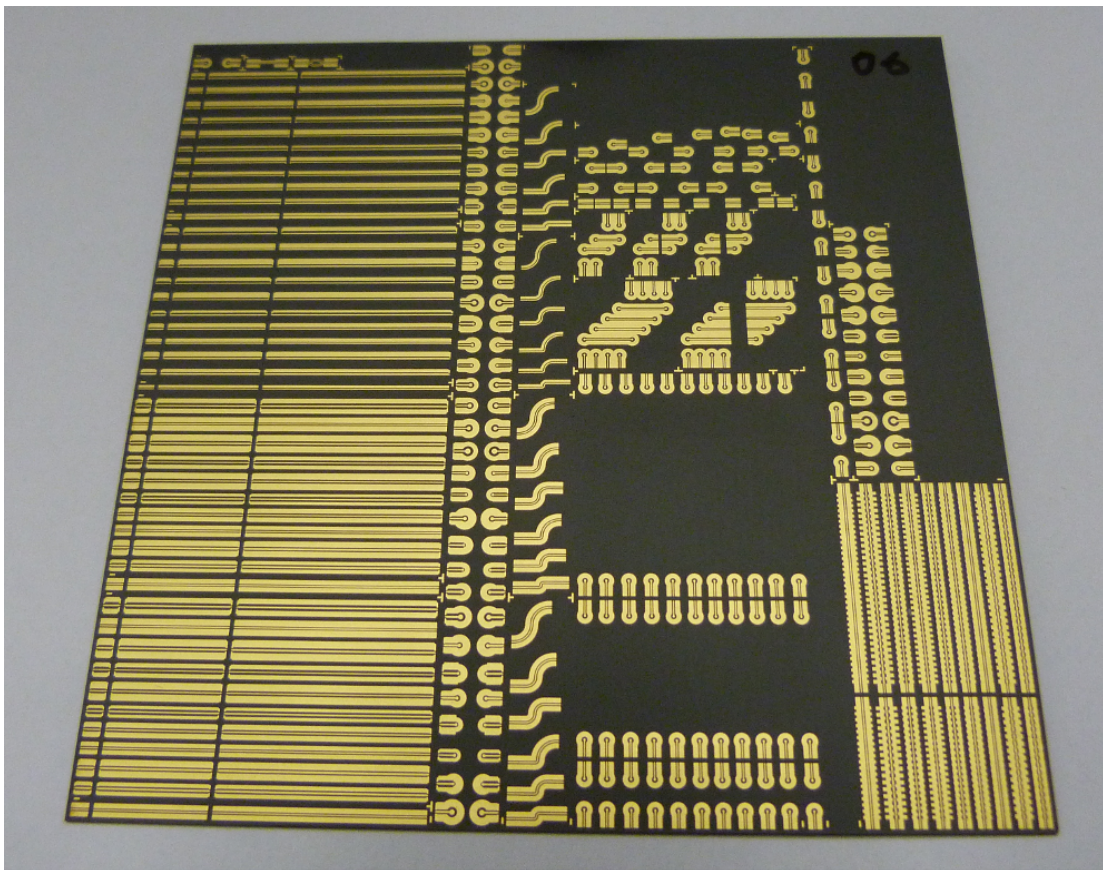
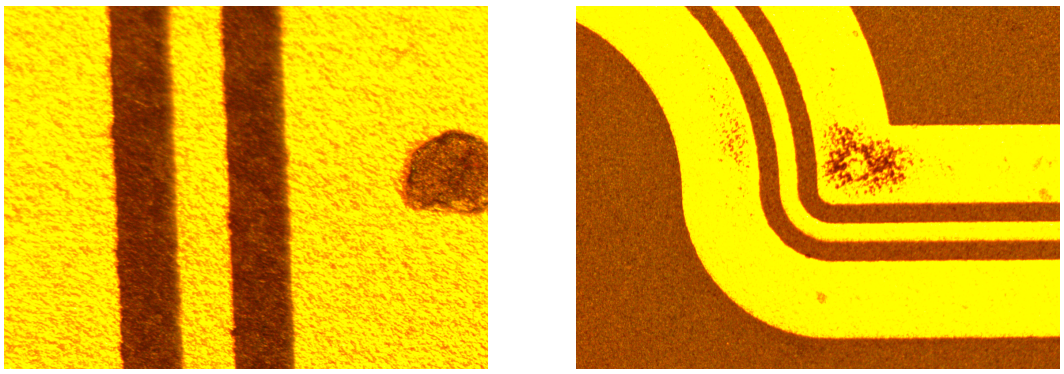


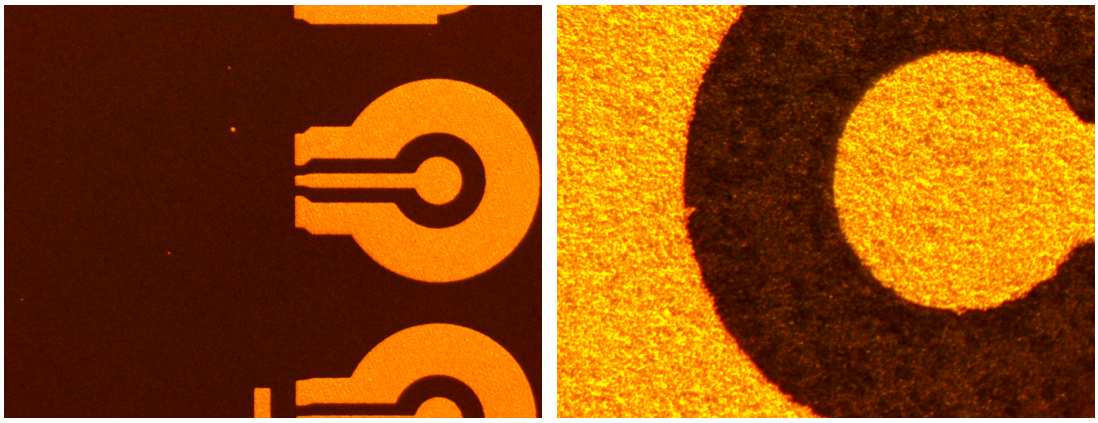
Figure 6.1: A picture of the board fabricated in co-fired AlN.

measurements that characterise the performance of the second designed vertical transition (Section 4.3). Finally, Section 6.4 presents the measurements of other structures fabricated to explore some complementary research ideas.

Ten copies of the co-fired boards were fabricated by Kyocera using AlN as the substrate (Figure 6.1). The shape of the fabricated boards is a square with length equal to 10 cm. The gold metallization has a target thickness of 3 µm for all metal layers. The substrate thickness could only be a multiple of 127 µm. The thickness of the top dielectric substrate (W_{00} in Figure 4.3) is 127 µm, and the thickness of the two following layers (W_{01}) are 254 µm each. The thicker ceramics are needed to acheive a characteristic impedance (Z_0) of 50 Ω in the SM-CPW and to be compliant with the design rules. All the vias were made with stencils so the final diameter of the holes is 100 µm. Circular catch pads covering the metal vias were needed to ensure contact between the planar metal layers and the via fill, and the catch pad diameter needed to be 150 µm bigger than the via diameter. The minimum feature size (metal line or gap between metals) is 100 µm. The minimal spacing between adjacent vias is 300 µm from centre to centre. The ten boards have the same layout. The fabricated layout for the top circuits and the buried circuits are shown in Figure 1.16. The ground structures are not interconnected and so a ground mesh is not used.



(a) Black residues



(b) Metal splashes (c) No defects

Figure 6.2: Very few visual defects were found in the co-fired AlN board.

6.1 Dimensional characterisation

A characterisation of the dimensions of the fabricated board was completed. First, Section 6.1.1 discusses the findings of a visual inspection of the board. Then, Section 6.1.2 presents some measurements done to characterise the metal thickness and the metal roughness. After that, Section 6.1.3 present measurements to characterise the rectangular features.

6.1.1 Visual inspection

Very few visual defects were found in the co-fired AlN board (Figure 6.2). Two black residues were found (Figure 6.2a), the black residue was only found in the two cases shown. The source of this residue is unknown. Very small metal splashes (Figure 6.2b) were found. These metal splashes were found only on a couple of places and none of these metal splashes short the metals. Most of the structures in the co-fired AlN board don't have defects (Figure 6.2c) and the definition of the metals is very good.

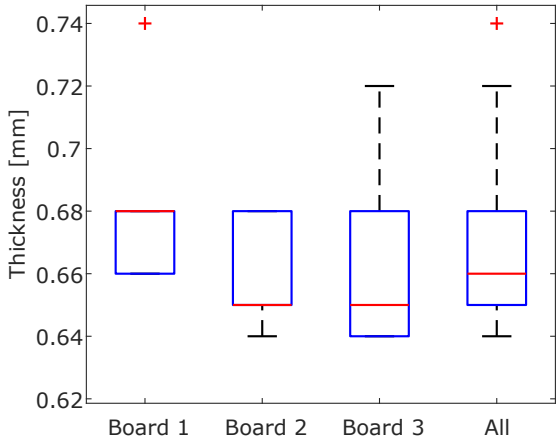


Figure 6.3: The co-fired AlN overall thickness.

The board thickness was measured using Vernier calipers (Figure 6.3). Three boards were measured in six different locations; the same locations were used on each board. The Vernier resolution was 0.01 mm and the three boards have similar thickness distributions. The thickness used for the design of the circuit is 635 µm assuming that the metal gets embedded in the substrate; that is, the metals do not contribute to the overall thickness. In comparison, the mean of all the measurements is 668 µm. This indicates that the layers are multiples of 133 µm rather than 127 µm.

6.1.2 Metal characterisation

The metal thickness was measured using a contact profilometer with a 5 µm stylus (Figure 6.4). Three profiles were measured: over the substrate, over the metal, and in a metal step. The substrate presents variations of around 2 µm. Furthermore, the metal presents similar variations probably caused by the substrate roughness while depositing the metal. In order to measure the metal thickness, the profile of a gold step was measured. The measurement of the step shows that the metal increases linearly to a maximum thickness in a length of around 100 µm, and that the maximum metal thickness is around 11 µm. This is thicker than the metal thickness used in the simulations (3 µm).

6.1.3 Characterisation of rectangular features

The gap width, the signal width, and the corners of the rectangular features of the CB-CPW were measured (Figure 6.5). The gap and the signal width were measured in order to verify the fabricated dimensions and to characterise the fabrication variation. The corners of the rectangular features were measured by fitting a circle and recording the diameter of that circle. The smaller the diameter means the sharper the corner. A total of 40 gap widths were measured, and the mean value of these measurements

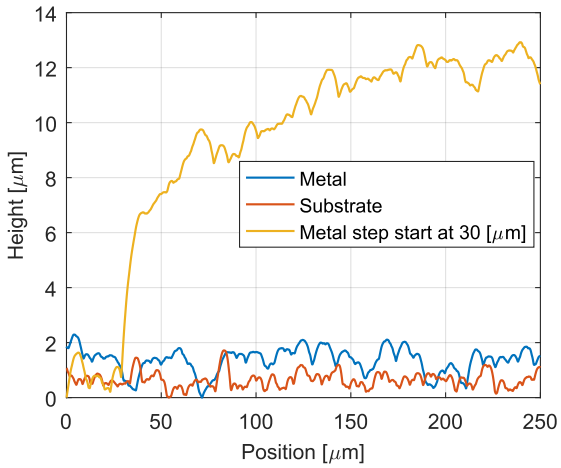


Figure 6.4: The surface profiles of the co-fired AlN board. The substrate is rough and that translates into rough metal. The metal step is around 10 µm.

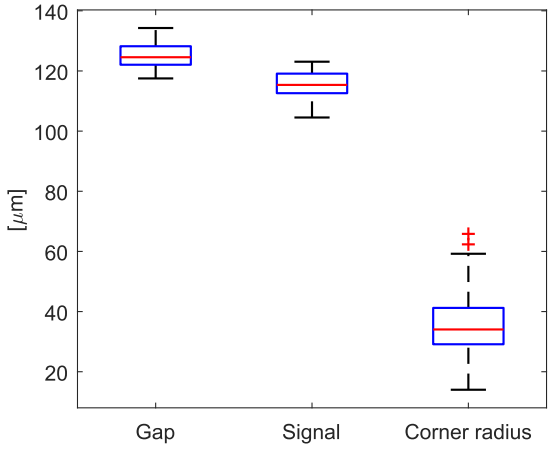


Figure 6.5: Measurements to characterise the rectangular structures in the co-fired AlN board. The gap label refers to the gap width of the CB-CPW and the signal label refers to the signal width of the CB-CPW. The measured dimensions agree with the designed layout.

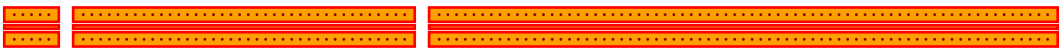


Figure 6.6: The structures used to characterise the CB-CPW in the co-fired AlN board. The three lengths that were measured were 1.9 mm, 11.9 mm and 21.9 mm.

was 125 µm. The layout specified a gap of 120 µm and thus the gap was 5 µm larger than expected. The interquartile range for the gap measurements is 6.15 µm. A total of 20 signal widths were measured, and the mean value of these measurements was 115.6 µm. The interquartile range for the signal line width measurements was 6.5 µm. The layout specified a signal with of 120 µm, therefore, the signal width was 4.4 µm shorter than expected. A total of 80 corners were measured, and the mean value of the fitted circle diameter was 35.85 µm with an interquartile range of 34.82 µm. A corner that visually looks very square has a diameter of 35 µm. The corners look very sharp to the eye. These results mean that the board dimensionally agrees with our designs and has well-shaped geometries.

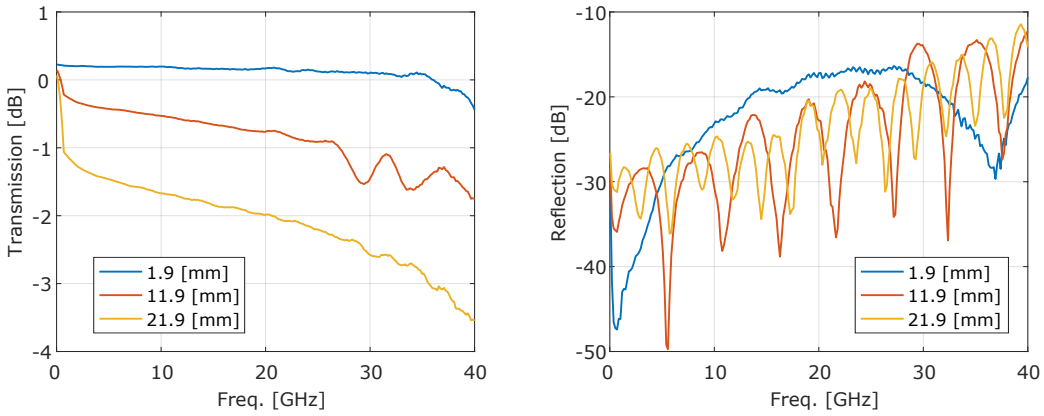
Section 6.1 presented the results of a visual inspection of the co-fired AlN board. The board presents just a few defects. Measurements by Vernier callipers shows that the substrate thickness is 133 µm rather than 127 µm. The substrate and the metal surfaces roughness was characterised and the metal thickness is found to be around 10 µm, a significant deviation to the 3 µm used in the design process. The measurement of several rectangular and circular geometries found that the gaps and the metal widths are the same as in the design and the sharpness of the geometries is good. All these finding must be accounted for when comparing the simulated to the measured results.

6.2 Transmission lines

The transmission lines were measured using the vector network analyser (VNA). First, Section 6.2.1 presents the measurements done to characterise the CB-CPW. Then, Section 6.2.2 does the same for the SM-CPW. Finally, Section 6.2.3 presents the measurements of some structures fabricated to explore the effect of the ground vias on the performance of the transmission lines.

6.2.1 CB-CPW

Three different lengths of CB-CPW lines were fabricated in the co-fired AlN boards. The lengths measured were 1.9 mm, 11.9 mm and 21.9 mm (Figure 6.6) . A first-tier short-open-load-thru (SOLT) calibration was performed using a commercial calibration substrate with the VNA. Ten copies, one for each fabricated board, were available for each length.



(a) (b)

Figure 6.7: Measured scattering parameters (S-parameters) for the CB-CPW structures in the co-fired AlN board. The measurements have some clear deviations from a perfect transmission line model.

The scattering parameters (S-parameters) measured directly from with the VNA (Figure 6.7) show some deviations from the simple transmission line model (Figure 2.15). The plots shown in Figure 6.7 are the average of two measurements. The repeatability was very good and thus only two were taken. The transmission (Figure 6.7a) for the 11.9 mm line shows some ripples. The reflection (Figure 6.7b) increases with the frequency and the quarter wave-length minimums are clearly defined.

Assuming that the measurements from the VNA represent only the transmission line, the transmission line parameters were calculated for each of the lines (Figure 6.8). The transmission line parameters were calculated with success by using the novel equations for long lines explained in Section 2.4.3, since even the shorter line includes a quarter-wavelength resonance. The attenuation (α) graph in Figure 6.8c shows that the attenuation for the different lines is not consistent. The phase propagation constant (β) in Figure 6.8d is similar for the three lengths. In order to remove parasitic features, a second-tier calibration was performed.

The second-tier calibration is a thru-only calibration. The thru used is the shortest element in the fabricated board with length equal to 1.9 mm. A short element of the same lengths can also be de-embedded from the two long lines by Equation 2.35 as discussed in the Section 5.2.1 by using the 11.9 mm and 21.9 mm lines. The A, B and the C parameters from the calculated ABCD matrix for the thru are shown in Figure 6.9. Since $A \not\approx 1$ and $C \not\approx 0$, the thru can not be approximated as a series impedance (Section 2.4.1)

Since the single impedance thru-only de-embedding is not possible, a symmetric Thru-line calibration was completed. The 1.9 mm line is used to calculate a symmetric pad and then the pad is de-embedded from the 11.9 mm and 21.9 mm lines. Also, the 11.9 mm line is used to calculate the symmetric pad and then de-embedded from

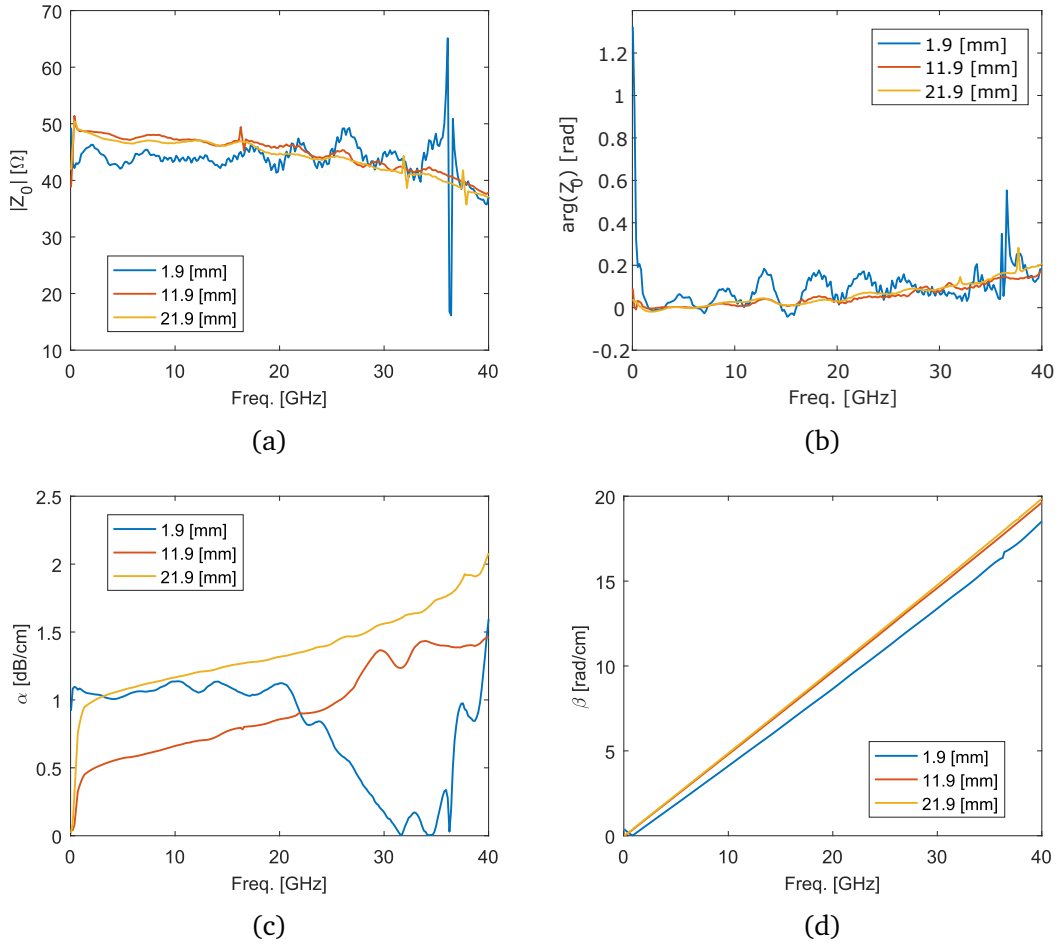


Figure 6.8: The transmission line parameters recovered directly from the VNA measurements for the co-fired AlN board. The results do not match the model of a transmission line due to parasitic effects on the measurements that need to be accounted for. Therefore, a second-tier calibration was performed.

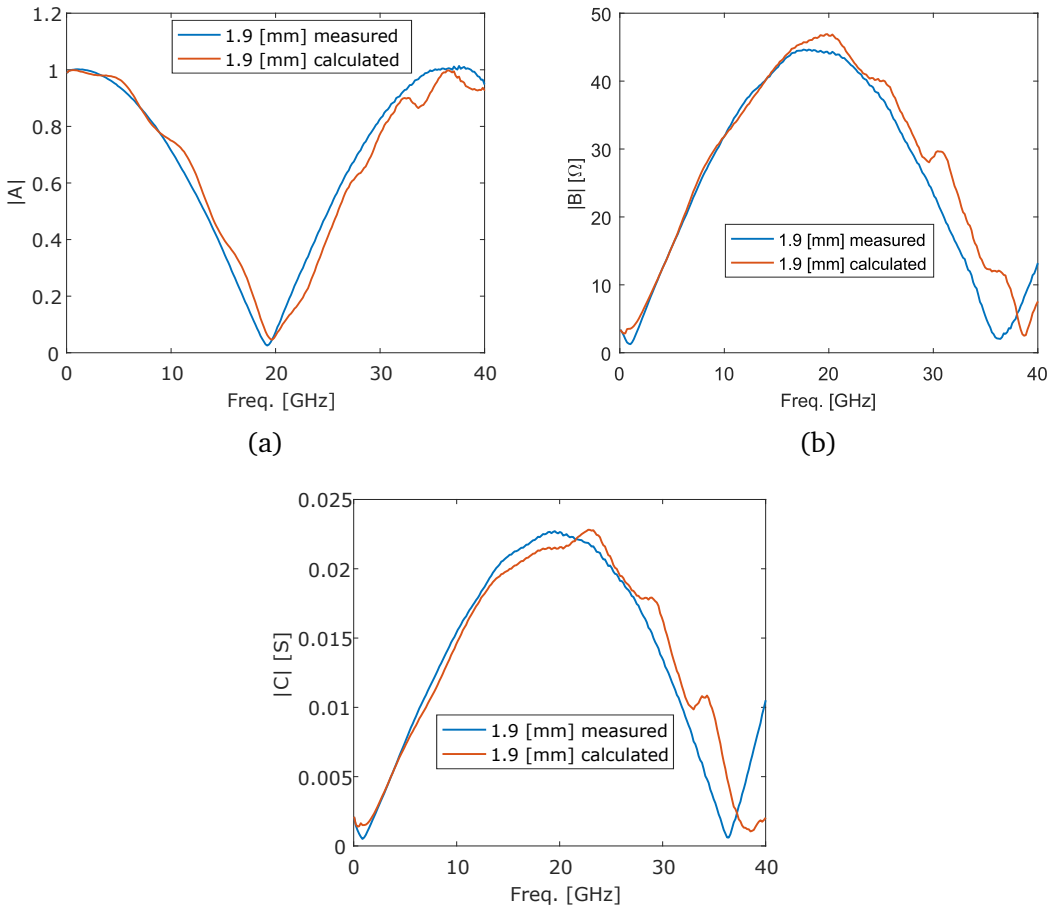


Figure 6.9: The A, B and C from the ABCD matrix for the CB-CPW thru in the co-fired AlN board. $C = D$ since the element is symetric. The measured results are for the fabricated 1.9 mm line and the calculated line is de-embedded from the measurements of the two long lines. Since $A \not\approx 1$ and $C \not\approx 0$ the thru cannot be approximated by a series impedance.

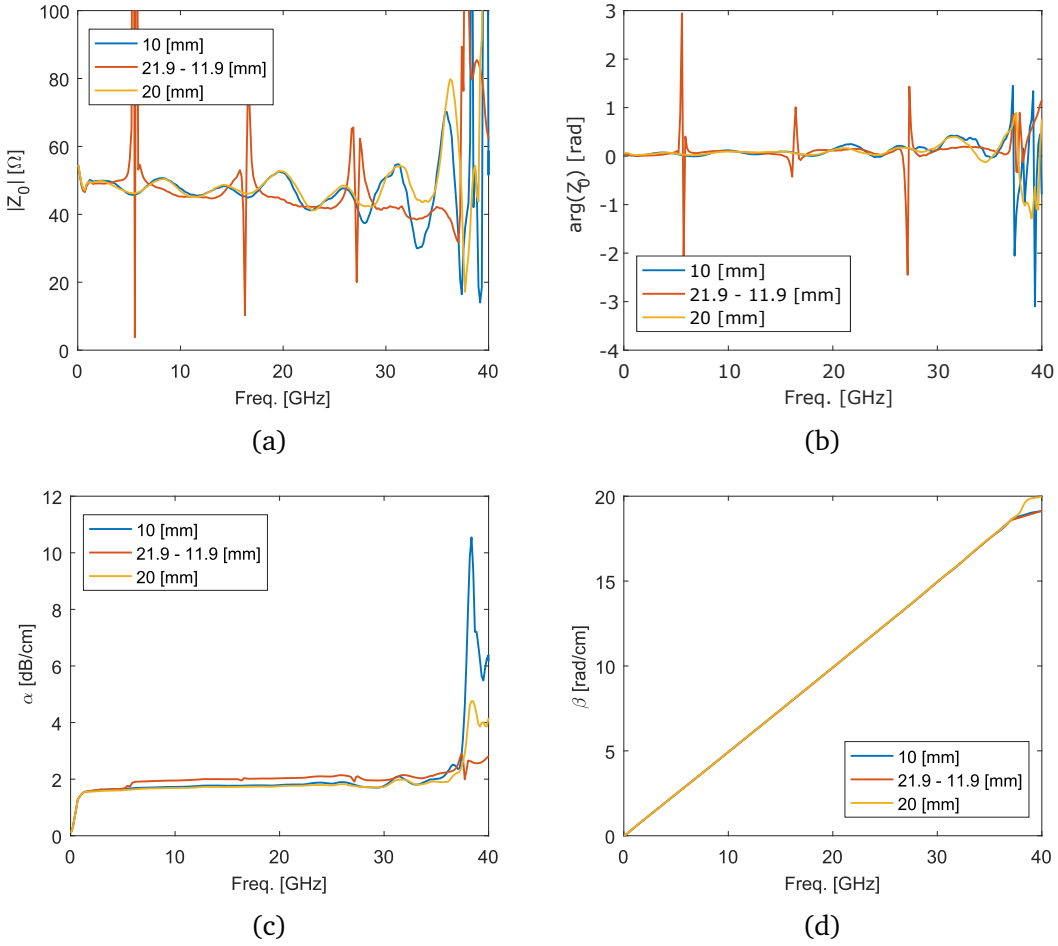


Figure 6.10: The CB-CPW transmission line parameters recovered from the co-fired AlN board calculated by using second-tier symmetric thru-only de-embedding. The second-tier calibration creates artefacts; however, the results suggest that the Z_0 is close to 50 Ω and has loss ≈ 2 dB cm^{-1} at 40 GHz

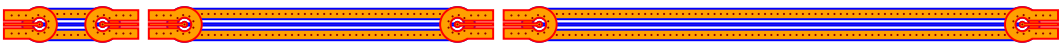


Figure 6.11: The structures used to characterise the SM-CPW in the co-fired AlN board. The structures have three different SM-CPW lengths.

the 21.9 mm line. The results show better agreement in the attenuation (α) and the phase constant (β) than the results without the second-tier calibration (Figure 6.10). However, the Z_0 results present some artefacts that were not present before. But, the results suggest that the Z_0 starts at 50 Ω decreasing with the frequency to 40 Ω, and that the loss is $\approx 2\,\mathrm{dB\,cm^{-1}}$ at 40 GHz.

In conclusion, the transmission line parameters were recovered from the measurement of several CB-CPW lines with different lengths. In order to calculate the transmission line parameters, a second-tier symmetric thru-only calibration was completed. The results show artefacts, but are good enough to suggest the Z_0 for the CB-CPW is close to 50 Ω and the loss is approximately $2\,\mathrm{dB\,cm^{-1}}$ at 40 GHz; accomplishing our objectives.

6.2.2 SM-CPW

Three different structures were created to characterise the SM-CPW (Figure 6.11). The structures have three different total lengths, 6.4 mm, 16.4 mm and 26.4 mm. The structure length is varied by changing the SM-CPW length. A first-tier SOLT calibration was performed using a commercial calibration substrate in the VNA. Ten copies, one for each fabricated board, were available for each structure. Additionally, the shortest structure from Figure 6.11 had copies in other places of the layout. Therefore, many structures were available for this measurements. However, the repeatability is very high and thus only 3 measurements are used.

In order to remove the effect of the vertical transition from the measurements of the structures, a symmetric thru-only de-embedding procedure is completed as described in Section 2.4.1. Using the 6.4 mm long segment as the thru element, SM-CPW segments with length equal to 10 mm and 20 mm can be de-embedded from the elements with length equal to 16.4 mm and 26.4 mm. Also, an SM-CPW with length equal to 10 mm can be obtained by using the 16.4 mm element as the thru element and de-embedding the symmetric pads from the 26.4 mm element. All the results contain artefacts since our thru elements are clearly not made by two symmetric pads. The best results were obtained for the 6.4 mm line used as the thru element and de-embedding into the 16.4 mm line, leaving a 10 mm segment. Even with the artefacts, the results show that the SM-CPW has a Z_0 close to 50 Ω and that it has a loss around $2\,\mathrm{dB\,cm^{-1}}$ at 40 GHz (Figure 6.12).

In conclusion, the de-embedding of the performance of the SM-CPW presents artefacts, however the results suggest that our lines meet our objectives.

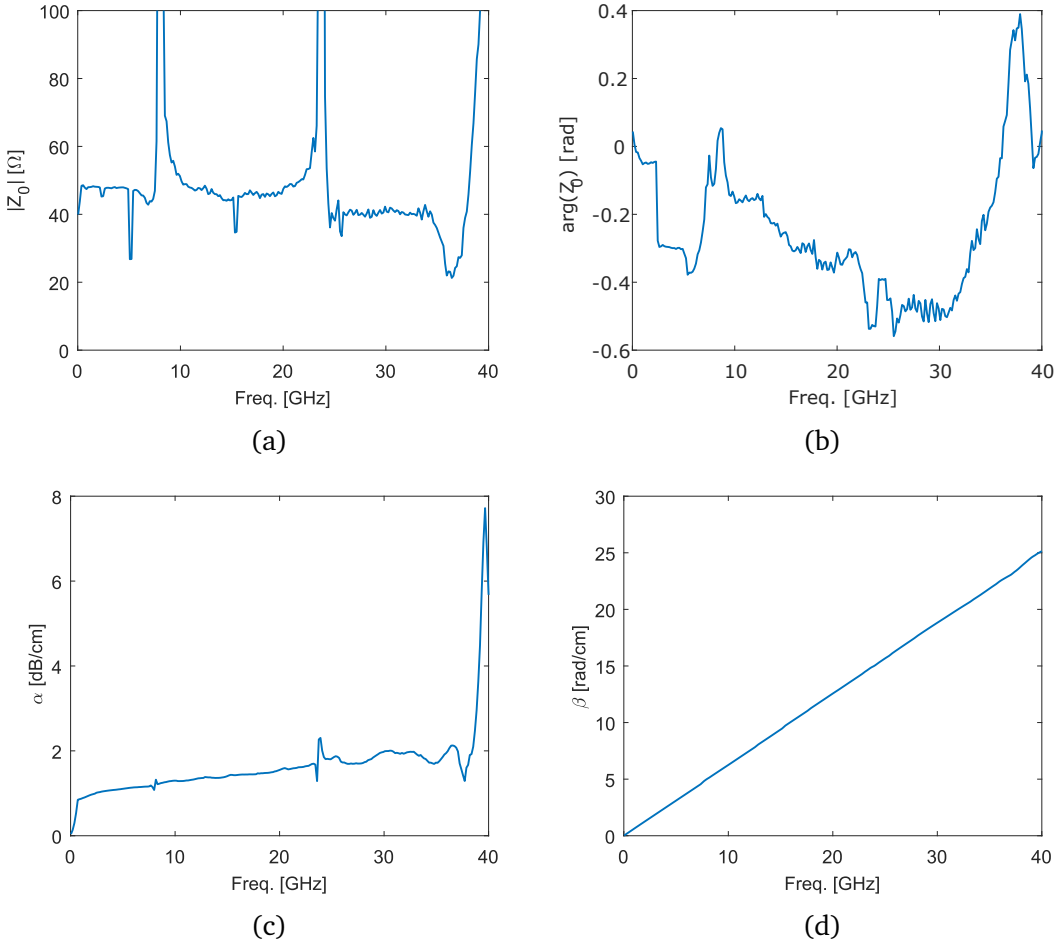
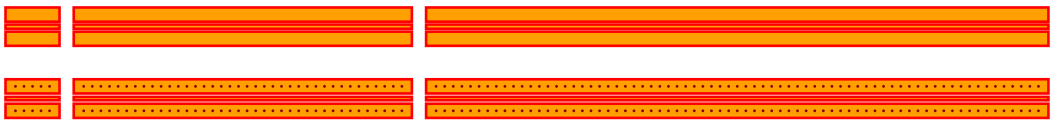
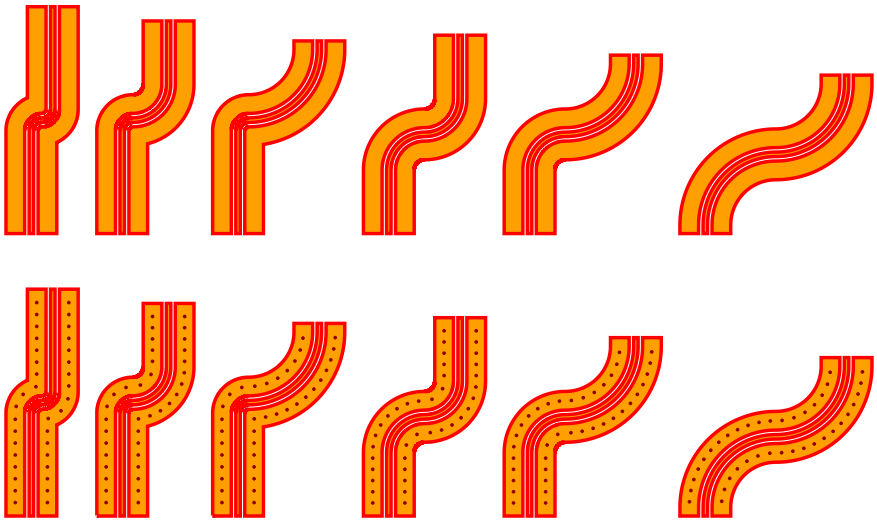


Figure 6.12: The SM-CPW transmission line parameters recovered from the co-fired AlN board calculated by using second-tier symmetric thru-only de-embedding (the 16.4 mm line de-embedded with the 6.4 mm). The second-tier calibration creates artefacts, however, the results suggest that the Z_0 is around 50 Ω and has loss ≈ 2 dB cm^{-1} at 40 GHz.



(a) Straight lines



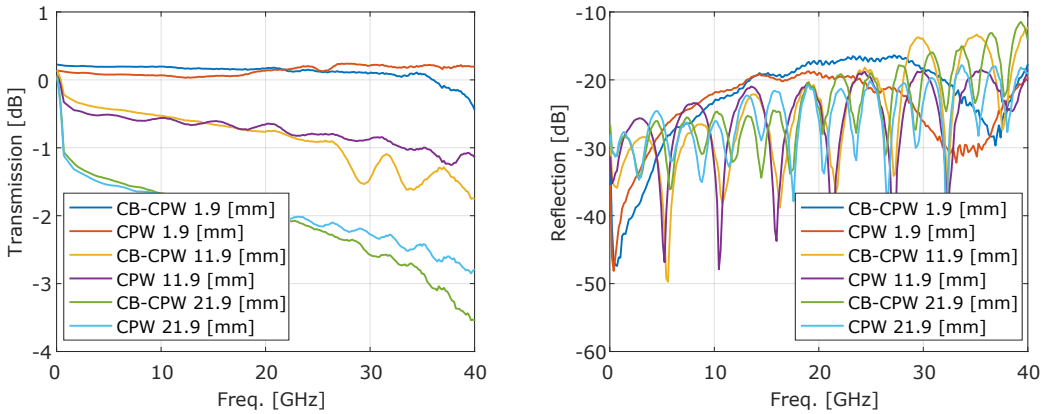
(b) Bends

Figure 6.13: Structures fabricated in the co-fired AlN board to characterise the effect of the ground vias in the CB-CPW.

6.2.3 Effect of the ground vias

Some structures were fabricated and measured to characterise the effect of the ground vias in the CB-CPW (Figure 6.13). First, three straight lines with a co-planar waveguide (CPW) transmission lines, ground metal present but no ground vias, were fabricated (Figure 6.13a). The CPW was designed to have a Z_0 equal to 50 Ω using the cross-sectional electromagnetic solver, the signal width was set to 150 µm, the gap width to 100 µm, and the ground width to 500 µm. The lengths of the CPW lines are 1.9 mm, 11.9 mm and 21.9 mm; the same as in Section 6.2.1 for the CB-CPW. Since the lines have the same length they provide a direct comparison. Additionally, several bends were fabricated for both the CPW and the CB-CPW. All the structures in Figure 6.13b have the same length (6 mm). Three curvature radii were used: 286 µm, 955 µm and 1891 µm, with an arc angle of $\pi/2$. All the possible combinations of two bends with these curvature radii were fabricated since a combination of mismatched bend radiuses could excite the CPW odd mode.

The scattering parameters (S-parameters) were measured using the VNA for the straight CPW structures and compared to the measurements of the CB-CPW straight lines (Figure 6.14). The CPW lines (without ground vias) do not present parasitic features related to the patch antenna modes of the ground metalsand, after 25 GHz, the CB-CPW has lower transmission and higher reflections than the CPW. This might indicate that the placement of the ground vias is creating additional losses and



(a) (b)

Figure 6.14: Comparison of the effect of the ground vias on the straight lines. The CPW lines (without ground vias) do not present parasitic features and the use of ground vias increases the loss of the lines.

impedance mismatches and that the vias should be placed further away from the signal metal.

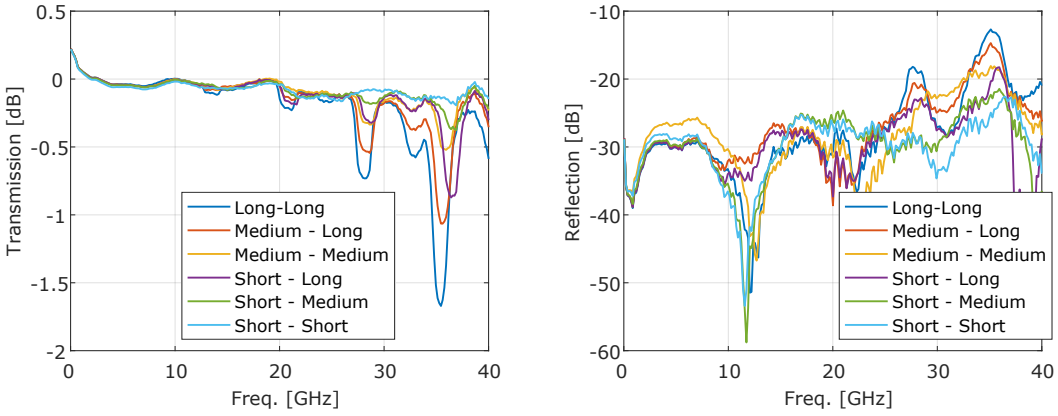
The bends using CPW and CB-CPW were measured for comparison (Figure 6.15). The CPW bends show some parasitic features at 27 GHz and 35 GHz. This effect is stronger when the bend radius is larger. However, the effect does not disappear in symmetric devices, as is expected if the source of the extra loss is due to the excitation of the odd mode. Therefore, the source of this parasitic effect is unknown. However, the ground vias are successful in removing this parasitic effects at 27 GHz and 35 GHz.

In conclusion, the ground vias increase the losses in the transmission lines, which might indicate the need for a larger separation between the ground vias and the signal metal. On the other hand, the ground vias remove a parasitic effect that occurs in bends with a large arc radius.

Section 6.2 presented the measurements that characterise the CB-CPW and the SM-CPW in a board fabricated using co-fired AlN. The results have some artefacts due to the second-tier de-embedding procedure. However, the results are good enough to show that the CB-CPW and the SM-CPW have a Z_0 close to 50 Ω and a loss approximately 2 dB cm^{-1} at 40 GHz. Finally, the measurement of some structures to understand the effect of the ground vias showed that the ground vias removed some parasitic effects created by bends, but also increased the loss of the transmission line.

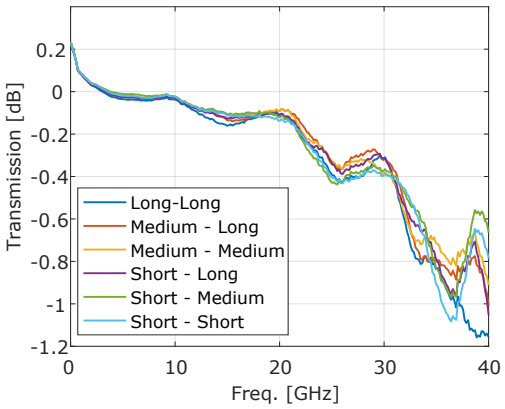
6.3 Vertical transition

The vertical transition was measured using a VNA and a digital communication analyser (DCA). The performance of the design presented in Chapter 4 is presented in

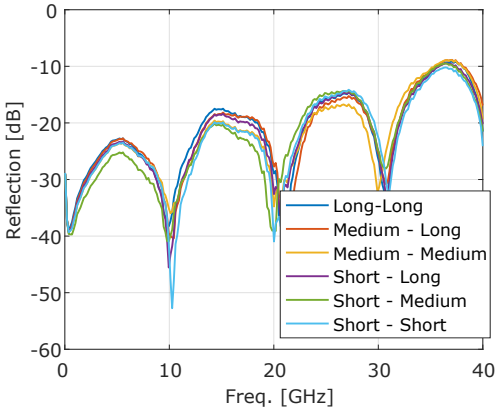


(a) CPW

(b) CPW

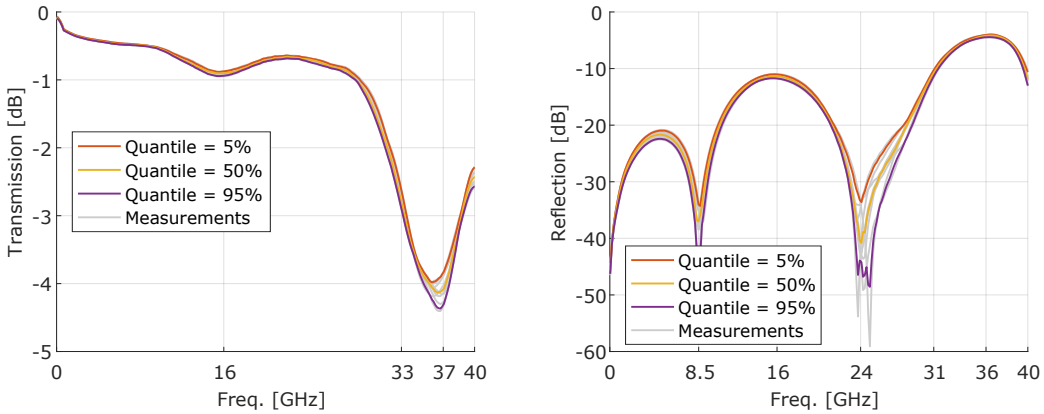


(c) CB-CPW



(d) CB-CPW

Figure 6.15: Comparison of bends using CPW and CB-CPW in co-fired AlN. The CPW bends show some parasitic features at 27 GHz and 35 GHz but less loss than the CB-CPW.



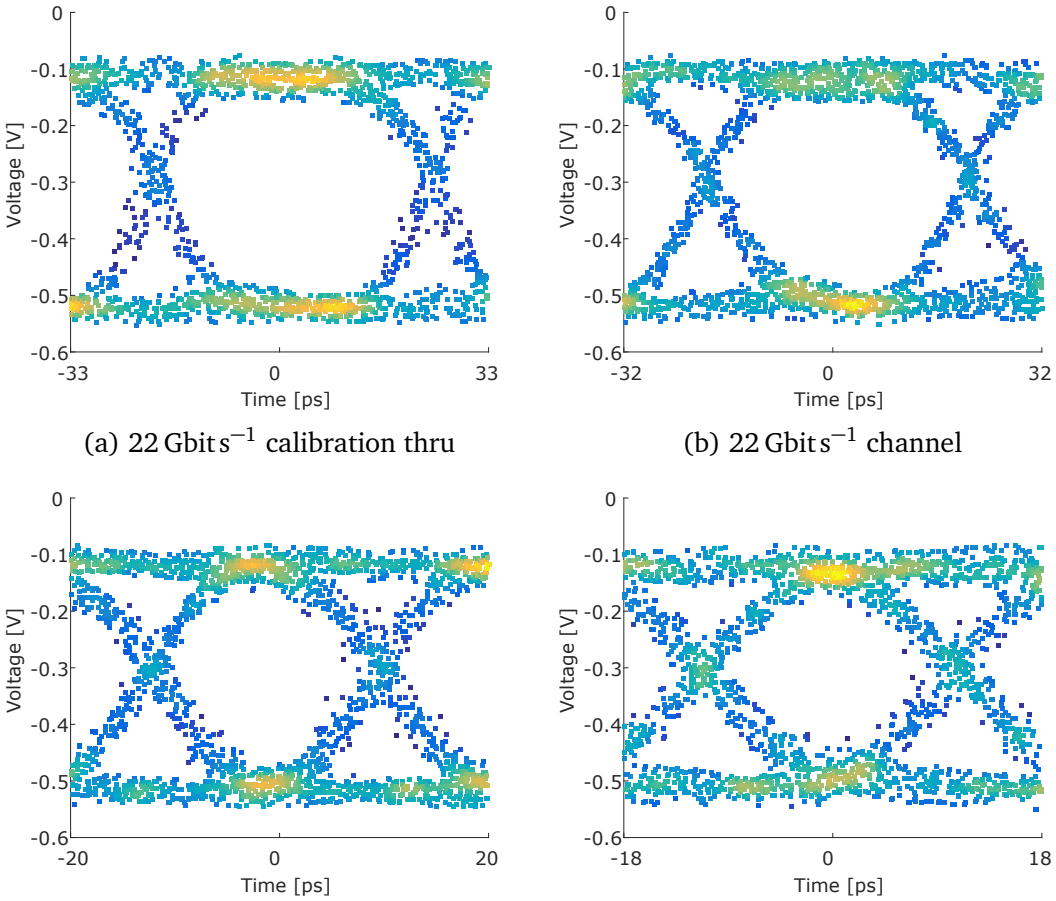
(a) (b)

Figure 6.16: The measured performance (VNA) of the vertical transition fabricated in co-fired AlN. The devices under test are 6.4 mm lines with two transitions. Fourteen devices were measured (plotted in grey). The 5 % and 95 % quantiles for all the measurements at each frequency were calculated. The transmission (S_{21}) shows a 3 dB bandwidth of 33 GHz. There is some manufacturing variability is low compared with the low-temperature co-fired ceramic (LTCC) board.

Section 6.3.1. An experiment was completed in order to optimise the transition and the measured results are presented in Section 6.3.2. Finally, Section 6.3.3 presents the fitting between the measurements and the electromagnetic full-wave model.

6.3.1 Measured performance

The transition showed good results with the VNA as can be seen in Figure 6.16. The devices under test are 6.4 mm lines with two transitions. A first-tier SOLT calibration, using calibration substrates, was performed to remove the effect of the cables and probes. As a second-tier calibration, the symmetric pads calculated from the CB-CPW by the thru-only calibration was tried but result in a large dip at 37 GHz that seems artificial. For this reason, the results include those parasitic effects. The fourteen measured reflection (S_{11}) and transmission (S_{21}) results are plotted in grey in Figure 6.16. The 5 %, 50 % (i.e. median) and 95 % quantiles for all the measurements at each frequency are also plotted in Figure 6.16. The transmission, shown in Figure 6.16a, shows a 3 dB bandwidth ($f_{3\,\mathrm{dB}}$) of 33 GHz but with a transmission above −3 dB at 40 GHz. This is due to a transmission minimum at 37 GHz. The manufacturing variability is below 0.1 dB for most of the frequency range, except for the dip at 37 GHz, which compares favourably to the LTCC board. The reflection variability is shown in Figure 6.16b. This variability is larger at frequencies around the quarter-wavelength dips (8 GHz and 24 GHz) and the reflection is below −10 dB up to 31 GHz.



(a) 22 Gbit s^{-1} calibration thru

(b) 22 Gbit s^{-1} channel

(c) 44 Gbit s^{-1} calibration thru

(d) 44 Gbit s^{-1} channel

Figure 6.17: The eye diagram transmitted through a double transition in the co-fired AlN board.

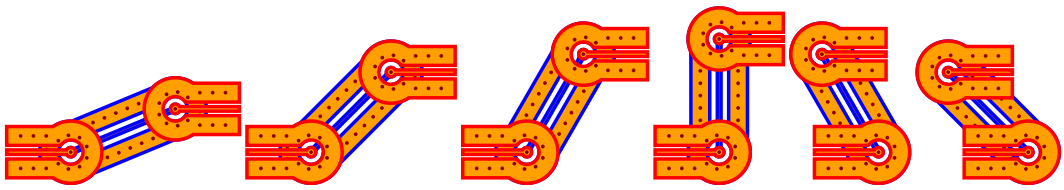
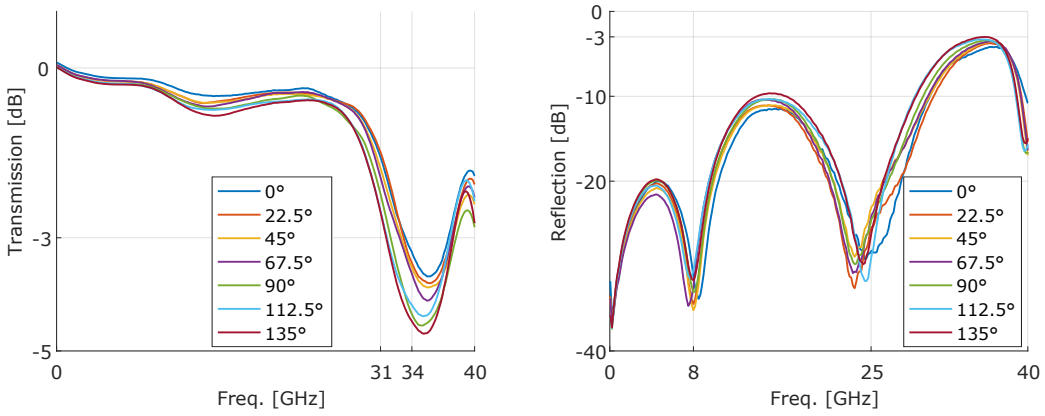


Figure 6.18: The vertical transition on the co-fired AlN under several angles of rotation.



(a) (b)

Figure 6.19: The results from the VNA for the vertical transition under rotation for the co-fired AlN board. The rotation only reduces the $f_{3\,\mathrm{dB}}$ by 3 GHz.

Figure 6.17 shows the results of the DCA measurements, using the same device that was measured with the VNA. The test setup, consisting of a DCA using 22 Gbit s^{-1} and 44 Gbit s^{-1} pseudorandom binary sequence generator (PRBSG) connected to the device under test (DUT) using RF probes. Figures 6.17a and 6.17c show the measured eye pattern of a thru from the calibration substrate, and Figures 6.17b and 6.17d show the measured eye diagram of the transition. The degradation is small and meets our objectives.

In conclusion, the VNA and DCA measurements show that the vertical transition meets the objectives defined for this research and can be used in channels working at data rates of 40 Gbit s^{-1}.

6.3.2 Vertical transition variations

Several vertical transitions with different angles were fabricated (Figure 6.18). The transitions have two sections of CB-CPW with a length of 1.7 mm and an middle section of SM-CPW with a length of 3 mm, for a total length of 6.4 mm; the same as in Section 6.3.1. Six structures with angles of 22.5°, 45°, 67.5°, 90°, 112.5° and 135° between the CB-CPW and the SM-CPW were measured.

The results from the VNA for the vertical transition under rotation for the co-fired

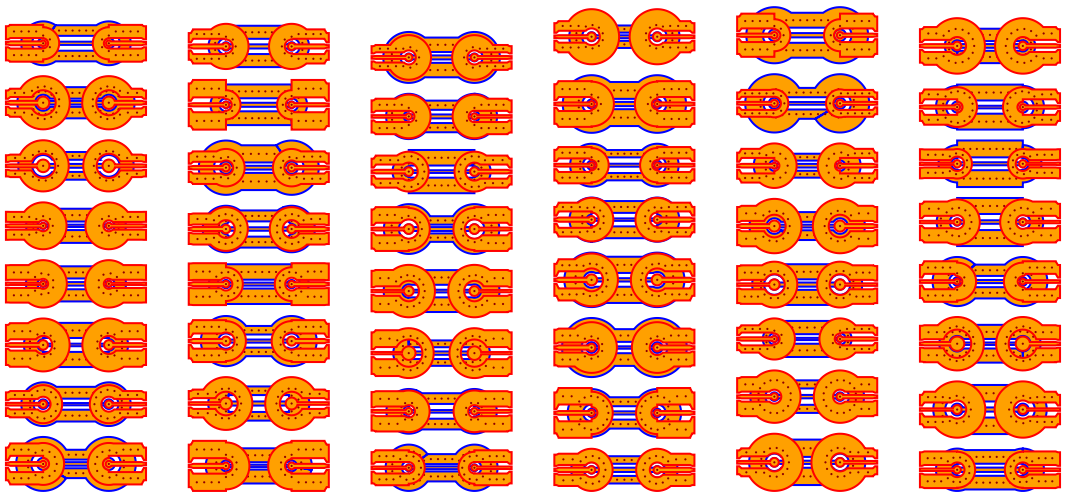


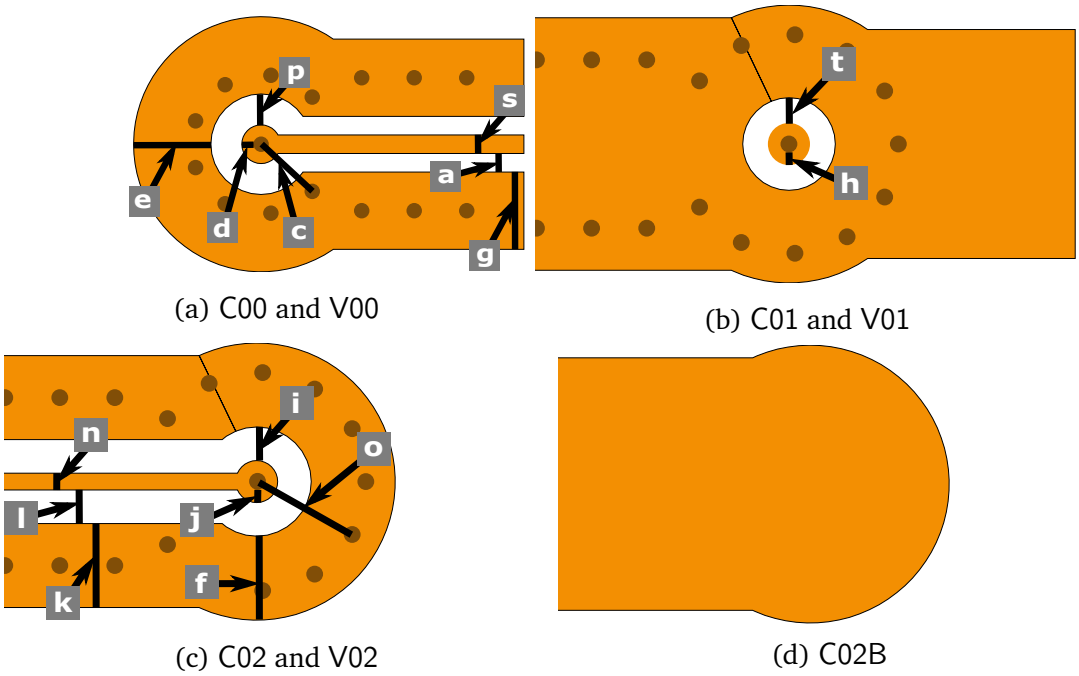
Figure 6.20: The 48 variations of the vertical transition for the co-fired AlN board.

AlN board show that the $f_{3\,\mathrm{dB}}$ is only reduced by 3 GHz. The reflection is also increased with the rotation angle, but only by around 2 dB. The performance is still good for the larger angles and the insertion penalty is small.

In order to optimize the vertical transition, 48 variations of the vertical transition were fabricated in the co-fired AlN board (Figure 6.20). The variations were constructed using the package *DiceDesign* for *R* [1]–[3]. *DiceDesign* was used to create a *Latin Hypercube Sampling* in order to sample the design space.

A total of 16 design parameters were used as variables for the sampling (Figure 6.20). The 16 design parameters used are: the three variables that define the CB-CPW in layer C00, the signal width (s), the gap width (a) and the ground width (g); three variables that define the coaxial-like catch-pad at layer C00, the signal via catch-pad oversize (d), the gap width (p) and the ground width (e); the coaxial-like radius at layer V00 (c); at the ground layer C01, the ground iris is defined by the signal catch-pad oversize (h) and the gap (t); as for the CB-CPW, the three variables that define the SM-CPW in layer C02, the signal width (n), the gap width (l) and the ground width (k); three variables that define the coaxial-like catch-pad at layer C02, the signal via catch-pad oversize (j), the gap width (i) and the ground width (o); finally, a second coaxial-like radius but this time for layers V01 and V02 (f).

The maximum and minimum for each design parameter in our experiment were defined in order to comply with the fabrication design rules (Table 6.1). The signal widths of the CB-CPW and the SM-CPW were varied from 100 µm to 300 µm. The low limit of 100 µm is imposed by the fabrication and the high limit of 300 µm is chosen since larger traces are not as practical for high-density applications. For similar reasons, the gap widths (a and l) range from 100 µm to 300 µm and the ground widths (g and k) range from 300 µm to 800 µm. The coaxial-like radii (c and o) are sampled in the range 350 µm to 800 µm. The minimum of 350 µm is needed in order to fit the signal via, its catch-pad and a gap of at least 100 µm. The signal catch-pads in the CB-CPW layer and the SM-CPW layer (d and j) are sampled between



(a) C00 and V00

(b) C01 and V01

(c) C02 and V02

(d) C02B

Figure 6.21: The 14 design parameters used for the experiment.

Table 6.1: The design parameters and their range for the optimization experiment in the co-fired AlN board.

Variables	Minimum [μm]	Maximum [μm]
s,n	100	200
a,l	100	300
g,k	300	800
c,o	350	800
d	75	(c-200)/2
p	100	c-d-150
e	c-p	900
j	75	(o-200)/2
i	100	o-j-150
f	o-i	900
h	75	min(c,o)-275
t	100	min(c,o)-h-75

Table 6.2: The value of each design parameters for the first 24 the variations from the optimization experiment on the co-fired AlN board.

Id	s	a	g	c	d	p	e	n	l	f	o	j	i	k	h	t
1	178	146	690	701	204	263	724	130	128	445	638	123	181	780	328	127
2	166	272	415	606	77	105	784	167	148	315	426	79	109	701	102	138
3	137	230	315	458	107	145	336	125	218	425	647	205	246	830	120	153
4	150	236	675	422	95	129	456	196	248	680	660	220	254	756	80	162
5	200	122	515	633	117	172	623	195	180	345	683	121	180	578	126	306
6	170	298	755	768	89	128	699	144	234	410	584	140	194	706	166	209
7	197	132	635	507	124	167	815	110	204	580	593	194	221	884	106	154
8	195	294	550	741	202	271	680	151	240	740	746	124	186	882	286	202
9	193	278	400	570	113	163	668	113	252	540	453	76	103	779	105	115
10	130	244	520	363	75	101	555	135	290	335	543	155	193	580	77	105
11	144	248	725	426	81	112	776	192	140	770	602	159	212	894	117	121
12	140	202	440	534	144	186	877	132	122	325	710	156	225	588	95	203
13	114	206	535	557	85	119	474	128	104	455	768	106	158	743	192	110
14	129	156	700	408	102	129	670	119	278	490	386	80	109	781	86	122
15	105	224	770	786	260	313	515	153	194	310	417	89	122	446	129	106
16	107	164	745	728	173	245	728	122	226	670	507	105	149	840	205	125
17	132	220	715	597	172	218	519	177	112	385	795	164	242	681	312	101
18	164	240	410	710	147	215	498	123	216	710	368	76	102	512	88	100
19	118	196	555	390	91	119	736	180	212	420	777	77	104	802	80	112
20	135	166	335	471	116	154	695	183	156	660	786	129	195	788	164	129
21	188	260	790	507	104	147	770	108	114	635	467	81	112	681	99	160
22	121	186	390	692	222	267	666	187	292	395	359	79	104	577	77	101
23	191	252	610	525	156	187	517	141	230	390	521	128	173	795	220	101
24	179	102	765	557	99	143	476	137	134	705	561	138	188	404	209	172

Table 6.3: The value of each design parameters for the final 24 variations from the optimization experiment on the co-fired AlN board

Id	s	a	g	c	d	p	e	n	l	f	o	j	i	k	h	t
25	182	114	505	678	145	210	593	157	270	500	368	75	100	836	88	102
26	157	190	475	494	118	161	525	173	152	785	692	235	270	684	80	113
27	147	266	795	399	91	122	401	184	206	630	449	102	139	415	98	110
28	187	256	430	444	116	146	719	190	254	595	516	142	180	426	135	125
29	171	286	565	620	91	130	686	163	116	450	701	227	272	683	339	100
30	121	180	360	656	117	173	528	104	200	540	611	168	220	558	302	124
31	168	176	735	543	167	196	794	116	260	690	624	88	126	614	187	105
32	103	136	670	485	76	102	853	162	166	555	444	88	123	523	123	100
33	143	104	460	440	84	116	819	106	142	585	476	89	125	515	83	168
34	138	140	305	683	238	266	614	175	190	355	674	194	251	642	181	217
35	174	174	380	746	233	290	642	166	104	525	534	134	180	812	158	171
36	177	152	600	354	76	101	505	148	266	485	719	193	260	498	79	100
37	115	160	620	575	117	169	484	199	176	625	489	79	109	728	83	159
38	109	268	490	624	153	211	870	189	272	755	728	220	279	543	242	135
39	156	128	640	791	277	319	574	112	162	645	570	126	179	457	77	165
40	123	290	575	377	78	106	629	143	186	515	494	144	171	755	99	100
41	111	228	650	651	106	156	721	160	288	730	759	115	173	595	198	247
42	101	118	485	476	120	158	347	139	224	770	413	90	123	588	105	107
43	150	280	450	719	82	114	660	120	242	725	656	203	249	466	280	159
44	161	196	585	777	143	214	859	170	136	565	399	87	119	311	109	102
45	127	210	365	665	150	214	891	148	174	790	615	145	203	753	268	120
46	160	148	665	759	107	160	878	155	296	370	737	144	214	688	167	244
47	154	216	330	377	82	110	697	101	168	605	390	90	119	271	84	105
48	114	158	665	638	188	237	570	188	146	690	629	183	232	547	281	100

a minimum of 75 µm, to comply with the fabrication design rules, and a maximum calculated so that the catch-pad leaves enough space for the minimum gap width required. The coaxial-like structure gaps widths (p and i) are sampled between a minimum of 100 µm again to comply with the design rules and a maximum that was calculated to ensure that the ground catch pads cover the ground vias. Similarly, the ground widths of the coaxial-like structure catch-pads (e and f) are sampled between a minimum calculated to ensure the pads cover the ground vias and a maximum of 900 µm. Larger catch pads have a footprint too large for or applications. Finally, the ground iris signal catch-pad (h) is sampled between a minimum of 75 µm to comply with the fabrication design rules and a maximum calculated to be large enough to ensure the coverage of both the coaxial ground vias in both layer V00 and layers V01 and V02. The values for each of the structures defined by the sampling are given in Tables 6.2 and 6.3.

The results of all the variations created for the optimization experiment were tested with the VNA (Figure 6.22). The results show some frequencies where dips in the transmission are recurrent, 15 GHz, 29 GHz and 35 GHz. The reflection shows that for most of the variations the reflection is above −10 dB at 10 GHz. The variations in the higher transmission average are the variation 18, 4 and 48 in that order. Transition 18 is the second from the top in the third column in Figure 6.20, transition 4 is the fourth from top in the first column and transition 48 is in the bottom of the sixth column. The comparison of the results of these three transitions to the manually optimized version (Section 6.3.1) shows that none of the transitions in the experiment has better $f_{3\,\mathrm{dB}}$ or lower reflection than the version optimized by time-domain reflectometry (TDR). However, transition 18 and 4 have better transmission from 10 GHz to 30 GHz and at 40 GHz. These results show that the design presented in Section 4.3 is well optimised.

Using the results in Figure 6.22a at 15 GHz, 30 GHz and 37 GHz; response-surface models for each of the three frequencies were calculated by using the rsm function in R [4]. The code used in this procedure is provided in Appendix A.2.3. The transmission shows high variability at these three frequencies that the response-surface model may help to explain. In order to calculate the models, all the variables (Table 6.1) are used to calculate the first-order fit. The results of the first-order fit are used to identify the seven variables with the highest effect by comparing the slope of the linear fit and then using these seven variables to calculate the response-surface model that includes the two-way interactions. Only seven variables are used for the two-way interactions to avoid having more fitting variables than response data. The response-surface contours for the two-way interaction with the highest effect in the transmission at the three chosen frequencies is shown in Figure 6.23 as example of the insights that this type of analysis provide.

In future work, in order to use this experiment to optimize the transition, *DiceEval*, or other model fitting techniques, used with the measured results of our experiment may provide ideas for further optimization. On the other hand, the dip around 35 GHz appears for most of the variations, pointing to a common cause. One thing that all these variations have in common is the substrate thickness and therefore the

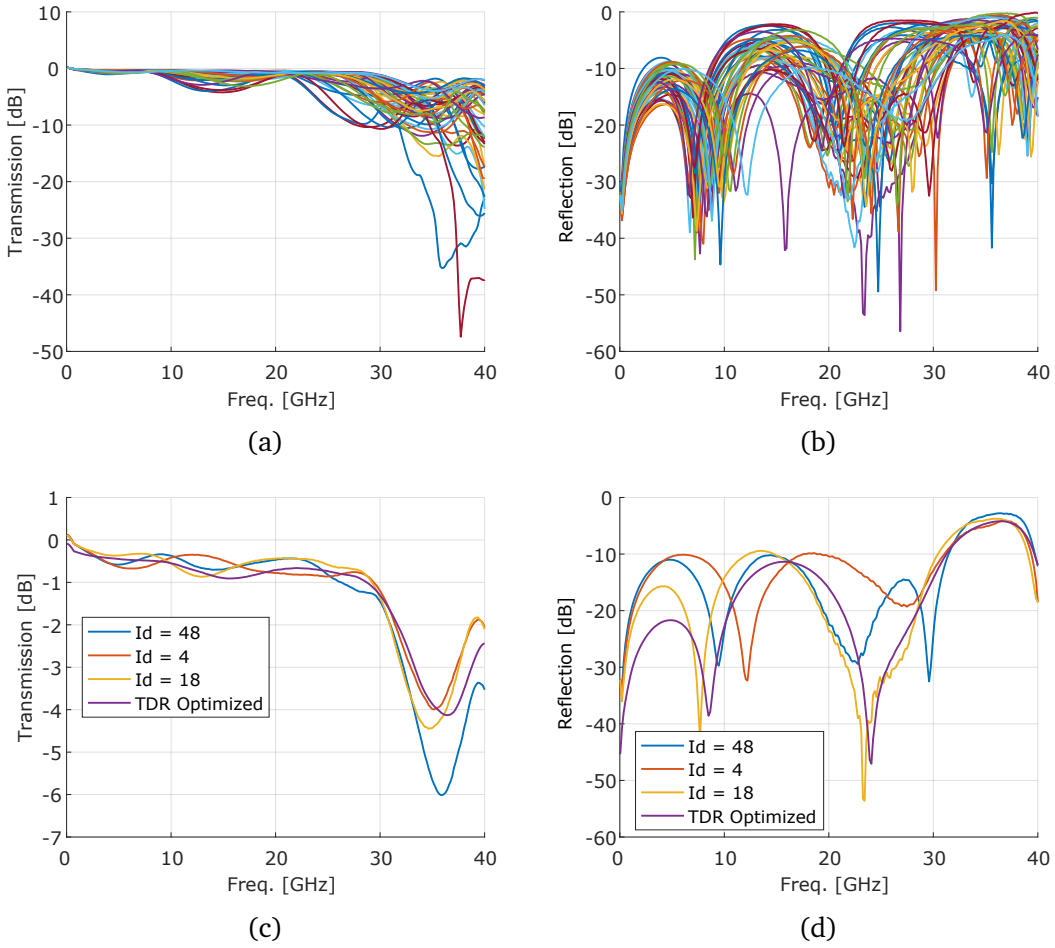
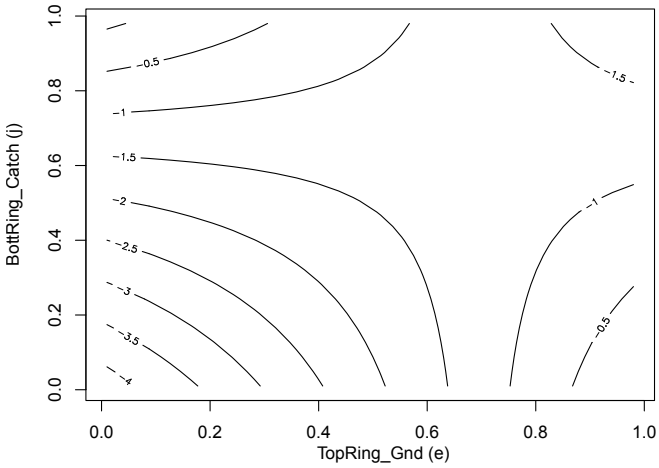
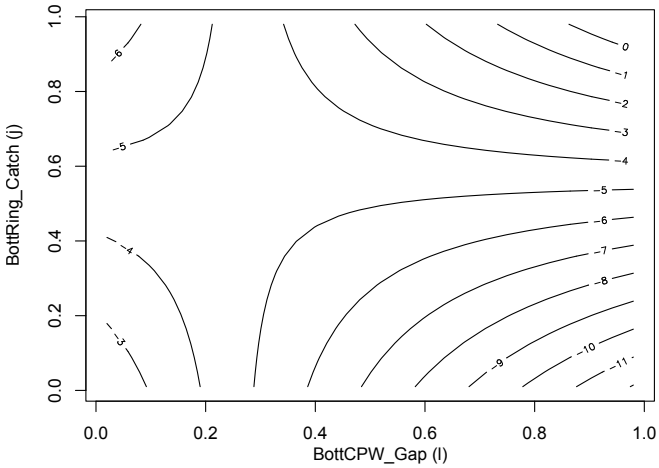


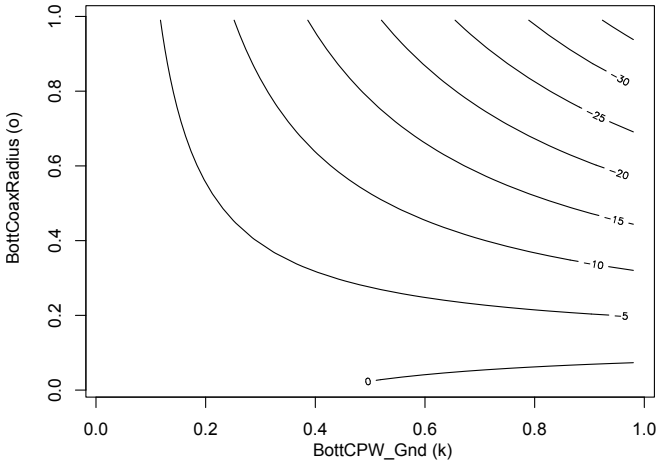
Figure 6.22: The measured results of the optimization experiment for the vertical transition in the co-fired AlN board. The best designs, (c) and (d), from the experiment have similar performance but not better than the original transition.



(a) 15 GHz



(b) 30 GHz



(c) 37 GHz

Figure 6.23: The contour plot of the main two-way effects on the response-surface model calculated from the experiment. All the other design parameters are set to the middle of the range.

resonance might come from a resonance that is fundamental and thus, compensation techniques would be needed to suppress this resonance.

In conclusion, the vertical transition shows good results under rotation and the optimization experiment found three designs with similar performance to the version that came from the design procedure in Section 4.3.

6.3.3 Fitting to the simulation model

As in Section 5.3.3, two models of the transition have been constructed: a full-wave simulation and a circuit simulation. The full wave model can be used to simulate the performance of variations of this transition and the circuit model can be used to simulate the performance of the transition in a given system.

The full-wave model is shown in Figure 6.24a. The model is for a 6.4 mm line with the same dimensions measured in Section 6.3.1. The full-wave model is the same used in Chapter 4 but with the metal thickness and the thickness of the substrate adjusted based on the measurements (Section 6.1).

The circuit model is shown in Figure 6.24b, it consists of three distinct elements: A transmission line model of a CB-CPW section (Chapter 3), a transmission line model of an SM-CPW section and the model of a CB-CPW to an SM-CPW vertical transition (Chapter 4). All the dimensions are the same as in the fabricated devices shown in the previous section and in the full-wave model. The CB-CPW model is based on the results presented in Chapter 3 with a length of 0.72 mm and the thickness measured in Section 5.1. The length of the SM-CPW is 1.34 mm. The CB-CPW to SM-CPW vertical transition (similar to Figure 4.17) has a total length of 1.81 mm, the length from the start of the CB-CPW to the signal via centre is 0.98 mm and the length from the signal via centre to the end of the SM-CPW is 0.83 mm. The scattering parameters (S-parameters) of the vertical transition were calculated using the full-wave simulation. The simulated circuit is constructed using two elements. First, the CB-CPW circuit is connected to the vertical transition model, then the SM-CPW circuit, followed by the vertical transition model again but with the ports swapped by reordering the scattering parameters (S-parameters) in the matrix. Finally, the last section of CB-CPW is added.

The full-wave model and the circuit model show good agreement (Figure 6.24). Also, the VNA measurements show good agreement with the simulation in the reflection. However, the VNA measurements show significantly higher loss than the simulations. The measurement result shown is the average of the measurements of all the available devices (Section 6.3.1). Figure 6.24c shows that the measured results are worse than the simulated results from the electromagnetic models. The most significant gaps occur around 36 GHz, even if we take into account the variability of the measurements (Figure 6.16. In contrast, Figure 6.24d shows good agreement between the simulated and measured reflection for most of the frequency range, except for 27 GHz. The probable sources of disagreement are: additional parasitic effects of the probe that were left since no second-tier calibration was possible, and the higher losses due to the metal roughness.

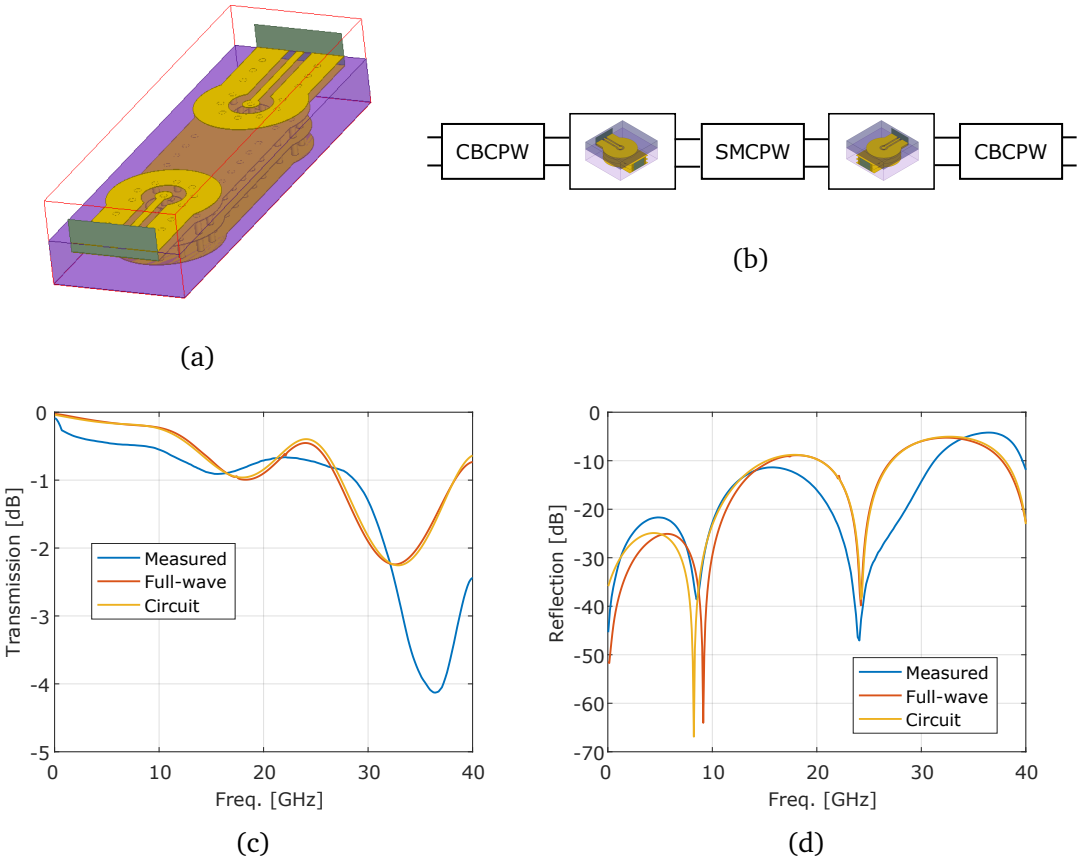


Figure 6.24: The comparison between the models used in the electromagnetic solvers and the measurements. (a) shows the 3D structure that is modelled using the full-wave electromagnetic simulator. (b) shows the model used in the circuit simulation. (c) shows that the transmission results are similar between the full-wave simulation and the circuit simulation, but the VNA measurements have higher losses. (d) shows that the reflection results agree between the full-wave simulation, the circuit simulation, and the VNA measurements.

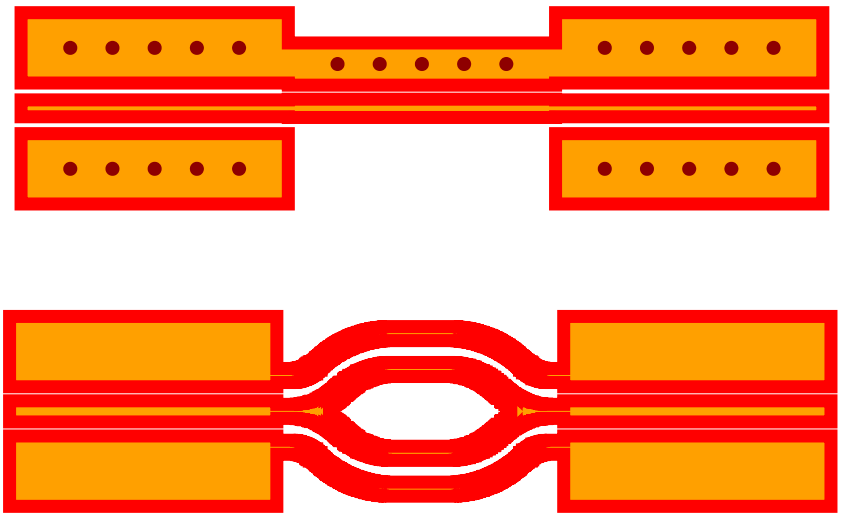


Figure 6.25: Two types of transition between ground-signal-ground (CPW) structure and ground-signal (slotline) structures.

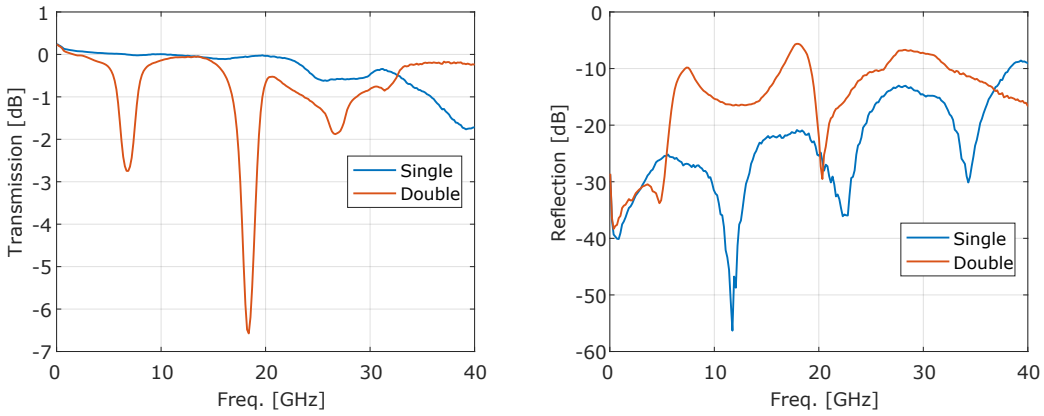
6.4 Other structures

Some other elements that are useful in carrier boards for photonic integrated circuits (PICs) were fabricated. Section 6.4.1 presents the measured results of two transitions between the CB-CPW to a conductor backed slotline (CB-SL) and Section 6.4.2 presents the measured results of a four channel phase-matched array.

6.4.1 CB-CPW to slotline transitions

Some high-speed PICs use only two metals (a ground and a signal) to bring the signal from the source [5]–[10]. However, the packaging interfaces are based on three metal structures, as are the test probes for frequencies above 20 GHz. For this reason, a transition between a three metal transmission line and a two metal transmission line is of interest.

Two types of transition between ground-signal-ground (CPW) structures and ground-signal (slotline) were fabricated in the co-fired AlN board (Figure 6.25). The first structure (the structure at the left in Figure 6.25) is a transition between a CB-CPW and an asymmetric CB-SL (CB-SL) can be described as an asymmetric conductor-backed co-planar stripline). The term asymmetric is used because the signal width is not equal to the ground width. The transitions found in the literature [11]–[17] do not use the vias to realize the transition and rather use air-bridges or bridges made with wires. The two metal transmission line was designed to be 50 Ω and to match dimensionally to the CB-CPW by using the cross-sectional electromagnetic solver. The signal width of the asymmetric CB-SL was set to 130 µm, the gap width is 100 µm and the ground width is 300 µm. The transition is the shortest possible since it consists of a back-to-back connection between the CB-CPW and the



(a) (b)

Figure 6.26: The results from the CPW to slotline transitions.

CB-SL. The second structure (the structure at the right in Figure 6.25) is a transition between a CPW and two co-planar striplines. The CPW has a Z_0 close to 50 Ω using a signal width of 150 µm, a gap width of 100 µm and a ground width of 500 µm as designed with the cross-sectional electromagnetic solver. The co-planar striplines were designed to have Z_0 around 100 Ω using signal and ground widths equal to 100 µm with a gap width equal to 155 µm. The signal metal is spliced in two, easily done using *PICDraw*, by using two bends. The separation between the two co-planar striplines is 496 µm edge to edge.

Both structures in Figure 6.25 were tested using the VNA (Figure 6.26). The CB-CPW to CB-SL transition results compare well with recently published designs [17] based on wire-bonding. The $f_{3\,\mathrm{dB}}$ for the back-to-back structure is above 40 GHz and the reflection is below −10 dB up to 37 GHz and these results include parasitic effects due to the missing second-tier calibration and the losses due to the 5.7 mm long transmission line, making the insertion loss even lower. In contrast, the CPW to two co-planar striplines has poor performance. The transmission presents some very deep dips at 7 GHz and at 18 GHz. The sources of these resonances are unclear and the search for these sources will be left for future work.

In conclusion, the CB-CPW to CB-SL transition shows good results compared to the literature as it is much shorter than others. In contrast, the CPW to double co-planar striplines has very poor performance.

6.4.2 Phase-matched array

A two and a four channel phase-matched array was fabricated in the co-fired AlN board (Figure 6.25). This type of phase-matched array is needed for PICs used in phase modulation devices like polarization multiplexed quadrature phase-shift keying (PM-QPSK). The layouts are for equally spaced channels. These arrays use the rotation capability of the second vertical transition to remove the bends and

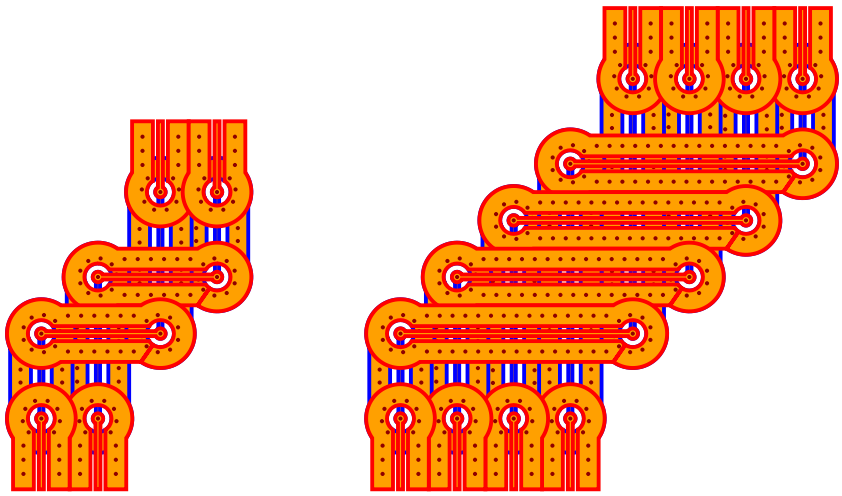


Figure 6.27: The phase-matched structures fabricatedoin the co-fired AlN board.

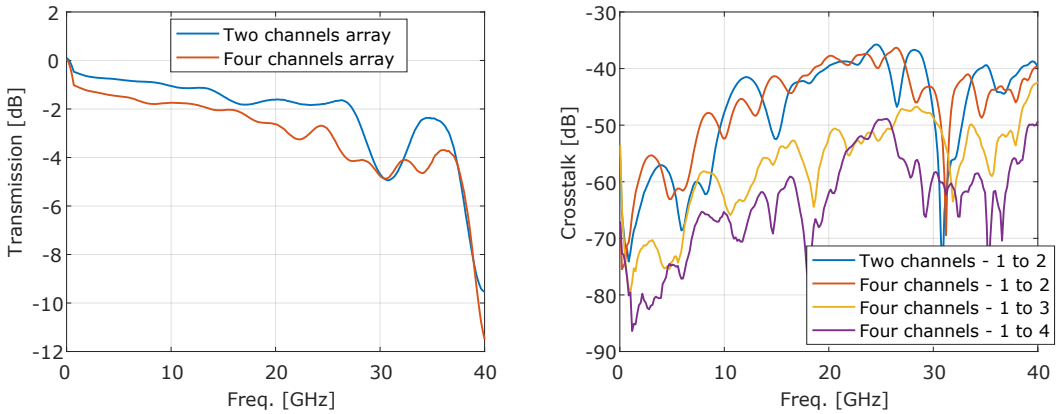
reduce the dimensions of the array. The length from top to bottom is 9 mm for the two channel array and 12 mm for the four channel array which is shorter than the 29 mm in the array fabricated in the LTCC board (Section 5.4.2). The channels start and end in CB-CPW sections but after a short distance a vertical transition is used to route the signal to the buried SM-CPW emulating the target interposer (Figure 1.9b). The routing is very simple thanks to the ease in crossing channels that the transmission lines and the vertical transition provides. After the SM-CPW section, another transition is used to bring the channel to the top layer. The phase is matched in the symmetry axis of the array. That is the point where our PIC would sit.

The transmission and crosstalk of the phase-matched arrays fabricated in co-fired AlN were measured using the VNA (Figure 6.28). The transmission is flat without many features compared to the phase-matched array in the LTCC board. The crosstalk was measured by probing adjacent channels. The crosstalk results show that the ground vias and the backside ground is able to reduce the crosstalk below −30 dB over the entire frequency range.

In order to understand the performance of the channels in the time domain, an eye diagram transmitted through one of the channels in the phase-matched array was measured using the DCA at 22 Gbit s^{-1} and 44 Gbit s^{-1} (Figure 6.29). In this way, we can evaluate the effect of the multiple features found in Figure 6.28a in the time-domain. The measured eye diagram is still open after the long channel and the four vertical transitions even at 44 Gbit s^{-1}. The comparison between the measurement of the short 500 µm thru load in the calibration substrate shows that the insertion penalties meet our objectives even for these long channels.

In conclusion, these structures have shown that the transmission lines and the vertical transition can be used to realise channels for the interposer that can achieve phase-matching and work at 44 Gbit s^{-1}.

Section 6.4 presented the measurement results of some special transitions and of a



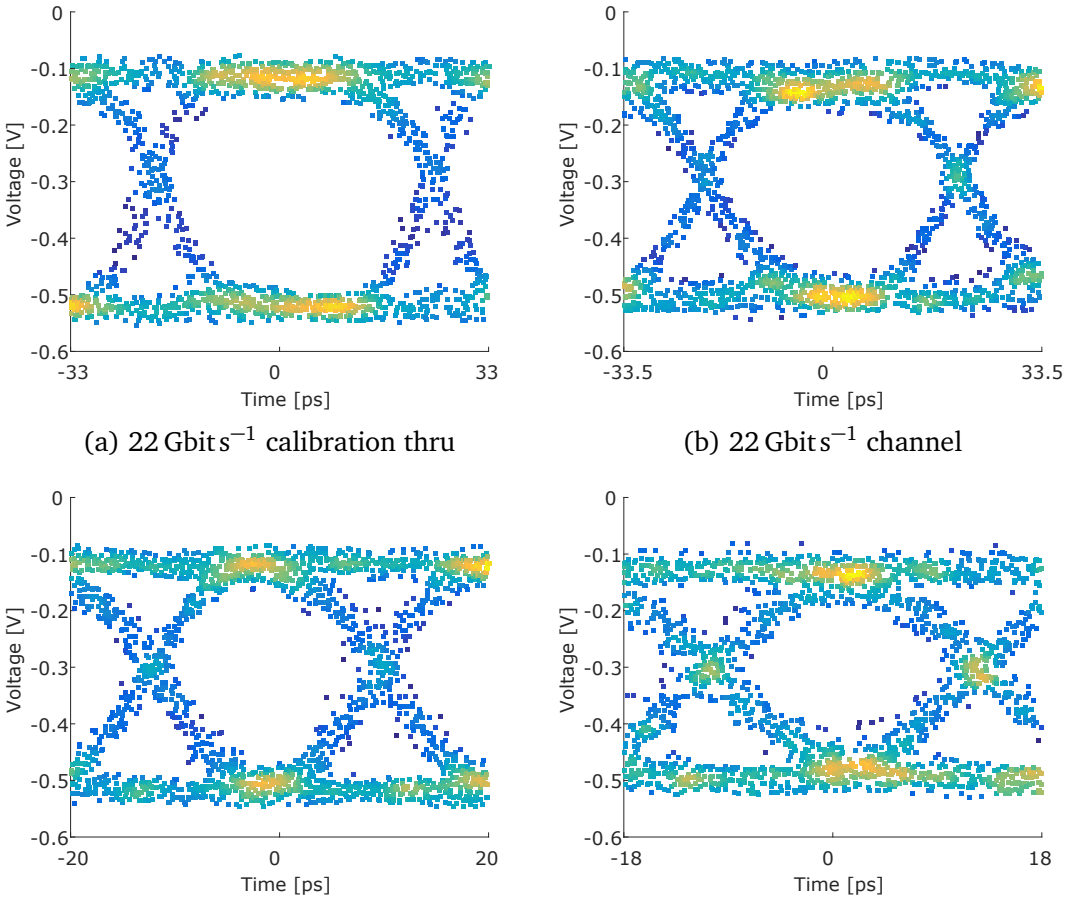
(a) (b)

Figure 6.28: The transmission and crosstalk of the phase-matched arrays fabricated in co-fired AlN.

phase-matched channel array. These structures are anticipating the requirements of future packaging for high-density PICs. The CB-CPW to CB-SL transition presented good results and the phase-matched channels performed well for our objectives with good phase-matching and acceptable penalties at 44 Gbit s^{-1}.

Chapter 6 presented the measurements done to characterise the fabricated transmission lines and vertical transition designed in Chapters 3 and 4 for co-fired AlN. The dimensional characterisation (Section 6.1) showed few defects, found by visual inspection, that explain the small variation in the electrical measurements. The measurement of the overall board thickness suggests that the substrate thickness is 133 µm rather than 127 µm. The substrate and the metal roughnesses is found to be high but better than in the LTCC board and the metal thickness is found to be around 8 µm in deviation to the 3 µm used in the design process. All these findings were accounted for when comparing the simulated to the measured results. This chapter also showed that the CB-CPW and the SM-CPW have a Z_0 close to 50 Ω and a loss less than 2 dB cm^{-1} at 40 GHz (Section 6.2). Finally, the measurement of some structures demonstrated the importance of having ground vias in realising good bends.

This chapter showed that the measurement results of the vertical transition meet our objectives and can be used in channels working at 40 Gbit s^{-1} (Section 6.3). The measurements of multiple variations of the transition show that the main design is close to optimum, with good agreement between theory and experiment for the reflection but higher losses in the measured transmission. Finally, this chapter presented the measurement results of a novel CB-CPW to CB-SL transition and of a phase-matched array (Section 6.4). The transition presented good results and the phase-matched channels performed well for our objectives with good phase-matching and acceptable penalties at 44 Gbit s^{-1}.



(a) 22 Gbit s^{-1} calibration thru

(b) 22 Gbit s^{-1} channel

(c) 44 Gbit s^{-1} calibration thru

(d) 44 Gbit s^{-1} channel

Figure 6.29: The eye diagram transmitted through one of the channels in the phase-matched array in the co-fired AlN board. The eye diagram shows that there is a small penalty resulting from the phase matched array compared to a thru element in the calibration substrate.

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Chapter 7
Conclusion

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This chapter concludes this thesis by summarising the main findings, discussing the most important conclusions and presenting the perspectives for this research.

> . . . the well in which Truth is said to reside is really a bottomless pit.
>
> *Oliver Heaviside*
> *Electromagnetic Theory, Volume I*

7.1 Findings

This section presents a summary of the main findings from this research divided into five categories: first, theoretical findings; second, findings related to the designed transmission lines; hird, findings related to the designed vertical transition; Fourth, finding related to the measurements of the designed structures in a board fabricated with low-temperature co-fired ceramic (LTCC); and fifth, findings related to the measurements of the designed structures in a board fabricated with co-fired aluminium nitride (AlN).

First, theoretical findings. An impedance-reconstruction from time-domain reflectometry (TDR) algorithm was completed with good results (Section 2.2.4). Similarly, an algorithm based on a set of equations to calculate the characteristic impedance (Z_0) and the complex propagation constant (γ) from the measurement of long lines was coded and tested (Section 2.4.3). Another theoretical novelty introduced in this thesis is the single-impedance thru-only calibration algorithm (Section 2.4.1). Other novelty is the wave-port that was designed to minimize the reflections for

full-wave time-domain simulations (Section 4.3.2). Finally, a procedure based on Latin hypercube sampling has been novelly used to investigate the optimization of the vertical transition (Section 6.3.2).

Second, findings related to the design of transmission lines. There are multiple planar waveguides that can be used, the co-planar waveguide (CPW) was found to provide the best way to mount components and the best way to shield for crosstalk (Section 3.1). The effects of the various dimensions of the structures on the microwave performance based on the cross-sectional electromagnetic solver have been found (Section 3.2). This included the effect of the ground vias in the transmission line performance, in the reduction of crosstalk and in the realisation of bends (Section 3.2).

Third, findings related to the design of the vertical transitions. Multiple vertical transitions were found in the literature, but none of them provided the right combination of cross-talk protection and performance for our application (Section 4.1). A novel vertical transition for LTCC was found to have a simulated 3 dB bandwidth ($f_{3\,\mathrm{dB}}$) above 40 GHz for a single transition (Section 4.2). An improved version of the transition for co-fired AlN that has rotation capabilities was optimized by TDR simulations and was found to have similar simulated performance (Section 4.3).

Fourth, findings related to the measurements of a board fabricated with LTCC. The visual inspection shows some recurrent defects, the dimensional measurements show that the quality of the rectangular corners is worse than for the co-fired AlN board and the measurement of the surfaces show very rough surfaces (Section 5.1). The conductor backed co-planar waveguide (CB-CPW) is found to have a Z_0 close to 50 Ω with a loss of around 1 dB cm^{-1} at 40 GHz and similar results were obtained for the shielded multi-layer co-planar waveguide (SM-CPW) (Section 5.2). However, the results for the SM-CPW have artefacts related to the second-tier de-embedding procedure. The microwave parameter extraction gave results with many of the second-tier calibration artefacts; however, the results point to higher losses than the ones used in the simulation in the metal and substrate. The first vertical transition showed a $f_{3\,\mathrm{dB}}$ of around 37 GHz for a double transition and small eye diagram penalties at 44 Gbit s^{-1} (Section 5.3). The full-wave electromagnetic simulation model of the vertical transition was found to agree with the measurements without the need of increasing the loss tangent ($\tan\delta$) or decreasing the metal conductivity. Finally, a high-speed load and a phase-matched array were found to have good performance too (Section 5.4).

Fifth, findings related to the measurements of a board fabricated with co-fired AlN. The visual inspection shows no recurrent defects, the dimensional measurements show that the quality of the rectangular corners is better than for the LTCC board, and the measurement of the surfaces show lower roughness in the

surfaces (Section 6.1). The CB-CPW is found to have a Z_0 close to 50 Ω with a loss of around 2 dB cm^{-1} at 40 GHz and similar results for the SM-CPW (Section 6.2). However, for all the results a second-tier calibration was not possible and the results show some artefacts. As in the LTCC board, the microwave parameter extraction found results with a lot of the second-tier calibration artefacts; however, the results point to higher losses than the ones used in the simulation in the metal and substrate. The second vertical transition showed a $f_{3\,\mathrm{dB}}$ of around 33 GHz for a double transition and small eye diagram penalties at 44 Gbit s^{-1} (Section 6.3). The results of 48 variations of the transition found two other designs with similar performance to the design optimized by TDR. The full-wave electromagnetic simulation model of the vertical transition was found to agree with the reflection measurements but show fewer losses than the measured transmission line. Finally, a transition between a CB-CPW and a conductor backed slotline (CB-SL) had good performance, as did the novel smaller phase-matched array (Section 5.4).

7.2 Conclusions

In conclusion, a novel system consisting of CB-CPWs, SM-CPWs and vertical transitions was designed and measured to show that it meets the typical requirements for the packaging of high-speed photonic integrated circuits (PICs) for channels working at 44 Gbit s^{-1} on boards fabricated with LTCC and with co-fired AlN. Additionally some specific conclusions are discussed next.

Some of the theoretical findings of this research could help to solve other similar problems. The novel impedance-reconstruction from the TDR algorithm was found to be useful for the optimization of the vertical transition in Section 4.3. Similarly, the novel equations to calculate Z_0 and the complex propagation constant were useful for the long lines that were fabricated. The second-tier calibration using the single impedance thru-only calibration procedure developed in this research was successful in the case of the LTCC board where short pads (50 µm) were left. The co-fired AlN was designed before developing this procedure and the pads were increased to 800 µm and thus the symmetric thru-only was the only option, which showed much worse results. The lesson here is to make sure to add structures to de-embed short pads and short lines in boards used to characterise transmission lines. The optimization procedure based on the simulated TDR experiment was very successful, together with the new lumped port and the impedance profile reconstruction algorithm, and can be repeated for any other type of transition. The experiment designed with the *Latin Hypercube Sampling* showed good results and can be used to create any other type of optimization experiment.

The CB-CPW and the SM-CPW are a good choice for transmission lines. The transmission lines show good microwave performance, that is low loss,

low crosstalk and good behaviour at bends. However, the separation between the ground vias and the signal metal is very important. The transmission lines were designed to ensure that the ground vias do not disturb the Z_0 while trying to keep the footprint small. However, the measurement indicate that the ground vias have introduced additional losses. The lesson here is to leave more space between the ground vias and the signal metal to minimize the loss.

The novel vertical transition with rotation capabilities could very useful for complex routing schemes. The rotatable vertical transition can be used with the transmission lines in systems which require channels working at speeds as high as 44 Gbit s^{-1}. The novel capability for rotation of the transition can be the key element that enables some systems that require complex routing and the use of passive microwave circuits.

LTCC offers excellent microwave performance. Structures in the LTCC board showed low losses even when there is considerable metal roughness. The importance of tight fabrication tolerances was obvious while calculating the variability on the measurements of the multiple copies of the vertical transitions.

Co-fired AlN is an attractive alternative to LTCC. In this research, the co-fired AlN board has shown higher losses than the LTCC board. However, co-fired AlN has the advantage of having a much higher thermal conductivity. Systems that include PICs need to remove the heat created by its components and to have a controlled temperature. Thus, the thermal management of the systems becomes expensive. The use of co-fired AlN can alleviate this cost and enable the system-in-a-package (SiP) concept for the next generation of PICs while still having acceptable microwave performance.

7.3 Future work

The impedance profile reconstruction algorithm was useful in the optimization of the second vertical transition. However, while the algorithm is numerically unstable and is not useful for measurements due to the noise, the author is interested in the idea of recovering the step function response by means of Equation 2.51 and then using the algorithm.

The use of symmetric pad thru-only calibration was not very successful as this resulted in artifacts for the SM-CPW and the vertical transition on the co-fired AlN board. Other de-embedding procedures are planned for future work.

Even though the CB-CPW and the SM-CPW showed good results, the use of *co-planar striplines (CPS)* is very interesting. The asymmetric *CPS* can be considered as part of the same family as the asymmetric CPW. Based on the good results of the simple transition between the CB-CPW and the asymmetric *CPS* (Section 6.4.1),

this is a good direction to realise a solution that can transition between two-metal (ground and signal) and three-metal (ground, signal and ground) transmission lines. Equation-based models could be developed by conformal mapping as in [1]–[4], spectral domain analysis (SDA) as in [5], [6] or curve-fitting as in [7].

The microwave performance of the vertical transition could be improved by using a compensating structure. The vertical transition has a resonance around 35 GHz that is very fundamental as our experiments confirmed. This resonance seems to be related to the substrate thickness based on the TDR results. A compensating structure could be used to remove this resonance as has been done for wire transitions in [8]–[11]. To develop this idea, the validated electromagnetic simulation models could be very useful.

In the future, the author plans on using the transmission lines and vertical transitions designed in this research in a system incorporating a PIC. Applications that would benefit most from these designs would have multiple high-speed channels. Besides the classic telecommunication applications, several additional applications that could use these designs exist in the field of microwave photonics, some examples in [12]–[16].

The main constraint that the LTCC and co-fired AlN present is the relatively large metal widths and via diameters. The minimal metal width is restricted by the substrate roughness and the via diameter by the brittleness of the ceramic. In the future, deposition of thermosetting epoxy layers to create multi-layer structures with etched vias on top of the ceramic, similar to the current solutions offered in the organic packages, might solve the problem of the minimum metal width and large via diameter. Two other technologies offer already smaller via diameter and metal widths: Silicon and glass. However, both technologies have fundamental problems. For Silicon is the high-speed performance and for glass is the thermal conductivity. The most likely scenario is that the multiple multi-layer technologies will find applications and continue to co-exist.

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Appendix A
Computer code developed in this research

This chapter lists code developed for this research. Appendix A.1 lists the code used to do the impedance reconstruction by multiple reflections time-domain reflectometry (TDR). Appendix A.3 presents the scripts developed to import the 2D layouts generated by PICDraw into the 3D full-wave electromagnetic simulator.

A.1 Time-domain reflectometry

This section presents the code developed to reconstruct and impedance profile taking into account the multiple reflections and a input voltage profile different from a perfect Heaviside's step function as discussed in Section 2.2.4.

A.1.1 Propagate a time step in a non-uniform transmission line

```
function [Go, Vro, Vlo] = propagate_step(Z00, Z0i, ZL, Vri, Vli, Vin)
% propagate_step — Propagates the fields of a NUTL one time step
%
% Outputs:
% Go = The reflection out of the NUTL
% Vro = An array of the field propagating to the right of NUTL
% Vlo = An array of the field propagating to the left of NUTL
%
% Inputs:
% Z00 = The source impedance
% Z0i = An array with the characteristic impedance that define the NUTL
% ZL = The final load impedance
% Vri = The fields propagating to the right at start of step
% Vri = The fields propagating to the left at start of step
% Vin = The fields propagating to the left at start of step

n = length(Z0i);
Z0 = linspace(0, 0, n+2);
Z0(1) = Z00;
```

```
Z0(2:end-1) = Z0i;
Z0(end) = ZL;

Vr = zeros(size(Z0));
Vr(1) = Vin;
Vr(2:end-1) = Vri;

Vl = zeros(size(Z0));
Vl(2:end-1) = Vli;

Vro = zeros(size(Z0));
Vlo = zeros(size(Z0));
Vri = zeros(size(Z0));
Vli = zeros(size(Z0));
for i = 2:2:n-1 % First row
    [Vri(i), Vli(i)] = propagate_lattice(Z0(i-1), Z0(i), Vr(i-1), Vl(i+1));
end
for i = 3:2:n-1 % Second row
    [Vro(i), Vlo(i)] = propagate_lattice(Z0(i-1), Z0(i), Vri(i-1), Vli(i+1)
        );
end

Vro = Vri + Vro;
Vlo = Vli + Vlo;

Go = Vlo(2);
Vro = Vro(2:end-1);
Vlo = Vlo(2:end-1);

end
```

```
function [Vro, Vlo] = propagate_lattice(Z0i, Z0ip1, Vr_im1, Vl_ip1)
    G = (Z0ip1-Z0i)./(Z0ip1+Z0i);
    Vro = Vr_im1.*(1+G) - Vl_ip1.*G;
    Vlo = Vr_im1.*G + Vl_ip1.*(1-G);
end
```

A.1.2 Impedance reconstruction by TDR with arbitrary input

```
function Z0X = reconstruct_impedance_tdr(Z00, R, Vin)
n = length(R);
Z0X(1) = Z00;
i_wf = 1;
```

```
Vwf = Vin(i_wf);
Vrp = zeros(0);
for j = 1:n
    % Propagate assuming matched load
    Z0X(end+1) = Z0X(end);
    [~, R_m] = propagate_diagonal(Z0X, Vrp, Vin(j));
    % Calculate next Z0X
    Gamma = calculateGamma(Z0X);
    Gamma_wf = (R(j) - R_m)./(Vwf*prod(1-Gamma.^2));
    Z0X(end) = Z0X(end-1).*(1 + Gamma_wf)./(1-Gamma_wf);
    % Propagete with new element
    [Vrp, ~] = propagate_diagonal(Z0X, Vrp, Vin(j));
end
Z0X = Z0X(2:end);
end
```

```
function [Vr, R] = propagate_diagonal(Z0X, Vrp, Vin)
n = length(Vrp)+1;
Vr = linspace(0, 0, n + 1);
Vl = linspace(0, 0, n + 1);
for i = n:-1:1
        if i == n
            [Vr(i), Vl(i)] = ...
                propagate_lattice(Z0X(i), Z0X(i+1), Vrp(i-1), 0);
        elseif i == 1
            [Vr(i), R] = ...
                propagate_lattice(Z0X(i), Z0X(i+1), Vin, Vl(i+1));
        else
            [Vr(i), Vl(i)] = ...
                propagate_lattice(Z0X(i), Z0X(i+1), Vrp(i-1), Vl(i+1));
        end
end
Vr = Vr(1:end-1);
end
```

```
function Gamma = calculateGamma(Z0X)
n = length(Z0X)-1;
Gamma = linspace(0, 0, n);
for i = 1:n
    Gamma(i) = (Z0X(i+1) - Z0X(i))./(Z0X(i+1) + Z0X(i));
end
end
```

A.1.3 Impedance reconstruction with stabilization

```
function Z0X = reconstruct_impedance_tdr_stable(Z00, R, Vin, Zmin)
n = length(R);
Z0X(1) = Z00;
i_wf = 1;
Vwf = Vin(i_wf);
Vrp = zeros(0);
for j = 1:n
    % Propagate assuming matched load
    Z0X(end+1) = Z0X(end);
    [~, R_m] = propagate_diagonal(Z0X, Vrp, Vin(j));
    % Calculate next Z0X
    Gamma = calculateGamma(Z0X);
    Gamma_wf = (R(j) - R_m)./(Vwf*prod(1-Gamma.^2));
    Z0X(end) = Z0X(end-1).*(1 + Gamma_wf)./(1-Gamma_wf);
    if abs(Z0X(end) - Z0X(end-1)) < Zmin
        Z0X(end) = Z0X(end-1);
    end
    % Propagate with new element
    [Vrp, ~] = propagate_diagonal(Z0X, Vrp, Vin(j));
end
Z0X = Z0X(2:end);
end
```

A.2 Several algorithms

A.2.1 Thru-only de-embedding algorithm

The next code is an implementation of the thru-only de-embedding algorithm used in this research

```
function [pad_sparameters, device_sparameter] = ...
    thru_only(thru_sparameters, measured_device_sparameters, method)

freq = thru_sparameters.Frequencies;

thru_abcd = abcdparameters(thru_sparameters);
thru_A = rfparam(thru_abcd, 'A');
thru_B = rfparam(thru_abcd, 'B');
thru_C = rfparam(thru_abcd, 'C');

measured_device_abcd = abcdparameters(measured_device_sparameters);
```

```
if nargin < 3
    if max(1 - abs(thru_A)) < 0.1
        if max(abs(thru_B)) < 0.1
            method = 'single-shunt';
        elseif max(abs(thru_C)) < 0.1
            method = 'single-series';
        else
            method = 'symmetric';
        end
    else
        method = 'symmetric';
    end
end

if strcmp(method, 'mangan')

    for itFreq = 1:length(freq)
        thru_inverse_abcd_parameters = inv(thru_abcd.Parameters(:, :,
            itFreq));
        H_abcd_parameters(:, :, itFreq) = ...
            measured_device_abcd.Parameters(:, :, itFreq)*...
            thru_inverse_abcd_parameters;
    end

    H_abcd = abcdparameters(H_abcd_parameters, freq);
    H_z = zparameters(H_abcd);
    H_swapped_z = swap_network(H_z);

    device_z_parameters = (H_z.Parameters + H_swapped_z.Parameters)./2;
    device_z = zparameters(device_z_parameters, freq);
    device_sparameter = sparameters(device_z);

    pad_sparameters = 0;

elseif strcmp(method, 'symmetric')

    pad_abcdparameters = thru_abcd;
    for itFreq = 1:length(freq)
        pad_abcdparameters.Parameters(:, :, itFreq) = ...
            sqrtm(thru_abcd.Parameters(:, :, itFreq));
    end
    pad_sparameters = sparameters(pad_abcdparameters);
    device_sparameter = ...
        remove_pad(pad_sparameters, measured_device_sparameters);

elseif strcmp(method, 'single-shunt')
```

```
    Y = thru_C./2;

    pad_A = ones(size(freq));
    pad_B = zeros(size(freq));
    pad_C = Y;
    pad_D = pad_A;

    pad_abcd_parameters = zeros(2, 2, length(freq));
    pad_abcd_parameters(1, 1, :) = pad_A;
    pad_abcd_parameters(1, 2, :) = pad_B;
    pad_abcd_parameters(2, 2, :) = pad_D;
    pad_abcd_parameters(2, 1, :) = pad_C;

    pad_abcd = abcdparameters(pad_abcd_parameters, freq);
    pad_sparameters = sparameter(pad_abcd);

    device_sparameter = ...
        remove_pad(pad_sparameters, measured_device_sparameters);

elseif strcmp(method, 'single-series')

    Z = thru_B./2;

    pad_A = ones(size(freq));
    pad_B = Z;
    pad_C = zeros(size(freq));
    pad_D = pad_A;

    pad_abcd_parameters = zeros(2, 2, length(freq));
    pad_abcd_parameters(1, 1, :) = pad_A;
    pad_abcd_parameters(1, 2, :) = pad_B;
    pad_abcd_parameters(2, 2, :) = pad_D;
    pad_abcd_parameters(2, 1, :) = pad_C;

    pad_abcd = abcdparameters(pad_abcd_parameters, freq);
    pad_sparameters = sparameter(pad_abcd);

    device_sparameter = ...
        remove_pad(pad_sparameters, measured_device_sparameters);

else
    warning('The method is not recognized')
end

end
```

```
function deembedded_sparameters = ...
    remove_pad(pad_sparameters, measurement_sparameter)

pad_abcd = abcdparameters(pad_sparameters);
pad_swaped_abcd = abcdparameters(swap_network(pad_sparameters));
measurement_abcd = abcdparameters(measurement_sparameter);

deembedded_abcd = measurement_abcd;
for itFreq = 1:length(deembedded_abcd.Frequencies)
    deembedded_abcd.Parameters(:, :, itFreq) = ...
        inv(pad_abcd.Parameters(:, :, itFreq))* ...
        measurement_abcd.Parameters(:, :, itFreq)* ...
        inv(pad_swaped_abcd.Parameters(:, :, itFreq));
end
deembedded_sparameters = sparameters(deembedded_abcd);
end
```

A.2.2 Characteristic impedance from long lines algorithm

```
function [freq, Z0, Gamma] =  ...
    calculate_TL_parameters(sparameters, L, method, n)

if nargin < 3
    method = 'standard';
    n = 2;
elseif nargin < 4
    n = 2;
end

freq = sparameters.Frequencies;

if strcmp(method, 'novel')

    ABCD = abcdparameters(sparameters);
    Line_A = rfparam(ABCD,'A');
    Line_B = rfparam(ABCD,'B');
    Line_C = rfparam(ABCD,'C');
    Line_D = rfparam(ABCD,'D');

    coshGammaL = (Line_A + Line_D)/2;
    sinhGammaL = ...
        abs(sqrt(Line_B.*Line_C)).*...
        exp(1i*(angle(Line_B.*Line_C))/2);
    expGammaL = coshGammaL + sinhGammaL;
```

```
    exp_alphaL = abs(expGammaL); % Forces alpha to be over 1
    exp_alphaL = unwrap_exp_alphaL(exp_alphaL);
    alphaL = log(exp_alphaL);
    betaL = unwrap_beta(angle(expGammaL));
    GammaL = alphaL + 1i*betaL;

    diff_Line_B = gradient(Line_B);
    diff_GammaL = gradient(GammaL);

    Z0sinhGammaL = Line_B;
    Z0coshGammaL = diff_Line_B./diff_GammaL;
    Z0expGammaL = (Z0sinhGammaL + Z0coshGammaL);
    MagZ0exp_alphaL = abs(Z0expGammaL);
    MagZ0 = MagZ0exp_alphaL./exp_alphaL;
    ArgZ0_plus_betaL = unwrap_beta(angle(Z0expGammaL));
    ArgZ0 = ArgZ0_plus_betaL - betaL;
    Z0 = MagZ0.*exp(1i*ArgZ0);

elseif strcmp(method, 'sqrt')

    Line_short = sqrt_sparameter(sparameters, n);

    ABCD = abcdparameters(Line_short);
    Line_A = rfparam(ABCD,'A');
    Line_B = rfparam(ABCD,'B');
    Line_C = rfparam(ABCD,'C');
    Line_D = rfparam(ABCD,'D');

    GammaL = acosh((Line_A + Line_D)/2);
    Z0 = sqrt(Line_B./Line_C);
    L = L/(2*n);
    alpha = real(GammaL)./L;
    beta = imag(GammaL)./L;
    Gamma = alpha + 1i*beta;

elseif strcmp(method, 'standard')

    ABCD = abcdparameters(sparameters);
    Line_A = rfparam(ABCD,'A');
    Line_B = rfparam(ABCD,'B');
    Line_C = rfparam(ABCD,'C');
    Line_D = rfparam(ABCD,'D');

    GammaL = acosh((Line_A + Line_D)/2);
    Z0 = sqrt(Line_B./Line_C);
```

```
    alpha = real(GammaL)./L;
    beta = imag(GammaL)./L;
    Gamma = alpha + 1i*beta;

end

end
```

```
function output = unwrap_exp_alphaL(input)

% Ensures first point is above 1
output = zeros(size(input));
diff_input = diff(input);
output(1) = 1 + abs(input(1) - 1);
good_diff = mean(diff_input(1:250));
for i = 2:length(output)-1
    output(i) = output(i - 1) + diff_input(i - 1);
    if output(i) < 1
        output(i) = output(i - 1) + good_diff;
        diff_input = -diff_input;
    end

end
end
```

```
function beta_unwrapped = unwrap_beta(beta_wrapped)

beta_unwrapped = beta_wrapped;
beta_unwrapped(1) = abs(beta_wrapped(1));
for i = 2:length(beta_wrapped)-1
    delta_beta(i-1) = abs(beta_wrapped(i) - beta_wrapped(i-1));
    mean_delta_beta = mean(delta_beta(1:i-1));
    std_dev_delta_beta = std(delta_beta(1:i-1));
    is_delta_beta_normal = ...
        delta_beta(i-1) < mean_delta_beta + 3*std_dev_delta_beta && ...
        delta_beta(i-1) > mean_delta_beta - 3*std_dev_delta_beta;
    if is_delta_beta_normal
        beta_unwrapped(i) = beta_unwrapped(i - 1) + delta_beta(i-1);
    else
        beta_unwrapped(i) = beta_unwrapped(i - 1) + mean_delta_beta;
        delta_beta(i-1) = mean_delta_beta;
    end
end
beta_unwrapped(end) = beta_unwrapped(end - 1) + mean_delta_beta;
```

```
end
```

A.2.3 Design of experiment for the vertical transition

```
# Create the experiment
VerticalTransition <-
  lhs.design(
    type = "optimum" ,
    nruns = 48 ,
    nfactors = 16
    ,
    digits = 2 ,
    seed = 19245 ,
    factor.names = list(
      TopCPW_Sig = c(0, 1),
      TopCPW_Gap =
        c(0, 1),
      TopCPW_Gnd = c(0, 1),
      TopRing_Catch = c(0, 1),
      TopRing_Gap = c(0, 1),
      TopRing_Gnd =
        c(0, 1),
      TopCoaxRadius = c(0, 1),
      Iris_Catch = c(0, 1),
      Iris_Gap = c(0, 1),
      BottCPW_Sig =
        c(0, 1),
      BottCPW_Gap = c(0, 1),
      BottCPW_Gnd = c(0, 1),
      BottRing_Catch = c(0, 1),
      BottRing_Gap = c(0, 1),
      BottRing_Gnd = c(0, 1),
      BottCoaxRadius = c(0, 1)
    )
  )
summary(VerticalTransition , brief = TRUE)
export.design(
  VerticalTransition,
  type = "all",
  path = "U:/Reference/R/VerticalTransition",
  file = "VerticalTransition",
  replace = TRUE
)
```

```
# Changing variable names to x1, x2, etc.
VerticalTransition.coded  <- code.design(VerticalTransition)

# Calculate the linear models
rsmModel_FO.15 <-
  rsm(X15.GHz ~ FO(x1, x2, x3, x4, x5, x6, x7, x8, x9, x10, x11, x12, x13,
                   x14, x15, x16),
      data = VerticalTransition.coded)
rsmModel_FO.30 <-
  rsm(X30.GHz ~ FO(x1, x2, x3, x4, x5, x6, x7, x8, x9, x10, x11, x12, x13,
                   x14, x15, x16),
      data = VerticalTransition.coded)
rsmModel_FO.37 <-
  rsm(X37.GHz ~ FO(x1, x2, x3, x4, x5, x6, x7, x8, x9, x10, x11, x12, x13,
                   x14, x15, x16),
      data = VerticalTransition.coded)

# Print the linear fit to identify more important 7 variables
summary(rsmModel_FO.15)
summary(rsmModel_FO.30)
summary(rsmModel_FO.37)

# Create a model including some two-way interactions
rsmModel.15 <-
  rsm(
    X15.GHz ~ FO(x1, x2, x3, x4, x5, x6, x7, x8, x9, x10, x11, x12, x13,
                 x14, x15, x16) + TWI(x3, x6, x7, x11, x13, x14, x16),
    data = VerticalTransition.coded
  )
rsmModel.30 <-
  rsm(
    X30.GHz ~ FO(x1, x2, x3, x4, x5, x6, x7, x8, x9, x10, x11, x12, x13,
                 x14, x15, x16) + TWI(x2, x3, x10, x11, x13, x14, x16),
    data = VerticalTransition.coded
  )
rsmModel.37 <-
  rsm(
    X37.GHz ~ FO(x1, x2, x3, x4, x5, x6, x7, x8, x9, x10, x11, x12, x13,
                 x14, x15, x16) + TWI(x6, x8, x9, x10, x11, x12, x16),
    data = VerticalTransition.coded
  )

# Print the summaries to indentify the main two-way interactions
summary(rsmModel.15)
summary(rsmModel.30)
summary(rsmModel.37)
```

```
# Ploting the main two-way interaction countours
contour(
  rsmModel.15,
  ~ x6 * x13,
  at = list(
    x1 = 0.5,
    x2 = 0.5,
    x3 = 0.5,
    x4 = 0.5,
    x5 = 0.5,
    x6 = 0.5,
    x7 = 0.5,
    x8 = 0.5,
    x9 = 0.5,
    x10 = 0.5,
    x11 = 0.5,
    x12 = 0.5,
    x13 = 0.5,
    x14 = 0.5,
    x15 = 0.5,
    x16 = 0.5
  )
)
contour(
  rsmModel.30,
  ~ x11 * x13,
  at = list(
    x1 = 0.5,
    x2 = 0.5,
    x3 = 0.5,
    x4 = 0.5,
    x5 = 0.5,
    x6 = 0.5,
    x7 = 0.5,
    x8 = 0.5,
    x9 = 0.5,
    x10 = 0.5,
    x11 = 0.5,
    x12 = 0.5,
    x13 = 0.5,
    x14 = 0.5,
    x15 = 0.5,
    x16 = 0.5
  )
)
```

```
contour(
  rsmModel.37,
  ~ x12 * x16,
  at = list(
    x1 = 0.5,
    x2 = 0.5,
    x3 = 0.5,
    x4 = 0.5,
    x5 = 0.5,
    x6 = 0.5,
    x7 = 0.5,
    x8 = 0.5,
    x9 = 0.5,
    x10 = 0.5,
    x11 = 0.5,
    x12 = 0.5,
    x13 = 0.5,
    x14 = 0.5,
    x15 = 0.5,
    x16 = 0.5
  )
)

#EOF
```

A.3 Import layout into 3D simulator

This section presents the scripts, developed during this research, to create the 3D electromagnetic models of the transition from the 2D layouts drawn in PICDraw.

A.3.1 Add custom substrate material

```
# The project and model should be already selected
oDesktop.RestoreWindow()
oProject = oDesktop.GetActiveProject()
oDesign = oProject.GetActiveDesign()
oEditor = oDesign.SetActiveEditor("3D Modeler")

# Defining the variables
sSubstrateMaterialName = "LCTT_Substrate"
sSubstrateEpsrName = "$SubstrateEpsr"
sSubstrateEpsr = "7.1"
sSubstrateTandName = "$SubstrateTand"
sSubstrateTand = "0.0015"
```

```
# Setting the model untis
oEditor.SetModelUnits(
    [
        "NAME:Units Parameter",
        "Units:=", "um",
        "Rescale:=", False
    ]
)

# Allow Material override
oDesign.SetDesignSettings(
    [
        "NAME:Design Settings Data",
        "Use Advanced DC Extrapolation:=", False,
        "Allow Material Override:=", True,
        "Calculate Lossy Dielectrics:=", False,
        "EnabledObjects:=", []
    ])

# The next variables need to be at the project, so they can be added
# to the material
oProject.ChangeProperty(
    [
        "NAME:AllTabs",
        [
            "NAME:ProjectVariableTab",
            [
                "NAME:PropServers",
                "ProjectVariables"
            ],
            [
                "NAME:NewProps",
                [
                    "NAME:" + sSubstrateEpsrName,
                    "PropType:=", "VariableProp",
                    "UserDef:=", True,
                    "Value:=", sSubstrateEpsr,
                    "Description:=", "Substrate permittivity"
                ]
            ]
        ],
        [
            "NAME:ProjectVariableTab",
            [
                "NAME:PropServers",
```

```
                "ProjectVariables"
            ],
            [
                "NAME:NewProps",
                [
                    "NAME:" + sSubstrateTandName,
                    "PropType:=", "VariableProp",
                    "UserDef:=", True,
                    "Value:=", sSubstrateTand,
                    "Description:=", "Substrate loss"
                ]
            ]
        ]
    ]
)

# Lets add the new materials
oDefinitionManager = oProject.GetDefinitionManager()

# Adding LTCC substrate to material list
oDefinitionManager.AddMaterial(
    [
        "NAME:" + sSubstrateMaterialName,
        "permittivity:=", sSubstrateEpsrName,
        "dielectric_loss_tangent:=", sSubstrateTandName
    ]
)

# Save the changes
oProject.Save()
```

A.3.2 Import layout

```
# The project and model should be already selected
oDesktop.RestoreWindow()
oProject = oDesktop.GetActiveProject()
oDesign = oProject.GetActiveDesign()
oEditor = oDesign.SetActiveEditor("3D Modeler")

# This is the path to the *.dxf file
sFilePath = "C:/Ansoft/PersonalLib/Scripts/SimpleVia/LTCC/SimpleVia.dxf"

# Setting the thickness and height
dScale = 0.000001
dV03_thickness = 127*dScale
```

```
dV03_height = 0
dC03T0_thickness = 8*dScale
dC03T0_height = dV03_height + dV03_thickness
dV02_thickness = 254*dScale
dV02_height = dV03_height + dV03_thickness
dC02T0_thickness = 8*dScale
dC02T0_height = dV02_height + dV02_thickness
dR02T0_thickness = 18*dScale
dR02T0_height = dV02_height + dV02_thickness
dV01_thickness = 254*dScale
dV01_height = dV02_height + dV02_thickness
dC01T0_thickness = 8*dScale
dC01T0_height = dV01_height + dV01_thickness
dV00_thickness = 127*dScale
dV00_height = dV01_height + dV01_thickness
dC00T0_thickness = 8*dScale
dC00T0_height = dV00_height + dV00_thickness
dR00T0_thickness = 18*dScale
dR00T0_height = dV00_height + dV00_thickness
dD00_thickness = dV00_height + dV00_thickness
dD00_height = 0
dD01_thickness = 500*dScale
dD01_height = dV00_height + dV00_thickness

# Defining the color of gold
sRGB_Gold = "gold"

# Calling the import function
oEditor.ImportDXF(
    [
        "NAME:options",
        "FileName:=", sFilePath,
        "Scale:=", dScale,
        "AutoDetectClosed:=", True,
        "SelfStitch:=", True,
        "DefeatureGeometry:=", False,
        "DefeatureDistance:=", 0,
        "RoundCoordinates:=", False,
        "RoundNumDigits:=", 4,
        "WritePolyWithWidthAsFilledPoly:=", False,
        "ImportMethod:=", 1,
        "2DSheetBodies:=", False,
        [
            "NAME:LayerInfo",
            [
                "NAME:0",
```

```
            "source:=", "0",
            "display_source:=", "0",
            "import:=", True,
            "dest:=", "0",
            "dest_selected:=", False,
            "layer_type:=", "signal"
        ],
        [
            "NAME:C00T0",
            "source:=", "C00T0",
            "display_source:=", "C00T0",
            "import:=", True,
            "dest:=", "C00T0",
            "dest_selected:=", False,
            "layer_type:=", "signal"
        ],
        [
            "NAME:C01T0",
            "source:=", "C01T0",
            "display_source:=", "C01T0",
            "import:=", True,
            "dest:=", "C01T0",
            "dest_selected:=", False,
            "layer_type:=", "signal"
        ],
        [
            "NAME:C02T0",
            "source:=", "C02T0",
            "display_source:=", "C02T0",
            "import:=", True,
            "dest:=", "C02T0",
            "dest_selected:=", False,
            "layer_type:=", "signal"
        ],
        [
            "NAME:C03T0",
            "source:=", "C03T0",
            "display_source:=", "C03T0",
            "import:=", True,
            "dest:=", "C03T0",
            "dest_selected:=", False,
            "layer_type:=", "signal"
        ],
        [
            "NAME:D00",
            "source:=", "D00",
```

```
            "display_source:=", "D00",
            "import:=", True,
            "dest:=", "D00",
            "dest_selected:=", False,
            "layer_type:=", "signal"
        ],
        [
            "NAME:D01",
            "source:=", "D01",
            "display_source:=", "D01",
            "import:=", True,
            "dest:=", "D01",
            "dest_selected:=", False,
            "layer_type:=", "signal"
        ],
        [
            "NAME:R00T0",
            "source:=", "R00T0",
            "display_source:=", "R00T0",
            "import:=", True,
            "dest:=", "R00T0",
            "dest_selected:=", False,
            "layer_type:=", "signal"
        ],
        [
            "NAME:R02T0",
            "source:=", "R02T0",
            "display_source:=", "R02T0",
            "import:=", True,
            "dest:=", "R02T0",
            "dest_selected:=", False,
            "layer_type:=", "signal"
        ],
        [
            "NAME:V00",
            "source:=", "V00",
            "display_source:=", "V00",
            "import:=", True,
            "dest:=", "V00",
            "dest_selected:=", False,
            "layer_type:=", "signal"
        ],
        [
            "NAME:V01",
            "source:=", "V01",
            "display_source:=", "V01",
```

```
            "import:=", True,
            "dest:=", "V01",
            "dest_selected:=", False,
            "layer_type:=", "signal"
        ],
        [
            "NAME:V02",
            "source:=", "V02",
            "display_source:=", "V02",
            "import:=", True,
            "dest:=", "V02",
            "dest_selected:=", False,
            "layer_type:=", "signal"
        ]
    ],
    [
        "NAME:TechFileLayers",
        "layer:=",
        [
            "SrcName:=", "V03",
            "DestName:=", "V03",
            "Thickness:=", dV03_thickness,
            "Elevation:=", dV03_height,
            "Color:=", sRGB_Gold
        ],
        "layer:=",
        [
            "SrcName:=", "C03T0",
            "DestName:=", "C03T0",
            "Thickness:=", dC03T0_thickness,
            "Elevation:=", dC03T0_height,
            "Color:=", sRGB_Gold
        ],
        "layer:=",
        [
            "SrcName:=", "V02",
            "DestName:=", "V02",
            "Thickness:=", dV02_thickness,
            "Elevation:=", dV02_height,
            "Color:=", sRGB_Gold
        ],
        "layer:=",
        [
            "SrcName:=", "C02T0",
            "DestName:=", "C02T0",
            "Thickness:=", dC02T0_thickness,
```

```
        "Elevation:=", dC02T0_height,
        "Color:=", sRGB_Gold
    ],
    "layer:=",
    [
        "SrcName:=", "R02T0",
        "DestName:=", "R02T0",
        "Thickness:=", dR02T0_thickness,
        "Elevation:=", dR02T0_height,
        "Color:=", sRGB_Gold
    ],
    "layer:=",
    [
        "SrcName:=", "V01",
        "DestName:=", "V01",
        "Thickness:=", dV01_thickness,
        "Elevation:=", dV01_height,
        "Color:=", sRGB_Gold
    ],
    "layer:=",
    [
        "SrcName:=", "C01T0",
        "DestName:=", "C01T0",
        "Thickness:=", dC01T0_thickness,
        "Elevation:=", dC01T0_height,
        "Color:=", sRGB_Gold
    ],
    "layer:=",
    [
        "SrcName:=", "V00",
        "DestName:=", "V00",
        "Thickness:=", dV00_thickness,
        "Elevation:=", dV00_height,
        "Color:=", sRGB_Gold
    ],
    "layer:=",
    [
        "SrcName:=", "C00T0",
        "DestName:=", "C00T0",
        "Thickness:=", dC00T0_thickness,
        "Elevation:=", dC00T0_height,
        "Color:=", sRGB_Gold
    ],
    "layer:=",
    [
        "SrcName:=", "R00T0",
```

```
                "DestName:=", "R00T0",
                "Thickness:=", dR00T0_thickness,
                "Elevation:=", dR00T0_height,
                "Color:=", sRGB_Gold
            ],
            "layer:=",
            [
                "SrcName:=", "D00",
                "DestName:=", "D00",
                "Thickness:=", dD00_thickness,
                "Elevation:=", dD00_height,
                "Color:=", "BlueViolet"
            ],
            "layer:=",
            [
                "SrcName:=", "D01",
                "DestName:=", "D01",
                "Thickness:=", dD01_thickness,
                "Elevation:=", dD01_height,
                "Color:=", "MidnightBlue"
            ]
        ]
    ])

# Assigning the materials
sSubstrateMaterialName = "LCTT_Substrate"

# Select all the CXXTXX elements
aCXXTXX = oEditor.GetMatchedObjectName("C*")
sCXXTXX = ",".join(aCXXTXX)

# Assign gold to all CXXTXX elements
oEditor.AssignMaterial(
    [
        "NAME:Selections",
        "Selections:=", sCXXTXX
    ],
    [
        "NAME:Attributes",
        "MaterialValue:=", "\"gold\"",
        "SolveInside:=", False
    ])

# Select all the VXX elements
aVXX = oEditor.GetMatchedObjectName("V*")
sVXX = ",".join(aVXX)
```

```
# Assign gold to all VXX elements
oEditor.AssignMaterial(
    [
        "NAME:Selections",
        "Selections:=", sVXX
    ],
    [
        "NAME:Attributes",
        "MaterialValue:=", "\"gold\"",
        "SolveInside:=", False
    ])

# Select all the D00 elements
aD00 = oEditor.GetMatchedObjectName("D00*")
sD00 = ",".join(aD00)

# Assign gold to all D00 elements
oEditor.AssignMaterial(
    [
        "NAME:Selections",
        "Selections:=", sD00
    ],
    [
        "NAME:Attributes",
        "MaterialValue:=", "\"" + sSubstrateMaterialName + "\"",
        "SolveInside:=", True
    ])

# Assign transparency to D00
oEditor.ChangeProperty(
    [
        "NAME:AllTabs",
        [
            "NAME:Geometry3DAttributeTab",
            [
                "NAME:PropServers",
                sD00
            ],
            [
                "NAME:ChangedProps",
                [
                    "NAME:Transparent",
                    "Value:=", 0.9
                ]
            ]
```

```
        ]
    ])

# Select all the D01 elements
aD01 = oEditor.GetMatchedObjectName("D01*")
sD01 = ",".join(aD01)

# Assign gold to all D01 elements
oEditor.AssignMaterial(
    [
        "NAME:Selections",
        "Selections:=", sD01
    ],
    [
        "NAME:Attributes",
        "MaterialValue:=", "\"air\"",
        "SolveInside:=", True
    ])

# Assign transparency to D01
oEditor.ChangeProperty(
    [
        "NAME:AllTabs",
        [
            "NAME:Geometry3DAttributeTab",
            [
                "NAME:PropServers",
                sD01
            ],
            [
                "NAME:ChangedProps",
                [
                    "NAME:Transparent",
                    "Value:=", 0.75
                ]
            ]
        ]
    ])

# Save the changes
oProject.Save()
```

This appendix listed some codes used in this research.

Appendix B
Literature review about vertical transitions

In Section 4.1.1, a summary of the vertical transitions found in the literature was provided, while this section provides case by case commenting on the vertical transitions in Table 4.1. The commenting is ordered in inverse chronological order. A few papers that are not listed in Table 4.1 are discussed here [1], [2]; these papers are not listed because they are not usable for our application but still show some interesting points.

In [3], a transition in low-temperature co-fired ceramic (LTCC) using a Dupont 9k7 substrate is presented. The transition is between a co-planar waveguide (CPW) and a stripline. The concept is based on removing the catch pads, and using transmission line ground vias, air cavities, and circular apertures in the backside ground. This transition presents the best microwave performance found in the literature and requires 4 layers of metallisation. The transition thickness is 110 µm and the total thickness is 432 µm. It does not provide cross-level cross-talk shielding, but does provide shielding to the substrate. The transition requires several non-standard features like metal widths below 100 µm, air cavities, 80 µm via diameters and 100 µm catch pads. The transition provides excellent microwave performance with a measured transition 3 dB bandwidth ($f_{3\,\mathrm{dB}}$) above 150 GHz, and a return loss below −10 dB up to 150 GHz.

In [4], a transition for LTCC using a Ferro A6M substrate is presented. The transition is between a microstrip and another microstrip. The concept is based on multiple ground apertures and catch-pads, and the use of a coaxial-like structure. The transition requires 7 layers of metallisation, a thickness of 600 µm, and a total thickness of 600 µm. This transition provides cross-level cross-talk shielding, but no shielding to the mounting substrate. The transition only requires standard features, has a measured transition $f_{3\,\mathrm{dB}}$ above 60 GHz, and a return loss below −10 dB up to 40 GHz. This paper also discusses the importance of having as many ground vias as possible around the signal via in the coaxial-like structure.

In [5], [6], a transition for LTCC using a Ferro A6M substrate is presented. The transition is between a conductor backed co-planar waveguide (CB-CPW) and a stripline using a coaxial-like structure. The transition requires 4 layers of metallisation, is 800 µm thick, and the total thickness of the substrate is 1120 µm. This transition does provide cross-level cross-talk shielding to the mounting substrate, and only requires standard features. The transition has a measured transition $f_{3\,\mathrm{dB}}$ of 30 GHz,

and a return loss below −10 dB up to 10 GHz. This work is also interesting because of the simple circuit model used to represent the transition, and because the paper confirms the importance of the use of ground vias to remove substrate modes.

In [7], [8], a transition for LTCC using an undisclosed substrate (probably Dupont 9K7 based on the relative permittivity (ϵ_r)) is presented. The transition is between a CPW and a surface mount pad, and it is based on staggered transitions. The transition requires 9 layers of metallisation, a transition thickness of 700 µm, and a total thickness of 700 µm. This transition provides cross-level cross-talk shielding to the mounting substrate. The transition requires non-standard features: such as features with a smaller size than 100 µm and dielectric cuts. The transition has a measured transition $f_{3\,\mathrm{dB}}$ above 20 GHz and a return loss below −10 dB up to 20 GHz.

In [9], a transition for liquid crystal polymer (LCP) is presented. The transition is between a CPW and a stripline with an intermediary microstrip. The transition requires 6 layers of metallisation, a transition thickness of 375 µm, and a total thickness of 450 µm. This transition provides cross-level cross-talk shielding to the mounting substrate and only requires standard features. The transition has a simulated transition $f_{3\,\mathrm{dB}}$ above 70 GHz and a return loss below −10 dB up to 70 GHz.

In [1], [2], a transition for LTCC is presented. The transition is between a pad and a stripline. The transition requires 2 layers of metallisation, a transition thickness of 416 µm and a total thickness of 832 µm. This transition does not provide cross-level cross-talk shielding but does provide shielding to the mounting substrate. The transition requires a non-standard feature, which is a nibbling technique to create a solid coaxial ground. The transition has a simulated transition $f_{3\,\mathrm{dB}}$ above 60 GHz and a return loss below −10 dB up to 45 GHz. This transition is not shown in the table because the transition is not between two planar waveguides. However, this work is interesting because it takes the idea of having many ground vias in the coaxial-like structure to the extreme, by replacing the ground vias by the solid coaxial ground at the expense of using non-standard features.

In [10], a transition for LCP is presented. The application is for a Land-Grid-Array (LGA) technology, so the transition is not a simple line to line transition. The transition requires 3 layers of metallisation, a transition thickness of 59 µm and a total thickness of 109 µm. This transition does not provide cross-level cross-talk shielding but does does provide shielding to the mounting substrate. The transition only requires standard features and has a simulated transition $f_{3\,\mathrm{dB}}$ of 60 GHz and a return loss below −10 dB up to 80 GHz.

In [11], a transition for LTCC with a Ferro A6M substrate is presented. The transition is between two boards based on coaxial like structures. The connection between the boards is analysed by using flip-chip or die-bonding. The transition requires 2 layers of metallisation, a transition thickness of 1 mm and a total thickness of 1 mm. This transition does not provide cross-level cross-talk shielding or shielding to the mounting substrate and only requires standard features. The transition has a simulated transition $f_{3\,\mathrm{dB}}$ above 11 GHz and a return loss below −10 dB up to 11 GHz. The transition was not characterised at higher frequencies. This paper also uses the idea of using time-domain reflectometry (TDR) to optimise the transitions.

In [12], a transition for LTCC using a Ferro A6M substrate is presented between a microstrip and a stripline. The transition requires 5 layers of metallisation, a transition thickness of 600 µm and a total thickness of 1200 µm. This transition provides cross-level cross-talk shielding, provides shielding to the mounting substrate and only requires standard features. The transition has a simulated transition $f_{3\,\mathrm{dB}}$ around 30 GHz and a return loss below −10 dB up to 40 GHz. This paper is also interesting because an asymmetric stripline is used to shorten the length of the transition, and also as an example of the importance of using the ground vias to shield against cross-talk and other parasitic features.

In [13], a transition for LTCC using a Ferro A6M substrate is presented. The transition is between a CB-CPW and a stripline based on stagger transitions and the use of stubs for compensation. The transition requires 5 layers of metallisation, a transition thickness of 300 µm and a total thickness of 500 µm. This transition provides cross-level cross-talk shielding and also provides shielding to the mounting substrate. The transition only requires standard features. However, it behaves as a band-pass filter, which is not desirable in our case and thus the $f_{3\,\mathrm{dB}}$ is not an applicable measurement.

In [14], a transition for LTCC using a Dupont 9K7 substrate is presented with a transition between a CB-CPW and a stripline based on a coaxial-like structure. This transition has one of the best performances, but it does not provide cross-level cross-talk shielding and uses non-standard features. The transition requires 3 layers of metallisation, a transition thickness of 127 µm and a total thickness of 254 µm. While this transition does not provide cross-level cross-talk shielding, it does provide shielding to the mounting substrate. The transition requires a non-standard feature, which is features smaller than 100 µm and has a simulated transition $f_{3\,\mathrm{dB}}$ of 100 GHz, and a return loss below −10 dB up to 100 GHz.

In [15], a transition for LTCC using a Dupont 951 substrate is presented between a CB-CPW and another CB-CPW at a different level. The transition requires 3 layers of metallisation, a thickness of 420 µm and a total thickness of 840 µm. This transition does not provide interlayer crosstalk shielding but it does provide shielding to the mounting substrate. The transition only requires standard features, but only simulated results were presented. The transition has $f_{3\,\mathrm{dB}}$ above 10 GHz and a return loss below −10 dB up to 10 GHz.

In [16], [17], a transition for LTCC is presented between a CB-CPW and another CB-CPW at a different level. Multiple transitions were simulated in these papers using several substrates. The following comments refer to a transition using substrate Dupont 951. The transition requires 4 layers of metallisation, a thickness of 600 µm and a total thickness of 600 µm. This transition does not provide cross-level cross-talk shielding, but it does provide shielding to the mounting substrate, and it only requires standard features. The transition has a simulated transition $f_{3\,\mathrm{dB}}$ above 45 GHz and a return loss below −10 dB up to 45 GHz. These papers also present simulations for a transition from a CB-CPW to a shielded multi-layer co-planar waveguide (SM-CPW), as the ones discussed in this research. But this was not using LTCC but rather for standard printed circuit board (PCB), and no measurements were completed. This is

the transition that is most similar to our transition, but our transition removes one substrate and metal layer making it simpler. The final transition showed measured $f_{3\,\mathrm{dB}}$ above 20 GHz and a return loss below −10 dB up to 20 GHz.

In [18], a transition for LTCC using an undisclosed substrate is presented between a flip-chip pad and a microstrip. The concept is a combination of the three-wire concept with a coaxial-like structure. The transition requires 5 layers of metallisation, a transition thickness of 400 µm and a total thickness of 560 µm. This transition provides cross-level cross-talk shielding, and also provide shielding to the mounting substrate. The transition only requires standard features. It has a measured transition $f_{3\,\mathrm{dB}}$ of 35 GHz and a return loss below −10 dB up to 45 GHz. This paper is also interesting because it shows the advantages of having as many ground vias as possible in the coaxial-like structure.

In [19], a transition for LTCC based on a Ferro A6M substrate is presented between a stripline and a microstrip. The concept is based on a coaxial-like structure, and the transition requires 6 layers of metallisation, a thickness of 600 µm and a total thickness of 800 µm. This transition provides cross-level cross-talk shielding, shielding to the mounting substrate, and only requires standard features. The transition has a measured transition $f_{3\,\mathrm{dB}}$ above 70 GHz and a return loss below −10 dB up to 25 GHz. This paper is also interesting because it shows the advantages of having as many ground vias a possible in the coaxial-like structure.

In [20], [21], a transition for LCP is presented between a CB-CPW and a microstrip. The general concept is based on adding gaps to the solid ground and a coaxial-like structure. The transition requires 2 layers of metallisation, a transition thickness of 100 µm and a total thickness of 100 µm. This transition does not provide cross-level cross-talk shielding or shielding to the mounting substrate, and only requires standard features. The transition has a measured transition $f_{3\,\mathrm{dB}}$ above 100 GHz and a return loss below −10 dB up to 100 GHz.

In [22], a transition for LCP is presented between a CB-CPW and an embedded CB-CPW. The transition is very simple, based on a three-wire structure. The transition requires 2 layers of metallisation, a transition thickness of 50 µm and a total thickness of 575 µm. This transition does not provide cross-level cross-talk shielding, but does provide shielding to the mounting substrate. However, it only requires standard features. The transition has a measured transition $f_{3\,\mathrm{dB}}$ above 40 GHz and a return loss below −10 dB up to 40 GHz.

In [23], a transition for LTCC is presented using an undisclosed substrate (probably Dupont 9K7 based on the reported ϵ_r) between a CPW and a stripline. The transition is based on staged transitions, replacing a long transition by several small transitions, and using air cavities. The transition requires 5 layers of metallisation, a transition thickness of 300 µm and a total thickness of 600 µm. This transition provides cross-level cross-talk shielding and shielding to the mounting substrate but requires non-standard features like air cavities. The transition was only measured between 50 GHz to 66 GHz. In this range, the insertion loss is around −2 dB and the return loss below is −10 dB.

In [24], a transition for LTCC using a Ferro A6M substrate is presented between a

CB-CPW and a CB-CPW, which is based on a slab-line. The transition has excellent performance and a small thickness, but it does not provide cross-level cross-talk shielding. The transition requires only 5 layers of metallisation, a transition thickness of 300 µm and a total thickness of 500 µm. This transition does not provide cross-level cross-talk shielding, but does provide shielding to the mounting substrate. The transition also requires non-standard features such as small catch-pads. It has a measured transition $f_{3\,\mathrm{dB}}$ of around 70 GHz and a return loss below −10 dB up to around 70 GHz.

In [25], several transitions for LTCC using a Ferro A6M substrate are presented. The transitions include a CB-CPW to CB-CPW transition, a CB-CPW to microstrip transition and a CB-CPW to stripline transition. These transitions require 4 layers of metallisation, while both the transition thickness and the total thickness vary from 400 µm to 800 µm respectively. However, the CB-CPW to stripline transition does not provide cross-level cross-talk shielding. Only the CB-CPW to stripline provides shielding to the mounting substrate. The transition from a CB-CPW to a stripline has excellent performance but requires non-standard features such as features smaller than 100 µm and no catch pads. The transitions show measured $f_{3\,\mathrm{dB}}$ around 60 GHz and a return loss below −10 dB up to 60 GHz. This paper is very interesting because of the use of the asymmetric stripline and an inductive slit to compensate for the high capacitance (low impedance) section.

In [26], three transitions for LTCC, two using a Ferro A6M substrate and one using Dupont 951 , are presented. The transition between a CB-CPW and a slotline is fabricated using a Ferro A6M substrate and the other between a microstrip and a slotline is fabricated using both substrates. The transition requires 4 layers of metallisation, a transition thickness from 500 µm to 600 µm, and a total thickness from 800 µm to 960 µm. These transitions provide cross-level cross-talk shielding and shielding to the mounting substrate, and they only requires standard features. The transition has a measured transition $f_{3\,\mathrm{dB}}$ around 50 GHz and a return loss below −10 dB up to 50 GHz. This paper is interesting because it shows that having a substrate with lower ϵ_r results in transitions with better performance. The second interesting point of this paper is the use of a rectangular catch-pad for the signal via. The dimension of the rectangular catch-pad seems to have a large impact on the transition performance. The paper does not explain the reasons, but a possible explanation is that the corners of the catch-pad produce an inductance capable of compensating for the high capacitance in the transition.

In [27], a transition for LTCC using a Ferro A6M substrate is presented between a CB-CPW and a stripline. The transition is done using only the ground vias of the transmission lines. It requires 5 layers of metallisation, a transition thickness of 500 µm and a total thickness of 800 µm. This transition does not provide cross-level cross-talk shielding but does provide shielding to the mounting substrate. It requires non-standard features, such as missing catch pads in intermediate layers. The transition has a measured transition $f_{3\,\mathrm{dB}}$ around 45 GHz and a return loss below −10 dB up to around 40 GHz.

In [28], a transition for LTCC using a Dupont 951 substrate is presented between a

microstrip and a microstrip, and it is based on two ground apertures. The transition requires 11 layers of metallisation, a transition thickness of 550 µm and the same total thickness. This transition provides cross-level cross-talk shielding, but does not provides shielding to the mounting substrate. It only requires standard features. The transition has a measured transition $f_{3\,\mathrm{dB}}$ around 40 GHz and a return loss below −10 dB up to 35 GHz.

In [29], a transition for LTCC in an undisclosed substrate is presented. The transition is between a microstrip and a stripline based on a coaxial-like structure. The transition requires 5 layers of metallisation, the transition thickness is 500 µm and the total thickness is 750 µm. This transition provides cross-level cross-talk shielding and provides shielding to the mounting substrate. The transition does not require non-standard features. The paper does not provide the measured $f_{3\,\mathrm{dB}}$ and the measured return loss is below −10 dB up to 30 GHz.

In [30], a transition for LTCC using a Ferro A6M substrate is presented between a CPW and a CPW using a three-wire configuration. The transition requires 2 layers of metallisation, a transition thickness of 300 µm and the same total thickness. This transition does not provide cross-level cross-talk shielding or shielding to the mounting substrate. It also only requires standard features. The measured $f_{3\,\mathrm{dB}}$ is above 25 GHz and the measured return loss is below −10 dB up to above 25 GHz.

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