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Title	A compact microwave rectifier for wireless power transfer and energy harvesting applications
Authors	Moloudian, Gholamhosein;Kumar, Sanjeev;O'Flynn, Brendan;Buckley, John L.
Publication date	2024-04-26
Original Citation	Moloudian, G., Kumar, S., O'Flynn, B. and Buckley, J. L. (2024) 'A compact microwave rectifier for wireless power transfer and energy harvesting applications', 2024 18th European Conference on Antennas and Propagation (EuCAP), Glasgow, United Kingdom, 17-22 March 2024, pp. 1-4. https://doi.org/10.23919/EuCAP60739.2024.10501088
Type of publication	Conference item
Link to publisher's version	10.23919/EuCAP60739.2024.10501088
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A Compact Microwave Rectifier for Wireless Power Transfer and Energy Harvesting Applications

Gholamhosein Moloudain*, Sanjeev Kumar, Brendan O'Flynn and John L. Buckley
Tyndall National Institute, University College Cork, Cork, T12R5CP, Ireland.
gh.moloudian@tyndall.ie

***Abstract*—This paper presents a microwave rectifier with compact size and high efficiency for radio frequency (RF) energy harvesting and low-power internet of things (IoT) applications. The proposed rectifier consists of a matching network, a doubler rectifier, a lowpass (LPF) structure and a low-power electronic circuit. An LPF structure is employed to pass a direct current (DC) rectified signal and to control harmonics which increases the output voltage ($V_{\mathrm{OUT-DC}}$) as well as power conversion efficiency (PCE). The proposed rectifier is designed to operate at f = 1.8 GHz which shows a maximum PCE of 62% for an RF input power (P_{IN}) level of 8 dBm and optimum load (R_{L}) of 820 Ω. A DC-DC boost converter and a super capacitor (C_{OUT} = 370 μF) is employed to deliver sufficient DC voltage to power a low-power electronic circuit. The proposed rectifier is demonstrated to be capable of powering a low-power circuit at varying P_{IN} levels. The developed rectifier can be used in RF energy harvesting and wireless power transmission systems to power sensor nodes and IoT devices.**

***Index Terms*—Energy Harvesting, Lowpass (LPF) harmonic structures, Radio Frequency (RF), Rectifier.**

I. Introduction

Recently, the demand for self-powered sensor nodes and low-power internet of things (IoT) devices has significantly increased. Energy harvesting and wireless power transfer are promising methods to provide sufficient direct current (DC) power for next generation of low-power electronic circuits and IoT devices [1], [2], [3]. At the heart of energy harvesting and wireless power charging systems, rectifying-antenna (rectenna) play a key role in harvesting radio frequency (RF) signals and converting them to DC power. A rectenna circuit is comprised of an antenna and a rectifier circuit [4]. The antenna is one of the primary building block components in rectenna circuits and is used to harvest/receive and transfer RF signals [5], [6]. The rectifier block has a similarly important role in energy harvesting and wireless power transfer systems as it is used to convert captured RF signals to DC power. The rectifiers are non-linear electronic circuits which generate several high-order unwanted harmonics during the rectification process [7]. These harmonics lead to a power dissipation in the diode rectifiers which impact on RF-to-DC power conversion efficiency (PCE). These harmonics should be controlled to increase PCE and DC output voltage ($V_{\mathrm{OUT-DC}}$) [7].

In recent years, several techniques have been employed to control these harmonics such as lowpass (LPF) structures [4], [7], [8], [9], [10], [11], [12], harmonic termination techniques in Class-F [13], [14], [15], [16], Class-F^{-1} [17], [18], and harmonic recycling methods [19]. These harmonic controlling methods manipulate the current and voltage waveforms of the rectifier diodes to reduce the overlap between them to reduce diode power consumption. According to the state of the art, in general the designed rectifier circuits requires an RF input power $P_{\mathrm{IN}} > 10$ dBm to meet the maximum PCE, however, providing this level of power is still a challenge in practical RF energy harvesting circuits.

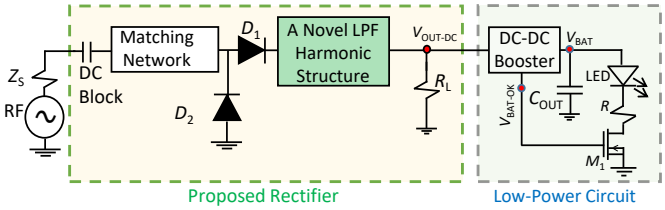


Fig. 1. Proposed topology for powering a low-power circuit.

This paper presents a compact microwave rectifier with high efficiency (PCE $> 40\%$) for a wide RF input range -1 dBm $< P_{\mathrm{IN}} <$ 16 dBm for use in RF energy harvesting and wireless power charging applications. Fig. 1 depicts the proposed modified rectifier for powering a low-power electronic circuit. To provide a concise overview of the primary aspects of the contributions, we can outline the key innovations of the proposed research as follows:

- The proposed rectifier employs a novel LPF structure to pass the DC frequency signal and suppress/control other harmonics up to 3^{rd} harmonics. The proposed LPF structure increases the DC Voltage signal which causes an improvement in PCE and as well as rectifier erformance. In contrast to the literature [4], [8], [9], [11], [12], [13], [15], [17], [18], [19], the proposed rectifier design demonstrates a desirable performance; PCE $> 40\%$ for a wide range of P_{IN} levels (-1 dBm $< P_{\mathrm{IN}} <$ 16 dBm).
- To validate rectifier performance a practical demonstration of its capabilities to power a low-power circuit and IoT devices, a DC-DC boost converter, a supercapacitor, a low-power electronic circuit are connected to the proposed rectifier is proposed. In contrast with the state of the art [4], [8], [9], [11], [12], [13], [15], [17], [18], [19] which powered a resistor, here in this case the authors propose to power up a low-power electronic circuit (light emitting diode, LED) to demonstrate the systems capability for powering more realistic low-power

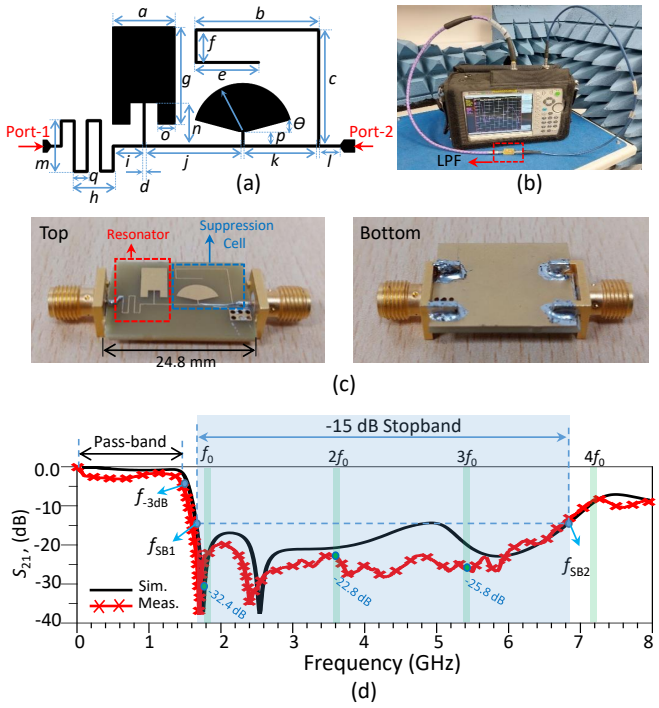


Fig. 2. Proposed LPF structure. (a) Topology/Layout. (b) Measurement setup. (c) Fabricated sample (Top and Bottom views). (d) Simulated and measured results. Dimensions: a = 5, b = 9.96, c = 9.2, d = 0.2, e = 5.2, f = 2.4, g = 7.75, h = 3.3, i = 2.26, j = 7.65, k = 5.8, l = 1.6, m = 4.2, n = 3.3, o = 1.4, p = 1, q = 1.2; (all in mm) and $\theta = \pi/12$. The total PCB size for the LPF structure: 24.8×11.6 mm^2.

circuits and modules such as wireless sensor nodes and IoT devices.

The rest of this paper is organized as follows. In Section II, an LPF structure and the rectifier circuit are designed, simulated, manufactured and measured. A low-power electronic circuit is powered in Section III to demonstrate the validation of the rectifier performance. Finally, Section IV concludes this paper.

II. Rectifier Design

The proposed rectifier consists of a matching network, a doubler rectifier, and an LPF structure. The proposed circuit is designed and fabricated on a low-cost FR4 substrate with a thickness of H = 1.6 mm, a dielectric constant ϵr = 4.4, loss tan(δ) = 0.02 and 35 μm cladding of copper.

1) LPF Structure Design: The LPF structure is shown in Fig. 2(a), which consists of an LPF resonator and a suppression harmonic cell. First, a third-order LPF resonator is designed based on the theoretical guidance provided in [20] which then is modified to achieve a sharper response and optimised resonance for use in an LPF structure. This modification manipulates the current surface distribution of the third-order LPF resonator which provides an improvement in the resonator performance [10]. To improve the stopband bandwidth of the LPF resonator, a suppression cell is employed which is encompassed by an open-end stub and a semi-radial stub. A photograph of the measurement setup for measuring insertion

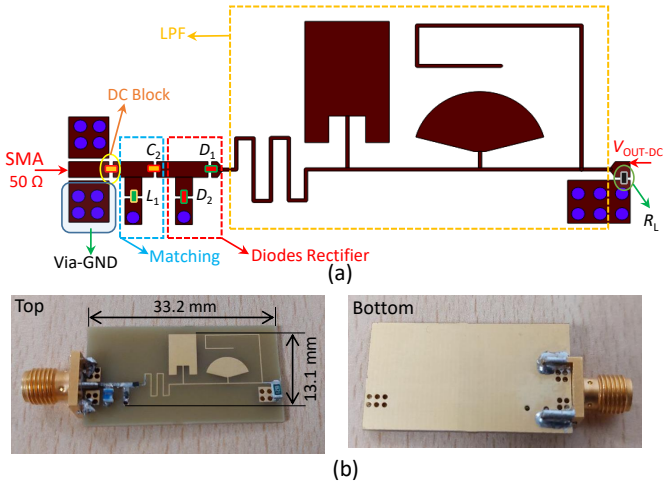


Fig. 3. Proposed rectifier circuit. (a) Topology/Layout. (b) Fabricated sample (Top and Bottom views). The total PCB size for the proposed rectifer: 33.2×13.1 mm^2. Components: Diodes = SMS7630 from Skyworks, R_L = 820 Ω package 0805 from Welwyn, L_1 = 13 nH package 0805 form Coilcraft, DC Block = 100 pF packaage 0402 from JANSON and C_2 = 47 pF packaage 0402 from JANSON.

loss (S_{21}) is shown in Fig. 2(b), and a photograph of the fabricated prototype of LPF structure are shown in Fig. 2(c). According to Fig. 2(d), the proposed LPF structure has a -3dB cut-off frequency at $f_{-3\text{dB}}$ = 1.52 GHz. The proposed LPF structure depicts a wide stopband bandwidth; from f_{SB1} = 1.65 GHz to f_{SB2} = 6.82 GHz. As the proposed rectifier is designed to operate at 1.8 GHz, the fundamental frequency (f_0 = 1.8 GHz) and the 2^{nd} and 3^{rd} harmonics ($2f_0$ and $3f_0$) are located in the stopband region that these harmonics are controlled/suppressed. Good agreement between the simulated and measured results for the proposed LPF structure is demonstrated. In the following subsection, the proposed LPF structure will be employed into a rectifier circuit to pass DC signal and control harmonics (f_0, $2f_0$ and $3f_0$).

2) Matching Network and Rectifier: As shown in Fig. 3, an impedance matching network at fundamental frequency (f_0 = 1.8 GHz) is employed to transfer maximum RF power from the antenna to the rectifier circuit. The proposed rectifier employs two Schottky diodes (SMS7630) as a doubler rectifier topology to convert RF power to DC voltage. The layout/topology and the fabricated prototype for the proposed rectifier circuit are shown in Fig. 3(b). As shown in the inset of Fig.4, the

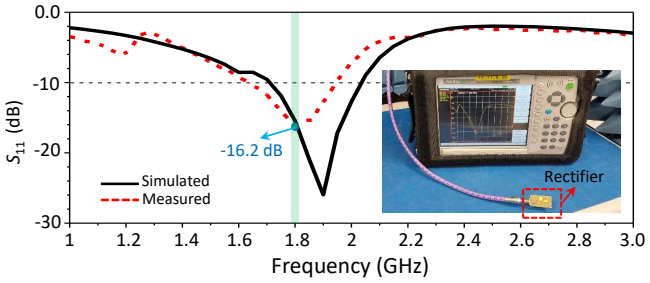


Fig. 4. Simulated and measured S_{11} response for the proposed rectifier at P_{IN} = 0 dBm at 1.8 GHz.

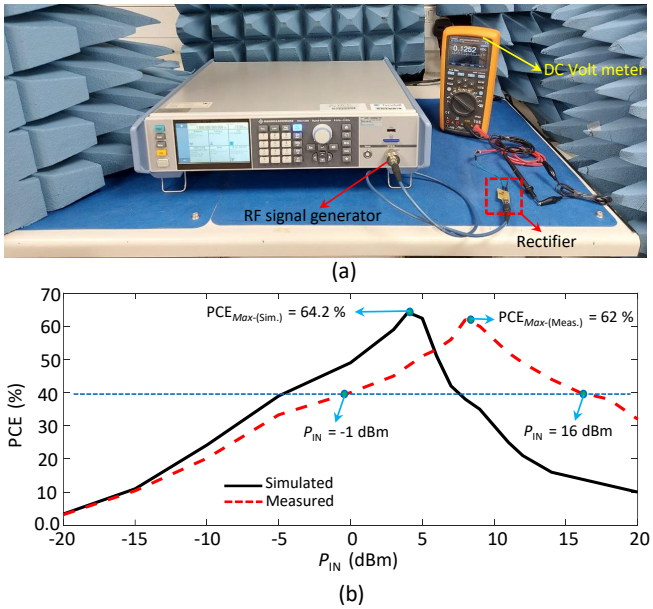


Fig. 5. (a) A photo of the experimental setup. (b) Simulated and measured PCE results at 1.8 GHz for varying P_{IN} levels for the proposed rectifier at optimum load; R_{L} = 820 Ω.

rectifier prototype is connected to an Anritsu MS2038C Vector Network Analyser (VNA) to measure reflection coefficient (S_{11}) parameter. Fig. 4 shows the simulated and measured S_{11} response at P_{IN} = 0 dBm (default P_{IN} levels for the VNA). The proposed rectifier shows a measured S_{11} better than -16 dB at f_0 = 1.8 GHz.

The experimental setup for measuring rectifier parameters such as PCE and $V_{\mathrm{OUT-DC}}$ is depicted in Fig. 5(a), where an RF signal generator is connected to the rectifier circuit to provide RF power with varying P_{IN} levels (-20 dBm < P_{IN} < +20 dBm). Moreover, a DC Volt-meter is employed to measure output DC voltage across R_{L}. According to the obtained results shown in Fig. 5(b), the proposed rectifier shows a maximum measured PCE of 62% at P_{IN} = 8 dBm for an optimum R_{L} = 820 Ω. The proposed rectifier demonstrates a high efficiency (PCE > 40%) for a wide RF input range -1 dBm < P_{IN} < 16 dBm for use in wireless power charging applications. In the next step, a low-power electronic circuit will be powered by the proposed circuit.

• III. Powering a Low-Power Circuit

To validate the rectifier performance, a DC-DC boost converter (BQ25504) from Texas Instrument inc. [21], and a supercapacitor (C_{OUT} = 370 μF) is employed to deliver sufficient DC voltage to power a low-power electronic circuit. The supercapacitor is implemented by two capacitors (C_1 and C_2); C_1 = 100 μF is the internal capacitance which is located inside of the DC-DC evaluation board and C_2 = 270 μF is an external capacitor. The low-power circuit consists of an NMOS transistor (M_1), a resistor and a light emitting diode (LED). Resistance R = 270 Ω is connected in series with the LED as a ballast resistor to limit the LED current in the forward bias. The NMOS transistor is employed to manage

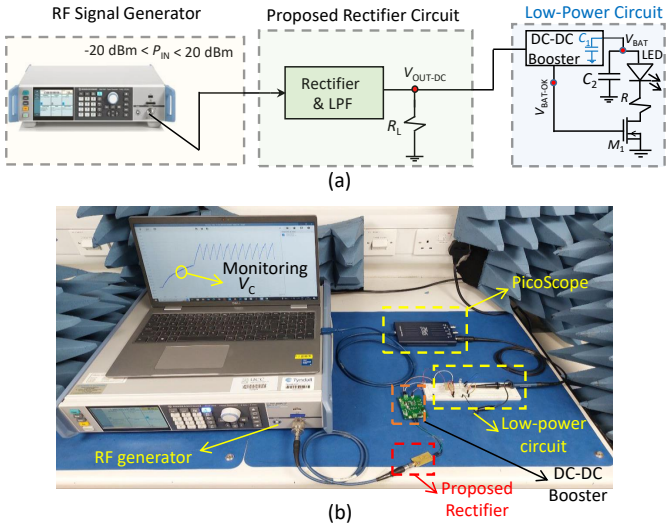


Fig. 6. (a) Proposed block diagram for powering the low-power circuit. (b) A photo of experimental setup. Equipment: RF Signal generator: RF signal generator: ROHDE & SCHWARZ SMA-100B up to 6 GHz, Transistor M_1: BSH105 N-channel MOSFET, R = 270 Ω, C_1 = 100 μF, C_2 = 270 μF and DAQ-PicoScope: PC-USB oscilloscope.

discharge time and create a discharge path during the discharge of C_{OUT}. The block diagram and a photo of experimental setup for powering the low-power circuit are depicted in Fig. 6. The voltage across the supercapacitor (V_{C}) and R = 270 Ω (V_{R}) were measured by the DAQ-PicoScope. According to Fig. 7, the V_{C} is measured for different P_{IN} levels (P_{IN} = -1 dBm and +2 dBm). First, the BQ25504 needs a cold-start time to reach at 1.51 (V_{COLD}), then it enters the charging mode, where it goes from V_{COLD} to V_{MAX}. When V_{MAX} is reached, a signal is sent from $V_{\mathrm{BAT-OK}}$ which can drive the NMOS gate. After driving the NMOS gate, the NMOS = "ON" which provides a path for discharging the C_{OUT} to the LED. During the discharging process, when the V_{C} meets the V_{MIN}, the booster goes back to the charging mode. In this work, the V_{MAX}, V_{MIN} and V_{COLD} are designed at 2.84, 1.82 and

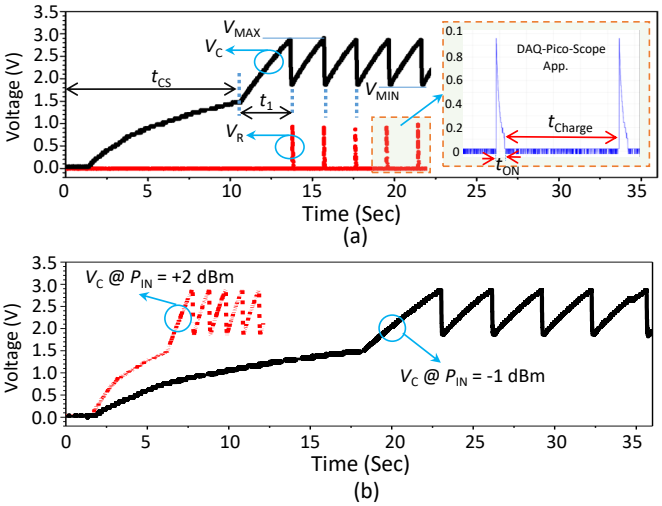


Fig. 7. (a) Measured results for V_{C} and V_{R} at P_{IN} = 0 dBm. (b) Measured V_{C} results for different P_{IN} levels (P_{IN} = -1 dBm and P_{IN} = +2 dBm).

1.51 (V). According to the obtained results (Fig. 7(b)), it can be seen that by increasing the P_{IN} level, the DC-DC booster needs a shorter cold-start time (t_{CS}) to rise from 0 to 1.51 (V). According to Fig. 7(a), when the V_{C} reaches at V_{MAX}, the supercapacitor discharges into R = 270 Ω and powers on the LED. A photo of the DAQ-PicoScope application is included in Fig. 7(a), where the discharge time (t_{ON}) and duty cycle (t_{ON} + t_{Charge}) are shown. The measured t_{ON}, t_{Charge} and duty cycle are 70 ms, 1836 ms and 1906 ms, respectively, for P_{IN} = 0 dBm. The proposed system demonstrated a desirable performance for powering a low-power electronic circuit, in this case an LED at different P_{IN} levels.

IV. Conclusion

In this paper, a rectifier circuit with a novel LPF structure was designed for use in wireless power transfer and energy harvesting applications. The LPF structure was employed in the rectifier circuit to control/suppress harmonics (f_0, $2f_0$, and $3f_0$) to increase the PCE. The proposed rectifier illustrated a maximum measured PCE of 62% at P_{IN} = 8 dBm for an optimum load of R_{L} = 820 Ω at 1.8 GHz. The rectifier demonstrated a desirable efficiency (PCE $>$ 40%) for a wide RF input range -1 dBm $< P_{\mathrm{IN}} <$ 16 dBm which is suitable for use in wireless power transfer applications. The proposed system successfully demonstrated desirable performance for powering an LED for different P_{IN} levels. The presented modified rectifier can be considered for use in low-power energy harvesting and wireless power transfer applications to power IoT devices and sensor nodes.

Acknowledgment

This work was supported in part by the European Union's Horizon 2020 Research and Innovation Programme through the Marie Skłodowska-Curie Grant Agreement by the Smart Manufacturing Advanced Research Training for Industry 4.0 (SMART 4.0) under Grant 847577, and in part by the Research Grant from the Science Foundation Ireland (SFI) through the Ireland's European Structural and Investment Funds Programme and the European Regional Development Fund 2014–2020 under Grant 16/RC/3918 (CONFIRM). Aspects of this work was supported by the CONNECT Centre for Future Networks and Communications (13/RC/2077).

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