Design of an adjustable bias circuit using a single-sided CMOS supply for avalanche photodiodes

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***Abstract*— A charge pump circuit operating from a single-sided CMOS supply, capable of biasing avalanche photodiodes up to 40 V with load currents in the mA range is presented. This circuit introduces new design elements that overcome previously published limitations. These elements include pass-gate voltage regulators and a mechanism for linking the negative voltage regulator to the positive voltage output. This design allows linear adjustment of the output voltage from a single control voltage. The circuit has compact dimensions of 1.55 mm × 1 mm, including bond pads, which makes it suitable for hybrid integration in a single package with an APD and two surface-mount capacitors.**

I. INTRODUCTION

Avalanche photodiodes are used in a wide range of lowlight sensing applications including astronomy [1], DNA sequencing [2], light detection and ranging (LIDAR) [3] and medical sensing [4]. Planar avalanche photodiodes (APDs) have been developed over a number of years that typically require bias voltages above 25 V [5], [6]. An integrable bias solution for these avalanche photodiodes was previously introduced in [7]. That circuit included a dual-rail charge pump to provide the high bias voltage and two shunt regulators to control the positive and negative outputs of the bias. The circuit is capable of sourcing mA range load currents for shallow-junction planar APDs that operate up to 40 V. There are several drawbacks to this circuit approach. Firstly, two control voltages require adjusting by the end user to provide the required output voltage. Secondly, since the current divider in the shunt regulator is under high potential, a high-voltage process is required to ensure the stability of the circuit's operation, thereby adding cost to the chip fabrication process. Finally, a negative supply rail is needed to control the negative output, which adds to the complexity of the circuit.

An alternative design that simplifies the voltage control, removes the need for a dual-rail supply, and reduces the overall circuit process cost is presented in this paper. This bias circuit overcomes the drawbacks of the circuit described in [7] while giving comparable performance. In this circuit, pass-gate based voltage regulators replace the shunt regulators thus reducing the maximum voltage for all the transistors in the circuit to Vdd. As a consequence, a high-voltage process is no longer required. Moreover, the negative voltage regulator is now linked to the positive output, which links the bias voltage to the reference voltage of the positive voltage regulator. This simplifies the overall control of the bias voltage and eliminates the need for a negative voltage rail in the circuit. The layout of the circuit was designed using the L-Foundry 0.15 µm process and the final design has a small footprint of 1.55 mm × 1 mm.

II. CIRCUIT DESCRIPTION

Fig. 1 shows the schematic of the bias circuit which consists of: (i) Positive and negative charge pumps to provide the high bias voltage for the APD. (ii) Positive and negative voltage regulators that control the voltage of the positive and negative output.

A. Positive and Negative Charge Pumps

The positive and negative charge pumps used in Fig. 1 are Dickson pump circuits [8]. The diodes in the circuit are used to transfer the charge and inverters are used to invert the phase of the input clocks. The neighboring pumping capacitors are connected to the two inverse clocks. Through every stage, the positive charge is transferred to the positive output and transferred away from the negative output [9]. At the output, a higher potential exceeding the magnitude of the system supply is obtained.

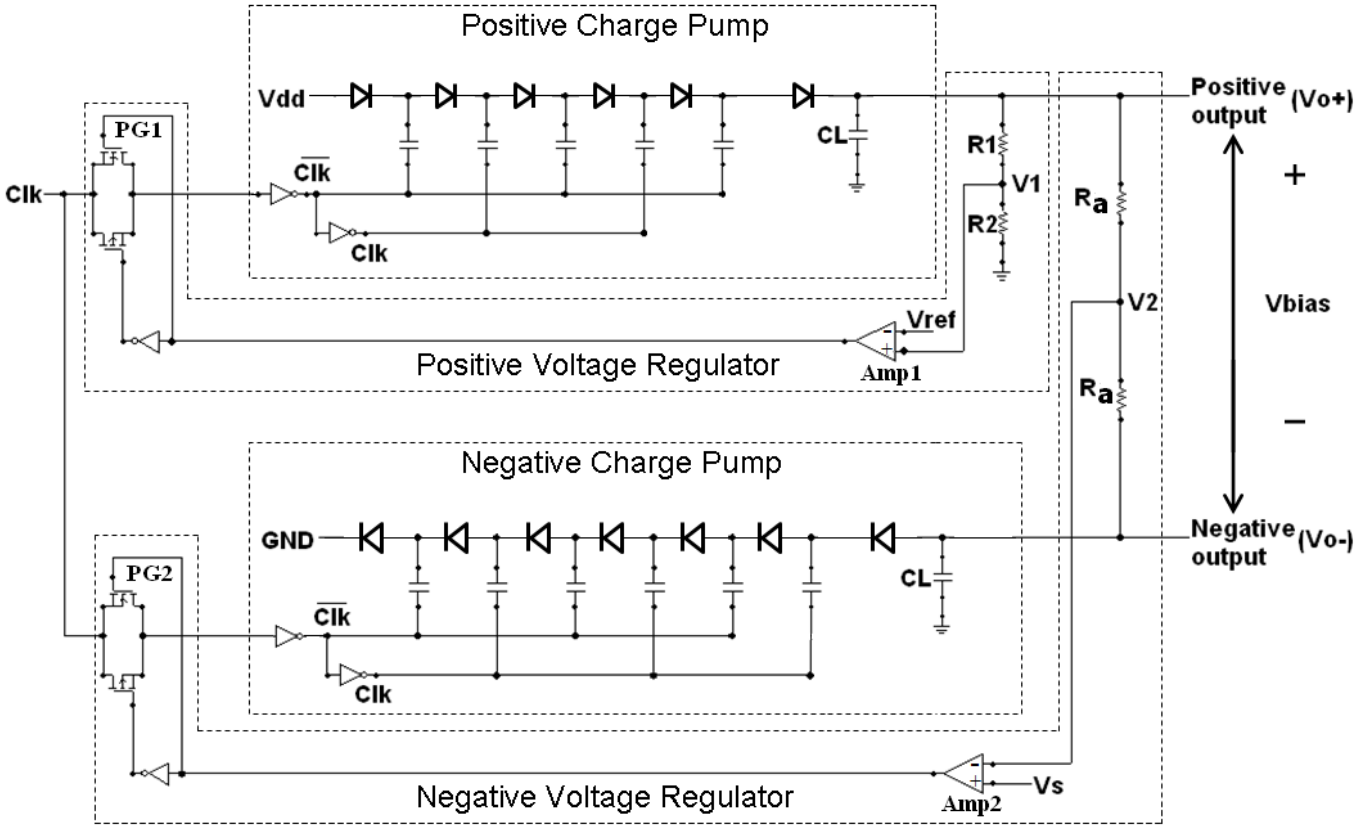

Fig. 1 Schematic of the bias circuit

B. Pass-gate based voltage regulators

The schematics of the positive and negative voltage regulators are shown in Fig. 1. Pass-gates (PG1 and PG2) are connected between the input clocks and the charge pumps and controlled by the output of the operational amplifiers (Amp1 and Amp2). R1, R2 and Ra are potential dividers used to limit the input voltage range at nodes V1 and V2. V1 is connected to the non-inverting input (+) of Amp1 and V2 is connected to the inverting input (-) of Amp2. For regulation of the positive output, if V1 exceeds the regulation level, Vref, the amplifier Amp1 generates an output voltage proportional to the difference between Vref and V1. The pass-gate PG1 is turned off to block the input clocks and the positive output is decreased. If the output falls below the regulation level, the pass-gate will be turned on and the output can be charged up. In this way, V1 can be set equal to Vref and the positive output voltage can be altered and Vo+ can be calculated using

$$V_{o+} = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \tag{1}$$

For regulation of the negative output, if V2 is less than the setting voltage, Vs, the amplifier Amp2 generates an output voltage proportional to the difference between Vs and V2. The pass-gate PG2 is turned off to block the input clocks to the negative charge pump, the amplitude of the negative output is decreased and V2 is increased. If V2 exceeds Vs, the pass-gate PG2 will be turned on, the amplitude of the negative output can be charged up and V2 will be decreased. In this way, V2 can be set equal to Vs and Vo- can be calculated using

$$V_{o-} = 2V_s - V_{o+} \tag{2}$$

The bias voltage V_{bias} is the difference between Vo+ and Vo-

$$V_{bias} = V_{o+} - V_{o-} \tag{3}$$

Replace Vo+ and Vo- using (1) and (2), gives

$$V_{bias} = 2V_{ref} \times \left(1 + \frac{R1}{R2}\right) - 2V_S \tag{4}$$

As can be seen from (4), when Vs is set to a constant voltage, the bias voltage of the circuit can be regulated linearly by setting the reference voltage Vref.

III. LAYOUT AND SIMULATIONS

The completed circuit layout is shown in Fig. 2. A 5-stage positive charge pump and a 6-stage negative charge pump are used. The pumping capacitors are set to 20 pF. Except for the 2 load capacitors, all the other components of the circuit are implemented on the chip. All the simulations reported are post-layout simulations.

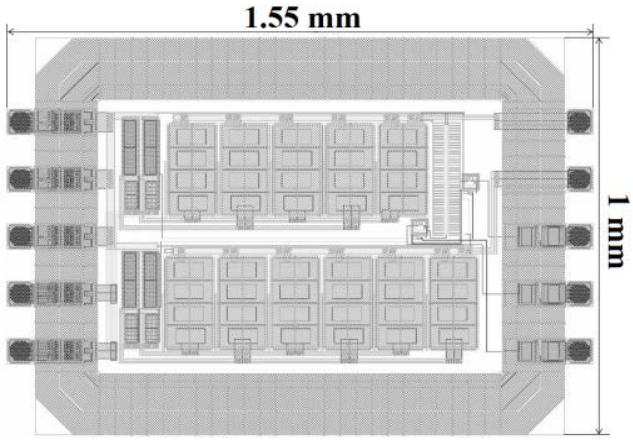

Fig. 2 Layout of the proposed circuit

For the simulations, the two load capacitors, set to 5 nF each, are the only external components of the circuit. The simulations were completed in the Cadence design environment. The clock frequency is 50 MHz with Vdd = Vclk = 5 V.

Fig. 3 shows the maximum load current and output power for different bias voltages. It is clear that the circuit is capable of meeting load current demands in excess of 1 mA for bias voltages up to 40 V.

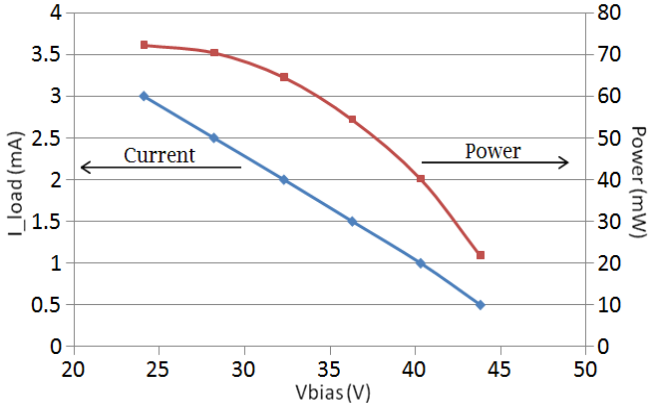

Fig. 3 Simulation results of maximum load current and output power for different bias voltages

Fig. 4 shows the Positive and negative output when the bias voltage is regulated to 30 V. Here the Vs is set to 1 V that makes the negative output voltage equals to (2 V - Positive output). As can be seen from the figure, with the voltage regulators, the bias voltage is precisely set to 30 V.

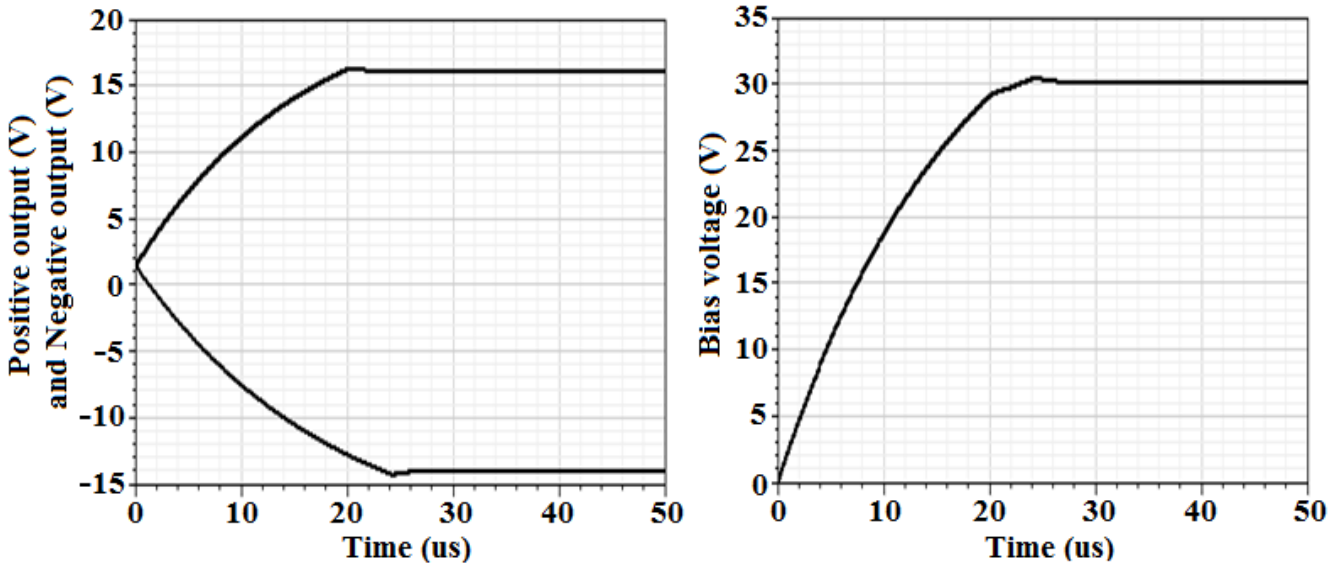

Fig. 4 Positive and negative output when the bias voltage is regulated to 30 V

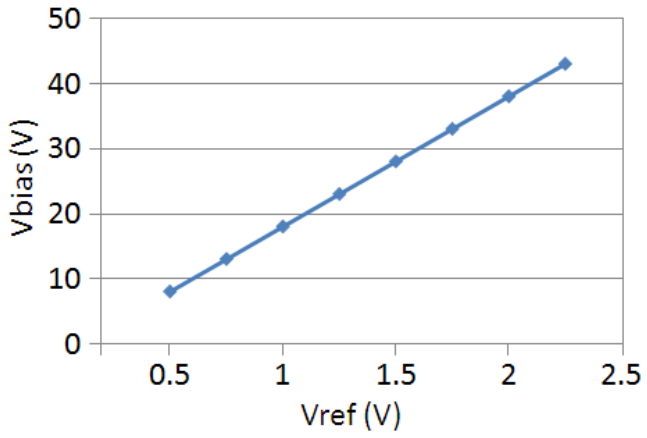

Fig. 5 Bias voltage adjustments for different Vref

Fig. 5 demonstrates the bias voltage adjustments for different reference voltages (R1/R2 is set to 9/1 and Vs is set to 1 V). Simulations show that the bias voltage can be accurately and linearly regulated with a peak-peak ripple of less than 40 mV using a single control voltage.

IV. CONCLUSION

This paper describes a new bias circuit that overcomes the weaknesses of the circuit proposed in [1] for the biasing of APDs operating up to 45 V. With this new architecture, a high-voltage CMOS process and a dual-rail power supply are no longer required and the bias voltage can be set by a single control signal. This results in a lower cost for the circuit implementation and simplification of the bias voltage control. The layout of this circuit was completed using a conventional CMOS process with a compact circuit footprint of 1.55 mm × 1 mm making it suitable for hybrid integrated with the 2 external capacitors and an APD in a single package.

ACKNOWLEDGMENT

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