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Heterogeneous integration of InP etched facet lasers to silicon photonics by micro transfer printing

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"I declare, this thesis resumes the research activities I was involved in the achievement of a transfer printable InP laser for silicon photonics.

This is to certify that the work I am submitting is my own and has not been submitted for another degree, either at University College Cork or elsewhere. All external references and sources are clearly acknowledged and identified within the contents. I have read and understood the regulations of University College Cork concerning plagiarism."

Ruggero Loi

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Abstract

Photonics Integrated Circuits allow optical functionalities and interconnects with small footprint, large band -width and -density, low heat generation. The silicon photonics platform (SOI) offers excellent waveguiding properties, large-area wafers and a highly developed CMOS infrastructure matured with electronics. Nevertheless, the key function of light amplification is missing due to the indirect band-gap of silicon. The light has to be provided to the SOI from a separate direct band-gap III-V material. InP based devices work in the infrared optical window of the electromagnetic spectrum and can be heterogeneously integrated to the SOI.

This research deals with the development of the first stand-alone InP Fabry-Perot lasers heterogeneously integrated to SOI by Micro Transfer Printing (μTP). The lasers are pre-fabricated and tested before transfer and are optimized to reach excellent optical, electrical and thermal performance. Lasers printed on Si substrates emit over 20 mW optical power, have threshold current of 16 mA and series resistance of 6 Ω; the thermal impedance of 38 K/W is half of that for the same laser printed directly on the SOI. The transfer printable InP ridge lasers have been designed as rectangular coupons with both contacts at the top and etched facets at the sidewalls. Two main release technologies based on the $FeCl_3$:H_2O (1:2) solution and a InGaAs or a InAlAs sacrificial layer were developed for releasing the devices from the original InP substrate with selectivity to InP greater than 4000 at 1 °C. The working principle of a polymer anchor system which restrains the devices to the substrate during the undercut were determined. The devices were printed on different silicon photonic substrates with excellent adhesion, with and without adhesive layers. A process for creating recesses into the SOI was developed to allow edge coupling the laser waveguide to the SOI or a polymer waveguide. High alignment accuracy along the three spatial directions can be achieved with alignment markers, reference walls and the interposition of a metal layer beneath the devices.

This work shows a possible path for the achievement of a laser source for silicon photonics and it has been the basis for the integration of others InP devices to PICs by micro transfer printing.

Glossary

- **2D**: Bi-dimensional.
- **3D**: Three-dimensional.
- **3σ**: Three sigma, 99.7 %.
- **5G**: Fifth generation cellular broadband network technology.
- **μTP**: Micro transfer printing.
- **AFM**: Atomic force microscope.
- **AlN**: Aluminium Nitride compound (ceramic).
- **ART**: Aspect ratio trapping.
- **ASIC**: Application specific integrated circuit.
- **BCB**: Benzocyclobutene.
- **BOE**: Buffered oxide etch.
- **BOX**: Buried oxide.
- **CMOS**: Complementary metal oxide semiconductor.
- **CPB**: Copper pillar bump.
- **CW**: Continuous wave.
- **DBR**: Distributed bragg reflector.
- **DFB**: Distributed feedback reflector.
- **DI**: De-ionized water.
- **DWDM**: Dense wavelength-division multiplexer.
- **DUV**: deep ultraviolet.
- **EAM**: Electro-absorption modulator.

- **e-beam**: Electron beam.
- **EIC**: Electronic integrated circuit.
- **$FeCl_3$**: Iron chloride compound.
- **FDM**: Finite difference model.
- **FEM**: Finite elements model.
- **FIB**: Focused Ion Beam.
- **FP**: Fabry-Perot.
- **FWHM**: Full width half maximum.
- **GaN**: Gallium nitride compound.
- **HF**: Hydrofluoric acid.
- **HMDS**: Hexamethyldisilazane.
- **HR**: Highly reflective.
- **IC**: Electrical integrated circuit.
- **ICP**: Inductively coupled plasma.
- **III-V**: Semiconductor alloys made by group III and V of the periodic table.
- **InAlAs**: Indium aluminium arsenide ternary III-V compound.
- **InGaAs**: Indium gallium arsenide ternary III-V compound.
- **InP**: Indium phosphide III-V compound.
- **IoT**: Internet of things.
- **IPA**: Isopropyl alcohol.
- **IR**: Infrared.
- **LD**: Laser diode.
- **LED**: Light emitting diode.
- **L-I**: Light-current characteristic.

- **LO**: Lift-off.
- **LSS**: Large spot size.
- **MBE**: Molecular beam epitaxy.
- **MEMS**: Micro electro mechanical systems.
- **MFD**: Mode field diameter.
- **MMI**: Multi mode interferometer.
- **MOVPE**: Metal-organic vapour phase epitaxy.
- **MOCVD**: Metal-organic chemical vapour deposition.
- **MQW**: Multi quantum well.
- **MRI**: MMI back reflector.
- **MSC**: Mode size converter.
- **NA**: Numerical aperture.
- **QD**: Quantum dot.
- **SBB**: Solder ball bump.
- **SOI**: Silicon on insulators.
- **SOI-PIC**: Silicon on insulators photonic integrated circuit.
- **PCB**: Printed circuit board.
- **PD**: Photo diode or photo detector.
- **PDMS**: Polydimethylsiloxane.
- **PECVD**: Plasma-enhanced chemical vapor deposition.
- **PIC**: Photonic integrated circuit.
- **PSM4**: Parallel single mode 4-channel signal transmission format.
- **PW**: Pulsed wave.
- **RMS**: Root Mean Square value.
- **RSOA**: Reflective silicon optical amplifier.

- **RTA**: Rapid thermal annealing.
- **SEM**: Scanning electron microscope.
- **SiN**: Silicon nitride.
- **SiN**$_x$: Silicon nitride compound.
- **SiO**$_2$: Silicon dioxide.
- **SOA**: Silicon optical amplifier.
- **SOI**: Silicon on insulator.
- **TEC**: Thermoelectric controller.
- **TLM**: Transmission line measurements
- **USA**: United States of America.
- **UV**: Ultraviolet.
- **VCSEL**: Vertical cavity surface emitting laser.
- **V-I**: Voltage-current characteristic.
- **WDM**: Wave division multiplexing.
- **WDM4**: Wave division multiplexing 4 channels signal transmission format.

Chapter 1

Introduction

The internet of the future has the purpose of making the world more energy efficient through the interconnection and management of systems and objects of the real world. This is the so called internet of things (IoT). In order to enable such a system, an infrastructure able to exchange continuously the enormous amount of data produced by the IoT has to be set in place. The internet is organized in a way that the data centres work as hubs for the data traffic management and storage. In turn, the performance of the data centres have to be improved in the first instance to enable faster and more energy efficient datacom. Use of photonics inside servers could be the solution for a real paradigm shift in the field of datacom and telecommunication.

This chapter introduces the reader to the motivations behind this thesis work. The data centre architecture and its main requirements are briefly discussed. Photonic integrated circuits (PICs) for datacom are discussed with particular reference to the silicon photonics platform. The lack of a light source in silicon photonics and the demand for integration of a III-V laser able to operate in the O- and C-optical bands of the electromagnetic spectrum are introduced. The chapter ends with an outline of the thesis to provide the reader indications on the structure of this work.

1.1 Data centres and the internet of the future

The advent of the Internet of Things (IoT) and the 5G telecommunication format requires an advanced internet infrastructure able to handle Zettabytes of data transmission. As reported in one of the last white papers from Cisco [1] the data traffic on the internet is expected to grow up to $\sim 280 \cdot 10^{18}$ B/month by 2021 [Fig. 1.1], corresponding to an average $\sim 8 \cdot 10^{2}$ Tbps rate.

Nowadays optical interconnects are widely deployed in the internet and in data centres down to the ultra-short-reach <10 m interconnects between server racks. The architecture of a data centre with the interconnections

types is reported in Fig. 1.2. The data centre is a hub of the internet where many optical links converge in order to access the data stored in servers. The external links access the core of the data centre from which an intricate amount of optical and copper interconnects, networking switches, routers and firewalls allow the access to particular servers and storage subsystems where the information required is stored. The long span inter-building interconnects (500 m to 10 km long links) are usually single mode fibers that allow parallel signal transmission formats as PSM4 and wavelength division multiplexing as WDM4. These interconnects can be operated at 40 to 100 Gbps and beyond (up to 400 Gbps). Optical inter-rack interconnects up to 200 m long are usually multi-mode optical fibers or active optical cables operated by vertical cavity surface emitting lasers (VCSELs) in SR4 format at 40 to 100 Gbps. Intra-rack interconnects up to 5 m long are direct attach cables made by copper that are still cheaper than optical interconnects and can operate up to 10 Gbps and beyond (moving to 25 Gbps). Use of optical interconnects for intra-rack communication would not introduce a great advantage in data rate transmission as the communication inside the servers is based on electronics [2]. The next step in enabling higher speed data flow consists in integrating photonics inside the servers for inter- and intra-chip interconnects [3], [4]. Photonics will allow one order of magnitude higher bandwidth of >100 Gbps, spatial density of about $Tb/s/mm^2$ and reduced 10-100 fJ/bit energy-efficiency compared to the actual electronic servers operating at <10 Gbps, $Gb/s/mm^2$, 1-10 pJ/bit while drastically reducing cross-talk, heating and then power-cooling issues [5], [6].

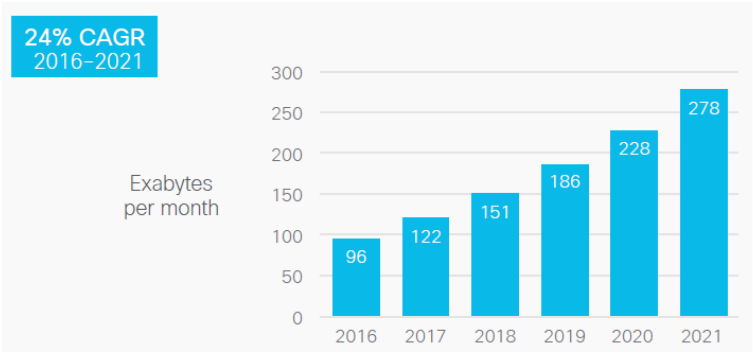


Figure 1.1: Cisco VNI forecasts 278 EB per month of IP traffic by 2021 [1].

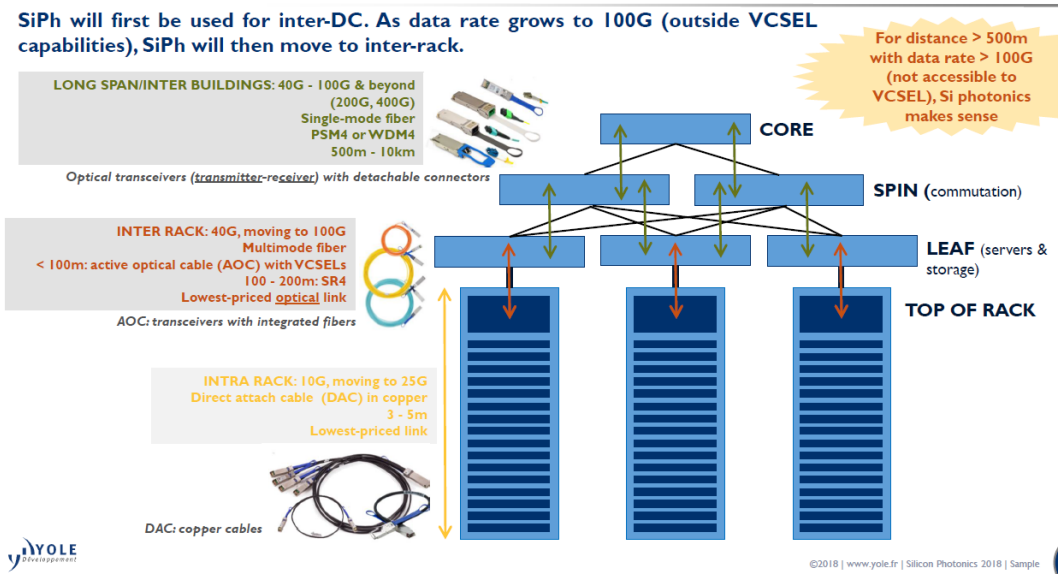


Figure 1.2: Data centre architecture and data rate allowed by the different interconnects [2].

1.2 Photonic integrated circuits for telecom and datacom

A photonic integrated circuit (PIC) is a platform that combines optical devices by connecting them through optical waveguides. Suitable platforms for PICs operating in the telecommunication wavelength range are InP and GaAs which offer integrated monolithic light sources, detectors and modulators; Another important candidate is silicon photonics, which can include SiGe and III-V hybrid integrated active elements; Dielectrics such as SiO_2 and Si_3N_4 offer low loss waveguides and passive elements over a wide wavelength range. PICs are a valuable way to achieve small optical interconnects and functionalities inside servers; PICs have reduced footprint, can be arranged in 3D stacks and can be easily interfaced with the driving or receiving electronics; most importantly PICs provide more bandwidth, low latency and low mutual interference between waveguides while keeping heat generation at minimum. This results in lower power consumption and cooling costs in data centers. High reliability is another aspect benefited by photonic integration [7]. Research in photonic integrated circuits will open new directions for novel optical functions.

PICs for telecom and datacom are modules which transmit or receive signals, the optical transmitters and receivers or a combination of the two, the so called transceivers. These modules are made by combining lasers, modulators, photodiodes and passive optical waveguides to the driving receiving

electronics. The laser allows generation of monochromatic light that can be modulated to transmit the information in a digital fashion. The higher the speed of signal transmission the more data that can be exchanged between two or more elements of a circuit per unit time. A laser can be modulated directly, or it can be powered in continuous wave while a modulator arranged in series with it modulates the light intensity or the phase. Photodiodes convert the light signals into current signals and are the core element of receivers.

The first 10×10 Gb/s wavelength division multiplexing (WDM) transcei ver was demonstrated in 2004 and since then most of the high-end PICs have been demonstrated on expensive III–V substrates [8], [9]. On the other hand silicon photonics transceivers have been demonstrated up to 25 Gbps [10], [11], and are gaining consent thanks to the reduced cost and the possibility to be fabricated with complementary metal oxide semiconductor (CMOS) technology [12]. The transceivers can be exploited at their best working on the wavelength, the modulation format (by acting on the phase or the amplitude) and by using WDM modulation format which allows multiple bidirectional communications over different waveguides and then parallel multiplication of datacom capacity.

PICs can be created with two main approaches, monolithically, as in the case of InP photonics, and heterogeneously as for Si photonics. The monolithic approach offers integrated, compact, efficient devices. InP active devices like lasers and modulators performs better than silicon-based technologies due to lack of misalignments to the waveguides defined on the same platform. However, passive waveguiding regions of the III-V wafer account for a large waste of the expensive material. The heterogeneous approach offered by Si photonics is more scalable not only because of the larger wafers but also due to the possibility of outsourcing the production of single photonic functions and the integration to different specialized companies. A similar assembly approach has been applied profitably in other large scale production areas as electronics and automotive. Market analysis and forecast show quick growth of the market and high investments in photonics and in particular in silicon photonics [Fig. 1.3] indicating the trend of industry in moving towards the SOI platform and so towards the heterogeneous integration approach.

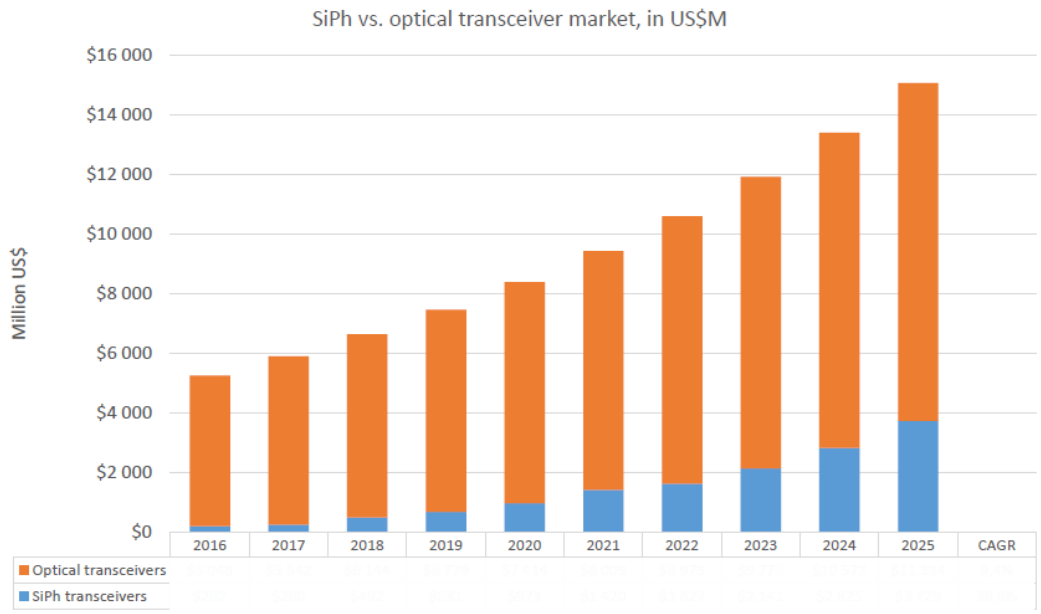


Figure 1.3: The Si photonics transceiver market is growing faster than the total optical transceiver market and is expected to reach more than 3500 M$ by 2025 [2].

1.2.1 Packaging of PICs

Packaging of PICs is perhaps the main challenge in creating optical transceivers, it requires tight micron alignment of the different optical and electronics elements, accurate temperature control and high spatial density integration of the different components. Telecom and datacom PICs are made by high bandwidth photonic devices connected by optical channels that can operate up to 25 Gbps and be multiplexed. Consequently, driving of the PIC components requires 25 Gbps electrical channels with low reflections and artifacts. Matching of photonics with electronics can be achieved with different layouts depending mainly on the final system. In some cases the PICs can be integrated with different layouts to an electronic integrated circuit (EIC), alternatively the PIC and the electrical integrated circuits (IC) can be integrated on a common EIC [10], [13], [14], [15]. In some cases, due to the large dimension of PICs it is convenient to integrate ICs along the PIC to drive the optical components [15]. The system is then connected to the electronics.

The electrical connection between a standard electronic printed circuit board (PCB) and the PIC can be achieved in different ways as there is not a standard layout for it. 50 Ω transmission lines able to deliver electrical signal to the photonic components connect a PCB to a PIC. A pitch-reducing

multi-level ceramic interposer matches the pitch of the PCB electrical channels to that of the PIC which can be a factor of three smaller [15]. The Interposer is connected to the PCB by $\sim$20 μm diameter and 100–500 μm long Au wire-bonds and to the PIC by bond pads [15]. The high-speed signals sent to the PIC must be then routed from the bond-pads to and from the relevant components on the PIC, tipically with a co-planar geometry. In small optical system such as transceivers, the vertical integration of a driver on the PIC is usually preferred over wire-bonds and interposers as it improves the high-speed electronic interface to the PIC with shorter and straight highly dense electrical connections that allow accurate sub-ns switching of multiple channels [15]. The vertical integration of an IC on a PIC can be achieved using $\sim$10 μm short solder-ball-bump (SBB) or copper-pillar-bump (CPB) interconnects, which provide an electrical, mechanical, and thermal interface between the two chips and minimize parasitic induction effects [16], [17], [18], [19], [20], [15]. A $<\pm 1$ μm accuracy alignment of the IC to the PIC can be achieved with a flip-chip system.

The light signals to and from the optical transceivers are coupled to optical fibers mainly through a grating or a mode size converter (MSC) in a edge-coupling configuration (see next chapter for more details about different types of light coupling) [15].

1.3 Silicon photonics integrated circuits

Silicon photonics is a large-area scalable platform offering up to 300 mm diameter wafers [21], this allows the integration of thousands of photonic components in waveguides above a buried silicon dioxide (BOX) cladding layer (Silicon on Insulator waveguides or SOI) [Fig. 1.4]. Silicon wafer are fabricated with the highest crystal lattice quality and are transparent in the wavelength range 1.1 μm to 8 μm allowing for light waveguiding in a broad range of wavelengths. This is of particular interest for the telecom wavelengths in the range 1.3 μm - 1.6 μm. Moreover, the SOI platform offers high index contrast between the Si waveguiding layer and the buried oxide allowing for high light confinement in tiny single mode waveguides of 220 nm $\times$ 450 nm cross section, with sharp bends of $<$5 μm bending radius that help reducing the foot print of the PIC. Silicon photonics integrated circuits (SOI-PICs) are able to provide multiple optical functions on wafer such as ring and Mach-Zehnder modulators normal and in-plane couplers, multi channel dense wavelength-division multiplexers (DWDM)

and demultiplexers. Ge hetero-structures as electro-absorption modulators (Ge-EAM) and photo-detectors (Ge-PD) can be monolithically integrated in particular spots of the SOI wafer. Optically pumped Raman lasers have been demonstrated too [22].

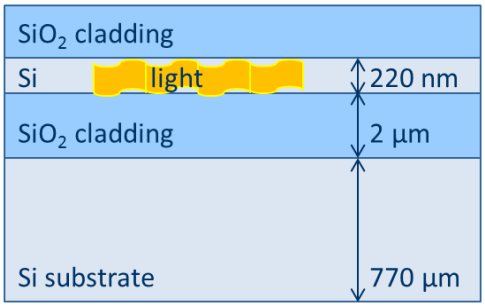


Figure 1.4: Schematic cross section of a standard SOI wafer. The light propagates in the 220 nm thick Si waveguiding layer, the top SiO_2 cladding layer is optional.

Silicon photonics, which is addressing many different opportunities and particularly optical interconnections for data centers, is an excellent platform for scaling photonics due to its similarity with the principles of the semiconductor electronics industry [23], [24], [25], [26], [12]. Silicon photonics exploits the fabrication experience, technology, and scalability already developed for complementary metal-oxide semiconductor (CMOS) electronics [4], [13], for the development of low-cost high-volume PICs with integrated electronics [3]. The functionalities of silicon photonics are revolutionizing the fields of telecommunication, datacom, high performance computing, medical devices, sensing automotive and military [27] [28], [23], [29], [Fig. 1.5]. Moreover SOI-PICs are applied in the creation of miniaturized spectrometers, bio-sensors, gas-sensors, lidar, optical coherence tomography etc. [15].

Contrary to III-V materials, Si is a naturally abundant material, it has high thermal conductivity of $\sigma(\text{Si}) = 1.3\ \text{W}\cdot\text{cm}^{-1\circ}\text{C}^{-1}$. Silicon photonics has the lowest cost per unit area with a 300 mm SOI wafer cheaper than a standard 50 mm diameter InP substrate. On the other hand the design and the development of new processes for silicon photonics accounts for most of the chip production costs, so the price per chip drops only when large scale fabrication can be achieved and only after that the processes have been optimized. Nevertheless, the key function of amplification (and lasing) is missing due to the indirect band-gap of silicon which makes it unlikely for electrons and holes to recombine radiatively when excited. Optical amplifiers in photonics are analogous of transistors in electronics, they are vital for creating lasers, switchers, for broadcast, wavelength conversion etc. Monolithic

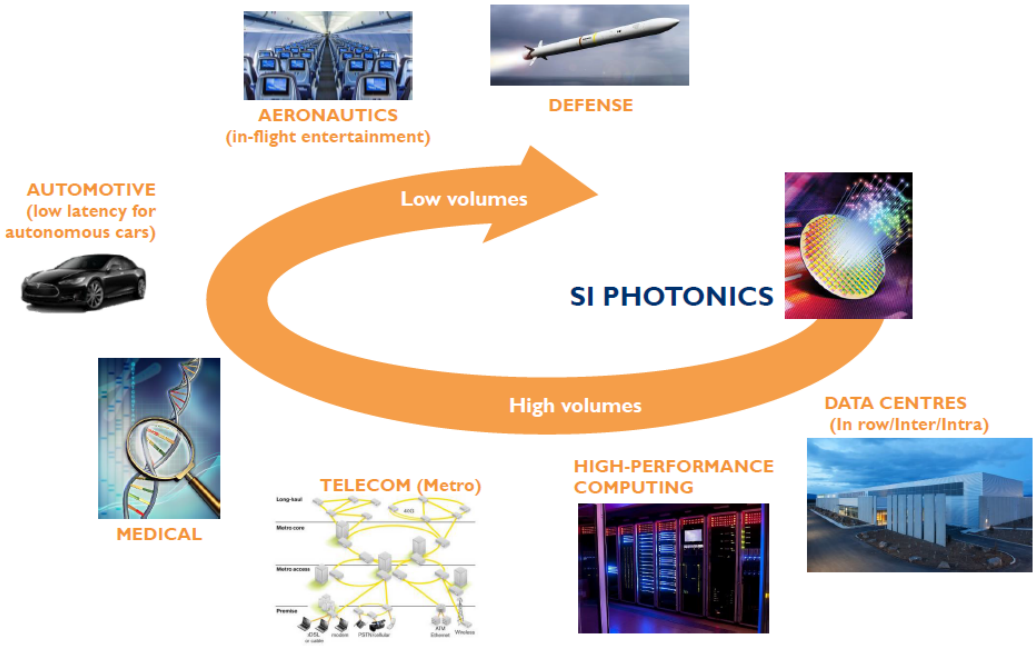


Figure 1.5: Silicon photonics applications production. [2].

integration of optical amplifiers on Si still requires more development (see section 2.2.2), Ge can be heavily doped and strained to achieve a pseudo direct band-gap but the radiative recombination rate still remains low for creating an efficient laser light source. Another possibility is to hybrid integrate a III-V component onto silicon for light amplification. This strategy has been proven to be the most effective (see chapter 2), but usually comes with light coupling issues between the III-V element and the SOI waveguides which need to be carefully evaluated as they can have important consequences for optical power budgets and energy efficiency of the whole PIC.

1.4 III-V materials and silicon photonics

III-V compound semiconductors are alloys containing elements from groups III and V in the periodic table. III-V typically are zincblende crystal structures with superior electron mobilities and direct band-gap which makes them suitable for efficient light amplification by stimulated emission. Changes in the alloy influences the lattice constant and the characteristic band-gap of the material, thus the wavelength of emission [Fig. 1.6]. These alloys can be lattice matched with ternary or quaternary compound semiconductors (alloys of three, four elements of III-V). This allows the realization of epitaxial structures whose wavelength of emission can be finely tuned. For example

the AlGaInAs active region of an InP telecom laser can be designed to emit at ∼1550 nm wavelength.

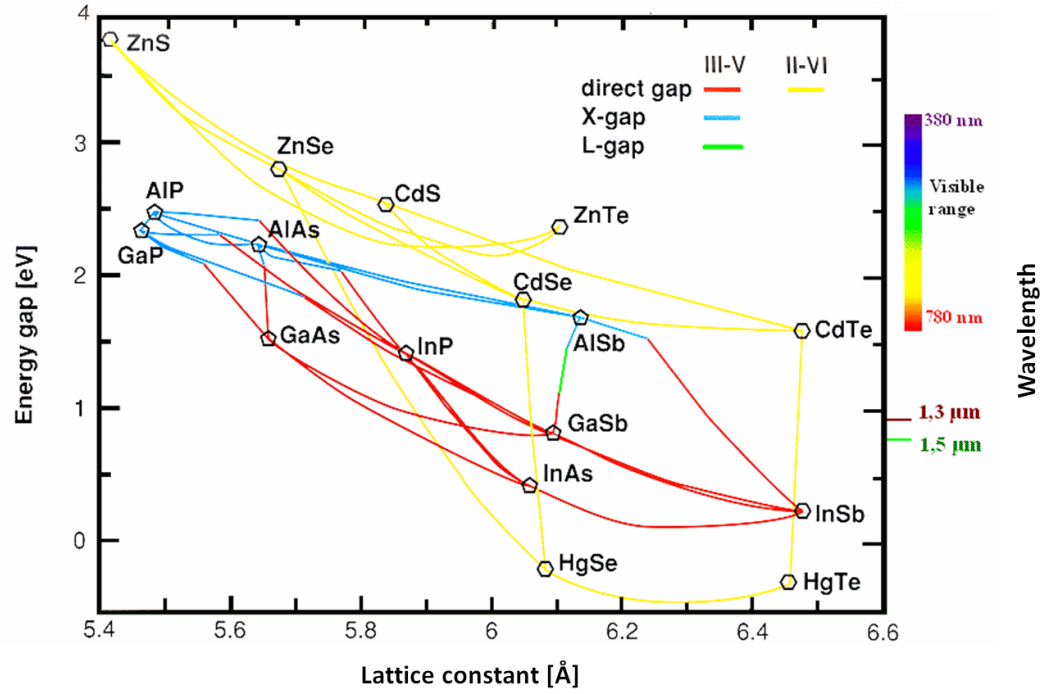


Figure 1.6: Energy gap versus lattice distance and corresponding emission wavelengths of the alloy. [30].

Driven by increasing global IP traffic, there are growing opportunities for III-V based semiconductor photonics components to be used in a diverse range of applications. These components need to be provided at low cost and should ideally scale in similar manner to silicon electronics. Nevertheless, due to the specific nature of individual III-V photonic components (lasers, modulators, detectors), it is highly challenging to monolithically integrate all these functions on a single substrate without compromising the performance of the individual devices [8] [31]. Thus, in general, a heterogeneous integration approach can be an effective way to combine optimized components for different PICs [32]. This would lead to the photonics components not being stand-alone but being co-integrated with different electronic and wave-guiding platforms.

Due to the lack of optical gain in silicon, an amplifier component needs to be integrated with silicon photonics in order to provide a gain medium and enable the most functional PICs. The laser light for the silicon photonics has to be provided from a separate direct band-gap III-V material. InP or GaAs based devices can be heterogeneously integrated depending on the

wavelength range it is desired to work at. GaAs based laser are used to operate in the optical band centered at 875 nm. As Si absorbs in the visible and near infrared (for wavelength λ<1200 nm), InP substrate based laser sources provide the most mature laser structures for data transmission in the optical C-band or in the O-band of the optical spectrum centered at 1550 nm and 1310 nm respectively. This wavelength range also offers easier interfacing of the PIC to the operational wavelength range of silica optical fibers. The heterogeneous integration of an InP-based devices to SOI has been demonstrated by using different integration techniques such as wafer bonding and micro transfer printing [33] [34] [35] [36] [37] (see section 2.2 for a more detailed discussion about these technologies).

III-V laser sources for telecom SOI-PICs are made by an InP section that amplifies the light and two mirrors that create a resonating cavity for the light generated. The light emitted by the device has to be single spatial mode in order to efficiently couple to a standard single mode SOI waveguide. Single mode emission is achieved by laterally confining the light with a micron scale wide ridge on top of the active region. These devices are realized as p-i-n junctions with the intrinsic region grown epitaxially as a few hundred nm thick multi quantum well structure. Ohmic electrical contacts have to be defined to the p side (over the ridge) and to the n layer in order to inject the electric current that activates the diode.

A crucial issue in the heterogeneous integration of InP active elements to SOI platforms is the thermal sinking of the heat produced by the device in operation [38], [39]. The heat generated by an integrated laser will increase the temperature of the active region shifting its wavelength and reducing its efficiency. The heat will also affect the platform on which the device operates through, for example, the resultant temperature distribution changing the properties of many devices (e.g. ring resonators, phase modulators) through the temperature dependence of the refractive index of silicon. In fact, while silicon is an excellent thermal conductor, the buried oxide in the SOI has poor thermal conductivity of $\sigma_{SiO(2)}$ $\sim$1.4 $\mathrm{Wm^{-1}K^{-1}}$. Since this represents an issue for the operation of the active devices on the SOI, the integration of III-V lasers requires careful attention of the system geometry and the materials involved to manage the heat produced [38], [40], [41], [42]. In the die bonding approach the heat should be dissipated through the buried oxide layer, so thermal shunts, metallic vias and trenches have been applied to sink the heat from the device to the Si substrate along preferential paths [42] [43], [34]. This approach involves a high level of complexity in

fabrication, especially after the integration of the III-V to the SOI. Another possibility consists in bonding the III-V laser die upside down on a metal sub-mount in contact with the Si substrate while achieving light coupling to the SOI waveguide by gratings [44], [45]. A different approach is to sink the heat to the substrate by μTP of the devices inside a recess on the SOI directly on the silicon substrate and then edge coupling the light to a waveguide [46] [47], [48].

1.5 Thesis structure

This work finds its main motivation in the development of a light source for silicon photonics; the structure of this work is summarized in 5 chapters which will guide the reader in a chronological description of the integration process of an InP transfer printable ridge laser with dry-etched facets to Si photonics by micro transfer printing.

- **Chapter 1**: As described at the beginning of this chapter, the first part focuses on the motivations behind this research. The data centre of the future requires photonic integrated circuits (PICs) for high speed intra-servers datacom. Si photonics results the best candidate for telecom PICs, but requires a III-V laser source able to operate in the infrared region 1300-1600 nm of the electromagnetic spectrum.

- **Chapter 2**: This section of the thesis reports the state of the art in the heterogeneous integration of III-V lasers to silicon photonics. The main strategies for light coupling between waveguides are discussed as they determine the final geometry of the integrated laser. The principal approaches used for light sourcing silicon photonics are reported with particular focus on the heterogeneous integration approach. The wafer bonding technology used for the integration of III-V to silicon photonics and the new emerging approach of micro transfer printing are reviewed here. The strategy chosen in this work for integrating an InP laser to silicon photonics is described in the final section.

- **Chapter 3**: The laser epitaxial structures used for transfer printable InP devices are discussed in this chapter. The design and the technological issues related to the fabrication of the device and its elements (facets, contacts, coupon shape) are described. The wet-etching release technology developed for the two main release structures used, InGaAs/InP and InAlAs/InP are described. The printing of the devices

with and without adhesives, the anchors removal and the adhesion enhancement methods are described too. Finally the recesses formation for laser integration and edge coupling to the SOI are described.

- **Chapter 4**: In this chapter are presented the electro-optical and the thermal characterization of the InP ridge lasers developed, before and after transfer printing to silicon photonics and other substrates. At the end of the chapter the effects of transfer printing on the device performance are discussed.

- **Chapter 5**: This chapter reports the simulations of the light edge-coupling of InP lasers to polymer and to SOI waveguides. The design and the sizing of the integrated system was determined by maximizing the light coupling efficiency. The demonstration of the first O-band laser heterogeneously integrated by μTP to recesses in the SOI and edge coupled to a multi-mode polymer waveguide is discussed together with the characterization steps performed.

- **Conclusions**: This section of the thesis summarizes the main results of this work focusing on the technological impact of this research. Future development and possible application of this technology are discussed at the end.

- **Appendixes**: Appendix A reports the main epitaxial structures used in this work for transfer printable InP lasers; Appendix B and C report the detailed fabrication processes for achieving a transfer printable InP Fabry-Perot laser coupon with and without encapsulation ledge. The ledge-less laser coupon is suitable for complete match of the emitting facet of the laser to a MSC on the SOI. Appendix D describes the fabrication process of recesses in the SOI, suitable for printing a laser coupon matched to the SOI.

Bibliography

[1] Cisco. *The zettabyte era: trends and analysis. Updated (07/06/2017)*. 2017.

[2] Yole Developpement. *Silicon Photonics 2018: Yes, we've reached Si photonics' tipping point!* 2018. URL: `https://www.i-micronews.com/report/product/silicon-photonics-2018.html` (visited on 11/21/2018).

[3] Roger Dangel et al. "Polymer waveguides for electro-optical integration in data centers and high-performance computers". In: *Optics express* 23.4 (2015), pp. 4736–4750.

[4] Günther Roelkens et al. "III-V/silicon photonics for on-chip and intra-chip optical interconnects". In: *Laser & Photonics Reviews* 4.6 (2010), pp. 751–779.

[5] David A B Miller. "Physical reasons for optical interconnection". In: *Intel J. Optoelectronics* 11 (1997), pp. 155–168.

[6] Sébastien Rumley et al. "Optical interconnects for extreme scale computing systems". In: *Parallel Computing* 64 (2017), pp. 65–80.

[7] Sai Chu et al. "Advanced photonic integration and high-index-contrast circuit". In: *Proc. Optoelectron. Commun. Conf.(OECC)*. 2009, pp. 1–2.

[8] Hyundai Park et al. "Device and integration technology for silicon photonic transmitters". In: *IEEE Journal of Selected Topics in Quantum Electronics* 17.3 (2011), pp. 671–688.

[9] Radhakrishnan Nagarajan et al. "Large-scale photonic integrated circuits". In: *IEEE Journal of Selected Topics in Quantum Electronics* 11.1 (2005), pp. 50–65.

[10] Akinori Hayakawa et al. "Silicon Photonics Optical Transceiver for High-speed, High-density and Low-power LSI Interconnect". In: *FUJITSU Sci. Tech. J* 52.1 (2016), pp. 19–26.

[11] Xuezhe Zheng and Ashok V Krishnamoorthy. "Si photonics technology for future optical interconnection". In: *Communications and Photonics Conference and Exhibition, 2011. ACP. Asia*. IEEE. 2011, pp. 1–11.

[12] Christopher Richard Doerr. "Silicon photonic integration in telecommunications". In: *Frontiers in Physics* 3 (2015), p. 37.

[13] Lockwood Tsybeskov, David J Lockwood, and Masakazu Ichikawa. "Silicon photonics: CMOS going optical [scanning the issue]". In: *Proceedings of the IEEE* 97.7 (2009), pp. 1161–1165.

[14] Cyriel Minkenberg et al. "Reimagining datacenter topologies with integrated silicon photonics". In: *Journal of Optical Communications and Networking* 10.7 (2018), B126–B139.

[15] Lee Carroll et al. "Photonic packaging: transforming silicon photonic integrated circuits into photonic devices". In: *Applied Sciences* 6.12 (2016), p. 426.

[16] Kerstin Worhoff et al. "Flip-chip assembly for photonic circuits". In: *Micro-Optics: Fabrication, Packaging, and Integration*. Vol. 5454. International Society for Optics and Photonics. 2004, pp. 9–20.

[17] XR Zhang et al. "Copper pillar bump structure optimization for flip chip packaging with Cu/Low-K stack". In: *2010 11th International Thermal, Mechanical & Multi-Physics Simulation, and Experiments in Microelectronics and Microsystems (EuroSimE)*. IEEE. 2010, pp. 1–7.

[18] KM Chen and TS Lin. "Copper pillar bump design optimization for lead free flip-chip packaging". In: *Journal of Materials Science: Materials in Electronics* 21.3 (2010), pp. 278–284.

[19] Philip Garrou, Christopher Bower, and Peter Ramm. *Handbook of 3D Integration, Volume 1: Technology and Applications of 3D Integrated Circuits*. John Wiley & Sons, 2011.

[20] JM Fedeli et al. "Development of silicon photonics devices using microelectronic tools for the integration on top of a CMOS wafer". In: *Advances in Optical Technologies* 2008 (2008).

[21] Shankar Kumar Selvaraja et al. "Highly uniform and low-loss passive silicon photonics devices using a 300mm CMOS platform". In: *Optical Fiber Communication Conference*. Optical Society of America. 2014, Th2A–33.

[22] Haisheng Rong et al. "A continuous-wave Raman silicon laser". In: *Nature* 433.7027 (2005), p. 725.

[23] Richard Soref. "The past, present, and future of silicon photonics". In: *IEEE Journal of selected topics in quantum electronics* 12.6 (2006), pp. 1678–1687.

[24] Michael Hochberg and Tom Baehr-Jones. "Towards fabless silicon photonics". In: *Nature Photonics* 4.8 (2010), p. 492.

[25] Solomon Assefa et al. "CMOS-integrated optical receivers for on-chip interconnects". In: *IEEE Journal of Selected Topics in Quantum Electronics* 16.5 (2010), pp. 1376–1385.

[26] Guoliang Li et al. "Ultralow-loss, high-density SOI optical waveguide routing for macrochip interconnects". In: *Optics express* 20.11 (2012), pp. 12035–12039.

[27] Chen Sun et al. "Single-chip microprocessor that communicates directly using light". In: *Nature* 528.7583 (2015), p. 534.

[28] Matthew Streshinsky et al. "The road to affordable, large-scale silicon photonics". In: *Optics and Photonics News* 24.9 (2013), pp. 32–39.

[29] Yasuhiko Arakawa et al. "Silicon photonics for next generation system integration platform". In: *IEEE Communications Magazine* 51.3 (2013), pp. 72–77.

[30] Prof. Dr. Helmut Foll. *III-V Semiconductors and Optoelectronics*. 2018. URL: `https://www.tf.uni-kiel.de/matwis/amat/semitech_en/kap_2/backbone/r2_3_1.html` (visited on 11/21/2018).

[31] Po Dong et al. "Silicon photonic devices and integrated circuits". In: *Nanophotonics* 3.4-5 (2014), pp. 215–228.

[32] Guang-Hua Duan et al. "New advances on heterogeneous integration of III–V on silicon". In: *Journal of Lightwave Technology* 33.5 (2015), pp. 976–983.

[33] Marco Lamponi et al. "Heterogeneously integrated InP/SOI laser using double tapered single-mode waveguides through adhesive die to wafer bonding". In: *Group IV Photonics (GFP), 2010 7th IEEE International Conference on*. IEEE. 2010, pp. 22–24.

[34] Günther Roelkens et al. "III-V/Si photonics by die-to-wafer bonding". In: *Materials Today* 10.7-8 (2007), pp. 36–43.

[35] Gunther Roelkens et al. "III-V-on-silicon photonic devices for optical communication and sensing". In: *Photonics*. Vol. 2. 3. Multidisciplinary Digital Publishing Institute. 2015, pp. 969–1004.

[36] Ruggero Loi et al. "Transfer printing of AlGaInAs/InP etched facet lasers to Si substrates". In: *IEEE Photonics Journal* 8.6 (2016), pp. 1–10.

[37] Andreas De Groote et al. "Transfer-printing-based integration of single-mode waveguide-coupled III-V-on-silicon broadband light emitters". In: *Optics Express* 24.13 (2016), pp. 13754–13762.

[38] Ruggero Loi et al. "Thermal Analysis of InP Lasers Transfer Printed to Silicon Photonics Substrates". In: *Journal of Lightwave Technology* 36.24 (2018), pp. 5935–5941.

[39] Chao Chen et al. "Sharing and placement of on-chip laser sources in silicon-photonic NoCs". In: *Networks-on-Chip (NoCS), 2014 Eighth IEEE/ACM International Symposium on*. IEEE. 2014, pp. 88–95.

[40] Zhi H Quan et al. "Thermal modelling of transfer-bonded thin-film gallium arsenide laser diode". In: *IET Optoelectronics* 10.2 (2016), pp. 51–56.

[41] Matthew N Sysak et al. "Experimental and theoretical thermal analysis of a hybrid silicon evanescent laser". In: *Optics Express* 15.23 (2007), pp. 15041–15046.

[42] Matthew N Sysak et al. "Hybrid silicon laser technology: A thermal perspective". In: *IEEE Journal of Selected Topics in Quantum Electronics* 17.6 (2011), pp. 1490–1498.

[43] Stanley Cheung et al. "Design optimization of energy-efficient hydrophobic wafer-bonded III-V/Si semiconductor optical amplifiers". In: *Optical Interconnects Conference, 2013 IEEE*. IEEE. 2013, pp. 108–109.

[44] Bowen Song et al. "3D integrated hybrid silicon laser". In: *Optics express* 24.10 (2016), pp. 10435–10444.

[45] Bowen Song et al. "High-Thermal Performance 3D Hybrid Silicon Lasers". In: *IEEE Photonics Technol. Lett* 29 (2017), pp. 1143–1146.

[46] *Micro-transfer printing for advanced scalable hybrid photonic integration*. Vol. 5. Valencia, Spain, 2018.

[47] Joan Juvert et al. "Integration of etched facet, electrically pumped, C-band Fabry-Pérot lasers on a silicon photonic integrated circuit by transfer printing". In: *Optics express* 26.17 (2018), pp. 21443–21454.

[48] *Edge-coupling of O-band InP etched-facet lasers to polymer waveguides on SOI by micro-transfer-printing*. Ghent, Belgium, 2019.

Chapter 2

III-V lasers for Si photonics and integration

The integration of III-V lasers to silicon photonics is an hot topic in recent research due to the possibility of joining the advantages of the III-V materials with those of the SOI platform for creating advanced photonic integrated circuits. The layout of a photonic circuit should depend mainly on the final packaging as the geometry and the layout of an integrated photonic device should be determined mainly by the way the light is coupled from the device to the waveguides. The engineering of the whole integration process should start with the analysis of these two main points. More often the integration goes the other way around with the devices to be integrated that determine the hosting platform layout. Still great efforts are needed in the standardization of the layouts of photonic integrated devices suitable for large scale production as the technology is at the early stage.

This chapter introduces the main approaches being used for coupling a III-V laser light source to silicon photonics with reference to the strategy used to couple the light between waveguides. The integration of III-V elements to silicon photonics has been successfully demonstrated through wafer bonding and it is discussed how it can be improved by micro transfer printing. The strategy chosen for the integration of a telecom InP laser to SOI is discussed at the end of the chapter.

2.1 III-V Laser sources for silicon photonics

Due to the indirect band-gap of Si it is challenging to create a laser light source from Si as the rate of radiative recombination when the material is excited is too low. Direct band-gap materials such as the III-V alloys provide efficient radiative recombination by stimulated emission when an external bias pumps the electric carriers in the conduction band. As mentioned in

the previous chapter it is possible to use strain and heavy doping to adjust the band-gap of Ge to being direct, but still the lasing performances of these materials are far from those of the III-V alloys. The advantages offered by the III-V compound semiconductors and their operation wavelengths make these materials suitable for creating efficient laser sources for silicon photonics. The light sourcing of silicon photonics with III-V must be achieved with a simple layout of integration and high light coupling efficiency in order to reduce powering budgets (as discussed in chapter 1). The III-V laser can be external to the PIC or integrated on it, then the light coupling can be achieved in different ways and with diverse layout of integration as outlined below:

- External laser
  - Laser to fiber to PIC
  - External cavity laser
- On-chip laser
  - Monolithically grown III-V laser
  - Heterogeneously integrated laser

Each of these configurations is classified as hybrid if the mirrors of the laser are positioned outside the III-V, i.e. on the SOI waveguide. Before discussing the different lasers for silicon photonics with their advantages and limitations, it is important to introduce the main light coupling strategies between waveguides as these determine the final layout of the device and of the PIC.

2.1.1 Light coupling between waveguides

The light coupling between dissimilar waveguides is particularly challenging due to mode mismatch being the main source of losses in the light insertion into a waveguide. For example, the mode size of a beam emitted by a single mode InP ridge laser is approximately $3.2 \times 1.7\ \mu m^2$ while in a typical SOI single mode waveguide is $0.5 \times 0.3\ \mu m^2$ in size. Phase matching and polarization issues can sensibly affect the light coupling between the laser and the SOI waveguide depending on the light coupling configuration and by the modes supported by the waveguides coupled. Polarization is usually a big issue when coupling the light through gratings and is a second order

loss in edge coupling. The light coming from an optical waveguide or fiber can be coupled to another waveguide in three main ways, by:

- Light coupling through gratings.
- Light evanescent-coupling.
- Light edge-coupling.

Each of these approaches has its own advantages and limitations, being more appropriate to a particular application. The principal aspects of these three different light coupling approaches applied to silicon photonics are discussed in the next sections.

Light coupling through gratings

Light coupling through gratings at infrared wavelength exploit a sub-micron periodic structure to create a coherent interference condition that diffractively couples the injected beam into the adjacent SOI waveguide [1], [2]. The incoming light has to be directed to the grating at a designed angle (usually of $\sim 10^{\circ}$) as to minimize the reflectance at the first order and maximize the injection according to the Bragg law. The etch depth of the grating changes the effective refractive index of the meta-material and has to maximize the transmittance while reducing the reflectance. The gratings are defined by immersion lithography or by electron beam (e-beam) lithography as shallow trenches etched into the SOI waveguiding layer [Fig 2.1(a)]; they can be shaped as mono dimensional or as bi-dimensional (2D) structures (more tolerant to misalignment) [Fig 2.1(b)]. Grating couplers do not need to be placed at the edge of the chip and can be wafer-scale tested before dicing and packaging. A typical 2D grating defined on a 220 nm thick SOI for matching the mode field diameter of a telecom optical fiber transmitting light at 1550 nm wavelength consists of a periodic array of 20 trenches about 70 nm deep and has a $\sim 10 \times 10$ μm^2 area footprint [3]. Typical light coupling configurations consist of an optical fiber (or a waveguide) to grating or grating-to-grating and the insertion losses are typically -3 dB. Recent works on uniform and apodized grating-couplers on SOI report a 1.6 dB and 1.2 dB insertion-losses [4], [5]. Insertion losses as low as 0.6 dB can be achieved by incorporating a metallic back-reflector, however this process is not scalable at the moment [6]. Grating couplers result highly spectral and polarization dependent behaviour typically allowing only <100 nm spectral

band-width. The polarization sensitivity is strong for linear grating couplers, however a 2D grating-coupler can be designed to accept any incoming polarization of light [7]. 2D grating couplers have insertion losses of 1.0 dB and 2.0 dB for designs with and without back-reflectors respectively, the polarization dependent losses can be as low as 0.3 dB [8], [9]. Grating couplers offer relaxed ± 2.5 μm in-plane alignment tolerances with an extra 1 dB penalty [10].

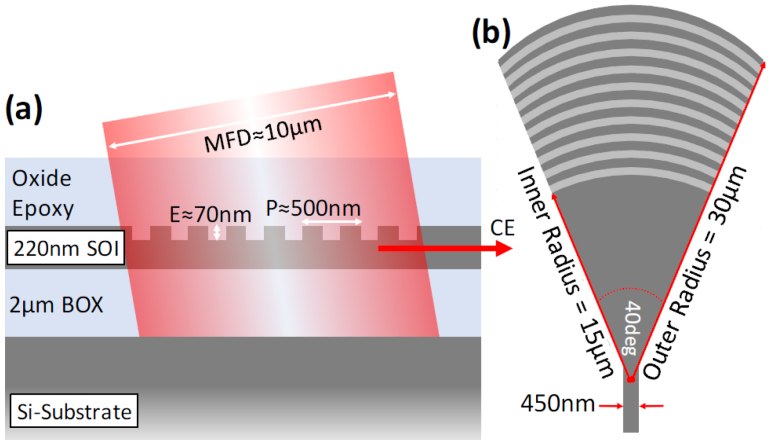


Figure 2.1: Fiber to SOI-PIC grating-coupling; (a) Side-view schematic of the grating-coupler defined on the SOI. The 10 μm mode field diameter (MFD) shines on the grating with a $\approx 10^{\circ}$ angle; (b) Top-view schematic of a 2D focusing grating-coupler. The footprint of the coupler matches the MFD of the optical fiber. [11].

Light evanescent-coupling

The evanescent coupling of the light between two adjacent waveguides is given by the interaction of the tail of the propagating modes. This strategy has been widely applied in the light coupling between III-V and SOI waveguides. Evanescent coupling between a III-V optical amplifier and an SOI waveguide were demonstrated at University of Santa Barbara (USA), IMEC (Belgium) and LETI (France), by using inverted taper structures [12], [13], [14] [15], [16], [17], [18], [19]. The light coupling efficiency was lower than 60 % as the light coupling between the III-V and the SOI waveguides was not completely adiabatic. The first truly adiabatic tapered structure for evanescent light coupling was demonstrated by IBM in 2015 [20]. In this case the light was completely evanescent coupled from an SOI waveguide to a single mode polymer waveguide with light coupling efficiency higher than 90 % [Fig. 2.2]. The same principles can be theoretically applied for the light coupling to glass-, SiN- or SiON-based waveguides coupled to the SOI. The evanescent coupling offers low insertion-loss of <1 dB, broadband

coupling, low sensitivity to polarization and relaxed alignment tolerances of ± 2 μm between single mode waveguides [20]. The inverted-taper of the evanescent coupler can be placed anywhere on the SOI, however its millimeter long foot print must be kept into account when designing a PIC.

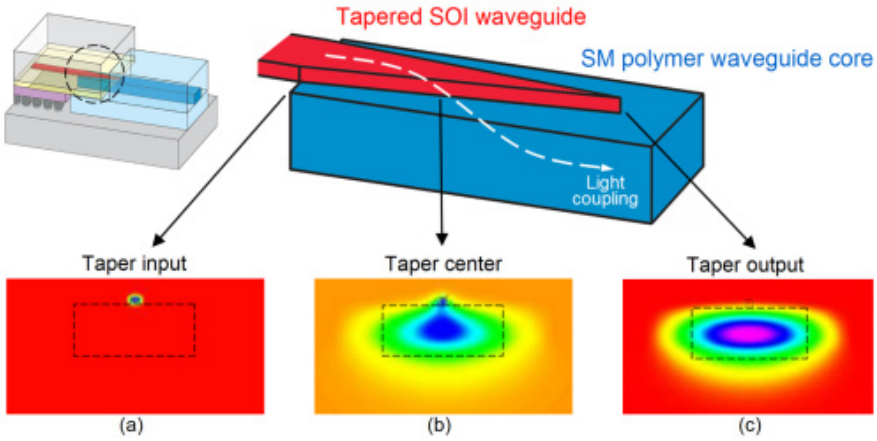


Figure 2.2: Schematic of the adiabatic evanescent coupling between SOI and polymer waveguides. The theoretical simulation of the optical coupling at λ=1550 nm show how (a) the light completely confined in the SOI waveguide, (b) is gradually squeezed in the polymer waveguide. (c) At the end of the taper all the light is completely confined in the polymer waveguide. [20].

Light edge-coupling

Light edge-coupling is achieved when butt coupling two waveguides one in front of the other. The edge-coupling has been widely applied in the light coupling between optical fibers and PICs and in commercial packaging of laser-chips to optical fibers [21] thanks to its broadband, polarization agnostic insertion-losses of better than -1 dB [22]. The mode mismatch between the two waveguides represents the main source of injection losses in this approach [23], [24], [25], [26]. In this configuration, the light is injected at the edge of the PIC into a mode-matched mode-size-converter (MSC) evanescent coupled to an underlying tapered SOI [Fig. 2.3]. MSCs can be made of SiON, polymer, SiO_x, Si_3N_4 waveguides embedding the inverted taper on the SOI waveguide [27]. Despite the many advantages offered, this strategy has not been widely applied to lasers integrated on-chip to silicon photonics due to the technological issues related to bulky packaging of lasers [28], [29], alignment and mode mismatch between the III-V laser waveguide and the SOI and due to requirement of using the etched facet technology. The particular application of the edge coupling to on-chip lasers and the state art of the device development is discussed more in detail in section 2.1.4.

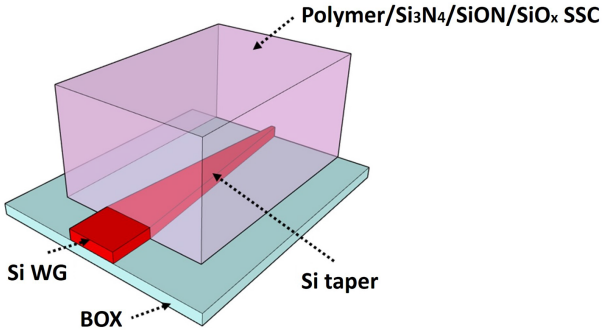


Figure 2.3: Diagram of a MSC for light edge coupling to a single mode SOI waveguide. The MSC can be made by an overlay of polymer, Si3N4, SiON or SiOx deposited over the taper defined on the SOI, this allow evanescent coupling and mode size conversion. [27].

2.1.2 External laser source

The light from an external laser source can be delivered to the SOI-PIC through an optical fiber and injected at an angle into a grating coupler on the SOI as already described. Another option is to cut the fiber facet at an angle and polish it to create a mirror that reflects the light down to the grating at the correct angle; this strategy offers a quasi-planar approach and reduced packaging dimensions [30], [31]. Alternatively, the fiber can be edge coupled to a mode transformer positioned at the edge of the SOI chip. These two strategies offer good light coupling efficiencies usually achieved through active alignment, however the injection of the light at the edge of the chip can be a limitation and requires use of large foot-print connection blocks [11]. In the edge coupling the SOI-PIC requires high precision dicing and polishing of the edges for achieving highly smooth matching surfaces on the SOI side. Another way to integrate lasers to the SOI is to pre-fabricate and pre-test a laser chip that can be light coupled in a dedicated location on the SOI as patented by Macom [32], or as demonstrated by Kotura and Oracle or by Luxtera [33], [34], [35]. This solution offers good alignment (<1 μm) and light coupling efficiency but is quite bulky (>100 μm thick) due to the packaging and can be not suitable for 3D stacking of SOI-PICs. Bulky PICs are usually more functional for stand alone applications as medical devices and sensors. A more compact layout is achieved by edge-coupling InP reflective semiconductor optical amplifier chips to silicon or silicon nitride photonics in external cavity laser configuration as demonstrated by Zilkie et al. [33] and more recently by Iadanza et al. [36]. In this case the coupling efficiency reaches up to 80 % for <1 μm and <0.5 μm lateral and vertical misalignment respectively.

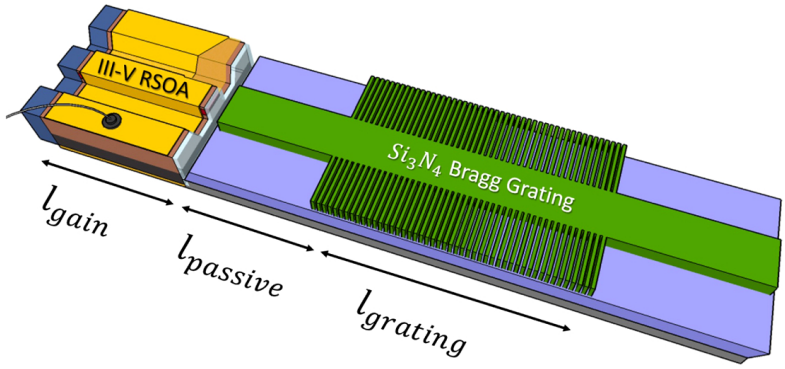


Figure 2.4: Schematics of the hybrid laser in external cavity configuration. The optical amplifier has a SiN mirror at the back facet and is edge-coupled to a SiN waveguide on the emitting side. The front reflector is on the SiN waveguide and consists in a Bragg grating. [36].

2.1.3 Monolithically grown III-V laser on silicon photonics

The development of a monolithic laser for silicon photonics is an hot topic in recent research [37], [38]. Germanium has been proposed as a possible monolithic light source due to its availability in CMOS factories today. Ge lasers monolithically grown on silicon have been demonstrated [39], however they show a threshold current density more than three orders of magnitude higher than that of III-V based lasers. This makes Ge lasers not applicable for commercial devices where low operating power is a key requirement for most applications. III-V monolithically grown on Si can be achieved by direct hetero-epitaxy and selective area hetero-epitaxy [40], [41], [42]. III-V laser epitaxial structures grown on Si have been grown directly on SOI allowing to create monolithic laser sources [43], [44], [45], [46]. Hetero-epitaxial growth of III-V to SOI can be achieved by molecular beam epitaxy (MBE) or metal-organic vapour phase epitaxy (MOVPE, also known as MOCVD). MOVPE and MBE allow very high control over thickness, composition and doping. In MOVPE, in contrast to MBE, the growth of crystals is by chemical reaction and not physical deposition. All these techniques provide high quality material only when grown on a substrate with the same lattice constant. Silicon and III-V present a mismatch in the lattice constant of 4.1 % for GaAs and of 8.1 % for InP, a different interface polarity and thermal expansion difference of ∼120 % for GaAs and ∼77 % for InP which make the direct growth of III-V to Si particularly challenging, especially for large area III-V grown on silicon. Different methods as special surface treatment, strained super-lattices, low-temperature buffers growth on patterned substrates have been used to reduce the lattice mismatch defects to <110

cm^{-2}, but this value is still about two orders of magnitude higher than that achieved with InP- or GaAs-based epitaxial wafers for room-temperature CW lasers. An alternative approach to reduce stress created by lattice mismatch between III-V and Si is to grow small area systems as quantum dots (QDs) or nano wires [47], [48], [49], [50]. Huge progress has been made with QDs laser grown on Si by Liu et al. [51], however a buffer layer and more development to combine this technology with silicon photonics are required. More recently aspect ratio trapping (ART) hetero-epitaxy has been used to mechanically trap a III-V seed on the Si substrate or the SiO_2 BOX in the SOI and grow locally the remaining layer structure [37], [52], [53], [54], [55]. ART eliminates the dislocations due by lattice mismatch between Si and III-V by selective growth of the III-V in high aspect ratio holes or trenches. The ART technique is suitable for integrating Ge or III-V devices with CMOS back-end process, it provides low thermal budget and can be applied to large wafers. However, the approach still requires a strategy to efficiently couple the light to the SOI. Moreover the III-V device fabrication on the SOI shows reliability issues [55], raises the complexity of the process and the risk of contamination of the CMOS.

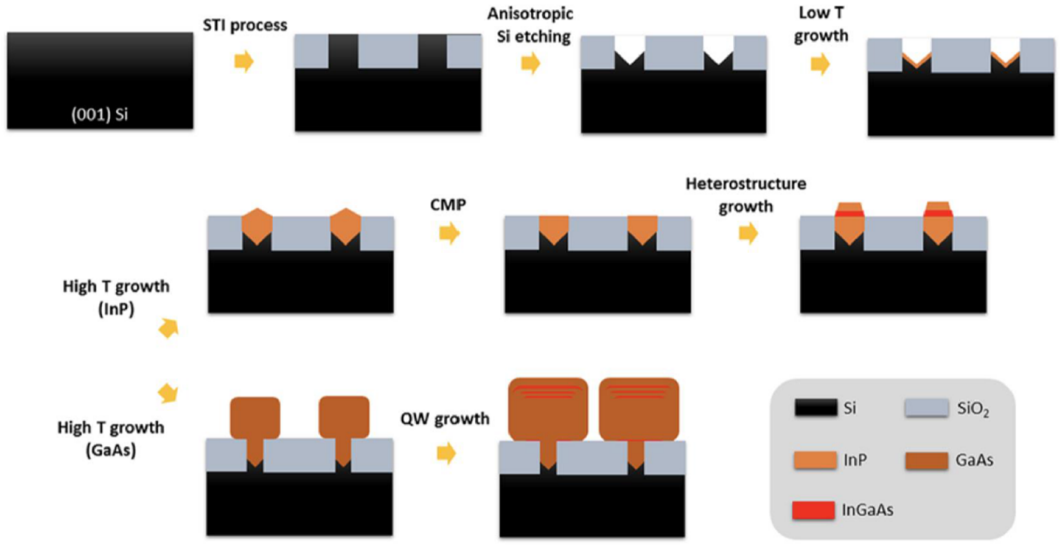


Figure 2.5: Schematic of the aspect ratio trapping hetero-epitaxy process for creating a III-V laser epitaxial structure in pre-fabricated trenches on the SOI. [56].

2.1.4 Heterogeneously integrated laser

A III-V die can be heterogeneously integrated to a desired location on the SOI-PIC for creating a silicon optical amplifier (SOA) or a laser. The III-V amplification cavity is usually arranged parallel to the plane of the SOI

waveguiding layer and the light coupling strategy chosen determines the final layout of the integrated device. Among the main heterogeneous lasers developed it is possible to classify them as evanescent lasers, laser coupled through gratings and edge-coupled laser. For each of these devices different layout of integration can be applied and by including components such as mode size converters, inverted tapers or a combination of the two.

Evanescent lasers

An evanescent laser is obtained by integrating a III-V waveguide on top of an SOI waveguide and by evanescent-coupling the light through inverted tapers that can be defined on the III-V, on the SOI or on both of them. The footprint of the device changes accordingly to the configuration used. The laser is usually hybrid, with the two grating reflectors defined on the SOI waveguide at the nano-scale that allow tuning the reflectivity and act as filters. Micro-ring reflectors can be used alternatively. The evanescent laser denomination differs according to the mirrors configuration adopted, the main layout developed are the distributed feedback (DFB) laser, the distributed bragg reflector (DBR) laser, the Fabry-Perot (FP) laser and the micro-ring-based laser. In the DFB configuration two shallow etched gratings separated by a $\lambda/4$ long section are defined on the SOI under the III-V die and interact with the evanescent part of the mode resonating inside the active region of the III-V. Inverted tapers are defined at the edges of the III-V die and on the SOI (or only on the SOI) to allow the light transfer from the SOI to the III-V and vice versa [Fig. 2.6 (a)] [57]. In the DBR configuration [Fig. 2.6 (b)], shallow etch gratings are defined on the SOI before and after the SOA, the evanescent-coupling of the light between the SOI and the III-V-SOA is provided by a double inverted taper structure [58], [16], [59]. A FP laser configuration can be achieved by using the same layout of the DBR except that the gratings are created by deep etching into the SOI. In this arrangement every grating acts as a facet with characteristic effective reflectivity and as a wavelength filter [Fig. 2.6 (c)] [60], [61]. Micro-ring reflectors are often employed in tunable lasers and can be defined on the SOI with different sizes that work as filters and reflectors for a particular mode of the laser [62], [63]. The evanescent coupling has been exploited more recently to couple the light of III-V devices heterogeneously integrated to the SOI by μTP [64], [65].

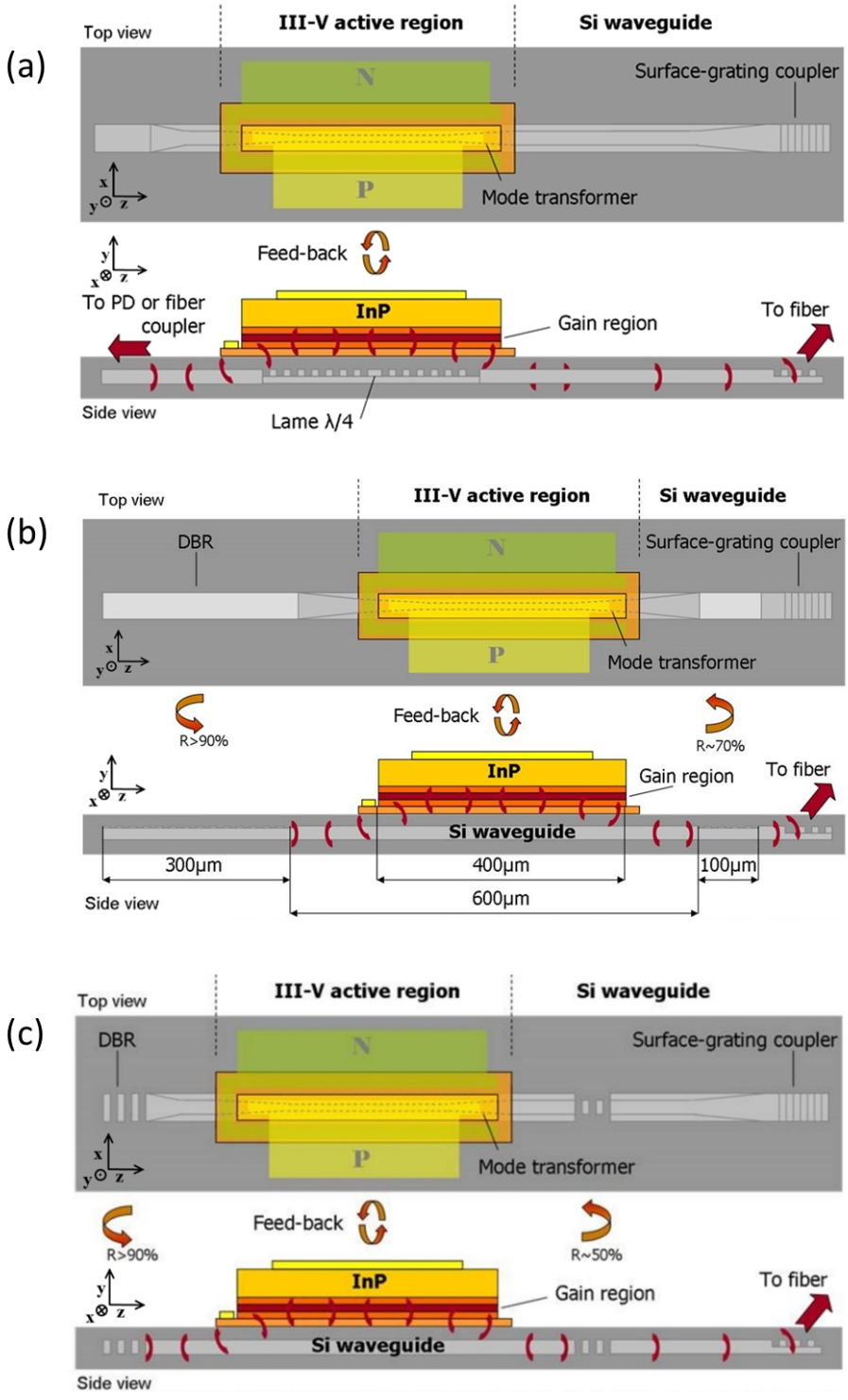


Figure 2.6: Schematic top view and longitudinal cross section for three different laser configurations developed by Leti (France). The light is evanescent-coupled between the III-V and the SOI by tapers. (a) A DFB laser is achieved by creating a DFB grating on the SOI, under the III-V [16]. (b) Two shallow etch DBR gratings defined on the SOI before and after the III-V section act as mirrors and wavelength selectors providing a DBR laser configuration [58]. (c) two deeply etched gratings provide a FP laser [60].

Edge-coupled laser

The edge-coupling configuration can be applied to heterogeneously integrate III-V lasers to a desired location on the SOI platform. A demonstration was given by Roelkens et al. [66], [67]. A III-V die is attached to the SOI with an intermediate benzocyclobutene (BCB) adhesive layer by using the die to wafer bonding technique (see section 2.2.1). A ridge waveguide and two dry-etched facets defined post integration create a Fabry-Perot resonating cavity on the III-V, next a mode size matched polymer MSC is butt-coupled to the ridge waveguide while being positioned on top of an inverted taper defined at the end of the SOI. The light is coupled from the polymer to the SOI by evanescent coupling. The optical mode in the III-V has to be optically insulated, this sets the height of the active region to the SOI and it makes challenging to match the mode to the polymer MSC. As we will see in the fourth chapter, devices integrated on the SOI show reduced thermal sink, especially if bonded with an intermediate thermally insulating layer. The post-integration fabrication of the ridge waveguide allows precise alignment to the SOI, on the other side the alignment of pre-fabricated III-V devices by using wafer bonding can be challenging. Other lasers edge coupled to a polymer waveguide section have been integrated on chip with a similar approach by Tseng et al. [29].

Another example of device on-chip edge-coupled to the SOI waveguide has been reported by Skorpios Technologies, III-V dies were integrated through an intermediate metal layer inside recesses on the SOI and have been edge coupled to the SOI to create lasers [68], [69]. The approach involves a >10 μm spacing between the emitting facet on the III-V and the SOI. This requires re-constructing the buried oxide layer in the gap and building an amorphous silicon waveguide with identical cross section to that of the crystalline silicon waveguide.

The strategies developed in this thesis for the heterogeneous integration of InP components to silicon photonics by using micro transfer printing technology enabled new architectures, parallel integration and precise alignment of the components involved [70]. InP Fabry-Perot laser coupons of calibrated thickness have been integrated by μTP inside recesses fabricate on a SOI wafer and edge-coupled to a trident MSC defined on the SOI [Fig. 2.7(a)], [71], [72]. The trident is made by two double tapers coupled to a taper defined at one end of the SOI [Fig. 2.7(b)] and can be defined during the SOI processing. The epitaxial structure of the lasers in ref. [71] provided

large spot size (LSS) lasers with a mode enlarged along the vertical axis compared to standard InP lasers, the cross section of the laser mode was simulated (with FIMMWAVE, by Photon Design [73]) of 5.5×2.7 μm^2 at $1/e^2$. The LSS lasers offer more relaxed tolerances on the vertical alignment in an edge-coupling configuration. The actual trident was mode matched to the LSS laser and squeezes the light in the SOI of mode size 0.5×0.3 μm^2. The devices were printed directly on the Si substrate inside the recesses while a n-InP cladding layer of calibrated thickness provided vertical alignment of the laser waveguide to the MSC. The layout developed involved the creation of recesses. The main technological issues related to the creation and integration of a III-V die in a recess on the SOI are discussed more in detail in chapter 5 (sections 5.2 and 5.3). Figure 2.7(c) shows the laser integrated and the emission spectrum [Fig. 2.7(d)] detected through an out-coupling-grating and an optical fiber.

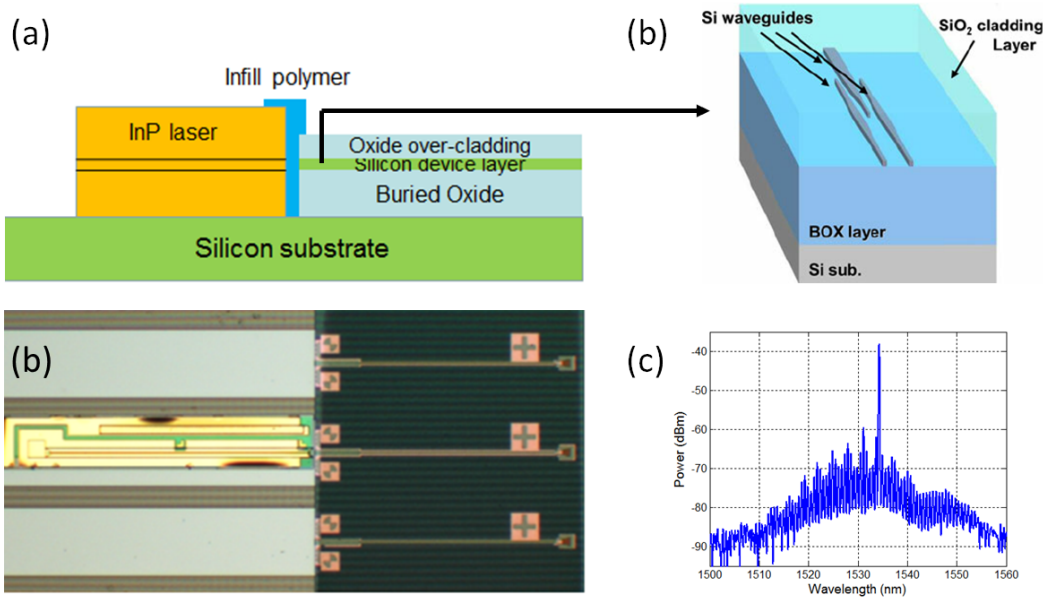


Figure 2.7: (a) Schematic of heterogeneously integrated InP laser on a silicon photonics platform. (b) Diagram of the trident MSC positioned at the edge of the recess between the laser and the SOI waveguide. (c) Digital microscope image of the real device integrated in a recess type 1 on the SOI. (d) Emission spectrum of the device. [71], [74].

Other devices edge-coupled on chip and integrated by μTP were reported, III-V LEDs and photodetectors (PDs) have been edge-coupled to polymer waveguides on a Si substrate by Liu et al. in order to create an optical interconnect suitable for electrical isolation [75], [76]. In chapter 5 it is presented an integration layout that combines the approaches presented in this section with the aim to achieve an InP laser integrated in a recess and

optically edge-coupled to a polymer waveguide or a polymer MSC connected to the SOI by accurately aligning the active region of the laser to the SOI along the vertical axis. The approach allows integrating lasers of different thickness thermally connected to the Si substrate.

Other heterogeneous lasers

In some cases the light coming from an heterogeneously integrated laser can be coupled to a grating at an angle as demonstrated by UCSB and Oracle [77], [78]. The coupling of an external laser to silicon photonics through a grating introduces an optical loss of typically -3 dB.

A less common option in heterogeneous integration of III-V to SOI is to integrate a vertical cavity surface emitting laser (VCSEL) on top of a grating and couple the light to it, this option can be problematic to implement due to requirement of injecting the light at an angle to the grating for achieving good light coupling efficiency [79], [80], [81]. Tilted-VCSEL allow passive flip-chip alignment to the PIC and rapid assembly at commercial volumes. However they are bulky and have large footprint which might be not suitable for PICs and 3D stacking.

2.2 Technologies for heterogeneous integration of III-V to SOI

The heterogeneous integration of a III-V laser source to the SOI can be achieved in different ways, the main techniques applied are:

- Flip-chip wafer bonding.
- Flip-chip die to wafer bonding.
- Micro transfer printing (μTP).

2.2.1 Wafer and die to wafer bonding

III-V have been successfully integrated by flip chip wafer bonding or die-to-wafer bonding [82] to the SOI. In wafer bonding and die to wafer bonding the wafer or the die are flipped and bonded with the substrate up at the desired area on the SOI, then the substrate is removed by wet-etch and a post-integration processing allows the definition of the devices. The post processing of the dies into devices reduces the misalignment of the III-V

waveguide to the SOI to lithographic tolerances (<0.5 μm). The coupons of III-V gain material are bonded directly, by molecular bonding, using a low temperature O_2 plasma-assisted surface activation or with an adhesive layer, usually made of benzocyclobutene (BCB) [82]. The light from the III-V has been coupled to the waveguide by edge coupling [67], [29], grating coupling [77] or by evanescent coupling through the use of tapers [19]. Wafer bonding has been applied by Intel to large scale production. The main issue with this approach is the large waste of the expensive III-V material. The die to wafer bonding mitigates the waste of the III-V compared to wafer to wafer bonding. Post integration processing of the III-V on the SOI requires careful process design to reduce contamination issues of the machinery during fabrication. Furthermore errors in processing one element of the circuit can propagate to the whole platform wasting all the preparatory work on the SOI. Pre-fabricated known good device integration would be desirable to reduce post-integration processing on the SOI to minimum and to allow testing the devices on the original III-V substrate before the integration to the SOI. Furthermore, pre-fabricated lasers could be fabricated by specialized companies and be lately integrated in different specialised facilities in a production chain fashion similar to other large scale fabrication areas as electronics and automotive. However full pre-fabrication of devices is not applicable to flip-chip wafer bonding as the substrate of the die prevents visual passive alignment of the devices to the SOI. In wafer bonding the epitaxial structure has to be grown upside down. Another limit of the technique is given by thermal expansion gradients between the wafer or die bonded and the new substrate which can be an issue especially for large area dies.

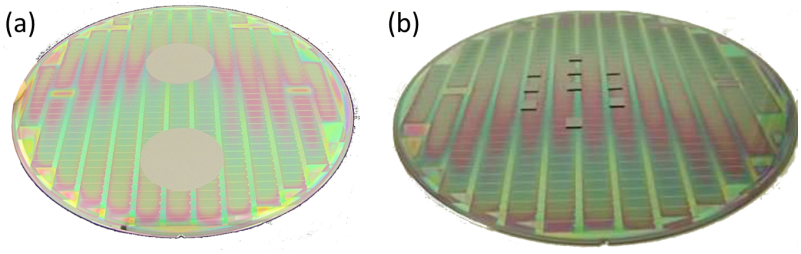


Figure 2.8: (a) 200 mm diameter SOI with two 50 mm diameter InP wafers bonded on it. (b) SOI with InP dies printed on top of it. [60].

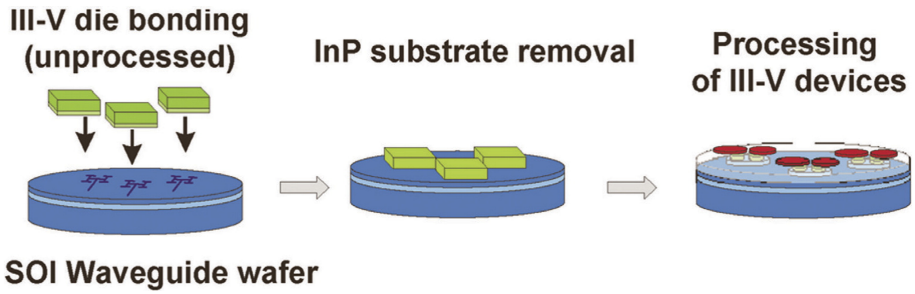


Figure 2.9: Diagram of the die to wafer bonding process for the integration of InP dies to the SOI platform. [66].

2.2.2 Micro Transfer Printing

Micro-Transfer-Printing (μTP) is emerging as an effective, accurate and massively parallel tool for the heterogeneous integration of photonic and electronic devices to different platforms including silicon photonics [83], [84], [85], [86], [74]. μTP offers epitaxial side-up transfer of dense arrays of coupons to structured substrates. The source coupons can be unprocessed, part or fully processed before transfer into devices with the appropriate structuring and electric contacts present. μTP has been demonstrated for multiple materials including silicon, graphene, dielectrics and III-V as InP, GaAs, InAs, GaN. In this work we present the development of μTP technology for the integration of InP ridge lasers completely pre-fabricated on the original substrate to SOI (chapter 3).

μTP involves the formation and registration of typically less than 5 μm thin coupons on a starting wafer, the release from the source wafer, the sequential, parallel transfer of stamp-selected arrays of coupons to selected matching locations on a target substrate. The primary requirement for bonding on the new substrate is that the mating surfaces are locally flat and coplanar. The bonding can be achieved by coating the surface of the target substrate with a thin layer of polymer which also assists the bonding. A direct bond can also be achieved through van der Waals forces if the surfaces involved are flat and smooth enough [87]. μTP is particularly enabled for thin and small dimensioned coupons. Solutions for the transfer of many different thin and small materials can be engineered according with the platform involved. The optimal device structures are distinct for different photonic functions which make their co-integration challenging.

A polydimethylsiloxane (PDMS) elastomeric stamp is used in μTP to retrieve and deterministically assemble arrays of devices onto non-native substrates [Fig. 2.10]. It is possible to collect or release the devices by varying the speed of the PDMS stamp according with the peel-rate-dependent

adhesion in visco-elastic elastomers [83], [88], [89], [90] [Fig. 2.11(a)]. If the PDMS stamp in touch with the top of the devices is peeled quicker than a critic speed, v_c, it can collect the devices and if it is peeled slower than v_c (after print) it can release them on the hosting substrate. The phenomenon, as reported by Meitl et al. [83], can be described by the separation energy G_{PDMS} of the PDMS to the top surface of a device. G_{PDMS} depends strongly on the speed of delamination, v, and it can be approximated by eq. 2.1:

$$G_{PDMS} = G_0 \left[1 + \left(\frac{v}{v_0} \right)^n \right] \tag{2.1}$$

where G_0 is the energy release at rest (v=0 m/s), v_0 is the speed at which G_{PDMS} is twice G_0 value, n is a fitting parameter. G_0 depends on the composition and the process to prepare the PDMS stamp. The PDMS stamps used in this work were provided by X-Celeprint Ltd. [91] and are protected by intellectual property. If the G_{PDMS} is greater than the adhesion of a coupon to its original substrate G_{SUB} then the coupon will be picked up. A pre-patterned transparent PDMS stamp allows collecting only the desired devices from the source wafer [Fig. 2.11(b)]. Each post on the PDMS stamp has the same shape of the coupon to maximize the contact area to it and in turn increase the yield of picked devices. A post with the same size of the coupon also reduces the chance to interfere to other objects both on the picking and on the printing substrate. The thickness of the stamp is protected by intellectual property of X-Celeprint [91]. The lifetime of a PDMS stamp has been tested by X-Celeprint of 60000 transfer-printing cycles. However, they advise to change the stamp after 10000 cycles for keeping the repeatability of the process maximum. Each transfer printer tool has a robotic arm which acts the PDMS stamp for collecting pre-released devices from a wafer and transfer them to a target substrate [Fig. 2.12]. μTP offers fast passive alignment of arrays of devices with $\leq \pm 1.5$ μm [70] through pattern recognition software (COGNEX VisionPro [92]) thanks to its transparent head stage, μTP is highly scalable so it is possible to transfer just one or thousand of devices in one step, it is suitable for both pre- and post-integration fabrication. Sub-micron alignments have been achieved for single post transfer printing [93], but still require optimization with the actual machinery. Other demonstrations of submicron alignment by transfer printing have been given at Stratchlyde University by J. McPhillimy et al. with a different tool [94], [95]] suitable only for prototyping.

The main limits of the μTP technology are given by sub-micron alignment (as reported above), by the integration speed in transferring a given number of devices to the target chip and by the number of devices integrable in one transfer step, which is limited by the size of the source wafer and by the size of the coupons.

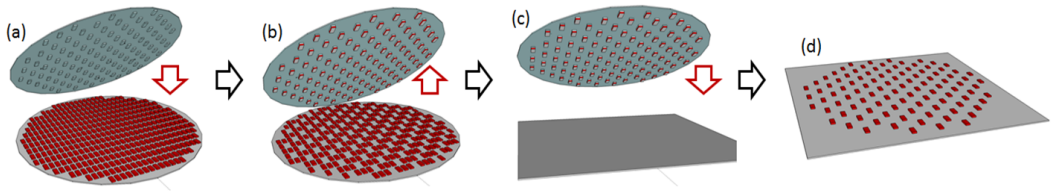


Figure 2.10: Scheme of the transfer printing process; (a) the pre-patterned PDMS stamp is lowered in touch with the top of the devices; (b) the robotic arm peels quickly off the PDMS which picks up the devices from the source wafer, (c) then the populated PDMS stamp is moved onto the target wafer and the devices are released in the desired location by gently peeling off the PDMS stamp.

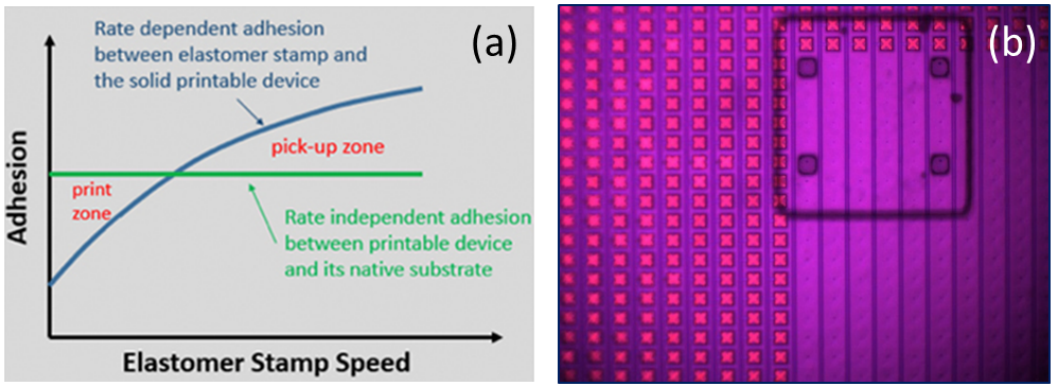


Figure 2.11: (a) Adhesion peel-rate curve for PDMS. It is possible to locate two regions of adhesion that depend on the peeling speed of the stamp allowing respectively to pick up and print the devices from and to a new substrate. (b) A stamp positioned on top of the source wafer ready to be positioned and pick-up some squared coupons, the view is from the operator perspective on the alignment screen. Images are courtesy of X-Celeprint Ltd. [91].

Transfer printable devices require four main extra steps to be incorporated in the fabrication process for preparing them to the μTP. First, it is necessary to include a sacrificial layer in the epitaxial structure of the wafer to allow the separation of the coupons from the source wafer. Second, a wet-etch technology has to be developed for the erosion of the sacrificial layer while keeping high selectivity to the surrounding materials. Third, an encapsulation layer must be defined to protect the sidewalls and the top of the coupon. Fourth, an anchor system able to restrain the coupons/devices on the original substrate with calibrated strength during the undercut has to be

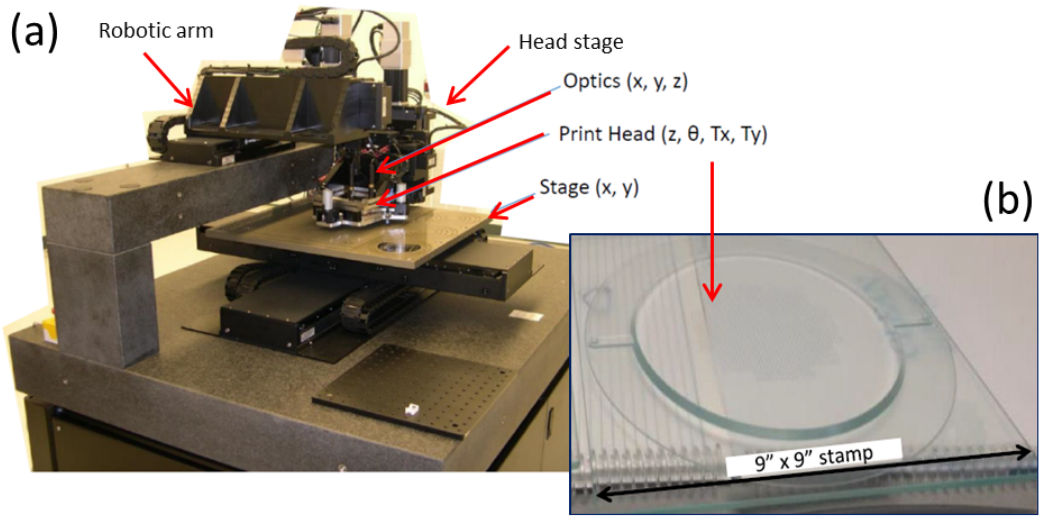


Figure 2.12: (a) Transfer printer machinery, model MTP-177, as used in this work for automated μTP. The robotic arm moves over a stone stage arranged on a anti vibration table. (b) the transparent head stage hosts the pre patterned transparent PDMS stamp. Images are courtesy of X-Celeprint Ltd [91].

engineered and defined on the device before the undercut. The final result of the preparatory steps is a suspended coupon ready for μTP to the new hosting substrate. An example of the transfer printing process including the preparation, undercut, and μTP steps applied to InP lasers is reported in Fig. 2.13 and discussed more in detail in the next chapter (section 3.1).

2.3 Choice of the strategy for the heterogenous integration of InP etched facet lasers to the SOI

An analysis of the main pros and cons of the different strategies for laser light coupling to SOI waveguides are summarized in table 2.1. The evanescent coupling offers many advantages for creating a III-V laser on the SOI and this is the reason of its wide application in the field. The edge-coupling offers most of the advantages of the evanescent coupling removing the requirement of defining sub-micron taper structures on the III-V which would require use of the e-beam. This translates to a smaller foot-print of the III-V and in turn in a reduced waste of the material. On the other side the total foot print of the laser and the MSC connected to the SOI it is very similar to that of the evanescent coupling. One of the main issues in edge-coupling a ridge laser to an SOI waveguide is the requirement of tight alignment

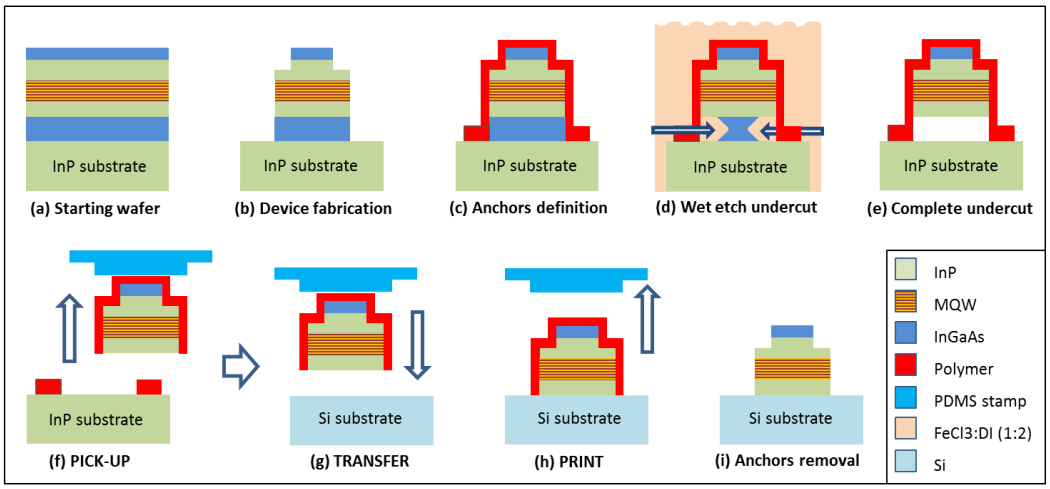


Figure 2.13: (a, b, c) Cross-section of a laser coupon fabricated on the InP wafer containing an InGaAs sacrificial layer and anchored to the substrate by a resist tether structure. (d, e) The undercut in $FeCl_3$:H_2O results in suspended coupons ready for micro-transfer-printing. (f, g, h) In μTP a PDMS stamp collects the devices from the original wafer and releases them to the target substrate. (i) Final step of the process is the removal of the polymer anchors. [87].

of $<\pm 1$ μm along the SOI plane and $<\pm 200$ nm along the remaining vertical spatial direction that are required for achieving high light coupling efficiency as analysed in chapter 5 (section 5.1). The edge-coupling layout also requires creation of recesses of calibrated depth on the SOI. The edge coupling does not require facets angled to the vertical axis as applied by Song et al. [77] for injecting the light in a grating at a specific angle.

Table 2.2 summarizes the main advantages and limits of wafer-to and die-to wafer bonding and micro transfer printing. Wafer bonding and die-to wafer bonding have shown excellent capabilities in integration of III-V to SOI, the post-integration fabrication of ridge waveguides allows high alignment of the laser waveguide to the SOI. On the other side, the post-integration fabrication is the only option possible in wafer bonding and prevents passive alignment due to the presence of the substrate. The approach is also limited by the waste of the expensive III-V material. As mentioned in section 1.3 most of the costs in the creation of a device are in the design and process development, but once the III-V waste is extended to large scale production it can become an issue.

The micro transfer printing offers epitaxial side up parallel integration of small III-V components with $<\pm 1.5\mu$m lateral alignment precision [70]. Thermal expansion issues can be reduced with the dimension of the coupons.

The comparison of advantages and limits of the different light coupling and integration strategies allowed to choose the strategy for creating a laser

Light coupling	Pros	Cons
Grating	Footprint Alignment Positioning	Light injection Insertion loss Polarization Narrow band
Evanescent	Alignment Positioning Insertion loss Broadband Polarization	Footprint Tapers
Edge	Footprint Positioning Insertion loss Broadband Polarization	Alignment Use of MSC

Table 2.1: Comparison of different strategies for light coupling of lasers to SOI.

Integration technique	Pros	Cons
Wafer bonding	- Mature - alignment	- Post-integration fabrication only - High material waste
Die bonding	- Mature - alignment	- Post-integration fabrication only - Material waste
μTP	- Parallel - Material saving - Multiple components - Pre- and Post- integration fabrication	- Early stage - <1 μm alignment

Table 2.2: Comparison of different techniques for the heterogeneous integration of III-V to SOI.

source for silicon photonics. The plan was to heterogeneously integrate, by μTP, a pre-fabricated Fabry-Perot InP ridge laser with etched facets to a recess pre-fabricated on the SOI in order to achieve a light edge-coupling configuration with tight alignment of the waveguides. The light can be edge coupled to a polymer waveguide and then evanescent-coupled to the SOI or in alternative the light can be edge-coupled to a MSC converter defined

at the end of SOI waveguide, a trident MSC works in this situation [71]. The strategy provides reduced footprint by keeping the tapers only on the SOI. A small footprint turns in reduced use of III-V material and reduced thermal expansion issues. The strategy offers the advantages and the flexibility of the etch facet technology (see section 3.2.4). μTP allows accurate planar alignment of the laser waveguide to the SOI, the vertical alignment is ensured by integrating the devices inside recesses of calibrated depth preformed on the SOI. An intermediate metal layer positioned at the bottom of the recesses allows to tune the height of the laser waveguide to the SOI and it allows to sink the heat to the substrate working as a thermal via. The strategy provides high electro-optical and thermal performance (as shown in chapter 4 and 5) with the theoretically low insertion losses associated to the edge-coupling. In particular, completely pre-fabricated and pre-tested InP lasers allow to micro-assemble only the working devices to the SOI. Consequently, increased reliability of the final PIC and simple layout of integration can be achieved by edge coupling the light from the laser to a polymer or SOI waveguide.

2.4 Conclusion

The review of the state of the art on III-V laser integration to silicon photonics has been presented in this chapter. The comparison of the advantages and limitations of the diverse techniques of integration and light coupling allowed to define the strategy for integrating a III-V telecom laser to silicon photonics, in agreement with the cleanroom laboratories and tools available at Tyndall National Institute.

The heterogeneous integration of an InP laser onto SOI by using μTP requires the device to be made transfer printable, so releasable from the original substrate with resulting surfaces suitable for the bonding to the new substrate. The preparation of the InP lasers for the transfer printing is discussed in all the technical aspects in the next chapter.

Bibliography

[1] Frederik Van Laere et al. “Compact focusing grating couplers for silicon-on-insulator integrated circuits”. In: *IEEE Photonics Technology Letters* 19.21-24 (2007), pp. 1919–1921.

[2] Günther Roelkens et al. “Grating-based optical fiber interfaces for silicon-on-insulator photonic integrated circuits”. In: *IEEE Journal of Selected topics in quantum Electronics* 17.3 (2011), pp. 571–580.

[3] Jun Su Lee et al. “Meeting the electrical, optical, and thermal design challenges of photonic-packaging”. In: *IEEE Journal of Selected Topics in Quantum Electronics* 22.6 (2016), pp. 1–9.

[4] Diedrik Vermeulen et al. “High-efficiency fiber-to-chip grating couplers realized using an advanced CMOS-compatible silicon-on-insulator platform”. In: *Optics express* 18.17 (2010), pp. 18278–18283.

[5] Xia Chen et al. “Apodized waveguide grating couplers for efficient coupling to optical fibers”. In: *IEEE Photonics Technology Letters* 22.15 (2010), pp. 1156–1158.

[6] Wissem Sfar Zaoui et al. “Bridging the gap between optical fibers and silicon photonic integrated circuits”. In: *Optics express* 22.2 (2014), pp. 1277–1286.

[7] Shibnath Pathak et al. “Compact SOI-based polarization diversity wavelength de-multiplexer circuit using two symmetric AWGs”. In: *Optics Express* 20.26 (2012), B493–B500.

[8] Lee Carroll et al. “Broad parameter optimization of polarization-diversity 2D grating couplers for silicon photonics”. In: *Optics express* 21.18 (2013), pp. 21556–21568.

[9] Lee Carroll et al. “Optimizing polarization-diversity couplers for Si-photonics: reaching the- 1dB coupling efficiency threshold”. In: *Optics express* 22.12 (2014), pp. 14769–14781.

[10] Dirk Taillaert et al. “Grating couplers for coupling between optical fibers and nanophotonic waveguides”. In: *Japanese Journal of Applied Physics* 45.8R (2006), p. 6071.

[11] Lee Carroll et al. "Photonic packaging: transforming silicon photonic integrated circuits into photonic devices". In: *Applied Sciences* 6.12 (2016), p. 426.

[12] Stevan Stankovic et al. "1310-nm hybrid III–V/Si Fabry–Pérot laser based on adhesive bonding". In: *IEEE Photonics Technology Letters* 23.23 (2011), pp. 1781–1783.

[13] Marco Lamponi et al. "Heterogeneously integrated InP/SOI laser using double tapered single-mode waveguides through adhesive die to wafer bonding". In: *Group IV Photonics (GFP), 2010 7th IEEE International Conference on*. IEEE. 2010, pp. 22–24.

[14] Hsu-Hao Chang et al. "1310nm silicon evanescent laser". In: *Optics Express* 15.18 (2007), pp. 11466–11471.

[15] Xiankai Sun et al. "Electrically pumped hybrid evanescent Si/InGaAsP lasers". In: *Optics letters* 34.9 (2009), pp. 1345–1347.

[16] Alexander W Fang et al. "A distributed Bragg reflector silicon evanescent laser". In: *IEEE Photonics Technology Letters* 20.20 (2008), pp. 1667–1669.

[17] Alexander W. Fang et al. "A distributed feedback silicon evanescent laser". In: *Opt. Express* 16.7 (2008), pp. 4413–4419.

[18] Alexander W Fang et al. "A continuous-wave hybrid AlGaInAs-silicon evanescent laser". In: *IEEE Photonics Technology Letters* 18.10 (2006), pp. 1143–1145.

[19] Alexander W Fang et al. "Electrically pumped hybrid AlGaInAs-silicon evanescent laser". In: *Optics express* 14.20 (2006), pp. 9203–9210.

[20] Roger Dangel et al. "Polymer waveguides for electro-optical integration in data centers and high-performance computers". In: *Optics express* 23.4 (2015), pp. 4736–4750.

[21] Jeong Hwan Song et al. "Practical design of lensed fibers for semiconductor laser packaging using laser welding technique". In: *Journal of Lightwave Technology* 27.11 (2009), pp. 1533–1539.

[22] Sharee J McNab, Nikolaj Moll, and Yurii A Vlasov. "Ultra-low loss photonic integrated circuit with membrane-type photonic crystal waveguides". In: *Optics express* 11.22 (2003), pp. 2927–2939.

[23] Andrew Huang et al. "A 10Gb/s photonic modulator and WDM MUX/DEMUX integrated with electronics in 0.13/spl mu/m SOI CMOS". In: *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International*. IEEE. 2006, pp. 922–929.

[24] Nobuaki Hatori et al. "A hybrid integrated light source on a silicon platform using a trident spot-size converter". In: *Journal of Lightwave Technology* 32.7 (2014), pp. 1329–1336.

[25] Jin-Hyoung Lee et al. "Demonstration of 12.2% wall plug efficiency in uncooled single mode external-cavity tunable Si/III-V hybrid laser". In: *Optics express* 23.9 (2015), pp. 12079–12088.

[26] M Lamponi et al. "Low-threshold heterogeneously integrated InP/SOI lasers with a double adiabatic taper coupler". In: *IEEE photonics technology letters* 24.1 (2012), pp. 76–78.

[27] Riccardo Marchetti et al. "Coupling Strategies for Silicon Photonics Integrated Chips". In: ().

[28] Takanori Shimizu et al. "High density hybrid integrated light source with a laser diode array on a silicon optical waveguide platform for inter-chip optical interconnection". In: *8th IEEE International Conference on Group IV Photonics*. IEEE. 2011, pp. 181–183.

[29] Ricky Tseng et al. "Laser integration with CMOS assembly process for Si photonics". In: *Optical Fiber Communications Conference and Exhibition (OFC), 2014*. IEEE. 2014, pp. 1–3.

[30] Bradley Snyder and Peter O'Brien. "Planar fiber packaging method for silicon photonic integrated circuits". In: *Optical Fiber Communication Conference*. Optical Society of America. 2012, OM2E–5.

[31] Chao Li et al. "Silicon photonics packaging with lateral fiber coupling to apodized grating coupler embedded circuit". In: *Optics express* 22.20 (2014), pp. 24235–24240.

[32] Alex A Behfar, Malcolm R Green, and Cristian Stagarescu. *Edge-emitting etched-facet lasers*. US Patent 9,893,488. Feb. 2018.

[33] AJ Zilkie et al. "Power-efficient III-V/Silicon external cavity DBR lasers". In: *Optics express* 20.21 (2012), pp. 23456–23462.

[34] Shiyun Lin et al. "Vertical-coupled high-efficiency tunable III-V-CMOS SOI hybrid external-cavity laser". In: *Optics express* 21.26 (2013), pp. 32425–32431.

[35] Yasuhiko Aoki et al. "Micro-optical bench for alignment-free optical coupling". In: *Applied Optics* 38.6 (1999), pp. 963–965.

[36] Simone Iadanza et al. "Thermally stable hybrid cavity laser based on silicon nitride gratings". In: *Applied optics* 57.22 (2018), E218–E223.

[37] Sebastian Lourdudoss. "Heteroepitaxy and selective area heteroepitaxy for silicon photonics". In: *Current Opinion in Solid State and Materials Science* 16.2 (2012), pp. 91–99.

[38] Alan Y Liu and John Bowers. "Photonic Integration With Epitaxial III–V on Silicon". In: *IEEE Journal of Selected Topics in Quantum Electronics* 24.6 (2018), pp. 1–12.

[39] Rodolfo E Camacho-Aguilera et al. "An electrically pumped germanium laser". In: *Optics express* 20.10 (2012), pp. 11316–11320.

[40] Clement Merckling et al. "Selective-area metal organic vapor-phase epitaxy of III-V on Si: What about defect density?" In: *ECS Transactions* 64.6 (2014), pp. 513–521.

[41] Weiming Guo et al. "Selective metal-organic chemical vapor deposition growth of high quality GaAs on Si (001)". In: *Applied Physics Letters* 105.6 (2014), p. 062101.

[42] Clement Merckling et al. "Heteroepitaxy of InP on Si (001) by selective-area metal organic vapor-phase epitaxy in sub-50 nm width trenches: The role of the nucleation layer and the recess engineering". In: *Journal of Applied Physics* 115.2 (2014), p. 023710.

[43] Zhechao Wang et al. "Room-temperature InP distributed feedback laser array directly grown on silicon". In: *Nature Photonics* 9.12 (2015), p. 837.

[44] Di Liang and John E Bowers. "Recent progress in lasers on silicon". In: *Nature Photonics* 4.8 (2010), p. 511.

[45] N Hossain et al. "Reduced threshold current dilute nitride Ga (NAsP)/GaP quantum well lasers grown by MOVPE". In: *Electronics Letters* 47.16 (2011), pp. 931–933.

[46] Jean-Rémy Reboul et al. "Continuous-wave operation above room temperature of GaSb-based laser diodes grown on Si". In: *Applied Physics Letters* 99.12 (2011), p. 121113.

[47] Daisuke Inoue et al. "Directly modulated 1.3 μm quantum dot lasers epitaxially grown on silicon". In: *Optics Express* 26.6 (2018), pp. 7022–7033.

[48] Bei Shi et al. "1.5 μm Room-Temperature Electrically Pumped Quantum Dot Lasers Monolithically Grown on Exact (001) Si". In: *2018 IEEE International Semiconductor Laser Conference (ISLC)*. IEEE. 2018, pp. 1–2.

[49] Alan Y Liu et al. "Quantum dot lasers for silicon photonics". In: *Photonics Research* 3.5 (2015), B1–B9.

[50] Zhechao Wang et al. "Polytypic InP nanolaser monolithically integrated on (001) silicon". In: *Nano letters* 13.11 (2013), pp. 5063–5069.

[51] Alan Y Liu et al. "High performance continuous wave 1.3 μ m quantum dot lasers on silicon". In: *Applied Physics Letters* 104.4 (2014), p. 041104.

[52] Qiang Li and Kei May Lau. "Epitaxial growth of highly mismatched III-V materials on (001) silicon for electronics and optoelectronics". In: *Progress in Crystal Growth and Characterization of Materials* 63.4 (2017), pp. 105–120.

[53] B Kunert et al. "III/V nano ridge structures for optical applications on patterned 300 mm silicon substrate". In: *Applied Physics Letters* 109.9 (2016), p. 091101.

[54] Ludovico Megalini et al. "Large-area direct hetero-epitaxial growth of 1550-nm ingaasp multi-quantum-well structures on patterned exact-oriented (001) silicon substrates by metal organic chemical vapor deposition". In: *Journal of Electronic Materials* 47.2 (2018), pp. 982–987.

[55] Ludovico Megalini et al. "1550-nm InGaAsP multi-quantum-well structures selectively grown on v-groove-patterned SOI substrates". In: *Applied Physics Letters* 111.3 (2017), p. 032105.

[56] Zhechao Wang et al. "Novel light source integration approaches for silicon photonics". In: *Laser & Photonics Reviews* 11.4 (2017), p. 1700063.

[57] Helene Duprez et al. "1310 nm hybrid InP/InGaAsP on silicon distributed feedback laser with high side-mode suppression ratio". In: *Optics express* 23.7 (2015), pp. 8489–8497.

[58] Guang-Hua Duan et al. "Hybrid III–V on Silicon Lasers for Photonic Integrated Circuits on Silicon". In: *IEEE Journal of selected topics in quantum electronics* 20.4 (2014), pp. 158–170.

[59] B Ben Bakir et al. "Electrically driven hybrid Si/III-V lasers based on adiabatic mode transformers". In: *Silicon Photonics and Photonic Integrated Circuits II*. Vol. 7719. International Society for Optics and Photonics. 2010, 77191F.

[60] Badhise Ben Bakir et al. "Electrically driven hybrid Si/III-V Fabry-Pérot lasers based on adiabatic mode transformers". In: *Optics express* 19.11 (2011), pp. 10317–10325.

[61] Badhise Ben Bakir et al. "Hybrid Si/III–V lasers with adiabatic coupling". In: *Group IV Photonics (GFP), 2011 8th IEEE International Conference on*. IEEE. 2011, pp. 169–171.

[62] Shahram Keyvaninia et al. "Demonstration of a heterogeneously integrated III-V/SOI single wavelength tunable laser". In: *Optics express* 21.3 (2013), pp. 3784–3792.

[63] Shuyu Yang et al. "A single adiabatic microring-based laser in 220 nm silicon-on-insulator". In: *Optics express* 22.1 (2014), pp. 1172–1180.

[64] Jing Zhang et al. "Transfer-printing-based integration of a III-V-on-silicon distributed feedback laser". In: *Optics express* 26.7 (2018), pp. 8821–8830.

[65] Andreas De Groote et al. "Transfer-printing-based integration of single-mode waveguide-coupled III-V-on-silicon broadband light emitters". In: *Optics Express* 24.13 (2016), pp. 13754–13762.

[66] Günther Roelkens et al. "III-V/Si photonics by die-to-wafer bonding". In: *Materials Today* 10.7-8 (2007), pp. 36–43.

[67] Günther Roelkens et al. "Laser emission and photodetection in an InP/InGaAsP layer integrated on and coupled to a Silicon-on-Insulator waveguide circuit". In: *Optics express* 14.18 (2006), pp. 8154–8159.

[68] Timothy Creazzo et al. "Integrated tunable CMOS laser". In: *Optics express* 21.23 (2013), pp. 28048–28053.

[69] Elton Marchena et al. "Integrated tunable CMOS laser for Si photonics". In: *2013 Optical Fiber Communication Conference and Exposition and the National Fiber Optic Engineers Conference (OFC/NFOEC)*. IEEE. 2013, pp. 1–3.

[70] David Gomez et al. "Process capability and elastomer stamp lifetime in micro transfer printing". In: *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*. IEEE. 2016, pp. 680–687.

[71] *Micro-transfer printing for advanced scalable hybrid photonic integration*. Vol. 5. Valencia, Spain, 2018.

[72] Joan Juvert et al. "Integration of etched facet, electrically pumped, C-band Fabry-Pérot lasers on a silicon photonic integrated circuit by transfer printing". In: *Optics express* 26.17 (2018), pp. 21443–21454.

[73] Photon Design. *FIMMWAVE, A powerful waveguide mode solver*. 2019. URL: `https://www.photond.com/products/fimmwave.htm` (visited on 07/21/2019).

[74] Brian Corbett et al. "Transfer Printing for Silicon Photonics". In: *Semiconductors and Semimetals*. Elsevier, 2018, pp. 43–70.

[75] Lei Liu et al. "Low-power-consumption optical interconnect on silicon by transfer-printing for used in opto-isolators". In: *Journal of Physics D: Applied Physics* 52.6 (2018), p. 064001.

[76] Lei Liu et al. "On-chip optical interconnect on silicon by transfer printing". In: *2018 Conference on Lasers and Electro-Optics (CLEO)*. IEEE. 2018, pp. 1–2.

[77] Bowen Song et al. "3D integrated hybrid silicon laser". In: *Optics express* 24.10 (2016), pp. 10435–10444.

[78] Xuezhe Zheng et al. "III-V/Si hybrid laser arrays using back end of the line (BEOL) integration". In: *IEEE Journal of Selected Topics in Quantum Electronics* 22.6 (2016), pp. 204–217.

[79] KS Kaur et al. "Flip-chip assembly of VCSELs to silicon grating couplers via laser fabricated SU8 prisms". In: *Optics express* 23.22 (2015), pp. 28264–28270.

[80] James Ferrara et al. "Heterogeneously integrated long-wavelength VCSEL using silicon high contrast grating on an SOI substrate". In: *Optics express* 23.3 (2015), pp. 2512–2523.

[81] Huihui Lu et al. "Flip-chip integration of tilted VCSELs onto a silicon photonic integrated circuit". In: *Optics express* 24.15 (2016), pp. 16258–16266.

[82] Günther Roelkens et al. "III-V/silicon photonics for on-chip and intra-chip optical interconnects". In: *Laser & Photonics Reviews* 4.6 (2010), pp. 751–779.

[83] Matthew A Meitl et al. "Transfer printing by kinetic control of adhesion to an elastomeric stamp". In: *Nature materials* 5.1 (2006), p. 33.

[84] Christopher A Bower et al. "Emissive displays with transfer-printed assemblies of 8 μm$\times$ 15 μm inorganic light-emitting diodes". In: *Photonics Research* 5.2 (2017), A23–A29.

[85] John Justice et al. "Wafer-scale integration of group III–V lasers on silicon using transfer printing of epitaxial layers". In: *Nature Photonics* 6.9 (2012), p. 610.

[86] Brian Corbett et al. "Transfer print techniques for heterogeneous integration of photonic components". In: *Progress in Quantum Electronics* 52 (2017), pp. 1–17.

[87] Ruggero Loi et al. "Transfer printing of AlGaInAs/InP etched facet lasers to Si substrates". In: *IEEE Photonics Journal* 8.6 (2016), pp. 1–10.

[88] Jongseung Yoon et al. "Heterogeneously integrated optoelectronic devices enabled by micro-transfer printing". In: *Advanced Optical Materials* 3.10 (2015), pp. 1313–1335.

[89] Tae-Ho Kim et al. "Kinetically controlled, adhesiveless transfer printing using microstructured stamps". In: *Applied Physics Letters* 94.11 (2009), p. 113502.

[90] Andrew Carlson et al. "Shear-enhanced adhesiveless transfer printing for use in deterministic materials assembly". In: *Applied Physics Letters* 98.26 (2011), p. 264104.

[91] X-Celeprint Ltd. *X-Celeprint Ltd.* 2019. URL: `https://x-celeprint.com/` (visited on 07/21/2019).

[92] COGNEX Corporation. *VISIONPRO, PC-based vision software for the most challenging 2D and 3D vision applications*. 2019. URL: `https://www.cognex.com/products/machine-vision/vision-software/visionpro-software` (visited on 08/18/2019).

[93] Nan Ye et al. "Transfer print integration of waveguide-coupled germanium photodiodes onto passive silicon photonic ICs". In: *Journal of Lightwave Technology* 36.5 (2018), pp. 1249–1254.

[94] John McPhillimy et al. "High accuracy transfer printing of single-mode membrane silicon photonic devices". In: *Optics express* 26.13 (2018), pp. 16679–16688.

[95] B Guilhabert et al. "Hybrid integration of an evanescently coupled AlGaAs microdisk resonator with a silicon waveguide by nanoscale-accuracy transfer printing". In: *Optics letters* 43.20 (2018), pp. 4883–4886.

Chapter 3

Transfer printing of InP lasers

The process of transfer printing a device to a new substrate is simple in principle, it consists in picking-up a pre-released device from the starting wafer, transferring it to the new substrate and printing it to the desired location. However, the different steps involved in making a device transfer printable, the preparation of the hosting substrate and the alignment of the waveguides require a large number of optimization experiments. The type of light coupling between the device and the photonic circuit requires the coupon geometry to match the printing location on the hosting substrate or the printing location to be designed for accommodating the device. Particular attention must be paid to the flatness and smoothness of the mating surfaces and to stress acting on the coupons to avoid complications in the μTP process. The alignment of the devices can be achieved visually by the operator at the transfer printer, the accuracy can be improved by using fiducial markers and optical pattern recognition [1].

In this chapter are described the methods for achieving a transfer printable InP ridge laser with etched facet, suitable for heterogeneous integration to silicon photonics end edge-coupling to the SOI waveguide. The main concepts behind a successful approach to device fabrication and integration on different substrates are outlined, the suitable epitaxial structure, the design and the fabrication of the lasers, the wet-etching technology developed for the release of the devices from the original wafer, the transfer printing and the post printing steps are discussed in their technological aspects.

3.1 Transfer printable InP Lasers

Transfer printing make possible to achieve new systems and layouts in photonics. Large arrays of devices can be integrated in parallel and in dedicated spots with $<\pm 1.5$ μm alignment (3σ) along the printing plane [1]. The devices can be completely pre-fabricated and pre-tested before transfer, or as

an alternative it is possible to transfer dies that can be processed after print. All these features make μTP very attractive for the integration of InP lasers to silicon photonics.

Transfer printable lasers, as other transfer printable devices or dies, have to be fabricated inside coupons and require the inclusion of a sacrificial layer in the epitaxial structure of the wafer to allow the separation from the source wafer. The fabrication must include an encapsulating layer to protect the coupons from being etched during the release by wet-etch. The development of a wet-etch undercut technology for the erosion of the sacrificial layer with high selectivity to the surrounding materials and the engineering of a proper anchor system able to restrain the coupons on the original substrate during the undercut have taken most of the efforts in the development of a μTP technology for InP. A grating-like structure is typically defined on the sacrificial layer around the coupons to provide multiple starting points to the etchant (see section 3.2.1 for more details about the grating). The suspended coupon resulting after the undercut can be then picked-up and transfer-printed to the new substrate. The overall process flow is shown schematically in Fig. 3.1.

Laser devices suitable for transfer printing and for edge-coupling to SOI waveguides have been developed and fabricated as arrays of ridge-waveguides in rectangular coupons (section 3.2). Different etching solutions were investigated in a range of temperatures and $FeCl_3$:H_2O (1:2) (Iron chloride) was proven to provide the best etch-rate to selectivity-to-InP ratio while still keeping the etch rate of InGaAs or InAlAs sacrificial layers high enough to allow the release of <120 μm wide coupon in few hours time [section 3.3]. The iron chloride etchant was compatible with the standard polymer used for the anchor system. A suitable anchor system for the devices has been engineered by investigating different tether shapes, dimensions and configurations, with the aim to achieve tethers that can break easily and cleanly when the device is picked up from the original wafer [section 3.2.5]. Finally, completely pre-fabricated and pre-tested InP devices were transferred to different non-native substrates by means of μTP with and without intermediate or adhesive layers [see section 3.4]. The strategy requires very little post-printing processing limited to the removal of the anchors. The methods for creating the lasers and transfer printing them are discussed more in detail in the next sections.

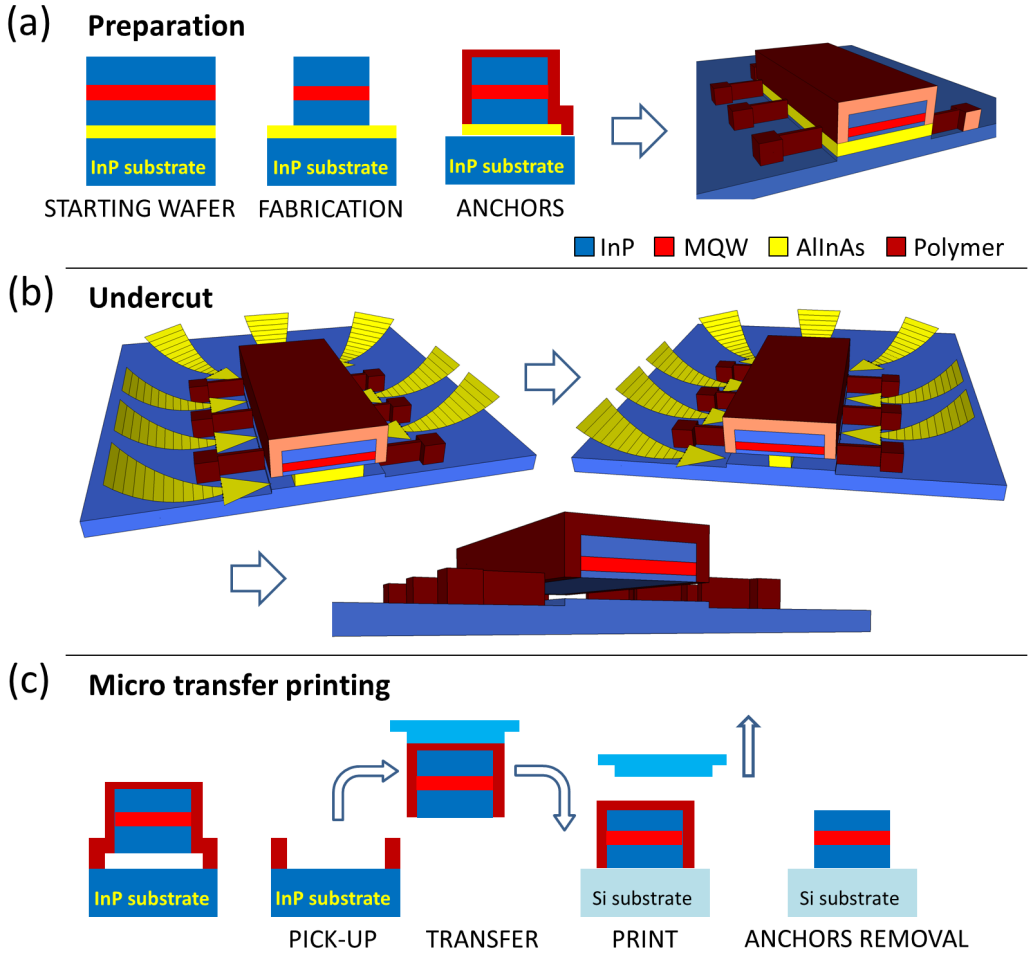


Figure 3.1: (a) Cross-section of a laser coupon fabricated on the InP wafer containing the InAlAs sacrificial layer and anchored to the substrate by a resist tether structure. (b) The undercut in $FeCl_3$:H_2O results in suspended coupons ready for micro-transfer-printing. (c) In μTP a PDMS stamp collects the pre-released devices from the original wafer and releases them to the target substrate. [2].

3.1.1 Epitaxial structure

InP based epitaxial laser structures including a lattice matched sacrificial layer were designed and fabricated in order to achieve transfer printable lasers. The laser epitaxial structures were grown by metal organic vapour phase epitaxy (MOVPE) with nitrogen as the carrier gas on a perfectly oriented (100) InP substrate [3], [4]. The wafers were designed and fabricated in a collaboration between the III-V materials and devices group and the Epitaxy group at Tyndall National Institute. The laser epitaxial structures developed in this work were grown on two main epitaxial release layers: a 1-μm-thick InGaAs or a 500 μm thick InAlAs sacrificial layers n-doped (1×10^{18} cm^{-3}). These layers were included between the substrate and the n-InP cladding layer of the laser to allow release the devices from the native wafer by means of a selective wet-etch [5]. The n-type doping makes the sacrificial layer electrically conductive in order to evaluate the lasers on the native substrate with a contact on the substrate side before the undercut. For the laser operating in the C-band of the optical spectrum, six 6-nm-thick compressively-strained AlInGaAs quantum wells and seven 10 nm thick tensile strained barriers form the 96 nm thick multi quantum well (MQW) active region in a step index waveguide of 336 nm total thickness (this number may vary, see appendix A). The waveguide is clad by 1.5-μm-thick n- and p- doped InP. A cap layer of p-doped InGaAs allows electrical contacting on the p-side. The bottom of the active region is 1615 nm from the sacrificial layer. The mode of a 2.5 μm wide ridge laser with the actual epitaxial structure was simulated with FIMMWAVE [6] [see section 5.1], [6]. The size of the transverse mode at 1/e of the intensity is $\sim$1 μm, with a mode overlap of 6.6 % with the quantum wells. The transverse mode reaches <0.5 μm into the InP cladding layers making the mode independent of the contact layer or features on the substrate side. This strategy makes this epitaxial structure particularly suited for either transferable devices and light edge coupling to the SOI. A p-doped InGaAs contact layer is finally grown at the top of the epitaxial structure to facilitate the creation of the electrical metal contact while reducing the diffusion of the metal into the semiconductor. The main laser epitaxial structures used in the experiments are reported in the appendix A at the end of the manuscript. All the laser epitaxial structures used in this work are similar and differ mainly in the sacrificial layer and the p-side layer structure in an attempt of creating a lower interface resistance.

A large spot size (LSS) laser epitaxial structure was grown for testing the

edge-coupling of InP devices to the SOI by integrating them inside recesses on the SOI wafer [7], [8]. The LSS laser structure has a lower light confinement along the epitaxial axis allowing for a larger mode size which increases the tolerances of the alignment between the laser and the SOI waveguides, especially along the vertical axis. The transfer printing principles and processing steps developed in this work were applied to the LSS laser to make it transfer printable. In addition, a number of epitaxial structures were grown by MOVPE on (100) perfectly oriented InP substrates ($\pm$ 0.1 degree angle) for the purposes of comparing between the different etch release layers and etchants. Each release layer (InGaAs, InAlAs) was 500 nm thick, n-doped (1×10^{18} cm^{-3}) with layers of InP adjacent to the release layer [5]. The overgrowth of the InAlAs layer was completed with a thin (10 nm) InGaAs layer to avoid aggregation issues and improve morphology of the InP [9], [10]. It was lately found that a 50-100 nm InGaAs buffer layer produces smoother released surfaces suitable for adhesive-less print.

3.2 Design and fabrication of the lasers

Dense arrays of Fabry-Perot lasers with up to 2000 devices per cm^2 on a fixed pitch are fabricated on the native InP substrate using lithography and anisotropic inductively coupled plasma (ICP) etching techniques to form the laser mirrors together with a conventional ridge waveguide. The lasers are fabricated as rectangular coupons with both anode and cathode on the epitaxial side [Fig. 3.2]. The resonating cavity for the light amplification is defined by the ridge that provides lateral light confinement, by the epitaxial structure refractive index gradient between cladding and active region which confines the light along the vertical direction and by two dry-etched facets positioned at the sidewalls of the coupon and perpendicularly to its longitudinal axis. The ridge extends to the edge of the facets with a V-shape so as to prevent the ridge etch from affecting the quality of the facet. The reduction in effective facet reflectivity due to diffraction in the tapered region is numerically calculated with FIMMWAVE to be 0.9 % [6]. The facets create a suitable arrangement for edge-coupling of the light to SOI or polymer waveguides on photonics platforms (see details about facets in 3.1.4). The lasers are completely pre-fabricated and can be tested before the release from the original InP substrate and after printing to an hosting substrate. They can be probed from the top or through an electrically conductive substrate when printed in direct contact to it, with a penalty of only few Ohms

on the series resistance. The choice of having a completely pre-fabricated and pre-tested device is based on the known good die approach which was considered very important in the context of an heterogeneous laser for silicon photonics. In fact, the approach improves the yield of integrated working lasers reducing the post-printing processing to minimum which turns in lower risk of damaging the hosting platform.

The lasers were designed as rectangular coupons 500 to 1000 μm long and 40 to 120 μm wide. Most of the devices tested were 500×60 μm^2, these dimensions provide a good balance between light amplification and thermal sink and provide reduced foot print compared to other light sources for silicon photonics [11], [12]. In the designs developed, one or more elements that constitute a laser can be defined separately or in the same lithography level. Different designs were explored in order to find out a suitable arrangement of the different components and the inclusion of the micro transfer printing preparation steps. Such type of lasers are generally composed by specific elements which must be defined inside a coupon:

- **Ridge waveguide**: for lateral light confinement.
- **Coupon profile, facets, n-recess**: define the coupon shape, the mirrors, and a access to the n-InP layer respectively.
- **p- and n- metal contacts**: for contacting the p-i-n junction.
- μTP elements:
  - **Encapsulation structure**: for protection of the sidewalls and facets.
  - **Grating structure**: on the sacrificial layer to give the etchant a starting point for the erosion.
  - **Anchor system**: to restrain the coupon to the substrate during the undercut.

The ability of the process designer resides in finding the combination which requires the lowest number of processing steps, which is usually related to the number of lithographies and the order they are arranged in the process. The main differences between the process-designs studied were related to the number of lithography steps, to the number of device-components defined in each level and to the geometry of the elements. Geometry variations were studied especially for probing pads and anchors. All the designs include transmission line measurements (TLM) patterns for

the p-metal contact evaluation and some mesas of different width without anchors for the evaluation of the undercut progress during the release.

3.2.1 Laser fabrication process

Initially, a nine-level lithography process was developed to realize lasers suitable for transfer printing. Other processes have been created by the same lithography levels defining them in different order; this permits to achieve different configurations of the final device. Additional masks were designed to separate some of the device-elements in different lithography levels. The process starts with the removal of native oxides on the starting InP wafer and the evaporation of a Ti:Au (10 nm : 110 nm) metal layer that defines a 1.5 μm wide and 490 μm long p-type contact. Next, a 2.5-μm waveguide ridge is defined by creating two trenches running parallel each other along the longitudinal axis of the coupon. The ridge depth is about 1.5 μm and stops before the MQW active region in order to control the optical confinement and losses while minimizing the current leakage. The ridge structure can be defined in the centre of the coupon with the 2 n-metal contacts parallel to it along the longitudinal axis of the coupon. This configuration provides a more symmetrical current injection improving electro-optical and thermal performances, but then it can be difficult to arrange probing pads of suitable area in coupons narrower than 60 μm. Next, a $Cl_2/CH_4/H_2$ ICP dry-etch defines the facets for the Fabry-Perot laser cavity together with the rectangular coupon profiles and a recess for the n-contact [Fig. 3.2]. These elements can be joined to the coupon profile definition or separated from each other if more flexibility in the etch depths is desired. The recesses reduce the flexural modulus of the coupons, so it is important to find a balance between correct area for the n-current flow and stiffness of the coupons which can become more sensitive to the stress produced by passivation layers. A flat evaporation of a Au:Ge:Au:Ni:Au (14 nm : 14 nm : 14 nm : 11 nm : 200 nm) metal layer defines the n-contact on the devices. Rapid thermal annealing (RTA) at 390 °C for 5 minutes was required to form a low resistance ohmic contact to the n-type InP layer.

An important componenent of the transfer printable devices is the encapsulation insulating layer, usually a SiN or a SiO_2 layer applied by Plasma-enhanced chemical vapor deposition (PECVD), which protects the epitaxial structure at the sidewalls and consequently the facets from oxidation and erosion during the wet-etches. The correspondent lithography level defines

a 2.5 μm large ledge around the coupon on a oxide layer sealing the coupon down to the n-InP layer. Next, a metal evaporation provides contact pads for electrical characterization. A final ICP dry-etch through the sacrificial layer reaches the InP substrate. A coarse grating shaping of the sacrificial layer around the coupons prevents the polymer layer for the anchor system to cover the sidewalls of the sacrificial layer in between the tethers. The resist is exposed in correspondance of the tips of the grating providing a starting location to the etchant for the erosion of the sacrificial layer, the shape of the grating also helps to manage the profile of the etch front. The grating is composed of 15 $\times$ 2.5 μm^2 tips arranged around the coupon on a 40 μm pitch [Fig. 3.3]. Finally, a 2.8 μm thick resist layer is patterned with tethers to anchor the mesas to the substrate during the undercut step. The polymer anchors give an additional protective layer to the coupon encapsulation and need to withstand the etchant attack and the capillary forces acting underneath the coupons during the undercut, rinse or drying steps. The polymer anchor system is usually composed by an array of tethers arranged around the coupon at a constant pitch, shape and dimension of the tethers are discussed more in detail in section 3.2.5. The spacing between one tether and the next allow the etchant to penetrate underneath the coupons.

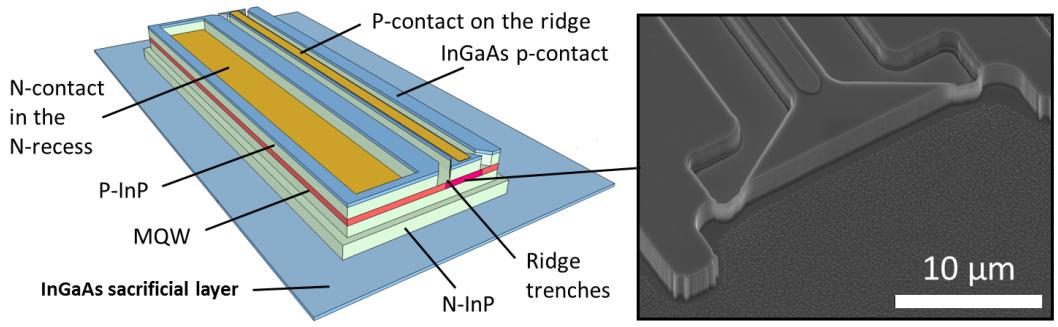


Figure 3.2: Schematic of the laser geometry used before etching through the sacrificial layer; p- and the n-contact are on the epitaxial side of the device. The right-hand side shows the scanning electron microscope (SEM) image of an etched facet prior to its passivation. [13].

3.2.2 Different geometries of the devices

The devices have been designed with different areas and pads geometries [Fig. 3.4(a) - (g)]. Most of the layouts explored have proven to provide working devices which can be easily probed [Fig. 3.4(a), (d), (f), (g)]; some other were more difficult to probe because of the geometry of the probing pads or have shown bad electrical contacts. For example, if the pads are

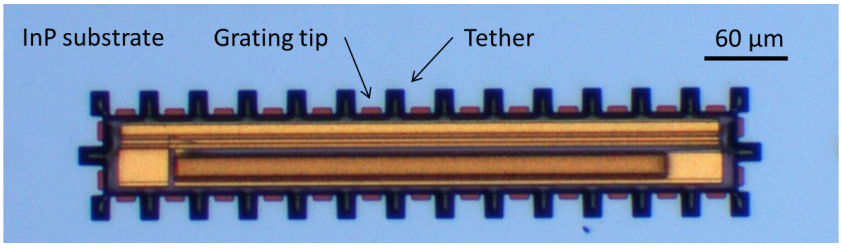


Figure 3.3: Top view of a laser coupon ready for undercut with the polymer anchor system in place. The grating offer multiple starting points for the etchant around the coupon. The tips of the grating are visible between the tethers. [13].

closer than 10 μm to each other and the lift-off is not perfectly developed, considering the pads are usually created by a 360 degree evaporation there will be some enlargement of the pad-shape which will create a short circuit between the p- and the n- pads [as for the layouts in Fig. 3.4 (b), (e)]. If the n-recess does not run along the whole length of the FP cavity the current flow will be negatively affected [Fig. 3.4 (f), (g)]. In the case the pads are deposited on an insulating layer deposited on top of one of the electrical contacts [Fig. 3.4(a), (d), (g)], then the insulating layer is required to be thicker than 100 nm in order to prevent short circuits between the pad and the underlying contact when probing with needles, and for preventing the creation of high capacitances. When one of the facets is incorporated inside the coupon a beam splitter can be arranged to prevent back reflections that could affect the emission spectrum of the laser [Fig. 3.4(c) - (g)].

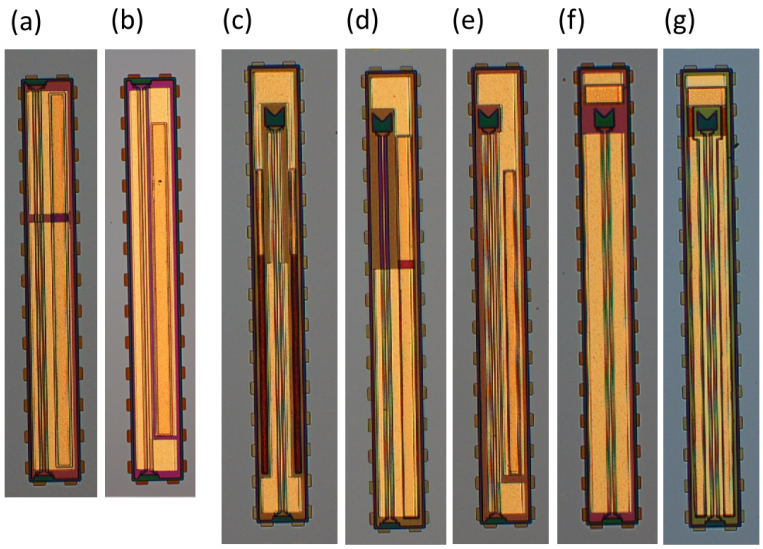


Figure 3.4: Example of the different layout explored for the contacting pads. all these devices have two emitting facets, when one of the facet is accommodated inside the coupon (c, d, e, f) a beam splitter is inserted to prevent double back reflection out of phase.

Metal pad layout	Advantage	Penalty
Probing ease	a, c, d, e	b, f, g
Fabrication complexity	a, f	b, c, e, g
Beam splitter at one facet	a, b	c, d, e, f, g
Proximity between contacts	a, c, d, f, g	b, e
Area in touch to the contacts	b, e	a, c, d, f, g
Overlap to the opposite contact	b, c, e, f	a, d, g
Series resistance	a, b, d, e	c, f, g
Symmetry of current flow	c, f, g	a, b, d, e

Table 3.1: Metal pads arrangement main features and influence on the device (as advantage or penalty) for the different the configurations reported in Fig. 3.4.

The standard process for transfer printable lasers (reported in Appendix B) has been evolved for creating a different encapsulation structure which gets rid of the encapsulation ledge and the grating around the coupons. This allows to achieve ledge-less devices which can be matched to a sidewall in the SOI and are suitable for light edge-coupling to a waveguide within the Rayleigh distance of the emitted light beam [7]. The same process requires a modified anchor system with tethers that start from the top of the coupon in order to allow the removal of the gratings structure on the sacrificial layer. The number of levels for fabricating a ridge laser with etched facets has been reduced down to 6 levels in this process. The process itself is reported in detail in Appendix C.

3.2.3 Stress management

When designing and fabricating a device is vital to keep in mind that the stress coming from the passivation and metal layers applied to the coupons needs to be kept at a minimum. In fact, if any compressive/tensile stress arises during the fabrication this could cause the passivation layers to delaminate [Fig. 3.5] or the devices to even break [Fig. 3.6] or to curl up after the release making the pick up and any adhesive-less printing impossible. In order to overcome this issue, the metal layer have minimal thickness and area, it is also possible to use tensile stressed passivation layers against compressive stressed layers or vice versa. Usually PECVD SiN and SiO_2 show tensile and compressive behaviour respectively, but these stress can change due to the stability issues of the process and the tool itself, it is then advisable to check regularly the value of the stress in order to achieve stress free

coupons. In order to overcome unexpected stress issues due to malfunctioning of the tool etc., it is always advisable to do an undercut test only on small part of the chip (which can be scribed from the main chip). If there are any stress problems the remaining chip can be recovered thinning the passivation layers or increasing the thickness of the resist layer for the anchors at the top of the coupons. In this case and if the actual anchor design is not suitable for the new resist thickness, the anchors lithography must be defined in two steps. First a rectangular area of resist has to be defined on top of the coupon, secondarily the anchor level has to be defined on top of it. The resolution of the tethers will be lower due to the increased step height to the substrate, but the anchors engineered in this work usually tolerate this step. Main issue for the printed devices is that they will tend to curl up once the anchors are removed, then the only way to print stressed devices is to use adhesive layers. Adhesive layers as BCB can be thinned down to a minimum and excellent adhesion and effective thermal sink can be achieved (see sections 3.4.3 and 4.3).

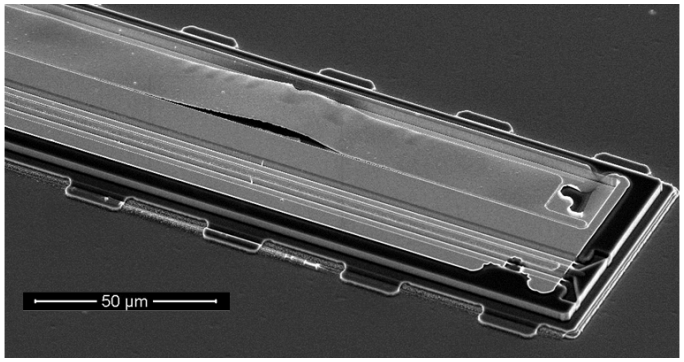


Figure 3.5: Coupon passivated with stressed sputtered SiO_2. The layer delaminated on top of the n-metal after the annealing of the contacts at the RTA.

3.2.4 Etched facets

Transfer printable lasers for edge-coupling of the light to the SOI require an emitting facet and a back reflector. The devices fabricated in this work use two of the sidewalls of the coupon as reflective facets to create a Fabry-Perot resonator. Use of etched facet technology offers many advantages, etched facets make the devices suitable for transfer printing as they prevent cleaving the original chip, this allows re-use the original InP substrate. Etched facets make the resonating cavity independent of the crystal direction and their reflectivity can be tuned by working on the thickness and the structure of the dielectric passivation layer. The passivation layer protects the devices

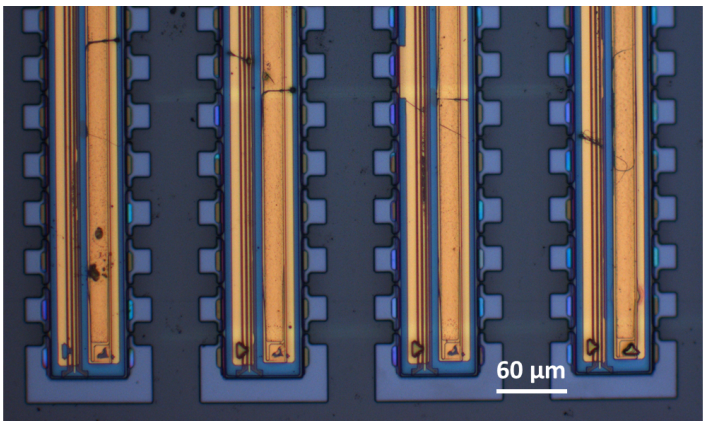


Figure 3.6: Coupons on chip and with the anchor system in place cracked after the undercut due to stressed passivation layer.

from erosion during the etch and allows them to operate in a non-hermetic environment. Metal layers can be deposited on top of the passivation for creating highly reflective (HR) coatings.

A facet must be as vertical, smooth and flat as possible in order to create a reflector that is as close as possible to the ideal mirror with resulting minimum losses [Fig. 3.7]. The state of the art literature indicates reflective dry-etched facets for semiconductor lasers have to reach verticality within θ<$\pm$1 degree angle, RMS roughness within S_q<5 nm and flatness f<5 nm/μm for <1 dB losses [14], [15], [16].

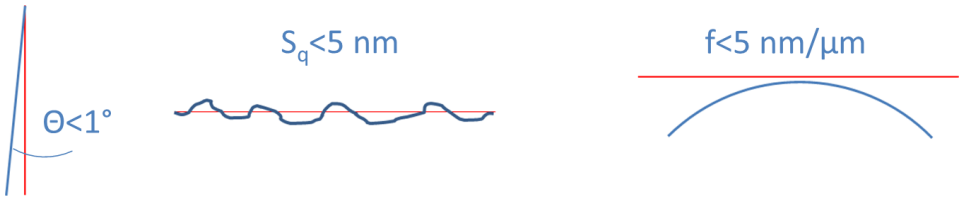


Figure 3.7: Quality of the dry-etched facets is determined by the verticality (a), the roughness (b) and the flatness (c) of the surface created.

Different fabrication processes have been investigated in order to achieve vertical, smooth and flat facets. The dry-etch facet is affected mainly by the hard mask used for defining the etch and by the etching parameters as the chemistry, the RF power and the temperature. A hard-mask with straight profiles, vertical walls and low roughness is needed to provide proper facets when etching the epitaxial structure. An optimization experiment was performed in order to determine the best process for creating facets. A SiO_2 layer was sputtered at room temperature on the InP wafer to create a 1 μm thick hard mask for the facet etch; the SiO_2 mask was patterned in different ways:

- Creating a 50 nm Cr mask patterned by:
  - A negative resist lift-off (Cr LO).
  - A positive resist plus a Cr wet-etch.
- Using AZ-5214 polymer as a positive resist to achieve a few degree angle negative slope sidewalls. This provides more vertical sidewall of the SiO_2 hard-mask.

A re-flow of the resist at 110 °C for 2 minutes for the definition of the chrome mask usually reduces curtain-like profiles of the oxide mask [Fig. 3.8]. A post processing treatment of the sidewalls of the SiO_2 hard mask in diluted BOE:H_2O (1:10) further reduces curtain effects. A possible solution of this issue is to define this level with an e-beam or with a deep ultraviolet (DUV) lithography, but these options were not investigated due to the acceptable quality of the facet fabricated. The most vertical, smooth and flat facets were achieved using the AZ resist for patterning the SiO_2 mask and a 30 s exposure to 1:10 diluted BOE:H_2O [Fig. 3.8]. The plasma etch for defining the SiO_2 mask was always operated with CF_4/CHF_3 based chemistry. A number of experiments allowed the determination of the optimal etching parameters.

The optimization of the facet passivation layer was fundamental for reducing the threshold current of the lasers developed; the initial configuration had both facets protected by a $\sim$300 nm thick SiO_2 or SiN layer and the threshold current for a 500 μm long 2.5 μm ridge laser printed on Si was $\geqslant$45 mA; the last laser with optimized facet reflectors shows a threshold current of $\sim$16 mA. The two facets work respectively as an emitter (partially reflective mirror) and as a highly reflective (HR) mirror. A SiO_2 protective passivation layer prevents the oxidation of the MQW region and must be deposited homogeneously while keeping the roughness as low as possible to prevent light losses due to non uniformity at the surface of the facet. The thickness of the SiO_2 layer is usually set to be neutral to the whole reflectivity of the facet with thickness $t \sim \lambda/2n$; However in the experiments performed during this work, passivation layers of thickness t<200 nm provide reduced roughness at the emitting facets resulting in reduced losses [Fig. 3.9]. The SiO_2 layer thickness was studied in order to obtain the maximum of reflectivity when introducing a HR metal coating at the rear facet and creating a fully reflective mirror. The reflectance of the facets at 1550 nm wavelength in air with and without an HR coating was simulated while varying

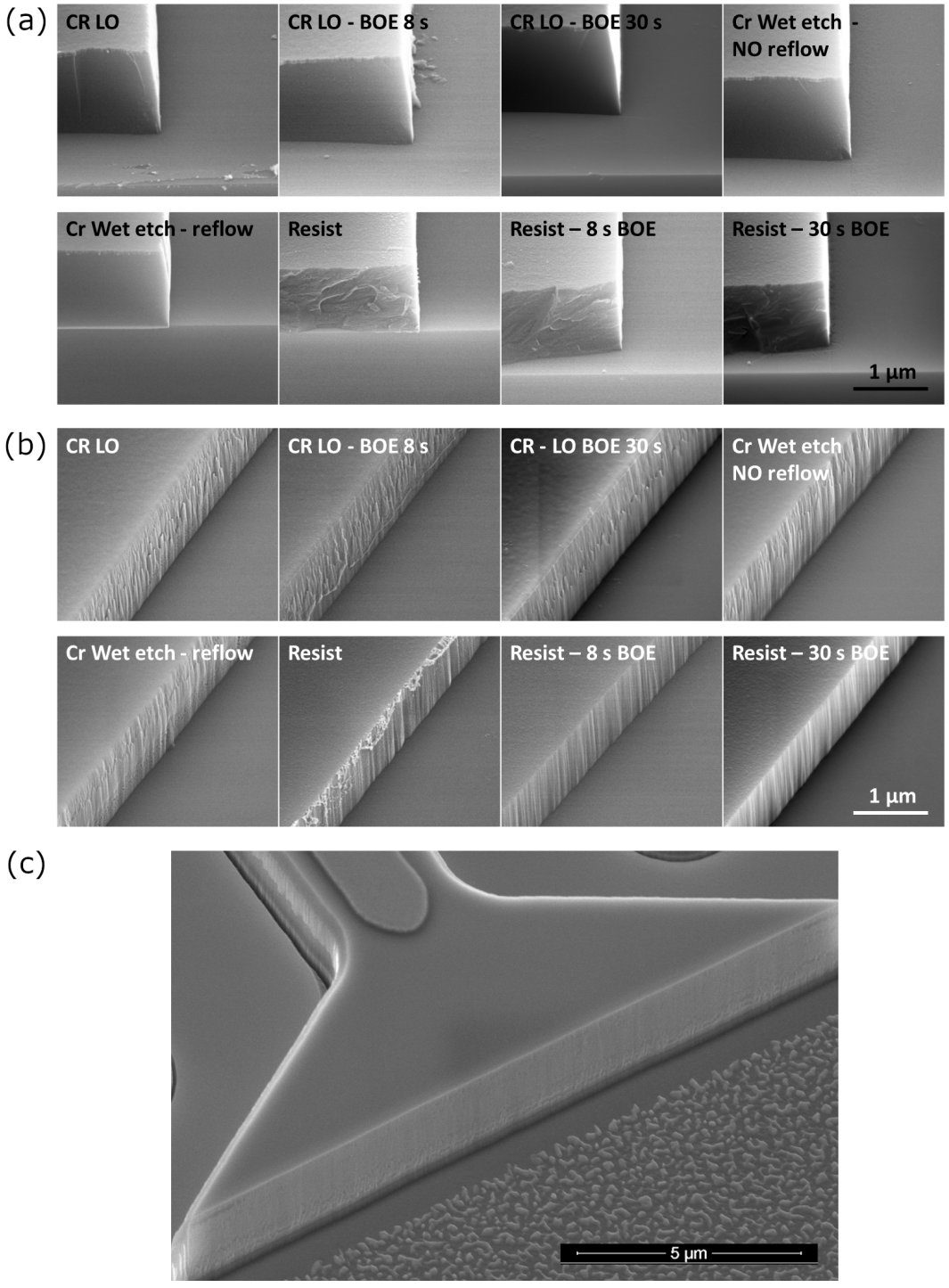


Figure 3.8: Scanning Electron Microscope image of the SiO_2 hard-mask sidewalls after dry-etching with CF_4/CHF_3 based chemistry. (a) The verticality and the (b) roughness of the sidewalls are different according to the type of mask used to pattern the hard-mask. (c) The best sidewall are obtained by patterning the SiO_2 hard-mask with a AZ5214 resist mask and etching it in diluted BOE:H_2O solution for about 30 s.

the SiO_2 passivation layer thickness [Fig. 3.10] by F. Floris and M.Passoni using the same scattering matrix model applied to other works [17], [18]. The metal layer evaporated on top of the SiO_2 passivation layer is a Ti:Au (5:110) nm and is kept fixed in the simulation. The thickness of the Ti layer has to be thin, due to the high absorption of this material, while providing adhesion to the Au layer. The main issue that is noticeable from the simulation is that the maximum of reflectivity for the emitting facet fits the min of the HR coated facet for a thickness of the SiO_2 passivation layer at $\lambda/2$. The simulations indicate that the highest reflectivity of the back mirror is achieved for a SiO_2 layer thickness between 50 nm < t < 100 nm. A thin SiO_2 passivation layer helps reducing the roughness at the facets while allowing to use a thin Ti adhesive layer for the HR Au layer deposition. Given the previous considerations, the thickness of the SiO_2 passivation has been set at about 100 nm to achieve the maximum of reflectivity of the HR metal coating at the rear facet and a good reflectivity at the front facet. A thickness of the passivation layer of ∼290 nm should provide low reflectivity of the emitting facet of R ∼10 % with a reflectivity of R>80 % at the back mirror, this configuration could be to implement a laser edge-coupled to the SOI with a DBR mirror on the SOI (as described in section 2.1.4).

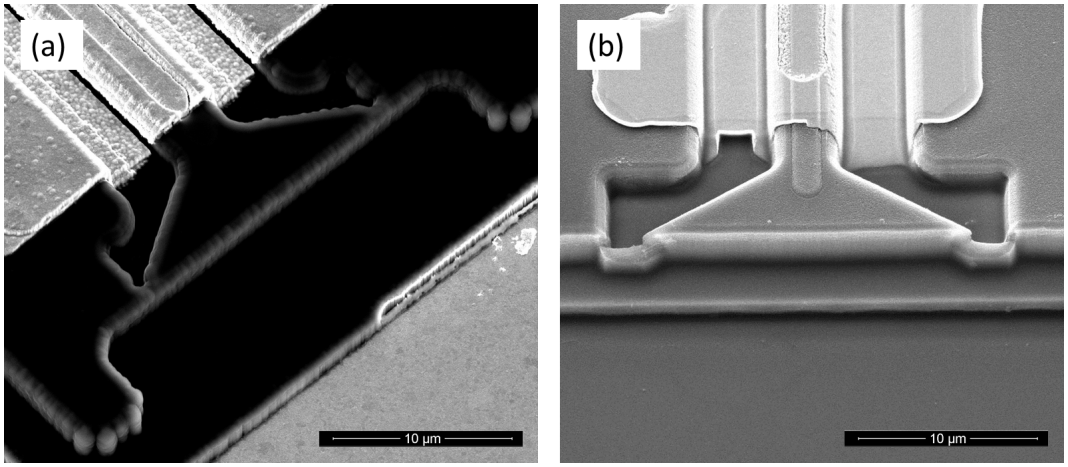


Figure 3.9: Facets with thick passivation layer show very rough surfaces compared to facets covered by a thin passivation layer.

Multi mode interferometer back reflector (MIR)

The fabrication of a multi mode interferometer (MMI) reflector (MIR) was investigated as an alternative of the HR back reflector. Different MIRs were fabricated for different ridge width W_r of the laser. The width of the MIR must be W ∼2·W_r [19], [20], [21]. Considering the length of the MIR can

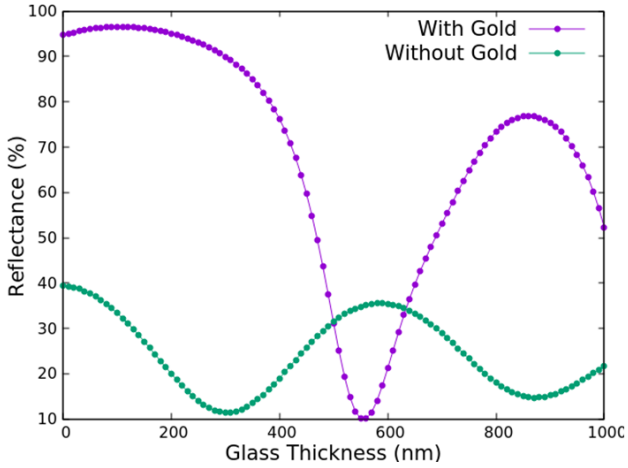


Figure 3.10: Reflectance dependence on the SiO_2 layer thickness at the emitting and at the rear facet when layered by an HR coating.

be approximated as $L \approx W^2$ this type of reflector would be not suitable for wide multimode ridges as the resulting footprint would be quite large for a transfer printable laser coupon; a 5 μm ridge would give a 100 μm long MIR. In the case of a 500 μm long single mode laser of W_r<2.5 μm, the length of the MIR is L<16 μm which does not alter much the length of the laser coupon. The outcome of this experiment was a partial fail due to difficulties in electrically probing the MIR section to make it optically neutral and because of the roughness at the reflective facets at the tip of the MIR that are not suitable for creating an effective mirror with reflectivity comparable to that of an HR coated facet. The reflectivity of the MIR for a 2.5 μm ridges was estimated from the threshold current to be R ~30% when passive. R is comparable to that of a dry-etched facet in air, but way far from the expected values simulated by Morrissey et al. of R>90 % [19].

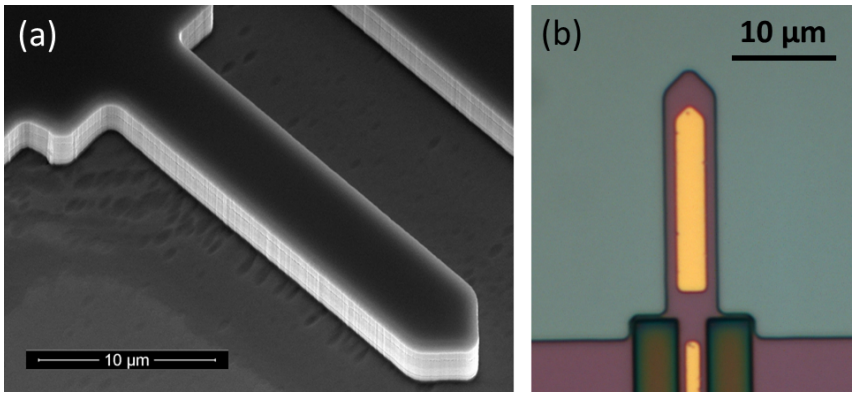


Figure 3.11: (a) SEM image of one of the MIR structures and (b) digital microscope image of a complete MIR for a 2.5 μm wide ridge waveguide, the reflectivity of the MIR is comparable to that of a standard emitting facet (R ~30%).

3.2.5 Anchor system

A vital part of the transfer printing is the anchor system which keeps the devices stable in place during the release from the original substrate. A typical anchor system is formed by a number of tethers arranged around the coupon at fixed pitch that hold it to the substrate. These structures have one end connected to the coupon and the other to the substrate (named foot or paw). During the undercut, the coupons are subject to capillary forces acting especially underneath them where the erosion of the sacrificial layer takes place. This is due to the thickness of the sacrificial layer which is usually 0.5 μm to 1 μm so within the action range of these forces. It is very important to hold the coupons steady during the undercut in order to prevent defect creation at the bottom surface. In fact, especially at the end of the release, the small pillars of remaining material of the sacrificial layer can break under stress action and detach part of the surrounding layers creating a series of pinholes at the bottom of the coupons, the so called "pitting" effect [Fig. 3.12]. The anchor system can be formed by a dielectric layer or by a polymer shaped in tethers that can break easily and cleanly when the device is picked up from the original wafer. The dielectric materials used for the anchors are SiN or SiO_2 and are recently receiving more attention than the polymers as they offer higher control of the mechanical properties. The polymer based materials investigated in this work are standard resists for lithography as S1828, S1813, SPR. The S1828 has been chosen as material for the development of the anchor system for the lasers due to the thickness being suitable for up to 5 μm thick coupons. The stress introduced by resist layers is usually lower than the flexural strength of the InP coupons, however thick resist layers can introduce stress that deform the coupons and create defects at the released surface as described above. The material can be patterned by UV lithography and is made stiffer and more brittle by a hard-bake at 125 °C. A suitable anchor system for the devices involved has been engineered starting from an investigation of different tether shapes, dimensions and configurations [Fig. 3.13] [22].

The tether must be easy to break while holding the coupon stable to the substrate, a high number of small tethers is then preferable to few big tethers that offer bigger lever to the coupon and then lower stability when the coupon is subject to forces. The experiments show few important guidelines to be followed when designing a new anchor system. First, the number of tether depends on the area of the coupon in order to withstand different capillary forces; second, the tether must be shaped as a large foot with a thinner

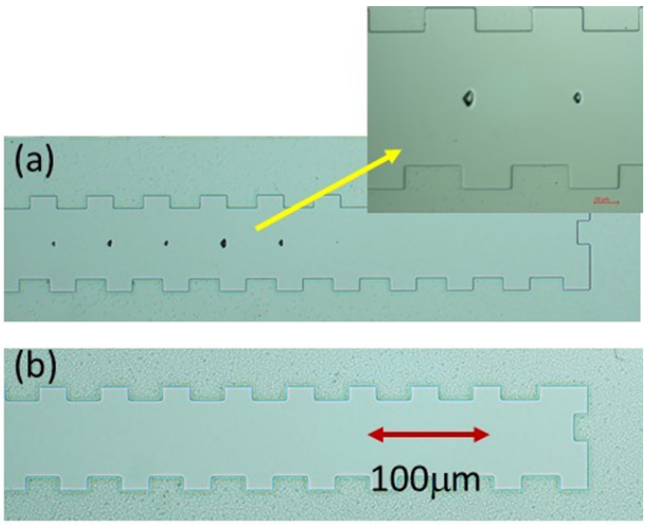


Figure 3.12: (a) Digital microscope images of stress induced pillars created on the released area of the substrate after undercutting a coupon encapsulated with a stressed layer. The same defects are present at the bottom of the released coupon. (b) clean surface achieved after the undercut of a coupon encapsulated by a stress free layer. [22].

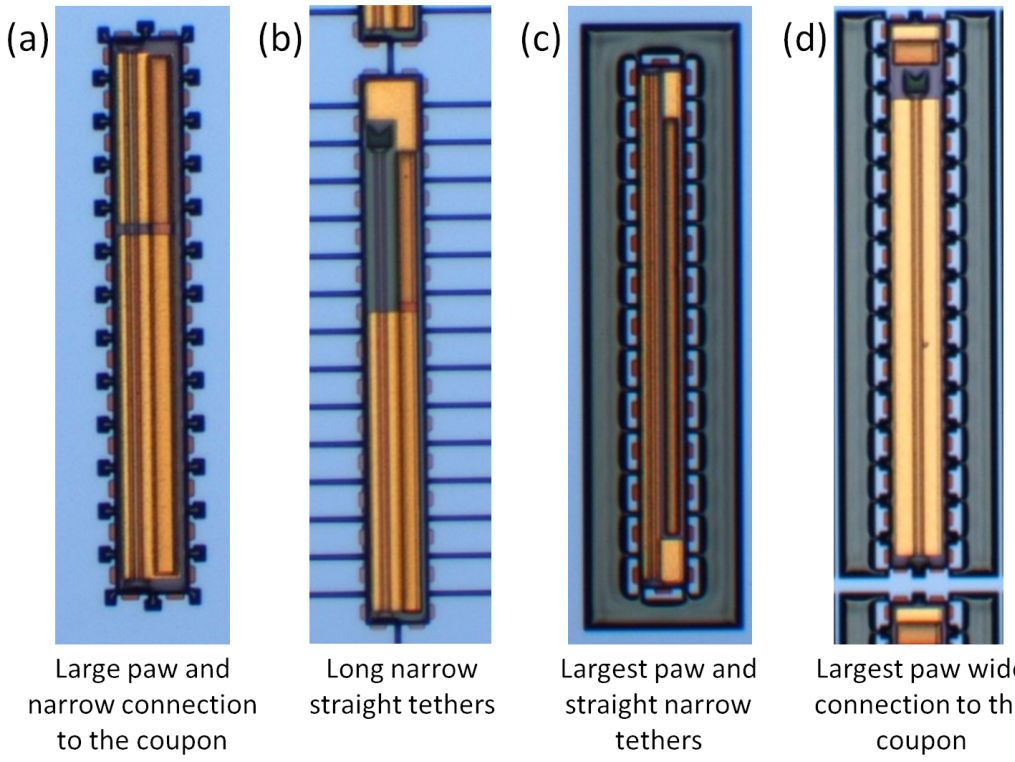


Figure 3.13: Optical microscope images of 60 μm and 40 μm wide laser coupons having different anchor geometries. (a) A tether with a large end (paw) ensures better adhesion to the substrate and breake close to the coupon. (b) long straight tethers can retain flaps which create high level of debris and disturb the printing. Designs (c) and (d) offer the largest paw resulting in cleaner breakage of the tether with lower debris formation [13]. (d) A large connection to the coupon offers higher stability during the undercut, however, the tether can be more difficult to break.

connection to the coupon for easy breakage of the tethers to facilitate the pick-up of the devices. Creation of strong adhesion gradients along the tethers allows them to break in the desired location, which is usually as close as possible to the coupon as this prevents flap and debris creation which could affect the printing. Third, the thickness of the polymer should be increased with the thickness of the coupon to prevent resolution issues in the lithography due by large step height between feet and top of the coupons.

Of the different tether arrangements initially tested for 500 μm long and 60 to 80 μm wide coupons with 1 μm thick sacrificial layer, the best configuration was given by a tether spacing of 40 μm with 15 μm wide tethers tapered to 5 μm at 10 μm distance to the coupon and by using the largest foot anchoring area [Fig.3.13(d)]. These parameters provided the best adhesion to the InP substrate, good stability during the undercut, good transport of the etchant beneath the coupons, easy and clean breaking of the tethers during the pick-up step. It is important to mention that all these anchor systems were hard-baked, it was later discovered that hard-baked anchors become stiffer and more brittle and consequently they can be larger than those that have not been hard-baked. The effects of hard-baking were studied for some "laser type" coupons 80 μm wide with length between 550-750 μm. Another purpose of the experiment was to explore the limits of the tether contact area versus breakage. The tethers were fabricated in a goblet shape of 15 μm width for enhanced stability of the coupon during the undercut provided by the large connection to the coupon. The shrinkage point was kept to 2.5 μm and was positioned 5 μm far from the coupon [Fig. 3.14(a-c)]. It was noticed that the hard-bake re-flows the resist making the tethers thicker in the shrinkage, but more brittle at the same time. The yield in pick-up was measured at y<10 % before hard-baking due to the tethers being too large and hard to break. No pitting effect was noticed under the coupons. The same structures after the hard-bake showed a 100 % yield in pick-up and still no pitting at the bottom. In this case the anchors broke creating some small stiff flaps which prevented the direct print to a Si substrate at room temperature. The higher stiffness was produced by the hard-bake. The print on a 1.2 μm Intervia [23] was successful anyway. Consequently the engineering of the anchors is fundamental to prevent flaps disturbing the printing steps and hard-baking of the tethers is not advisable. The mechanical properties of the tethers can change in time due to hygroscopic property of the material and solvent evaporation. In order to keep the results of the experiment consistent is always advisable to define the anchors

only few days before the transfer printing.

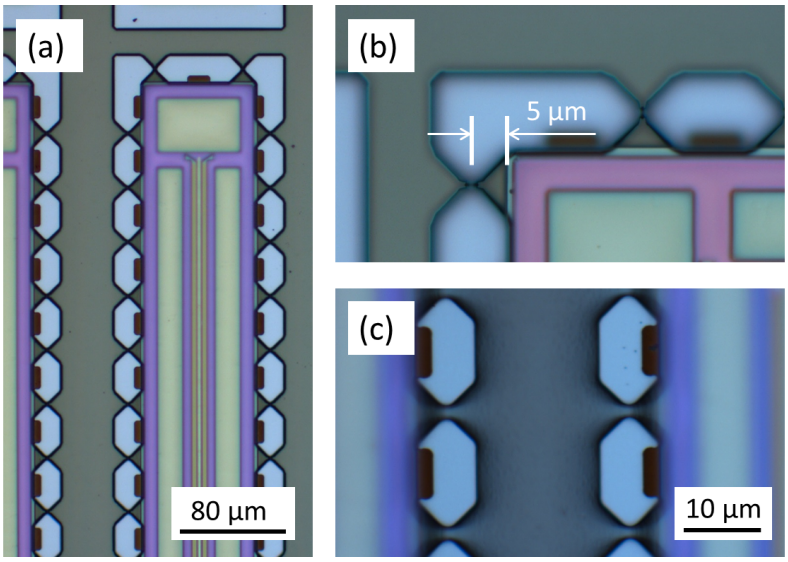


Figure 3.14: (a) Image of the tether used to explore the dimension limits and the hardbake effects. (b) The tethers before hard-bake are disconnected in the upper part of the shrinkage offering a weaker breakage point. (c) The hard-baked tethers reflow creating a more bulky tether which however breaks easily due to increased brittleness.

The different fabrication runs of the lasers were exploited for exploration and improvement of the tether design. One of the designs optimized is reported in Fig. 3.15(a), it shows a tether with different sections of different areas, this layout creates adhesion gradients along the tether during pick-up favouring the breakage in a particular location Fig. 3.15(b). This type of tether offers multiple breakage points along the tether, if the tethers fails to break in the first expected location, another two breakage points with higher adhesion to the substrate gradients are offered to the tether. These tethers tolerate large step heights and do not need any hard-bake. Fig. 3.16 reports three different anchor designs (Design 1, 2 and 3) defined on a layer of S1828 resist deposited on coupons having a $\sim$4 μm and a $\sim$6 μm step height to the substrate. The tethers defined on the larger step height lose resolution, but still break correctly during the pick-up step. Design 1 gives the best yield in pick-up, if the tether does not break at the coupon as expected, it breaks at the shrinkage of the tether which in this case is the narrowest of the three designs with a 2 μm wide section. In the case the breakage fails at the shrinkage, the adhesion gradients provide more chances for fracturing the tether without creating big flaps. The design 2 has a shrinkage of 3 μm and the largest paw, it offers similar pick-up yield to design 1. Some paws are picked up with the tether as the shrinkage is wider than 2.5 μm. Design

3 has a wider connection to the coupon of 8 μm and a 5 μm wide shrinkage plus a graded paw; it can be picked up with good yield, but partial pick-up of the paw is likely to happen due to the smaller adhesion gradient between the shrinkage and the paw. Uneven breakage of the tethers can be due also to tethers which connect to the coupon with a V-shape. This can cause the anchors at one side of the coupon to be thinner than those on the other side producing uneven breakage of the tethers. The solution to this issue is given by adding a 2.5 μm long rectangular section to the tether at the connection to the coupon. The width of the tether at the connection to the coupon must be kept in the range of 5-8 μm. All the designs studied allowed good transport of the etchant beneath the coupons.

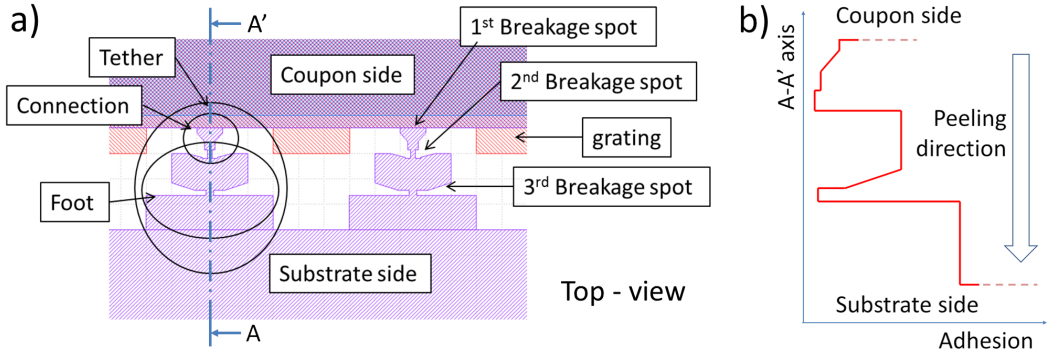


Figure 3.15: (a) Diagram of the engineered anchor structure. (b) The adhesion profile given by the tether shape allows break the tether in the desired spot, if the 1^{st} breakage spot fails a 2^{nd} and a 3^{rd} breakage points help reducing flap creation.

3.3 InGaAs and InAlAs release technologies

In μTP, a sacrificial layer usually positioned between the epitaxial structure and the substrate can be eroded by immersing the chip in a wet-etching solution. An oxidation-reduction selective chemical reaction consumes the sacrificial layer while preserving the surrounding layers. One of the elements in the solution oxidizes the sacrificial semiconductor material and the other remove the oxide. Wet-etching of the sacrificial layer has been investigated in order to obtain released devices with flat and smooth bottom surfaces suitable for direct printing to the new substrate. The etch rates along different crystal directions of the release layer and the selectivity over InP were investigated first for an InGaAs/InP release structure with a 1 μm thick InGaAs sacrificial layer using different etching solutions. An iron chloride based solution demonstrated the highest selectivity to the InP

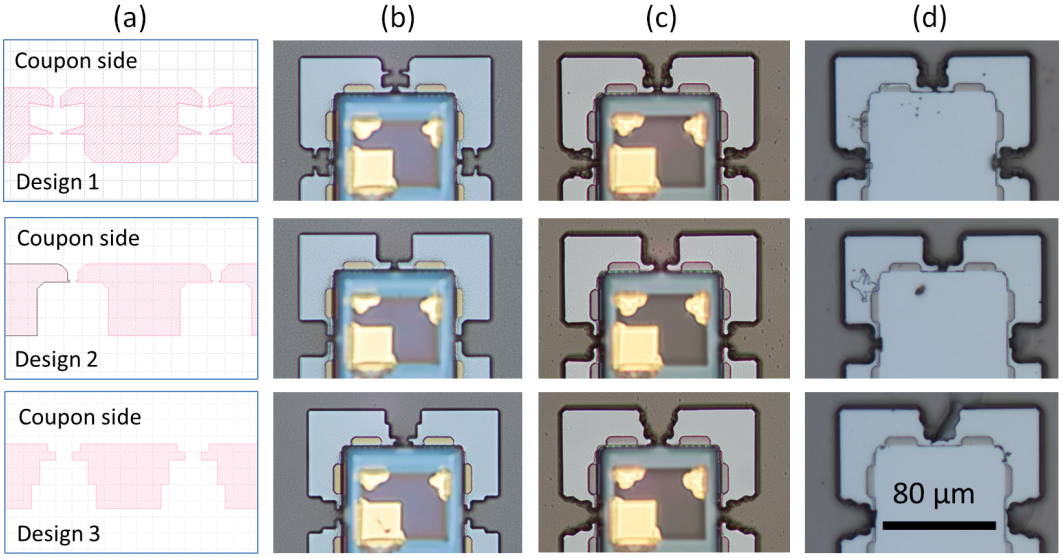


Figure 3.16: Comparison of the three main anchor structures studied to control the breakage, going left to right are reported the (a) design layout, (b) the tethers defined on a ~4 μm step height, (c) on a 6 μm step height and (d) the result after the pick-up of the coupons. [22].

at low temperature and was then tested on a InAlAs/InP release structure demonstrating improved selectivity as reported in the next two sections. The InGaAs/InP release structure shows crystallographic dependent etch rate along the <010> and <001> directions, then proper flatness and roughness for adhesive-less print up to 80 μm wide coupons can be achieved if the coupons are arranged at 45 degrees to the major axis. If the ridge waveguide needs to be aligned along the <011> directions, as in conventional laser processing, then the release takes several hours with added dishing of the released InP surface. On the other hand the InAlAs release structure offers isotropic and higher etch rate and consequently a higher selectivity to InP. In this case wider coupons can be accommodated and undercut along the desired orientation on the wafer [5].

3.3.1 InGaAs/InP release structure

Experiments to determine the InGaAs/InP etch parameters have been conducted on a number of wafers containing an InGaAs layer between the substrate and the lower layer of the epitaxial structure. The wafers were processed to create a pattern of rectangular coupons (mesas) of 500 μm in length and with different widths (from 40 μm to 120 μm) arranged at 45 degree angle to the major axes of the crystal [Fig. 3.17(a)]. Such a layout allows the exploitation of the anisotropic behaviour of the etchant [24] while giving an

etch front that retains the rectangular coupon profile. The even evolution of the etch front reduces uneven stress on the coupon due to capillary forces during the undercut and prevents formation of defects at the bottom surface of the coupons [13]. The etch rates along different crystal directions of the InGaAs release layer and the selectivity over InP were investigated for different etching solutions as indicated in table 3.2.

Etchant	Chemical composition	E_r(InGaAs) nm/min	E_r(InP) nm/min	S -
Phosphoric	H_3PO_4:H_2O_2:H_2O (1:1:8)	315	0.4	787
Sulphuric	H_2SO_4:H_2O_2:H_2O (3:1:1)	480	15	<50
Citric	$C_6H_8O_7$:H_2O_2 (7:1)	175	0.3	585
Tartaric	$C_4H_6O_6$:H_2O_2 (1:1)	300	0.6	500
Chrome-etchant	$HClO_4$:NH_4:Ce_6NO_3 (1:1:2)	650	4	125
Iron Chloride	$FeCl_3$:H_2O (1:2)	1330	1.8	735

Table 3.2: Etching properties for different solutions tested with the InGaAs/InP release structure.

The tests showed the highest lateral etch rate of InGaAs is obtained with the $FeCl_3$ based solution along the <010> and <001> crystal planes and is 1330 nm/min at 18 °C. The selectivity, S, has been calculated as the ratio between the lateral etch rate of InGaAs and the vertical etch rate of InP along the <100> crystal planes. The best selectivity at 18 °C is given by the phosphoric based solution and the $FeCl_3$:H_2O respectively at S = 787 and S = 735. Sacrificial mesas which were 5 μm longer and wider than the other coupons and without anchor system were used to monitor the etch progress during the undercut. The etch rate and selectivity were studied for temperatures in the range of 1-18 °C [Fig. 3.17(b)] as the $FeCl_3$:H_2O selectivity has been reported to increase at lower temperatures [24]. A cold-tunable plate was used to keep the temperature constant during the etching with an accuracy of $\pm$0.1 °C. When the bath temperature is decreased from 18 °C to 1 °C the etch rate of InGaAs decreases almost linearly to 160 nm/min along the <010> and <001> planes. Nevertheless, there is an increase in the selectivity to InP by a factor 2 at temperatures between 2 °C and 12 °C which results in released surfaces with improved flatness and superficial roughness allowing the release of wider coupons. As a result the profile of a 60 μm wide coupon at the bottom has a deviation from flatness of less than 20 nm and a RMS surface roughness S_q=2.2 nm. This allows the undercut of a 60 μm wide coupon in approximately 50 minutes at 8 °C. At temperatures lower

than 1 °C the transport of the etchant beneath the mesas reduces and some solid residuals are generated due to $FeCl_3$ precipitation and ice formation affecting the etch homogeneity and the resulting cleanliness of the sample. The precipitation phenomenon is linked to the lower solubility threshold of $FeCl_3$ in deionized water as the temperature decreases. The homogeneity of the iron chloride solution can be improved by filtering it from undissolved particles remaining at the end of the preparation. The erosion of the resist tethers is negligible in the temperature range studied.

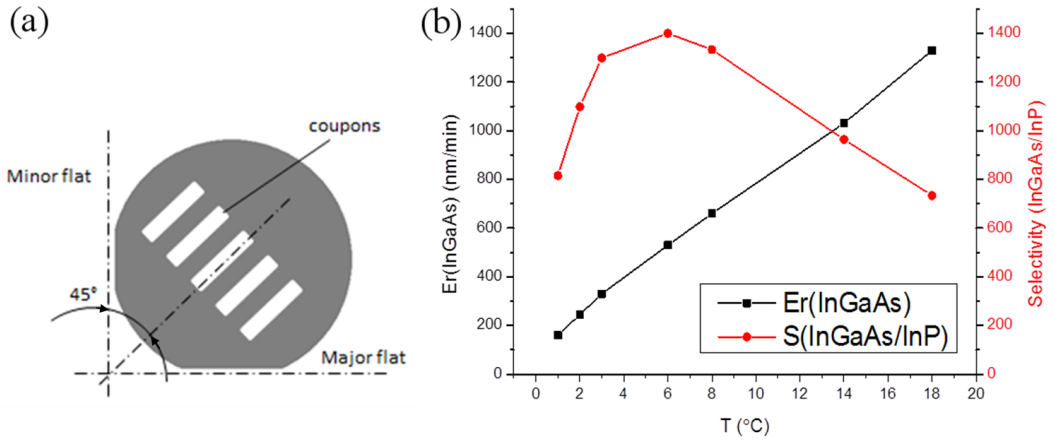


Figure 3.17: (a) Coupon arrangement with respect to the crystal planes of the wafer; the <010> and <001> crystal planes are at 45° to the major axis. (b) Etch-rate of $FeCl_3$:H_2O (1:2) for InGaAs along <010> and <001> planes and the related selectivity to InP for bath temperatures in the range 1-18 °C. [13].

3.3.2 InAlAs/InP - InGaAs/InP comparison

In this section the InAlAs material is characterized as an alternative lattice-matched release layer to InGaAs for InP devices. We show that in this case the etching provides higher selectivity to InP with much less dependence by the release etchant on the crystal orientation. This enables the orientation of the devices along the primary crystal axes and the release of wider coupons without penalty.

Two epitaxial structures were grown by MOVPE on (100) perfectly oriented InP substrates (+/- 0.1 degree angle) for the purposes of comparing between the different etch release layers. Each release layer (InGaAs, InAlAs) was 500 nm thick, n-doped ($1x10^{18}$ cm^{-3}) with layers of InP adjacent to the release layer. The overgrowth of the InAlAs layer commenced with a thin (10 nm) InGaAs layer to avoid aggregation issues and improve the morphology of the InP [9], [10]. Rectangular and circular coupons ranging from

40 μm to 400 μm in width and 50 μm to 500 μm in diameter were realized. The rectangular coupons were orientated at 0, 45, and 90 degrees angle with respect to the major flat of the crystal. Such a layout allowed the detection of preferential directions of the etching [24] while giving an etch front that retained the coupon profile. The even evolution of the etch front prevents the formation of defects at the bottom of the coupons. The coupons were fabricated using the sequence shown schematically in [Fig. 3.18]. An initial mask of SiO_2 is deposited, patterned and etched to just above the release layer (1). SiN_x is then deposited (2) in order to encapsulate the sidewalls of the coupons, which prevents the coupon material from being etched during the undercut step. The SiN_x is patterned (3) with a slightly wider profile in order to keep the sidewalls of the coupon protected. The encapsulated coupon is wet-etched to just above the release layer (4). A SiO_2 passivation layer is deposited (5) and patterned as a grating like structure around the coupons. This (as seen in 3.2.1) serves to further encapsulate the coupon and define its base with respect to the release layer. After the SiO_2 layer is etched (6) the grating structure is etched through the release layer into the substrate to a depth of $\sim$500 nm (7). Resist anchors 2.8 μm thick are patterned by lithography to restrain the coupon to the substrate during the undercut. The previously defined grating structure prevents resist from entirely covering the sidewalls and blocking exposure of the sacrificial layer while providing to the etchant a starting point for the undercut of the device. Finally, the undercut (8) produces a chip of suspended coupons ready for transfer printing to the target substrate (9).

The etching experiments were conducted on both round and rectangular coupons. The selectivity, S, has been calculated as the ratio between the lateral etch rate along the (011) and the (011) crystal planes of the sacrificial layer and the vertical etch rate of InP along the <100> crystal axis. The etch properties were studied in the temperature range of 1-20 °C [Fig. 3.19(a)], a cold-tunable plate was used to keep the temperature constant during the etching experiments with an accuracy of $\pm$0.1 °C. The InGaAs based coupons were etched for 30, 60, 120, 240 and 360 minutes and the InAlAs coupons were etched for 15, 30, 60 and 120 minutes. Figure 3.19(b) shows the comparison of the etch depths along the <011> crystal direction as a function of time for the two different sacrificial layers. The etch rate is similar along the <011> direction.

The first aspect to note is that the etch rate by the $FeCl_3$:H_2O solution for InAlAs is over a factor of four higher than that of InGaAs during the first

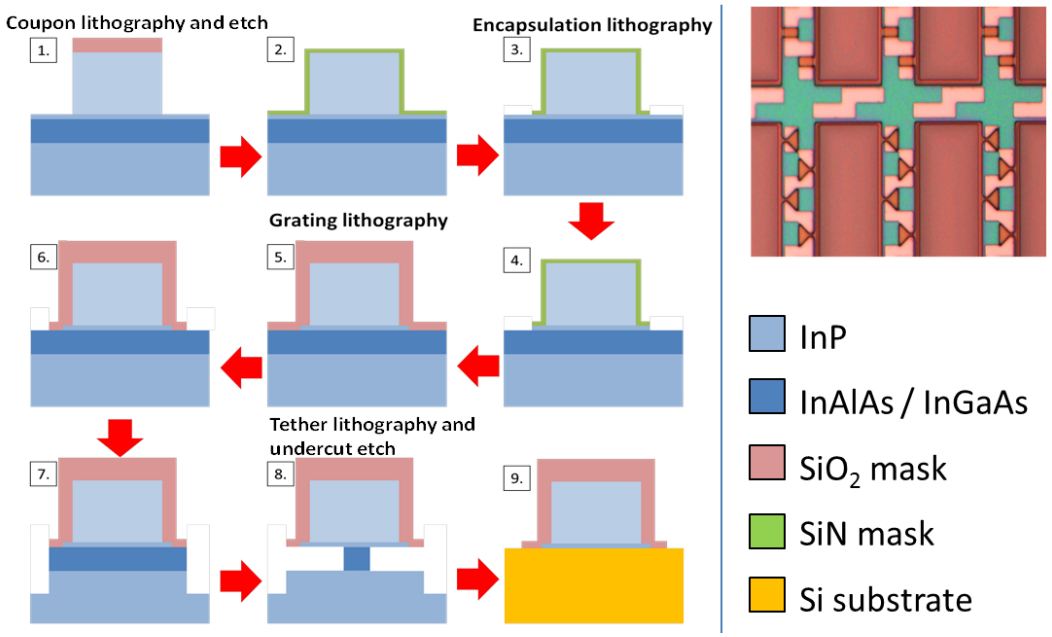


Figure 3.18: Schematic of the coupon fabrication process for μTP with steps 1 to 9 as described in the text. The inset (upper right) shows completed tethered coupons prior to μTP. The orange features around the rectangular coupons are the resist tethers while the light green areas between the tethers is the grating structure on the sacrificial layer where the etching starts. [5].

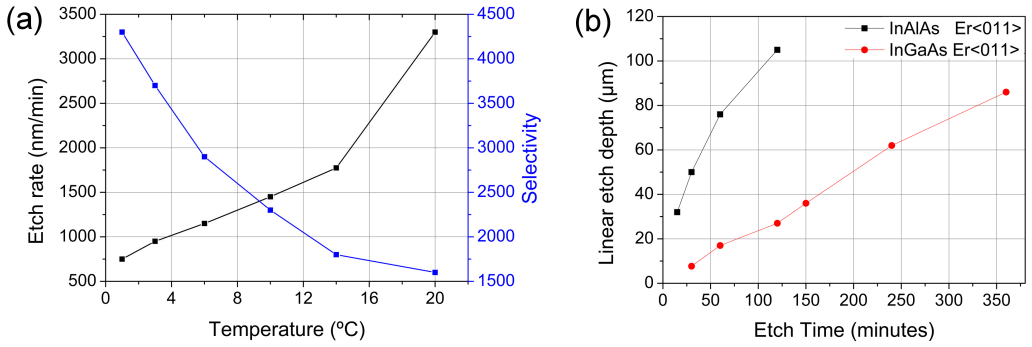


Figure 3.19: (a) Etch rate of $FeCl_3$:H_2O (1:2) for the 500 nm thick InAlAs sacrificial layer and its selectivity to InP at different bath temperatures. (b) Comparison of etch depths along the <011> crystal directions as a function of time for 500 nm thick InGaAs and InAlAs release layers at 6 °C bath temperature. [5].

60 minutes of etching, when measured along the <011> crystal direction, at 6 °C temperature. The selectivity can be further increased to over 4000 at lower temperatures. It is however desirable to etch at temperatures higher than 1 °C in order to avoid precipitation of the $FeCl_3$ inside the iron chloride solution as this could lead to a drastic reduction of the etchant transport and the unwanted creation of debris which could affect the print of the devices. The etch rate after 60 minutes starts to decrease gradually due to reduced transport of the etchant under the coupons. A second difference between the etched layers is the crystallographic dependence for the evolution of etch front [Fig. 3.20(a-d)]. The InGaAs based coupons have a high crystallographic dependence on the etch rate with preferential etching along the (001) and the (010) crystal planes whereas the InAlAs based coupons show negligible crystallographic dependence. In the case of the rectangular coupons oriented along the (011) or (011) planes the InGaAs based coupons show etching from the corners along the (001) and the (010) crystal planes creating a diamond like structure whereas in the InAlAs based coupons show no crystallographic dependency etching evenly around the coupon. Again the undercut etch rates along and at right angles to the (011) plane are over four times higher than those measured in the InGaAs based coupons.

The impact of the higher etch rate and reduced crystallographic dependence on the smoothness and flatness of the coupon surface was further investigated. This was done by examining the coupon site or "stub" after undercut and removal of the coupon. In fact, the coupons are very thin and can be deformed by the presence of the dielectric and resist layers whereas the stub is not. Figure 3.21 shows the cross section of the stub for 110 μm wide and 800 μm long rectangular coupons orientated parallel to the major axis sitting on InGaAs and InAlAs sacrificial layers and completely undercut. The cross-sectional profiles were measured across the long axis of the coupon, at the centre, at 200 μm and at 380 μm from the centre of coupon. The InGaAs coupon was undercut for six hours while the InAlAs coupon only required one hour for complete release. A significant difference between the flatness of the coupons is apparent at the centre of the coupon. For the InGaAs based coupons, a height difference of up to 100 nm from the middle of the coupon to the edge is measured. This can be reduced to 30 nm if the coupons are orientated at 45 degrees to the major axis since the undercut time is much reduced. However, this orientation for the coupon may not be suitable for some other processes. Note that this height difference is

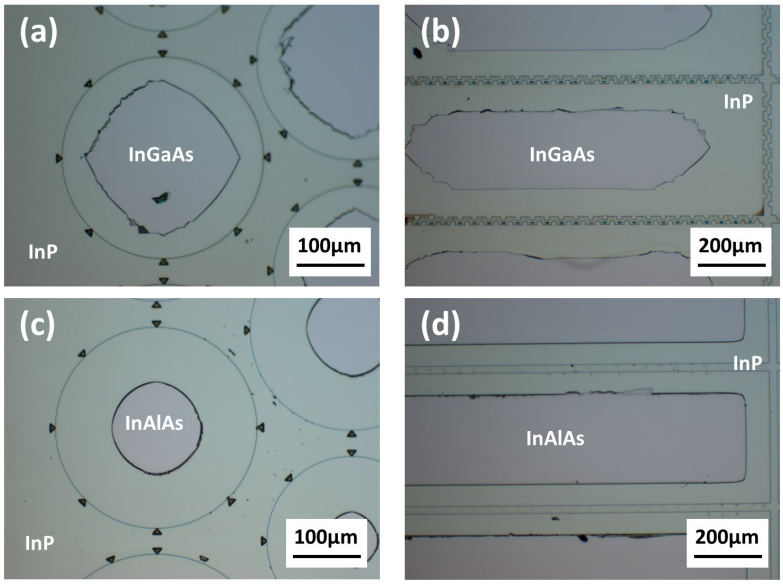


Figure 3.20: Comparison of the etch fronts for circular and rectangular coupons on a InGaAs and a InAlAs release layers partially undercut in $FeCl_3$:H_2O (1:2) at 6 °C and peeled off by tape. It is possible to observe the profile of the remaining part of the sacrificial layer. (a) Circular and (b) rectangular coupons with InGaAs release layer after 120 and 360 minutes etch time show a crystallographic dependent etch front. Similar InAlAs based coupons (c, d) show an isotropic etch profile after 60 minutes. [5].

reduced towards the front of the coupon due to the release layer being undercut earlier at these locations. The height difference from the centre to the edge in the InAlAs coupons is less than 10 nm for a 110 μm wide coupon. The nominal roughness of the stub surfaces, expressed by the root mean square value (RMS), was measured by atomic force microscope (AFM) to be <9 nm in the case of coupons including an InGaAs sacrificial layer etched for 240 minutes and <2 nm for coupons with the InAlAs sacrificial layer. The roughness increases with the etch duration.

To demonstrate the impact of the flatness of the bonding surface of the coupon on the transfer print process, coupons of identical size with an InGaAs and a InAlAs sacrificial layers were released from the original substrate and transfer printed on a quartz substrate. The coupons were picked-up from their native substrates using a flat piece of polydimethylsiloxane (PDMS). The PDMS was then pushed gently against a quartz wafer heated to 90 °C for one minute. The quartz substrate was then observed through the bottom to inspect the contact between the mating surfaces. Figure 3.22(a,b) shows two arrays of coupons printed on a quartz substrate, one was released from an InGaAs sacrificial layer and the other from an InAlAs sacrificial layer. The contact area at the bonding surface is clearly reduced for

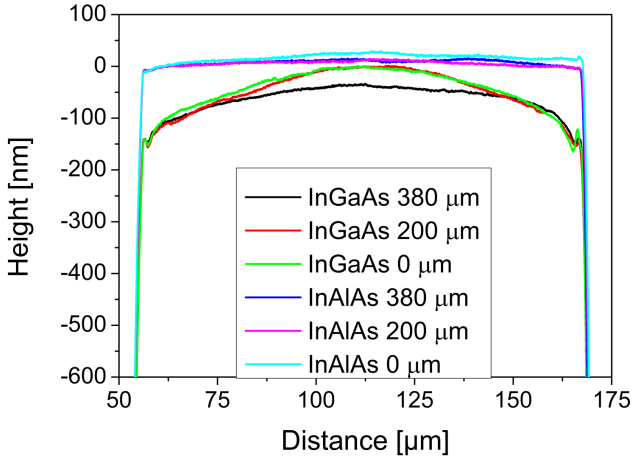


Figure 3.21: Plot of the profiles for the stubs from 110 μm wide and 800 μm long coupons including InGaAs and InAlAs release layers. The profiles have been measured at three different positions along the stub, at the centre, at 200 μm and at 380 μm from the centre along the coupon. [5].

the coupons with the InGaAs sacrificial layer due to dishing of the surface caused by prolonged exposure to the etchant, confirming the measurements made at the profilometer Fig. 3.21.

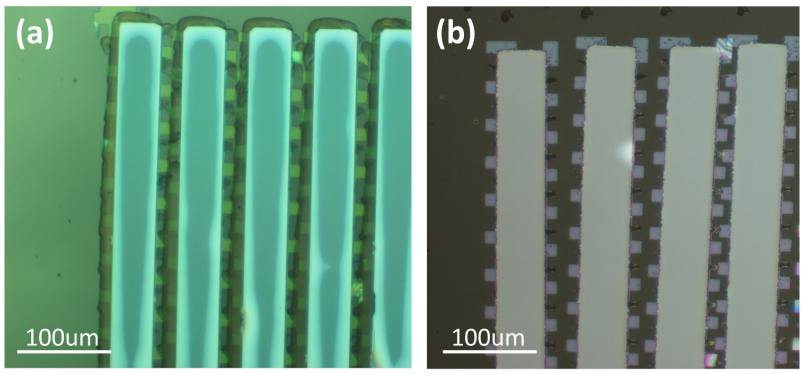


Figure 3.22: Microscope images of the bonding interface of coupons with (a) an InGaAs and (b) an InAlAs sacrificial layer transfer-printed on a quartz substrate. The coupons with an InGaAs sacrificial layer show reduced adhesion area (grey area) due to dishing of the bonding surface, some air gaps are visible (lighter coloured areas) along the edges of the coupons due to poor flatness. The coupons released from a InAlAs sacrificial layer show a monochrome grey-color bonding indicating a flat contact with the quartz substrate. [5].

If one is relying solely on Van der Waals forces for the purposes of bonding, then the flatness and the roughness of the coupons are paramount for good and reliable adhesion. Differences in height can be accommodated by using a thin layer of Benzocyclobutene (BCB) but this excludes the use of direct electrical contact to a substrate and adds an addition step to the μTP

process. Using InAlAs as a release layer is shown to have significant advantages over that of the InGaAs release system in terms of release speed, crystallographic dependence, coupon flatness and roughness. To validate InAlAs as a sacrificial layer suitable for the release of InP devices with high quality surfaces, a chip of etched facet ridge lasers with high reflective coating at one of the facets was fabricated on a epitaxial structure including an InAlAs release layer. Some of the lasers were then adhesive-less transfer printed both manually and at the transfer-printer, at room temperature, to a Si substrate demonstrating unvaried electro-optical performances before and after print [5]. Figure 3.23(a, b) shows the light current characteristics and the lasing spectrum of such devices powered in continuous wave mode. The lasers before and after transfer have similar threshold current, at about 19 mA at 20 °C (Fig. 3.23(a)). The main emission peak is at about 1554 nm wavelength at room temperature before and after print. The free spectral range of the resonator is at $\Delta\lambda$ = 0.66 nm as expected for a 500 μm long Fabry-Perot resonant cavity.

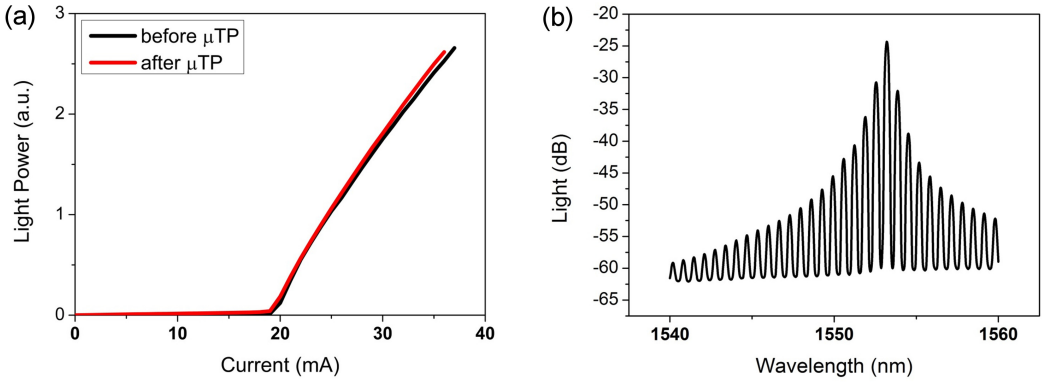


Figure 3.23: Light current characteristics at 20 °C for a laser using the InAlAs layer in its release structure, before and after μTP to a Si substrate (a). Lasing spectrum of a printed device (b). [5].

3.4 Transfer printing of the lasers

The lasers fabricated were transfer-printed to different substrates [Tab.3.3] first manually, with a PDMS bulk using a tweezer, and at the transfer printer (model MTP 177). The PDMS bulk is usually of mm scale size in order to be handled with the tweezers and it collects all the lasers touched on the source chip, allowing only parallel transfer printing of the devices. The devices transfer printed with the tool were picked-up only with a pre-patterned single-post PDMS stamp allowing μTP of single devices and the creation

of arrays by sequential μTP. Devices that print manually, print at the transfer printer in >90 % of the cases. The manual print is used as a preliminary test to evaluate the pickability of the devices from the starting chip and the printability of the devices to a specific substrate, before moving to the transfer-printer.

Devices have been printed in direct contact to the substrate or with an adhesive intermediate layer (sections 3.4.1, 3.4.2). The 3.5-μm-thick laser coupons were adhesive-less printed onto the substrate in the range of temperatures 18 - 110 °C. The highest yield of correctly printed devices is obtained at the highest temperature. Printing temperatures higher than 110 °C cause the resist to re-flow affecting the printing. Printing on adhesive layers is usually performed at room temperature or below 80 °C to prevent the adhesive layer (e.g. BCB or Intervia) to re-flow and the coupon to sink in it being misaligned. The printing on glass or quartz transparent substrates allowed monitoring of the flatness of the bottom surface of the coupons and the bonding to the substrate in order to optimize the process parameters. When the surfaces are sufficiently flat, no shadowed areas or interference fringes are visible through the glass [Fig. 3.24]. In this case the coupons are bonded to the substrate by Van der Waals forces which are strong enough to permit subsequent processing steps and electrical probing without having the coupons moving from the original site. The adhesive-less printing of coupons with deviation from flatness of >30 nm over 30 μm results in a lower yield of printed devices due to reduced contact area and adhesion between the device and the substrate. This would lead to a decrease in the thermal sinking. After the printing step, the resist is removed by oxygen plasma and/or solvents. The highest yield of adhesive-less printed devices was achieved on bare Si and on a Si substrate coated by a Ti : Au (10 : 100)nm thick layer. The Au layer offers thermal connection of the device to the substrate and can be used as a thermal via to channel the heat produced by the device in operation somewhere else. Issues related to Au diffusing in the semiconductor [25] seems to have negligible effects on the electrical performance of the lasers as the current voltage characteristics of the laser are very similar for devices printed on different substrates. It is anyway possible to mitigate diffusion by coating the Au layer with a thin layer of Pd, the device performance result unaltered by this additional layer. The contamination of the substrates associated with the μTP process is mainly related to the debris created during the wet-etch undercut and to a clean breakage of the anchor system during pick-up (as mentioned in the previous sections).

The alignment of the devices on the receiving substrate was not required for adhesion and thermal evaluation. The alignment of the laser to the SOI was achieved with the transfer printer by visual check. Pattern recognition software and alignment markers were not used during the alignment as the pattern recognition system was out of order during the experiments. No alignment metrology has been studied during this thesis as the number of devices integrated on each substrate during this work (<20 devices) was suitable only for indication on the yield of the transfer printing process, >50 devices are usually required for metrology evaluation of the transfer printing process. The evaluation of the adhesion of printed coupons to a hosting substrate was evaluated mechanically by pushing the coupons sideways with the electrical probes, the adhesion was considered adequate for the process when the coupon breaks before moving from the printing spot (rupture test).

Substrate	intermediate layer	adhesive layer
Bare Si (500 μm)	-	-
Si (500 μm)	Ti : Au (10 : 150) nm	-
Si (500 μm)	SiO_2 (50 nm)	-
Si (500 μm)	SiO_2 (1 μm)	-
Si (500 μm)	-	BCB (50 nm)
Si (500 μm)	-	BCB (1.2 μm)
SOI (Si:770 μm)	Si (220 nm) / SiO_2 (2 μm)	-
SOI (Si:770 μm)	-	-
AlN (650 μm)	-	-
AlN (650 μm)	-	BCB (60 nm)
Glass slide (2 mm)	-	-
Quartz (500 μm)	-	-

Table 3.3: InP lasers and dies were printed different substrates, mostly manually, but also at the transfer printer, on intermediate or adhesive layers. The adhesive layer is always deposited on top of the substrate or on the intermediate layer deposited on a substrate.

3.4.1 Adhesive-less printing

The adhesive-less printing of a device to a new substrate has been developed starting from previous works dealing with direct bonding of III-V to SOI; particular reference was given to integration by wafer or die bonding techniques. One of the main methods used for enhancing the adhesion at

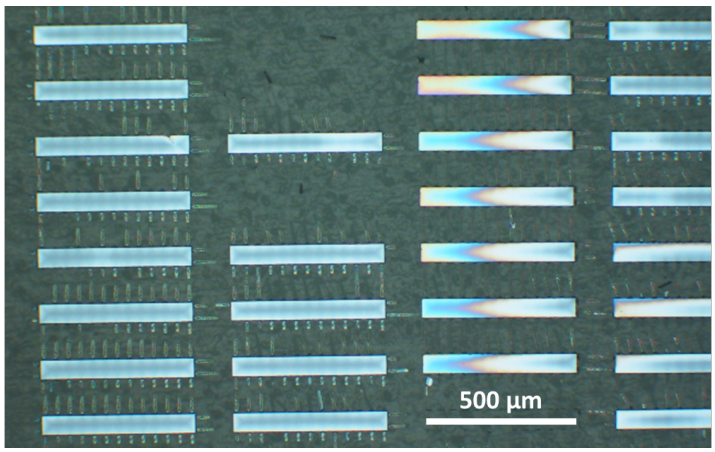


Figure 3.24: InP coupons manually printed on a glass slide, the coupons on the right side were not correctly bonded to the glass, interference fringes were due by an air lamina at the bonding interface.

the bonding interface is the O_2 plasma assisted bonding which was previously developed for creating SOI wafers at low temperature [26], [27]. In this strategy the Si and III-V bonding surfaces need to be perfectly clean of native oxides, then a thin layer of SiO_2 is created by exposing the surface to an O_2 plasma treatment (O_2 plasma activation). During this step the surfaces are converted from hydrophobic to hydrophilic by the oxide layer which has an high density of -OH groups. Then the two activated surfaces are put in contact at room temperature and the Van der Waals forces ensure the initial bond. An annealing step at about 300 °C while applying a pressure of the order of MPa for a couple of hours increase the adhesion to rupture test level due to the formation of covalent bonds at the bonding interface. The gases produced in the reaction can accumulate creating voids at the interface and reducing the adhesion, the usual strategy in this case is to create some outgassing vertical channels in the SOI and to the porous buried oxide layer [28].

In transfer printing to silicon, the surface can be cleaned by any native oxide with a wet-etch exposure to the HF based BOE (5:1) solution for about 5 s. Then the sample is exposed to an oxygen plasma activation for about 2 minutes at 50 W. The coupons released from the original InP substrate must be transfer printed as soon as possible to the hosting substrate. The stubs on the original InP substrate resulting after the undercut of the coupons have surface properties specular to the bottom surface of the released devices. The surface flatness and roughness of the stubs and the hosting substrates were determined at the profilometer [Fig. 3.21] and at the atomic force microscope (AFM) [Fig. 3.25]. In the case the sacrificial layer is InAlAs

buffered to the InP with a thin InGaAs layer, the resulting etched surface is slightly better than the surface of the stub on the substrate side. This is due to the slower etch rate of the iron chloride for InGaAs and the consequent reduced exposure of the InP to the etchant, especially on wider coupons.

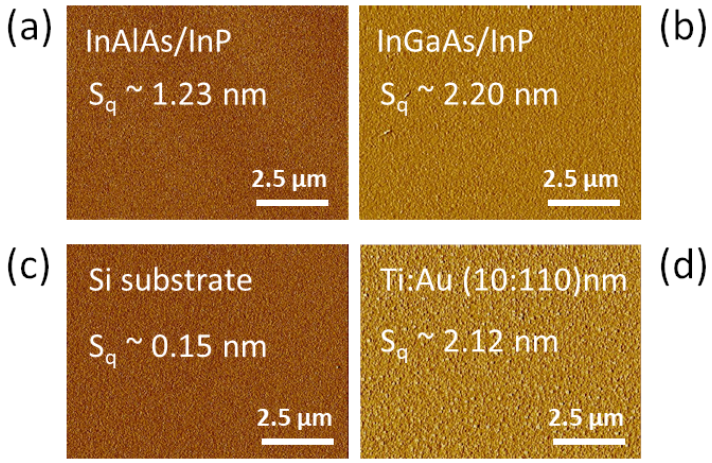


Figure 3.25: AFM-Amplitude images of the surfaces of the stubs, "amplitude" representation. (a) Devices with an InAlAs sacrificial layer result in flatter and smoother surfaces than those (b) with an InGaAs sacrificial layer. (c) The Si surface becomes rougher (d) when coated with a Ti:Au layer, however S_q is still good for adhesive-less printing.

If the roughness and the flatness of the III-V bonding surface are within certain limits adhesive-less print can be achieved. It was empirically determined that the Van der Waals forces ensure the first bonding at the interface if the flatness is f$\leq$0.5 nm/μm and the RMS roughness is S_q<2.5 nm (comparable to that of an epitaxially-grown layer), for coupons up to 120 μm wide. However low flatness and roughness are not enough to ensure the adhesive-less print can be achieved. In fact, aggregation issues at the interface between the sacrificial layer and the n-InP can produce defects at the n-InP bottom surface, visible at the AFM after the undercut [Fig. 3.26(a)]. Protrusion type defects can be high enough to reduce the contact area at the bonding interface preventing the adhesive-less print [Fig. 3.26(b)] while being sparse enough to not change the values of S_q sensibly. As already seen in the previous sections the dishing of the surfaces due to low selectivity can be a factor which leads to reduced contact area at the bonding interface preventing the direct print of a coupon to a flat substrate [Fig. 3.27(a, b)].

After the adhesive-less printing, the anchors can be removed and the adhesion can be enhanced through an annealing at 300 °Cand low pressure (see section 3.4.3). Devices were printed, both manually and at the transfer printer, in direct contact to silicon [Fig. 3.28] and SOI substrates (top Si layer

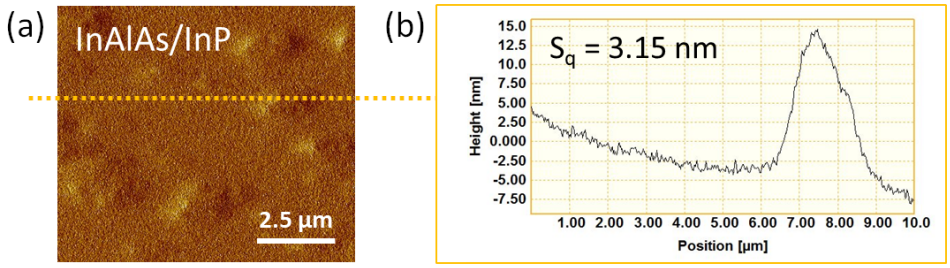


Figure 3.26: (a) AFM amplitude and (b) profile along one of the protrusion of the released surface on the n-InP side of the coupon. In this case the printing yield was very low (<5 %) and the nominal roughness S_q was just above 3 nm.

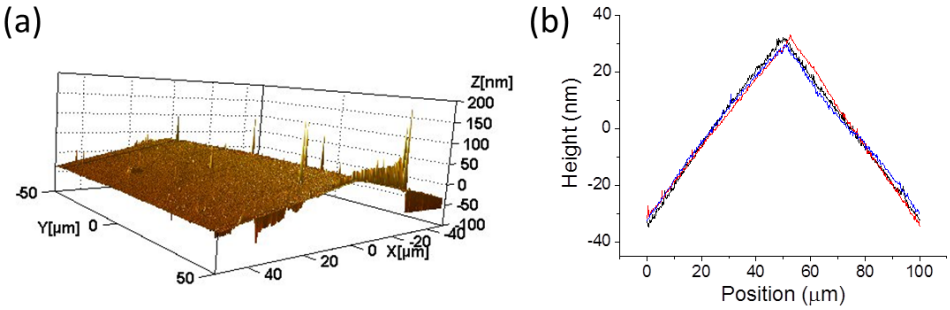


Figure 3.27: (a) AFM 3D-diagram of the released surface of a coupon with an InGaAs sacrificial layer oriented along the major axis of the wafer and (b) profile of the central cross section of the coupon. In this case the yield of printed devices is null due to high dishing of the bonding surface of the coupon.

and Si substrate), to gold coated Si [Fig. 3.29], to glass, SiO_2 and to ceramic AlN substrates.

3.4.2 Print with adhesives

Direct printing on the target substrate usually requires an enhancement adhesion step at 300 °C. In many cases could be desirable not to heat up the integration platform. In this case, or when flatness and roughness of the surfaces fall out of the limits imposed by adhesive-less transfer printing, an adhesive layer can be applied to hold the printed coupons in place. The adhesive layer is usually made of thermoplastic, elastomers or thermosetting materials. Thermoplastic and elastomer materials re-flow when heated so are not suitable for post-integration processing and for holding the coupon precisely in position; thermosetting materials become stable after curing. In this work the integration of a known good die it has been explored on proprietary thermosetting materials as Benzocyclobutene (BCB) and Intervia. These materials crystallize after curing at temperatures in the range 150 - 340 °C for BCB [Fig. 3.30] and 175 - 200 °C for Intervia. No byproducts

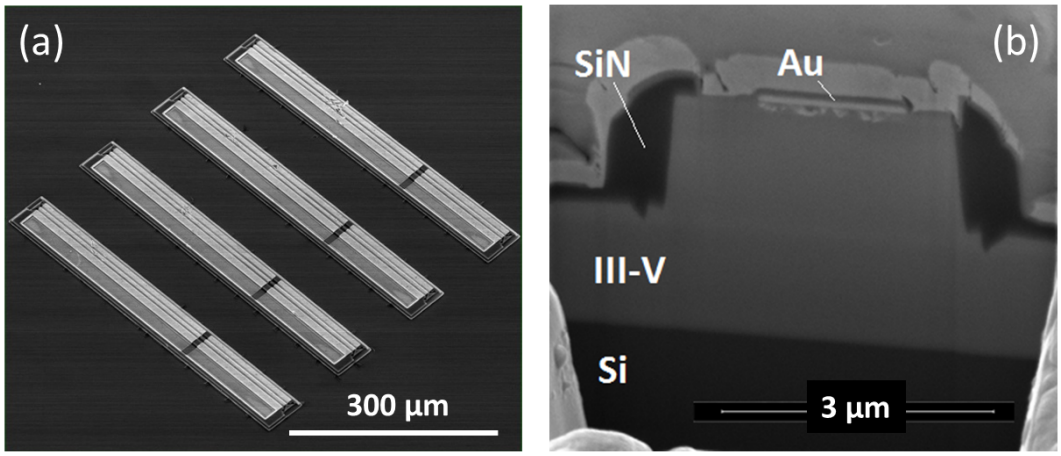


Figure 3.28: (a) SEM image of an array of 4 lasers printed manually on a Si substrate. (b) The SEM image of a focused Ion Beam (FIB) cross section of the ridge region shows defect free bonding between the laser and the Si substrate.

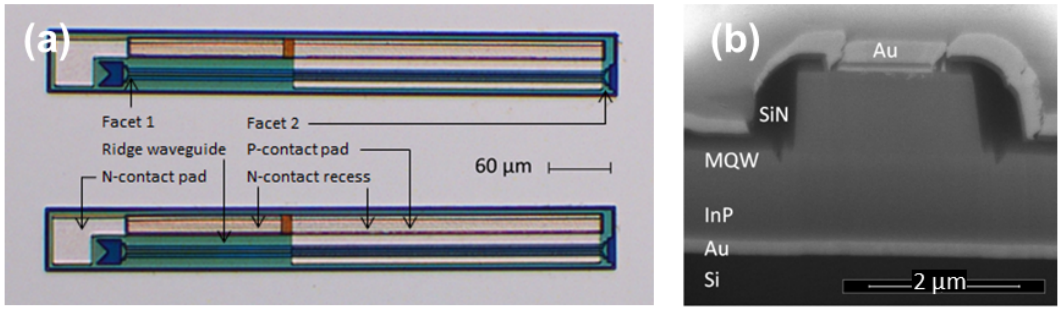


Figure 3.29: (a) Top view of two laser coupons printed manually on an Au coated Si substrate. The various components are illustrated. (b) A Focused Ion Beam (FIB) cross section of the ridge region shows defect free bonding between the laser and the Au coated Si substrate. [13].

are formed after curing the material, so that the adhesion at the bonding interface creates a full contact.

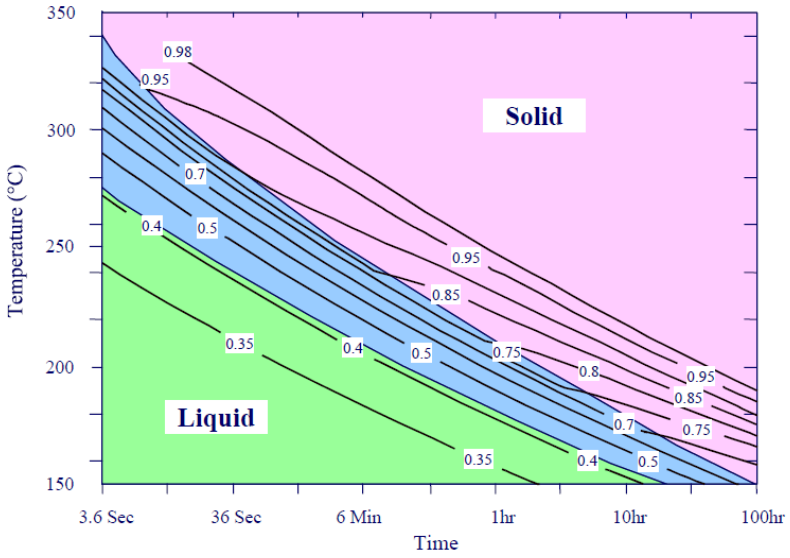


Figure 3.30: The extent of BCB cure as a function of temperature and time [29].

The advantage of BCB over Intervia is given by its wide use in electronics, so all its thermal and electrical properties are well known. On the other side Intervia is a quite relatively new material with many physical properties still to be determined, however it can be cured faster at lower temperature and offers a lower thermal conductivity verified experimentally at $\sigma \sim 0.6$ W/m·K. However, when working with Intervia it is important to consider that the layer thickness shrinks down after cure potentially misaligning the device to the printing spot. Devices have been printed on layers of BCB and Intervia spun with different thickness on different type of substrates, both manually and at the transfer printer. The printing has been performed at room temperature to prevent the devices sinking in the adhesive layer. The flatness of the coupons on the adhesive layer can be assessed by measuring the profile height at the nose the tail and in the centre of the coupons. The thickness of the adhesive layer needs to be taken in high consideration when designing the layout of the integrated device as it can affect the alignment along the vertical axis and the thermal performance. In fact, due to the dielectric nature of the adhesive layer these materials are usually thermal insulators and their thickness can affect the thermal sink of the devices in operation. As reported in the next chapter (section 4.3), enhanced thermal sink can be achieved by using thin thermally insulating adhesive layers.

BCB or Intervia are usually in liquid state and they can be spun on the chip to create a layer of calibrated thickness by changing the spinning parameters and by diluting them with solvents. Layers as thin as 50 nm can be achieved with proper dilution. Spinning of liquid adhesives can be a problem when printing inside recesses due to accumulation of the material inside them, so a spray coating is more appropriate in this case. The application of a nanometer scale thin vapor coated hexamethyldisilazane (HMDS) layer inside the recesses on the SOI has proven a 100% high yield in printing as observed when printing an array of 20 devices on an Au coated Si substrate.

The adhesive layers can be defined only in the desired spots or left all over the chip and removed later if desired. The devices can then be printed on the target spot and the polymer anchors removed. The final step is the curing of the adhesive layer to make it stiffer, stable, resistant to external agents and to achieve maximum adhesion of the device to the substrate.

3.4.3 Post printing treatments

Post printing processing should be reduced to minimum, every post integration process step involves the hosting platform rising the risk of damaging it and the complexity of the fabrication process. The pre-fabrication of the devices reduces post printing processing to minimum and it allows testing the devices before integration, only the polymer anchors removal and some thermal treatment for the adhesion enhancement or for curing the adhesive layer are required. The polymer anchor removal is usually achieved by isotropic dry-etch under oxygen plasma and it can take up to several hours according to the polymer thickness and the power of the plasma etch. It is important to underline that a too high power of the etching could harden the polymer of the anchors making more difficult its removal or lead to heating issues that could affect the device or the hosting platform. Another possible option is to apply liquid solvents (Acetone or Isopropyl alcohol (IPA)) on the printed devices with the aim to melt and remove the anchors. An interesting new strategy for the removal of the anchors is described in the next section.

Reduction of post printing processing of the devices to minimum could be particularly beneficial when integrating to silicon photonics or highly dense populated PICs as a failure in one of the processing steps could affect the whole platform wasting a lot of expensive work previously done. Other

post-printing processing steps are the enhancement of the adhesion of the coupon to the hosting substrate and the deposition of metal pads for electrical connection of the device to the hosting platform. The development of such electrical connection has not be considered in this work as the devices were electrically contactable with standard needle probes on their original pads.

Anchors removal by acetone gas-vapour

Once the devices are printed a great amount of time can be spent to remove the polymer anchors at the oxygen plasma etcher used at low power. Immersion of the printed lasers in liquid solvents could also lead to surface tension that could deteriorate the quality of the adhesion to the hosting substrate. An alternative method developed during this work consists in using acetone gas-vapour in quasi-controlled amounts. In this case the anchors are removed in less than 30 seconds [Fig. 3.31(a)], a last finish at the plasma etcher helps get rid of any eventual stain or polymer remnant. This technique was experimented only manually by squeezing gently the acetone bottle and avoiding the liquid to come out. The vapours of acetone have been observed to also remove soft baked BCB for devices printed on that adhesive layer. After the adhesive layer has been exposed to the acetone gas-vapour, it can be also exposed to small amount of liquid acetone and be thinned down gradually without observing, with a digital microscope, any appreciable lateral displacement of the coupon at the micron scale [Fig. 3.31(b)]. In this case the adhesive layer was thinned down to nanometer scale under most of the device area. This technique has proven to be valuable on printing stressed coupons in contact to the substrate allowing them to reach the same thermal impedance of an adhesive-less printed device [Fig. 3.32(a-c)]. When using this technique there is no need of patterning the adhesive layer as it can be removed outside the printing area during or just after the anchor removal, the time required for removing the anchor is also strongly reduced. Another advantage is that the acetone jet can be dimensioned and directed in a particular spot not affecting the surrounding polymer objects. However, an optimization of the process and the creation of a proper tool for applying this technique would be required beforehand.

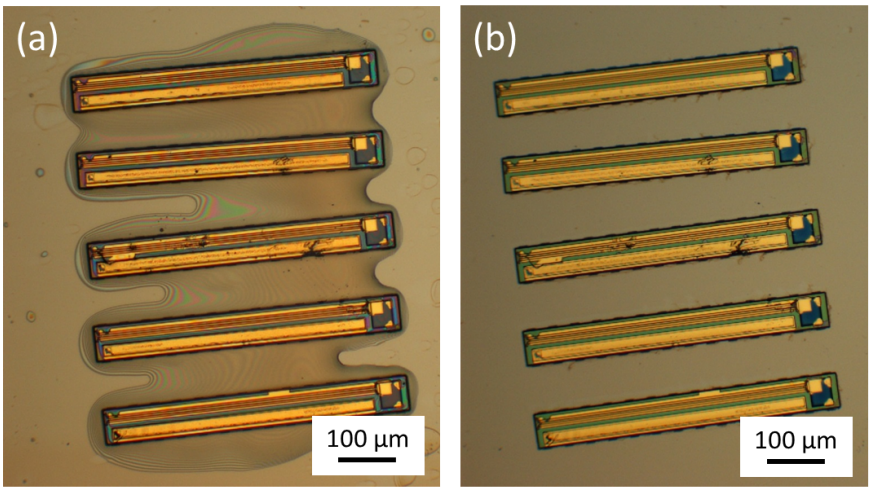


Figure 3.31: (a) Lasers printed manually on a 50 nm thick BCB layer deposited on SOI after 10 s acetone gas exposure, the anchors are completely removed and the BCB starts dissolving around the coupons. (b) Same lasers after liquid acetone exposure, the anchors and the underlying BCB have been thinned down to a few nm.

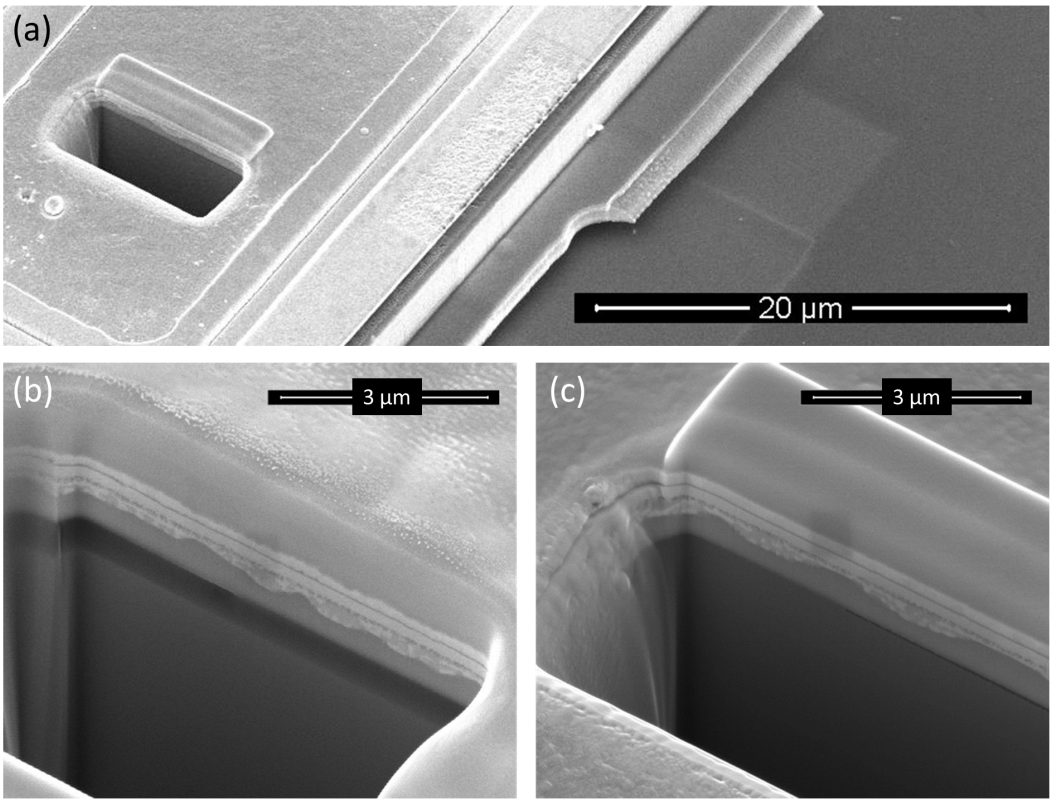


Figure 3.32: (a) SEM of an FIB-cross-section of a laser at about 10 μm far from the edge for a coupon printed manually on ~700 nm thick BCB. (b) Zoom on the FIB-cross-section. (c) FIB cross section of a laser printed on the same substrate and exposed to vapours of acetone and later to liquid acetone for about 10 s. Some BCB is still present at the edge of the coupon probably due to short exposure to the acetone. The process still needs to be optimized.

Adhesion enhancement

The adhesion of the printed coupons to the new hosting substrate can be enhanced mainly in two ways, by a soft annealing step in a low pressure chamber or by using an adhesive layer. In the first case the soft annealing is performed inside the loading chamber of a PECVD machine, the sample holder is an hotplate which keeps the sample at 300 °C and the vacuum system can lower the pressure down to few mTorr. Once the sample is loaded and the chamber purged, most of the air molecule are taken out of the chamber, in particular the air molecules trapped at the interface between the device and the substrate are outgassed by the increased temperature and by the lower pressure in the surrounding environment. In the case of <100 μm wide coupons, after about 30 minutes the outgassing will be enough and it will be possible to vent the chamber. While venting the chamber, the pressure at the top of the devices is higher than that at the bottom due to the reduced number of molecule that can access the bonding interface region. This pressure gradient allows the coupons to be pushed against the substrate enhancing the number of contact points at the bonding interface resulting in enhanced adhesion to rupture test (the device breaks before detaching from the substrate) and higher thermal sink. No displacement of the coupons is detected after this step.

It can be desirable not to heat up the sample, in this case adhesive layers are the recommended choice for achieving enhanced adhesion as described in section 3.4.2. Moreover polymer layers can be used after printing to define pads that can lock the device to the substrate (more details about this strategy are reported in chapter 5).

3.5 Conclusion

The creation of a suitable process for transfer-printable pre-fabricated InP lasers has been reported in this chapter. The development of the iron-chloride based etching technology for InGaAs and InAlAs sacrificial layers allows the release of the devices from the starting substrate with flat and smooth surfaces suitable for adhesive-less printing. The engineering of the polymer-anchor provides clean pick-up of the devices without creation of particles that could prevent the printing to the new substrate. The devices were printed onto different substrates to evaluate the capabilities offered by the technology and to explore the limits of the printing, it was discovered that

flatness and smoothness of the mating surfaces are important parameters to be considered in the process. The lasers were always transfer-printed first manually as a preliminary test before moving to the transfer printer. In fact, devices that print manually print also at the transfer printer in >90 % of the cases. The knowledge achieved from printing on different substrates was applied for integrating the devices inside a recess on the SOI on different substrates as reported in chapter 5 (section 5.2). The analysis of the performance of the devices before and after μTP allows to determine if the process damages the devices and how the thermal conductivity of the new substrate and the adhesion to it can affect the final performance of the device. The next chapter reports the electro-optical and thermal analysis of the laser developed and discuss the improvement of the performance through the runs of fabrication.

Bibliography

[1] David Gomez et al. "Process capability and elastomer stamp lifetime in micro transfer printing". In: *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*. IEEE. 2016, pp. 680–687.

[2] Ruggero Loi et al. "Thermal Analysis of InP Lasers Transfer Printed to Silicon Photonics Substrates". In: *Journal of Lightwave Technology* 36.24 (2018), pp. 5935–5941.

[3] Valeria Dimastrodonato et al. "AlGaAs/GaAs/AlGaAs quantum wells as a sensitive tool for the MOVPE reactor environment". In: *Journal of Crystal Growth* 312.21 (2010), pp. 3057–3062.

[4] Agnieszka Gocalinska et al. "Surface organization of homoepitaxial InP films grown by metalorganic vapor-phase epitaxy". In: *Physical Review B* 86.16 (2012), p. 165307.

[5] James O'Callaghan et al. "Comparison of InGaAs and InAlAs sacrificial layers for release of InP-based devices". In: *Optical Materials Express* 7.12 (2017), pp. 4408–4414.

[6] Photon Design. *FIMMWAVE, A powerful waveguide mode solver*. 2019. URL: `https://www.photond.com/products/fimmwave.htm` (visited on 07/21/2019).

[7] *Micro-transfer printing for advanced scalable hybrid photonic integration*. Vol. 5. Valencia, Spain, 2018.

[8] *Top-Hit project*. 2019. URL: `http://www.tophit-ssi.eu/` (visited on 02/11/2019).

[9] Agnieszka Gocalinska et al. "Unusual nanostructures of "lattice matched" InP on AlInAs". In: *Applied Physics Letters* 104.14 (2014), p. 141606.

[10] Enrica E Mura et al. "Tuning InP self-assembled quantum structures to telecom wavelength: A versatile original InP (As) nanostructure "workshop"". In: *Applied Physics Letters* 110.11 (2017), p. 113101.

[11] Badhise Ben Bakir et al. "Electrically driven hybrid Si/III-V Fabry-Pérot lasers based on adiabatic mode transformers". In: *Optics express* 19.11 (2011), pp. 10317–10325.

[12] Alexander W Fang et al. "Electrically pumped hybrid AlGaInAs-silicon evanescent laser". In: *Optics express* 14.20 (2006), pp. 9203–9210.

[13] Ruggero Loi et al. "Transfer printing of AlGaInAs/InP etched facet lasers to Si substrates". In: *IEEE Photonics Journal* 8.6 (2016), pp. 1–10.

[14] LY Kuritzky et al. "Chemically assisted ion beam etching of laser diode facets on nonpolar and semipolar orientations of GaN". In: *Semiconductor Science and Technology* 31.7 (2016), p. 075008.

[15] F Binet et al. "Realization and optical characterization of etched mirror facets in GaN cavities". In: *Applied physics letters* 72.8 (1998), pp. 960–962.

[16] H. Sugimoto et al. "Fabrication of crystal-facet mirrors for short cavity lasers by selective InP epitaxy on etched sidewalls". In: 1995, pp. 65–67.

[17] Franscesco Floris. "Surface electromagnetic modes application in plasmonic and photonic nanostructures for emitting and sensing devices". PhD thesis. University of Pavia, 2016.

[18] Marco Passoni et al. "Optimizing band-edge slow light in silicon-on-insulator waveguide gratings". In: *Optics express* 26.7 (2018), pp. 8470–8478.

[19] Padraic E Morrissey et al. "Coupled cavity single-mode laser based on regrowth-free integrated MMI reflectors". In: *IEEE Photonics Technol. Lett* 28.12 (2016), pp. 1313–1316.

[20] Emil Kleijn, Meint K Smit, and Xaveer JM Leijtens. "Multimode interference reflectors: a new class of components for photonic integrated circuits". In: *Journal of Lightwave Technology* 31.18 (2013), pp. 3055–3063.

[21] J Zhao et al. "On-chip laser with multimode interference reflectors realized in a generic integration platform". In: *IPRM 2011-23rd International Conference on Indium Phosphide and Related Materials*. IEEE. 2011, pp. 1–4.

[22] Brian Corbett et al. "Transfer Printing for Silicon Photonics". In: *Semiconductors and Semimetals*. Elsevier, 2018, pp. 43–70.

[23] Rohm and Haas Electronic Materials. *INTERVIA^{TM} PHOTODIELECTRIC 8023 SERIES*. 2019. URL: `http://microchem.com/products/images/uploads/Intervia_Photodielectric_8023_UL-PF08N013R2.pdf` (visited on 07/10/2019).

[24] Thomas Kusserow et al. "Micromachining of InP/InGaAs multiple membrane/airgap structures for tunable optical devices". In: *MEMS, MOEMS, and Micromachining III*. Vol. 6993. International Society for Optics and Photonics. 2008, 69930B.

[25] V Parguel et al. "Gold diffusion in InP". In: *Journal of Applied Physics* 62.3 (1987), pp. 824–827.

[26] Donato Pasquariello and Klas Hjort. "Plasma-assisted InP-to-Si low temperature wafer bonding". In: *IEEE Journal of Selected Topics in Quantum Electronics* 8.1 (2002), pp. 118–131.

[27] Günther Roelkens et al. "III-V/silicon photonics for on-chip and intra-chip optical interconnects". In: *Laser & Photonics Reviews* 4.6 (2010), pp. 751–779.

[28] Di Liang and John Edwards Bowers. "Highly efficient vertical outgassing channels for low-temperature InP-to-silicon direct wafer bonding on the silicon-on-insulator substrate". In: *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* 26.4 (2008), pp. 1560–1568.

[29] Dow Chemical Company. *CYCLOTENE^{TM} 3000 Series Advanced Electronic Resins*. 2012. URL: `http://msdssearch.dow.com/PublishedLiteratureDOWCOM/dh_08b4/0901b803808b4ed7.pdf?filepath=/888-00006.pdf&fromPage=GetDoc` (visited on 10/16/2018).

Chapter 4

Characterization of the transfer printable lasers

The performance of the lasers developed in chapter 3 are discussed here. The devices were characterized electro-optically and thermally, before the release from the growth substrate and after the integration to the hosting substrates. The iterative fabrication-integration-characterization of the devices was useful for improving the technology. In particular, a low threshold current depends mainly on the quality and the type of passivation layers at the facets and on the annealing of the contacts that must provide ohmic electric contacts and low series resistance for achieving low operating temperature. The layout of the metal pads of a completely pre-fabricated laser determines how easy it can be to probe such small devices and characterize them. No particular changes in the electro-optical performance were detected due to the transfer printing process, the type of hosting substrate on which the devices are printed affects the thermal properties instead.

The measurement setup used for the characterization of the lasers is reported in this chapter. The electro-optical analysis of the lasers and the performance of the final laser developed are compared to the first run of laser fabricated. The thermal characterization of the lasers combined to simulations determined the actual thermal performance and the effects produced by changes in the geometry, layout and materials of the integrated laser and the hosting platform involved. Finally the effects of the μTP on the performance of the devices are discussed.

4.1 Measurement setup

The experimental setup allows the electro-optical and thermal characterization of the devices through the measurement of the light-current (L-I) and the voltage-current (V-I) characteristics in continuous wave (CW) and

pulsed wave (PW) modes, and through the spectra detection. The setup used [Fig. 4.1] was connected to different labview management software and is composed by:

- Thermally controlled stage for sample positioning (Submount).
- Thermal control unit.
- Pulse generator for generation of pulsed wave (PW) current signals.
- Multimeter for continuous wave (CW) current generation and for current, voltage and resistance measurements.
- Probes for electrical contact of the devices.
- Current probe with inductor for pulsed measurements.
- Electrical cables.
- Optical apparatus for the collection of the light:
  - Optical lenses mountable to different alignment stages.
  - Photo-diode (PD) working in the wavelength range 780÷1800 nm.
  - Light power meter.
  - Optical fibers for light transportation.
- Oscilloscope.
- Spectrometers for emission wavelength detection and analysis.

The thermally controlled stage is made from a copper heat sink platform in thermal contact with a thermoelectric cooler managed by a thermoelectric controller (TEC). The substrates with the devices is mounted at the edge of the stage with an intermediate layer of thermally conductive paste, this strategy allows respectively a better collection of the emitted light and to sink properly the heat to the thermal sink [Fig. 4.2]. The lasers are usually printed at the edge of the substrate to facilitate light collection, if they are recessed to the substrate edge part of the light could be not collected by the lens. A power supplier and a function generator are used to electrically activate the devices in CW or PW mode. Stage probes with metal

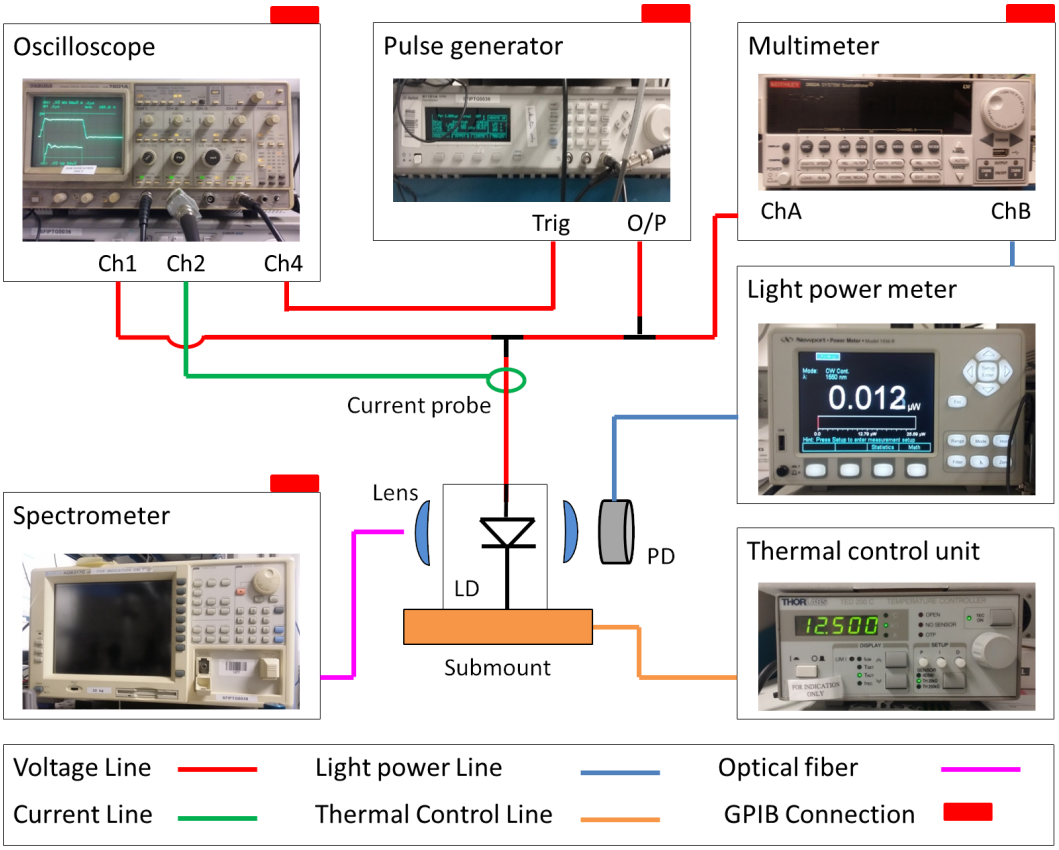


Figure 4.1: Diagram of the experimental setup assembled for electro-optical and thermal characterization of the laser devices studied. The laser diode (LD) is mounted on the submount as indicated in Fig. 4.2.

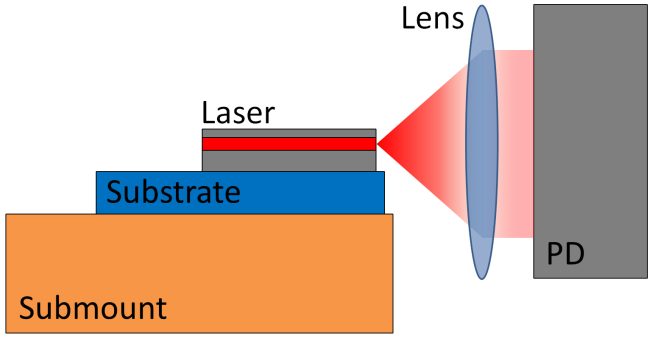


Figure 4.2: Diagram of the chip mounted at the edge of the submount for correct light collection. The lasers are usually printed at the edge of the substrate to facilitate light collection.

needles are used to electrically contact the device, an induction probe connected to the cables allows the detection of the current injected into the device (when in PW regime) and translates it into a voltage pulse measurable at the oscilloscope. Lenses can be moved around the platform by a micrometer positioning stage, to collect the light emitted by the devices. The PD sensing element is a 3 mm diameter Ge detector, a movable holder allow to position it around the platform and the focusing lenses. Optical fibers can be used to collect the light at the lens focus and bring it to the optical spectrum analyser. The oscilloscope can be included in the setup for visualization and collection of the injected current voltage values or for the analysis of the photo-current coming from the photo-diode. The photo-current is converted to a light power value by the light power meter including its own calibration factor related to the full-scale set. The setup includes two main spectrometers one has low resolution in wavelength of $\sim$3.1 nm full width half maximum (FWHM) with the "$w/25$ μm" slit and it is used for the emission peak detection; The other optical spectrum analyser allows measure the spectra with resolution of $\Delta\lambda\pm0.05$ nm at 1550 nm and monitoring the wavelength shifts of the main peak and of the individual Fabry-Perot (FP) modes. High resolution is necessary for the thermal analysis as the FP modes shift with temperature (see section 4.3). Several devices were tested on each source-chip (>10 lasers) from different areas and on each substrate ($\geq$3 lasers) after μTP in order to validate that the reported values were representative of a particular process.

4.2 Laser characterization

The laser diode characterization consists in the determination of the electrical, spatial, spectral, optical and dynamic properties of the laser [1], [2]. The electrical properties of the laser allow characterize the efficiency of the material and the laser waveguide in converting current to light and some of the thermal properties. The electrical properties are determined by measuring the Light-current (L-I) and the voltage-current (V-I) characteristics. The L-I characteristics (L-Is) allows the determination of the threshold current I_{th} (current at which lasing begins), the threshold current density which is useful for comparison between different devices as it does not depend on the geometry of the device. L-Is allow the determination of the slope efficiency and other laser efficiency related parameters such as the external differential quantum efficiency (efficiency in converting electron-hole pairs in

emitted photons), the internal quantum efficiency (efficiency in converting electron-hole pairs in photons), the internal losses (which determine how many photons find a way out to the laser cavity) [2]. The L-Is at different temperatures allow the calculation of the characteristic temperature of the device which indicates how the material responds to different environmental temperatures. The V-I characteristics allow the determination of the diode drop and of the series resistance of the device. The spatial properties of the laser regarding the output light intensity profile in the far and in the near field and the beam spatial divergence. The spectral properties are related to the emission spectrum of the laser diode and give indication on the type of laser, the spectral width, the centre emission wavelength, the free spectral range and the thermal behaviour and the thermal impedance of the devices (as described in section 4.3) [2]. The optical properties of the laser concern astigmatism and wave-front characteristics. The dynamic properties measure the noise, the intermodulation distortion, rise time and fall time, chirping of laser pulses if the device is operated dynamically [1].

The V-I and the L-I characteristics were measured both in pulsed and continuous wave modes. The light emitted by the laser was collected by a high numerical aperture lens (NA $\sim$0.7) positioned a few mm away so as to position the facets of the devices in the focal plane of the lens, a photo-diode detected the light collected by the lens. Given a far field beam-divergence of $\sim$60 degree FWHM along the vertical axis and the numerical aperture of the focusing lens, an estimated >70 % of the emitted light could be collected with the devices positioned at the edge of the chip or the hosting substrate (for transfer-printed devices). It was possible to collect a reasonable portion of emitted light estimated >30 % for a distance of the device to the lens <1 cm. This setup allows approximate the L-I characteristics and determine the threshold-current value at different temperatures. The lasers developed in this project were optimized on similar InP-based epitaxial wafers by working mainly on the geometries and the fabrication. The following two paragraphs report about the electric, the spectral and the spatial characterization of the first and one of the last optimized batch of lasers fabricated, to highlight the improvement achieved in the laser performance. The optical and the spatial analysis have not been treated here as the aberrations of the wave-front are neglected and the devices are designed to operate in CW mode.

4.2.1 Initial run of fabricated lasers

The first run of dry-etched-facet lasers was fabricated on the A1779 epitaxial structure (see Appendix A). The devices before transfer show a threshold current, I_{th}, of 45 mA, for a 500 μm long and 2.5 μm wide ridge waveguide operating at 18 °C. The resulting threshold current density J_{th} was at 600 A/cm^2 per quantum well, at room temperature (18 °C). J_{th} was about three times higher than that of similar cleaved facet devices. The higher value of J_{th} has been ascribed to a low reflection at the facets due to a SiN passivation layer being thinner than λ/n of 778 nm (for n=1.99 at 1550 nm wavelength). The roughness of the facet due to the dry-etch was estimated only as a second order effect on the reflectivity reduction as similar test etched-facets ridge lasers with different thickness of the passivation layer reported a I_{th}<35 mA. The reduced mirror reflectivity of $R \sim 18\%$ was estimated with few percentage points error from similar test ridge lasers with cleaved facets by measuring the inverse differential quantum efficiency, η_d, at different cavity lengths, L, and by applying eq. 4.1.

$$\frac{1}{\eta_d} = \frac{1}{\eta_i}\left[1 + \frac{\alpha_i}{ln(1/R)}L\right] \Rightarrow R = exp^{-\frac{\alpha_i}{m\cdot\eta_i}} \tag{4.1}$$

With η_i the internal quantum efficiency, α_i the internal losses and m=$\alpha_i/[\eta_i \cdot ln(1/R)]$. η_i and α_i were determined from the cleaved facet lasers. Another second order contribution to the I_{th} increase was ascribed to the release layer of InGaAs acting as a thermal barrier due to the reduced thermal conductivity of σ(InGaAs) = 0.05 W·cm^{-1}°C^{-1} compared to that of InP, σ(InP) = 0.68 W·cm^{-1}°C^{-1}, which is about one order of magnitude higher. The reduced thermal conductivity of InGaAs increased the thermal impedance of the devices on the native substrate of few K/W. The increased thermal insulation in addition to the lower reflectivity at the facets resulted in the devices operating only in pulsed mode (duty cycle D =0.1 %, T =500 μs) before transfer. Lasers were directly printed (without adhesion enhancement) on plain Si and they showed I_{th} of 45 mA at 18 °C, in pulsed mode. In this case it was possible to use duty cycles up to two orders of magnitude higher compared to the devices on the native substrate. The improved performance was ascribed to the increased thermal sinking associated with the removal of the InGaAs layer. The thermal conductivity of silicon σ(Si) = 1.3 W·cm^{-1}°C^{-1} is about twenty six times higher than σ(InGaAs). Moreover, finite element simulations of a similar GaAs laser (thermal conductivity σ(GaAs) = 0.52 W·cm^{-1}°C^{-1}) reported increased thermal sink due to

the higher thermal conductivity of the new substrate when the distance between the heat-source and the substrate was <3 μm [3]. In this case the separation between the active region and the Si substrate was 1.5 μm. Lasers printed on Au coated Si substrate and annealed in the PECVD chamber for enhanced adhesion demonstrated continuous wave lasing [Fig. 4.3(a)] with up to an estimated few mW emitted power. Only a portion of the light power was collected with the actual setup was due to the lasers being printed far from the edge of the substrate. The improved thermal sinking was given mainly by the improved bonding quality provided by the adhesion enhancement and only partially by the higher thermal conductivity of Au compared to that of Si, σ(Au)=3.14 W·cm^{-1}°C^{-1} as demonstrated later in the thermal analysis of printed devices [4]. Moreover, the annealing step improved the electric contacts reducing the series resistance from ∼60 Ω to 25 Ω and giving lower heat generation. It was later realized how proper annealing of the contact is vital for achieving a low series resistance and in turn a low thermal impedance of the device. The threshold current was measured of I_{th} ∼45 mA at room temperature in PW mode and varied from 50 mA to 80 mA for a change in the stage temperature from 20 °C to 45 °C with the laser operating in CW mode. The value of the characteristic temperature, T_0, was calculated to 57.5 K from the shift of the threshold current in temperature while operating the devices in PW mode. The diode turned on at 0.8 V and the series resistance of the device was calculated at ∼25 Ω (for a 2.5 μm wide and 500 μm long ridge).

The emission spectrum was collected by positioning one end of a multimode fiber in place of the PD and connecting the other end of the fiber to a high resolution spectrometer. The main emission peak of a laser printed on a Au coated Si substrate is at 1542 nm wavelength when operating at 15 °C temperature [Fig. 4.3(b)]. The free spectral range of the resonator $\Delta\lambda$ is given by $\lambda_0^2/2nL$, where n is the group index in the resonator, L is the cavity length, and λ_0 is the light wavelength. The expected $\Delta\lambda$ for L ∼500 μm is in agreement with the measured value $\Delta\lambda_{exp}$ =0.66 nm. The spatial characterization of the far-field indicates a beam divergence of 60 degrees FWHM along the vertical axis and 19 degrees FWHM along the horizontal plane.

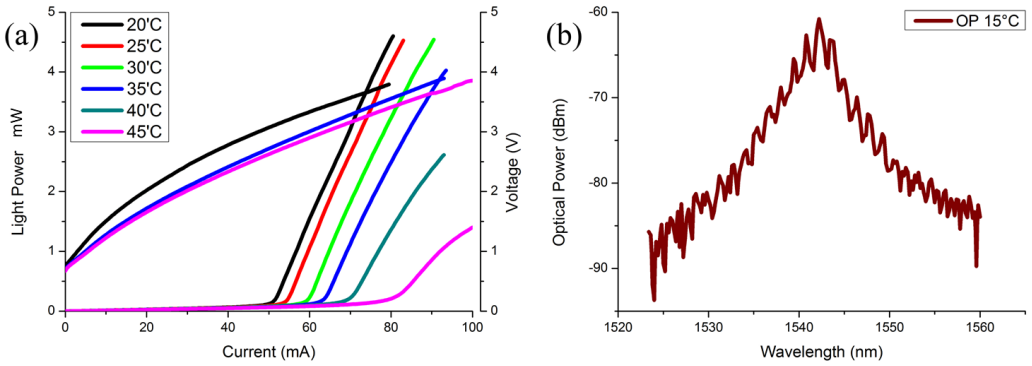


Figure 4.3: (a) L-I and V-I characteristics of a laser printed on Au coated Si operating in CW at temperatures in the range 20-45 °C and (b) spectrum of the same devices at 15 °C. The light power collected is only a portion of the total, due to the lasers being printed far from the edge of the hosting substrate. [5].

4.2.2 Final run of fabricated lasers

During the development of the transfer printing process for the InP lasers, a parallel improvement of the performances of the lasers has been carried out. The threshold current has been lowered mainly by working on the facet passivation layer, the highly reflective coating at the rear facet and by optimizing the annealing of the metal contacts. The initial SiN layer with low reflectivity was exchanged with a calibrated ∼100 nm thick SiO_2 layer (as discussed in section 3.2.4), in addition a highly reflective (HR) coating was deposited on one of the facets. The devices on-chip operated up to 120 °C in PW and up to 110 °C in CW mode [Fig. 4.4(a, b)], the lasing threshold current was ∼16 mA and the threshold current density was J_{th} ∼213 A/cm^2, the light power collected in PW and CW mode was about 8 mW and 6 mW respectively, at 150 mA and 20 °C temperature. The slope kink in the light power at current values of ∼60 mA is ascribed to mode hopping of the laser. The turning voltage was at about 0.8 V, the series resistance, R_S between 6 Ω and 8 Ω resulted 1/3 lower compared to the initial run of lasers by optimizing the annealing step for the contacts as described in section 3.2.1. The free spectral range was measured of $\Delta\lambda$ ∼0.66 nm as expected for a 500 μm long Fabry-Perot laser. The red-shift of the main emission peak when operating in CW is about 46 nm for a change in the stage temperature from 20 °C to 90 °C, or 0.65 nm/°C; the corresponding shift in band-gap is about 23 meV [Fig. 4.5(a)]. The characteristic temperature of the devices and a more detailed thermal characterization are reported in the next section. The same devices printed on a Si substrate and on a gold coated Si substrate operate in CW up to 110 °C. The emitted light power reaches ∼25 mW at 200 mA [Fig.

4.5(b)] depending on the thermal sink properties of the hosting substrate and the adhesion to it (see next section 4.3). The threshold current after printing was measured again of I_{th} ∼16 mA at 20 °C [Fig. 4.4(b)]. The turning voltage and the series resistance remained unvaried after integration. The spatial characterization of the far-field indicates a beam divergence of 60 degrees FWHM along the vertical axis and 19 degrees FWHM along the horizontal plane. A calculation of the Rayleigh range has been included in the simulation of the laser mode in section 5.1.

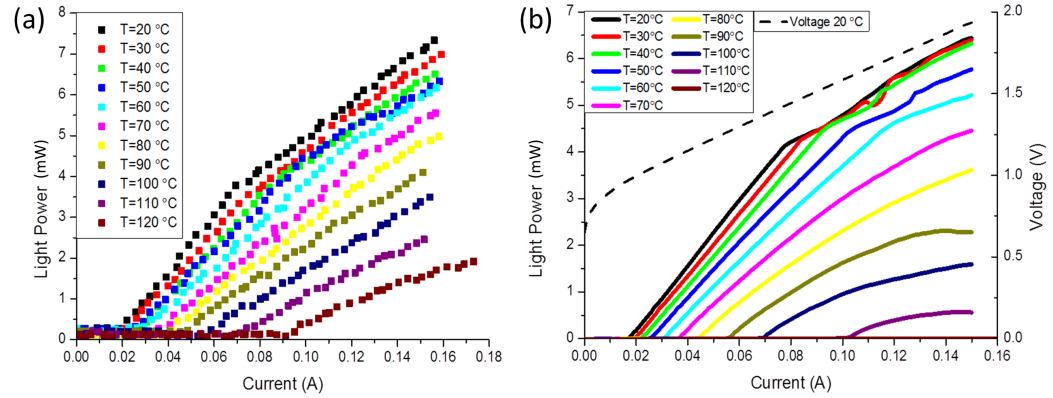


Figure 4.4: (a) Experimental L-I characteristics for the laser on the original InP wafer before the undercut and biased in PW-mode [4]. The device operated up to 120 °C. (b) The same laser biased in CW-mode works up to 110 °C, the turning voltage is of 0.8 V and the series resistance of ∼8 Ω.

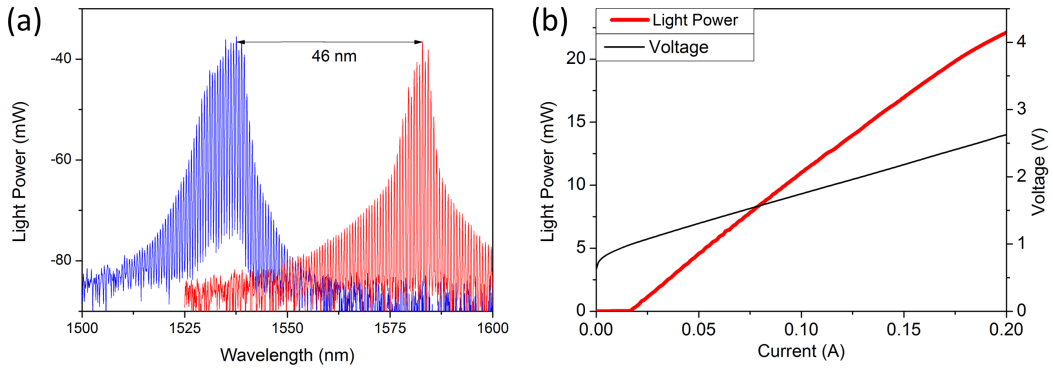


Figure 4.5: (a) Spectra of the laser on chip at 20 °C and 90 °C while operating at 100 mA. (b) Experimental L-I and V-I characteristics for a laser printed on Au-coated Si. The actual device exhibits threshold of ∼16 mA, emitted light power >20 mW at 200 mA and a series resistance of ∼8 Ω. [4].

4.3 Thermal characterization

The intrinsic thermal properties of the lasers and the heat sinking properties of the hybrid system were assessed by measurement of the characteristic temperature and thermal impedance of the lasers before and after μTP to different substrates. The analysis of the threshold current at different temperatures permits the extraction of the characteristic temperature, T_0, according to [eq. 4.2]:

$$I_{th} = I_0 e^{(T/T_0)} \Rightarrow T_0 = \Delta T / \Delta ln(I_{th}) \tag{4.2}$$

Where, I_{th} is the threshold current, I_0 is a fitting parameter, T is the temperature of the stage and T_0 is the characteristic temperature. High values of T_0 imply that the threshold current density of the device increases less with temperature. AlInGaAs lasers emitting at 1550 nm usually show T_0 in the range 50-100 K [6], [7]. T_0 was calculated from the L-I characteristics before μTP [Fig. 4.6] and by applying eq. 4.2 in the range of temperatures 20 °C - 90 °C [Fig. 4.6]. The measurements were performed in pulsed mode with 2% duty cycle and pulse width of 500 ns to ensure limited additional heating. The characteristic temperature of the laser is determined to be T_0 ~67 K.

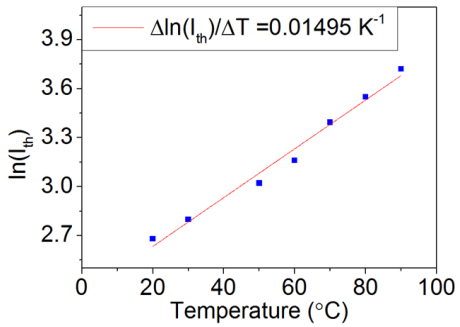


Figure 4.6: Logarithm of the threshold current against temperature was determined from the LIs at different temperatures reported in Fig. 4.4(a). The characteristic temperature of the lasers was determined to be T_0 ~67 K. [4].

The spectrum of the FP laser depends on the temperature of the active region. The emission wavelength is modulated by the gain curve which is related to the band-gap of the material that changes with temperature. The single FP mode shift with temperature is related to the effective refractive index of the active material and to the actual length of the resonating cavity. Variations of the electric power injected into the device and variations of the stage temperature vary the temperature of the active material. In turn,

the analysis of the wavelength-shift of a single FP mode can provide useful information on the thermal properties of the device. The analysis of the wavelength shift is usually not applied to the main peak of the spectrum as it can be affected by mode hopping that could misrepresent the real shift.

The thermal impedance quantifies the temperature rise of the laser junction for a given input power and thus how efficiently the heat can be removed to the heat sink. The experimental thermal impedance, Z_{EXP}, can be determined by comparing the shift in wavelength for an individual longitudinal single FP mode as a function of injected electrical power at room temperature, $\Delta\lambda_{FP}/\Delta P$, to the wavelength shift of an individual longitudinal mode given by a change in the stage temperature at a constant injected current $\Delta\lambda_{FP}/\Delta T$ [eq. 4.3].

$$Z_{EXP} = \frac{\Delta\lambda_{FP}}{\Delta P} / \frac{\Delta\lambda_{FP}}{\Delta T} \tag{4.3}$$

$\Delta\lambda_{FP}/\Delta T$ is measured in pulsed mode in order to ensure that there is minimal device heating other than that provided by the temperature controlled stage. Due to the increase of I_{th} at higher temperatures, the current injected into the devices is always of 100 mA in order to ensure above threshold current operation and enough light is emission from the laser when working at high temperatures. $\Delta\lambda_{FP}/\Delta T$ is measured to be 0.102$\pm$0.004 nm/K. The $\Delta\lambda_{FP}/\Delta P$ set of measurements are performed in CW. In all the experiments a single longitudinal mode in the laser spectrum is monitored. The experimental thermal impedance, Z_{EXP}, of the lasers on-chip and printed on different substrates are reported in Tab. 4.1. The lasers on the source InP wafer (before μTP) have a measured Z_{EXP} of 57 K/W. Lasers that are printed directly on bare Si show lower values of Z_{EXP} of 38 K/W, in this case the threshold current is similar to the devices on chip indicating there are no negative effects introduced on the device by μTP. The devices printed on a Ti : Au (10 nm : 150 nm) coated Si substrate show the lowest Z_{EXP} of 37 K/W. In particular, the introduction of this layer allows for potential electrical connections through the bottom side of the laser. The thermal impedance of devices printed on an adhesive or thermally insulating intermediate layer such as BCB or SiO_2 increases with the thickness of this layer. Lasers printed on SOI have Z_{EXP} of 94 K/W which is more than twice that of the devices on a 500 μm thick Si substrate. As the substrate material is highly influential on the resulting thermal impedance, some lasers were printed on ceramic AlN which is known to have high thermal conductivity with values depending on its preparation method. Here we used a 650 μm

thick AlN substrate (σ=170 $Wm^{-1}K^{-1}$) with surface roughness of 30 nm and up to 60 nm high grains that required a 60 nm thick BCB adhesive layer in order to bond the laser to the substrate. In this case, the thermal impedance was still comparable to the devices on chip and measured at Z_{EXP}=52 K/W. This experiment underlines once again the importance of having highly flat and smooth bonding surfaces in order to obtain adhesive-less printed devices and the best thermal sinking to the substrate [5].

Integration platform	Z_{EXP} (K/W)
On-chip InP (350 μm)	57 ± 4
Bare Si (500 μm)	38 ± 3
Ti : Au (10 : 150) nm	37 ± 2
SiO_2 (50 nm) on Si (500 μm)	43 ± 3
SiO_2 (1 μm) on Si (500 μm)	79 ± 4
SOI (top Si layer 220 nm)	94 ± 4
BCB (50 nm) on Si (500 μm)	56 ± 4
BCB (1.2 μm) on Si (500 μm)	206 ± 9
BCB (60 nm) on AlN (650 μm)	52 ± 3

Table 4.1: Experimental thermal impedances of lasers on the original InP substrate and transfer-printed on different target substrates. [4].

4.3.1 Simulated heat transfer

The junction temperature, T_{max}, of a laser depends on the amount of heat that is generated, on the location of the heat source, by the heat sink and the ambient temperature. Important parameters in the determination of T_{max} are the thermal conductivities and the geometry of the surrounding layers (including contact and passivation layers) and components (substrate, sub-mount, etc.). The heat generated by the laser is due to Joule heating associated to the series resistance of the device and by non-radiative processes such as Auger recombination and free carrier absorption which generate heat mainly in the active region or in the adjacent p- cladding layer [8], [9]. Here we consider a 500 μm long active region with cross section of 2.500×0.106 μm^2 as the source of power dissipation. This region is positioned under the ridge and above the 115 nm thick cladding layer and the 1.5 μm thick InP n-layer. We use σ=68 $Wm^{-1}K^{-1}$ for the whole epitaxial structure. If we include the lower thermal conductivity of the active region in the model, the increase in Z_t is simulated to be 0.5 K/W for the

laser printed on Si. The model considers a SiO_2 encapsulation layer which insulates the device at the top side making the heat dissipation possible only through the bottom surface, although this is not completely accurate as some heat could spread through the probes used for contacting the devices or in the surrounding air. The heat transfer characteristics of the laser were modeled using COMSOL Multiphysics [10] which uses Fourier's law of heat conduction to calculate the 2D steady state heat flow [11]:

$$q = -\sigma \cdot \bigtriangledown T \tag{4.4}$$

Where q is the heat flux, σ the thermal conductivity tensor and $\bigtriangledown T$ is the thermal gradient between the heat source and the heat sink. The finite elements model (FEM) provides 2-D cross-sectional temperature distributions for the laser on-chip and printed on the diverse platforms. The cross-section and the dimensions of the heterogeneous laser used in the model are illustrated in Fig. 4.7. They match the geometry of the lasers measured. The thermal parameters used for modeling the different materials are indicated in Tab. 4.2. It is important to note that the density ρ and the specific heat C_p do not influence the steady state simulations and are reported only for reference here.

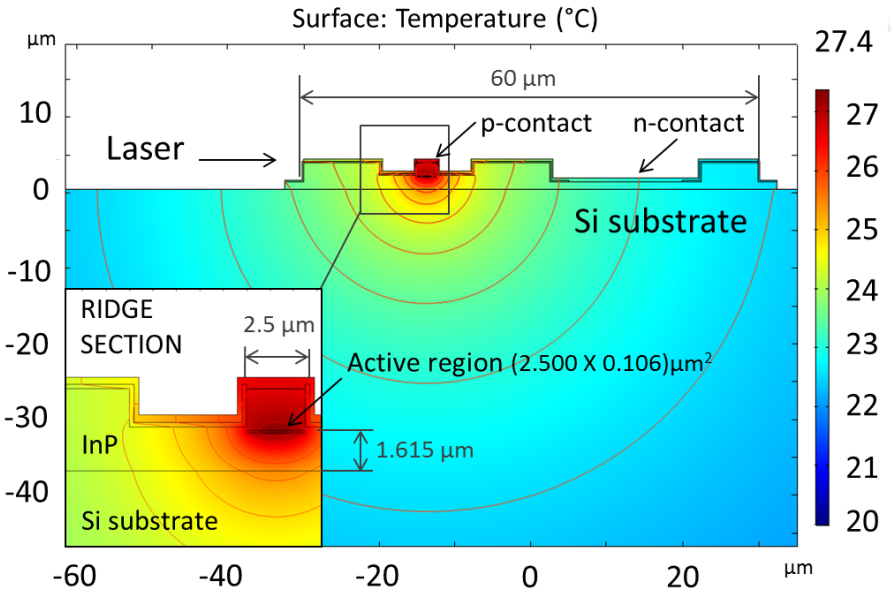


Figure 4.7: Cross section of the InP laser printed on a Si substrate (scale 1:1) and the simulated 2D-temperature distribution. T_{max}=27.4 °C is reached at 100 mA and 2 V bias. [4].

Material	ρ (Kg·m^{-3})	C_p (J·Kg^{-1}K^{-1})	σ (W·m^{-1}K^{-1})
InP	4810	310	68
InAlAs	4734	340	15
Si	2329	700	131
Au	19300	129	318
AlN	3300	740	170
BCB	957	2180	0.29
SiO_2	2200	730	1.4

Table 4.2: Density, ρ, thermal capacity, C_p, and thermal conductivity, σ, of the materials used in the model.

Each laser configuration is characterized by its theoretical thermal impedance, Z_t, which is approximated by the simplified steady-state analytic expression:

$$Z_t = \frac{\Delta T}{\Delta P} = \frac{T_{max} - T}{P_{el} - P_{opt}} \tag{4.5}$$

where ΔT is the temperature variation induced by the heating. T_{max} is the maximum temperature in the device and T is the temperature of the heat sink. ΔP approximates the heat generated in the junction per unit time and is given by subtracting the optical power emitted by the device, P_{opt}, from the total electrical power, P_{el}, injected into the device. P_{el} and P_{opt} are calculated from the experimental V-I and L-I characteristics. P_{el} is much larger than P_{opt} – the best lasers at this wavelength range have wall plug efficiencies <30% – and gives the strongest contribution to the determination of the thermal impedance. This highlights why heat management is a significant issue even for the most efficient laser devices. Finally, the simulations provide T_{max} for each configuration and eq. (4.5) allows the calculation of the thermal impedance. Table 4.3 compares the simulated and the experimental thermal impedances. All the Z_t values are calculated for the laser operating at 100 mA and for the heat sink temperature at 20 °C. For currents lower than ∼50 mA, the simulated ΔP is not linearly dependent on the injected current, due to its calculation from the experimental V-I and L-I curves. In this case eq. 4.5 is not reliable for the calculation of Z_t [Fig. 4.8].

A 500 μm long laser on the original 350 μm thick InP substrate before undercut has a simulated T_{max}=29.3 °C when operating at 100 mA. Considering an estimated thermal conductivity of the InAlAs layer, σ(InAlAs) 15 Wm^{-1}K^{-1} [12], [13], Z_t is calculated to be 60.5 K/W. The same laser without

Integration platform	Z_{EXP} (K/W)	Z_t (K/W)
On-chip InP (350 μm)	57 ± 4	60.5 ± 0.2
InP NO-InAlAs (350 μm)	-	57.3 ± 0.2
Bare Si (500 μm)	38 ± 3	38.0 ± 0.2
Ti : Au (10 : 150) nm	37 ± 2	37.5 ± 0.2
AlN (650 μm)	-	32.9 ± 0.2
SiO_2 (50 nm) on Si (500 μm)	43 ± 3	42.7 ± 0.2
SiO_2 (1 μm) on Si (500 μm)	79 ± 4	82.7 ± 0.2
SOI (top Si layer 220 nm)	94 ± 4	104.8 ± 0.2
SOI (Si substrate)	-	40.1 ± 0.2
BCB (50 nm) on Si (500 μm)	56 ± 4	54.0 ± 0.2
BCB (1.2 μm) on Si (500 μm)	206 ± 9	205.7 ± 0.2
BCB (60 nm) on AlN (650 μm)	52 ± 3	52.4 ± 0.2

Table 4.3: Comparison of the experimental, Z_{EXP}, and the modeled, Z_t, thermal impedances for the lasers printed onto different platforms. [4].

the InAlAs sacrificial layer would have Z_t=57.3 K/W. The thermal impedance for lasers printed directly on a 500 μm thick Si substrate is 38 K/W and is reduced to 37.5 K/W with a Ti : Au (10 nm : 150 nm) intermediate layer. Adhesive-less printing the laser to a 650 μm thick AlN substrate (σ(AlN) 170 $Wm^{-1}K^{-1}$) should give Z_t=32.9 K/W if ideal bonding can be achieved. With a 60 nm BCB adhesive layer Z_t rises to 52.4 K/W. If a 50 nm or 1 μm thick SiO_2 layer is interposed between the device and a Si substrate the simulated thermal impedance is respectively 42.7 K/W and 82.7 K/W. In particular, a laser printed on the 220 nm thick Si waveguiding layer on top of a 2 μm buried oxide and a 770 μm Si substrate (SOI) would have Z_t=104.8 K/W. The same laser printed directly on the 770 μm thick Si substrate of the SOI would have a reduced thermal impedance of 40.1 K/W. In the case where a 50 nm or a 1.2 μm thick adhesive BCB layers is used to bond a laser to a 500 μm thick Si substrate, Z_t is expected to be 54.0 K/W and 205.7 K/W respectively. The simulation results are within 10 % of our experimental results. Differences between experiment and model can be ascribed to less-than-optimum adhesion to the substrate given by interface roughness or difference in layer thickness. Heat spreading through the metal probes can also become significant, especially for situations with high thermal impedance to the substrate.

Changes in the geometry of the hybrid system have been investigated in

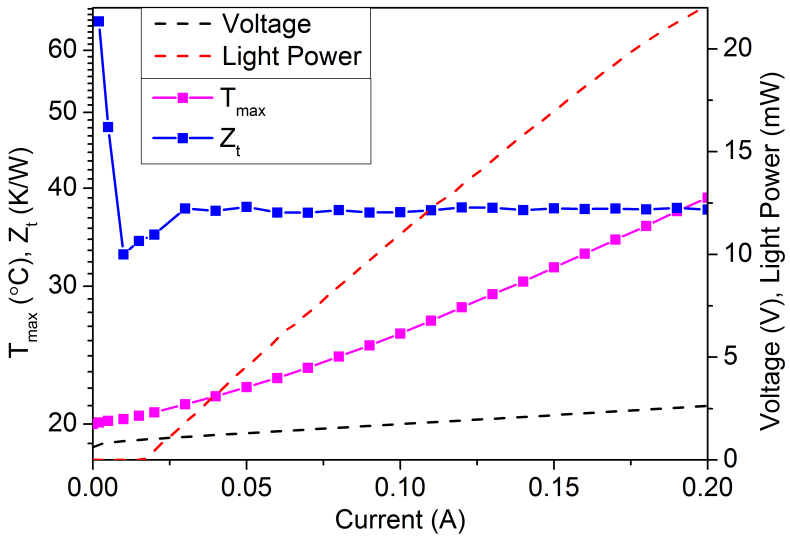


Figure 4.8: Experimental L-I and V-I characteristics for the laser printed on Au-coated Si along with the simulated T_{max} and Z_t. For currents higher than 50 mA, Z_t is within 0.2 K/W of its asymptotic value. The actual device exhibits threshold current of ∼16 mA, emitted light power >20 mW at 200 mA and a series resistance of 8 Ω. [4].

order to understand their effects on the thermal impedance. Lasers transfer-printed to highly thermally conductive substrates such as Si or AlN offer superior thermal impedance compared to those on the native InP [Fig. 4.9(a)]. Consequently, a lower limit for the thermal impedance of a heterogeneously integrated laser is set by the substrate, in particular by its thermal conductivity and only partially by its thickness (usually >350 μm). The variation of Z_t with the thickness of diverse intermediate layers between the Si substrate and the devices is reported in Fig. 4.9(b). Thick, highly thermally conductive intermediate layers only slightly enhance the thermal sink properties of the system while insulating layers reduce the heat sinking as their thickness increases. In particular, the simulation shows how a BCB layer thinner than 50 nm would reduce the Z_t of the integrated device. The lasers printed on top of an SOI wafer have shown more than twice the thermal impedance of those printed directly on the Si substrate. As shown in Fig. 4.9(c), the cross-sectional temperature profile of the SOI indicates that the heat tends to spread sideways and preferentially along the Si waveguiding layer potentially affecting other elements on the integration platform located at up to 100 μm far from the ridge. This is due to the insulating properties of the buried oxide. This issue could be addressed by defining thermally insulating trenches around the laser in order to channel the heat downwards but this would lead to a few K/W increase in Z_t. Moreover, the arrangement of such trenches at the front and the back facet can be difficult especially if the

SOI waveguide lies under the device as in the case of evanescent coupled devices. Printing the laser source directly on the substrate of the SOI offers a lower Z_t with another advantage being due to the thermal insulating properties of the buried oxide which prevents the heat to re-flow up towards the Si waveguiding layer and the other components on it. In the case of adhesive-less printing, Z_t decreases by a few K/W if the active region is closer than 3 μm to the substrate by thinning the n-InP layer. For standard edge coupled laser designs the thickness of this layer must be greater than 1.5 μm in order to avoid any modal interaction with the Si substrate [14], [5]. On the other hand, if a thermally insulating layer is interposed between the printed device and the substrate then a thicker n-InP layer helps the thermal sinking reducing Z_t [Fig. 4.9(d)]. In this case the heat produced per unit time is distributed on a bigger volume around the active region reducing T_{max} and so Z_t.

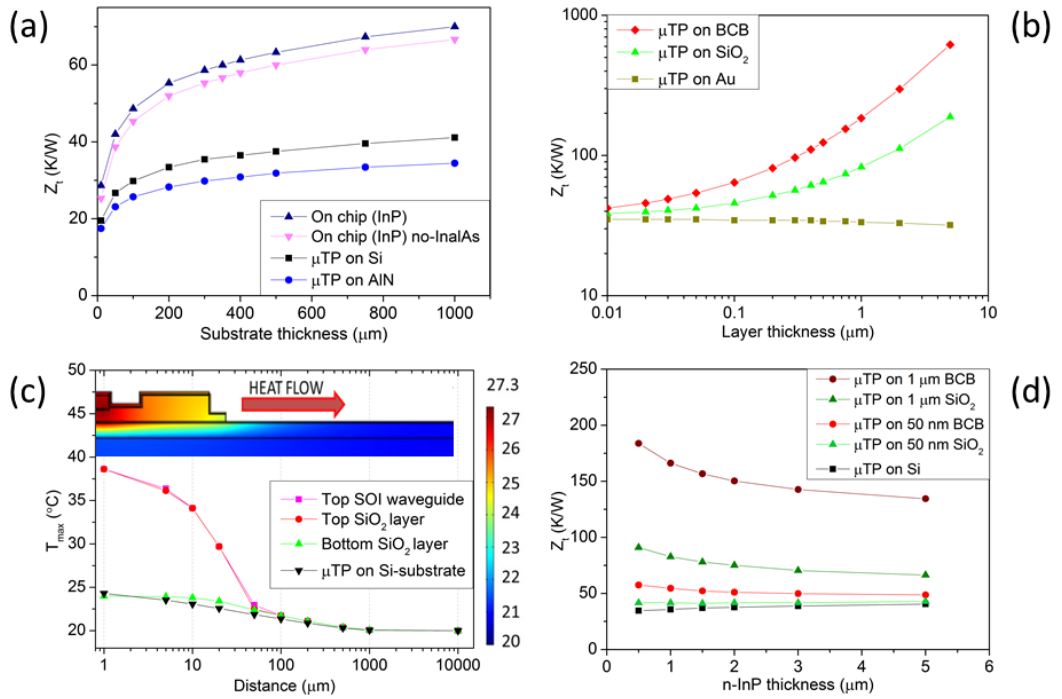


Figure 4.9: (a) Variation in Z_t with the substrate thickness for lasers on-chip and adhesive-less printed onto Si and AlN substrates. (b) Z_t dependence on the thickness of Au, SiO_2 or BCB layers interposed between the device and a 500 μm thick Si substrate. (c) Temperature profile along the different layers of the SOI when the laser is in operation. The inset shows a 2D-temperature profile (using the log-scale for distance) graphically illustrating the lateral heat spreading. (d) Z_t dependence on the thickness of the n-InP layer for different substrate configurations. [4].

Scaling analysis keeping the injection current constant shows that Z_t decreases inversely to the cavity length since the heat generation per unit area is correspondingly lower [Fig. 4.10(a)]. In the case the current density is

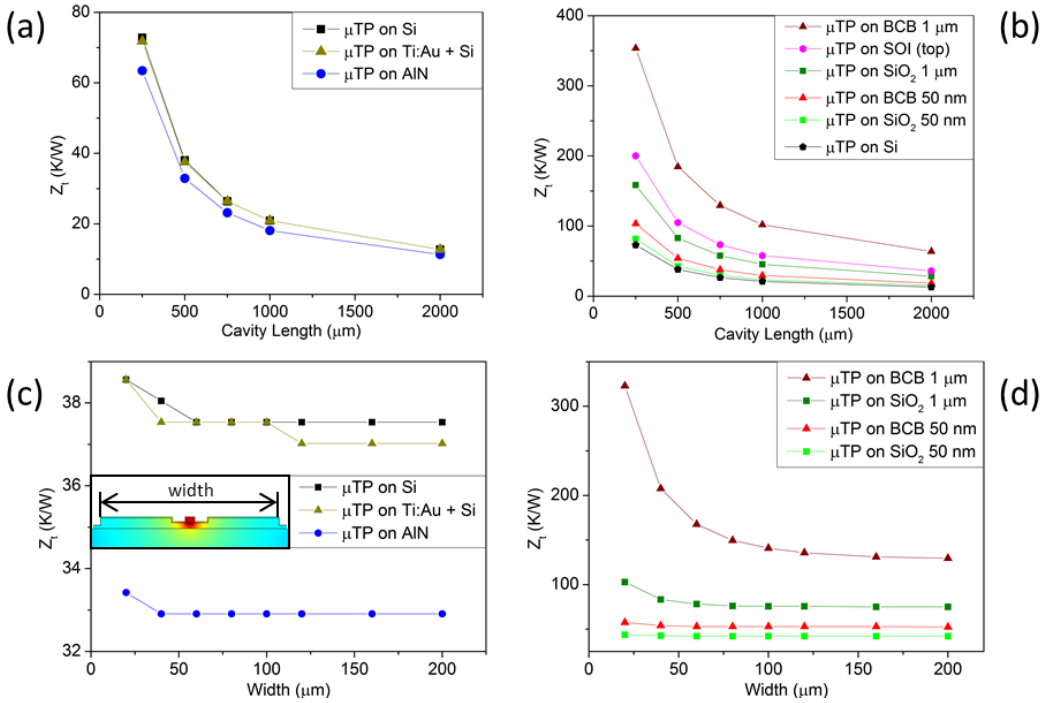


Figure 4.10: (a) Z_t dependence on cavity length for devices printed on highly thermally conductive substrates and (b) on thermally insulating interface layers. (c) Z_t versus width for coupons adhesive-less printed on highly thermally conductive substrates and (d) with thermally insulating adhesive layers. [4].

kept constant while varying the cavity length, the Z_t variation with the cavity length is even stronger. Z_t variations with the cavity length are reduced for lasers longer than 1 mm in both cases. A 1 mm device shows a simulated thermal impedance of 18.6 K/W. If the lasers are printed on an intermediate or adhesive insulating layer the variation in Z_t with cavity length is stronger, especially for cavity lengths <1 mm [Fig. 4.10(b)]. More generally, the thermal impedance of longer devices is less affected by the material and the thickness of the intermediate layer. While Z_t is lower for longer devices the absolute heat generated and the electrical power injected in a long laser may be higher than for shorter lasers due to the reduced slope efficiency of longer devices. It is important to find the right balance between the total heat produced by the device, the electrical power and the cavity length according with the final application. Changes in the laser coupon width were studied for lasers with the ridge in the center of the coupon and no n-contact recess [Fig. 4.10(c) inset]. Adhesive-less printed coupons wider than 60 μm exhibit a reduction of Z_t <1 K/W [Fig. 4.10(c)]. Reduction in Z_t with the width of the coupon is more evident for devices printed on thick insulating layers like SiO_2 or BCB [Fig. 4.10 (d)]. For a laser with electrical contacts on the top side, the distance of the n-contact recess to the active ridge only

marginally affects the thermal impedance of devices adhesive-less printed on Si or AlN, but can have an effect as large as a few K/W on devices printed on thermally insulating layers because of the higher lateral heat spreading. Increased thickness of the p-contact metal and reduced thickness of the dielectric layer used for passivation of the coupon can potentially reduce Z_t further. In order to estimate such reduction, the heat exchange to the surrounding air must be included in the model [3]. Use of metallic thermal vias from the top of the devices to the underlying substrate is also an option for reducing Z_t of devices printed on the thermally insulating layers.

4.4 Influence of μTP on the devices

The electrical and spectral characterization of the lasers were carried out before and after transfer printing to determine the the variation introduced by the transfer printing on the device performance. Lasers printed directly on bare Si exploit the high thermal sinking properties offered by a Si substrate and show Z_{EXP} as low as 38 K/W, in this case the threshold current is similar to the devices on chip indicating that there are no negative effects introduced on the device mirrors by μTP [Fig. 4.11]. Unaltered voltage current characteristics between the devices on-chip and those transfer printed on all the substrates involved indicate that the electric-contacts and the epitaxial material are not appreciably affected by stress occurring during the transfer printing process. The electrical performance of the devices printed on metal layers do not result appreciably degraded by eventual Au particles diffusion in the n-InP layer [15], compared to devices printed on other substrates. The spectral analysis reported in the previous section shows the influence of the substrate where the devices operate on the thermal impedance. Thermal effects due to the adhesion enhancement step at 300 °C (as described in section 3.4.3), exposure to solvents (as Acetone and IPA) and the environment did not introduce any variation in performance of the lasers indicating that the encapsulation layer preserves the materials correctly and that heating and cooling due to operation of the devices have negligible effects on the performance. Despite lasers printed on different substrates showed no degradation of the adhesion or the performance after sitting in the lab environment for about 2 years, an endurance test (Telecordia type) of the devices would be required to assess the adhesion and the performance over time.

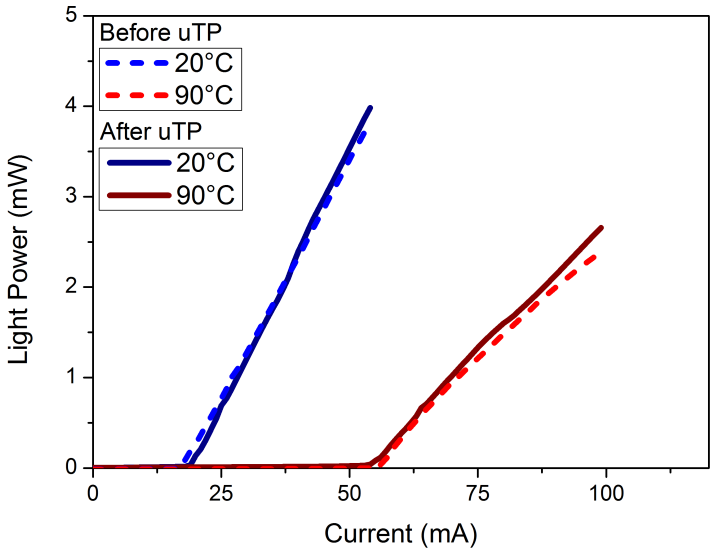


Figure 4.11: Comparison of CW - LIs for etched facet lasers on-chip and printed on Si. The light power before μTP is normalized to those printed on Si as the on-chip light collection is compromised by the adjacent devices. [4].

4.5 Conclusion

The work reported in this chapter shows how the etch facet technology developed combined to the engineering of the passivation layer has been vital to achieve state-of-the-art electro-optic performance with the InP transfer-printable lasers. The thermal analysis allowed to understand how the geometry of the devices and the layout of the integrated system can affect the heat sink and the device whole performance. Optimization is still required to control the reflectivity at the facet more accurately, to lower the series resistance and to improve the thermal performance. However, this analysis put the basis for the engineering of a suitable layout for the edge coupling of InP lasers to SOI, InP etched facet lasers were printed inside recesses on the SOI in order to achieve the vertical alignment of the laser waveguide to the SOI while achieving improved thermal sink to the Si substrate. The details of the work made to achieve an edge coupled laser are reported in the next chapter and represent the achievement of the final goal of integrating an InP laser to silicon photonics, which is the light coupling to the waveguide.

Bibliography

[1] a Newport Corporation brand Tyll Hertsens ILX Lightwave. *Measuring Diode Laser Characteristics, in An overview on laser diode chatacteristics, Appliction note, 5*. 2005. URL: https://www.newport.com/medias/sys_master/images/images/he9/hd7/8797049520158/AN05-Laser-Diode-Characteristics-Overview.pdf (visited on 03/26/2019).

[2] Newport Corporation Kamran S. Mobarhan. *Test and characcterization of laser diodes: Determination of principal parameters, in Appliction note, 1, fiber opptics and photonics*. 1999. URL: https://www.ele.uva.es/%20pedro/optoele/lasers/LD_parameters_Newport.pdf (visited on 03/26/2019).

[3] Zhi H Quan et al. "Thermal modelling of transfer-bonded thin-film gallium arsenide laser diode". In: *IET Optoelectronics* 10.2 (2016), pp. 51–56.

[4] Ruggero Loi et al. "Thermal Analysis of InP Lasers Transfer Printed to Silicon Photonics Substrates". In: *Journal of Lightwave Technology* 36.24 (2018), pp. 5935–5941.

[5] Ruggero Loi et al. "Transfer printing of AlGaInAs/InP etched facet lasers to Si substrates". In: *IEEE Photonics Journal* 8.6 (2016), pp. 1–10.

[6] Wang Yang et al. "High characteristic temperature InGaAsP/InP tunnel injection multiple-quantum-well lasers". In: *Chinese Physics Letters* 27.11 (2010), p. 114201.

[7] Yasuaki Yoshida et al. "Analysis of characteristic temperature for InGaAsP BH lasers with pnpn blocking layers using two-dimensional device simulator". In: *IEEE journal of quantum electronics* 34.7 (1998), pp. 1257–1262.

[8] Joachim Piprek, Patrick Abraham, and John E Bowers. "Carrier nonuniformity effects on the internal efficiency of multiquantum-well lasers". In: *Applied physics letters* 74.4 (1999), pp. 489–491.

[9] Joachim Piprek, J Kenton White, and Anthony J SpringThorpe. "What limits the maximum output power of long-wavelength AlGaInAs/InP laser diodes?" In: *IEEE journal of quantum electronics* 38.9 (2002), pp. 1253–1259.

[10] COMSOL Inc. *COMSOL Multiphysics Reference Manual, version 5.3*. 2019. URL: `https://www.comsol.com` (visited on 07/21/2019).

[11] COMSOL. "Heat Transfer Theory". In: *IEEE journal of quantum electronics* 4.0.9 (2010).

[12] Sadao Adachi. "Lattice thermal resistivity of III–V compound alloys". In: *Journal of Applied Physics* 54.4 (1983), pp. 1844–1848.

[13] Sadao Adachi. "Lattice thermal conductivity of group-IV and III–V semiconductor alloys". In: *Journal of Applied Physics* 102.6 (2007), p. 063502.

[14] John Justice et al. "Wafer-scale integration of group III–V lasers on silicon using transfer printing of epitaxial layers". In: *Nature Photonics* 6.9 (2012), p. 610.

[15] V Parguel et al. "Gold diffusion in InP". In: *Journal of Applied Physics* 62.3 (1987), pp. 824–827.

Chapter 5

Laser to waveguide light edge-coupling

The chapter reports the edge-coupling of the laser developed in this work to polymer and SOI waveguides. The devices have been integrated inside recesses pre-fabricated on the SOI by μTP, aligned to the coupling waveguide and thermally connected to the substrate for reduced thermal budget. The edge-coupling was initially developed for a large-spot-size (LSS) laser integrated to silicon photonics inside a recess and edge-coupled to a MSC defined on the SOI [1], [2]. Different layout of integration were analysed for achieving the edge-coupling of a Fabry-Perot laser to SOI. The devices were finally transfer-printed inside recesses of calibrated depth that allow vertical alignment of the laser waveguide with tenth of nanometer accuracy, μTP ensures $<\pm 1.5$ μm along the printing plane [3]. The process developed for creating recesses into the SOI, suitable for different layouts of integration, is presented. The strategy allows coupling the laser waveguide to a MSC converter in the SOI or to a polymer waveguide coupled to an SOI or to another device. The light edge-coupling was simulated with FIMMWAVE for maximum coupling efficiency. The layout developed paves a roadmap for active polymer-waveguide-based or hybrid polymer-SOI-waveguide silicon photonics integrated circuits.

Finally, the first O-band ridge laser with etched facets, integrated by μTP to recesses into the SOI and edge-coupled to a polymer waveguide is presented. The heterogeneous device was characterized by electrical and spectral analysis. The thermal performance were evaluated by simulations with COMSOL [4] and a layout for improved thermal sink is proposed.

5.1 Design of the Light edge-coupling

The edge-coupling was the strategy chosen to couple the light emitted by the laser waveguide to the SOI or to a polymer waveguide (as motivated in section 2.3). The highest potential coupling efficiency with this configuration is achieved when the laser mode field is matched to that of the waveguide in size and in phase. Tight <1 μm spatial alignment must be considered in order to achieve $\leq$1 dB injection losses when coupling the light from the device to the waveguide.

The first step in the design of the system to achieve the best coupling efficiency was to simulate the laser source using FIMMWAVE [5] in order to evaluate the mode size of the light generated. The ridge lasers developed show a single mode behaviour for ridges narrower than 2.5 μm. The TE_0 mode-size in the active region of a laser fabricated on the A2541 wafer (see Appendix A.2) under a 2.5 μm wide ridge is reported in Tab. 5.1 for different cross sections. A 3D and a section plot graphical representations are shown in Fig. 5.1. The mode size at the emitting facet is calculated to be very similar to that under the ridge section as it is not affected by the V-shape of the ridge at the facet [6]. After the determination of the mode size of the laser it was possible to dimension the cross section of a polymer waveguide edge coupled to the facet of the laser and sitting on a 3 μm thick oxide cladding of an SOI. The simulation aimed to achieve optimal mode matching between the laser and the waveguide and consequently the highest light coupling efficiency η. The simulations give η $\sim$98.5 %, with $\sim$83 % of the light transmitted into the fundamental mode TE_0 of the waveguide and the reflection at the interface laser facet to polymer-waveguide being of 15.5 %. The best SU8-polymer waveguide (of refractive index n $\sim$1.57) was simulated to be of 2.5 μm wide and with a $\sim$0.8 μm thick profile. In this case an air cladding is considered on top of the polymer waveguide. As an alternative a SiO_2 cladding can be included.

Mode-size	Horizontal (μm)	Vertical (μm)
FWHM	2.14	0.69
1/e	2.56	0.95
$1/e^2$	3.29	1.78

Table 5.1: Waist size of the laser TE_0 mode at different sections simulated with FIMMWAVE [5] for the device fabricated on the A2541 epitaxial structure.

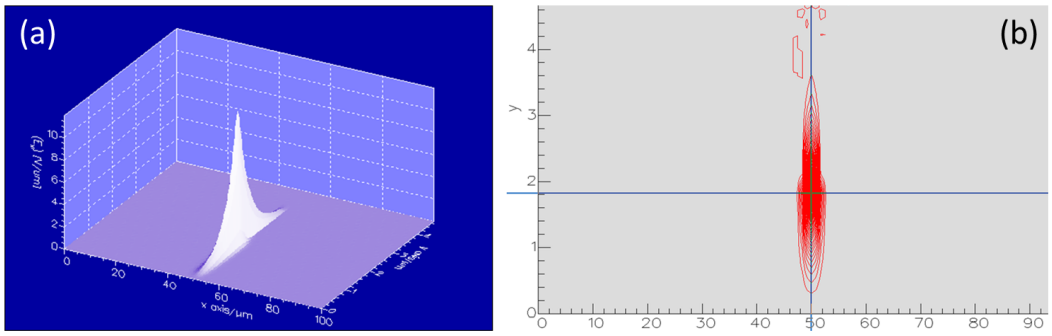


Figure 5.1: (a) 3D intensity profile of the mode propagating inside the active region of the laser. (b) cross section at the facet. The x scale is tuned to highlight the shape along the vertical axis.

The Rayleigh range z_R of the laser beam was calculated for the vertical component of the beam as it has the narrower waist. The light injected in the SU8-polymer waveguide has wavelength λ_0 =1.55 μm and the refractive index of the polymer at that wavelength is n(SU8)$\sim$1.57. For a mode size of 1.78 μm at $1/e^2$ along the vertical axis, the beam waist is ω_0=1.78/2 μm, consequently the Rayleigh range for the beam emitted in a infinitely wide SU8-polymer waveguide can be approximated by eq. 5.1:

$$z_R = \frac{\pi \cdot \omega_0^2 \cdot n}{\lambda_0} = \frac{3.14 \cdot 0.79 \cdot 1.57}{1.55} \simeq 2.53 \mu m \tag{5.1}$$

The Rayleigh range can be applied to estimate the distance for which the beam coming out of the laser adjusts to the new medium. This means that the edge-coupling studied is tolerant to longitudinal misalignment of up to 2.5 μm and in turn that the encapsulation ledge described in chapter 3 does not influence the coupling efficiency of the laser fabricated on the A2541 epitaxial structure. An accurate study of the longitudinal misalignment by using ledge-less coupons would be required to confirm this speculation.

The actual lasers coupled to polymer waveguides were fabricated as 2 μm wide ridge waveguides on the A2940 epitaxial structure emitting at 1340 nm wavelength and TM polarized (see Appendix A.3). The simulations of the mode size of the laser show a beam-waist of ω_0 $\sim$1.15 μm along the vertical direction [Tab. 5.2]. This is due to a higher confinement of the light in the active region of these devices compared to the lasers fabricated on the A2541 material. The smaller beam waist gives a reduced Rayleigh range of z_R $\sim$1.22 μm for emission in SU8-polymer, so the spacing given by the 1.4 μm wide encapsulation ledge present around the coupon could affect the light coupling efficiency in this case. Further experimental evaluation of the longitudinal misalignment versus coupling efficiency would

be required also in this case. The simulations show a light coupling efficiency of η ~90.5 % for a 1 μm thick and 3.2 μm wide SU8-polymer waveguide, the light transmission into the fundamental mode TM_0 of the polymer waveguide is ~75 % and the reflectivity at the facet of the laser is of 15.5 %. The simulated polymer waveguide lies on a 3 μm thick oxide lower cladding and it is surrounded by an air cladding at the top. The study of the lateral misalignment was performed with LUMERICAL software and the (FDTD) solver included in the [7] with a model of the actual laser built by F. Floris; the vertical misalignment was determined with FIMMWAVE using the FDM solver. The results shows a <1 dB loss of coupling efficiency for $\Delta x < \pm 1.1$ μm and $\Delta y <$+0.2 μm and $\Delta y <$-0.7 μm, respectively [Fig. 5.2]. The asymmetric behaviour of the light coupled when moving the laser vertically [Fig. 5.2(b)] is due to the geometry of the system with the cladding below the polymer waveguide and the air on top of it.

Mode-size	Horizontal (μm)	Vertical (μm)
FWHM	1.93	0.50
1/e	2.40	0.66
$1/e^2$	3.25	1.16

Table 5.2: Waist size of the laser TM_0 mode at different sections, simulated with FIMMWAVE [5], for the 2 μm wide ridge lasers fabricated on the A2940 epitaxial structure.

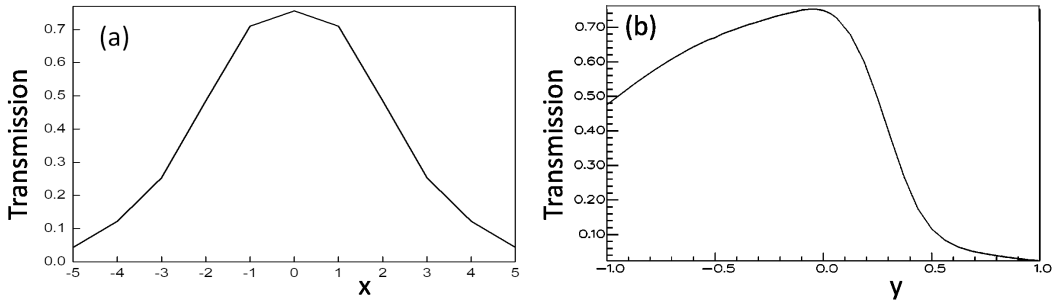


Figure 5.2: Study of the light transmission from the laser to the polymer waveguide versus (a) lateral (x) and (b) vertical (y) misalignment (in μm) simulated with LUMERICAL [7] and FIMMWAVE [5] respectively.

5.2 Integration strategies

A laser edge-coupled to the SOI requires to be integrated inside a recess in the SOI in order to achieve alignment of the emitting facet to the SOI along the vertical axis. Recesses suitable for transfer printable edge-coupled devices require alignment markers for lateral alignment and vertical sidewalls with facet quality defined at the end of the SOI waveguide or the MSC for maximum coupling efficiency, the etch must not damage the delicate tip of any taper on the SOI. As the position of the III-V die along the vertical axis inside the recesses has to be calibrated carefully, different configurations have been designed to achieve this objective [Fig. 5.3]. The first layout shows a recess etched to the Si substrate and a III-V laser printed in direct contact to the Si substrate with the n-InP layer of calibrated thickness that positions the laser waveguide in-line to the SOI waveguide [Fig. 5.3(a)]. This layout provides the best thermal sink and performances (see section 4.3 or [8]), but requires growth of a thick and calibrated n-InP cladding. If the n-InP layer has a not calibrated thickness, then a metal layer of proper thickness of typically >500 nm (for lasers coupled to a 2 μm thick oxide SOI) can be evaporated at the bottom of the recess on the Si substrate with $\pm$10 nm tolerance [Fig. 5.3(b)]. Another option is to calibrate the recess depth into the buried oxide layer of the SOI and then adjust finely the height of the coupon by evaporating a <200 nm thin metal layer at the bottom of the recess [Fig. 5.3(c)]. This metal layer can be connected to the substrate through a secondary trench and work as a thermal via and as n-electrical contact. This strategy removes the requirement of calibrating the n-InP layer thickness or evaporating a thick metal layer. The same three layouts can be applied for edge-coupling the laser to a polymer waveguide sitting on a cladding layer or for edge-coupling to a MSC. Fig. 5.3(d) reports a diagram of the layout in Fig. 5.3(c) applied to edge-coupling of an InP laser to a polymer waveguiding section working as a MSC connected to the SOI.

5.2.1 Formation of recesses in the SOI

Two main fabrication processes for recesses have been developed in this work for the different layouts of recesses designed. The processes are described here and the detail of the fabrication steps are reported in Appendix D. The first type of recess (Recess type 1) suits the layouts shown in Fig. 5.3(a, b), the recess is fully etched to the Si substrate and the laser can be printed in direct contact to the Si substrate or on a metal layer deposited on

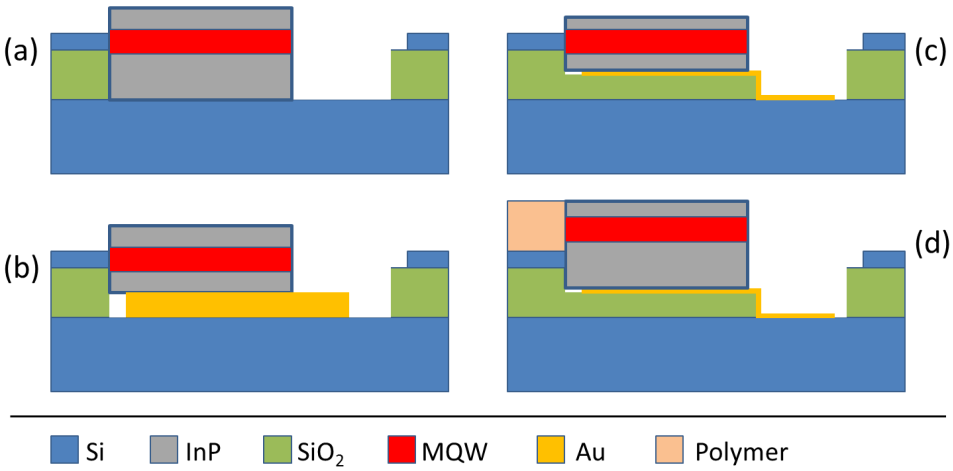


Figure 5.3: Possible layouts for edge-coupling a laser by printing in a recess. (a) A laser die with an n-InP layer of calibrated thickness aligned to the SOI while in direct contact to the Si substrate. (b) A laser aligned to the SOI with an intermediate metal layer of calibrated thickness. (c) A laser printed in a recess of calibrated depth, a thin intermediate metal layer provides fine tuning of the vertical alignment to the SOI and heat sink to the Si substrate. (d) Same layout as (c) for light coupling to a polymer waveguide.

the Si substrate at the bottom of the recess [Fig. 5.4(a-d) and Fig. 5.5(a)]. The second design (Recess type 2) is suitable for edge-coupling an arbitrary thick laser to the SOI (as shown in Fig. 5.3(c, d)) and does not require the evaporation of a thick intermediate metal layer at the bottom of the recess. In this case the recess is dry-etched into the oxide layer without reaching the Si substrate, then a thin (<200 nm) metal layer is deposited at the bottom of the recess for fine adjustment of the height of the coupon to the SOI and for thermal sink to the substrate through a trench arranged close to the printing area [Fig. 5.4(e-i) and Fig. 5.5(b)]. Both types of recesses must have vertical sidewalls that allow matching the emitting facet of the laser to the SOI and flat and smooth bottom surface suitable for direct printing. Spinning of adhesive layers can problematic as the thickness of the adhesive layer inside trenches is not easily predictable as on flat surfaces. An unwanted adhesive layer thickness generates issues on the alignment and on the thermal performance [8]. The best way to introduce adhesives in the process is to spray coat or evaporate them (as discussed in 3.4.2). Lodgements for eventual remnants of tethers and grating can be defined at the sidewalls especially if matching the coupon to two of the sidewalls of the recess. A schematic of the layout designed for edge-coupling a laser to a polymer waveguide and to the SOI by integrating it in a recess type 2 by transfer printing is reported in Fig. 5.6.

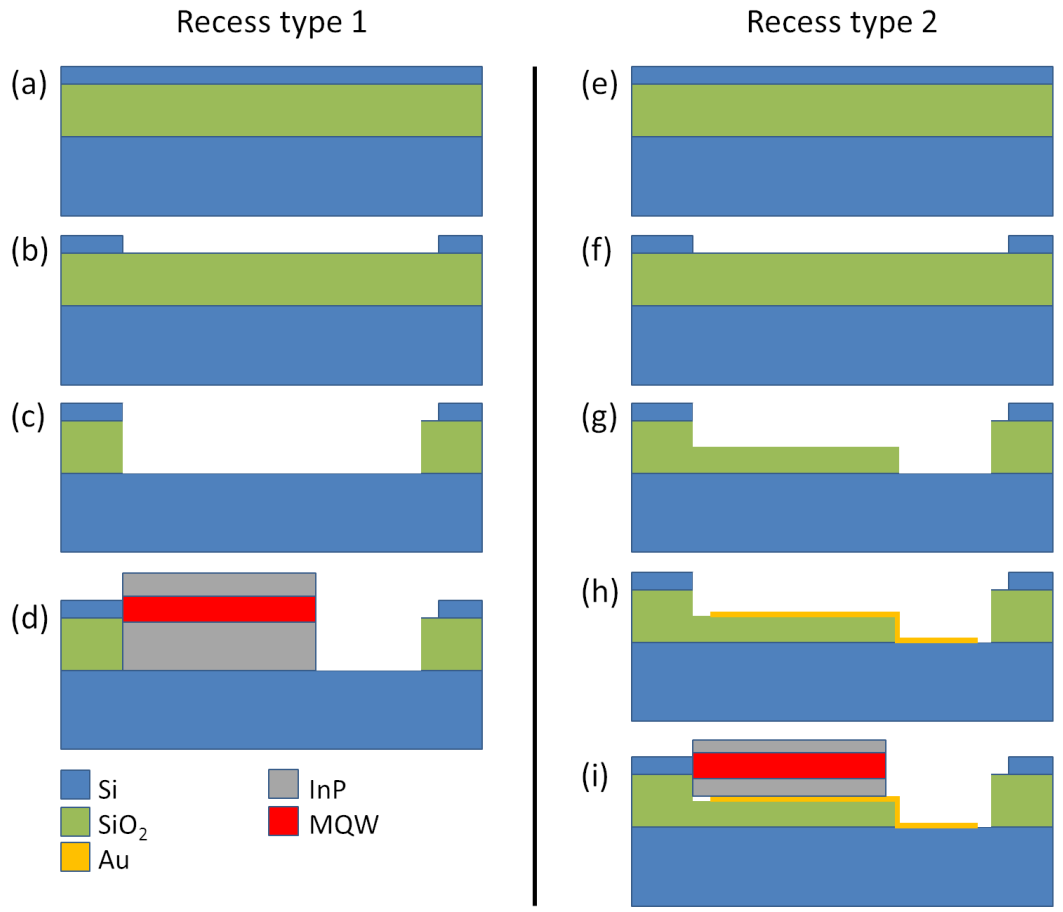


Figure 5.4: Fabrication of type 1 and type 2 recesses. (a) Type 1 recesses are formed on the SOI wafer by (b) etching the Si layer and (c) by etching down to the Si substrate. (d) The active region of a laser coupon of specific thickness can be edge coupled to the SOI waveguide with or without an intermediate metal layer. (e) Type 2 recesses are created by dry-etching the SOI layer, (f) the oxide (without reaching the Si substrate) and (g) a recess to the Si substrate; (h) then a metal layer is evaporated to adjusts the recess depth and sinks the heat to the substrate. (i) In this case coupons of different thickness can be integrated and edge coupled to the SOI or a polymer waveguide.

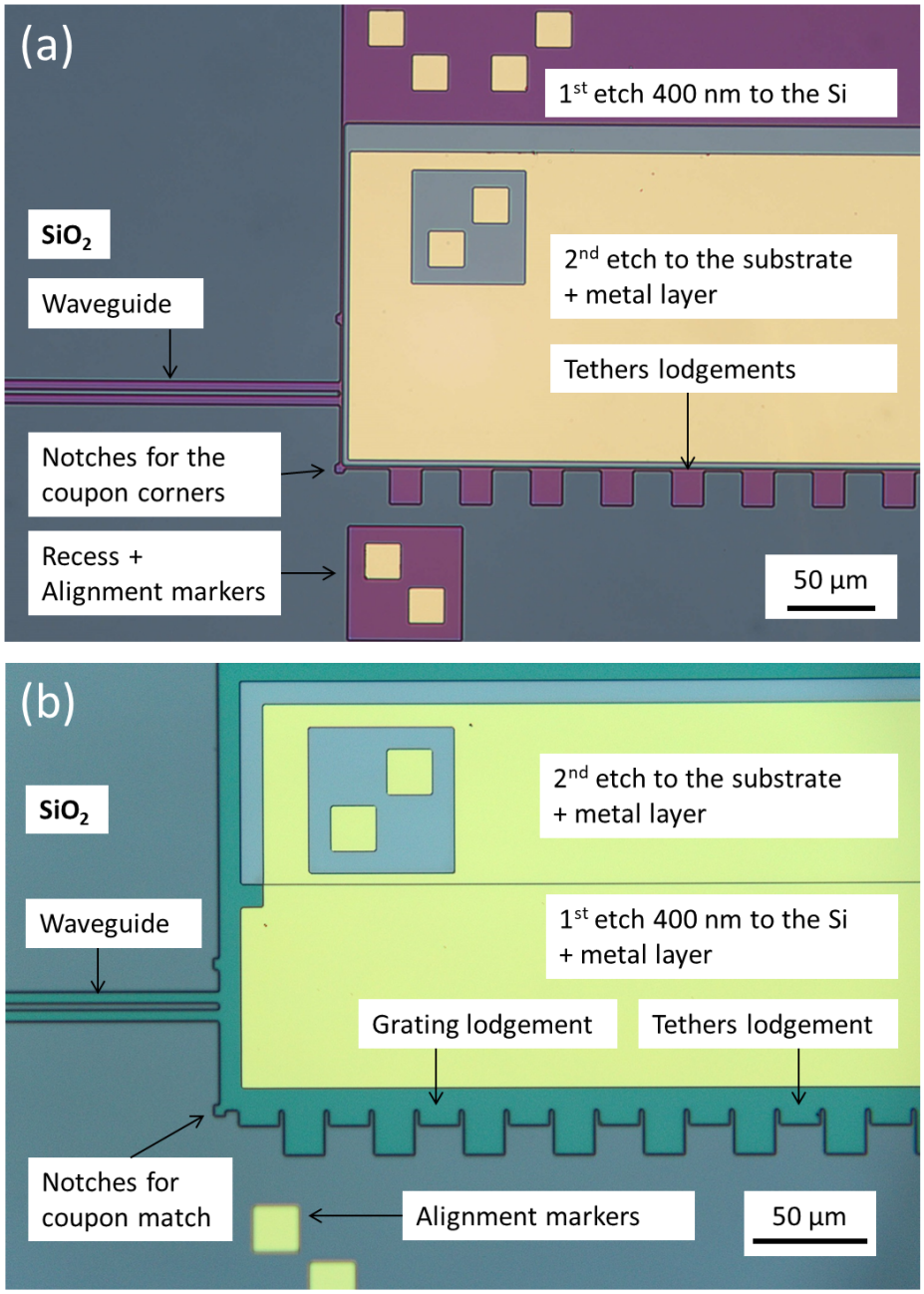


Figure 5.5: (a) Recess type 1 etched in two steps (dry- plus wet-etch) to the Si substrate with a ∼600 nm thick metal layer at the bottom of it. The sidewall have been protected while etching the recess. (b) Recess type 2 in the SiO_2, etched 400 nm to the Si substrate with ∼200 nm metal layer that connects to the Si substrate.

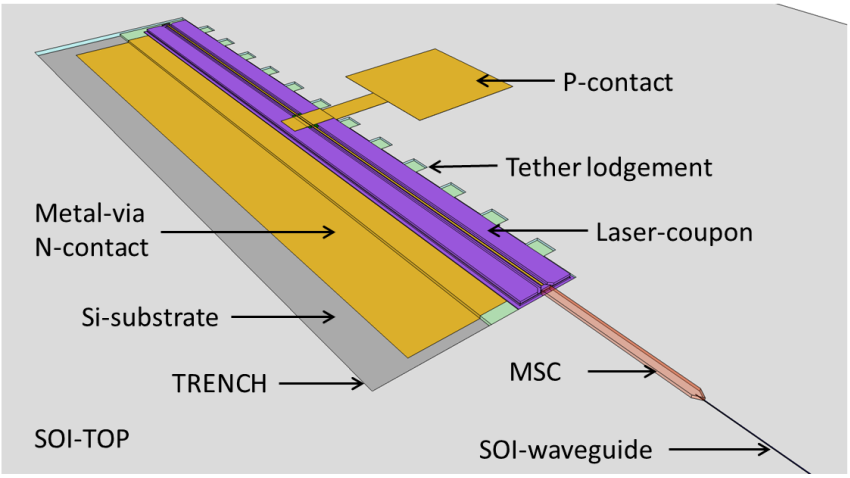


Figure 5.6: Diagram of a laser printed in a recess coupled to a polymer waveguide and then to the SOI; a thermal via underneath the device sinks the heat to the Si substrate and allows for electrical contacting to the n-InP.

Type 1 recesses were dry-etched into the SiO_2 and finished by wet-etch in a HF based acid solution (BOE 5:1) in order to prevent formation of defects on the Si substrate surface. In fact, dry-etching to the Si substrate results in rough surfaces not suitable for direct printing [Fig. 5.7(a)]. During the wet-etch it is important to protect the sidewall from being etched by the BOE, a resist polymer layer is applied for this purpose and a particular process has been developed for it. The resist layer is patterned by lithography with 5 μm smaller rectangular openings arranged inside the main recesses, then the remaining SiO_2 is wet-etched to the Si substrate while the polymer protects the sidewalls of the recess [Fig. 5.7(b)]. This strategy leaves a $\sim$2.5 μm wide ledge at the foot of the sidewall after the wet-etch of the remaining oxide which could prevent matching the coupon to the sidewall. In this case a calibrated over-etch in BOE would remove it. Alternatively, if an intermediate metal layer is used for adjusting the height of the coupon it must be kept thicker than the oxide ledge in order to allow the coupon to be matched to the sidewall without physical obstacles. This layout offers accurate alignment and superior thermal performance as the bottom of the device sinks the heat directly to the Si substrate (as discussed in section 4.3). On the other hand the epitaxial growth of thick n-InP layer could reduce the thermal sink [8] and be expensive; Moreover fabrication of thicker coupons is harder to implement and transfer printing could be not obvious. Similarly, the evaporation of thick metal layers can be expensive and requires extra care in the preparation of the Si surface and in the evaporation parameters for achieving flat and smooth surfaces suitable for μTP. A flat and smooth

metal layer is vital for achieving direct printing or to bond with thin adhesive layers. Imperfections and dirtiness present on the starting surfaces or use of fast rate metal evaporations can lead to seeding effects which create protrusions up to 800 nm in diameter on the final surface [Fig. 5.8]. These defects require the coupons to be printed with a thick adhesive layer which affects the vertical alignment of the coupon. An experiment was conducted to determine the influence of the surface preparation, three samples were prepared with a different procedure:

- Bare Si in 1165 solvent [9] (90 °C, 15 minutes).
- Bare Si in 1165 solvent (90 °C, 15 minutes) + O_2 Plasma (100 W, 5 minutes).
- Bare Si in 1165 solvent (90°C, 15 minutes) + H_2SO_4:H_2O_2:H_2O (1:1:3) (10 s).

The sample treated with sulphuric acid provided better metal surfaces with smaller defects of up to 150 nm in diameter that appear on the surface with very low density. A reduced evaporation rate was lately proven to be the most effective strategy for reducing the imperfections at the surface. Thin metal layers of thickness <200 nm with quasi-defect-free surfaces can be evaporated by using a 1 Å/s deposition rate.

Recesses of type 2 were dry-etched in the SOI providing high quality surfaces suitable for direct printing. The smoothness of the final surface depends mainly on the initial surface quality. A low rate 1 Å/s flat evaporation of Ti:Au (10:110) nm and a following low rate 1 Å/s 360° angled Ti:Au (10:40) nm evaporation ensured the creation of a smooth flat metal layer suitable for adhesive-less printing at the bottom of the recess. The resulting surface of the metal layer achieved with slow rate evaporation shows flatness of <0.03 nm/μm and nominal roughness of <1 nm along a 100 μm linear profile. A flat and smooth metal layer is vital for achieving direct printing as imperfections and debris present on the metal surfaces require thick adhesive layers that would affect the alignment and the thermal performance [8]. High flatness and smoothness of the underlying SiO_2 surface is vital to prevent defect formation on the metal layer. Evaporation on rough SiO_2 substrates need an extra care as defects can affect the final metal layer smoothness [Fig. 5.8]. The metal layer was connected to the Si substrate creating a thermal via for the heat sink. The metal layer thickness can be tuned with $\pm$10 nm accuracy and it allows accurate alignment of the laser

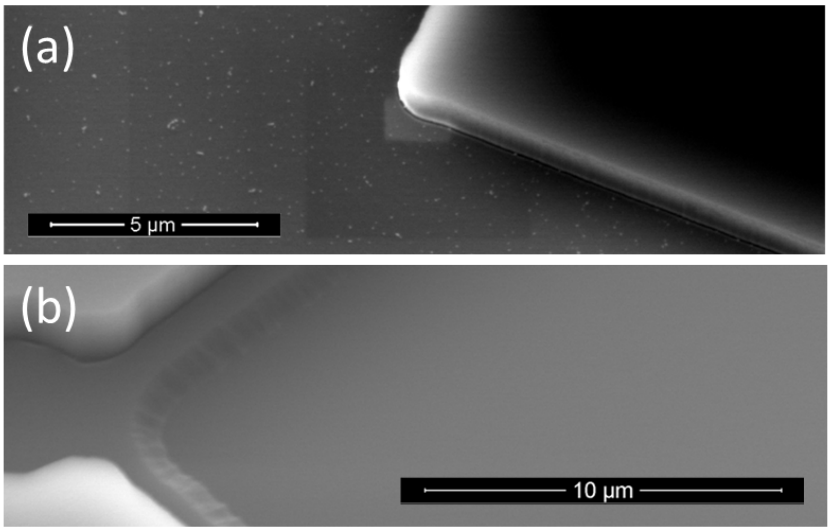


Figure 5.7: (a) SEM image of a recess in the SOI. The dry-etch to the Si substrate creates defects at the surface which lower the yield of printed devices. (b) The etch of the SiO_2 to the Si substrate made in two steps (dry plus wet-etch) by using a resist layer protects the sidewalls during the wet-etch and provides clean surfaces. The ledge at the bottom of the sidewall has to be lower than the eventual metal layer which tunes the height of the coupon.

waveguide to the polymer waveguide along the vertical axis. This design is suitable for edge-coupling laser coupons with different n-cladding thickness to polymer and SOI waveguides.

5.3 Edge-coupling of InP lasers to polymer waveguides on silicon photonics

The edge-coupling of C-band InP-based etched-facet lasers to SOI has been recently demonstrated as reported in section 2.1.4. [1], [10], [2]. In this case the recesses were similar to type 1 recesses developed in this work and they were formed by using a chrome mask with the etching stopped at the interface with the silicon substrate. The aim of using a chrome mask was to achieve straighter profiles with reduced curtain effect (as discussed in section 3.2.4). The sidewalls of the recess were etched just at the edge of the trident MSC for optimal longitudinal alignment of the laser to it which makes challenging not to damage the tips of the trident. The lateral alignment of each laser relied on high contrast fiducial markers present on both the laser and on the target substrate and was $\leq \pm 1$ μm. The resulting printed lasers were recessed from the waveguide facet by ~ 3 μm along the longitudinal

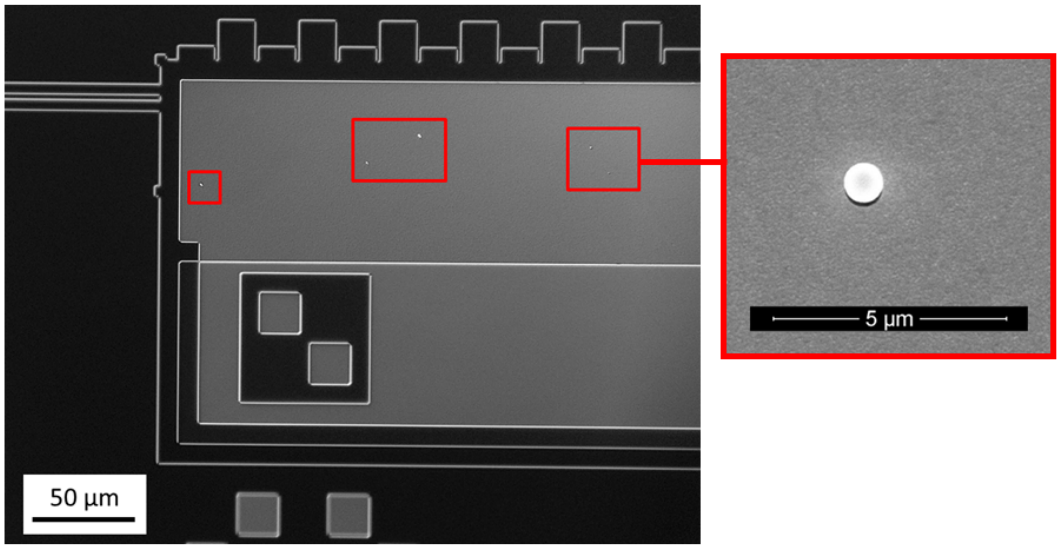


Figure 5.8: Digital microscope Nomarski-image of a recess in the SOI with the metal layer deposited on a rough SiO_2 surface and connected to the Si substrate for thermal sink. The portion of metal on the SiO_2 shows higher defect density at the surface. The inset shows a SEM picture of one of the defects formed at the metal surface.

axis. The vertical alignment was achieved by a calibrated thickness n-InP layer.

A similar approach has been applied for edge-coupling InP lasers to a polymer waveguide defined on the oxide layer of an SOI [Fig. 5.9] [11]. The silicon photonics chip was fabricated as an array of aligned type 2 recesses suitable for accommodating devices that could face each other and that could be connected by straight polymer waveguides, or by hybrid polymer-SOI waveguides. Two lasers were heterogeneously integrated by μTP into the recesses and one of them was edge-coupled to an SU8-polymer waveguide coupled to an SOI waveguide. The integration strategy involves shearing the coupon to the sidewall while in light contact to the bottom of the recess and then bonding the coupon when matched. The edge-coupling configuration requires mode size matching between the laser and the waveguide or a MSC, then particular care of the alignment of the emitting facet to the waveguide is required for high light coupling efficiency, especially along the vertical axis due to the narrower waist of the mode along that axis. The depth of the recesses for achieving efficient light coupling between the laser and the polymer waveguide has to be determined by the thickness of the laser and of the mode matched polymer waveguide. The approach developed allows the adhesive-less μTP of generic thickness InP transfer printable devices in a desired location and on the desired layer of the SOI while

achieving accurate alignment of the emitting facet to the SOI. This strategy enables the creation of PICs based on pre-fabricated devices connected by polymer waveguides or hybrid polymer-SOI waveguides.

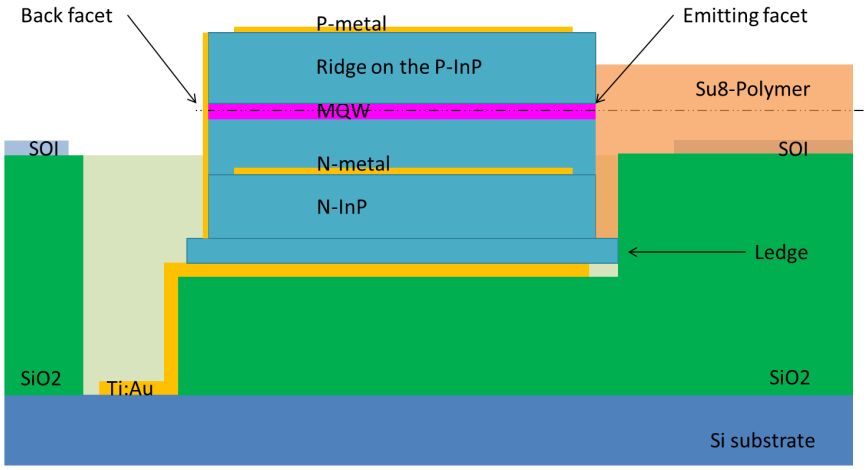


Figure 5.9: Diagram reporting the longitudinal cross section of the laser printed in a recess on the SOI and edge coupled to an SU8-polymer waveguide connected to an SOI tapered waveguide.

5.3.1 Laser devices

The lasers were pre-fabricated on the A2940 source InP wafer which offers emission in the O-band with *TM* polarization. The devices were fabricated with a process similar to that described in section 3.2 as 550 μm long and 60 μm or 80 μm wide coupons. A 2 μm wide ridge etched just above the active region provides the lateral confinement of the light for single mode output. The 500 μm long Fabry-Perot cavity were defined by dry-etched facets passivated by an optically neutral SiO_2 layer, the back facet of each laser was then coated with a reflective $Ti : Au$ $(5 : 200)$nm metal layer. Accessible P- and N-type metal contacts were defined for testing the devices before and after transfer. The fabrication of the lasers included the steps for preparing the coupons to the undercut and the μTP as discussed in section 3.1 and in previous work [12], [6]. The coupons were released from their native substrate by selectively etching a 500 nm thick InAlAs sacrificial layer arranged at the bottom of the N-InP cladding in $FeCl_3$:H_2O (1:2) kept at 1.0$\pm$0.1 °C for maximum selectivity to InP. The resulting suspended devices were then picked up and transfer-printed epitaxial-side-up to pre-fabricated recesses on the SOI.

5.3.2 Recesses on the SOI

A 220 nm SOI layer on a 3 μm thick buried oxide cladding was patterned to create an array of 1.54 μm deep rectangular recesses suitable for edge-coupling to polymer waveguides [Fig. 5.10]. Electron-beam (e-beam) lithography and a dry-etch opened the 220 nm thick SOI layer to define the recess areas and some 0.6 μm wide single mode tapered waveguides. A second dry-etch into the SiO_2 with an end-point detection allowed etching a 1.32 μm deep recess; a third dry-etch to the Si substrate defined type 2 recesses. A low rate evaporation created a 170 nm thick metal layer suitable for adhesive-less printing at the bottom of the recess, with nominal roughness of <1 nm and flatness of <0.03 nm/μm. The metal layer was connected to the Si substrate creating the thermal via for the heat sink.

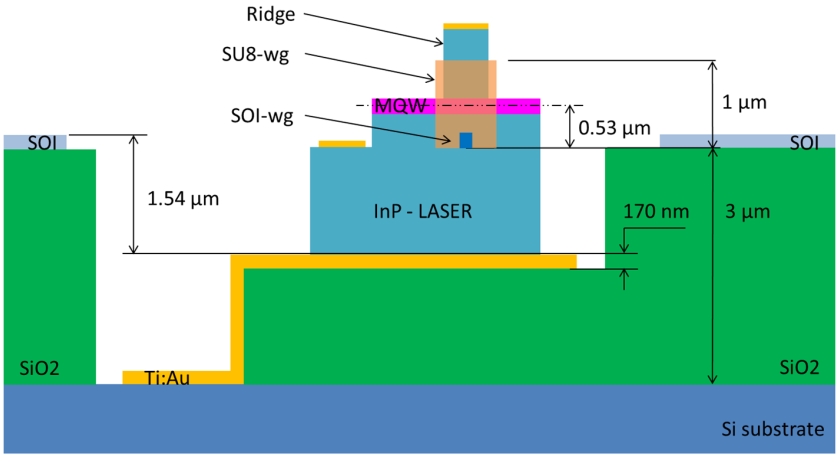


Figure 5.10: Diagram of the transverse cross section of the laser printed in a 1.54 μm deep recess formed on the SOI, the 170 nm thick metal layer allows tuning the height of the active region (MQW) to 0.53 μm above the oxide layer, the 1 μm thick SU8 waveguide is aligned to the ridge. [11].

5.3.3 μTP of the lasers to the SOI

The layout of integration developed for type 2 recess allowed engineering the alignment of the laser along the vertical axis and thermal sink to the substrate. The alignment of the emitting facet to the SOI along the two remaining spatial directions ofΔx=1.6 μm and Δz=0.0 μm was achieved by μTP in full manual mode and without using alignment marker and pattern recognition [Fig. 5.11]. The integrated laser was completely matched to one of the sidewalls [Fig. 5.11 inset], however the 1.4 μm wide encapsulation ledge spaces the facet of Δz $\sim$1.4 μm to the recess sidewall along the longitudinal axis being just out of the Rayleigh range of the beam of the laser for

emission in a free space of SU8-polymer (z_R ~1.22 μm). The rotation of the laser has been estimated of <±0.001 degrees angle by measuring, at the digital microscope, the distance from the nose and the tail of the coupon to the edge of the recess defined by e-beam lithography. Matching of InP coupons to two of the sidewalls has been explored during this work to reduce the lateral misalignment and rotation, no lasers have been printed on the SOI with this strategy. The results show that it is possible in principle, as long as the corners of the recess are not rounded, this underlines the importance of having notches at the corners of the recess to achieve complete match of the coupon to sidewalls of the recess. The same considerations must be applied to lodgements for the tethers and the grating remnants. As the application of a nanometer scale thin vapour coated HMDS layer improved the yield of printed arrays of ~20 devices from >90 % to 100 % over a Au coated Si substrate, a layer of HMDS was applied inside the recesses before μTP.

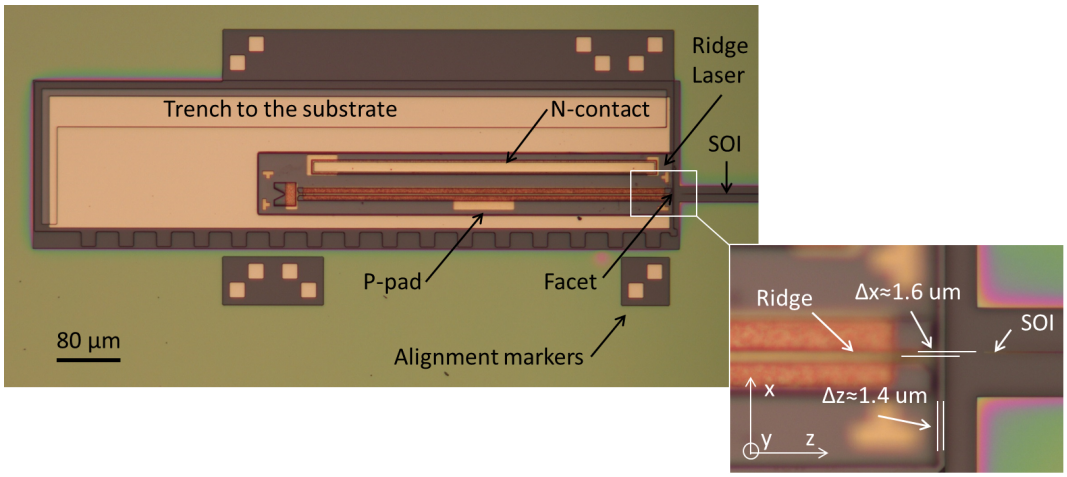


Figure 5.11: Digital microscope image of a laser printed in a type 2 recess in the SOI. A zoom on the emitting facet shows a misalignment of Δx ~1.6 μm and Δz ~1.4 μm to the SOI given by the encapsulation ledge.

5.3.4 Edge-coupling to the polymer waveguide

A straight polymer waveguide was defined post-integration on top of the SiO_2 cladding and edge coupled to the laser [Fig. 5.12(a)] with <1 μm lateral misalignment to the ridge [Fig. 5.12(b)]. A SU8-polymer layer of 1.5 μm thickness was spun on the SOI after printing the devices in the prefabricated recesses. The thickness of the polymer layer was targeted at 1 μm with the difference between expected and actual thickness due to the topography present on the SOI. An etch-back of the polymer waveguide

can be applied to bring the height of the waveguide back to 1 μm. An e-beam lithography defined a 7.5 μm wide and 2 mm long waveguide edge coupled to the ridge of the laser with <0.7 μm misalignment. Simulations with FIMMWAVE suggest the best coupling of 90.5 % is to a 3.2 μm wide polymer waveguide. The complete matching of the polymer waveguide to the facet of the laser is achieved by defining the waveguide over the coupon for a length of 0.5 to 1 μm [Fig. 5.13]. The polymer waveguide incorporated a parallel SOI waveguide positioned at 4.75 μm distance from the edge of the recess. This strategy allows etching the recesses without impacting the 140 nm wide tip of the taper. The transverse misalignment of the polymer waveguide to the SOI was of $\sim$2.25 μm. The other end of the polymer waveguide lands in another recess which was fabricated in line to the first. Some polymer pads were defined around the coupon for locking the device in place as further processing on the sample could affect the adhesion [Fig. 5.12(a)].

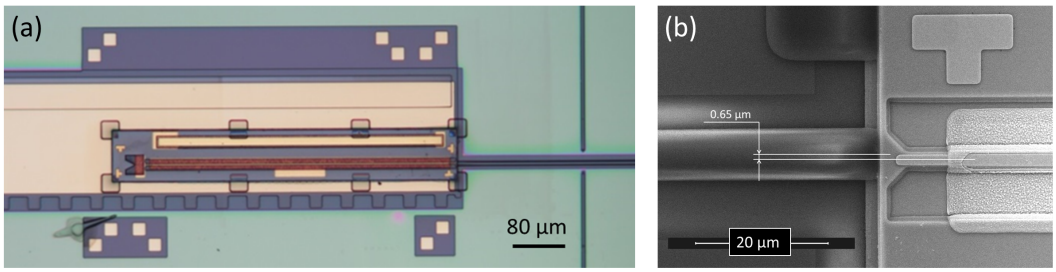


Figure 5.12: (a) Digital microscope image of the InP laser printed in a recess on the SOI and edge coupled to the polymer waveguide. (b) A scanning electron microscopy image of the waveguide aligned to the ridge of the laser shows <0.7 μm lateral misalignment. [11].

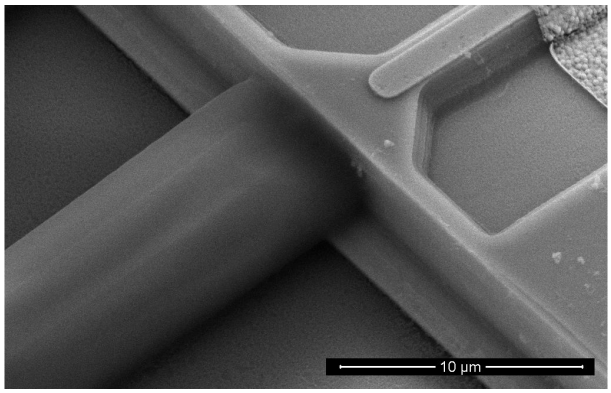


Figure 5.13: (a) SEM image of the polymer waveguide, detail of the full edge-coupling at the facet.

5.4 Characterization of the lasers integrated

Two devices were integrated into the recesses and were characterized electro-optically before and after μTP to the recesses. One of them was characterized also after being coupled to the polymer waveguide. The light-current characteristics of the devices show a threshold current of ~17 mA before and after μTP to the SOI that rises to ~23 mA after coupling the light to the SU8 waveguide due to reduced reflectivity of 15.5 % at the front mirror compared to emission in air. The light emitted by the laser operating at 20 °C has peak of emission at ~1340 nm wavelength. The light coupling to the polymer waveguide was detected with an infrared (IR) camera that showed the light coming out at the end of the 2 mm long polymer waveguide [Fig. 5.14].

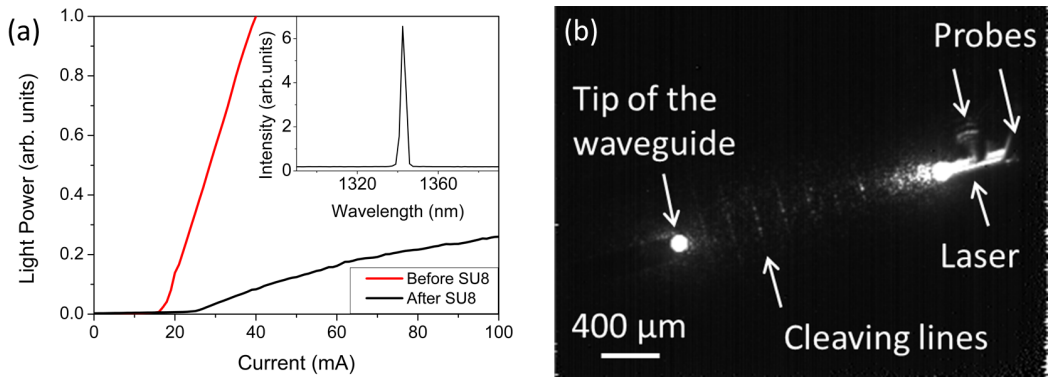


Figure 5.14: (a) L-I characteristics for the laser printed in the recess before and after coupling the light to the SU8 waveguide. The inset shows the emission wavelength of ~1340 nm with the laser operating at 20 °C before transfer. (b)IR camera imaging of the laser operating on the SOI and coupled to the 2 mm long polymer waveguide, the light comes out at the free end of the waveguide. Some transverse traces (cleaving lines) are due to recesses formed on the SOI to allow cleaving the chip. [11].

The efficiency of the light coupling has to be determined and improved through better alignment which can be achieved by using markers and pattern recognition at the transfer printer. The fabrication of a 3 μm wide and 1 μm thick SU8-polymer waveguide will optimize the mode matching to the laser output. The measurement of the thermal impedance will provide a characterization of the thermal performance of the proposed laser and of the thermal via applied. A model of the real laser set in COMSOL [4] provides a simulated thermal impedance of Z_t ~99 K/W while the same laser printed on top of the SOI would provide a higher thermal impedance of Z_t ~132 K/W. The simulations show that a thermal via that sinks the heat to the substrate with a shorter path from the heat source [Fig. 5.15] can reduce the

thermal impedance of the laser from 99 K/W to ∼49 K/W. Simulations also suggest that an increase in the thickness of the thermal via further reduces the thermal impedance of few K/W, especially when sinking the heat far from the active region of the device.

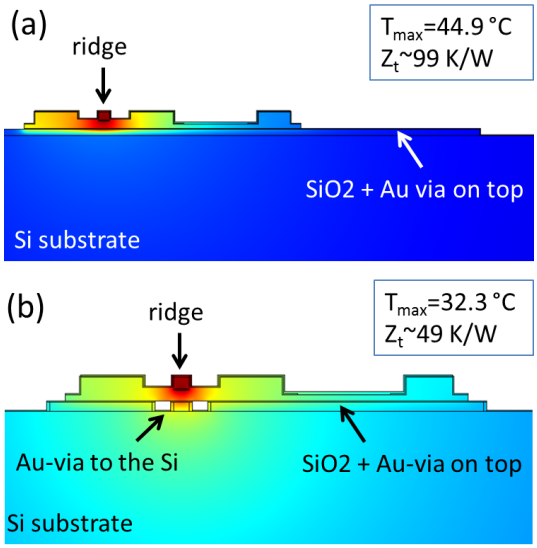


Figure 5.15: Diagrams of the thermal sink simulated with COMSOL [4], (a) for the O-band laser integrated in the recess on top of a metal thermal via and (b) for the same laser with a modified thermal via that shortens the heat path to the sink. The Z_t drops from 90 to 45 K/W.

5.5 Conclusion

The chapter reported the study of the edge-coupling from the design of the light coupling to the fabrication of the recesses in the SOI. The heterogeneous integration of a telecom InP laser to silicon photonics and the light coupling to polymer and SOI waveguides has been achieved. Optimization work is still required for the alignment of the different components involved in the integration and to control the dimensions of the polymer waveguide. The light coupling efficiency must be determined in order to assess the real performance of the edge-coupling, further maximization of the coupling efficiency should be required. Finally, the layout for the improvement of the thermal performance of the laser integrated simulated with COMSOL [4] must be verified experimentally, especially for lasers printed at the top of the SOI.

Bibliography

[1] *Micro-transfer printing for advanced scalable hybrid photonic integration*. Vol. 5. Valencia, Spain, 2018.

[2] *Top-Hit project*. 2019. URL: http://www.tophit-ssi.eu/ (visited on 02/11/2019).

[3] David Gomez et al. "Process capability and elastomer stamp lifetime in micro transfer printing". In: *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*. IEEE. 2016, pp. 680–687.

[4] COMSOL Inc. *COMSOL Multiphysics Reference Manual, version 5.3*. 2019. URL: https://www.comsol.com (visited on 07/21/2019).

[5] Photon Design. *FIMMWAVE, A powerful waveguide mode solver*. 2019. URL: https://www.photond.com/products/fimmwave.htm (visited on 07/21/2019).

[6] Ruggero Loi et al. "Transfer printing of AlGaInAs/InP etched facet lasers to Si substrates". In: *IEEE Photonics Journal* 8.6 (2016), pp. 1–10.

[7] LUMERICAL Inc. *FDTD*. 2019. URL: https://kb.lumerical.com/solvers_finite_difference_time_domain.html (visited on 07/21/2019).

[8] Ruggero Loi et al. "Thermal Analysis of InP Lasers Transfer Printed to Silicon Photonics Substrates". In: *Journal of Lightwave Technology* 36.24 (2018), pp. 5935–5941.

[9] Dow Chemical. *MICROPOSIT™ REMOVER 1165*. 2019. URL: http://microchem.com/products/images/uploads/Remover-1165-DataSheet-RH.pdf (visited on 07/10/2019).

[10] Joan Juvert et al. "Integration of etched facet, electrically pumped, C-band Fabry-Pérot lasers on a silicon photonic integrated circuit by transfer printing". In: *Optics express* 26.17 (2018), pp. 21443–21454.

[11] *Edge-coupling of O-band InP etched-facet lasers to polymer waveguides on SOI by micro-transfer-printing*. Ghent, Belgium, 2019.

[12] James O'Callaghan et al. "Comparison of InGaAs and InAlAs sacrificial layers for release of InP-based devices". In: *Optical Materials Express* 7.12 (2017), pp. 4408–4414.

Chapter 6

Conclusions

High performance InP ridge lasers with etched facets have been edge-coupled to silicon photonics by micro transfer printing as discussed in this work.

The edge-coupling of the laser waveguide to the SOI was achieved by integrating the devices inside recesses pre-fabricated on the SOI. The integration layout requires/exploits the dry-etched facet technology, the etched facets allow new geometries of the device with a small foot print and are suitable for the edge-coupling configuration.

The spatial alignment of the emitting facet to the SOI has been achieved by μTP and by depositing a calibrated thickness metal layer at the bottom of the recesses. The laser waveguide can be coupled directly to a mode matched polymer waveguide or MSC defined on top of the oxide layer of the SOI or it can be coupled to a MSC defined on the SOI layer. The light coupled to a polymer waveguide can be evanescent coupled to an SOI waveguide or to another device for polymer waveguide based PICs.

The key processing steps for the release of the devices from the donor substrate and the μTP to silicon photonics substrates with and without bonding or intermediate layers were developed in this work. The transfer printable InP lasers were completely pre-fabricated on the original InP wafer. Pre-fabricated devices are suitable for performance evaluation before and after integration, the fabrication of the III-V can be made in a separate environment reducing the risk of contamination when processing the silicon photonics in CMOS.

The laser epitaxial structures developed provide the optical mode to be independent of the hosting substrate making it suitable for edge light emission. The epitaxial structure developed include a sacrificial layer a the bottom to allow the release of coupons from the InP substrate.

Two release technologies based on a InGaAs and a InAlAs sacrificial layers and a iron chloride etching solution have been introduced for the release. The InAlAs sacrificial layer proved to be superior to InGaAs as it etches

faster and it is crystallographic independent. These features provide higher selectivity to InP and free orientation of the coupons on the InP wafer allowing the undercut and the adhesive-less integration of large area InP based devices to different substrates with high thermal sink and possibility of electrical contacting through the bottom of the laser. A 100 μm wide coupon can be released in less than 50 minutes with deviation from the flatness <5 nm over a 100 μm long linear profile and <2 nm nominal roughness. In comparison the undercut of coupons with an InGaAs sacrificial layer oriented along the major flat of the wafer result in surfaces with a significant dishing and roughness which requires use of adhesive layers.

Enhanced adhesion of adhesive-less printed lasers to the hosting substrate can be achieved by an annealing at 300 °C and few mTorr pressure inside the PECVD vacuum chamber. Higher adhesion to the substrate provides better thermal sinking and in turn lower thermal impedance. Adhesive-less print reduces the complexity of the integration process and use of adhesive layers as, for example, BCB, usually require the engineering of thermal vias to overcome its low thermal conductivity of 0.0029 $Wcm^{-1}{}^{\circ}C^{-1}$ at 25 °C. A few nanometers thin BCB layer can be achieved by treating the printed device and the substrate with vapour and liquid acetone. The technique gives high adhesion of the coupon to the substrate and thermal impedance comparable to that of adhesive-less printed devices. Use of adhesive layers inside recesses must be achieved by spray coating or evaporation to avoid unexpected thickness of the layer at the bottom of the recess, as shown for a HMDS adhesive layer, these techniques allow tuning the thickness of the adhesive layer more accurately.

The validation of the integration strategy was made through electrical, spectral, spatial and thermal characterization of the devices. Lasers printed on Si and Au-coated-Si substrates are shown to operate up to 110 °C in continuous-wave. The threshold current can be improved by engineering the reflectivity at the facets and the electrical ohmic contacts quality. The optimized dry-etch and passivation process developed for the facets and the thermal annealing of the contact provided a threshold current density of 1/3 to that of the original devices of I_{th} ~200 $A{\cdot}cm^{-2}$ per quantum well (on the 6 multi-quantum-well laser structures used). The spectral shift characterization showed that heat management represent a significant challenge for the printed lasers depending on the thermal conductivity and the geometry of the hosting platform.

This work shows that μTP is a potentially disruptive technique for wafer-scale integration of high-performance InP lasers onto Si and other substrates. The stamps can be designed to transfer hundreds to thousands of discrete coupons in a single pick-up and print operation. The μTP technique is not sensitive to the wafer-size mismatch problems or the need for large flat regions as required for wafer bonding. In addition, multiple prints can be employed to transfer many different device types leading to versatile integration strategies. This technology can be applied to datacom, sensing and medical devices.

6.1 Future development

This work shows a roadmap for the integration of InP lasers to SOI and edge-coupled to polymer and SOI waveguides. In any case, still much work is required for demonstrating photonic integrated circuit with devices connected through polymer or hybrid polymer-SOI waveguide. More work is required to characterize and optimize the light coupling efficiency and it would be advisable to work on the following points for future development:

- The integration of more devices through μTP by using alignment markers and pattern recognition in order to achieve <1 μm lateral alignment and demonstrate high yield of the process at scale.
- The transfer printing of devices with ledge-less encapsulation will allow juxtaposing the emitting facet to the recess sidewall with <0.1 μm longitudinal misalignment improving the light coupling efficiency further.
- For the laser edge-coupled to the waveguide, a study of the thermal performance must assess the actual thermal impedance of the device.
- A method for measuring the slope efficiency of the laser printed inside recesses or far from the edge of the PIC must be developed for a comprehensive electro-optical characterization and optimization of the lasers. Out-coupling gratings and polymer waveguide cleaved at the edge of the PIC could be an option.
- The test of a different thermal via layout able to sink the heat to the substrate from close to the active region (see section 5.3) should be evaluated for enhanced thermal performance.

- Calibration tests for achieving polymer waveguides of the desired cross section must be carried out in order to obtain waveguides comparable to those simulated with FIMMWAVE [1].
- An etch back process for calibrating the thickness of the polymer layer should be developed.
- The light evanescent-coupling from the polymer waveguide to the inverted taper of the SOI waveguide must be simulated and fabricated and evaluated experimentally with the aim to dimension the different components and achieve the highest light coupling efficiency.
- An alternative layout for InP etched facet ridge lasers edge coupled to SOI could be achieved by moving the front mirror from the emitting facet to a grating defined on the SOI. The reflectivity at the facet could be lowered by positioning it at an angle and by coating it with an anti-reflective (AR) passivation layer, in this way most of the light can be injected into the MSC and then into the SOI. The grating-mirror will offer accurate tuning of the reflectivity and it will filter the emission wavelength.
- An alternative approach to LSS lasers for enhancing the tolerances of the alignments in the edge-coupling would be to embed a MSC on the III-V die to enlarge the emitted mode. Then the alignment of the laser mode to a mode matched MSC embedded into the SOI would provide more relaxed alignments. This would obviously increase the complexity of fabrication on the III-V, but still it would be interesting to explore this possibility.

Bibliography

[1] Photon Design. *FIMMWAVE, A powerful waveguide mode solver*. 2019. URL: https://www.photond.com/products/fimmwave.htm (visited on 07/21/2019).

Chapter 7

List of publications

The work made during this thesis produced a number of publications in internationally renowned scientific journals and conferences. A conspicuous number of contribution to other works testifies the impact of this research in the area of integrated InP devices to silicon photonics and in the area of micro transfer printing. The publications are listed in a chronological order. Poster and talks prepared for internal conferences at Tyndall National Institute or at IPIC centre are not reported in the list. Talks hold for outreach and abstracts submitted to competitions have not been reported in the list.

- Journal papers:
  - Loi, R., S. Iadanza, B. Roycroft, J. O'Callaghan, L. Liu, K. Thomas, A. Gocalinska, E. Pelucchi, A. Farrell, S. Kelleher, R.F. Gul, A. J. Trindade, D. Gomez, L. O'Faolain, and B. Corbett. "Edge-coupling of O-band InP etched-facet lasers to polymer waveguides on SOI by micro-transfer-printing." Journal of Quantum Electronics, submitted 21 June 2019.
  - Liu, Lei, Ruggero Loi, Brendan Roycroft, James O'Callaghan, Antonio Jose Trindade, Steven Kelleher, Agnieszka Gocalinska et al. "Low-power-consumption optical interconnect on silicon by transfer-printing for used in opto-isolators." Journal of Physics D: Applied Physics 52, no. 6 (2018): 064001.
  - Loi, Ruggero, James O'Callaghan, Brendan Roycroft, Zhiheng Quan, Kevin Thomas, Agnieszka Gocalinska, Emanuele Pelucchi, Antonio Jose Trindade, Christopher Anthony Bower, and Brian Corbett. "Thermal Analysis of InP Lasers Transfer Printed to Silicon Photonics Substrates." Journal of Lightwave Technology 36, no. 24 (2018): 5935-5941.

- Corbett, Brian, Ruggero Loi, James O'Callaghan, and Gunther Roelkens. "Transfer Printing for Silicon Photonics." In Semiconductors and Semimetals, pp. 43-70. Elsevier, 2018.
- O'Callaghan, James, Ruggero Loi, Enrica E. Mura, Brendan Roycroft, Antonio Jose Trindade, K. Thomas, A. Gocalinska et al. "Comparison of InGaAs and InAlAs sacrificial layers for release of InP-based devices." Optical Materials Express 7, no. 12 (2017): 4408-4414.
- Zhang, Jing, Andreas De Groote, Amin Abbasi, Ruggero Loi, James O'Callaghan, Brian Corbett, Antonio Jose Trindade, Christopher A. Bower, and Gunther Roelkens. "Silicon photonics fiber-to-the-home transceiver array based on transfer-printing-based integration of III-V photodetectors." Optics express 25, no. 13 (2017): 14290-14299.
- Corbett, Brian, Ruggero Loi, Weidong Zhou, Dong Liu, and Zhenqiang Ma. "Transfer print techniques for heterogeneous integration of photonic components." Progress in Quantum Electronics 52 (2017): 1-17.
- Loi, Ruggero, James O'Callaghan, Brendan Roycroft, Cedric Robert, Alin Fecioru, Antonio Jose Trindade, Agnieszka Gocalinska, Emanuele Pelucchi, Christopher A. Bower, and Brian Corbett. "Transfer printing of AlGaInAs/InP etched facet lasers to Si substrates." IEEE Photonics Journal 8, no. 6 (2016): 1-10.

- Conferences:
  - Loi, R., S. Iadanza, B. Roycroft, J. O'Callaghan, L. Liu, K. Thomas, A. Gocalinska, E. Pelucchi, A. Farrell, S. Kelleher, R.F. Gul, A. J. Trindade, C. A. Bower, L. O'Faolain, and B. Corbett. "Edge-coupling of O-band InP etched-facet lasers to polymer waveguides on SOI by micro-transfer-printing." In European Conference on Integrated Optics (ECIO'2019), 2019.
  - Corbett, B., R. Loi, J. O'Callaghan, L. Liu, K. Thomas, A. Gocalinska, E. Pelucchi et al. "Transfer-printing for heterogeneous integration." In Optical Fiber Communication Conference, pp. M2D-1. Optical Society of America, 2019.
  - Loi, R., J. O'Callaghan, B. Roycroft, K. Thomas, E. Mura, A. Gocalinska, E. Pelucchi, A. Fecioru, A. J. Trindade, C. A. Bower, and

B. Corbett. "Transfer Printable InP lasers for Si photonics." In Photonics Ireland, 2018.

- Roelkens, Gunther, Jing Zhang, Andreas De Groote, Joan Juvert, Nan Ye, Sulakshna Kumari, Jeroen Goyvaerts et al. "Transfer printing for silicon photonics transceivers and interposers." In 2018 IEEE Optical Interconnects Conference (OI), pp. 13-14. IEEE, 2018.
- Loi, R., J. O'Callaghan, B. Roycroft, Z.Quan, K. Thomas, A. Gocalinska, E. Pelucchi, A. J. Trindade, C. A. Bower, and B. Corbett. "InP lasers for Silicon photonics by micro transfer printing." In Epixfab 2018, poster, 2018.
- Mura, Enrica E., A. Gocalinska, R. Loi, G. Juska, S. T. Moroni, B. Corbett, and E. Pelucchi. "MOVPE-Grown Metamorphic Lasers at 1.3 μm: Solving Critical Growth, Material and Design Issues." In ICMOVPE-XIX, 2018.
- Loi, R., B. Roycroft, J. O'Callaghan, J. Justice, A. Gocalinska, E. Pelucchi, A. J. Trindade, C. A. Bower, Gunther Roelkens, and B. Corbett. "Micro-transfer printing for advanced scalable hybrid photonic integration." In European Conference on Integrated Optics (ECIO'2018), pp. 98-100. 2018.
- Liu, Lei, Ruggero Loi, Brendan Roycroft, James O'Callaghan, John Justice, Antonio Jose Trindade, Steven Kelleher et al. "On-chip optical interconnect on silicon by transfer printing." In 2018 Conference on Lasers and Electro-Optics (CLEO), pp. 1-2. IEEE, 2018.
- Corbett, B., R. Loi, D. Quinn, J. O'Callaghan, and N. Liu. "Transferred III-V Materials-Novel Devices and Integration." In Integrated Photonics Research, Silicon and Nanophotonics, pp. ITu2A-4. Optical Society of America, 2017.
- Loi, R., J. O'Callaghan, B. Roycroft, A. Gocalinska, E.E. Mura, E. Pelucchi, A. J. Trindade, A. Fecioru, C. A. Bower, and B. Corbett. "Heterogeneous integration of telecom lasers to Si substrates by micro transfer printing." In Smart Systems Integration (SSI'2017), 2017.
- Quinn, D., J. O'Callaghan, B. Roycroft, R. Loi, J. Justice, A. J. Trindade, A. Gocalinska, E. Pelucchi, C. A. Bower, and B. Corbett. "Transfer printing of photovoltaic power converter." In Smart Systems Integration (SSI'2017), 2017.

- Zhang, Jing, Amin Abbasi, Andreas De Groote, Ruggero Loi, James O'Callaghan, Brian Corbett, Antonio Jose Trindade, Christopher A Bower, and Gunther Roelkens. "Silicon photonic transceiver array based on the transfer printing of III-V O-band photodetectors." In European Conference on Integrated Optics (ECIO'2017), pp. 1-2. 2017.
- Loi, R., J. O'Callaghan, C. Robert, A. Fecioru, A. J. Trindade, C. A. Bower, and B. Corbett. "Technologies for Transfer Printing of InP Based Etched Facet Lasers." In MRS Spring Meeting & exhibit (MRS 2016), 2016.
- Loi, R., J. O'Callaghan, C. Robert, A. Fecioru, A. J. Trindade, C. A. Bower, and B. Corbett. "Transfer Printing of InP Etch Facet Lasers." In Photonics Ireland, 2015.

Appendix A

Epitaxial structures for transfer printable lasers

In this appendix is reported the layer structure of the main epitaxial wafers used for the fabrication of the lasers involved in this work. The releasable lasers were initially fabricated on the A1779 epitaxial structure [Tab. A.1], emitting at 1550 nm wavelength with polarization TE. A1779 was obtained by adding a 1 μm thick InGaAs sacrificial layer to a previously developed laser epitaxial structure named A1741. Subsequently the InGaAs sacrificial layer was exchanged with a 500 μm thick InAlAs sacrificial layer for achieving isotropic etch in $FeCl_3$:H_2O (1:2), the resulting structure was the A2541 [Tab A.2]. Another InP based laser structure emitting at 1310 nm wavelength with polarization TM, named A2940 [Tab. A.3], developed by L.Liu et Al., was employed in the demonstration of the laser edge coupled to a polymer waveguide on the SOI (see chapter 5). The A2940 epitaxial structure was originally grown for edge emitting LED to reduce the emission from the top surface by making the device work in TM mode. The TM emission was achieved by increasing the In percentage in the quantum well region which shifted the emission wavelength to $\sim$1340 nm.

A1779

Layer	Material	Thickness nm	Doping level cm^{-3}	Dopant	Comment
26	InGaAs	40	>1x10^{19}	Zn	-
25	InGaAs	80	>1x10^{19}	Zn	-
24	InP	1500	∼1x10^{18}	Zn	-
23	InGaAsP	6	∼5x10^{17}	Zn	Etch stop layer
22	InP	40	∼1x10^{17}	Zn	
21	CIL	<5			Minimal thickness
20	$(Al_{.9}Ga_{.1})_{.47}In_{.53}As$	40			
19	$(Al_{.7}Ga_{.3})_{.47}In_{.53}As$	75			
8 x 6	$(Al_{.45}Ga_{.65})_{.51}In_{.49}As$	10		As A1734	Tensile strained barrier ∼-0.3 %.
7 x 6	$(Al_{.25}Ga_{.75})_{.3}In_{.7}As$	6		As A1734	Compressive strained quantum well ∼1.1 %.
6	$(Al_{.45}Ga_{.65})_{.51}In_{.49}As$	10			Tensile strained barrier ∼-0.3 %.
5	$(Al_{.7}Ga_{.3})_{.47}In_{.53}As$	75			
4	$(Al_{.9}Ga_{.1})_{.47}In_{.53}As$	40	1x10^{18}	Si	
3	InP	1500	1x10^{18}	Si	Lower cladding
2	InGaAs	1000	∼1x10^{18}	Si	Sacrificial layer
1	InP	100	1x10^{18}	Si	buffer
	InP substrate		N-type		3 wafers

Table A.1: A1779 epitaxial structure, provides laser emission at 1550 nm with TE polarization. This structure was derived from the A1741 adding the 1 μm thick InGaAs sacrificial layer between the InP lower cladding and the substrate.

A2541

Layer	Material	Thickness nm	Doping level cm^{-3}	Dopant	Comment
26	InGaAs	40	>1x10^{19}	Zn	Do not add C
25	InGaAs	80	>1x10^{19}	Zn	Do not add C
	InGaAsP	20	2x10^{18}	p (Zn)	Interface layer
24	InP	1500	∼1x10^{18}	Zn	
23	InGaAsP	6	∼5x10^{17}	Zn	Etch stop layer
22	InP	40	∼1x10^{17}	Zn	
21	CIL	<5			Minimal thickness
20	$(Al_{.9}Ga_{.1})_{.47}In_{.53}As$	40			
19	$(Al_{.7}Ga_{.3})_{.47}In_{.53}As$	75			
8 x 6	$(Al_{.45}Ga_{.65})_{.51}In_{.49}As$	10		As A1734	Tensile strained barrier ∼-0.3 %.
7 x 6	$(Al_{.25}Ga_{.75})_{.3}In_{.7}As$	6		As A1734	Compressive strained quantum well ∼1.1 %.
6	$(Al_{.45}Ga_{.65})_{.51}In_{.49}As$	10			Tensile strained barrier ∼-0.3 %.
5	$(Al_{.7}Ga_{.3})_{.47}In_{.53}As$	75			
4	$(Al_{.9}Ga_{.1})_{.47}In_{.53}As$	40	1x10^{18}	Si	
3	InP	1500	1x10^{18}	Si	Lower cladding
	InGaAs (CIL)	10	1x10^{18}		Interface layer.
2	AlInAs	500	∼1x10^{18}	Si	Sacrificial layer
1	InP	100	1x10^{18}	Si	buffer
	InP substrate		N-type		3 wafers

Table A.2: A2541 epitaxial structure, provides laser emission at 1550 nm with TE polarization.

A2940

Layer	Material	Thickness nm	Doping level cm^{-3}	Dopant	Comment
26	InGaAs	120	>1x10^{19}	Zn	Dont add C
25	InGaAsP	20	2x10^{18}	p (Zn)	
24	InP	1150	∼1x10^{18}	Zn	
23	InP	400	∼5x10^{17}	Zn	Etch stop layer
22	InP	100	∼1x10^{17}	Zn	
21	InGaAS (CIL)	<5			Minimal thickness
20	$Al_{.352}Ga_{.118}In_{.53}As$	100			Lattice matched waveguide
9 x 6	$Al_{.3}Ga_{.08}In_{.62}As$	20			Compressive strained barrier ∼+0.6 %.
8 x 6	$Al_{.0325}Ga_{.6175}In_{.35}As$	10			Tensile strained quantum well ∼-1.35 %.
7	$Al_{.3}Ga_{.08}In_{.62}As$	20			Compressive strained barrier ∼+0.6 %.
6	$Al_{.352}Ga_{.118}In_{.53}As$	100			Lattice matched waveguide
5	InP	500	5x10^{17}	Si	Lower cladding
4	InP	1150	1x10^{18}	Si	Lower cladding
3	InGaAs	100	1x10^{18}		Interface layer.
2	AlInAs	500	∼1x10^{18}	Si	Sacrificial layer
1	InP	300	1x10^{18}	Si	buffer
	InP substrate		N-type		3 wafers

Table A.3: A2940 epitaxial structure, provides laser emission at 1310 nm with TM polarization.

Appendix B

Etched facets ridge lasers for μTP to PICs

In this appendix is reported a summary of the main process used for fabricating transfer printable InP lasers. The process is the result of the optimization achieved along different runs of fabrication and after the design of other processes. The main steps of the process are grouped by level of lithography. The final step of the process is the undercut of the devices from the native substrate. After this step the devices will be ready for μTP. A process-flow chart is reported at the end of the appendix.

PROCESS DATA

Wafers: A2541, A1779, A2940, A2651
Date: May 2018
Designer: Ruggero Loi

L1 P-METAL + ALIGNMENT MARKERS

The first level of lithography defines 1.5 μm wide and 495 μm long p-contacts and the alignment markers for the following levels of lithography by a metal evaporation.

- Create a lift off resist structure with a 500 nm thick S1805 resist layer and a 300 nm thick LOR-3A layer.
- Lithography L1, expose with a dose of 50 mJ/cm^2 dose at 405 nm wavelength.
  - Higher accuracy in defining the thin 1.5 μm wide p-contact could be achieved by deep UV lithography or by e-beam lithography.

- Flat evaporation of a Ti:Au (10:110) nm metal layer.

L2 RIDGE TRENCHES

The second lithography defines two parallel trenches that create the ridge structure for the lateral confinement of the light.

- PECVD of 300 nm thick SiO_2 hard mask.
- Spin a 1.3 μm thick resist layer of S1813 on the sample.
- Lithography L2, expose with a dose of 140 mJ/cm^2 dose at 405 nm wavelength.
- SiO_2 hard mask dry-etch (complete) with CF_4:CHF_3 chemistry.
- Dry-etch ∼1500 nm deep ridge trenches with $Cl_2/CH_4/H_2$ chemistry above the active region.
  - Finish by wet-etch of p-InP to the CIL layer in H_3PO_4:HCl (4:1).
- *Optional: SiO_2 mask thinning by dry-etch with CF_4:CHF_3 chemistry.

L3 RECESSES TO ACCESS THE N-InP LAYER

The third lithography serve for creating a recess that accesses the n-InP layer. The recess is usually one (can be two) and is arranged beside the ridge trenches.

- PECVD of 400 nm thick SiO_2 hard mask.
- Spin a 1.3 μm thick resist layer of S1813 on the sample.
- Lithography L3, expose with a dose of 140 mJ/cm^2 dose at 405 nm wavelength.
- SiO_2 hard mask dry-etch (complete) with CF_4:CHF_3 chemistry.
- Dry-etch ∼2500 nm deep trenches with $Cl_2/CH_4/H_2$ chemistry.
- SiO_2 mask thinning by dry-etch with CF_4:CHF_3 chemistry.

L4 N-METAL EVAPORATION

This level of lithography serves for the N-metal definition at the bottom of the recess created to access the N-InP layer. This approach allows have both the contacts at the top of the device.

- Create a lift off resist structure with a 1.3 μm thick S1813 resist layer and a 1 μm thick LOR-10A layer.
- Lithography L4, expose with a dose of 140 mJ/cm^2 dose at 405 nm wavelength.
- SiO_2 hard mask dry-etch (complete) with CF_4:CHF_3 chemistry.
- Flat evaporation of a Au:Ge:Au:Ni:Au (14:14:14:11:200) nm. metal layer.
- PECVD of a 400 nm thick SiN hard mask for protection of the metal during the alloy.
- Alloying n- and p-metal contact at the furnace or RTA at 390 °C.
- SiN mask thinning with CF_4 based chemistry.

L5 FACETS + COUPON PROFILES

The fifth level of lithography is used to define the coupon profile and the facets of the Fabry-Perot resonator.

- Sputter of a 500 nm thick SiO_2 hard mask.
- Spin a 1.3 μm thick resist layer of AZ5214 on the sample (negative slope at the sidewalls).
- Lithography L5, expose with a dose of 140 mJ/cm^2 dose at 405 nm wavelength.
- SiO_2 hard mask dry-etch (complete) with CF_4:CHF_3 chemistry.
- Dry-etch $\sim$3000 nm deep or >500 nm into the n-InP layer with $Cl_2/CH_4/H_2$ chemistry.
- SiO_2 mask thinning by dry-etch with CF_4:CHF_3 chemistry.
- SEM inspection of facet quality (roughness straightness and flatness.

L6 ENCAPSULATION OF THE COUPONS

The sixth lithography defines the encapsulation profile around the coupon on a SiO_2+SiN hard mask.

- Sputter of a 150 nm thick SiO_2 hard mask (it will be *sim* 100 nm at the facet sidewalls) for neutral-reflection coating.
- PECVD of a 450 nm thick SiN hard mask.
- Spin a 2.8 μm thick resist layer of S1828 on the sample.
- Lithography L6, expose with a dose of 400 mJ/cm^2 dose at 405 nm wavelength.
- SiN and SiO_2 hard mask dry-etch (complete) with CF_4:CHF_3 chemistry.
- Wet-etch with H_3PO_4:HCl (4:1) the n-InP layer 500 nm to reach the AlInAs release layer.

L7 GRATING ON THE AlInAs sacrificial layer

The seventh level of lithography allows defining a grating structure on the sacrificial layer, this prevent the anchors to cover the sidewalls of the sacrificial layer and give the etchant multiple starting points around the coupon.

- PECVD of a 300 nm thick SiN hard mask.
- Spin a 2.8 μm thick resist layer of S1828 on the sample.
- Lithography L7, expose with a dose of 400 mJ/cm^2 dose at 405 nm wavelength.
- SiN hard mask dry-etch (complete) with CF_4 based chemistry.
- Dry-etch to the substrate (+$\sim$500 nm over-etch into the InP) with $Cl_2/CH_4/H_2$ chemistry.

L8 OPEN DIELECTRIC ON THE P- AND N-CONTACTS

The eighth lithography level create some openings on the hard mask to access the p- and the n- contacts.

- Spin a 2.8 μm thick resist layer of S1828 on the sample.

- Lithography L8, expose with a dose of 400 mJ/cm^2 dose at 405 nm wavelength.
- SiN hard mask dry-etch (complete) with CF_4:CHF_3 based chemistry.

L9 METAL PROBING PADS and HR MIRRORS

The ninth lithography level creates a lift-off structure for the metal probing pads and the highly reflective coating to be deposited at the rear facet of the laser.

- Create a lift off resist structure with a 2.8 μm thick S1828 resist layer and a 1 μm thick LOR-10A layer.
- Lithography L9, expose with a dose of 140 mJ/cm^2 dose at 405 nm wavelength.
- 360 metal evaporation of a Ti:Au (5:200) nm metal layer.Ti layers thicker than 5 nm must be avoided as they absorb the light.
- SiN mask thinning at the isotropic dry-etcher (Asher) with CF_4 based chemistry.
- SEM inspection of the devices (in particular the facets).
- **Electro-optical (+ thermal) characterization of the devices prior to μTP.**

L10 ANCHOR SYSTEM DEFINITION

The tenth level of lithography is the last of the process and defines the polymer anchor system as an arrangement of tethers around the coupons, to hold them stable to the substrate during the undercut (see next step).

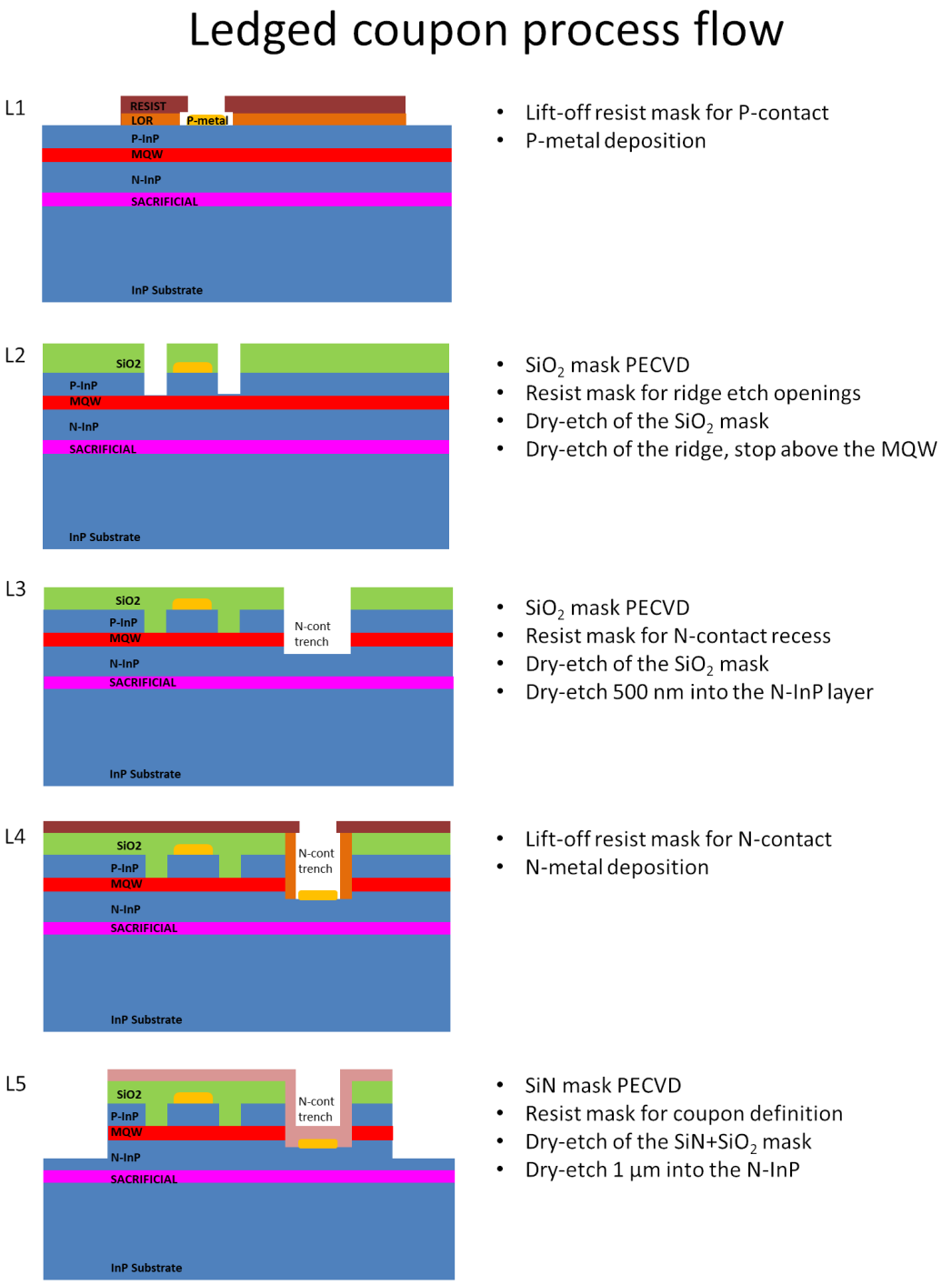
- Spin a 2.8 μm thick resist layer of S1828 on the sample.
- Lithography L10, expose with a dose of 400 mJ/cm^2 dose at 405 nm wavelength.
  - *Optional hard-bake (5 minutes at 125 °C) for anchors easier to break.

WET-ETCH OF THE SACRIFICIAL LAYER (AlInAs)

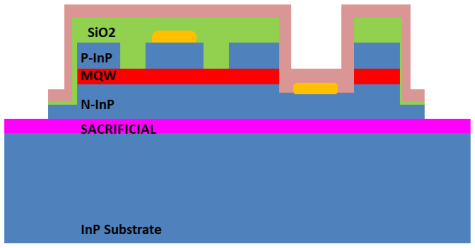
The goal of this step is to undercut the devices in order to release them from the original substrate. The released device will be ready for μTP.

- slice a piece of the chip for the undercut testing
- Etch in Iron chloride acid solution, $FeCl_3$:H_2O (1:2), at 1 °C.
- Rinse multiple times and very gently in DI water by using a pipette until the acid is completely removed.
- Dry the sample gently by air-gun.
  - If tethers break during rinse, dry the sample in a hotplate at 60 °C, 1min.

Figure B.1: Process flow chart according to the lithography levels. L1 defines the p-metal; L2 defines the ridge; L3 defines the recess to access the N-InP layer; L4 defines the N-contact; L5 defines the facets together with the coupons profile. L6 defines the encapsulation ledge around the coupon; L7 is for the grating structure; L8 opens the passivation layers to access the P- and N-contacts; L9 defines the metal probing pads; L10 defines the anchor system.

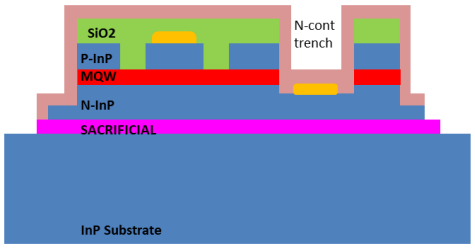


L6



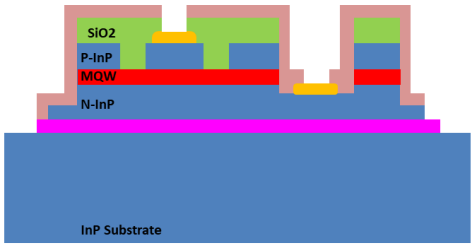
- SiO_2 mask PECVD, facet passivation
- SiN mask PECVD, coupon encapsulation
- Resist mask for encapsulation
- Dry-etch of the SiN+SiO_2 mask
- Wet-etch the N-InP to the sacrificial

L7



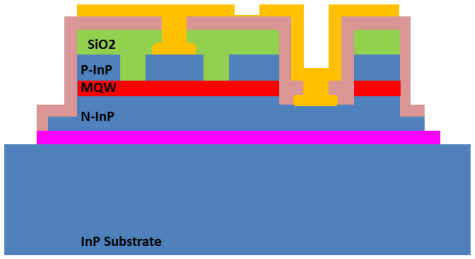
- SiN mask PECVD, grating
- Resist mask for the grating
- Dry-etch of the SiN mask
- Dry-etch 500 nm into the InP substrate

L8



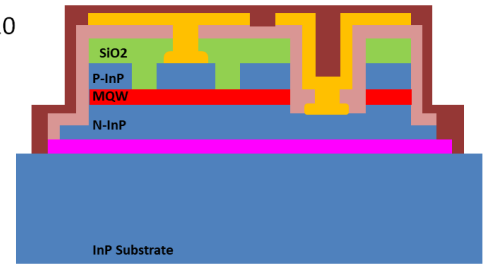
- Resist mask to open P- and N-contacts
- Dry-etch the SiN+SiO_2 mask

L9



- Lift-off resist mask for probing pads
- Pad-metal and HR-mirror deposition

L10



- Resist mask for the anchors

Appendix C

Ledge-less etched facets ridge lasers for μTP to PIC

In this appendix is reported the process for the fabrication of the transfer printable InP laser including the removal of the encapsulation ledge and the grating structure around the coupon. This process represents the best evolution of the fabrication process to achieve transfer printable InP lasers, it has 2 lithographic steps less than the standard process in appendix B and allows the complete edge coupling of the facet of the laser to the sidewall of recesses on the SOI. This process was based on the same principles developed by J.O'Callaghan for processing similar edge-coupled devices without encapsulation ledge.

PROCESS DATA

Wafers: A2541, A1779, A2940, A2651
Date: May 2018
Designer: Ruggero Loi

L1 P-METAL + ALIGNMENT MARKERS

The first level of lithography defines 1.5 μm wide and 495 μm long p-contacts and the alignment markers for the following levels of lithography by a metal evaporation.

- Create a lift off resist structure with a 500 nm thick S1805 resist layer and a 300 nm thick LOR-3A layer.
- Lithography L1, expose with a dose of 50 mJ/cm^2 dose at 405 nm wavelength.

  - Higher accuracy in defining the thin 1.5 μm wide p-contact could be achieved by deep UV lithography or by e-beam lithography.

- Flat evaporation of a 10 nm Ti + 110 nm Au metal layer.

L2 RIDGE TRENCHES

The second lithography defines two parallel trenches that create the ridge structure for the lateral confinement of the light.

- PECVD of 300 nm thick SiO_2 hard mask.
- Spin a 1.3 μm thick resist layer of S1813 on the sample.
- Lithography L2, expose with a dose of 140 mJ/cm^2 dose at 405 nm wavelength.
- SiO_2 hard mask dry-etch (complete) with CF_4:CHF_3 chemistry.
- Dry-etch ~1500 nm deep ridge trenches with $Cl_2/CH_4/H_2$ chemistry above the active region.
  - Finish by wet-etch of p-InP to the CIL layer in H_3PO_4:HCl (4:1).
- *Optional: SiO_2 mask thinning by dry-etch with CF_4:CHF_3 chemistry.

L3 RECESSES TO ACCESS THE N-InP LAYER

The third lithography allows creating a recess to accesses the n-InP layer. The recess is usually one (can be two in wide coupons for symmetrical current injection) and is arranged beside the ridge trenches.

- PECVD of 400 nm thick SiO_2 hard mask.
- Spin a 1.3 μm thick resist layer of S1813 on the sample.
- Lithography L3, expose with a dose of 140 mJ/cm^2 dose at 405 nm wavelength.
- SiO_2 hard mask dry-etch (complete) with CF_4:CHF_3 chemistry.
- Dry-etch ~2500 nm deep trenches with $Cl_2/CH_4/H_2$ chemistry.
- SiO_2 mask thinning by dry-etch with CF_4:CHF_3 chemistry.

L4 N-METAL EVAPORATION

This level of lithography serves for the N-metal definition at the bottom of the recess created to access the N-InP layer. This approach allows have both the contacts at the top of the device.

- Create a lift off resist structure with a 1.3 μm thick S1813 resist layer and a 1 μm thick LOR-10A layer.
- Lithography L4, expose with a dose of 140 mJ/cm^2 dose at 405 nm wavelength.
- SiO_2 hard mask dry-etch (complete) with CF_4:CHF_3 chemistry.
- Flat evaporation of a Au:Ge:Au:Ni:Au (14:14:14:11:200) nm. metal layer.
- PECVD of a 400 nm thick SiN hard mask for protection of the metal during the alloy.
- Alloying n- and p-metal contact at the furnace or RTA at 390 laser source
- SiN mask thinning with CF_4 based chemistry.

L5 FACETS + COUPON PROFILES + ENCAPSULATION

The fifth level of lithography is used to define the coupon profile and the facets of the Fabry-Perot resonator.

- Sputter of a 500 nm thick SiO_2 hard mask.
- Spin a 1.3 μm thick resist layer of AZ5214 on the sample (negative slope at the sidewalls).
- Lithography L5, expose with a dose of 140 mJ/cm^2 dose at 405 nm wavelength.
- SiO_2 hard mask dry-etch (complete) with CF_4:CHF_3 chemistry.
- Dry-etch $\sim$3000 nm deep or >1 μm into the n-InP layer with $Cl_2/CH_4/H_2$ chemistry.
- SiO_2 mask thinning by dry-etch with CF_4:CHF_3 chemistry.
- SEM inspection of facet quality (roughness straightness and flatness.

- Encapsulation of the coupons:
  - Sputter of a 150 nm thick SiO_2 hard mask (it will be *sim* 100 nm at the facet sidewalls) for neutral-reflection coating.
  - PECVD of a 450 nm thick SiN hard mask.
  - SiN and SiO_2 hard mask dry-etch (by using end-point detection) with CF_4:CHF_3 chemistry. The passivation layer will still be present at the top and at the sidewall of the coupon keeping it encapsulated.
- Wet-etch with H_3PO_4:HCl (4:1) the n-InP layer 500 nm to reach the AlInAs release layer.
- Dry-etch to the substrate (+∼500 nm over-etch into the InP) with $Cl_2/CH_4/H_2$ chemistry.

L6 OPEN DIELECTRIC ON THE P- AND N-CONTACTS

The sixth lithography level use the eighth level of the mask to create some openings on the hard mask to access the p- and the n- contacts.

- Spin a 2.8 μm thick resist layer of S1828 on the sample.
- Lithography L8, expose with a dose of 400 mJ/cm^2 dose at 405 nm wavelength.
- SiN hard mask dry-etch (complete) with CF_4:CHF_3 based chemistry.

L7 METAL PROBING PADS and HR MIRRORS

The seventh lithography level uses the ninth level of the mask for creating a lift-off structure for the metal probing pads and the highly reflective coating to be deposited at the rear facet of the laser.

- Important: SiN mask thinning at the isotropic dry-etcher (Asher) with CF_4 based chemistry. This step allows deposit the metal HR coating directly on the SiO_2 layer passivating the facets.
- Create a lift off resist structure with a 2.8 μm thick S1828 resist layer and a 1 μm thick LOR-10A layer.
- Lithography L9, expose with a dose of 140 mJ/cm^2 dose at 405 nm wavelength.

- 360 metal evaporation of a Ti:Au (5:200) nm metal layer. Ti layers thicker than 5 nm must be avoided as they absorb the light.
- SEM inspection of the devices (in particular the facets).
- **Electro-optical (+ thermal) characterization of the devices prior to μTP.**

L8 ANCHOR SYSTEM DEFINITION

The eighth level of lithography is based on a further level of lithography that allows define the polymer anchor system with a different arrangement of tethers around the coupons, in particular the tethers are connected to the top of the coupon and the sidewall of the coupon remain exposed to the etchant. If the encapsulation is not good at the corners there could be some erosion issue which could ruin all the preparatory work.

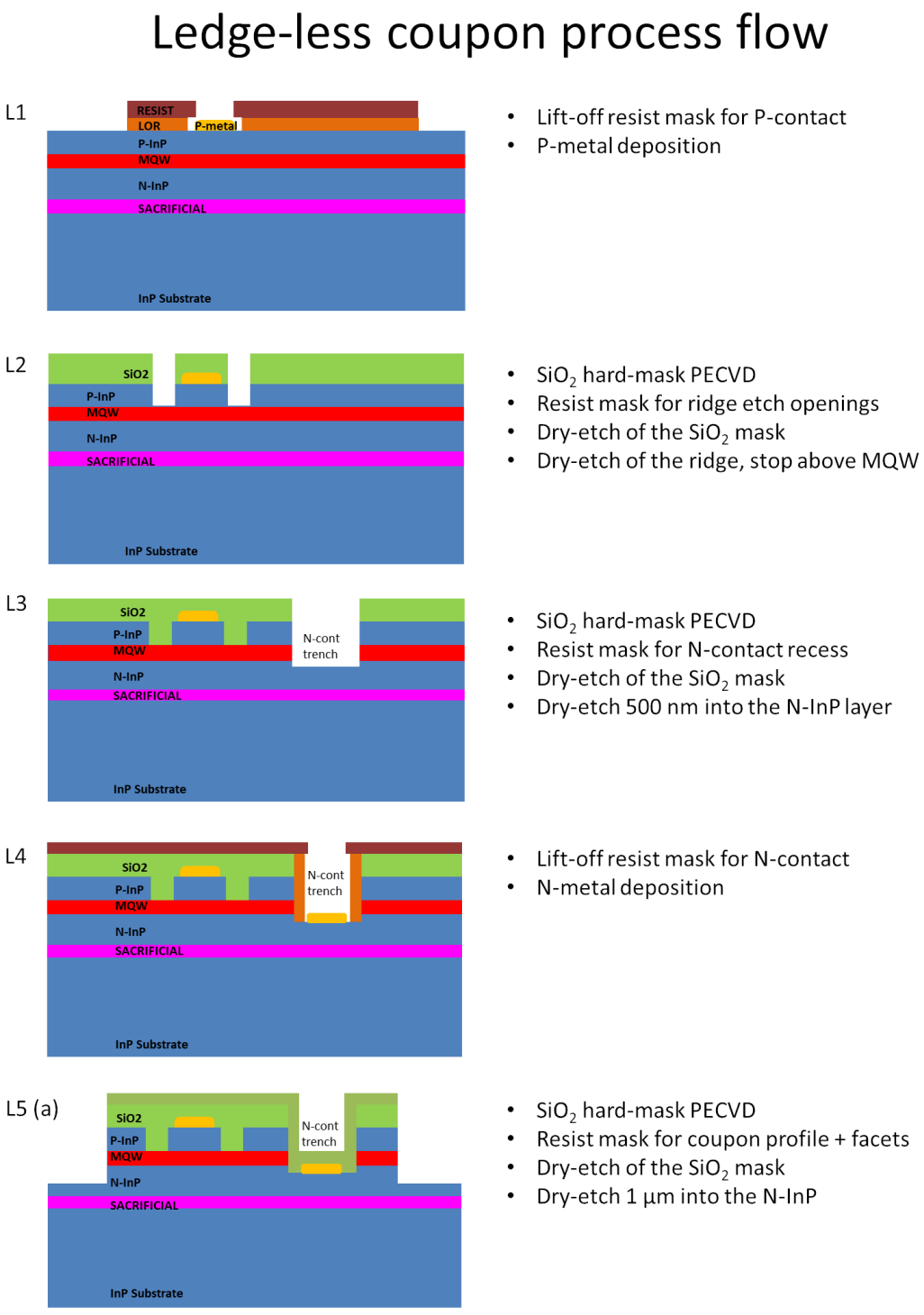
- Spin a 2.8 μm thick resist layer of S1828 on the sample.
- Lithography L10, expose with a dose of 400 mJ/cm^2 dose at 405 nm wavelength.
  - *Optional hard-bake (5 minutes at 125 °C) for anchors easier to break.

WET-ETCH OF THE SACRIFICIAL LAYER (AlInAs)

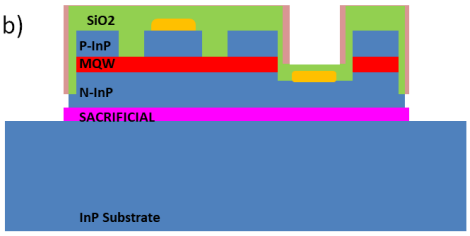
The goal of this step is to undercut the devices in order to release them from the original substrate. The released device will be ready for μTP.

- slice a piece of the chip for the undercut testing
- Etch in Iron chloride acid solution, $FeCl_3$:H_2O (1:2), at 1 °C
- Rinse multiple times and very gently in DI water by using a pipette until the acid is completely removed.
- Dry the sample gently by air-gun.
  - If tethers break during rinse, dry the sample in a hotplate at 60 °C, 1min.

Figure C.1: The diagram report the process steps according to the lithography levels. L1 defines the p-metal; L2 defines the ridge; L3 defines the recess to access the N-InP layer; L4 defines the N-contact; L5 (a) defines the facets together with the coupons profile and (b) the encapsulation without ledge around the coupon; L6 opens the passivation layers to access the P- and N-contacts; L7 defines the metal probing pads; L8 defines the anchor system.

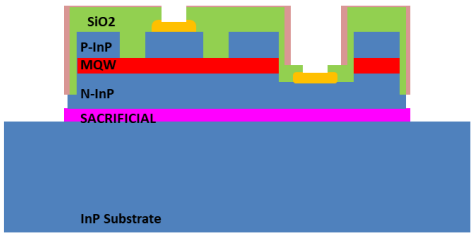


L5 (b)



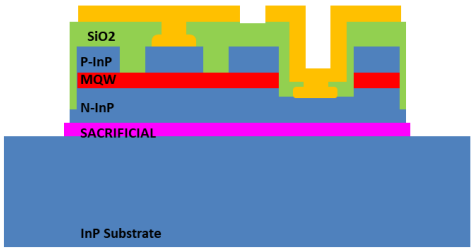
- SiO_2 hard-mask PECVD, facet passivation
- SiN hard-mask PECVD
- Dry-etch of the SiN+SiO_2 mask
  - **The sidewall remain passivated**
- Wet-etch to the sacrificial
- Dry-etch 500 nm to the InP substrate

L6



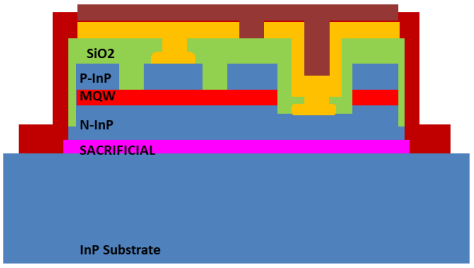
- Resist mask to open P- and N-contacts
- Dry-etch the SiN+SiO_2 mask

L7



- Lift-off resist mask for probing pads
- Pad-metal and HR-mirror deposition

L8



- Resist mask for the anchors

Appendix D

Recesses on the SOI for laser edge-coupling

In this appendix is reported the process for the fabrication of the recesses type 1 and type 2 on a SOI wafer. These type of recesses are suitable for transfer printable InP laser of different thickness. In addition, the process includes the micro transfer printing to the new substrate and the definition of polymer waveguides.

PROCESS DATA

Wafers: SOI
Date: May 2018
Designer: Ruggero Loi

L1 SOI WAVEGUIDES, RECESSES, ALIGNMENT MARKERS.

The first level of lithography defines the SOI waveguides and opens the SOI layer on the recesses area; the level includes the definition of fiducial markers for alignment by pattern recognition. Some alignment markers for the following lithography levels are defined too.

- Spin a 400 nm thick layer of ZEP resist on the sample.
- Lithography L1 at the e-beam, expose with a dose of 60 $\mu C/cm^2$.
- Si dry-etch with Cl_2:N_2 chemistry and by using the end point detection for target depth at $\sim$220 nm to the SiO_2.
- Measure real depth of the recess at the profilometer.

L2 RECESSES ON THE SiO_2 LAYER OF THE SOI

The second lithography defines the recess-profiles aligned to the SOI waveguides. The recess depth into the SiO_2 depends on the recess arrangement chosen (i.e. trench type 1 or type 2).

- Spin a 1.3 μm thick resist layer of AZ5214 on the sample.
- Lithography L2, expose with a dose of 140 mJ/cm^2 dose at 405 nm wavelength.
- SiO_2 dry-etch with CF_4:CHF_3 chemistry and by using the end point detection for target depth at $\sim$1800 nm into the SiO_2.
- Measure real depth of the recess at the profilometer.

L3 ETCH TO THE SUBSTRATE

The third level of lithography opens a trench to the Si substrate suitable for the thermal via.

- Spin a 2.8 μm thick resist layer of S1828 on the sample.
- Lithography L3, expose with a dose of 400 mJ/cm^2 dose at 405 nm wavelength.
- Etch of the SiO_2 to the substrate
  - Type 1 trenches: wet-etch with BOE 5:1.
  - Type 2 trenches: dry-etch with CF_4:CHF_3 based chemistry.

L4 THERMAL VIAS AND ALIGNMENT MARKERS FOR μTP

Level 4 defines the thermal via and the alignment markers of the target for the μTP. The marker have to comply with the standards required by the pattern recognition software.

- Create a lift off resist structure with a 2.8 μm thick S1828 resist layer and a 1 μm thick LOR-10A layer.
- Lithography L4, expose with a dose of 140 mJ/cm^2 dose at 405 nm wavelength.

- Metal evaporation:
  - Type 1 trenches: flat evaporation of a Ti:Au metal layer of calibrated thickness for vertical alignment of the coupon.
  - Type 2 trenches: low rate 1 Å/s flat evaporation of a Ti:Au (10:110) nm metal layer + a low rate 1 Å/s 360° angled Ti:Au metal layer of calibrated thickness for vertical alignment of the coupon and thermal sink to the substrate.
- Measure real depth, RMS-roughness and flatness of the printing area at the profilometer.
- SEM inspection of the trenches (in particular of the printing surfaces for defects).
- Nomarsky microscope inspection of the printing areas for double checking presence of defects.

PREPARATION OF THE PRINTING SURFACE

This step of the process regards the treatment of the hosting substrate to allow the device to be printed onto it with and without adhesive layers. This step must be performed just before the transfer printing in order avoid degradation or dirtying of the printing surface.

- Adhesive-less printing:
  - Depending on the surface the treatment may vary.
  - Important: to have clean smooth surfaces (S_q<3 nm) with flatness f<1 nm/μm.
- Print with adhesives:
  - Spin the adhesive layer of calibrated thickness. Thermal treatment are usually required pre and post printing.
  - Print inside recesses may require spray coating or evaporation of the adhesive layer in order to keep uniform the thickness of the adhesive layer.

TRANSFER PRINTING

This is the last step of the heterogeneous integration of the laser to the silicon photonics. If polymer waveguides are used they can be defined on the SOI pre- or post-integration.

- Test pickup of the coupons by manually acting a PDMS stamp.
- Test printing of the coupon on test surfaces.
- Pick-up and print of the devices using alignment markers and pattern recognition at the transfer printer.
- Anchors removal.

L5 SU-8 WAVEGUIDES DEFINITION

Some of the recesses fabricated on the SOI-PIC expect the laser integrated into them to be edge-coupled to polymer waveguides. The waveguides can be defined prior or post integration of the device on the oxide cladding layer of the SOI.

- Prepare an SU8-polymer of calibrated 1 μm thickness on the sample.
- Lithography L5 at the e-beam, expose with a dose of 5 $\mu C/cm^2$ (to be optimized). Develop with EC solvent and IPA.
- Cure the polymer at 180 °C according to the datasheet guidelines.
  - *Optional: SiO_2 cladding deposition at the sputter.