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Low-power SAR ADC for Biomedical portable devices

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Declaration

This is to certify that the work I am submitting is my own and has not been submitted for another degree, either at University College Cork or elsewhere. All external references and sources are clearly acknowledged and identified within the contents. I have read and understood the regulations of University College Cork concerning plagiarism and intellectual property.

Madhan Venkatesh
December 2024

Abstract

In energy constrained edge devices such as wireless sensor nodes, Internet of Things (IoT) devices and biomedical implants, ultra-low power operation is a critical consideration when operating from a lifetime battery or an energy harvesting source. In such applications, it is important to ensure that all the sub-blocks are optimally powered, which means that each sub-block is provided with just enough energy to complete its task and no more.

Successive-Approximation-Register (SAR) Analog to Digital Converters (ADCs) stand out as the preferred choice for such applications due to their remarkable energy efficiency and nearly digital architecture. The SAR architecture's scalability allows for energy consumption optimisation across a broad spectrum of applications, ranging from a few kS/s for biomedical devices to a few MS/s for wireless communication. In SAR ADCs, the primary source of power dissipation is the comparator. Unlike other digital blocks such as control logic and DAC switching, the comparator's energy consumption does not scale in the same manner with the supply voltage.

Reducing power consumption in SAR ADCs with resolutions exceeding 10-bits poses challenges due to the power required in the comparator to meet stringent quantization noise specifications at low supply voltages. For medium resolutions (8-12 bits), the comparator typically constitutes 50%-60% of the ADC's energy consumption.

This thesis focuses on the design and implementation of a low-power embedded 14-bit SAR ADC on a 65nm Complementary Metal-Oxide-Semiconductor (CMOS) process. The thesis introduces a switched-supply based comparator that reduces the effective supply voltage of the comparator during the decision phase without the requirement of a dedicated DC-DC down converter or an external supply rail. The proposed comparator achieves a 28% power consumption reduction when compared to the conventional designs. In addition, the design utilises a clock-boosting circuit instead of a bootstrapped switch on the input switch without degrading the achievable Signal-to-Noise-and-Distortion ratio (SNDR) and also achieves 46% reduction in power consumption compared to the bootstrapped switch. Synchronous low-power handcrafted logic is used to further reduce the power consumption. The 14-bit SAR ADC was fabricated in 65 nm CMOS and consumes 9.14 μ W from a 1 V supply and achieves an SNDR of 71.7 dB at 0.5 MS/s resulting in a Walden Figure of Merit (FOM) of 5.7 fJ/Conv.

This thesis also presents a programmable switched-supply comparator that uses a programmable reservoir capacitor to achieve a reduced effective supply voltage

during the decision phase. This comparator achieves up to 50% power consumption reduction compared to a conventional dynamic comparator. Fabricated in 65nm CMOS, the silicon results of the PMOS-input programmable comparator show programmable power consumption and energy efficiency ranging from 2.7 - 4.1 μW and 0.22 - 0.5 pJ/conv, respectively. Similarly, the input-referred noise can be programmed from 100 - 180 μV_{rms} . Additionally, the power (energy efficiency) and input-referred noise can be programmed at any clock cycle, making this design an ideal solution for a two-comparator SAR ADC architecture.

In summary, this thesis presents design techniques focused on reducing the energy per conversion of SAR ADCs, with a primary emphasis on minimising energy during the comparison phase, making the developed design an excellent choice for IoT applications.

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Dedication

To my parents Sudha and Venkatesh for their lifelong support which made everything possible, to my wife Cathy and her family, my friends Sachin, Sagar, Anthony, Monish and Ghegappa.

“The magic you are looking for is in the work you are avoiding.”

- **Wise man**

Acronyms

ADC	Analog to Digital Converter
BBM	Break Before Make
CDAC	Capacitive Digital to Analog Converter
CDF	Cumulative Distribution Function
CMOS	Complementary Metal-Oxide-Semiconductor
CMFB	Common Mode Feedback Circuit
DAC	Digital to Analog Converter
DEC	Digital Error Correction
DNL	Differential Non-Linearity
ENOB	Effective Number of Bits
FFT	Fast Fourier Transform
FoM	Figure of Merit
INL	Integral Non-Linearity
LSB	Least Significant Bit
MIM	Metal-Insulator-Metal
MOM	Metal-Oxide-Metal
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MSB	Most Significant Bit
PDK	Process Design Kit
PVT	Process, Voltage, Temperature
QFN	Quad Flat No-leads
RFID	Radio-Frequency Identification
SAR	Successive Approximation Register
S/H	Sample and Hold
SR	Set-Reset
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
TSMC	Taiwan Semiconductor Manufacturing Company

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Chapter 1

Introduction and Motivation

1.1 Internet of Things

The phrase “Internet of Things” was first coined in 1999 by the computer scientist Kevin Ashton during his work at Procter & Gamble to promote Radio Frequency Identification (RFID) technology. The Internet of Things (IoT) [1, 2] can be defined as a network of interconnected things that are capable of sensing, actuating, communicating and interacting with each other and their surroundings. These smart things or smart objects can share data and autonomously react to physical world events, initiating processes and services with or without direct human intervention. The Internet of Things has the potential to revolutionise our daily interactions. Through a network of sensors and cameras, a large amount of data will be collected, processed, and used to optimise various aspects of our lives [3–7]. Moreover, this network is currently evolving rapidly, becoming significantly more dynamic. In the early IoT iterations, the sensory nodes were stationary, located in fixed positions, and transmitted the collected data to the cloud for analysis and interpretation. However, in the evolving IoT world, nodes are attached to drones, robots, humans, and vehicles, transforming from mere data collectors to closed-loop systems capable of sensing and interpreting, enabling distributed autonomous behaviour [8].

Integrated Circuits (ICs) play a vital role in the internet of things (IoT) ecosystem, enabling connectivity, miniaturisation, sensor integration, data processing, and security. They drive the proliferation of IoT devices by facilitating energy-efficient designs and enabling real-time data collection [9]. IC scalability and cost-effectiveness have led to widespread adoption of the IoT. Emerging trends like Artificial Intelligence (AI) integration and low-power designs promise further advancements in IoT technology, shaping its future landscape.

Figure 1.1 shows some of the application areas of IoT. The Internet of Things has become common in our lives because it is being used by a wide range of appli-

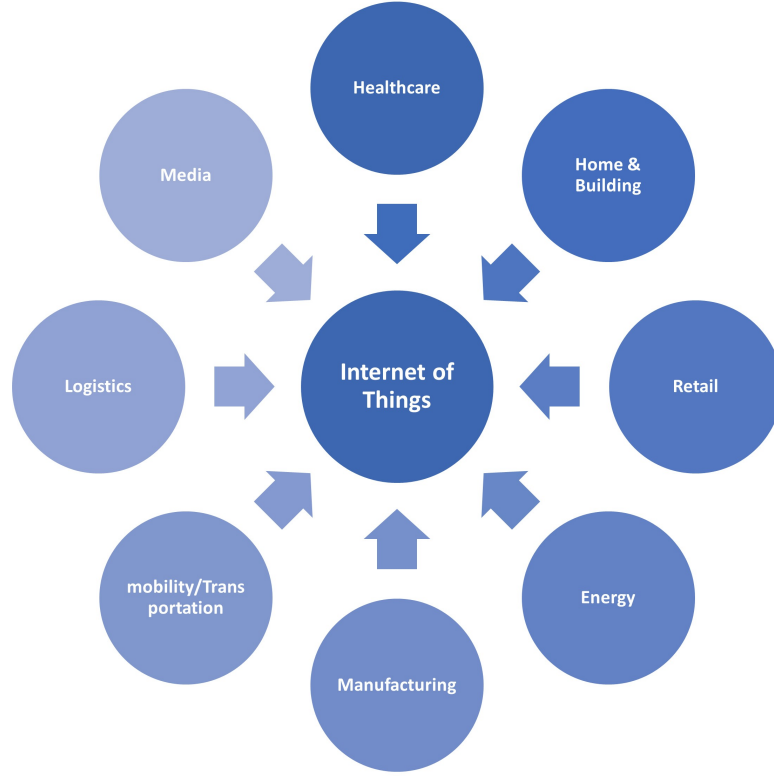


Figure 1.1: Applications of Internet of Things.

cations. By 2025, it is estimated that there will be 75 billion devices worldwide [10]. Healthcare is one of the sectors that is expected to benefit greatly from this growth. IoT is also transforming other sectors beyond healthcare, such as transportation, manufacturing, and agriculture, and has the potential to reshape our society as a whole.

1.2 Biomedical acquisition system

Wearable and implantable biomedical systems, which interact with the body and nervous system, are increasingly vital tools in our quest to promote wellness and advance healthcare. In 2021, the global medical electronics market was valued at US\$6.3 billion, and it is projected to grow to US\$8.8 billion by 2026. This growth is driven by various factors, such as the ageing population and increased life expectancy, the adoption of IoT enabled smart medical devices, the growing demand for portable medical equipment, and the ongoing advancements in disease diagnosis and treatment techniques [11].

Advancements in low-power CMOS circuit design have made portable health monitoring a reality today [12–15]. These technological breakthroughs have enabled the development of energy-efficient devices capable of monitoring various health parameters, from wearable fitness trackers to remote patient monitoring systems.

Improvements in low-power CMOS circuit design are helping to create better ways to monitor health with portable devices [16–21]. This makes healthcare more accessible and more effective. These medical tools have progressed significantly in recent years since their early stage, becoming more selective, sensitive, intelligent, and adaptable to various modes. They must now accurately capture weak signals, even in noisy and high-interference conditions. Integrated circuits and System on a Chip (SoCs) must perform all these functions with strict power and size limits.

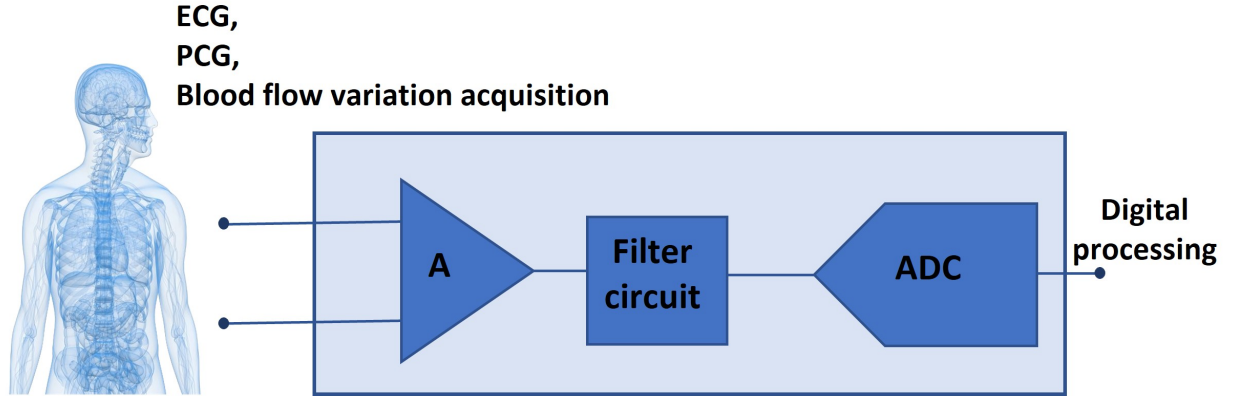


Figure 1.2: Biomedical Acquisition System consisting of a gain stage (A), Analog filtering, and an Analog to Digital Converters.

In modern electronic implantable devices, such as monitoring and treating epilepsy and Parkinson’s disease, electrodes collect biological signals that are then amplified, converted into digital signals for analysis (for example, for the detection of epilepsy seizures) and transmitted wirelessly as necessary. An important focus in the design of nearly all battery-powered implantable devices is reducing the power consumption of their integrated circuits.

Figure 1.2 shows the block diagram of the Biomedical Acquisition Circuit consisting of a gain stage (A), Analog Filtering, and Analog to Digital Converters (ADCs). ADCs are a key component of biomedical devices used in health monitoring, and reducing their power consumption is of utmost importance [22]. Bio-potential signals typically have amplitudes in the micro-volt to milli-volt range, and the frequency range of interest for these signals is from 0.01 Hz to 10 kHz [23]. Biomedical implants often require a low sampling rate mainly due to the narrow bandwidth of biological signals [14],[13]. Energy efficiency in both normal operation and standby mode for long-term operation of the ADCs is important to eliminate the need for frequent battery replacements. Among the different ADC architectures [24], the Successive Approximation Register (SAR) ADCs are ideal for bio-potential digitisation in battery operated portable devices; firstly, because of their low analog complexity and mainly because they consist of digital circuits that become faster and consume less lower power as technology scales.

Table 1.1 ADC target specifications.

Specification	Target
Technology	TSMC 65 nm
ENOB	12
Sample rate (MSps)	0.5
Supply Voltage (V)	1
SNDR (dB)	> 70
Power (μ W)	< 70

1.3 Research goals and Thesis Structure

This thesis focuses on the design and implementation of a low-power embedded 14-bit SAR ADC in a 65nm process, with a primary emphasis on minimising the energy consumption of various blocks in the SAR ADC. The structure of the thesis is as follows.

- **Chapter 2** provides an overview of the fundamentals of Analog to Digital converters, important dynamic and static performance metrics of ADCs, the classification of ADCs, as well as ADC figures of merit and their trends with bandwidth and resolution.
- **Chapter 3** gives an overview of the SAR ADC and reviews the current start-of-the-art of low-power SAR ADCs. It also discusses current state of the art low-power comparators and several Capacitive DAC switching schemes and discusses the main considerations to achieve low-power SAR ADC design. The chapter concludes with a discussion of the advances in reducing the energy consumption of various blocks (DAC, controller, and comparator) inside a SAR ADC to reduce its Walden FoM over the years.
- **Chapter 4** introduces the proposed architecture to implement the 14-bit SAR ADC on a 65nm process. It introduces a switched supply based comparator that reduces the effective supply voltage of the comparator during the decision phase without the requirement of a dedicated DC-DC down converter. The proposed comparator achieves a reduction in 28% power consumption compared to conventional designs. In addition, the design utilises a clock boosting

circuit instead of a bootstrapped switch on the input switch without degrading the achievable SNDR and also achieves a reduction in 46% power consumption compared to a bootstrapped switch. The 14-bit SAR ADC was fabricated in 65 nm CMOS and consumes 9.14 μ W from a 1 V supply and achieves an SNDR of 71.7 dB at 0.5 MS/s resulting in a Walden FoM of 5.7 fJ/Conv.

- **Chapter 5** presents the design and implementation of a programmable switched-supply comparator that uses a programmable reservoir capacitor to achieve a reduced effective supply voltage during the decision phase. This comparator achieves a reduction in power consumption of up to 50% against the conventional dynamic comparator. The silicon results of the PMOS-input programmable comparator show programmable power consumption and energy efficiency ranging from 2.7 - 4.1 μ W and 0.22 - 0.5 pJ/Conv, respectively. Similarly, the input-referred noise can be programmed from 100 - 180 μ Vrms. Additionally, the power (energy efficiency) and input-referred noise can be programmed at any clock cycle, making this design an ideal solution for the two-comparator SAR ADC architecture.
- **Chapter 6** presents the details of a 14-bit, low-power, 277 kS/s SAR ADC using the programmable switched-supply comparator, implemented in a 65nm CMOS process. This work details the design and integration of the programmable switch supply comparator within the SAR ADC, replacing coarse and fine comparators to address mismatch issues and reduce power consumption. In summary, this chapter presents design techniques focused on reducing the energy per conversion of SAR ADCs, with a primary emphasis on minimising energy during the comparison phase, making it an excellent choice for IoT applications.
- **Chapter 7** provides a chapter-wise summary of the thesis and evaluates the overall performance of the design within the context of current state-of-the-art solutions. It discusses factors limiting the design's performance and offers recommendations for future work aimed at improving performance and reducing the overall energy consumption of a data acquisition system.

1.4 Publications

The work outlined in this thesis has led to the following publications to date:

- M. Venkatesh, G. M. Salgado, K. G. McCarthy and I. O'Connell, "A 500 kS/s 71.8 dB 5.7 fJ/Conv-step Switch Supply Based Comparator SAR ADC for Biomedical Portable Devices," 2023 IEEE Biomedical Circuits and Systems

Conference (BioCAS), Toronto, ON, Canada, 2023, pp. 1-5, doi: 10.1109/BioCAS58349.2023.10388868.

- M. Venkatesh, G. M. Salgado, K. G. McCarthy and I. O'Connell, "A Low Power Programmable Switch Supply Dynamic Comparator," 2024 IEEE International Symposium on Circuits and Systems (ISCAS), Singapore, 2024, pp. 1-5, doi: 10.1109/ISCAS58744.2024.10558322.

Chapter 2

Fundamentals of Analog to Digital Converters

2.1 Analog to Digital converter fundamentals

In every IoT application, the gathering of data and its conversion into a digital format are essential components. The operation of an analog to digital conversion involves a series of basic elementary steps. In Figure 2.1, an Analog to Digital converter is illustrated as a cascade of four functions: the anti-aliasing filter, sample and hold, analog to digital quantization and digital signal processing. A large body of literature provides a comprehensive background to these functions [22],[24],[25].

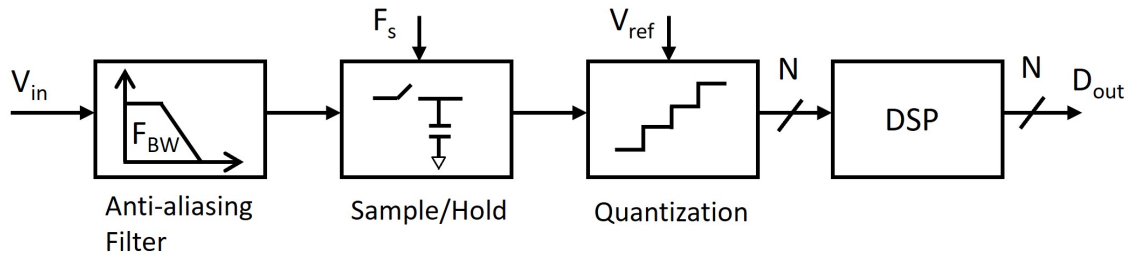


Figure 2.1: The basic functions of an A/D converter are represented in the block diagram, which includes an anti-aliasing filter, a sample-and-hold stage, analog-to-digital quantization, and digital signal processing.

2.1.1 Sampling

A continuous-time analog signal is converted into a discrete-time signal by the sampling process [22]. Sampling an analog signal makes it discrete in time but still continuous in amplitude. If $x(t)$ is the continuous-time analog signal, the sampled

signal $x[n]$ can be represented as:

$$x[n] = x(nT_s), \quad (2.1)$$

where T_s is the sampling period, n is an integer, and $x[n]$ denotes the value of the signal at the n^{th} sample. The sampler produces a series of delta functions where the amplitude matches the signal at the sampling instances. For uniform sampling with a period T_s , the output of the sampler can be expressed as:

$$x[n] = x(nT_s) = \Sigma x[t] * \delta(t - nT_s). \quad (2.2)$$

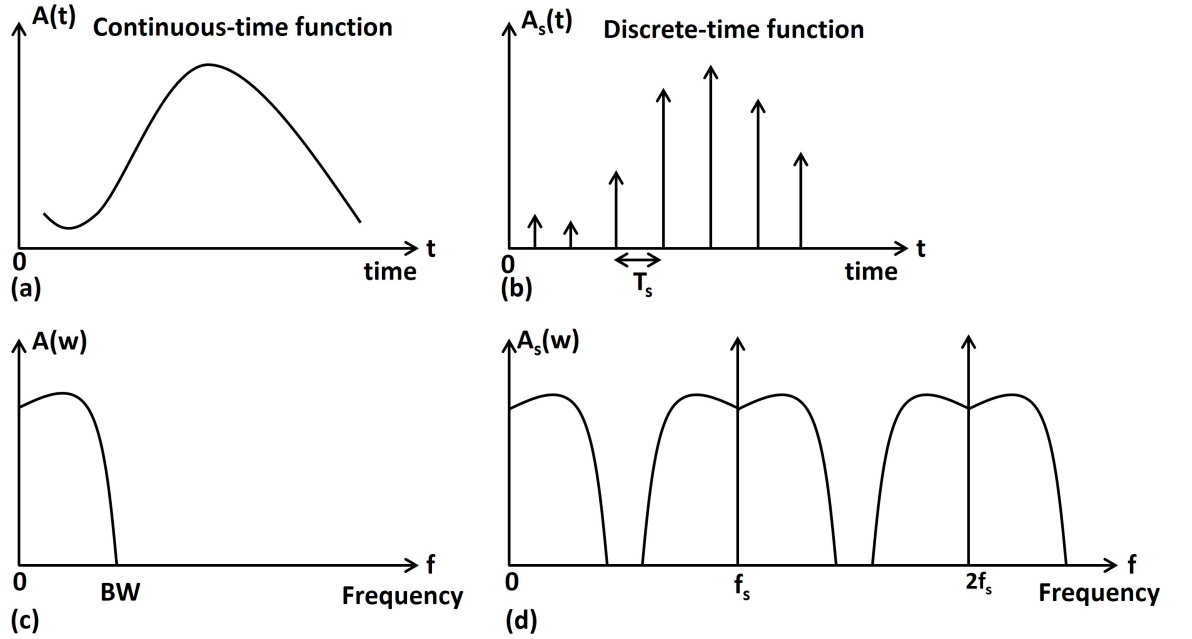


Figure 2.2: Sampling an analog signal (a) in the continuous-time domain results in a series of analog signal samples (b). The frequency domain of the continuous-time signal (c) is folded around the sampling frequency and its multiples (d).

A signal $A(t)$ is sampled at a rate f_s as shown in Figure 2.2. This signal corresponds in the frequency domain to $A(w)$ with a bandwidth from $f = 0$ Hz to $f = BW$. Mathematically, sampling is performed by multiplying the continuous-time function $A(t)$ with a sequence of Dirac pulses, resulting in a discrete-time signal $A_s(t)$ in Figure 2.2(b). The product of the continuous-time function and the Dirac sequence is defined for those time moments equal to multiples of the sampling period T_s . The Nyquist sampling theorem [22] specifies that the sampling frequency, f_s , must be at least twice the signal bandwidth BW (i.e. $f_s > 2*BW$) to avoid aliasing, as shown in Figure 2.3(a). If the sampling frequency, f_s , is less than twice the signal bandwidth, BW , the spectrum of the sampled signal will lead to the overlap of the

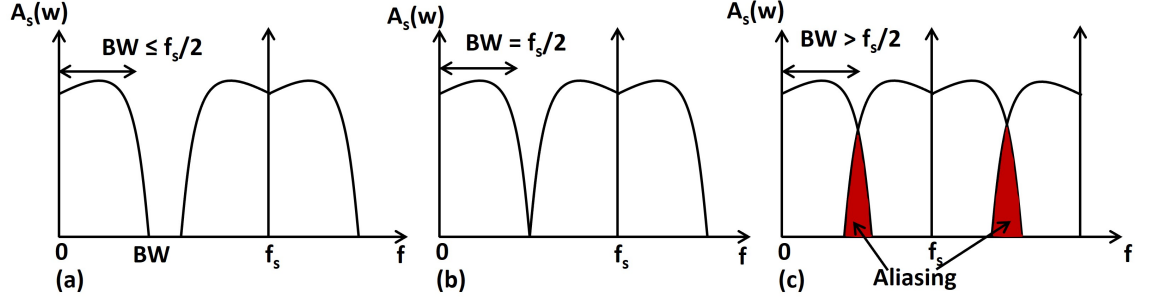


Figure 2.3: Illustration of relation between bandwidth (BW) and sampling frequency f_s as described by Nyquist sampling theorem [22]: (a) when $BW \leq f_s/2$; (b) when $BW = f_s/2$; (c) when $BW > f_s/2$, where overlapping signal bandwidth results in data mixing, a phenomenon known as aliasing.

signal bandwidths after sampling and mixing of the data, a phenomenon known as aliasing, as illustrated in Figure 2.3(c). Continuous-time periodic signals exhibit a repetitive spectrum due to their Fourier series representation, which consists of discrete harmonics repeating indefinitely. On the other hand, a non-repetitive spectrum is observed in continuous-time aperiodic signals, where the Fourier transform provides a continuous and unique frequency representation without periodicity.

2.1.2 Quantization

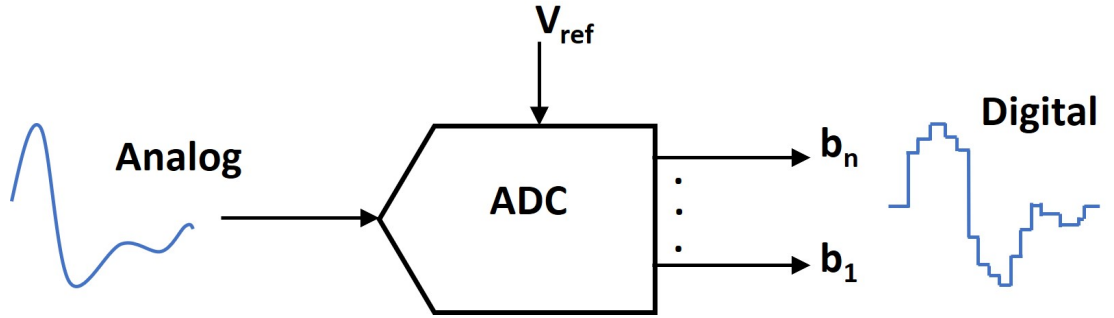


Figure 2.4: ADC block diagram showing the conversion of an analog input signal to its quantized digital representation.

The quantization operation involves the mapping of a continuous analog input into a finite range of discrete output values. This process introduces an associated quantization error, which is the difference between the original analog value and its quantized digital equivalent. The quantization error is an unavoidable fundamental limit of the process of quantization; it tends to zero as the number of bits grows to infinity. Figure 2.4 shows an ADC block diagram illustrating the quantized digital output. The resolution of the ADC is determined by the number of quantization levels. For example, an ADC with 10-bit resolution can represent the analog signal

using $2^{10} = 1024$ values. In simple terms, quantization can be considered to be a combination of division, normalisation, and truncation.

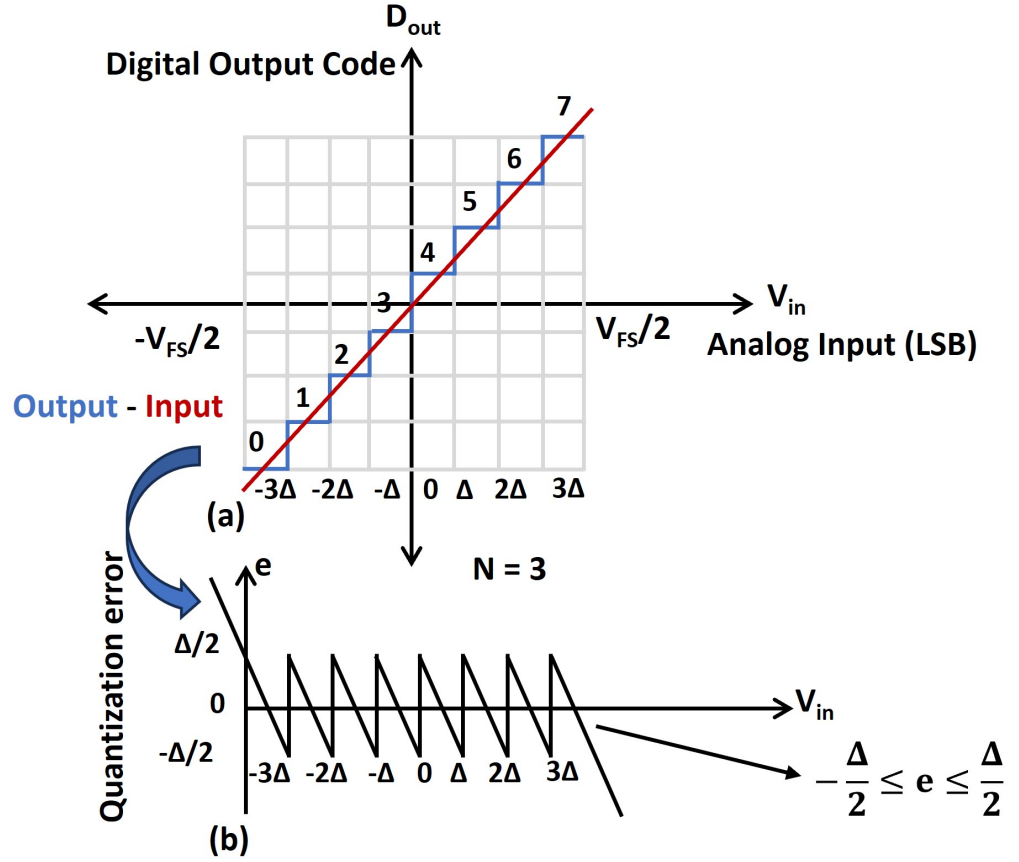


Figure 2.5: a) Transfer characteristics of an ideal 3-bit ADC and b) Relationship of quantized input signal and quantization error.

The quantization error is usually referred to as quantization noise. This results in a staircase transfer function where each step represents one LSB (Least Significant Bit). Figure 2.5(a) shows the transfer function of an ideal 3-bit ADC ($2^3 = 8$ codes) that maps the input voltages to the output codes. The blue colour signal is the digital output resulting from the analog input in red for the 3-bit conversion, as shown in Figure 2.5(a). Knowing the LSB size (Δ) is the key to converting between codes and voltages. The LSB size is equal to the full-scale input range divided by the total number of ADC codes given by Equation 2.3:

$$LSB\ Size(\Delta) = \frac{V_{FS}}{2^N}. \quad (2.3)$$

Where V_{FS} is the full scale input voltage of the ADC and N is the number of bits in the ADC output code. 2^N is equal to the total number of ADC codes. In general, the ADC input voltage is related to the output code by a relationship as shown in

Equation 2.4:

$$V_{in-conv}(V) = D_{out} * \Delta. \quad (2.4)$$

Where D_{out} is the digital output code.

From Figure 2.5(a) the magnitude of the quantization error is obtained by subtracting the input (red) from the output (blue) curves. This quantization error is bounded between $-\frac{\Delta}{2} \leq e \leq \frac{\Delta}{2}$; otherwise, the quantizer will become overloaded, resulting in a boundless quantization error, where Δ is the LSB size.

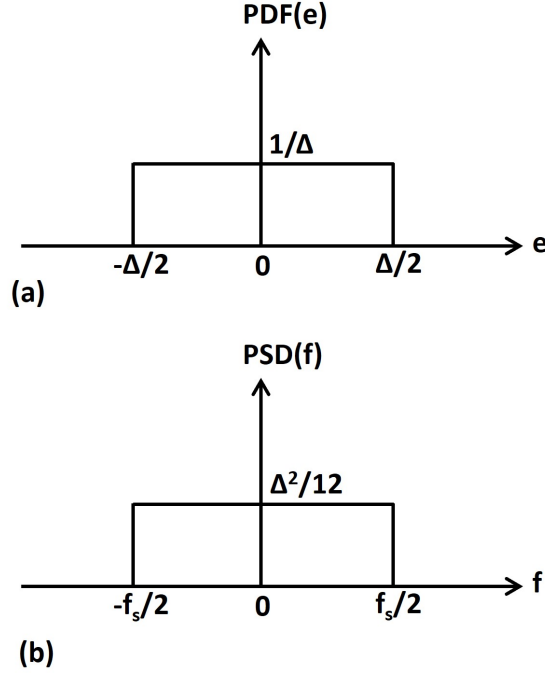


Figure 2.6: (a) Probability density function (PDF) of the Quantization error. (b) Power spectral density (PSD) of the quantization error.

The quantization error e is given by Equation 2.5, assuming $V_{in} \in [0, V_{FS}]$:

$$e = D_{out} * \Delta - V_{in} = D_{out} \left(\frac{V_{FS}}{2^N} \right) - V_{in}. \quad (2.5)$$

One of the limitations of every analog to digital converter is the quantization error. The Power Spectral Density (PSD) of the quantization error is evaluated by assuming $0 \leq V_{in} \leq V_{FS}$, $V_{in} \gg \Delta$, N is large, e is independent of V_{in} . The quantization noise is uniformly distributed and the quantization noise spectrum is white as shown in Figure 2.6(a), which is the probability density function (PDF) of the quantization error (e). It can be seen in Figure 2.6 (a), that the quantization error will be evenly distributed between $\pm\Delta/2$. Moreover, as depicted in Figure 2.6(b), the power spectral density of the quantization noise may remain uniform within the Nyquist frequency range. The quantization noise power σ_e^2 is determined

from Figure 2.6 as shown in Equation 2.6:

$$\sigma_e^2 = \int_{-\Delta/2}^{\Delta/2} e^2 \cdot \frac{1}{\Delta} \cdot de = \frac{\Delta^2}{12}. \quad (2.6)$$

This quantization noise provides a theoretical limit to the maximum achievable Signal-to-Noise-ratio for an ideal N-bit ADC.

2.2 Static performance metrics

Static/DC errors provide an understanding of the converter behaviour and its accuracy when converting DC or very low-frequency input signals. The accuracy of the ADC depends on several key metrics. These metrics include Differential Non-Linearity (DNL), Integral Non-Linearity (INL), offset error, and gain error. Each can be expressed in LSB or as a percentage of the full-scale range.

2.2.1 Differential Non-Linearity

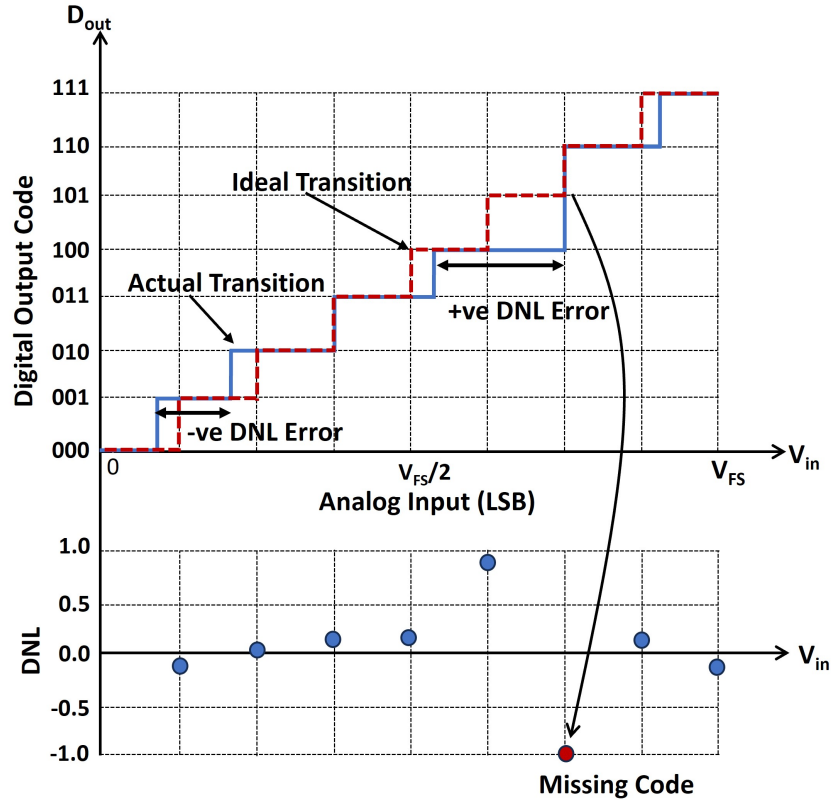


Figure 2.7: The dashed (red) line is the transfer characteristics of an ideal ADC with the width of each step equal to Δ . The transfer characteristics in blue shows a real 3-bit ADC illustrating DNL errors.

The DNL error [24, 25] is the difference between the actual step width and the ideal step width. DNL reveals how far a code is from the neighbouring code. If the actual step width is equal to 1 LSB, then the differential non-linearity is zero. If the DNL exceeds more than 1 LSB, the converter becomes non-monotonic, resulting in missing codes, as illustrated in Figure 2.7. A DNL error of $|E_{DNL}| \leq 1\text{LSB}$ guarantees no missing codes. Mathematically the DNL is given by:

$$DNL_K = \frac{k^{th} \text{ step size} - \Delta}{\Delta}. \quad (2.7)$$

2.2.2 Integral Non-Linearity

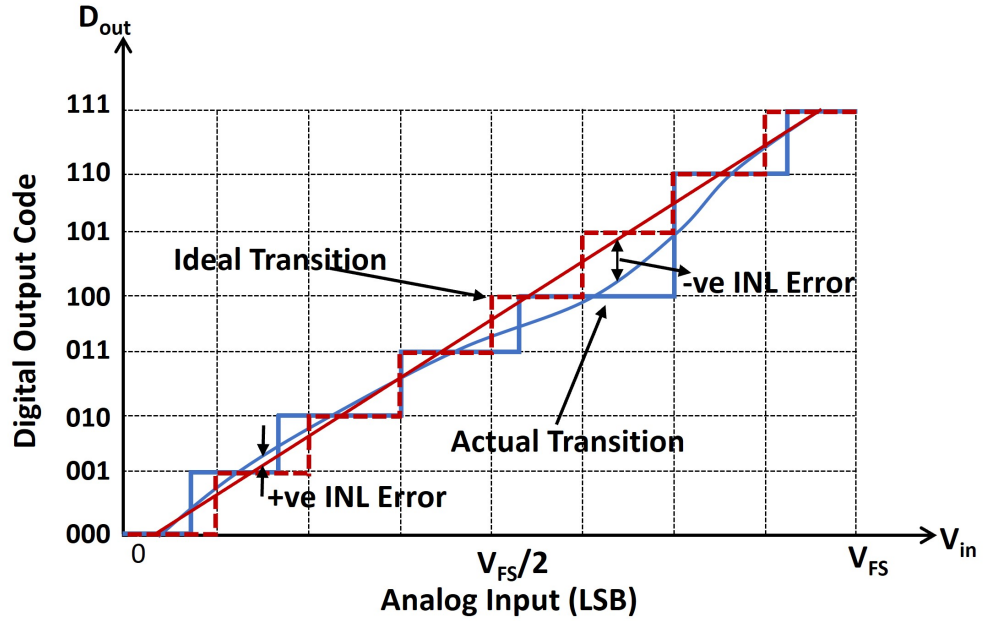


Figure 2.8: The dashed (red) line is the transfer characteristics of an ideal ADC with the width of each step equal to Δ and With the midpoints lie on the best fit line. The transfer characteristics (in blue) shows a real 3-bit ADC illustrating INL errors.

The INL [24, 25] is the deviation of the actual transfer function with respect to the ideal transfer function for an ADC as shown in Figure 2.8. It indicates the amount of deviation of the actual curve from the ideal transfer curve. INL for a given code is the summation of the DNL values up until that code. It can be also defined as the cumulative sum of DNL and its mathematical Equation is given by:

$$INL_i = \sum_{j=0}^i DNL_j. \quad (2.8)$$

With a DNL error of $|E_{DNL}| \leq 1\text{LSB}$, and a monotonic input-output characteristic,

there is no guarantee that the INL error is less than $\frac{1}{2}\text{LSB}$. If the INL error (E_{INL}) is $|E_{INL}| \leq \frac{1}{2}\text{LSB}$ and the input output characteristic is monotonic, the DNL is no more than $\pm 1\text{LSB}$. If the ADC exhibits a bow-shaped INL, it indicates that the second harmonic in the output signal is dominant. Conversely, if the ADC has an S-shaped INL, it suggests that the third harmonic is dominant (assuming that the input is not a DC signal).

2.2.3 Offset, Gain and Full scale errors

Offset error is defined as the difference between the nominal and actual offset points as shown in Figure 2.9 and can be positive or negative. The gain error is defined as the full-scale error minus the offset error as shown in Figure 2.9. The full-scale error is measured at the last ADC conversion on the input output characteristic and compared against the ideal ADC input output characteristic assuming a positive input voltage.

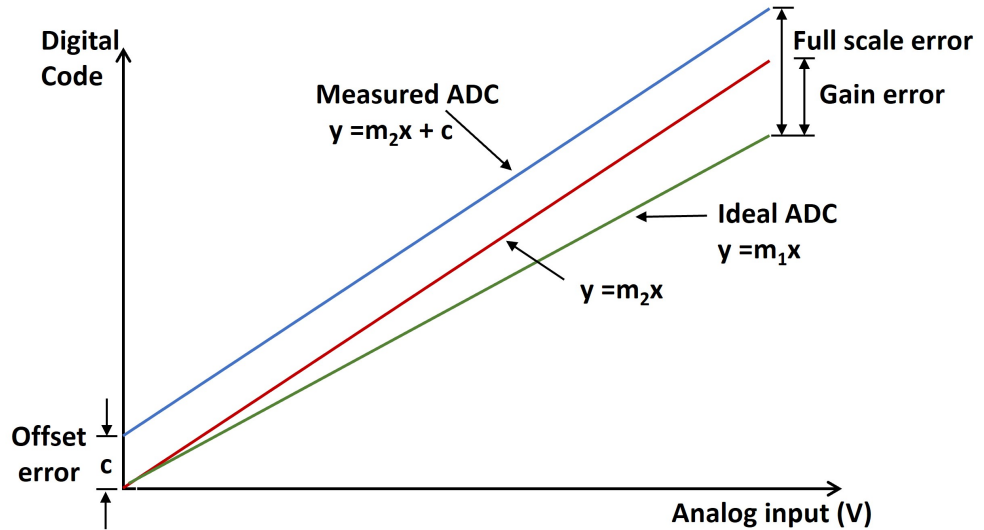


Figure 2.9: Diagram showing the offset error, gain error and full-scale error between actual and ideal Transfer function of an ADC.

2.3 Dynamic performance metrics

An ADCs performance is characterised by several key specifications when the input signal changes rapidly. These parameters, which define the ADCs dynamic performance, are typically measured using a single input frequency. The ADCs output array is analysed using the Fast Fourier Transform (FFT) to determine its dynamic specifications. Each specification is usually associated with input signal specs in terms of frequency and amplitude. The speed and frequency response of the analog

components of the ADC determine its dynamic performance. The Dynamic/AC performance is quantified using these metrics: Signal-to-Noise-Ratio (SNR), Total Harmonic Distortion (THD), Signal-to-Noise and Distortion ratio (SNDR), Spurious Free Dynamic Range (SFDR), Effective number of Bits (ENOB), and Dynamic Range.

Signal to noise ratio (SNR): SNR is the ratio of the signal power to the noise power. It is usually represented in decibels. It is calculated from the frequency spectrum of the ADC output and the SNR calculation usually integrates noise up to the Nyquist frequency. SNR reveals where the noise floor of the converter is. Figure 2.10 provides a graphical representation of SNR. In an ideal ADC with no noise sources and finite resolution, the maximum achievable SNR due to quantization noise alone (assuming a periodic sinewave signal) [22] is given by:

$$SNR[dB] = 6.02N + 1.76, \quad (2.9)$$

where N is the resolution of the ADC. For example, an ideal 10-bit ADC will have an SNR of 61.96 dB.

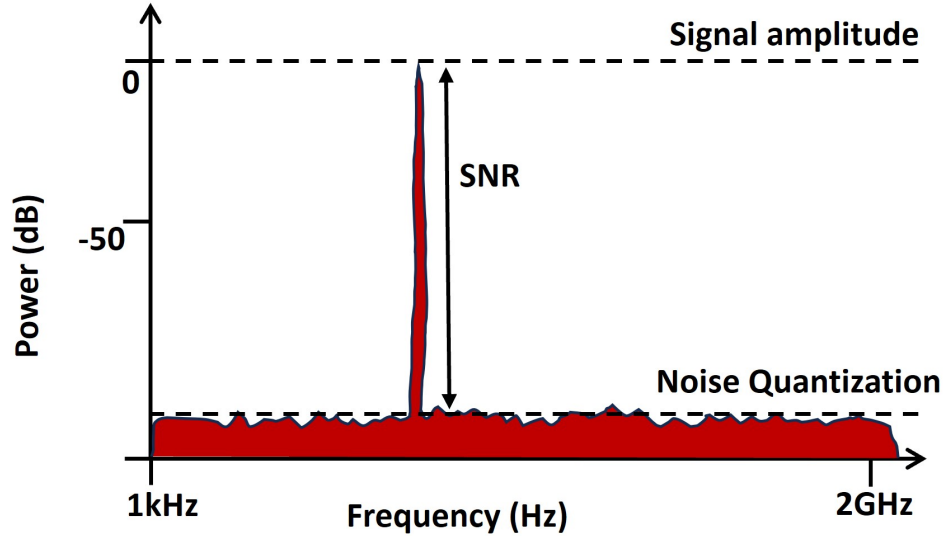


Figure 2.10: Signal to Noise ratio illustration.

Total Harmonic Distortion (THD): THD is defined as the ratio of the rms sum of the harmonic components to the fundamental harmonic within the band of interest. THD can be calculated (assuming a periodic sinewave signal) using Equation 2.10:

$$THD[dB] = 20 \log_{10} \left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + \dots V_n^2}}{V_1} \right), \quad (2.10)$$

where V_1 is the rms amplitude of the fundamental. V_2, V_3, V_4, V_5 and V_n are the rms amplitude of the second through n^{th} harmonics. THD provides information regarding the harmonic energy present in the frequency spectrum for a particular input frequency. The THD value increases with an increase in frequency. The THD should have minimum value for lower distortion. As the input signal amplitude increases, the distortion also increases. The THD value of an ADC should be low to achieve better performance.

Signal to Noise and Distortion Ratio (SNDR): SNDR is defined as the fundamental signal power divided by the power in the noise and harmonics. It provides information regarding the noise and harmonic energy present in the frequency spectrum. SNDR is a function of the input frequency. As frequency increases toward the Nyquist limit, SNDR decreases. SNDR can be calculated from SNR and THD (assuming a periodic sinewave signal) using Equation 2.11:

$$SNDR = -10 \log_{10} (10^{\frac{-SNR}{10}} + 10^{\frac{-THD}{10}}). \quad (2.11)$$

Dynamic Range : The dynamic range is the range of input signal powers where the SNDR or SNR is 0 dB or higher. An ADCs dynamic range is the range of signal amplitudes which the ADC can resolve. The dynamic range illustrates the

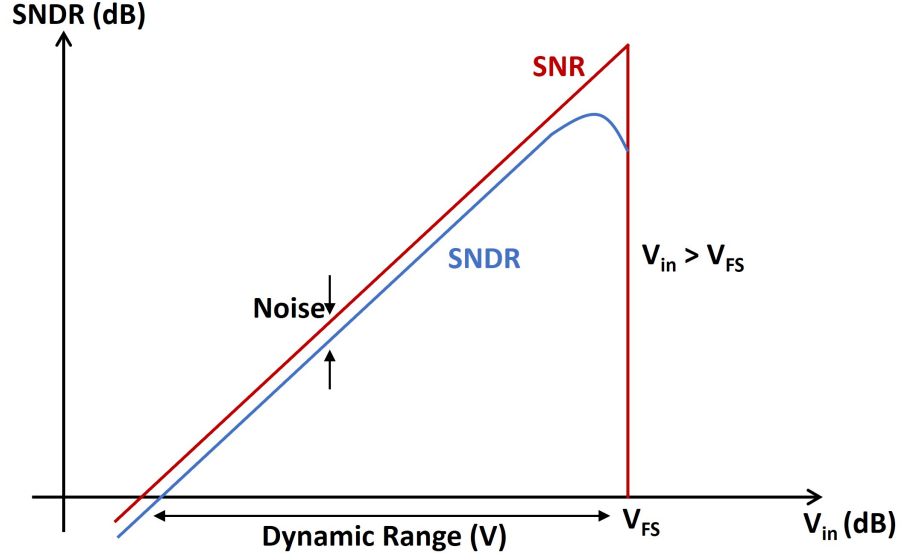


Figure 2.11: Dynamic range.

maximum achievable SNR as shown in Figure 2.11. The peak SNDR is limited by the larger signal distortion effects. The dynamic range is an important performance metric of an ADC for applications where signal strengths vary dramatically. If the signal is too large, it overranges the ADC input. If the signal is too small, it gets lost in the quantization noise of the converter.

Spurious Free Dynamic Range (SFDR) : SFDR is defined as the difference

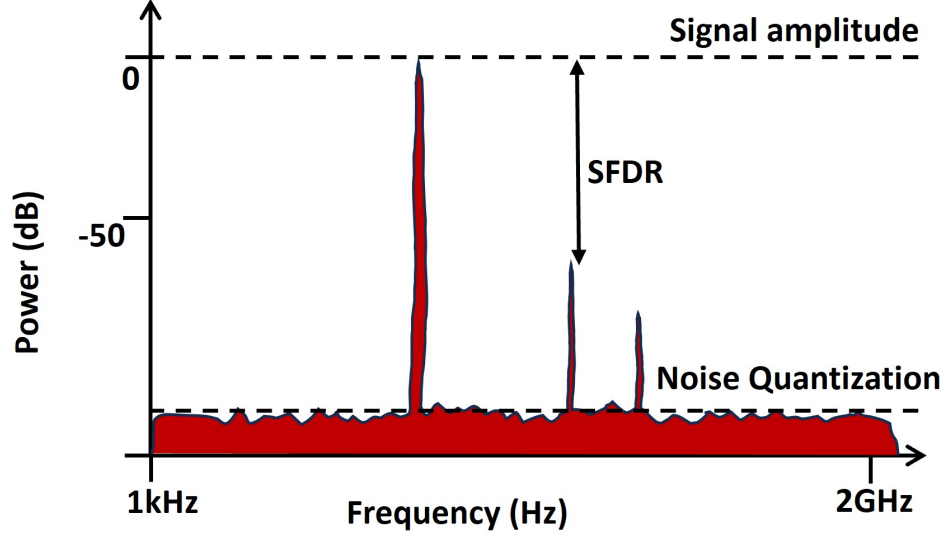


Figure 2.12: Spurious Free Dynamic Range illustration.

between the fundamental signal power and the maximum power of the remaining frequency in the output spectrum. The definition of SFDR is shown graphically in Figure 2.12. INL often shows major transitions and cubic/quadratic bows. For visible cubic or quadratic bows of INL [22], SFDR can be roughly estimated using the Equation below:

$$SFDR = -20 \log_{10} \left(\frac{INL_{fit}}{2^N} \right). \quad (2.12)$$

SFDR is important in certain communication applications that require maximising the dynamic range of the ADC.

Effective number of Bits (ENOB): ENOB is the number of bits that denotes the effective resolution of an ADC. It is derived from the fundamental quantization noise analysis of an ideal ADC [22], and the derivation is explained in the Appendix B.2. It is another way of representing the SNDR and is given by Equation 2.13:

$$ENOB = \frac{SNDR - 1.76}{6.02}. \quad (2.13)$$

2.4 Thermal noise

One of the fundamental limits of data converters is quantization noise. kT/C noise is another unavoidable limit in data converters. It is due to the unavoidable thermal noise associated with the sampling switch [22]. The kT/C noise only goes to zero for infinite sampling capacitance or zero temperature. This is why in any real sampled-data system it is described as a fundamental limit [25]. A basic sampling circuit using a single transistor is shown in Figure 2.13(a). The input voltage charges the capacitor

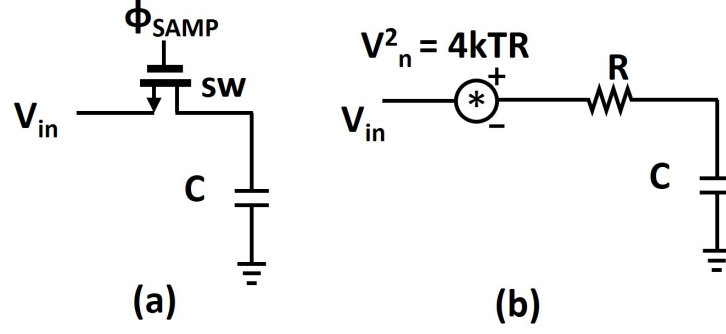


Figure 2.13: Basic sampling circuit. (a) Single transistor as sampling switch. (b) Equivalent thermal noise of sampling circuit.

through the sampling switch. At the sampling time, the switch is turned off, holding the input voltage across the capacitor. Figure 2.13(b) provides the equivalent circuit for the noise estimation. The resistance R_{ON} in Figure 2.13(b) represents the series on-resistance of the switch. The thermal noise power contributed by the resistor is given by:

$$\overline{V_n^2} = 4kTR \cdot \Delta f \text{ V}^2/\text{Hz}, \quad (2.14)$$

where k is the Boltzmann constant, T is the temperature in Kelvin, R is the on-resistance of the switch, and Δf is the noise bandwidth. The total output thermal noise power of an RC circuit is given by [22]:

$$\overline{V_n^2} = \frac{kT}{C} \quad (2.15)$$

$$V_n = \sqrt{\frac{kT}{C}}. \quad (2.16)$$

Hence, the total output noise power is independent of the value of R . Capacitors do not generate noise, but they do affect the total amount of noise in the circuit. For example, sampling any signal using a 1 pF capacitor introduces a noise voltage of 64.5 μ V. If the sampling capacitance increases by n the noise voltage reduces by $\sqrt{n}$.

2.5 RC settling

Settling time is the time at which the step response of a DAC enters and subsequently remains within a specified error band around its final value. The RC settling time of the Capacitive Digital to Analog Converter (CDAC) determines the minimum necessary settling time for each conversion step. The conversion time is determined by the comparator decision time, logic processing time, and Digital to

Analog Converter (DAC) settling time. The DAC settling time and the capacitance sizing dictate the switch sizes for the DAC.

Incomplete settling during the sampling stage will cause errors in the output and affect the overall accuracy of the ADC. Bigger capacitors are more advantageous for matching requirements and reducing the thermal noise, but they also increase the RC settling time constant of the circuit [22]. To assess the settling requirements, the sampling circuit can be viewed as an RC circuit where R represents the on-resistance of the sampling switch and C represents the total sampling capacitance of the CDAC, as depicted in Figure 2.14. For a N -bit ADC, assuming a full scale step input, the minimum time required to settle within $\frac{1}{2}LSB$ of the input voltage is given by:

$$T_s \geq \tau \cdot \ln(2 * 2^N), \quad (2.17)$$

where N is the resolution of ADC, T_s is the settling time, and τ is the time constant. For a 10 bit ADC, where $\frac{1}{2}$ LSB accuracy is desired, the ADC requires a minimum of 7.62 time constants of settling to ensure that the analog input voltage is captured accurately.

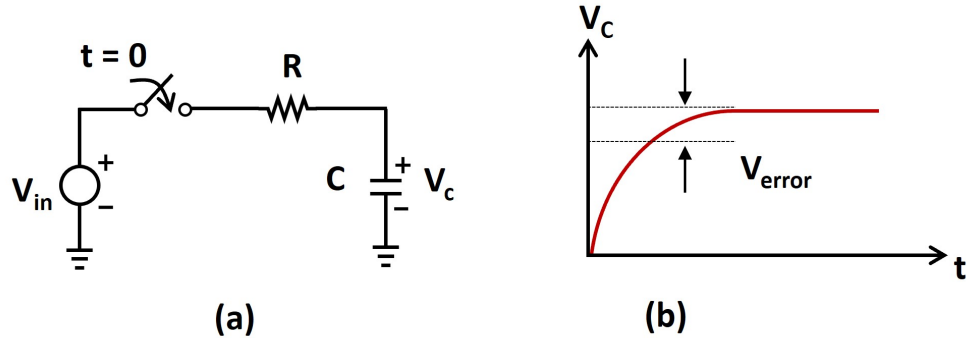


Figure 2.14: (a) Model of sampling circuit (b) RC settling time error.

2.6 Classification of ADCs

ADCs come in various types, each tailored for specific data rates, signal bandwidths, power consumption levels, and resolutions. Four of the most widely used ADC architectures are:

- Flash ADCs
- Pipeline ADCs
- Sigma-Delta ADCs
- Successive Approximation Register ADCs

Each of these ADCs has their own distinct trade-offs between resolution and sampling frequency, as illustrated in Figure 2.15. Furthermore, ADCs are classified as Nyquist rate or over-sampled converters based on the ratio of the input signal bandwidth f_{in} to the sampling rate f_s . In Nyquist rate ADCs, f_{in} can extend to $f_s/2$, while in over-sampled converters, as the name implies, f_{in} is much lower than $f_s/2$.

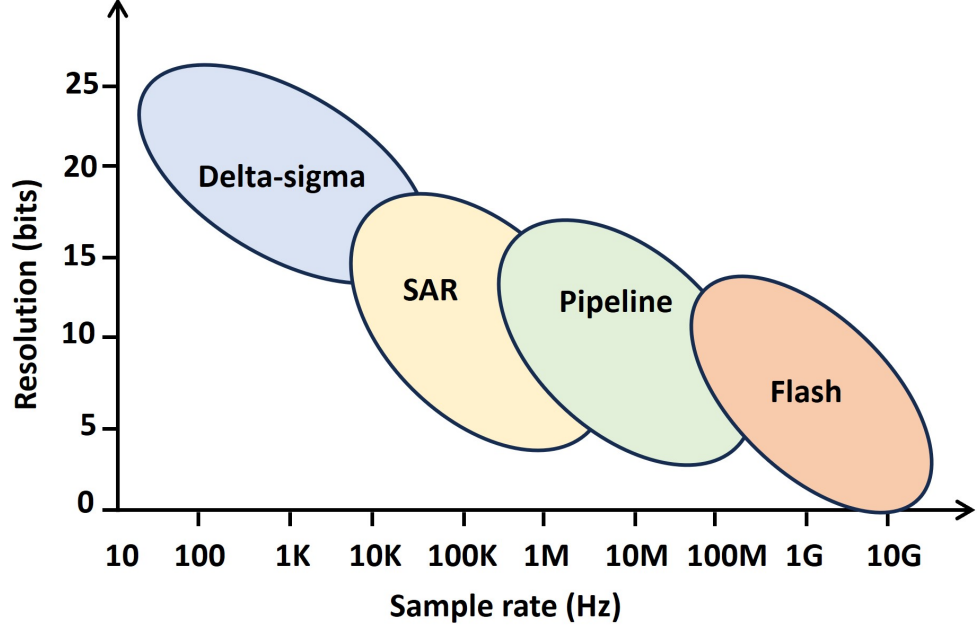


Figure 2.15: Comparison of ADC architecture with resolution and sampling rate.

2.6.1 Flash ADCs

Flash ADCs [26],[27] are generally used for high-speed applications, with a sampling frequency in the GHz range. Flash ADCs require 2^N resistors and $2^N - 1$ comparators, where N is the resolution of the ADC. Figure 2.16 shows the block diagram of a Flash ADC. In this ADC the input is sampled to all decision levels in parallel. As the resolution increases, the number of comparators also increases exponentially, so Flash ADCs are generally limited to resolutions less than 8 bits [28–32]. Additionally, comparator offsets further limit the maximum achievable resolution. Since Flash ADCs are used in high-speed designs, the signal and clock timing paths to each comparator need to be carefully designed [33–36]. Each comparator may sample a different input voltage due to mismatch propagation delay, and any mismatch in propagation delay causes an error at the output.

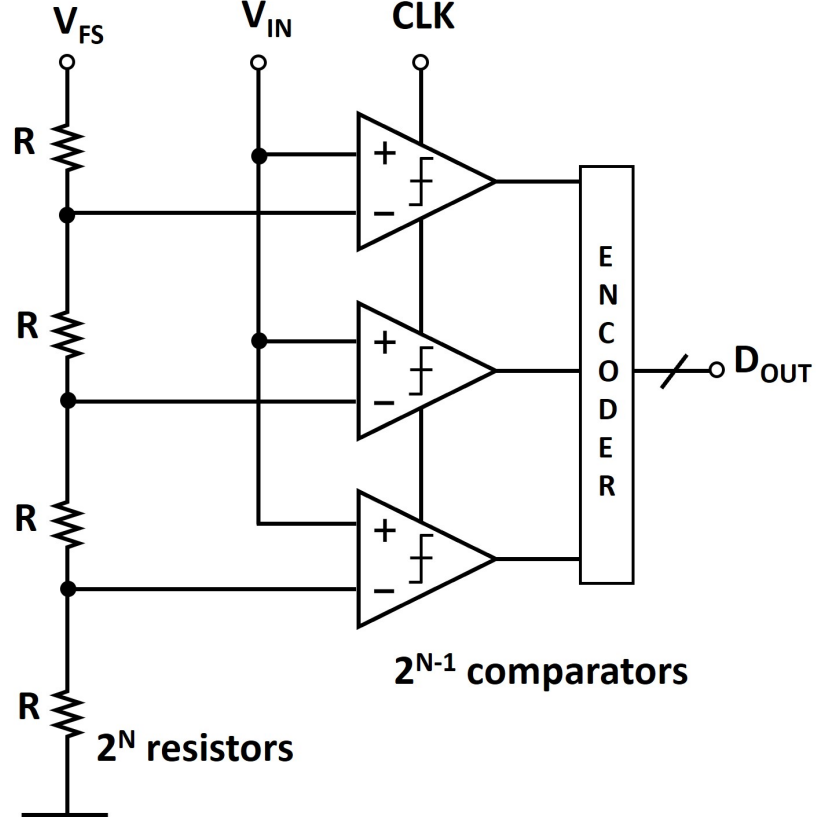


Figure 2.16: Flash ADC block diagram showing 2^N resistors, 2^{N-1} comparators and an Encoder.

2.6.2 Pipelined ADCs

The Pipelined architecture [37],[38] overcomes the limitation of the flash ADC architecture. This ADC divides the conversion task into several consecutive stages. Each of these stages, as illustrated in Figure 2.17, consists of a sample-and-hold circuit, an N-bit ADC, and an N-bit DAC. They can achieve sampling frequencies in the GHz range by cascading low-resolution stages. Pipeline ADCs achieve higher resolutions and dynamic range than flash ADCs [39–43]. The overall resolution of the ADC is the sum of the resolutions of the individual flash ADCs; however, some extra overlapping bits are required for error correction [22]. Pipeline ADCs are useful in configurations where latency (length of time necessary for all of the internal stages of pipeline to complete the conversion) is not critical (i.e., where the ADC is in open-loop path). In principle, a pipelined converter with k pipeline stages, each with a b -bit flash converter, can produce a high speed ADC with a resolution of $n = k * b$ bits using $k * (2^b - 1)$ comparators. Pipelined converters can achieve higher resolutions than flash converters with a similar number of comparators. However, this comes at the cost of increasing the total conversion time from one cycle to k cycles. Despite this, since each stage samples and holds its input, k conversions can be processed simultaneously. Thus, the total throughput can match that of a flash

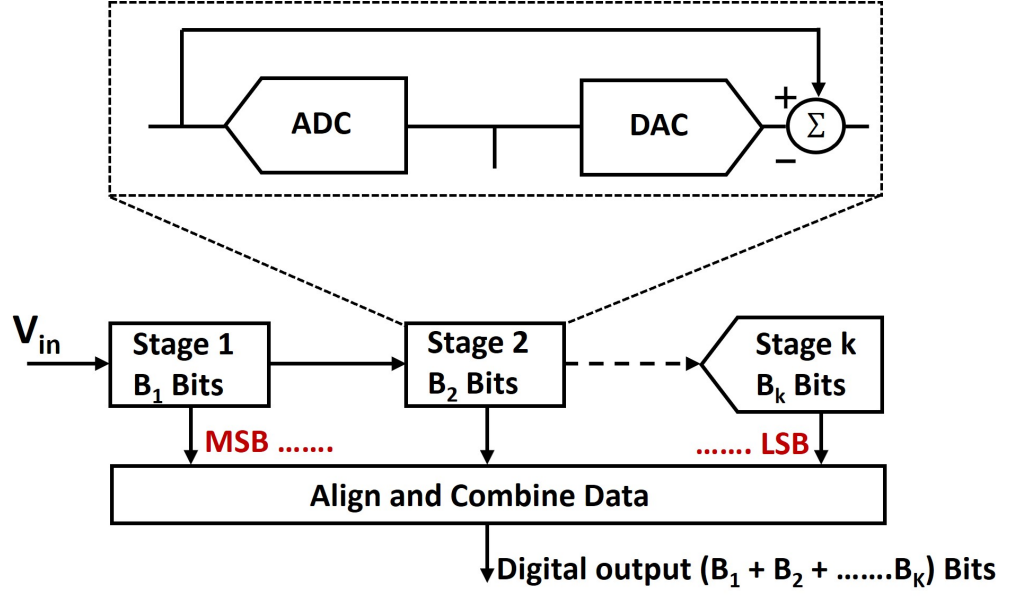


Figure 2.17: Pipeline ADC block diagram.

converter with one conversion per cycle. The key difference is that pipelined converters introduce a latency of k cycles equal to the number of stages in the architecture [44–47].

2.6.3 Sigma-Delta ADCs

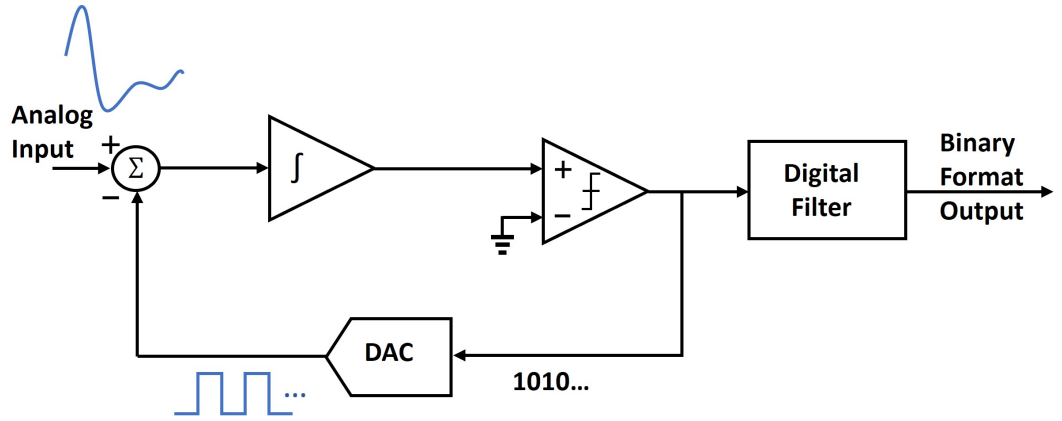


Figure 2.18: Sigma Delta ADC block diagram.

Sigma-Delta converters [48], [49] are used for high-resolution, low-bandwidth applications and use oversampled clocks (faster sampling rate). A basic first-order Sigma-Delta modulator consists of an integrator, a comparator, and a one-bit DAC as shown in Figure 2.18. The output of the DAC is subtracted from the input signal, and the resulting error signal is integrated. The integrator's output voltage is then converted into a single-bit digital output (1 or 0) by the comparator. This bit is

fed back into the DAC, and the process repeats, forming a closed-loop system that operates at a very high oversampling rate. The ADC generates a stream of ones and zeros, where the input signal value is proportional to the density of ones in the output. This bit stream is then digitally filtered and decimated to produce a binary format output [50–54].

A key advantage of the Sigma-Delta architecture is its ability to perform noise shaping, a process that effectively shifts much of the low-frequency noise to higher frequencies, keeping it out of the band of interest. Figure 2.19 illustrates the principle of the noise-shaping in the oversampled ADC. This feature has made the Sigma-Delta architecture widely used in designing high-resolution ADCs for precision measurement applications with low bandwidth requirements [55–58]. Additionally, due to the high oversampling rate at which the input is sampled, the Sigma-Delta architecture reduces the need for external anti-alias filtering [59].

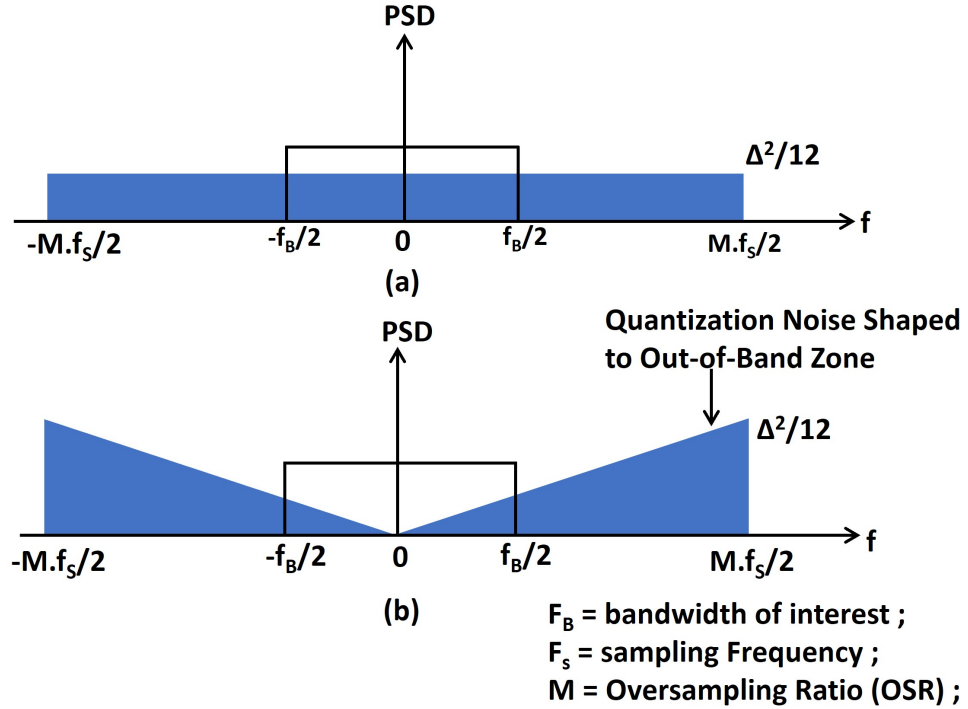


Figure 2.19: Illustration of noise shaping oversampled ADC concept.

Sigma-Delta ADCs exhibit the highest latency among various ADC architectures, primarily due to the decimation filter used to average the output bit stream [24]. These latency issues render Sigma-Delta converters unsuitable for many event-triggered IoT applications that prioritise minimising information loss for critical events, such as in healthcare monitoring.

Time-interleaving: Time-interleaving is a technique and not a properly defined analog-to-digital conversion architecture. Originally, time-interleaving [24] was adopted as an effective method to increase the speed of analog-to-digital converters

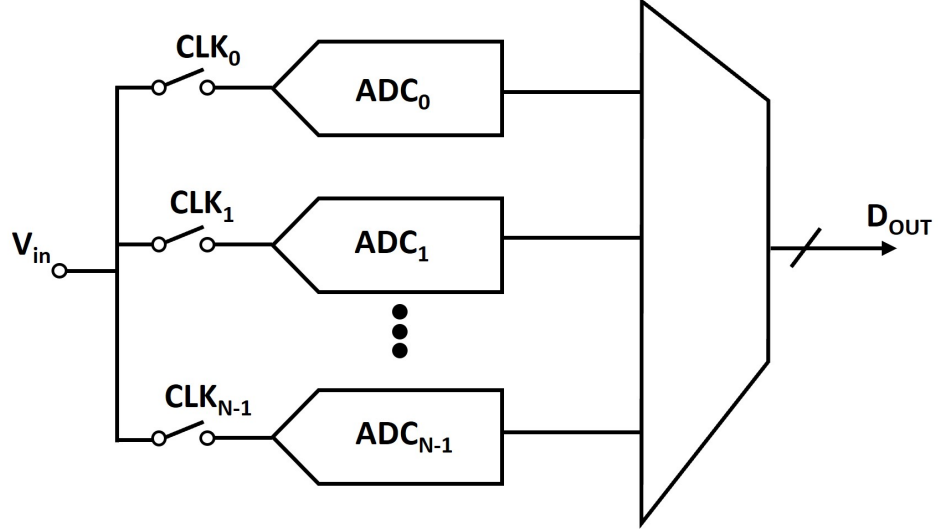


Figure 2.20: Time-Interleaved ADC

despite its associated area and power penalties [60, 61]. However, it has emerged as a viable solution for balancing power and speed trade-offs, addressing various issues even when speed is not the primary limitation. The fundamental operational concept is depicted in Figure 2.20. As the speed of a single-channel ADC approaches technological limits, the power-speed trade-off becomes non-linear, demanding disproportionately higher power for incremental speed gains. Time-interleaving mitigates this trade-off, facilitating higher conversion speeds [62–66].

Time interleaving [67] is a method that enables the utilisation of multiple identical analog-to-digital converters (ADCs) to process regular sampled data sequences at a faster rate than the operating sample rate of each individual data converter [68, 69]. In simple terms, time interleaving involves time multiplexing a parallel array of N identical ADCs to achieve a higher net sample rate f_s , even though each ADC in the array samples (and converts) at a lower rate of f_s/N [22]. For instance, by interleaving four 10-bit/50 MSPS ADCs, one could theoretically achieve a performance equivalent to a single 10-bit/200 MSPS ADC.

The significant limitations of interleaved ADCs include offset and gain mismatch between channels. These sources of error, which are negligible in high-speed single-converter applications, become important in interleaved architectures, as they are converted into dynamic errors during system operation.

Other considerations such as area and power consumption also increase in proportion to the number of ADCs employed, thereby placing a practical constraint on the total number of ADCs in the system.

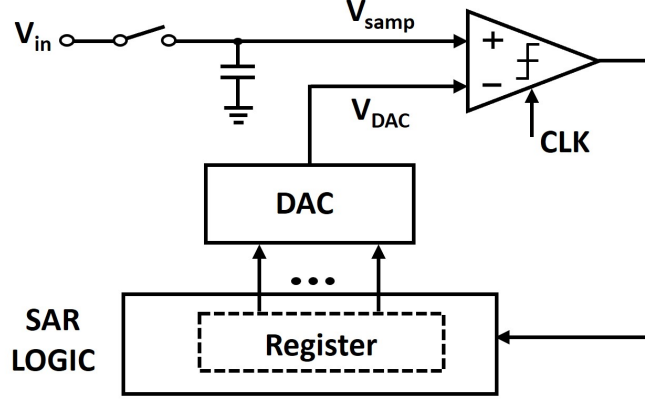


Figure 2.21: SAR ADC block diagram.

2.6.4 Successive approximation Register ADCs

The SAR ADC is one of the most energy-efficient ADCs for low-to-medium resolution applications, leveraging both technology scaling and circuit techniques ([23, 70–75]). A SAR ADC mainly consists of three blocks: the comparator, the SAR logic and the DAC as shown in Figure 2.21. While a flash converter uses many comparators to convert in a single cycle; a SAR converter uses a single comparator over many cycles to make its conversion. The power consumption of the SAR logic benefits directly from technology scaling, while reducing the comparator, and DAC power consumption relies on various innovative techniques.

As the name suggests, the SAR ADC operates on a binary search algorithm. Consequently, although the internal circuitry may operate at several MHz, the ADC sample rate is a fraction of this value because of the successive-approximation algorithm. SAR ADCs can process signals within the full Nyquist bandwidth for a given clock rate. The output data at the end of conversion is a direct representation of the sampled analog signal and can be directly used without any further manipulation or averaging.

2.6.5 Binary search algorithm

A SAR ADC employs a binary search algorithm to identify the digital code that most accurately corresponds to the analog input [76]. This algorithm requires exactly N steps to find the N -bit digital code. Consider a 3-bit ADC as illustrated in Figure 2.22. An analog input voltage (V_{in}) is converted into an output code within a full-scale signal range of -1 to +1 V. In the first step, the unknown voltage V_{in} is compared with a reference voltage (V_{ref}) that is initially set to the midpoint of the range (0 V in this case). If V_{in} is less than V_{ref} , as depicted in the figure, the first bit is resolved to zero. The reference is then shifted to the midpoint of the remaining search range. Given that V_{in} must lie between -1 V and 0 V, the new reference level is

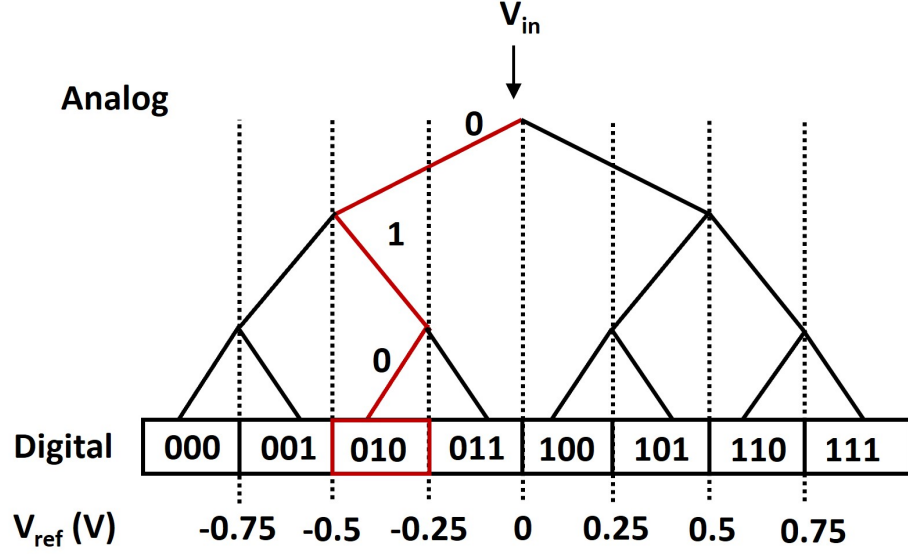


Figure 2.22: A binary search tree of a 3-bit SAR ADC.

set to -0.5 V. In the subsequent cycle, if V_{in} is greater than V_{ref} , the second resolved bit is set to 1. Consequently, the reference voltage is updated to -0.25 V. A final comparison determines the third bit, which is 0, resulting in the final digital code of 010.

2.7 ADC Figures of Merit and their trends with bandwidth and resolution

Over the last 40 years, the energy efficiency of analog to digital converters has shown steady improvement, with the most efficient ADCs achieving nearly six orders of magnitude better efficiency compared to earlier models. The highest figure-of-merit (FoM) [77] is typically attained by a specific type of ADC, characterised by certain resolution and speed limitations. However, the range of applications where these top-performing ADCs are used has expanded. To evaluate the performance of ADCs across various resolution, energy consumption, speed, and input bandwidth scenarios, the two commonly used FoMs are the Walden figure-of-merit (FoM_W), and the Schreier figure-of-merit (FoM_S) [77].

2.7.1 Walden FoM

The FoM_w generally favours low-resolution designs. The FoM_w is given by Equation 2.18:

$$FoM_W = \frac{P}{2^{ENOB} \cdot F_s}, \quad (2.18)$$

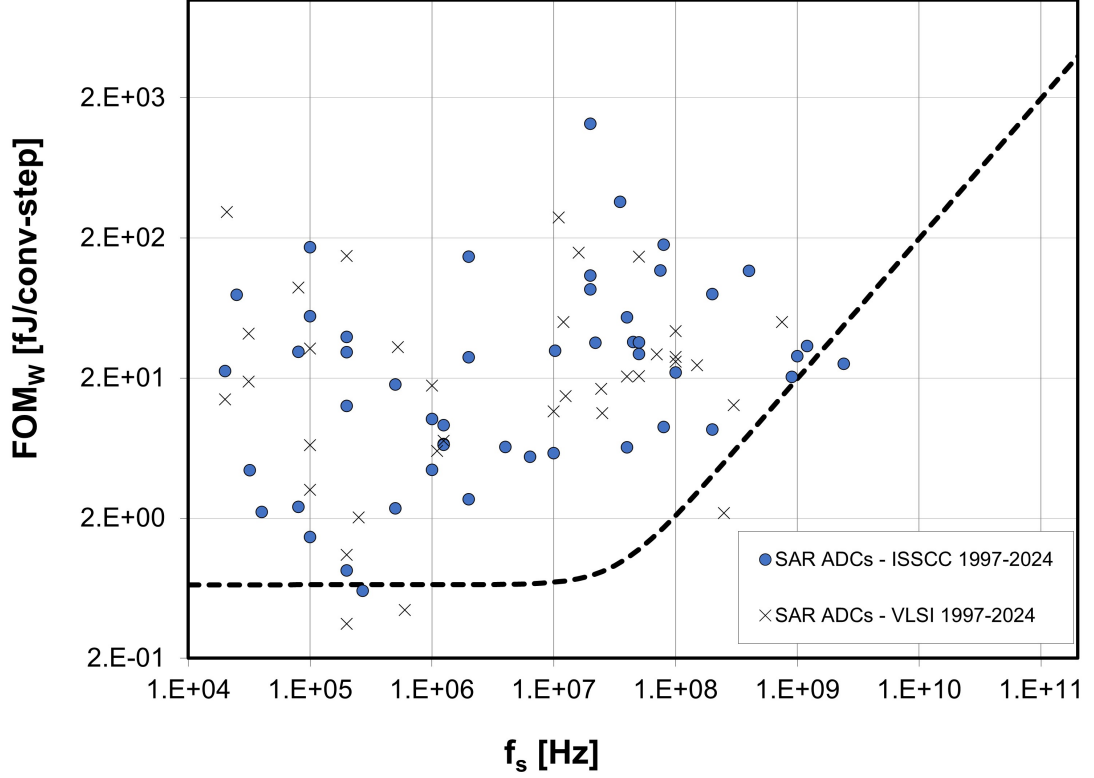


Figure 2.23: Walden FoM for recent SAR ADC publications [77]. The dashed line indicates the benchmark for performance of the State-of-the-Art ADCs.

where P is the power consumption, $ENOB$ is the effective number of bits, and F_s is the sampling frequency. During the last decade or so, the Walden Figure of Merit has shown a tremendous decrease, especially for the SAR ADCs. Figure 2.23 illustrates the relationship between the FoM_W and the sampling frequency for state-of-the-art SAR ADCs. A lower value indicates better FoM performance. Over the years, research on low-power SAR converters has primarily aimed at reducing supply power consumption by improving DAC switching efficiency, designing low-noise dynamic comparators, and optimising control logic. These techniques have reduced the FoM_W , the most common benchmark for low-to-moderate-resolution ADCs.

FoM_W was formulated with the assumption that the power scales proportionally to both the effective number of bits [ENOB] and the sampling frequency. This assumption is particularly suitable for ADCs limited by quantization noise. However, in high resolution ADCs of 10 bits or more, resolution is primarily constrained by thermal noise, represented by $\sqrt{\frac{kT}{C}}$. To improve the resolution by 1-bit, the capacitance (C) must increase fourfold. This is true for architectures like Flash ADCs and medium resolution SAR ADCs that gain advantages from voltage scaling and are constrained by hardware limitations (such as the number of comparators)

or quantization levels with a specified voltage range.

2.7.2 Schreier FoM

With a fixed sampling frequency, doubling the resolution requires quadrupling the power consumption. This implies that improving the resolution by 1-bit automatically worsens the FoM by a factor of two. Therefore, for ADCs constrained by thermal noise, the FoM_S is used and is described by Equation 2.19:

$$FoM_S = SNDR_{dB} + 10 \log \frac{BW}{P}, [77] \quad (2.19)$$

where $SNDR$ is the Signal-to-Noise-and-Distortion-Ratio in dB, BW is the Nyquist Bandwidth of the ADC and P is the power consumption. Figure 2.24 illustrates the relationship between the FoM_S and the frequency for state-of-the-art SAR ADCs. It can be seen that it is relatively easier to achieve good FoMs, but as frequency increases beyond a corner frequency, the efficiency deteriorates. The slope of the fit line shows approximately 10 dB per decade drop, and corresponds to power increasing quadratically with speed.

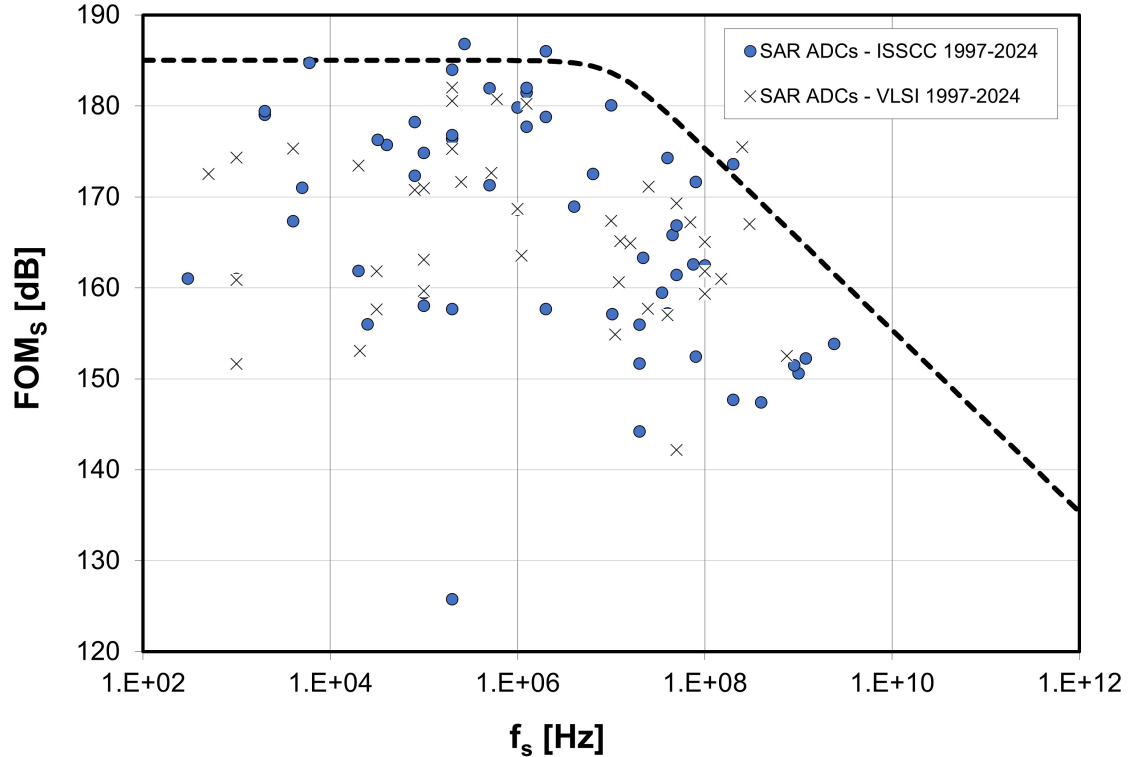


Figure 2.24: Schreier FoM for recent SAR ADC publications [77] The dashed line represents the best performance trend of the State-of-the-Art ADCs

2.7.3 Summary

This chapter provided an overview of the fundamentals of the ADCs, the basics of sampling and quantization, the important dynamic and static performance metrics of ADCs and the classification of ADCs. Having introduced the most common types of ADC and their most important FoM, the SAR ADC was chosen as the architectural choice mainly due to its power efficiency for medium-resolution ADCs.

Chapter 3 will provide a more in-depth analysis of the SAR ADC and discusses the main considerations to achieve a low-power design, which is the architecture choice for this research.

Chapter 3

Successive Approximation Register ADC

This chapter provides a complete overview of the SAR ADC that is chosen for this work. The chapter then covers various DAC switching schemes, state-of-the-art low-power comparators, and sampling methods. It concludes by highlighting efficient SAR logic implementation.

3.1 Introduction

SAR ADCs have a long history [24, 73–76, 78–83]. They have gained prominence due to the benefits of process scaling and the emergence of new architectural innovations. These developments have led to enhancements in power efficiency and conversion speed. SAR ADCs excel in power efficiency when compared to other architecture [77], particularly for medium accuracy levels from 40 to 70 dB of SNDR. One of the factors contributing to the success of SAR ADCs is their use of simple analog and digital circuits, which scale effectively and take advantage of recent process technologies. Furthermore, their uncomplicated structure often enables operation at lower supply voltages, resulting in additional power savings.

3.2 Successive approximation Register operation

3.2.1 Charge Redistribution Conversion

The SAR ADC architecture is appreciated for its three main characteristics: its potential to achieve higher resolutions, the absence of operational amplifiers, and the ability to operate with zero static power dissipation. In addition, the comparator offset does not introduce any distortion, but simply shifts the overall characteristic.

SAR ADCs commonly utilise capacitor-based DACs. This is because DAC capacitors have the ability to sample the input voltage before conversion starts. This is often referred to as charge redistribution [76]. An additional benefit of these types of DACs is that they do not consume any static power because it only requires power during switching events and do not have any direct current path.

A SAR ADC architecture with charge redistribution DAC [71] for a 4-bit operation is shown in Figure 3.1. The initial state of the shift register is zero, and the bottom plates of all capacitors are set to V_{ref} . The DAC consists of binary weighted capacitors C to $8C$. During the acquisition phase, the bottom plates of all the capacitors are connected to V_{in} , while their top plates are set to zero. Subsequently, the bottom plate of $8C$ shifts to V_{ref} , while the others go to the ground. The comparator is subsequently clocked and makes a decision that results in one of two possible outcomes. If $V_{in}/2 > V_{ref}$ the subsequent residue is required to take on a value of $3V_{ref}/4 - V_{in}$, which is achieved by shifting the bottom plate of $4C$ to V_{ref} . This means that the next most significant bit (MSB) in the register is set to 1. If $V_{in}/2 < V_{ref}$, a new residue equal to $V_{ref}/4 - V_{in}$ must be created by setting

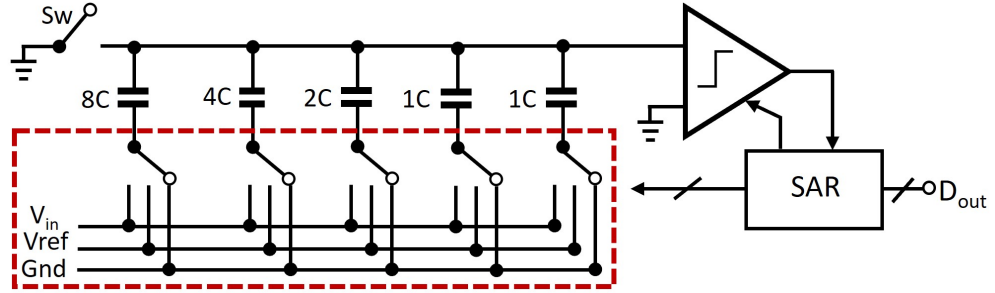


Figure 3.1: Charge Redistribution SAR ADC.

the first MSB to zero and the next to one. The conversion process continues until the residue falls below 1 LSB.

Figure 3.2 shows an example of a 4-bit conversion. The y-axis represents the DAC output voltage. In the given example, V_{in} is less than V_{DAC} . As a result, bit 3 is set to 0. The DAC is then set to 0100 for the second comparison. Since V_{in} is greater than V_{DAC} , bit 2 remains at 1. The DAC is then set to 0110 for the third comparison. Bit 1 is set to 0, and the DAC is then set to 0101 for the final comparison. In the end, bit 0 stays at 1 because V_{in} is greater than V_{DAC} .

3.2.2 Synchronous logic

In a conventional SAR ADC, the successive approximation logic operates based on a synchronous clock to define the clock period (T_s) for each phase of the conversion process [84]. In a synchronous architecture, all clock periods are equal and must

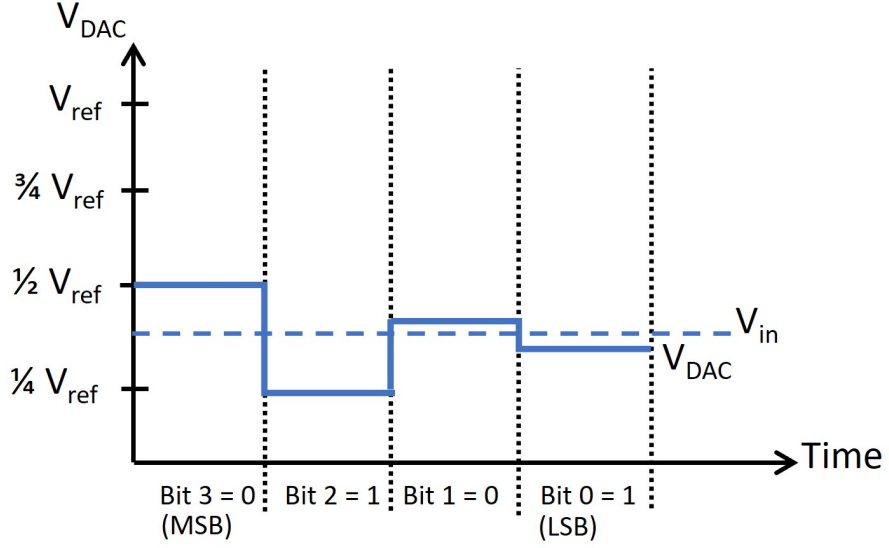


Figure 3.2: SAR operation (4-bit ADC example).

accommodate both the worst-case MSB settling time in the DAC array and the worst-case comparison time for an LSB decision. Each period is uniform in length. For instance, in an N -bit converter with a conversion rate of F_s , a synchronous approach necessitates a clock frequency of at least $(N + 1) \cdot F_s$. Consequently, even if the comparator reaches a decision within a fraction of T_s during a bit trial, the state machine must still wait for the entire period, T_s , before proceeding to the next bit trial [85]. This is because every clock cycle must accommodate the worst-case comparison time, which involves the maximum DAC settling time and the maximum comparator decision time based on the minimum resolvable input level.

3.2.3 Asynchronous logic

Asynchronous operation is preferred for event-triggered IoT applications, where the ADC needs to perform conversions only in short bursts in response to external events and can then enter a low-power sleep mode after completing the conversion [85]. In asynchronous successive approximation logic, the internal control logic generates the necessary clock cycles for the SAR conversion phase using handshaking signals from the comparator output [86]. The duration of each conversion phase varies. Once the comparator reaches a decision, the state machine immediately proceeds to the next bit trial. Consequently, each bit decision time doesn't need to account for the worst-case decision time. This allows the conversion speed of an asynchronous SAR ADC to potentially double compared to a synchronous design, without impacting the power consumption of any analog blocks in the design [87]. Moreover, asynchronous designs generally consume less power than synchronous ones because they do not require an internal high-speed clock [88]. Additionally, asynchronous de-

signs reduce the required logic complexity, leading to lower digital power consumption compared to conventional synchronous implementations [72]. Consequently, asynchronous digital logic architectures often achieve better FoM than equivalent synchronous architectures.

Metastability is an error phenomenon whose characteristics are difficult to predict, as it depends on both the applied input and circuit implementations. The resulting impairment is typically not quantified in terms of signal-to-noise ratio in data converters because the rate of its occurrence is relatively low. Instead, the error is characterised as a probability error.

In a synchronous architecture [84], each bit cycle is allocated an individual timing margin to handle metastability. If the comparator input happens to be large during some bit cycle, its time margin is wasted. In the asynchronous architecture [86], a shared timing margin is allocated across all bit cycles. This approach prevents wasted timing margins and allows more time for the hard decision when needed.

Compared to the synchronous architecture, the asynchronous counterpart significantly improves metastability performance for the same conversion time and total fixed delay.

3.3 Energy efficient DAC switching schemes

DAC switching significantly contributes to power consumption in SAR ADCs, often limiting their energy efficiency. The size of the DAC capacitor, determined by the sampling noise requirement, leads to substantial power usage due to DAC switching. This Section provides an overview of efficient DAC switching aimed at reducing energy consumption in SAR ADCs.

3.3.1 Conventional switching

The conventional differential charge-redistribution DAC switching algorithm [73] used in a 3-bit differential ADC architecture, shown in Figure 3.3, is less susceptible to power supply and substrate noise and has better common-mode noise rejection compared to its single-ended counterpart [76].

During the sampling phase, the bottom plates of each half of the differential DAC capacitors are sampled to the differential input signal, while the top plates are reset to the common-mode voltage, V_{cm} . At the end of sampling, the switches connected to common-mode voltage and the input signal are turned off, and the bottom plate of the MSB capacitor in the DAC array is switched to V_{ref} , while the bottom plates of all other bit capacitors are switched to ground. The top plates, V_{DACP} and V_{DACN} , are then compared.

If $V_{DACP} > V_{DACN}$, the bottom plates of the capacitors $4C$ (MSB) and $2C$ (MSB-1) for the positive half of the differential DAC are switched to ground and V_{ref} , respectively, causing a downward shift of $V_{ref}/4$ at the corresponding top plate. Simultaneously, the bottom plate of the MSB-1 capacitor in the negative half of the differential DAC is switched to V_{ref} , resulting in an upward shift of $V_{ref}/4$ at its top plate. If $V_{DACP} < V_{DACN}$, the switching of the bottom plates in the differential DAC is complementary. V_{DACP} and V_{DACN} are compared again, and this cycle repeats until the LSB decision is made. At the end of the SAR conversion cycle, V_{DACP} and V_{DACN} are within an LSB voltage difference from V_{cm} . This conventional switching mechanism is energy inefficient because each bit capacitor must be charged to V_{ref} .

In addition, 50% of codes need preset-evaluate-reset switching operations, which consume significant additional energy. While bottom-plate sampling is utilised in [73], the top-plate sampling method has a similar energy consumption. Although top-plate switching reduces the energy needed for MSB reconfiguration, it consumes reset power.

The average switching energy of an N - bit conventional switching algorithm is given by :

$$E_{conventional} = \sum_{i=1}^N 2^{N+1-2i} (2^i - 1) C V_{ref}^2, \quad (3.1)$$

where N is the number of bits, C is the total capacitance and V_{ref} is the reference voltage.

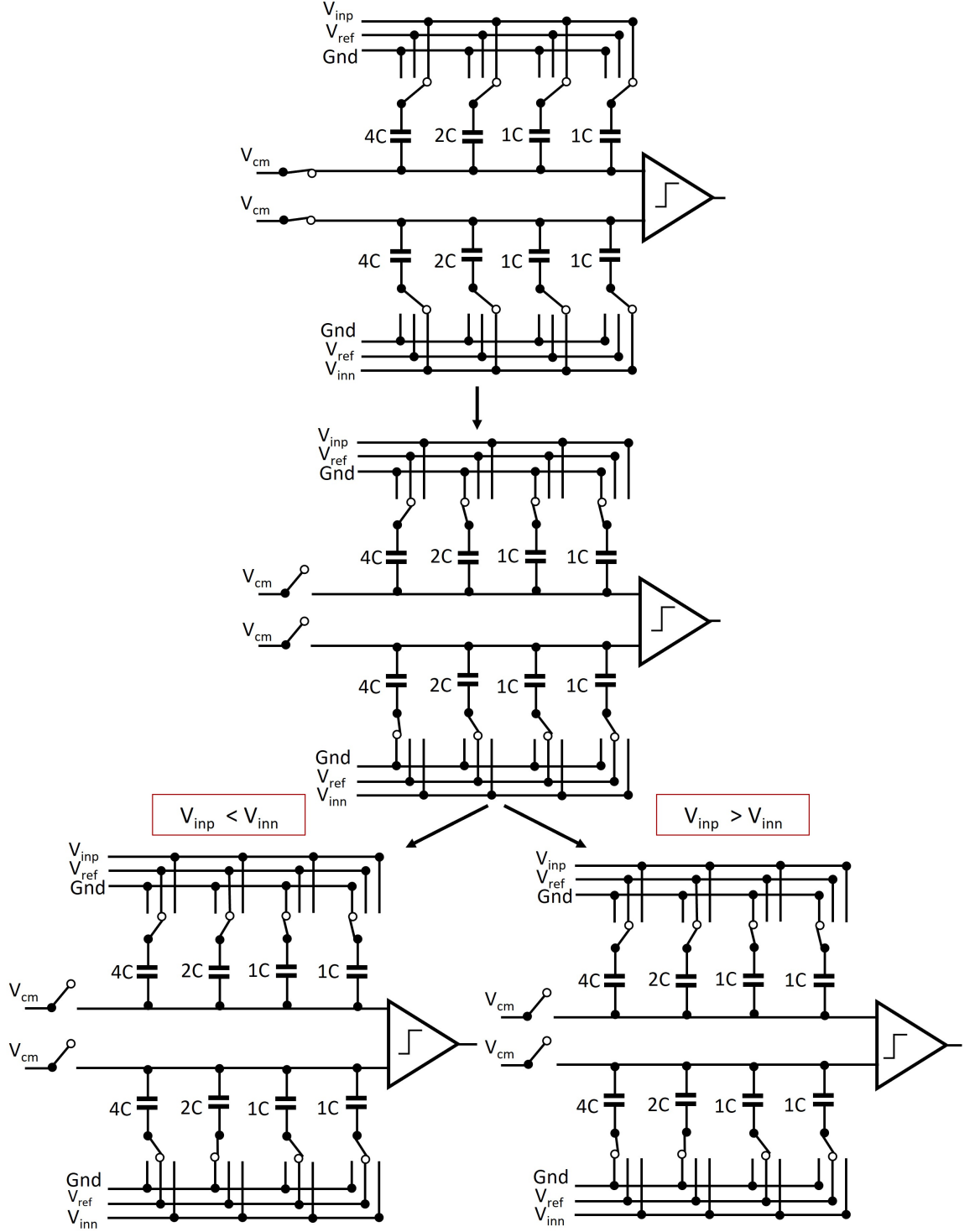


Figure 3.3: 3-bit example of conventional switching algorithm

3.3.2 Monotonic switching

To overcome the limitations of the conventional switching mentioned in Section 3.3.1 [80] reported the monotonic switching technique. A 3-bit example of a monotonic switching algorithm is shown in Figure 3.4. The top-plate sampling technique is

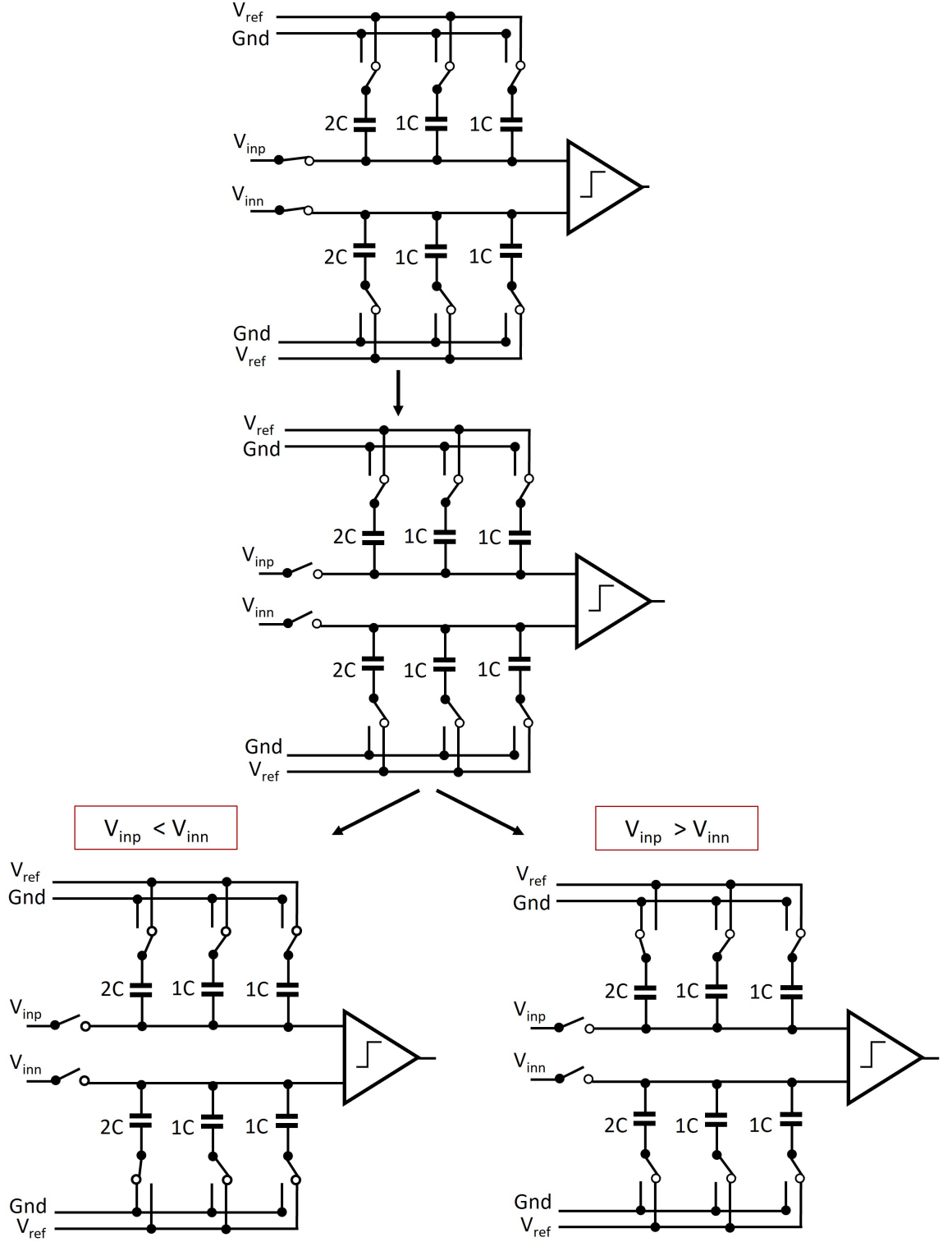


Figure 3.4: 3-bit example of monotonic switching algorithm

implemented, where the DAC bottom plates are reset to V_{ref} . This approach eliminates the power consumption associated with MSB reconfiguration and resetting. Additionally, each reconfiguration requires only single-sided capacitor switching, removing the need for the preset-evaluate-reset process. This algorithm de-

creases the DAC array size by half, if the DAC sample capacitor value is not limited by kT/C noise. This is because the input signal is sampled on the top plate, enabling the MSB comparison immediately after sampling without requiring any bit switching [22],[80]. This algorithm improves energy efficiency through two primary mechanisms. Initially, it determines the MSB bit by directly comparing V_{inp} and V_{inn} , eliminating the need to switch any capacitors, thus conserving energy. This method effectively increases resolution by 1-bit for the same total capacitance, since the MSB bit determination does not involve capacitor switching. Secondly, it avoids operations that necessitate discharging a capacitor charged in one bit trial for a subsequent bit trial, further optimising energy usage.

The monotonic switching algorithm achieves an energy reduction of 81.3% compared to the conventional switching algorithm, all without the need for additional switches or capacitors. The average switching energy of an N-bit monotonic switching algorithm is given by:

$$E_{monotonic} = \sum_{i=1}^{N-1} 2^{N-2-i} C V_{ref}^2. \quad (3.2)$$

However, all capacitors can only switch from V_{refp} to ground, leading to a monotonically decreasing DAC output common-mode voltage that falls from V_{cm} to ground. This reduction limits the linearity of the SAR conversion [89], as it causes significant performance variations in the comparator, including noise, offset, and speed issues.

3.3.3 Tri-level switching algorithm

A tri-level switching scheme for a SAR is proposed in [90]. In this scheme, the input is sampled onto the top plates of the positive and negative capacitor arrays, as illustrated in Figure 3.5. Similar to the monotonic switching scheme, the tri-level switching approach inherently provides one additional bit of resolution compared to the conventional schemes.

The MSB comparison can be performed immediately without the need for additional capacitor switching, thus consuming no extra energy. A third reference voltage, V_{cm} is also used. During sampling and the MSB bit trial, the bottom plate of each capacitor is connected to V_{cm} . After a bit decision is made, the bottom plate of the relevant capacitor is switched to V_{refp} or ground and remains there, avoiding the need to discharge the capacitor, which saves energy.

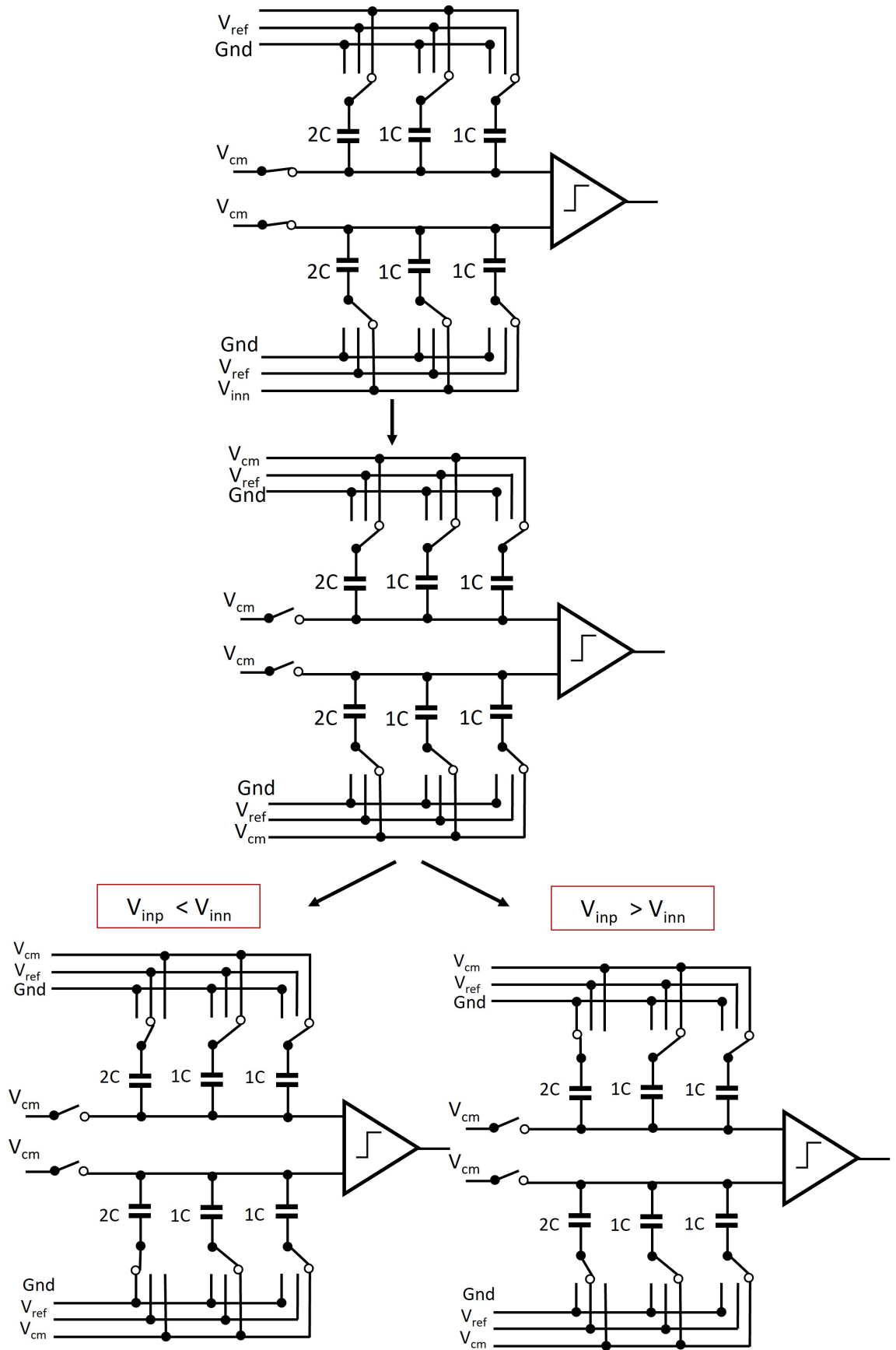


Figure 3.5: 3-bit example of Tri-level switching algorithm

The tri-level switching scheme boasts even higher efficiency than the monotonic switching scheme, consuming 87.5% less energy compared to the conventional method. The average switching energy is given by:

$$E_{Tri-level} = \sum_{i=1}^{N-1} 2^{N-3-2i} C V_{ref}^2. \quad (3.3)$$

The common-mode voltage of the CDAC remains constant throughout the conversion process, which simplifies the comparator design and enhances the ADCs linearity. However, the tri-level scheme has a drawback: the voltage on the top plate does not start and return to the same level during the conversion process, due to the input being sampled on the top plate of the CDAC array. Consequently, the top plate and comparator input become susceptible to parasitic capacitors at that node, impacting the ADC's linearity.

3.3.4 Split-Capacitor switching

In [91], a split-capacitor switching scheme is proposed where the MSB capacitor is divided into a binary weighted sub-capacitor array. The total capacitance of this MSB array remains unchanged. A 3-bit example of the split-capacitor switching scheme is shown in Figure 3.6, illustrating that the original MSB capacitor is split into binary weighted sub-capacitors (2C,C,C).

In the split-capacitor switching algorithm [91],[92] the MSB capacitor of an N-bit DAC array is divided into an N-1 bit sub-capacitor array, with each sub capacitor switchable individually. As in conventional sampling, the bottom plates of each half of the differential DAC sample the differential inputs, and the top plates are reset to V_{cm} . However, at the start of the conversion phase, before the MSB comparison, the bottom plates of all sub-capacitors comprising the MSB are switched to V_{ref} on both sides of the differential DAC.

If $V_{DACP} > V_{DACN}$, the downward transition of $V_{ref}/4$ on the top plate of the positive half of the DAC is achieved by switching the bottom plate of its largest sub-capacitor in the MSB array to ground. This contrasts with conventional switching, where the bottom plate of the entire MSB capacitor is discharged to the ground, and the MSB-1 capacitor is charged to V_{ref} . For an upward transition of $V_{ref}/4$ on V_{DACN} , the bottom plate of the MSB-1 capacitor in the negative half of the differential DAC is switched to V_{ref} . If $V_{DACP} < V_{DACN}$, the switching action is complementary. For a full-scale sinusoidal input signal, the split-capacitor mechanism reduces the DAC switching energy by 37% compared to the conventional method. The average switching energy of an N-bit split-capacitor switching scheme

is given by:

$$E_{split-capacitor} = 2^{N-1} \sum_{i=2}^N 2^{N+1-2i} (2^{i-1} - 1) C V_{ref}^2. \quad (3.4)$$

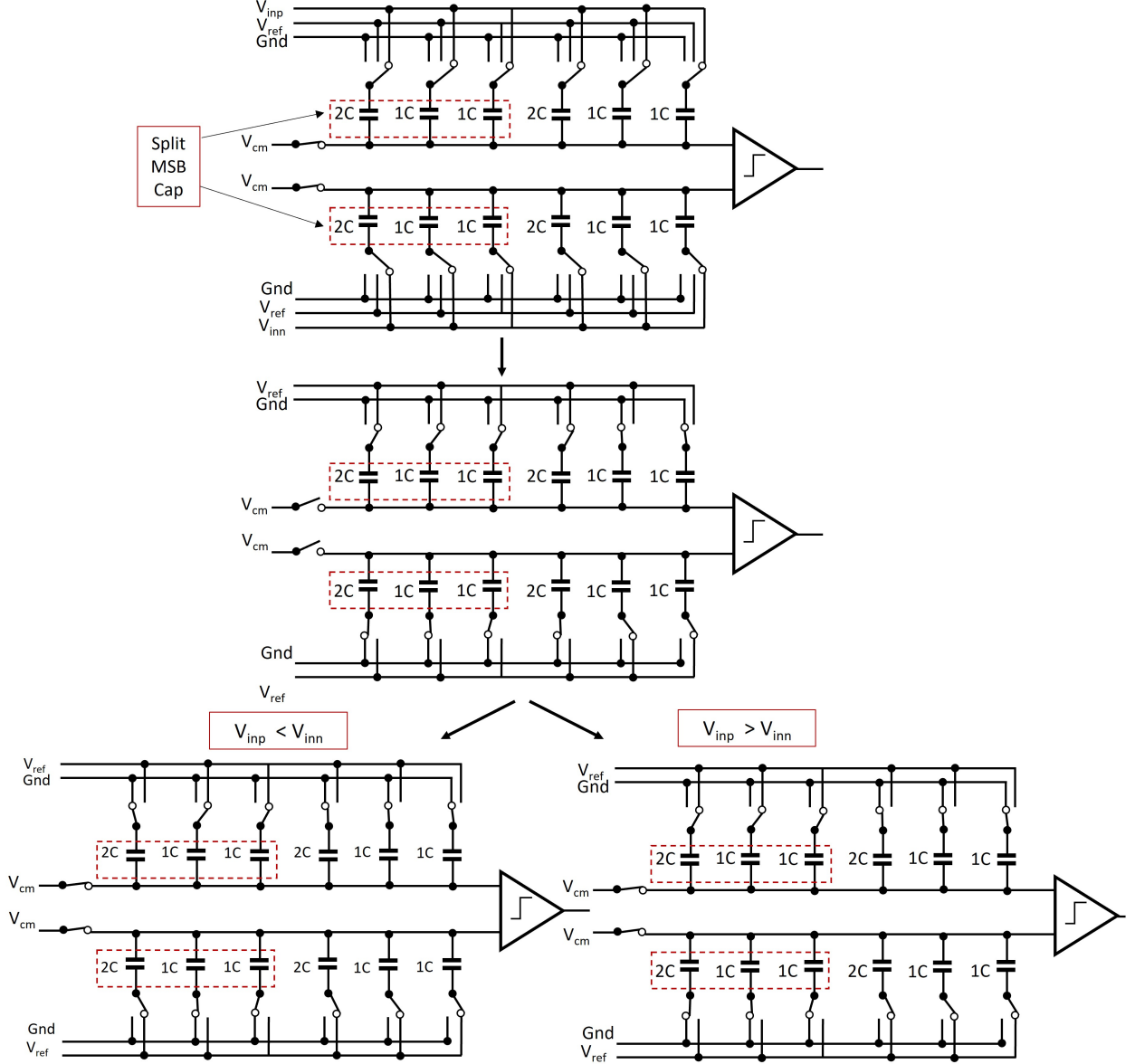


Figure 3.6: 3-bit example of the split-capacitor switching algorithm

In the V_{cm} -based switching technique [73], during the sampling phase, the bottom plates of the DAC are reset to V_{cm} , eliminating the reset power. During the SAR operation, the DAC is switched differentially to maintain a constant common-mode voltage. This approach achieves a 75% power reduction compared to the conventional design, at the expense of an additional reference voltage V_{cm} and increased switch driving power.

Although several other switching schemes exist, such as the bidirectional single

Architecture	Conversion energy (CV^2) (J)	Reset energy (CV^2) (J)	Normalised total energy (J)	Number of unit capacitors
Conventional	682.65	0	1	2^{N+1}
Monotonic	255.5	0	0.37	2^N
V_{cm} -based	170.2	0	0.25	2^N
Split-capacitor	170.2	255.5	0.63	2^{N+1}

Table 3.1: Average switching energy of a 10-bit SAR ADC (The energy is expressed as a multiple of (CV^2)).

side switching scheme [93], the charge-average switching technique [94], the Integral non linearity splitting switching [95], and the detect and skip scheme [96], the V_{cm} -based and split-capacitor based switching schemes are preferred. These methods strike a favourable balance between energy efficiency, implementation simplicity, and effective common-mode control. Table 3.1 above compares the average conversion energy, the reset energy, and the total required unit capacitor elements for the different schemes.

3.4 Prior Art - Dynamic comparators

The comparator is the essential circuit block that converts the difference between the input signal and the analog DAC voltage into a digital decision. The comparator plays an important role in determining the performance of SAR ADCs. It generally includes a preamplifier to amplify the input signal and to provide initial gain, followed by a regenerative latch to make the final decision based on positive feedback. The preamplifier reduces offset, noise, and latch kickback (kickback noise refers to undesired voltage or current transients that occur when a comparator rapidly switches from the cut-off region to the saturation region). With adequate preamplifier gain, the comparator's noise levels are generally determined by the preamplifier itself.

Offset errors in the comparators only induce a linear shift in the transfer function, which can be corrected [22]. Importantly, these offset errors do not trigger any linearity issues, as they are independent of the input signal. Two factors contribute to the signal independence of the comparator's offset error. Firstly, in a SAR architecture, typically only one comparator is used, resulting in a constant offset during

the ADC operation. Secondly, following each conversion, the top plate voltages of the CDAC, which serve as inputs to the comparator, are reset to a known voltage. Consequently, the common-mode voltage of the comparator remains consistent across the entire input range, ensuring a constant offset.

SAR ADCs scale with both technology and supply voltage due to their highly digital architecture. However, 50% - 60% of the total energy consumption in SAR ADCs is due to the comparator, which does not scale as effectively with supply voltage and technology as the digital blocks such as logic and DAC switches [70, 71, 97]. The stringent quantization noise requirement at low voltages makes reducing the energy consumption of each comparator operation particularly challenging. The StrongArm latch depicted in Figure 3.7, has been widely used as a comparator in SAR ADCs over the past several decades. The operation of the StrongArm latch [98] can be divided into two phases: the preamplification phase and the latch regeneration phase, with the turn-on of the PMOS cross-coupled pair separating the two phases. The analyses in [98], [99] and [100] demonstrate that the preamplifier noise of the StrongArm latch can be represented as:

$$\overline{V_{n,pre}^2} \approx \frac{I_D}{g_m} \cdot \frac{4kT\gamma}{V_{thn}C_x}, \quad (3.5)$$

where V_{thn} is the threshold voltage for NMOS device, g_m is the transconductance, C_x is the integrating capacitance, and γ is the noise factor, typically equal to $2/3$. To minimise noise, the g_m/I_D ratio of the input pair can be raised by biasing it in a weak inversion, but with an upper limit of q/nkT , where n represents the sub-threshold slope factor. However, boosting the g_m/I_D ratio often leads to a decrease in speed [98]. Another effective method to decrease comparator noise is by increasing the loading capacitor, C_x . However, this directly results in higher comparator power consumption.

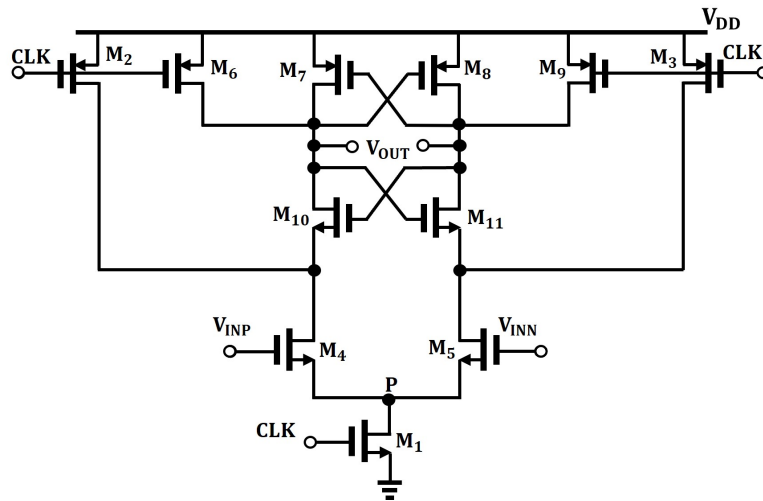


Figure 3.7: The StrongARM latch comparator [98].

The StrongArm latch is a single-stage architecture that requires voltage head-room [98]. Furthermore, since there is no isolation between the regenerative latch and the differential input stage, it suffers from significant kickback [98]. These problems are mitigated by the dual-tail comparator architecture shown in Figure 3.8 as presented in [101].

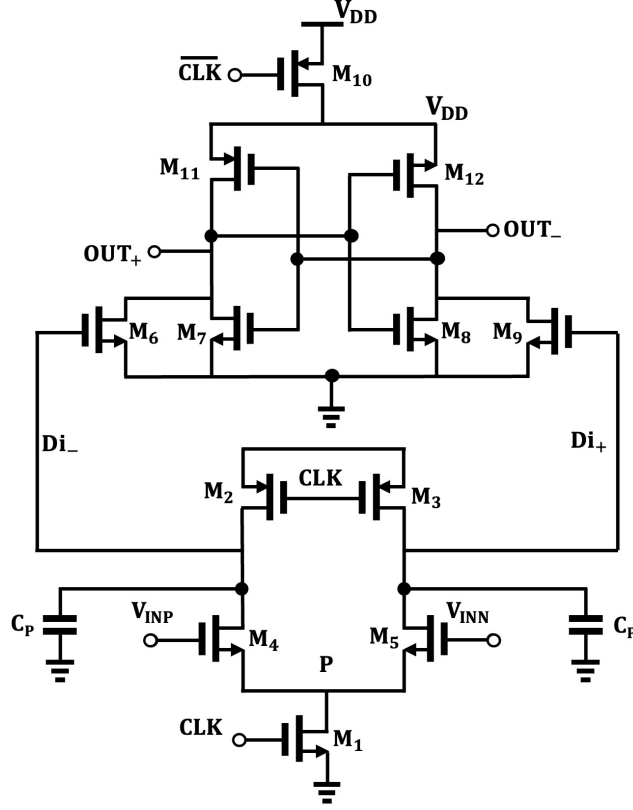


Figure 3.8: dual-tail comparator [101].

This configuration expands the input common mode range. Additionally, it provides an extra level of flexibility through separate tail transistors, one for the preamplifier and one for the latch stage. This arrangement allows independent control over the common mode current for the preamplifier and regeneration time for the latch stage. In the dual-tail comparator [101] shown in Figure 3.8, the output nodes of the preamplifier (Di_- and Di_+) discharge completely to ground at the end of the comparison phase. Consequently, the preamplifier consumes a fixed energy equivalent to $2 \cdot C_P \cdot V_{DD}^2$ for each comparator operation. Moreover, the capacitance C_P at each of the preamplifier output nodes dictates the input referred noise, so they have to be sized appropriately to achieve the desired SNR. As a result, the preamplifier typically accounts for approximately 80% of the total energy consumption of the comparator [71]. The dual-tail architecture faces challenges in efficiently managing energy consumption for a given SNR due to simultaneous operation of the preamplifier and the regenerative latch. Since both the preamplifier

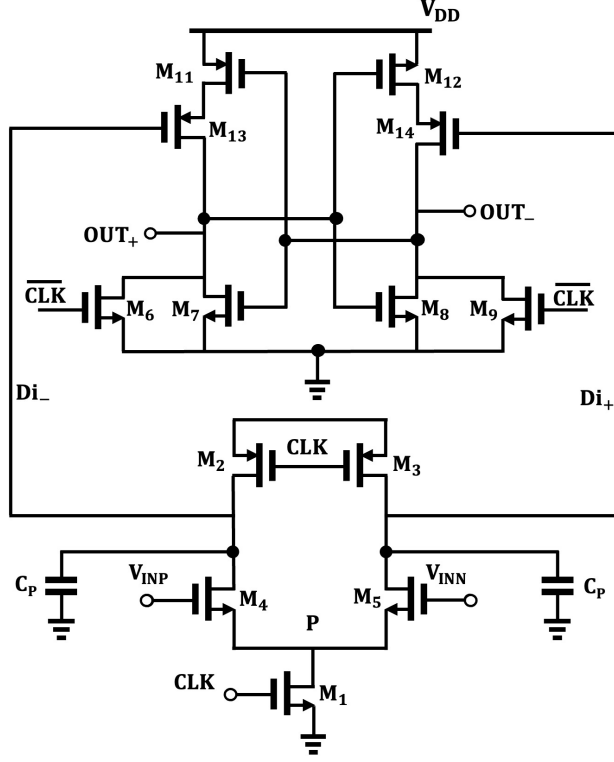


Figure 3.9: Elzakker's Comparator [71].

and the regenerative latch start operating simultaneously, the regenerative latch begins conducting when the output voltage of the preamplifier is nearly zero at the start of the comparator operation. Consequently, the latch stage operates without generating a significant SNR, making it less suitable for low-power applications like medium to high resolution SAR ADCs. Elzakker's comparator [71] shown in Figure 3.9 (above) mitigates this problem by delaying the activation of the latch stage until sufficient voltage gain is achieved across the preamplifier output nodes.

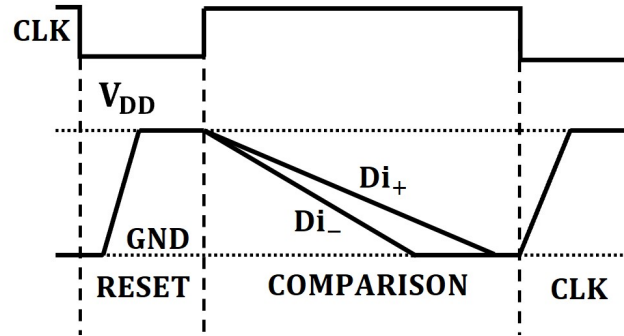


Figure 3.10: Timing waveform of the Elzakker's comparator.

The preamplifier stage is the same as that of the dual-tail comparator [101], the output nodes of the preamplifier are fed to M_{13} and M_{14} , which turns on when the output nodes of the preamplifier crosses its threshold voltage. Subsequently, the latch stage transistors start from their saturation region, leading to a higher

gain and reduced comparator noise and offset. The timing waveform of Elzakker's comparator is shown in Figure 3.10. The Elzakker's comparator consumes a fixed energy of $2 \cdot C_P \cdot V_{DD}^2$. Since a large C_P is required to reduce noise, as shown previously in Equation (3.5), the preamplifier consumes the majority of the power.

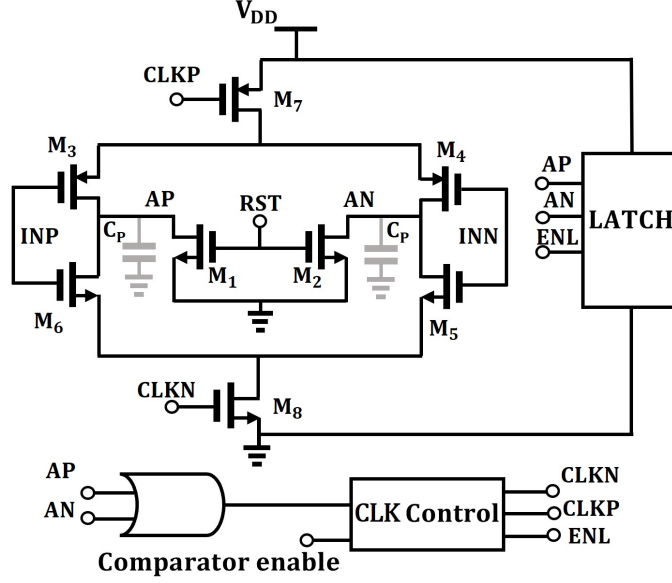


Figure 3.11: Bidirectional comparator [102].

The Bidirectional comparator [102] shown in Figure 3.11 (above) mitigates this problem by achieving higher energy efficiency by increasing the effective preamplification gain. In Elzakker's comparator [71] the preamplifier load C_P discharges completely to ground, during comparison, consuming a fixed energy of $2 \cdot C_P \cdot V_{DD}^2$. The bidirectional comparator improves the energy efficiency of the preamplifier itself. The preamplifier stage consists of NMOS and PMOS input pairs. In the initial half of the preamplifier phase, the PMOS pair turns on to charge the preamplifier loads from ground. Once the voltage crosses half of V_{DD} , the PMOS side is turned off, and the NMOS pair turns on to complete the second half of the preamplification. Consequently the preamplifier loads revert to their initial state, thereby avoiding reset power consumption. This method consumes only $C_P \cdot V_{DD}^2$ energy, where C_P is the integrating capacitance while achieving comparable gain and noise performance to conventional designs. Theoretically, it doubles the energy efficiency of the preamplifier. However, due to the additional control circuits required, the overall energy efficiency improvement of the comparator is 1.5 times that of a StrongARM latch. The Dynamic Bias comparator [103] shown in Figure 3.12 prevents the full discharge of the integration capacitors C_P and increases the g_m/I_D of the input pair, thus improving the energy efficiency. By the use of the degeneration capacitor C_{Tail} , the source voltage, V_P , is charged up, which in turn results in the reduced overdrive voltage of the input pair. First, as the source voltage, V_P , is charged up, V_{GS} of

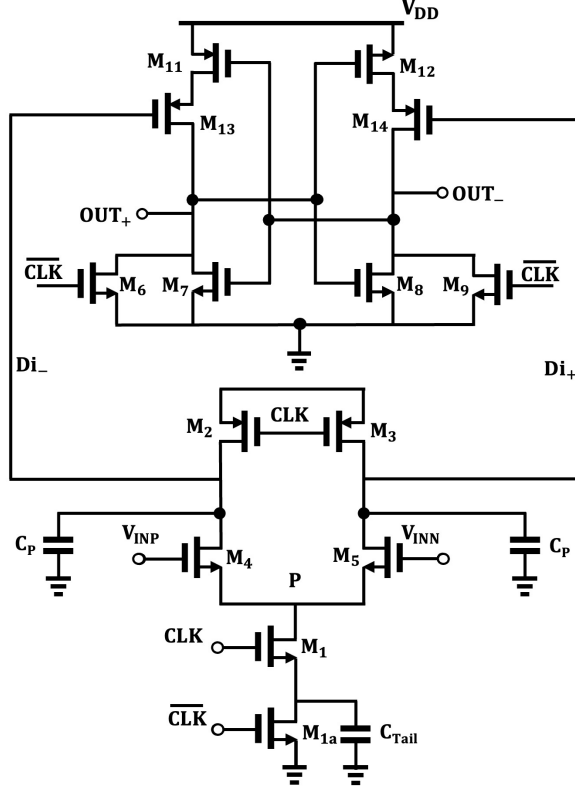


Figure 3.12: Dynamic bias comparator [103].

the input pair keeps decreasing, and eventually, the input pair is cut off, and the dynamic integration stops. This prevents the full discharge of the loading capacitors. Second, the reduced overdrive voltage results in an increased g_m/I_D during the integration time. The increase in g_m/I_D of the integrator along with the integrating capacitors effectively lowers the input-referred noise [100], [99]. The noise and offset contributed from the latch is attenuated by the integrator gain A_{int} as shown in Equation (3.6).

$$\sigma_{n(os),in} \approx \sqrt{\sigma_{n(os),int}^2 + \frac{\sigma_{n(os),latch}^2}{A_{int}^2}}, \quad (3.6)$$

where $\sigma_{n(os),int}^2$ is the offset voltage of the integrator, $\sigma_{n(os),latch}^2$ is the offset voltage of the regenerative latch and A_{int} is the integration gain.

To reduce thermal noise, a higher g_m/I_D is needed as well as a large loading capacitor. The offset and the noise contributed from the latch is attenuated by the integrator gain. The dynamic bias comparator consumes 2.8 times less energy than the dual-tail comparator.

The Floating Inverting Amplifier [104] as shown in Figure 3.13 realises current reuse which boosts the g_m/I_D , and prevents the full discharge of the integration capacitors, thus significantly improving the energy efficiency. This preamplifier provides an isolated voltage domain for the dynamic integration since it is powered by

a floating reservoir capacitor. This isolated power domain provided by the reservoir capacitor makes the amplification insensitive to the input common-mode voltage and Process, Voltage, and Temperature (PVT) variations. With only the differential input voltage sensed by the preamplifier input, it achieves input common-mode and process corner robustness without a dedicated Common-Mode Feedback Circuit (CMFB). This comparator is seven times more energy efficient than the Strong-Arm latch.

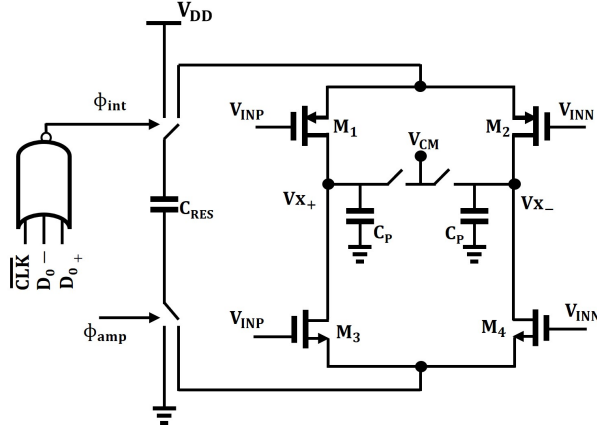


Figure 3.13: Floating-inverting amplifier [104].

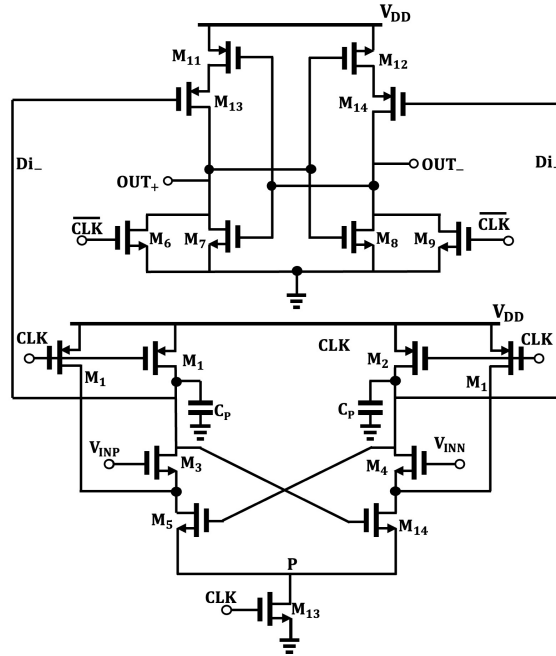


Figure 3.14: 1 V cross-coupled low-power comparator [105].

The 1 V cross-coupled low-power dynamic comparator [105] shown in Figure 3.14 uses cross-coupled devices to the input differential pair and prevents the internal nodes of the comparator from being fully discharged to ground, thereby increasing

the efficiency of the comparator. This comparator has 30% power reduction and similar noise levels compared to the conventional designs. This circuit has a lower area and does not require any external large capacitors or complex logic other than integrating capacitors C_p .

Table 3.2 summarises the comparator architectures discussed and their energy consumption equations.

Comparator Architecture	Energy consumption equation
Dual-tail	$2 \cdot C_P \cdot V_{DD}^2$
Bidirectional comparator	$C_P \cdot V_{DD}^2$
Dynamic Bias comparator	$[2 \cdot C_P \cdot V_{DD}^2 - C_P \cdot V_{DD} (V_{D1} + V_{D2})]$
Floating inverting amplifier	$2 \cdot C_P \cdot V_{DD} \cdot \Delta V_{XCM}$
1V comparator	$C_P \cdot V_{DD} \cdot (V_{D1} + V_{D2})$

Table 3.2: Summary of comparator architecture and their energy consumption equations, where V_{XCM} is the output common mode voltage, C_P is the integrating capacitance, V_{DD} is the supply voltage.

The energy efficient comparator with a Floating Inverting Amplifier based comparator achieves the best energy efficiency which represents more than 2.5-time improvement over the state of the art. This pre-amplifier is powered by a floating reservoir capacitor, which provides an isolated voltage domain for the dynamic integration and does not require any dedicated CMFB.

3.5 Circuit limitations

3.5.1 DAC mismatch and noise

When designing a DAC, key considerations include noise, speed, and mismatch [106], [107]. Noise is introduced during the track-and-hold process, compounded by additional noise from control switch on-resistance and the reference voltage. Speed is a concern due to the formation of an RC network each time a switch in the DAC is activated, leading to exponential settling of the output to the new level. The RC time constant limits the maximum operational speed, which is crucial for accurate comparisons in subsequent SAR cycles. To improve speed, options include reducing capacitor size or enlarging switches to minimise on-resistance.

Mismatch is a significant issue in DAC design, often restricting the achievable linearity in SAR ADCs [108]. Figure 3.15 illustrates the effect of mismatch on

the search tree. In this case, the capacitor that generates the voltage step has a mismatch. As a result, not only this reference but also the references of the sub-branch of this tree will be shifted with an amount equal to the error of this capacitor. Selecting the total DAC capacitance value involves a trade-off: larger values improve noise and matching performance, while smaller values are preferred for power consumption, chip area, and operational speed. Mismatch errors lead to non-linearity in the ADC output, observed as INL and DNL errors.

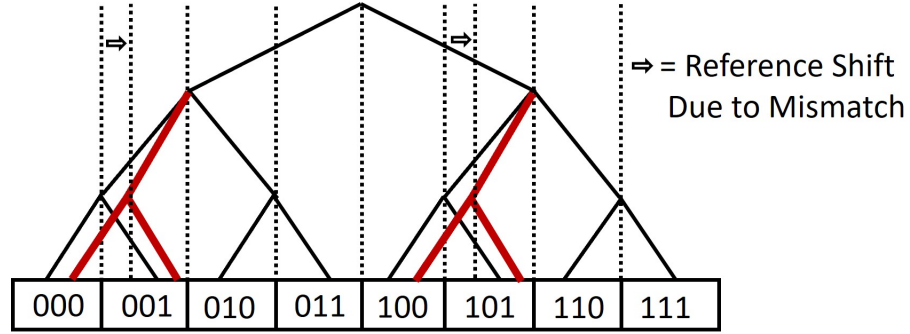


Figure 3.15: The effect of capacitor mismatch on the search tree.

3.6 Sampling

In charge redistribution SAR ADCs, bottom-plate and top-plate sampling are commonly used techniques for charge redistribution SAR ADCs. The difference between the two techniques is the connection of the sample-and-hold circuit to either the bottom plate or top plate of the capacitor array.

3.6.1 Top plate sampling

Top plate sampling involves connecting a single sampling switch to a common terminal that ties all the top plates of the capacitors together. It can make the first bit decision immediately after sampling (without redistributing any charge) which consumes less energy. An N -bit ADC requires only an $(N - 1)$ -bit DAC. Since the signal is sampled on the top plate, it will experience no attenuation toward the comparator. However, the swing on the top plate due to the reference voltage steps will be reduced by the capacitive division. This configuration is attractive for low-power and low-voltage designs because only one sampling switch is required as shown in Figure 3.16(a). However, top plate sampling has limitations. It is sensitive to top-plate parasitics and charge injection, which can impact the linearity of the ADC. Typically, it is suitable for ADCs with a resolution of 10 bits or below [109].

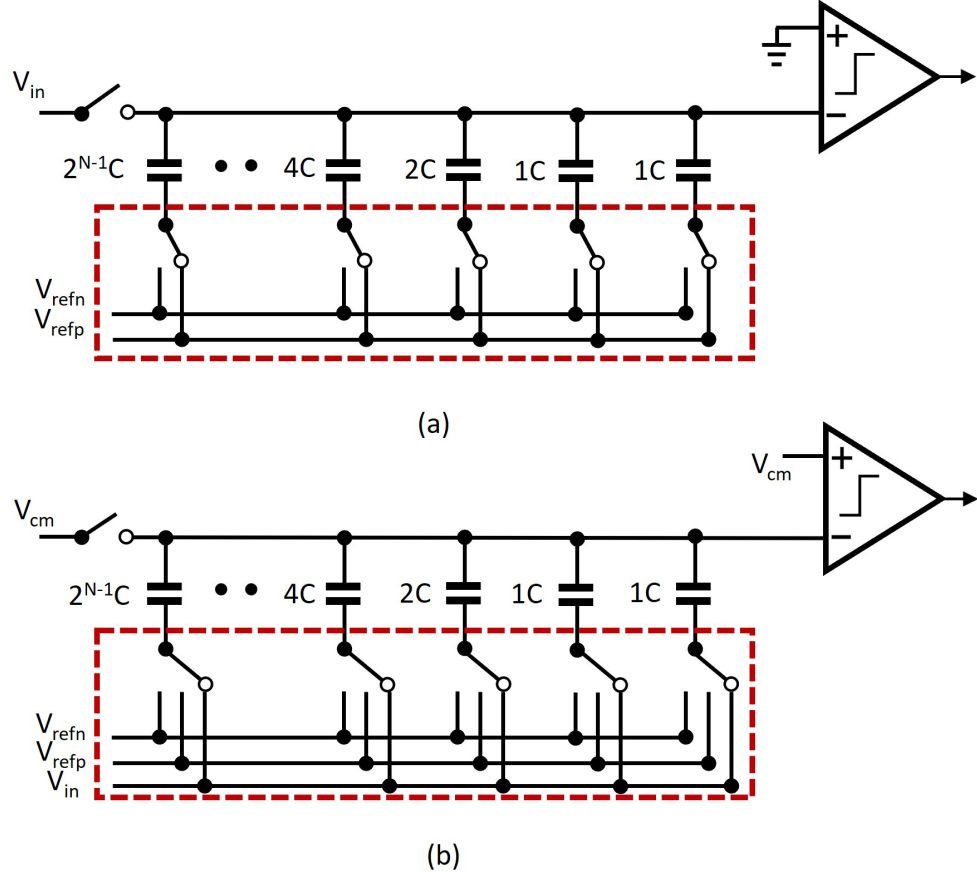


Figure 3.16: (a) Top plate sampling SAR and (b) bottom plate sampling techniques of SAR ADC.

3.6.2 Bottom plate sampling

In bottom plate sampling, the analog input is connected to the bottom plate of the capacitor array. The input signal is sampled at the grounded side of the capacitor to achieve signal independent sampling. Figure 3.16(b) illustrates this configuration, where each capacitor has a sampling switch at its bottom plate. This approach reduces the impact of charge injection, which occurs when the sampling switch is turned off, and also mitigates the effects of parasitic capacitance at the top plate of the capacitor. Bottom plate sampling is often used to achieve linearity greater than 10 bits in SAR ADCs. In addition, bottom plate sampling can also improve linearity [110].

3.7 Sampling switch

The sampling switch is a circuit that tracks the input and at some point samples the signal to perform quantization. Sampling errors cannot be corrected, even with redundancy. Consequently, the design of the sampling switch is critical to the overall

performance of the ADC.

The sampling switch can be designed using a single NMOS or PMOS transistor, or a transmission gate [111]. However, certain limitations constrain the use of single-transistor switches or complementary switches in specific designs. When using a single PMOS or NMOS transistor, the input dependence of the on-resistance (R_{on}) causes distortion in the output spectrum. Conversely, a transmission gate allows the rail-to-rail input voltage swing, and while the R_{on} dependence on V_{in} is less pronounced, it remains variable and can still induce distortion at the switch output. While a larger transmission gate may yield a nearly constant R_{on} , it introduces significant parasitics and increased power consumption. Clock boosting and bootstrapping techniques can be used to overcome this limitation. Both solutions are shown in Figure 3.17 and 3.18 respectively. For illustration, an NMOS switch is used. In order to facilitate rail-to-rail operation, the gate at the high level is not connected to the supply voltage but to a level beyond the supply voltage so that rail to rail operation is obtained.

3.7.1 Bootstrap circuit

The bootstrapping principle is shown in Figure 3.17. In a bootstrapping circuit [112], the gate source voltage is shifted by an amount of V_{DD} beyond the input signal to the amount equal to $V_{DD} + V_{in}$. In this way, the gate source voltage V_{gs} when turned on is always equal to V_{DD} , resulting in a constant gate overdrive that gives better linearity. Since the gate source voltage is equal to V_{DD} and never exceeds V_{DD} , it also has better reliability. The key features of the bootstrap circuit are:

- Clock (CLK) shifted to $V_{DD} + V_{IN}$
- Voltage swing : $0 \leq V_{IN} \leq V_{DD}$
- Constant overdrive, V_{ov}
- V_{gs} equal V_{DD}

3.7.2 Clock Booster circuit

The principle of clock boosting [113] is illustrated in Figure 3.18. In a clock boosting circuit, the clock is multiplied by a fixed factor, for example, by a factor of 2. The high level of the clock now becomes twice the V_{DD} . By using this approach, a rail-to-rail input swing is achieved. However, theoretically the gate source voltage V_{gs} cannot go beyond the supply voltage, which might result in reliability issues for the transistor. The main features of the clock boosting circuit are:

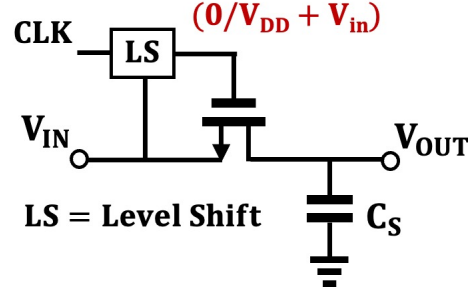


Figure 3.17: Bootstrap circuitry [112].

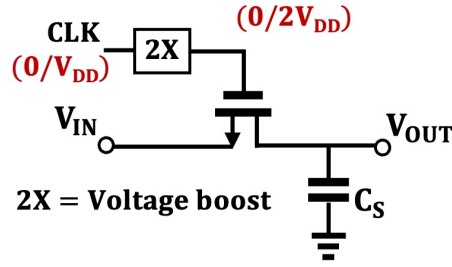


Figure 3.18: Clock booster circuitry [113].

- CLK boosted $> V_{DD}$
- Voltage swing : $0 \leq V_{IN} \leq V_{DD}$
- Larger overdrive, V_{ov}
- V_{gs} can be $> V_{DD}$

3.8 Summary

This chapter provided an overview of SAR ADCs, focusing on low-power SAR ADCs and advancements in low-power comparator designs, DAC switching schemes, circuit limitations, and sampling techniques. It has highlighted key considerations for achieving low-power SAR ADC designs and concluded with a discussion on reducing energy consumption in core components of SAR ADCs (DAC, controller, and comparator).

Chapter 4 will provide a more in-depth analysis of the design and implementation of a low-power 14-bit 500 kS/s SAR ADC. It will also introduce a switched-supply technique that can be used to achieve a low-power operation. This technique reduces power consumption while achieving a performance of 71.7 dB.

Chapter 4

A 14-bit SAR ADC using a switched-supply comparator and clock boosting circuit

4.1 Introduction

This chapter provides an in-depth discussion on the implementation of a 14-bit, low-power, 500 kS/s SAR ADC using a 65 nm CMOS process. The design and functionality of each block, including the comparator, CDAC, switches, break-before-make control, and digital logic, are thoroughly explained.

4.2 Switched-supply comparator

The strongArm latch is a single-stage comparator architecture that requires large voltage headroom, suffers from kickback noise, and shows large power consumption [101]. On the other hand, the dual-tail dynamic latch comparator is a two-stage architecture that can operate from a reduced supply voltage, has less kickback noise and shows reduced power consumption thanks to its dynamic operation, i.e. it has no static current [101, 114]. Due to its power efficiency, the dynamic comparator is often used in low-power SAR ADCs [71, 72, 115–117]. A conventional double-tail latch-based comparator with PMOS input consisting of a preamplifier and a latch is illustrated in Figure 4.1. During the reset phase, when CLK is high, the preamplifier output nodes are reset to ground. During the integration phase, when CLK is low, the input differential voltage is amplified, triggering the regenerative latch [99, 100] to make a decision/conversion, as previously outlined in Section 3.4.

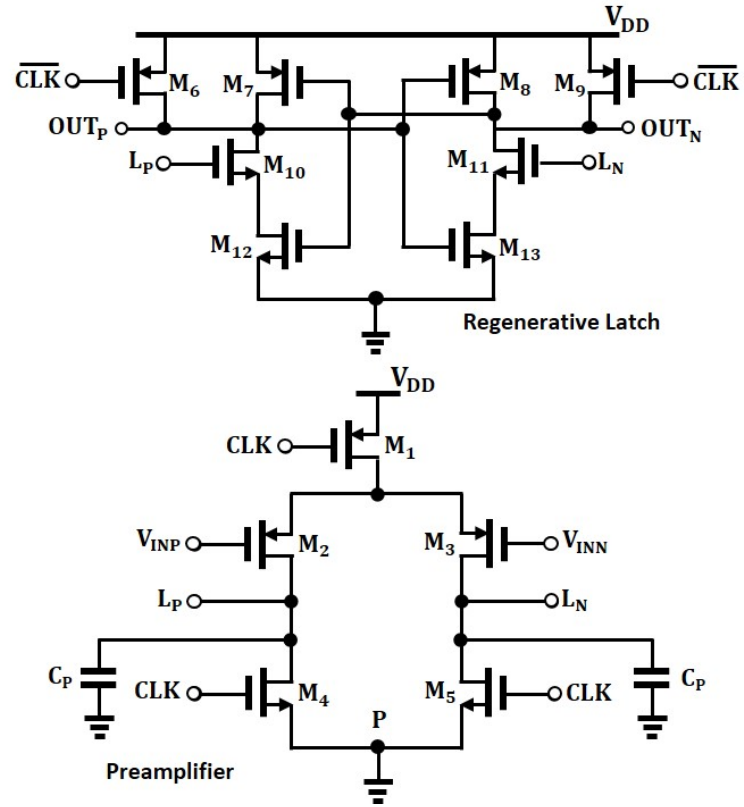


Figure 4.1: Conventional PMOS input dynamic comparator

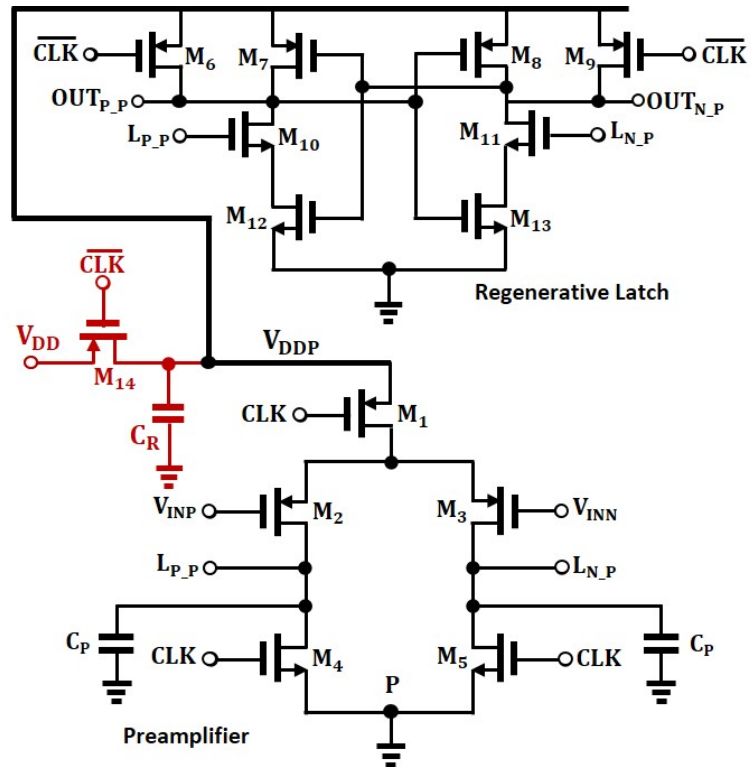


Figure 4.2: proposed switched-supply comparator

4.2.1 Design and schematic implementation

The power consumption of the comparator is dominated by the preamplifier [101, 103], which charges and discharges the loading capacitors, C_P . For each decision/conversion, the preamplifier uses a total energy:

$$E = 2 * C_P * V_{DD}^2. \quad (4.1)$$

From Equation 4.1 it is clear that the energy required to perform a conversion is proportional to the square of the supply voltage. Therefore, a supply voltage reduction would lead to a significant reduction of the energy per conversion. One way to achieve this is by implementing a dedicated DC-DC down-converter to reduce the supply voltage. However, the conversion efficiency of the down-converter can easily outweigh any energy savings made in the preamplifier stage. This work proposes a switched-supply comparator that significantly reduces the energy per conversion by reducing the supply voltage of the comparator, without the need for a dedicated DC-DC down-converter. The proposed comparator is shown in Figure 4.2, which includes the addition of a reservoir capacitor, C_R , and a switch on the power supply realised using a PMOS transistor, M_{14} . The equivalent circuit of the preamplifier during the amplification and integration phase is shown in Figure 4.3. The timing diagram of the proposed comparator in comparison with conventional comparator at critical nodes is illustrated in Figure 4.4. During the reset phase, C_R is charged to the supply voltage, V_{DD} , and at the end of the reset phase, C_R is disconnected from V_{DD} , providing the V_{DDP} voltage to the comparator. The effective voltage across the preamplifier in the integration phase, with CLK low, is given by:

$$V_{DDP} = \left(\frac{C_R}{C_R + 2C_P} \right) * V_{DD}. \quad (4.2)$$

Therefore, the energy per conversion of the proposed switching supply comparator, E_P , is:

$$E_P = 2C_P * \left(\frac{C_R}{C_R + 2C_P} \right)^2 * V_{DD}^2. \quad (4.3)$$

From Equation 4.3, it is clear that C_R can be used as a design variable to control the amount of energy per conversion in the proposed comparator. To validate Equation 4.3, Figure 4.5 shows transistor-level simulation results of the proposed comparator power consumption as a function of C_R , considering $C_P = 250$ fF, $V_{DD} = 1$ V and $f_{CLK} = 10$ MHz.

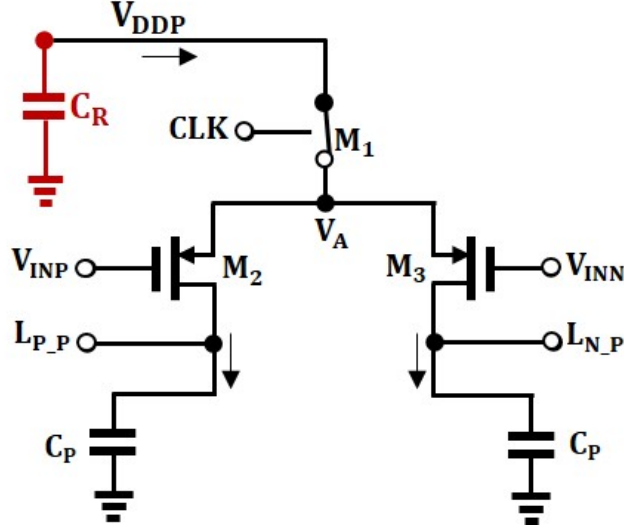


Figure 4.3: Equivalent circuit of the preamplifier in the proposed comparator during the integration/amplification phase.

In general, smaller values of C_R lead to lower power consumption, but this new design parameter cannot be set arbitrarily. There is a compromise between the maximum energy savings and the minimum effective voltage at which the preamplifier can still function. For this design $C_R = 3$ pF was selected as the best compromise giving a 28% reduction in energy per conversion.

The input referred noise [99, 100] in the conventional and proposed comparators is proportional to V_{DD} and V_{DDP} respectively:

$$V_n^2 = \frac{4kT}{g_{m,in}} * \frac{I_D}{(V_{DD} - V_{OUT,CM}) * C_{TOTAL}} \quad (4.4)$$

$$V_{np}^2 = \frac{4kT}{g_{m,in}} * \frac{I_D}{[(\frac{C_R * V_{DD}}{C_R + C_P + C_P}) - V_{OUT,CM}] C_{TOTAL}} \quad (4.5)$$

where C_{TOTAL} is the total capacitance (i.e., $C_R + 2C_P$).and $V_{OUT,CM}$ is the output common mode voltage. From Equations (4.4) and (4.5) it can be seen that the design variable C_R also serves to control the amount of input-referred noise in the comparator. Transistor-level simulations of the proposed comparator have shown that the input-referred noise decreases for smaller values of C_R , as illustrated in Figure 4.6.

In order to measure the input-referred noise for both types of comparators, a static differential input voltage, V_{IN} is applied and many comparisons are performed.

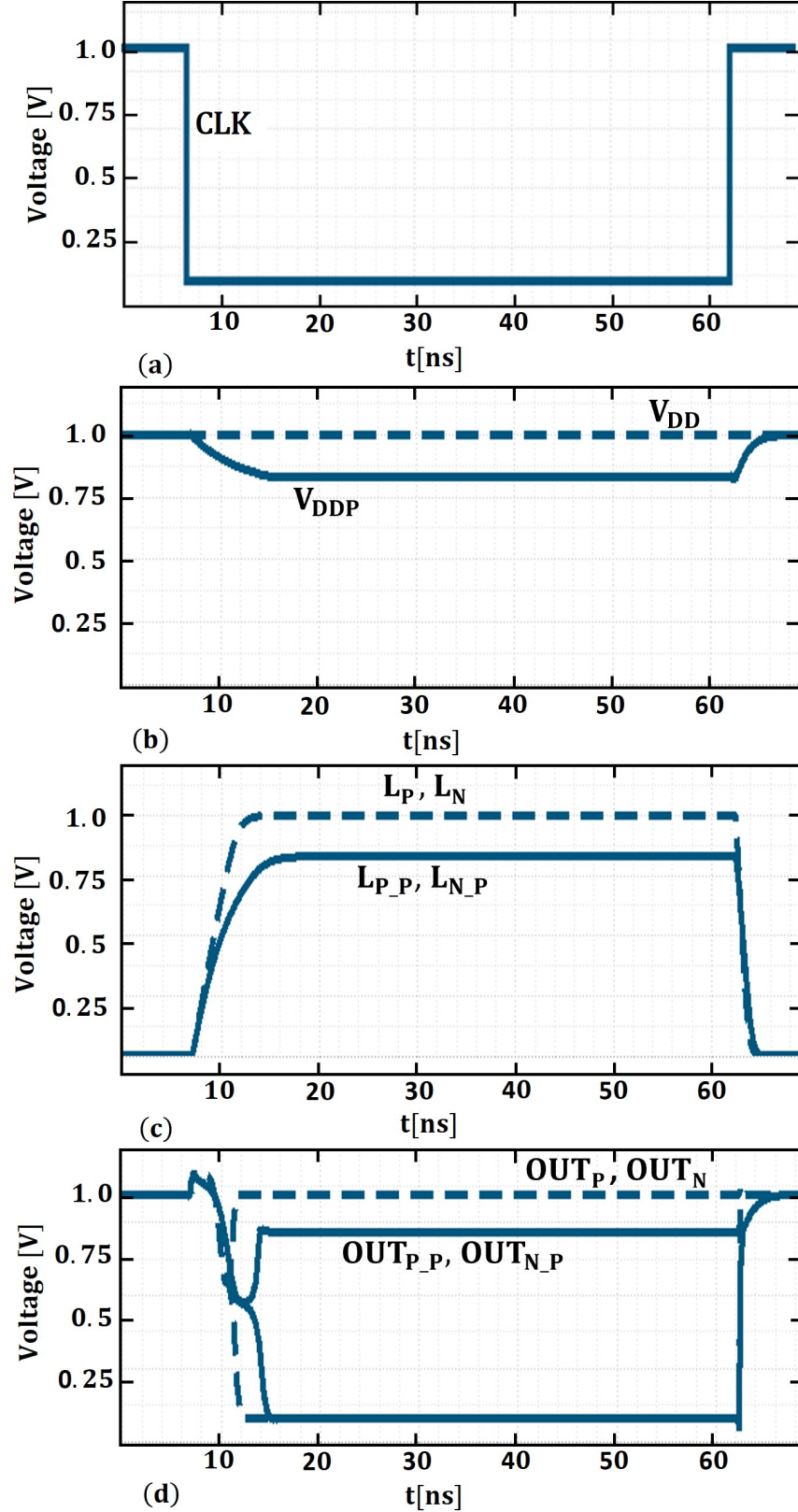


Figure 4.4: Simulated timing diagram of conventional and proposed comparator with 1 LSB input differential voltage (a) applied clock (b) internal generated supply (c) output nodes of the preamplifier (d) regenerative latch output nodes. Dotted curves are the conventional circuit (design parameters and the simulator used are mentioned in Appendix B.1).

From that data the ratio of the number of outcomes resulting in $\text{OUTPUT}(\text{OUT}+) = V_{DD}$ to those resulting in $\text{OUTPUT} = 0$ is computed. This process is repeated for small increments in V_{IN} to generate the Cumulative Distribution Function (CDF) for the probability of getting $\text{OUTPUT}(\text{OUT}+) = V_{DD}$ as a function of V_{IN} . Fitting the measurements to a Gaussian CDF, as shown in Figure 4.8, indicates an RMS input-referred noise voltage of 65 μV for the proposed comparator and 70 μV for the conventional comparator.

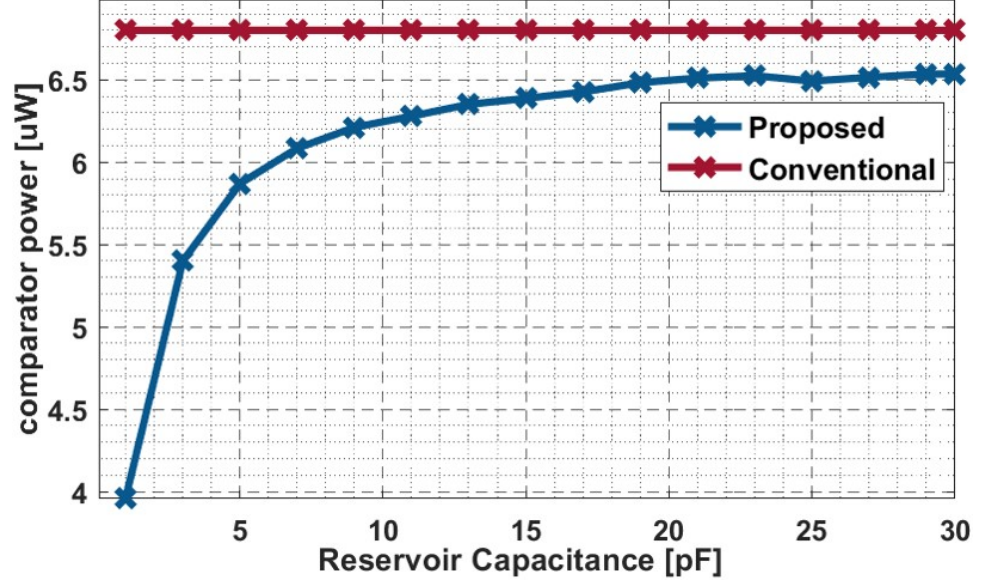


Figure 4.5: Power consumption of conventional and proposed comparators.

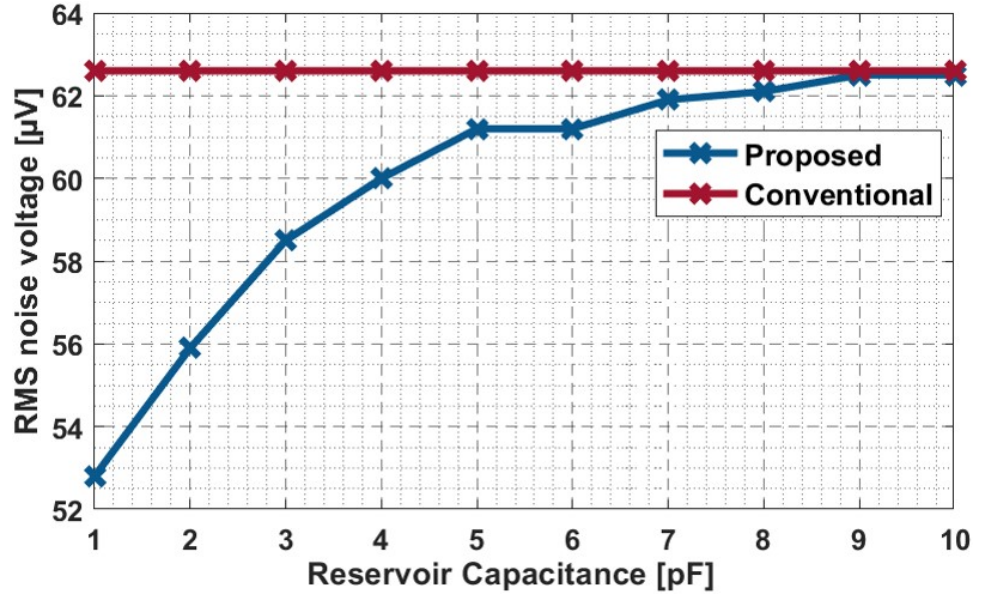


Figure 4.6: RMS noise voltage of conventional and proposed comparators.

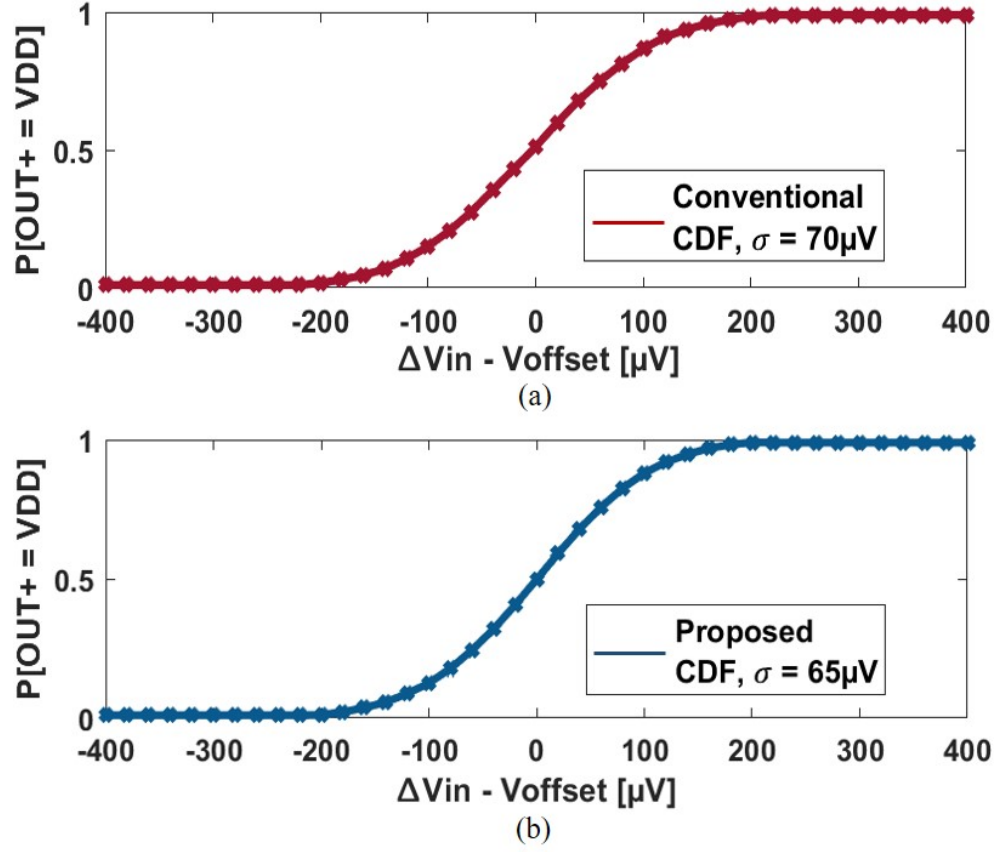


Figure 4.7: Simulated probability of an output high (one's) fitted with CDF for conventional in (a) and proposed comparator in (b).

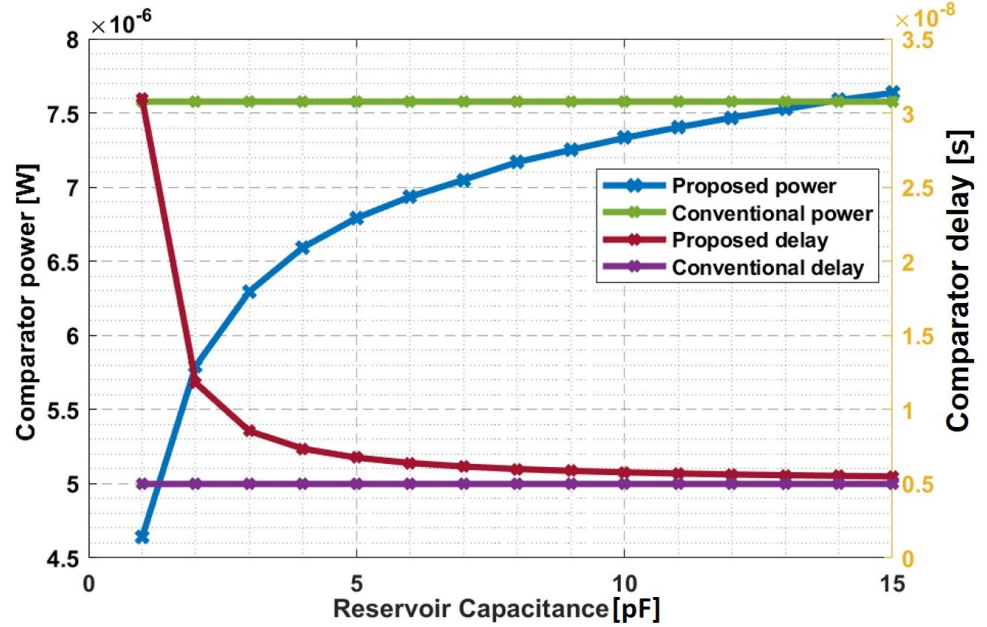


Figure 4.8: Power consumption and propagation delay for different values of reservoir capacitance. The reference power and propagation delay of a conventional comparator (with no switched-supply) are also shown for convenience.

Figure 4.8. shows a transistor-level simulation of the proposed comparator propagation delay as a function of the reservoir capacitance, C_R , along with the power consumption in comparison with the conventional comparator when considering $C_P = 250$ fF, $V_{DD} = 1$ V and $f_{CLK} = 10$ MHz. As expected, small values of C_R lead to reduced power consumption in the proposed comparator. However, this comes at the expense of reduced operating speed, as the comparator takes significantly longer to make a decision.

The proposed switched-supply comparator also reduces the effect of any power supply disturbance. When the output nodes of the preamplifier cross the threshold voltage of the NMOS transistors M_{10} and M_{11} , the regenerative latch turns on and it is at this decision point that the comparators are most sensitive to disturbances on the supply voltage. This is mitigated by the proposed comparator. Hence, any disturbances occurring on this supply do not corrupt or influence the resultant comparator decision. Any power supply noise during the reset phase is effectively sampled at the end of the reset phase and manifests as an offset to the applied supply voltage and, as such, has negligible impact on the comparator operation or performance.

Figure 4.9 shows the probability of the comparator making a HIGH decision (i.e., the output of the comparator being equal to 1) when subjected to a differential input voltage of 1 LSB, simulated with transient noise for 10,000 samples; in addition the circuit is also subjected to supply noise with an amplitude of 100 mV and a frequency ranging from 5 to 50 MHz, superimposed on the supply. It is evident that the proposed comparator outperforms the conventional comparator when subjected to supply disturbance and it has performance close to that of an ideal comparator which has no added noise.

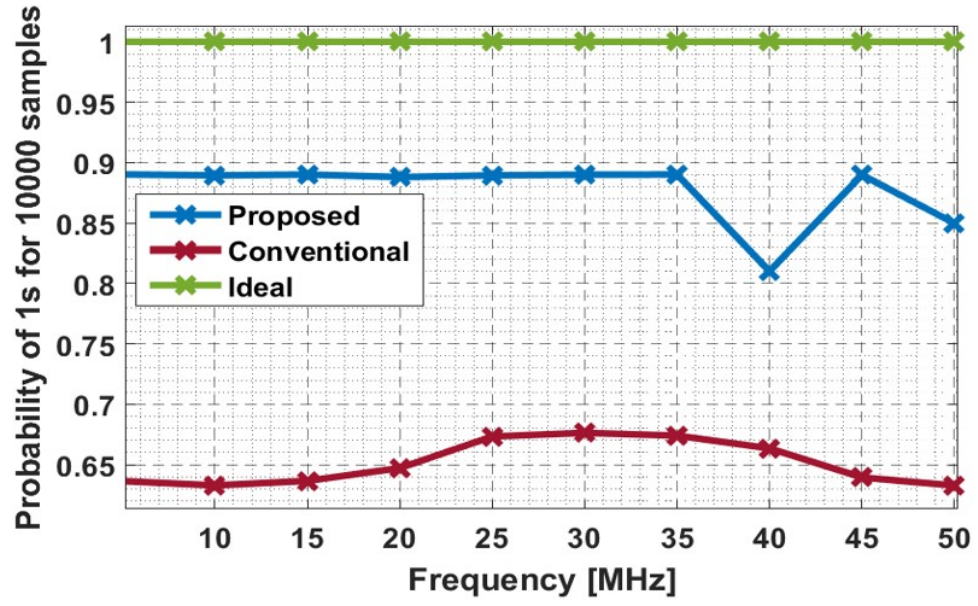


Figure 4.9: Comparison of power supply rejection of comparators

4.2.2 Layout

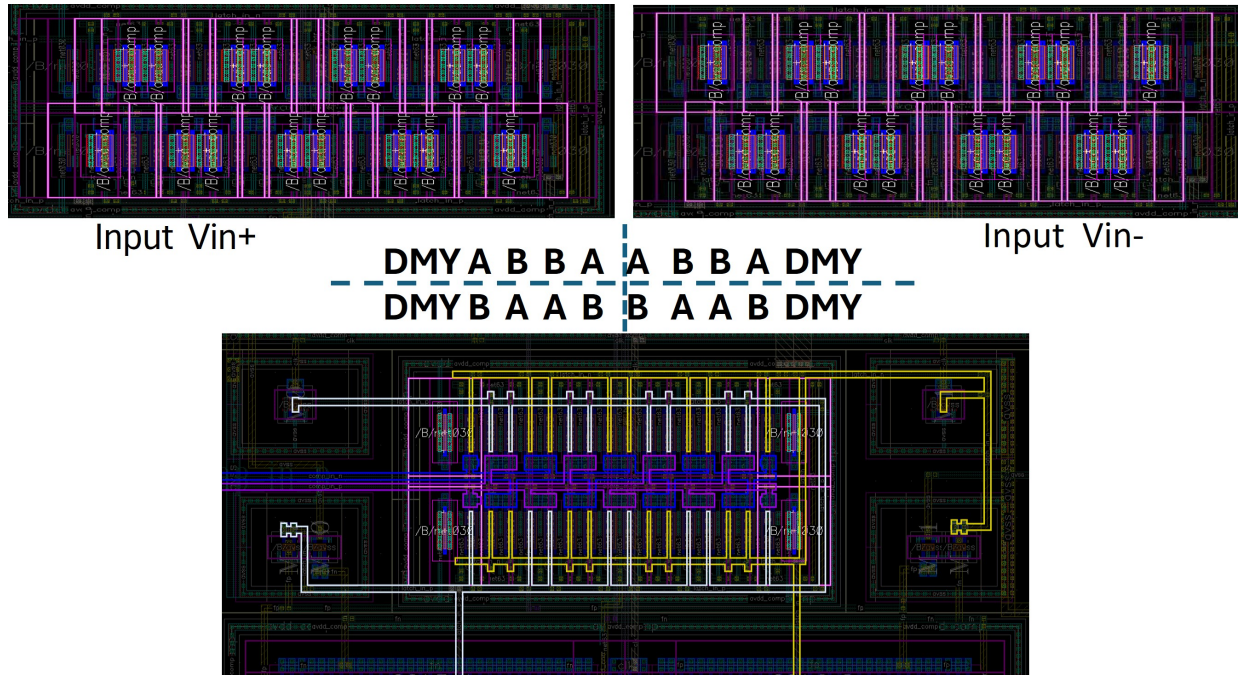


Figure 4.10: Layout of the preamplifier showing input placement.

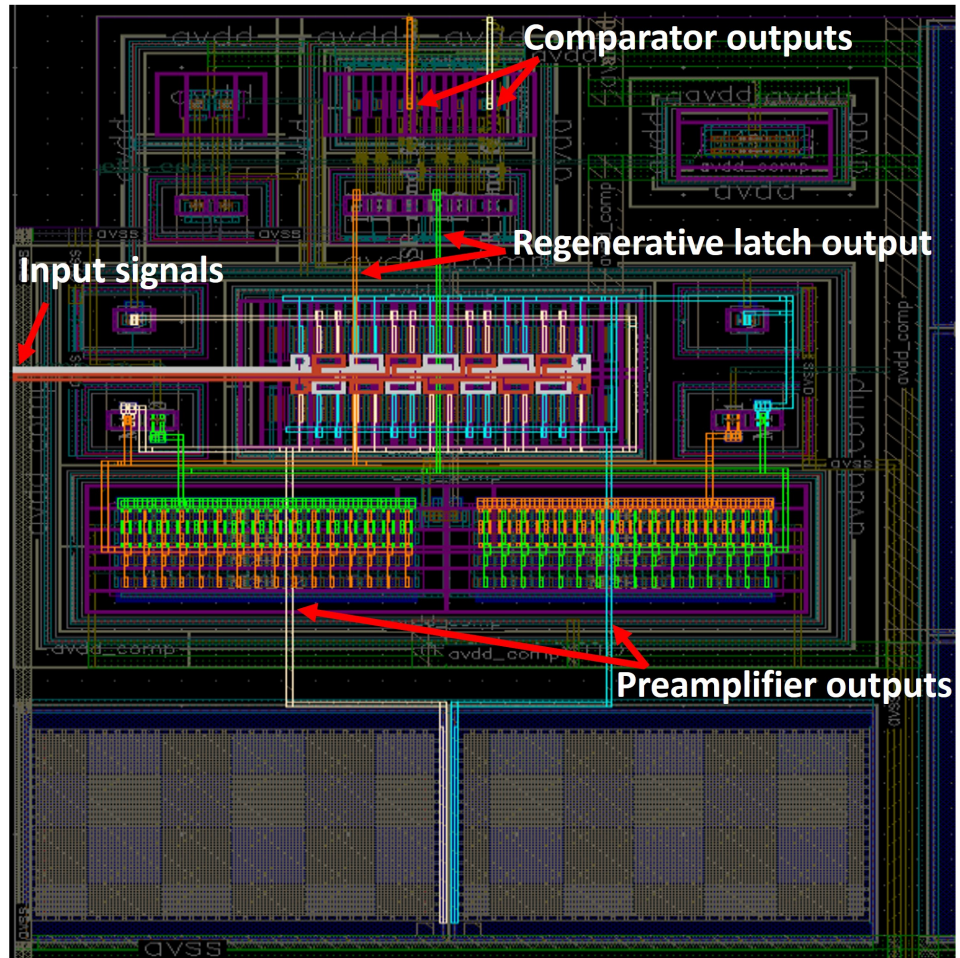


Figure 4.11: Layout of the comparator without the reservoir capacitance.

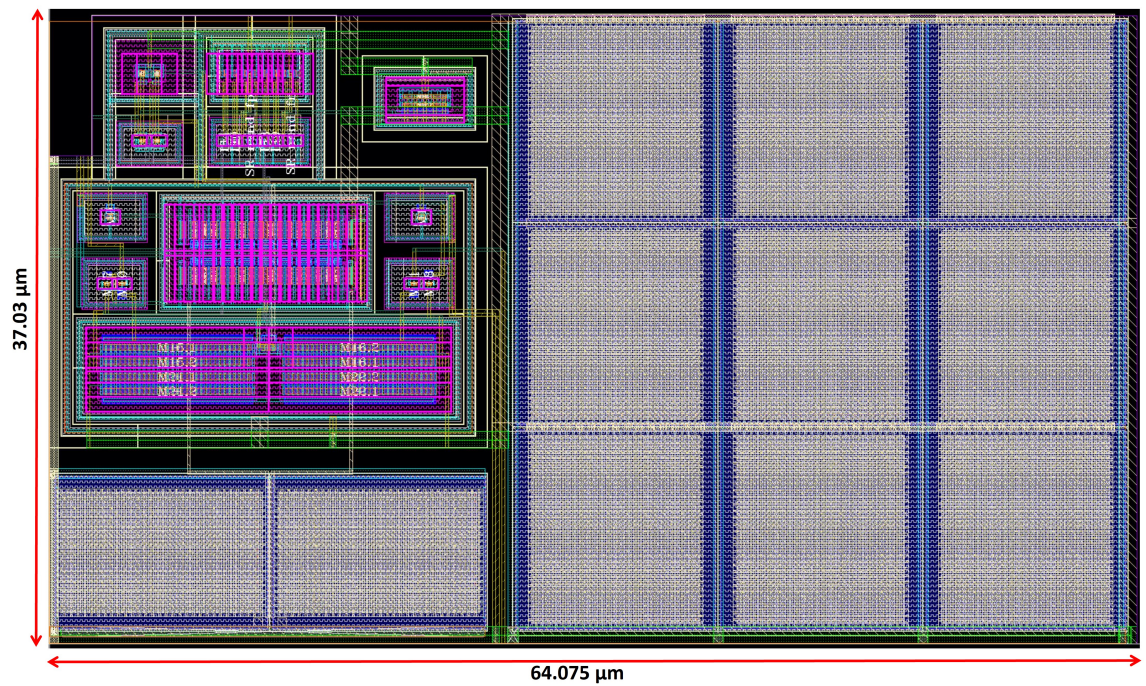


Figure 4.12: Layout of the switched supply comparator.

The input pair in the preamplifier of the proposed comparator is placed in a cross quad structure. The Interdigitated technique [118],[119] is used to improve matching for the input pair (i.e., the fingers of one transistor are interdigitated with the fingers of the second transistor. Figure 4.10 illustrates the layout of the preamplifier input stage. Figure 4.11 shows the layout of the comparator without the reservoir capacitance and illustrates the key nodes of the preamplifier and of the regenerative latch. Figure 4.12 illustrates the complete layout of the switched-supply comparator. The area of the switched-supply comparator is $64.075 \mu\text{m} \times 37.03 \mu\text{m}$ in the target 65 nm CMOS process.

4.3 Capacitive Digital to Analog Converter

When designing a DAC, the primary considerations are noise, speed, and capacitor mismatch. Noise is introduced at the moment the Sample and Hold samples the input onto the capacitor array. Additionally, further noise arises from the on-resistance of the control switches. Moreover, the supply voltage, V_{DD} used as the DAC's reference may introduce noise into the system.

Regarding speed, whenever a switch in the DAC toggles, it forms a resistor-capacitor (RC) network, causing the output to settle exponentially to the new level. As a result, this RC time constant limits the maximum operational speed, as accurate comparison in the next SAR cycle depends on complete settling of the DAC. To increase speed, either the capacitor size can be reduced or the switches can be enlarged to lower their on-resistance.

Mismatch is often a major challenge in DAC design, frequently limiting the achievable linearity in a SAR ADC. It is important to note that the capacitors in the DAC are ideally binary-scaled. However, when the capacitors exhibit random or systematic variations, leading to non-binary scaling, the search tree will no longer be optimal; further details are discussed in Section 3.5.

The choice of the total DAC capacitance value involves a trade-off: while a larger capacitance reduces noise and improves matching performance, a smaller capacitance is advantageous for power consumption, chip area, and operational speed. Due to the mismatch sensitivity, the layout of the individual capacitors and the layout of the overall array is critical. For the entire array, it is important to utilise symmetric common-centroid placement along with dummy capacitors to improve matching. For the individual elements, the designer can either rely on foundry-default devices or, occasionally, propose manually optimised units to reduce the value of the unit capacitor or enhance parasitic shielding.

A significant practical challenge in implementing the CDAC array is the large area it occupies. Increasing the CDAC area increases power consumption. One

method to reduce area is to employ two sub-arrays connected by an attenuating capacitor, known as a bridge capacitor. A capacitive array with a bridge capacitor is also known as a split-capacitor array, due to the array being split into two parts. This design allows for larger unit capacitors, enhancing matching. It also increases speed while maintaining similar INL and reducing DNL compared to a conventional binary-weighted capacitor array [91]. Each array resolves $N/2$ bits. The maximum capacitance is $2^{N/2-1}C$ and the lowest capacitor value is C . The total capacitance per array is $2^{(N/2)}C$ and the total capacitance is reduced from $2^N C$ to $2 \times 2^{N/2} C$. This bridge capacitor architecture helps to decrease the total input capacitance, area, and power consumption of the CDAC [120],[121],[122]. Typically in bridge capacitor architecture, the DAC is split evenly so that N is even. In practice, the optimum location of the bridge capacitor is a function of the process technology, capacitor matching, and target linearity.

Figure 4.13 illustrates an example of an 8-bit CDAC, both without (a) and with (b) the bridge capacitor. When a bridge capacitor is not used, the total CDAC capacitance is $256C$, but with the bridge capacitor, it is reduced by nearly eight times to $(32 + 1/15)C$. Consequently, if the same unit capacitor size is used without a bridge capacitor, the total capacitance and, therefore, the power, will be significantly higher. For a given total capacitance, the unit capacitor can be designed to be larger while still meeting the same thermal noise requirements, resulting in improved capacitor matching.

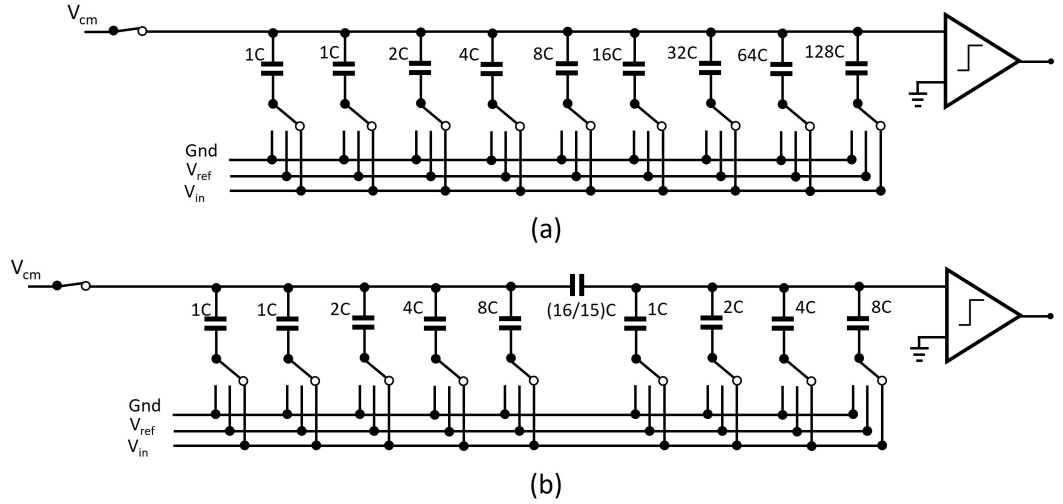


Figure 4.13: (a) 8-bit CDAC without a bridge capacitor (b) 8-bit CDAC with a bridge capacitor

The series combination of C_B (Bridge capacitor) and the entire right array must equal to C . Thus, the value of C_B is given by:

$$C_B = \left[\frac{2^{N/2}}{2^{N/2} - 1} \right] C. \quad (4.6)$$

4.3.1 Schematic

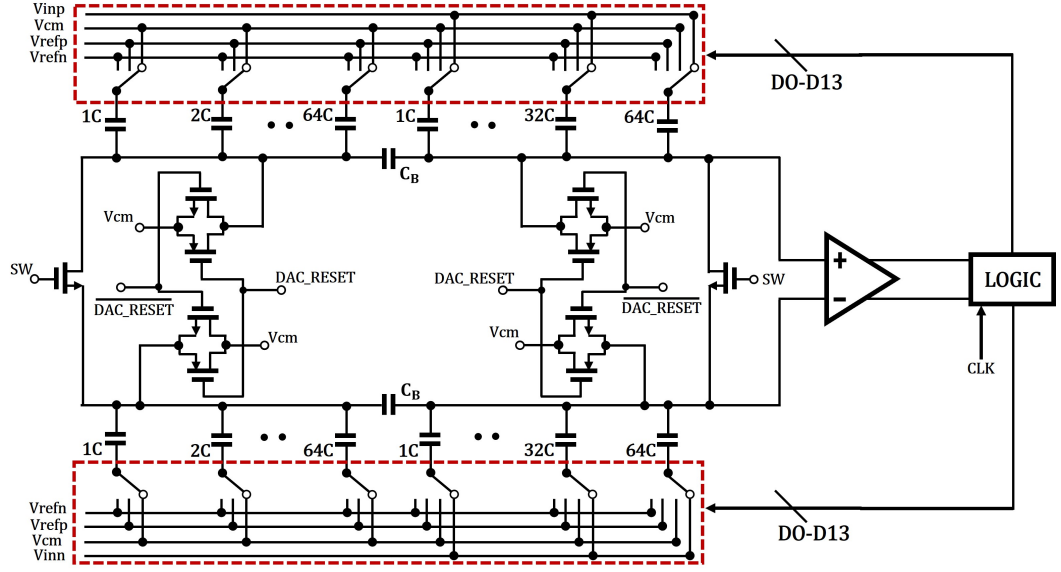


Figure 4.14: Block diagram of the implemented 14-bit SAR ADC

The high level block diagram of the implemented 14-bit CDAC in this design is shown in Figure 4.14. The Capacitive Digital-to-Analog Converter (CDAC) uses the bridge or split configuration, with 7 bits to either side. The MSBs are split into multiple 16C columns with dedicated switches, and a common centroid approach is used to enable excellent matching while simultaneously reducing the design and layout effort.

4.3.2 Unit capacitor sizing

One of the key factors to consider when designing a capacitive DAC for a SAR ADC is the sampled thermal noise, as it establishes the ADC's minimum noise floor. The total capacitance in the DAC ($C_{DAC-total}$) determines the sampled thermal noise in the ADC, as shown in Equation 4.7:

$$V_{noise} = \sqrt{\frac{kT}{C}}. \quad (4.7)$$

The sampled thermal noise is determined as follows:

$$\sqrt{\frac{kT}{C_{DAC-total}}} < \frac{1}{2}LSB. \quad (4.8)$$

In this design, to account for the randomness of thermal noise, the kT/C noise is limited to:

$$\sqrt{\frac{kT}{C_{DAC-total}}} < 77.76 \mu V, \quad (4.9)$$

where C_{DAC} is the DAC capacitance of the single ended array

$$C_{DAC} = 0.685 \text{ pF}. \quad (4.10)$$

A DAC capacitance of 0.685 pF was used, since the choice of implementation of CDAC was for matching rather than noise as the design specification was limited by the kt/C noise limit. The following calculations show the achievable SNR for the given reference voltage and total CDAC capacitance, where the reference voltage V_{ref} is equal to 0.7 V

$$SNR = \frac{P_{signal}^2}{\frac{2kT}{C} + P_{comp,noise}^2 + P_{comp,noise}^2 + P_{quant,noise}^2 + P_{mismatch}^2} \quad (4.11)$$

$$SNR = \frac{1/2(0.7)^2}{\frac{2*1.38*10^{-23}*300}{127*5.4*10^{-15}} + 60\mu^2 + 24\mu^2 + 24\mu^2} \quad (4.12)$$

$$SNR = \frac{0.245}{1.20734 * 10^{-8} + 3.6 * 10^{-9} + 0.576 * 10^{-9} + 0.576 * 10^{-9}} \quad (4.13)$$

$$SNR = 10 \log_{10}(14565992.87) \quad (4.14)$$

$$SNR = 71.63 \text{ dB} \approx 11.6 \text{ ENOB}. \quad (4.15)$$

It is important to note that the sampled thermal noise from the LSB array of the CDAC is not taken into account, as its thermal noise is attenuated by the bridge capacitor when referred to the comparator inputs. As a result, its contribution to the overall thermal noise is negligible. The total capacitance of the MSB array is $128C_u$, wherein the minimum unit capacitance C_u required to meet the thermal noise specifications is:

$$C_u = 5.4 \text{ fF}. \quad (4.16)$$

4.3.3 Unit capacitor design

The unit capacitor is a key specification in the design of the CDAC, as it directly impacts the level of thermal noise, mismatch, area, and power consumption of the DAC [123]. The area of the capacitor is particularly significant, with mismatch determined by Pelgrom's inverse-area mismatch model [106]. In CDAC design, two primary types of capacitors are commonly used: Metal-Insulator-Metal (MIM) capacitors and Metal-Oxide-Metal (MOM) capacitors.

MIM capacitors: MIM capacitors are made up of two parallel metal plates and a dielectric layer between them, as shown in Figure 4.15. MIM capacitors have relatively good area efficiency, but are constrained by strict layout rules, which restrict the minimum capacitance to a range of several fF or tens of fF. In addition, they require specialised metal layers and processing steps, making them unsupported

by some process technologies [124].

The relationship between the capacitance of a MIM capacitor and the permittivity of the dielectric, the thickness of the oxide, and the area of each metal plate is given by below Equation:

$$C_u = \varepsilon_0 \varepsilon_r \frac{A}{d}, \quad (4.17)$$

where A is the area of the metal layers, d is the distance between between the metal layers, ε_0 is the the vacuum permittivity and ε_r denotes the relative permittivity of the dielectric material. Since MIM devices utilise a thin dielectric with high permittivity, their area can be significantly minimised. As demonstrated in the MIM model in Figure 4.15, capacitance occurs vertically between two metal layers, with the bottom plate shielding the top plate from the substrate, thereby decreasing the parasitic capacitance associated with the top plate.

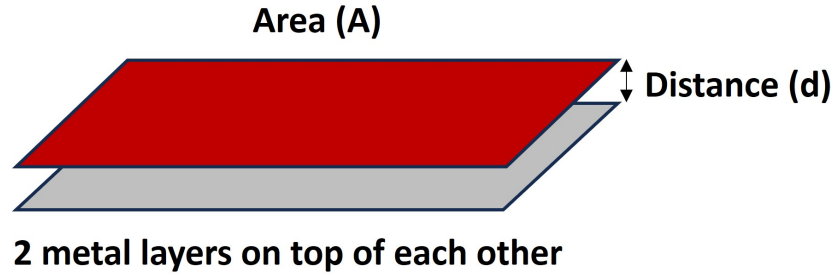


Figure 4.15: MIM capacitor structure

MOM capacitors: MOM capacitors are created using standard metal interconnect layers found in CMOS processes. These capacitors, arranged in an interdigitated pattern, can be customised to be very small, with their size only constrained by metal spacing and width design rules. Moreover, the capacitance density of the MOM capacitor can exceed that of the MIM capacitor when more metal layers are used in nanoscale CMOS processes. Due to this flexibility, increasing capacitor density, and the ability to avoid additional processing steps, a custom MOM capacitor[125] was chosen for this design.

The top view and the cross-sectional view of the MOM capacitor structure is shown in Figure 4.16. The lateral capacitance (C_{LY}) between the adjacent metal lines is shown in Figure 4.16(a). In different metal layers, the vertical capacitance (C_{AY-1}) in Figure 4.16(b) With this kind of arrangement, the MOM capacitor takes advantage of the lateral and vertical fields to extend the capacitance density [125]. Figure 4.17 shows a top view of the custom MOM unit capacitor, where the top plate is fully surrounded by the bottom plate. This design significantly reduces parasitic effects by isolating the top plate, ensuring it only interacts with the bottom plate and avoiding any path to ground. This feature is a major advantage of using

a custom MOM capacitor. The complete capacitor includes metal-2 and metal-5 layers at the bottom and top, respectively (not shown for clarity). After extraction, the unit capacitor was measured to be 5.4 fF, which meets the design's thermal noise requirements. The unit capacitor is a custom MOM capacitor with a size of $2.8 \mu\text{m} \times 2.8 \mu\text{m}$, which gives a 5.4 fF capacitance after parasitic extraction, which is shown in Figure. 4.18.

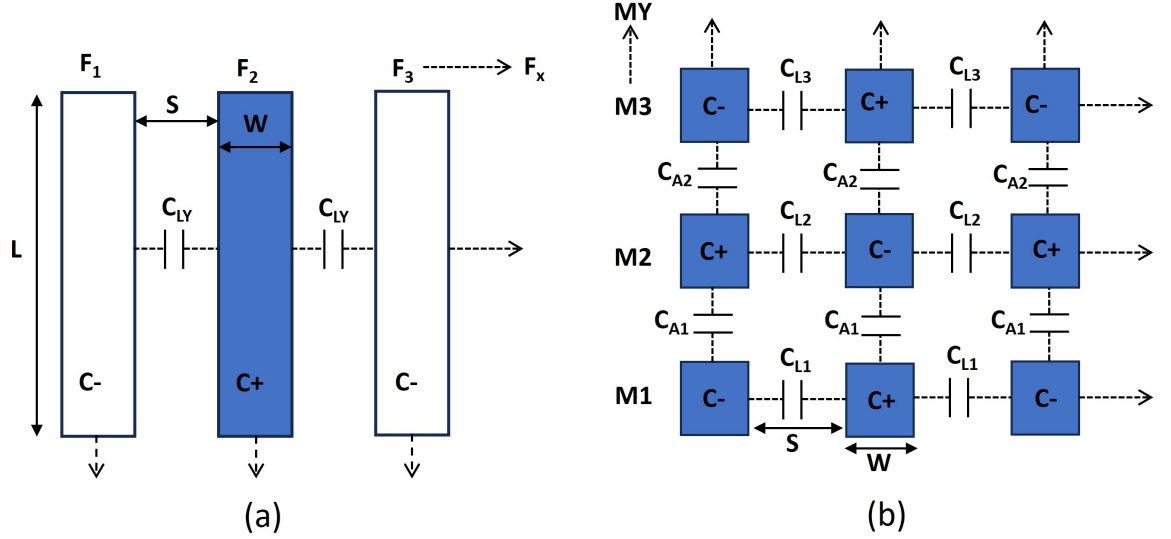


Figure 4.16: MOM capacitor structure layout (a) top view and (b) cross-sectional view [122], where F_X is finger numbers, L is the metal length, (C_{LY}) is the lateral capacitance, (C_{AY-1}) is the vertical capacitance.

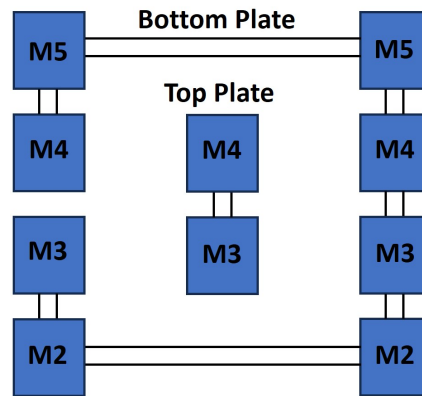


Figure 4.17: Custom MOM unit capacitor cross section.

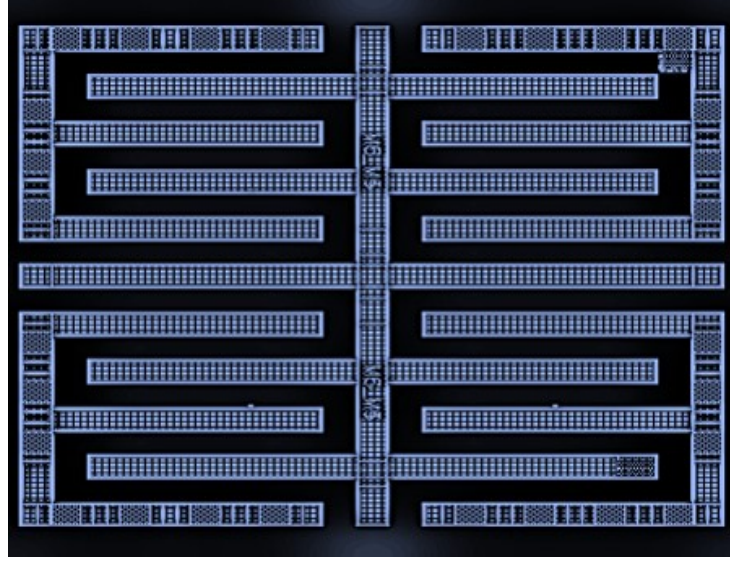


Figure 4.18: Layout of the custom MOM unit capacitor.

The physical design of the custom MOM capacitor is similar to that implemented in [126], where the top plate is completely enclosed by the bottom plate. The capacitor top plate is shielded with Metal 2 and Metal 5, which are connected to the bottom plate of the capacitor. As the bottom plate surrounds the top plate in all directions, any parasitic capacitance from the top plate is to the bottom plate, where it adds only to the core capacitance and not to the ground, thus preserving the DAC linearity [94, 126].

4.3.4 Layout and Matching

Figure 4.19 provides an illustration of the CDAC array layout, which is built using an array of C_u columns. A base column of $16C_u$ cells, where each cell is $1C_u$, was constructed. To enhance matching and minimise metal gradient effects, dummy capacitors with their top and bottom plates connected to ground were included. This $16C_u$ column was then replicated to create additional columns, with specific values (e.g. $4C_u$, $8C_u$) obtained by grounding any unused C_u cells within the array.

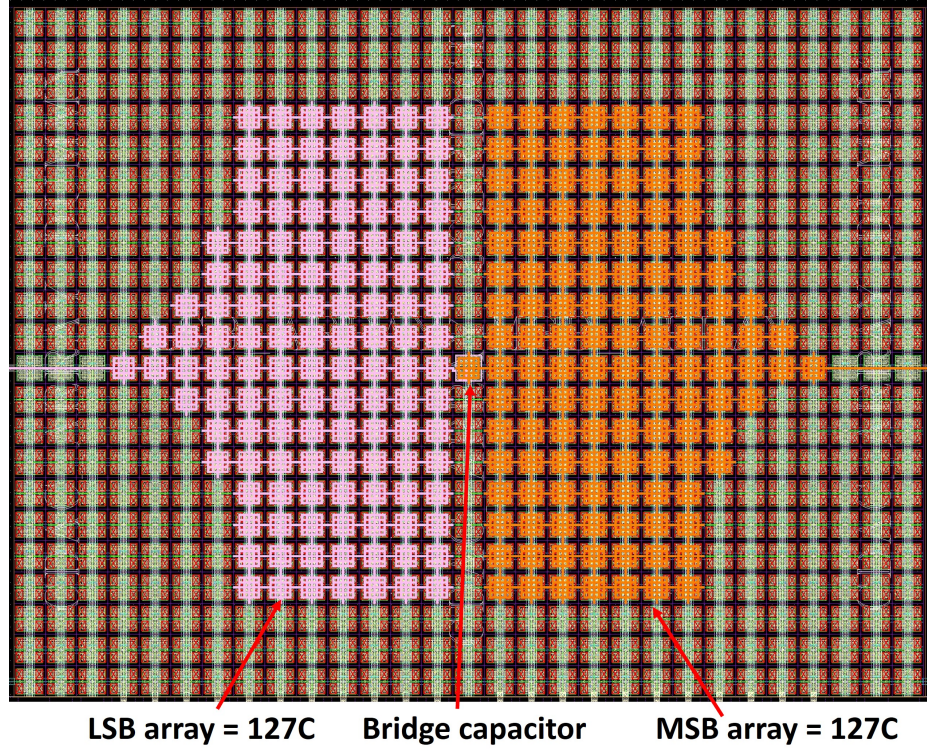


Figure 4.19: Illustration of the CDAC array layout

Column	MSB	LSB
Cbit0/cbit7	14.1373	14.1387
cbit1/cbit8	20.5314	20.5304
cbit2/cbit9	33.5065	33.5041
cbit3/cbit10	59.4533	59.453
cbit4/cbit11	111.397	111.396
cbit5_column0/cbit12_column0	111.4	111.427
cbit5_column1/cbit12_column1	111.403	111.405
cbit6_column3/cbit13_column0	111.396	111.399
cbit6_column2/cbit13_column1	111.399	111.397
cbit6_column1/cbit13_column2	111.395	111.394
cbit6_column0/cbit13_column3	111.431	111.397

Table 4.1: CDAC extracted results (values in fF).

This allowed for efficient layout while maximising matching, as each array is an exact copy of the other. Additional dummy cells were placed around the sides of each column to further improve matching properties affected by boundary conditions. Table 4.1 above summarises the total capacitor value for each column after parasitic extraction for both MSB and LSB arrays.

4.4 Switches

4.4.1 Reference and sampling switches

For the reference and V_{in} switches, as detailed in Section 2.3.2, a minimum settling time of 10.4 time constants is necessary to ensure that the CDAC voltage stabilises within $\frac{1}{2}LSB$ for a 14-bit accuracy. To achieve this, the switches must be sized with a sufficiently low R_{on} for a given period and known capacitance. All switches in the sampling path must be considered when calculating R_{on} , including the V_{in} switch in each switch column, as illustrated in Figure 4.20.

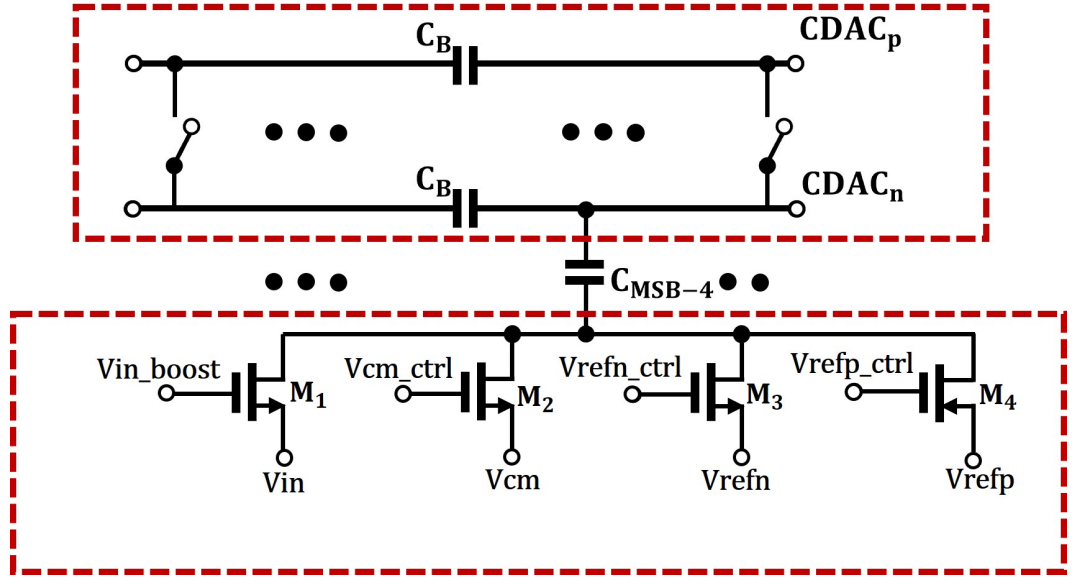


Figure 4.20: Schematic of switch column

In Figure 4.20, V_{refn} is connected with a single NMOS transistor, V_{refp} is connected with a single PMOS transistor, and a single NMOS transistor is needed for V_{cm} to pass the common-mode voltage. Additionally, a single NMOS transistor is used for the V_{in} sampling switch. To maintain a constant R_{on} for the NMOS V_{in} sampling switch, clock booster circuitry is required as explained in Section 3.7.2. However, the clock booster circuitry was not integrated within the switch column. Instead, one clock booster circuit is implemented for both $CDAC_p$ and $CDAC_n$, with its output routed to all NMOS sampling switches within the switch columns.

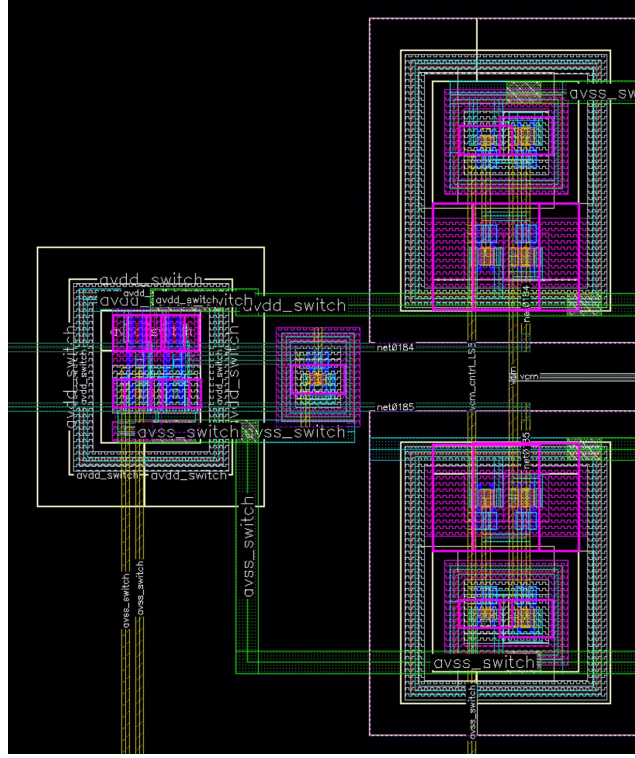
This approach was taken to minimise the overall power consumption.

To satisfy the settling time requirements, appropriately-sized minimum gate-length transistors were used. The switches were arranged in columns. This arrangement allowed for the complete CDAC to be built up one column at a time. Each capacitor column requires one switch column. V_{in} is not sampled on the LSB side of the CDAC array, so the switch column for the LSB side was modified to replace the V_{in} switch with a dummy transistor.

4.4.2 Top plate and helper switch

A top plate switch is required to reset the top plate of the CDAC to a known voltage after each conversion, as illustrated previously in Figure 4.14, and it also serves as part of the input sampling network. If the top plate of each capacitor is not reset to a known voltage after each conversion, any residual charge from the previous conversion could affect the bit trial of the subsequent bit. This can cause a dependency on the input voltage of the conversions, potentially creating output distortion.

After each conversion, the top plate is reset to V_{cm} . During the reset phase, the bottom plate voltage of each capacitor is set to the same voltage. In total, four reset switches are required: one for the MSB array and one for the LSB array for both $CDAC_P$ and $CDAC_n$. Additionally, a helper switch is used to connect the top plate of $CDAC_P$ to the top plate of $CDAC_n$ during the reset and sampling phases. This configuration ensures that both top plates are reset to the same voltage (V_{cm}) during sampling and allows for only one switch to be opened (rather than two simultaneously) to capture the sampled charge. This approach prevents offset mismatches during sampling, which could occur if the V_{cm} switches of $CDAC_P$ and $CDAC_n$ were not opened simultaneously, assuming the helper switch was not employed. The layout, including the deep N-Well of the top plate V_{cm} switches for both $CDAC_P$ and $CDAC_n$, as well as the helper switch for the MSB array, is depicted in Figure 4.21.


 Figure 4.21: Layout of the top plate V_{cm} and helper switch.

4.5 Break-Before-Make control

A Break-Before-Make (BBM) scheme is necessary to prevent multiple switches from being connected to the capacitor's bottom plate at the same time, which could create a short circuit between the V_{in} , V_{cm} , V_{refp} , and V_{refn} nodes. If two switches were to be on simultaneously, it would lead to performance issues and significant current spikes, degrading overall performance. The break-before-make mechanism ensures that one switch is turned off before another is activated.

Specifically, a BBM is needed for the bootstrap sampling switch to guarantee that it is disconnected from the capacitor's bottom plate before activating the V_{cm} reference switch. Figure 4.22 and Figure 4.23 depict the schematic of a BBM circuit for the MSB and LSB arrays. The schematic for the BBM circuit related to the clock boosting is presented in Figure 4.24. Since all capacitors in the CDAC are connected or disconnected from V_{in} at the same time, only one bootstrap BBM circuit is required for each clock boosting circuit configuration, serving both $CDAC_p$ and $CDAC_n$. The proposed BBM circuit varies slightly in comparison to Standard BBM circuits, It includes an additional control signal ($V_{cm_n_bp_cntrl}$) and a 3-input AND gate to ensure synchronous behaviour with differential SAR Logic, preventing the V_{refn} and V_{refp} switches from being turned on at the same time.

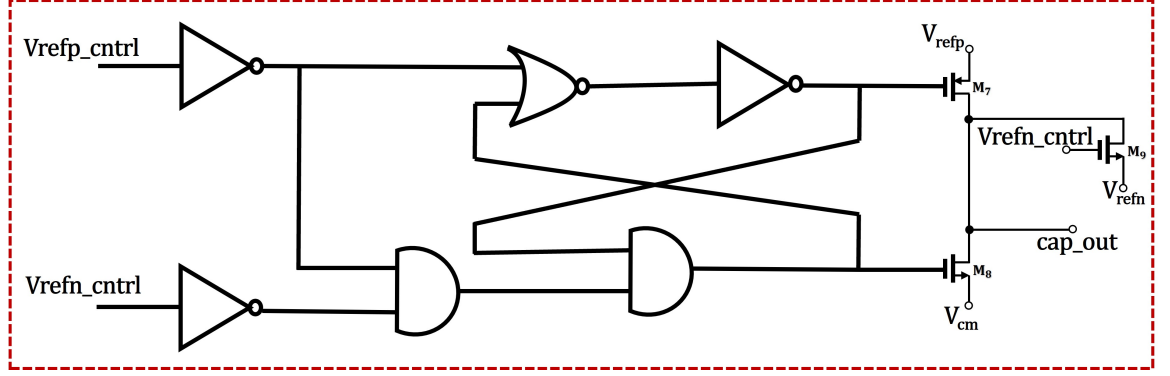


Figure 4.22: BBM circuit for LSB column.

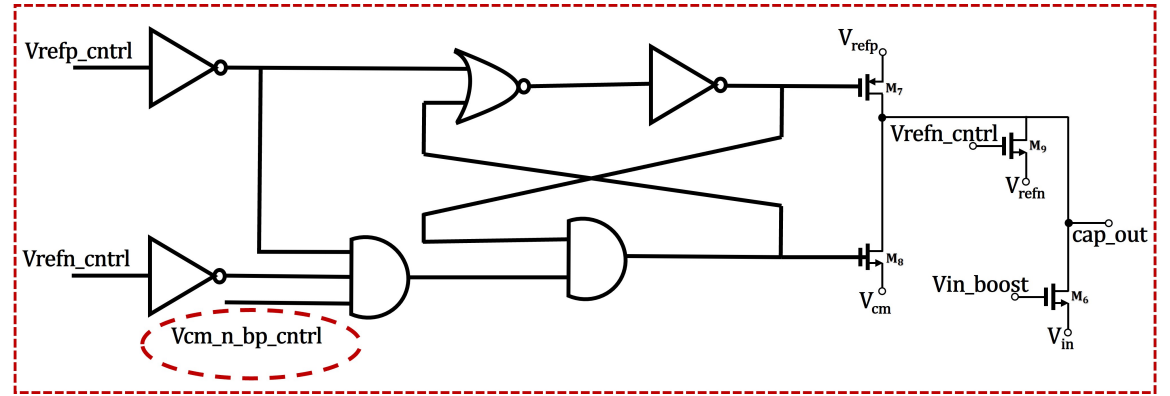


Figure 4.23: BBM circuit for MSB column.

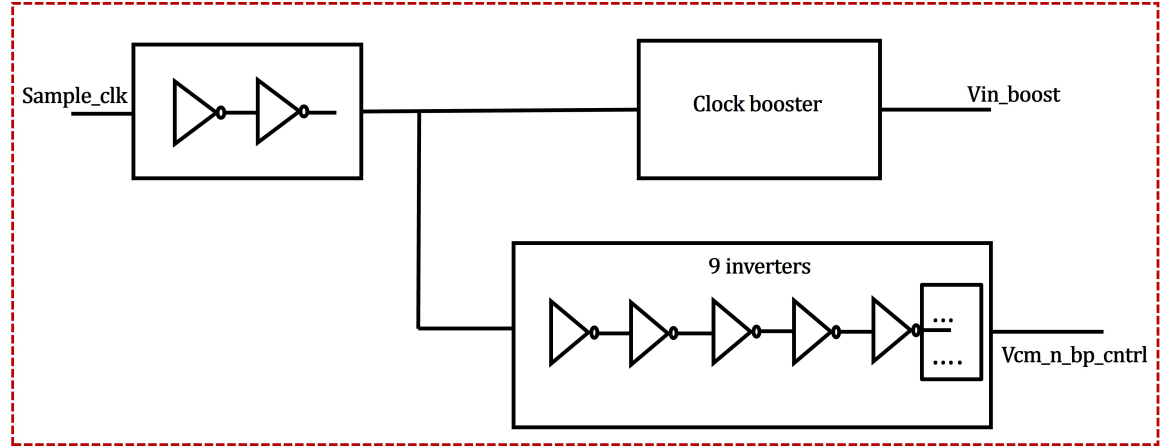


Figure 4.24: BBM circuit for the clock booster circuit and to generate the control signal for the MSB column.

4.6 Internal clock generator circuit

Figure 4.25 shows the circuit diagram of the internal clock generation circuit. D-type flip-flops, in combination with AND, OR, and NOR gates, are used to generate

internal control and clock signals. The DAC_reset and Clock_sar_1 are external signals provided off-chip. These two signals are used to generate a Start Of Conversion (SOC) signal for the synchronous SAR logic, which functions to reset all the flip-flops before the start of a conversion. The Enable clock signal is also used for the synchronous SAR logic to set the flip-flop and to shift the comparator data. Figure 4.25(b) and Figure 4.25(c) show the circuit diagrams for generating the internal signals, namely the sample clock, control signals, and the comparator clock (CLK_comparator). The comparator clock is only disabled during reset, sampling, and when the bottom plate V_{cm} signals are connected. It only turns on when the SOC signal (active low signal) is enabled.

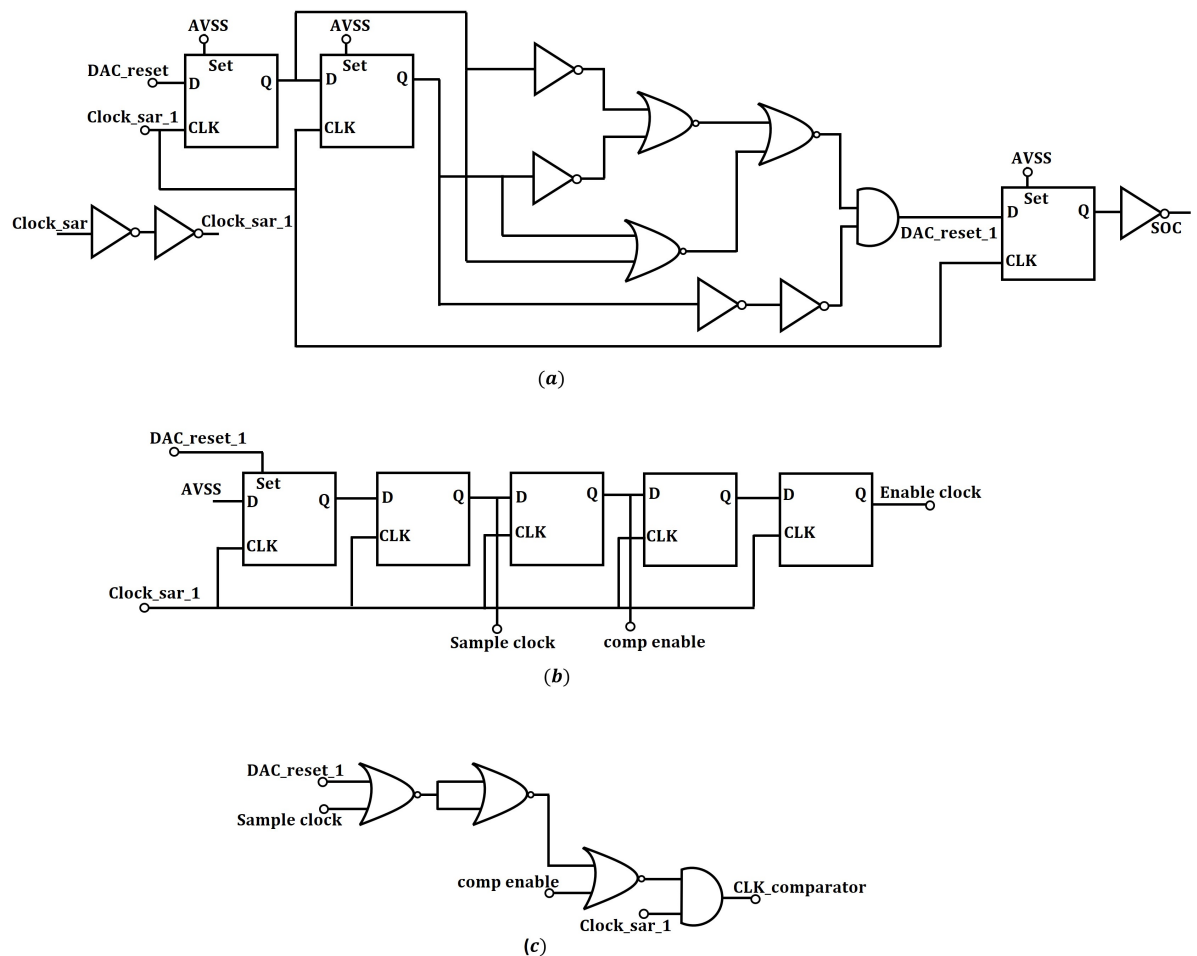


Figure 4.25: Internal clock generator circuit (a) To generate SOC, DAC_reset_1 signals and Clk_sar_1 signals, (b) To generate sample clock and enable clock signals, (c) To generate the CLK comparator signal.

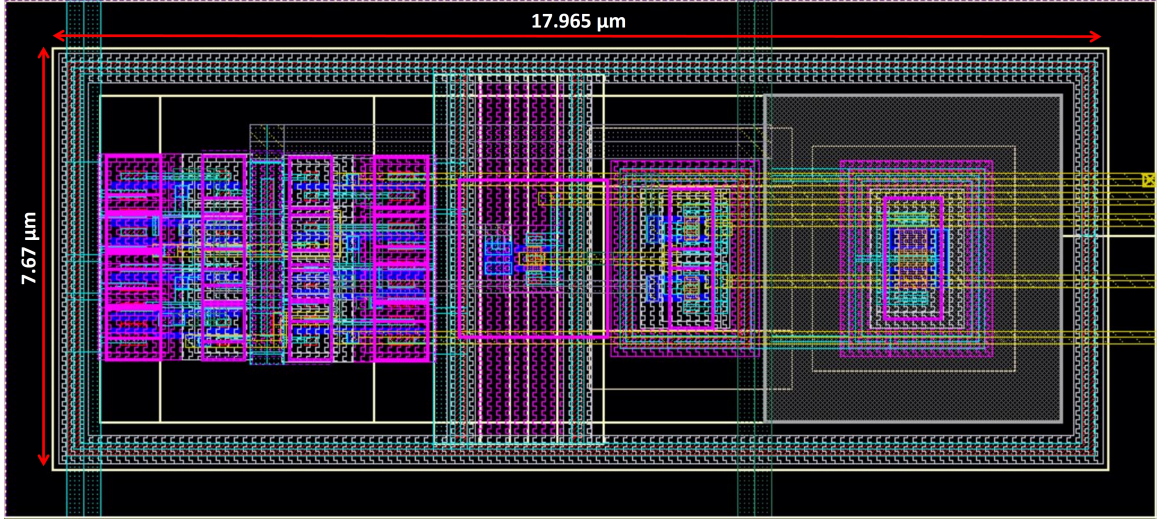


Figure 4.26: Layout of MSB column with BBM

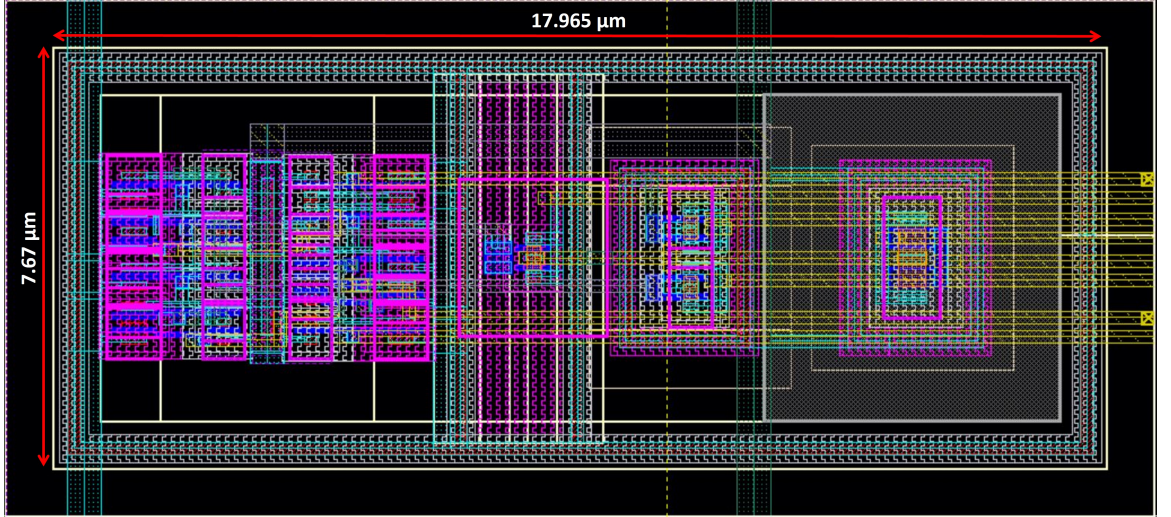


Figure 4.27: Layout of LSB column with BBM

Additionally, a BBM is essential to ensure that the V_{cm} is disconnected prior to activating either of the reference voltages, V_{refp} or V_{refn} . Given that each capacitor in the CDAC can be individually connected to each reference voltage, a separate BBM is needed for each column within the CDAC array. V_{in} is sampled only on the MSB array side of the bridge capacitor, which necessitates modifications to the LSB array BBM to accommodate this configuration. Figures 4.26 and 4.27 depict the layout of the MSB and LSB columns with a size of $17.065 \mu\text{m} \times 7.67 \mu\text{m}$. Since V_{in} is not sampled on the LSB side of the CDAC array, the switch column on the LSB side was modified by replacing the V_{in} switches with dummy transistors.

4.7 Clock boosting circuit

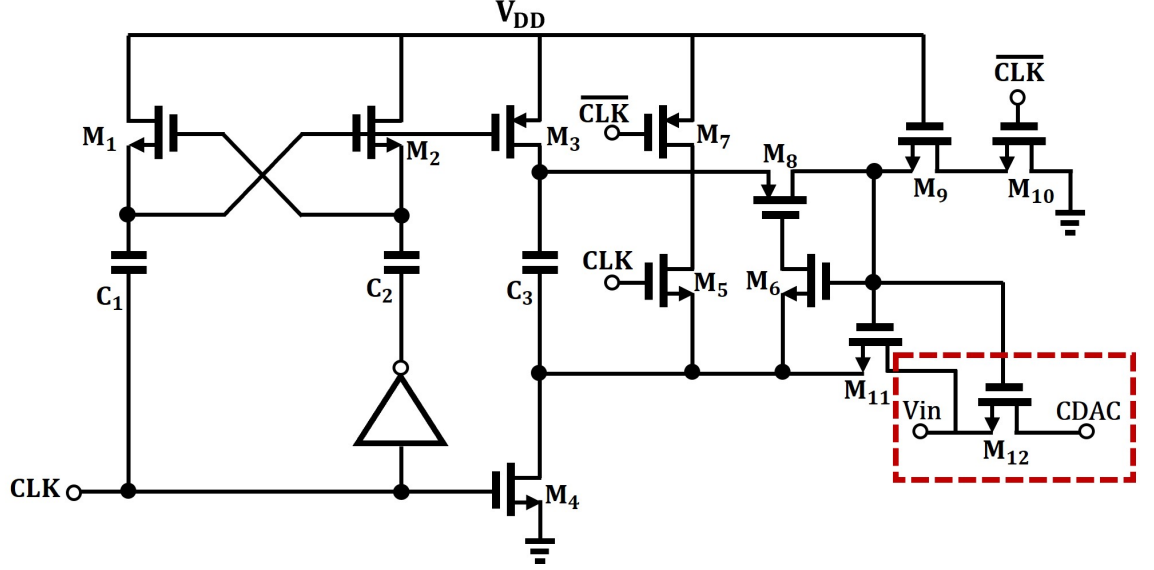


Figure 4.28: Schematic of bootstrap circuit

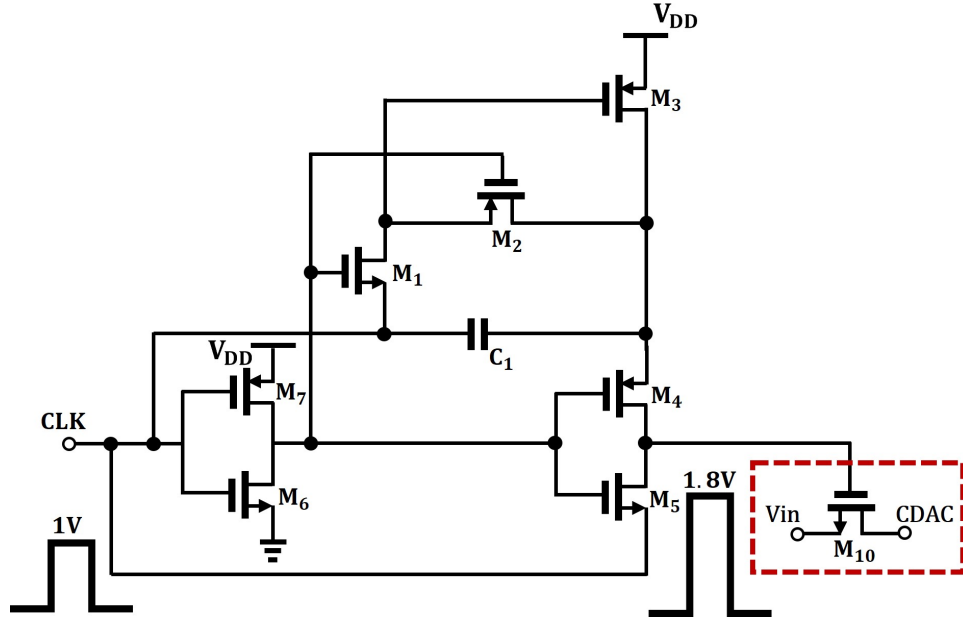


Figure 4.29: Schematic of proposed clock-boosting circuit

As described in Section 3.7, maintaining a relatively constant on-resistance for the sampling switch is crucial to prevent input-dependent distortion during the sampling process. A clock bootstrapping technique is another technique to maintain constant on-resistance to prevent input-dependent distortion during the sampling process, and to improve the speed of the Sample and Hold process in ADCs [127, 128]. The schematic of the bootstrap circuit is illustrated in Figure 4.28. The output of the

bootstrap is at the gate of M_{11} , which is bootstrapped and connected to the gate of the NMOS input (M_{12}) sampling switch. It operates in two phases namely, reset and sampling phases. The reset phase occurs when the applied clock signal is low, the transistor M_{10} is on and pulls the gate of M_6 to ground, which results in the sampling switch to be turned off. In this phase, C_3 is recharged to restore any charge that might have been lost during the previous phase as a result of charge sharing. The sampling phase occurs when the clock signal goes high, During this phase the gate of M_6 is pulled to V_{DD} by the PMOS transistor M_8 . As the voltage at the gate of M_6 continues to rise toward V_{DD} , the NMOS transistor M_{11} will eventually turn on. When this happens, the bottom plate of capacitor C_3 starts to follow the input voltage V_{in} . Since the charge on C_3 remains constant, the voltage on the top plate and, consequently, the voltage at the gate of M_6 also follows the input voltage V_{in} .

4.7.1 Schematic and Layout

There have been proposed improvements to reduce the power consumption of the previously mentioned type of circuits [112, 129–132]. In this work, the use of a clock-boosting circuit is proposed instead of a bootstrap circuit. The clock-boosting circuit has a lower power consumption and comparable distortion to the conventional bootstrap [112]. The proposed circuit is shown in Figure 4.29. It uses a single clock phase; when CLK is low the boosting capacitor C_1 is charged to V_{DD} . When CLK is high the voltage of the clock is boosted and serves as the supply of the output inverter. Note that the output inverter only drives a small output capacitance dominated by the gate capacitance of M_4 , and therefore does not impose a significant loading on the input clock.

The power consumption and silicon area of the proposed circuit are lower than that of the conventional bootstrap. Figure 4.30, compares the power dissipation of clock-boosting and bootstrap circuit as a function of sampling frequency. From Figure 4.30, it is evident that the proposed clock-boosting circuit has up to 46% less power dissipation compared to conventional bootstrap circuit at 0.5 MS/s. The absence of a fixed gate source voltage at the sampling switch could make the sampler sensitive to distortion; however, the presence of the clock-booster circuit ensures that the minimum gate-source voltage is close to V_{DD} , similar to that of a bootstrapped switch, ensuring that the NMOS switch is always turned fully on. Any variation in the applied input signal, has minimal impact on the switch on-resistance and does not result in distortion. One additional benefit of the proposed circuit is that it does not place extra loading on the input signal, because the input signal only drives the drain of M_4 . Figure 4.31 shows the layout of the clock-boosting circuit with a size of $12.22\mu\text{m} \times 18\mu\text{m}$.

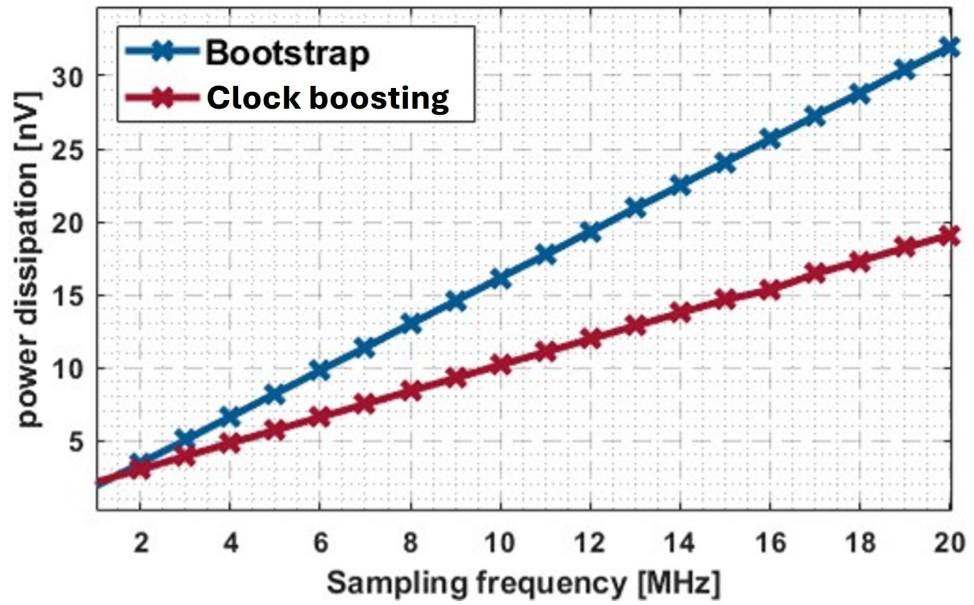


Figure 4.30: Comparison of simulated power power dissipation of clock boosting and bootstrap circuit.

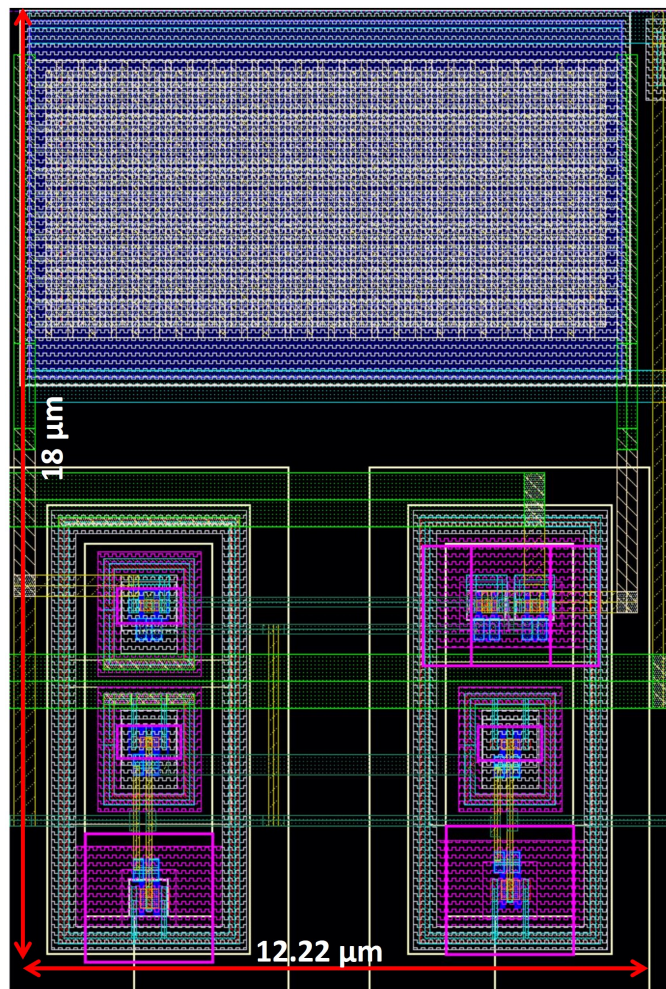


Figure 4.31: Layout of clock-boosting circuit

4.8 Hand crafted digital logic

4.8.1 Schematic and Layout

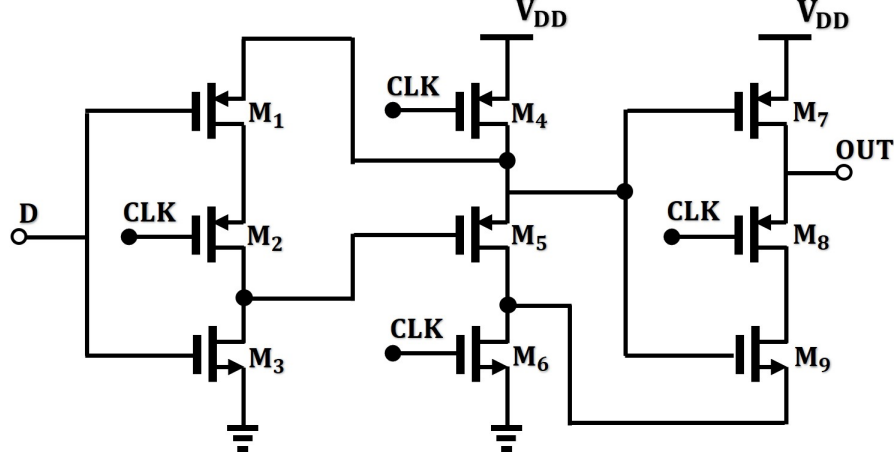


Figure 4.32: Proposed hand crafted TSPC D-type Flip-Flop.

D flip-flops are key components in synchronous digital systems, playing a crucial role in control logic, such as finite state machines. The clock distribution network often accounts for a significant portion of the total system power consumption. As a result, it is essential to reduce both the number of global clocks and the gate capacitance tied to clock nets. To address this, a True Single Phase Clock (TSPC) [133] methodology has been introduced.

A True-Single-Phase clock (TSPC) logic structure consumes less power and less area than other methods, although originally proposed for high-speed designs. It avoids the need for generating two nonoverlapping clocks, as it operates on a single clock signal. TSPC logic mainly consists of alternating PMOS and NMOS transistors, with the same clock driving all the flip-flops. The proposed D-Flip Flop is based on TSPC logic with nine transistors, six PMOS and three NMOS transistors, in three stages. It is similar to the approach in [134] in terms of the number of transistors used. Figure 4.32 shows the schematic of the proposed TSPC logic. The power consumption of the proposed TSPC logic is reduced by 10% by using the charge of M_4 to turn on the transistor M_1 and also by not allowing transistor M_9 to settle to ground completely. When the Clock (CLK) transitions from low to high and $D=0$, the red line in Figure 4.33 indicates the conducting path when CLK is high, while the green line represents the conducting path when CLK is low. Similarly, when CLK transitions from low to high and $D=1$, the red line in the Figure 4.34 indicates the conducting path when CLK is high, and green line shows the conducting path when CLK is low. Figure 4.35 shows the resultant layout of the TSPC logic with size of $8.65 \mu\text{m} \times 5.96 \mu\text{m}$.

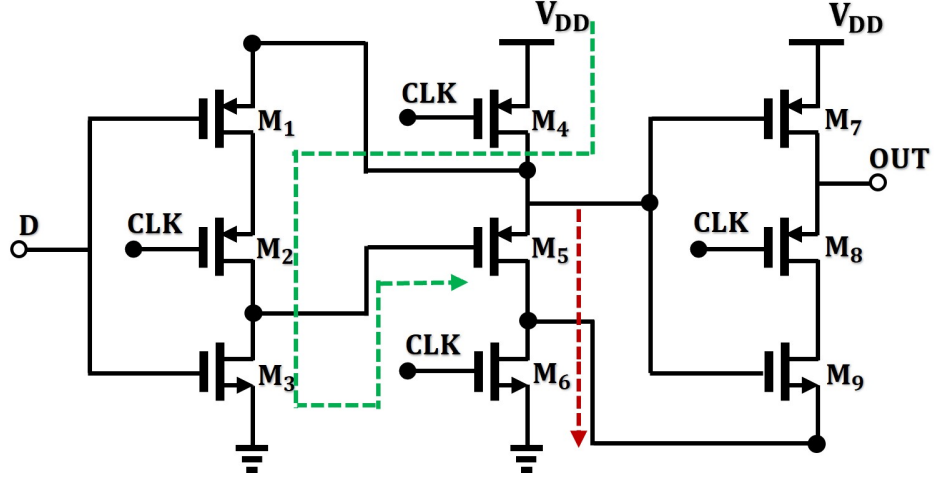


Figure 4.33: CLK : 0 $\rightarrow$ 1 ; D =0.

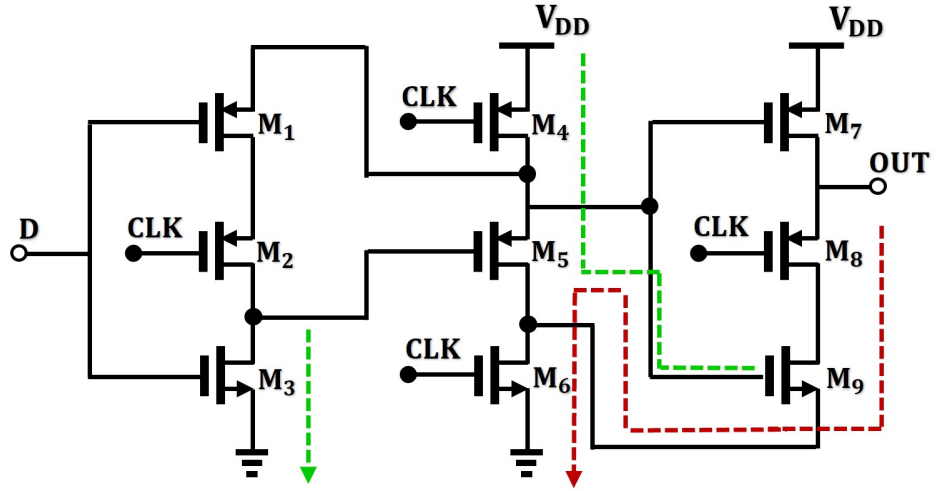


Figure 4.34: CLK : 0 $\rightarrow$ 1 ; D =1.

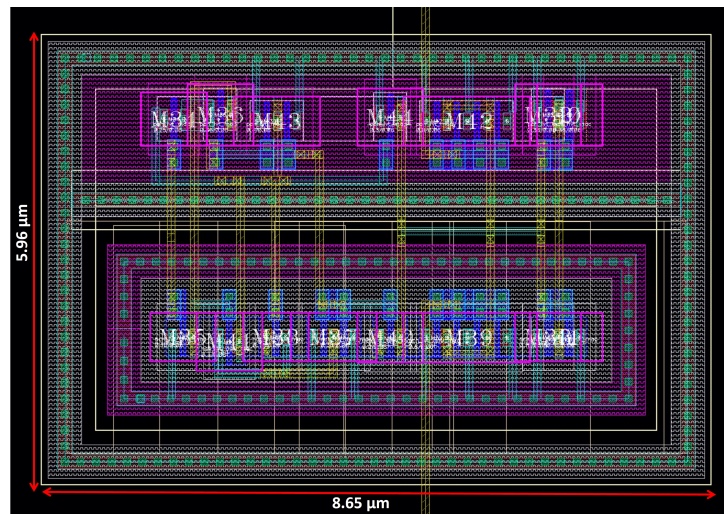


Figure 4.35: Layout of the TSPC D-type Flip-Flop.

Figure 4.36 shows the timing diagram of the TSPC logic. The Set and Clear signals are implemented by adding an additional transistors at the output of TSPC logic. Figure 4.37 shows the circuit diagram of the implemented SAR control logic. 45 TSPC cells were used for the synchronous SAR control logic. Figure 4.38 shows the complete layout of the SAR logic implemented with TSPC logic with a size of $98.33 \mu\text{m} \times 17.86 \mu\text{m}$. Figure 4.39 illustrates the Implemented Synchronous SAR logic timing diagram.

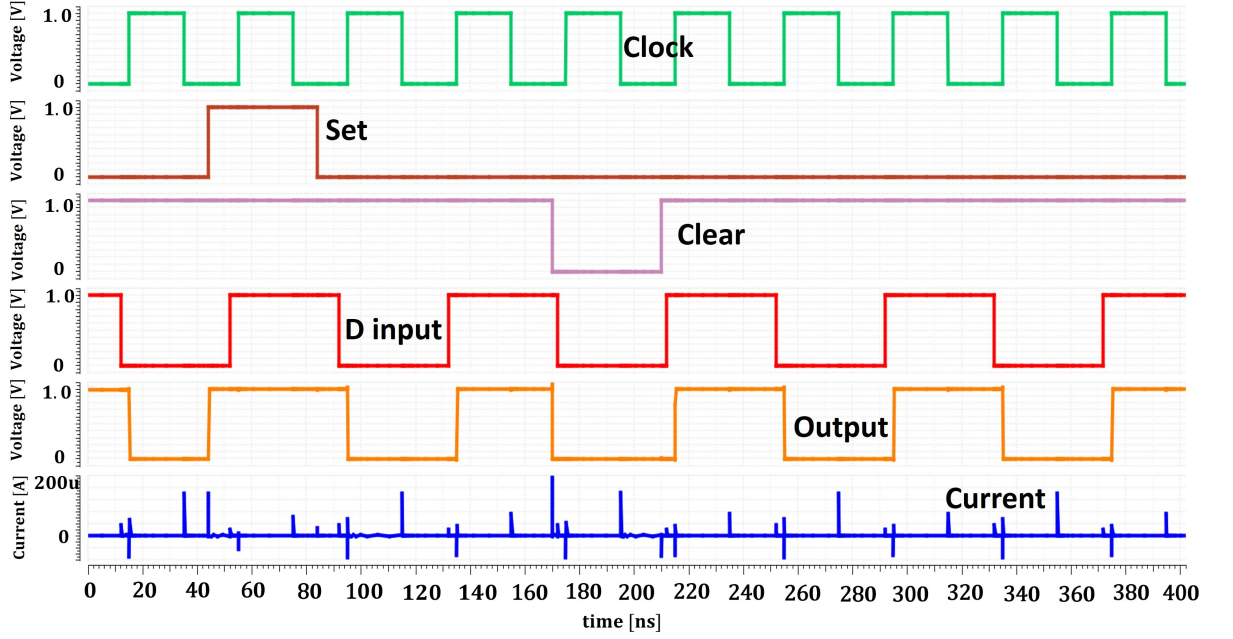


Figure 4.36: Timing diagram of TSPC D-type Flip-Flop.

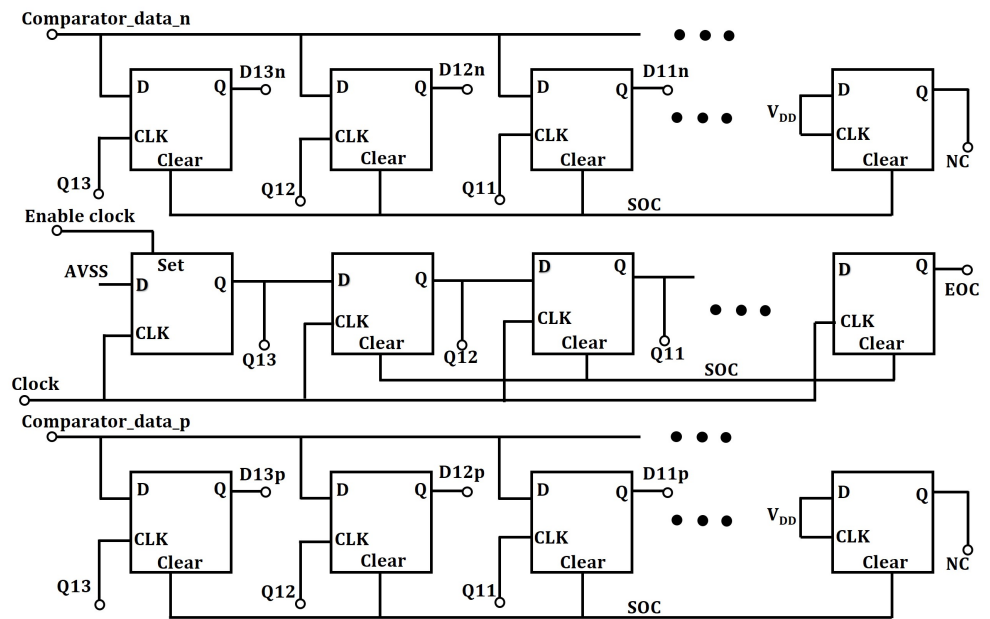


Figure 4.37: SAR control logic.

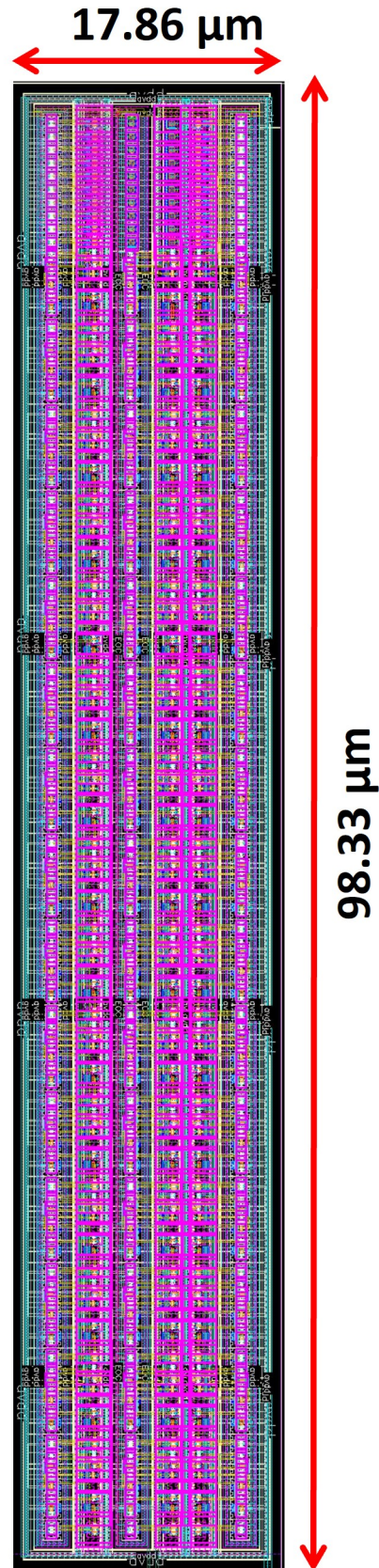


Figure 4.38: Layout of the SAR logic implemented using TSPC logic.

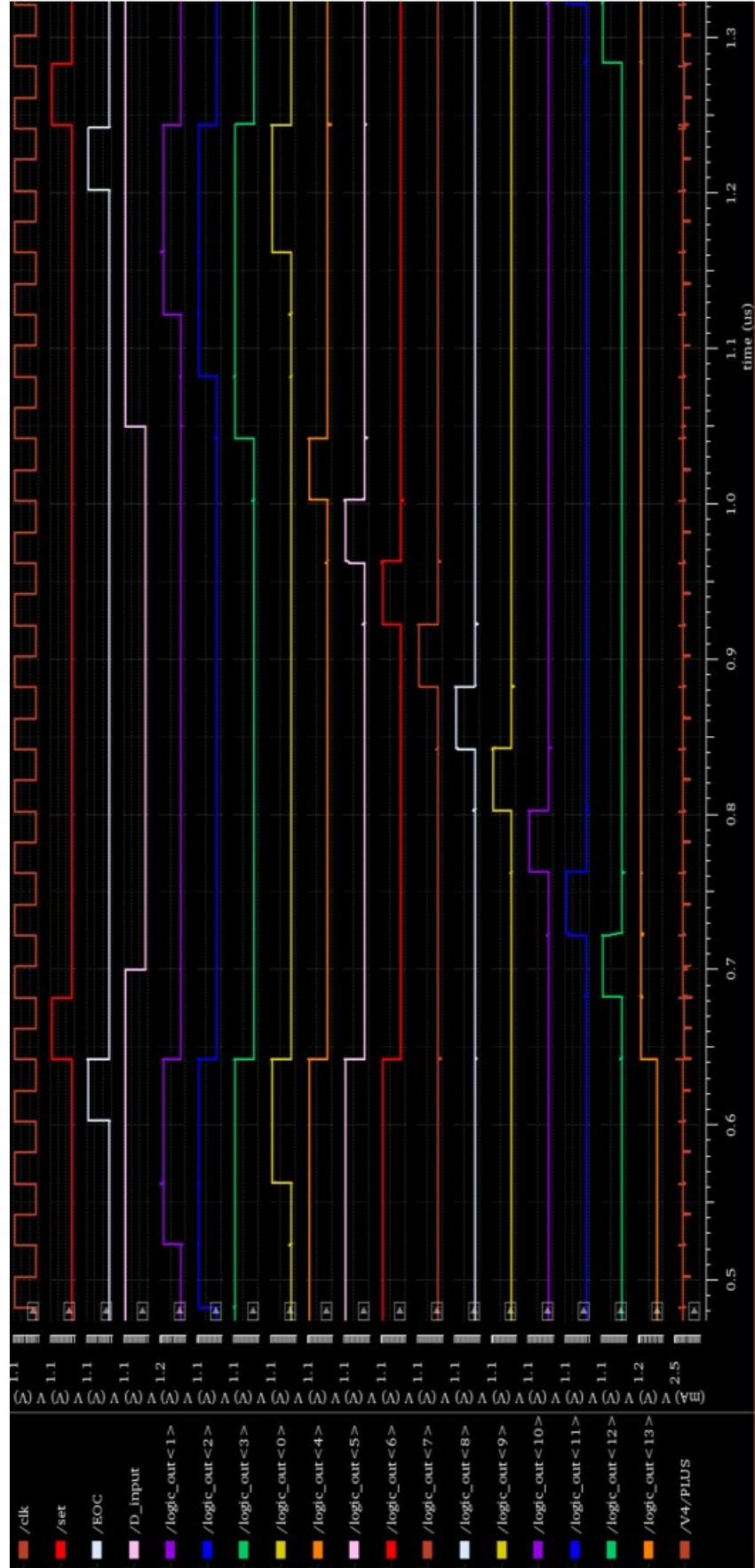


Figure 4.39: SAR logic timing diagram (Top level simulation obtained from Cadence spectre).

4.9 Top level

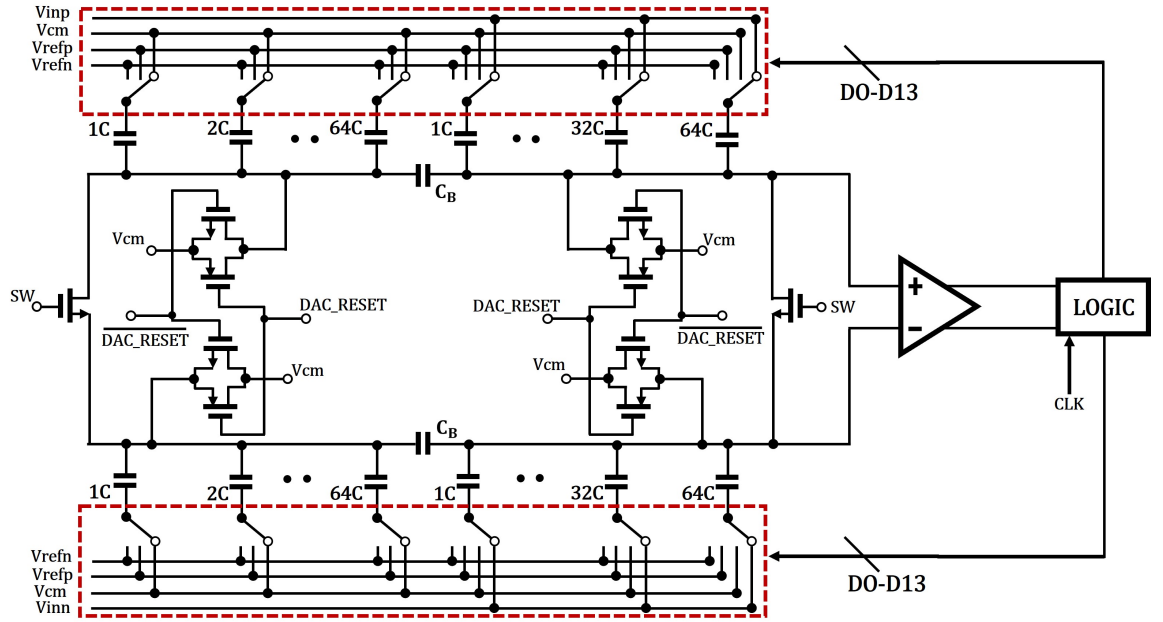


Figure 4.40: Implemented 14-bit SAR ADC with switched supply comparator.

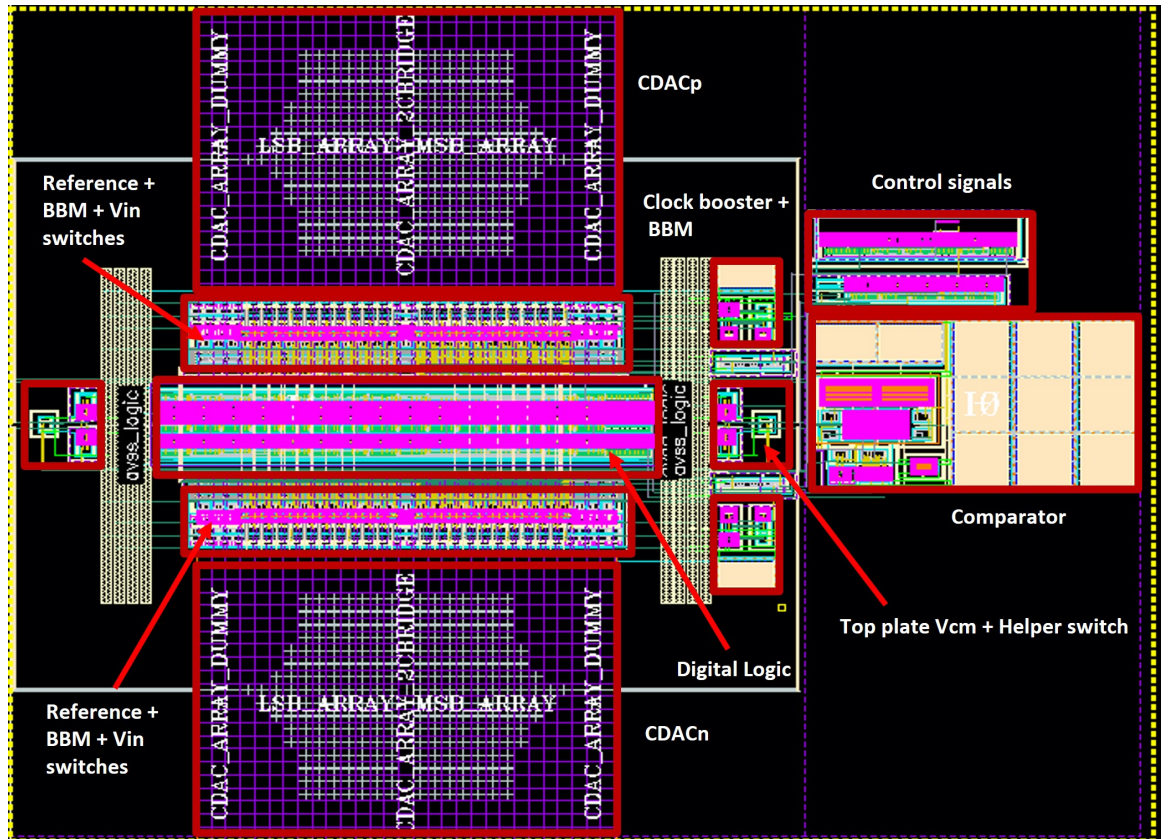


Figure 4.41: Layout of ADC core.

A high level block diagram of the SAR ADC is shown in Figure 4.40. One challenge with bridge capacitor CDAC architectures is that the top plate voltage of the LSB array cannot exceed the supply rails during a conversion [20, 121]. To avoid this, as shown in Figure 4.40, the analog input voltage (V_{in}) is sampled only on the MSB side of the CDAC array, not the LSB side. The complete core ADC layout is shown in Figure 4.41. Figure 4.42, illustrates the timing diagram of a single conversion of the implemented ADC, which requires 18 clock cycles to complete one conversion.

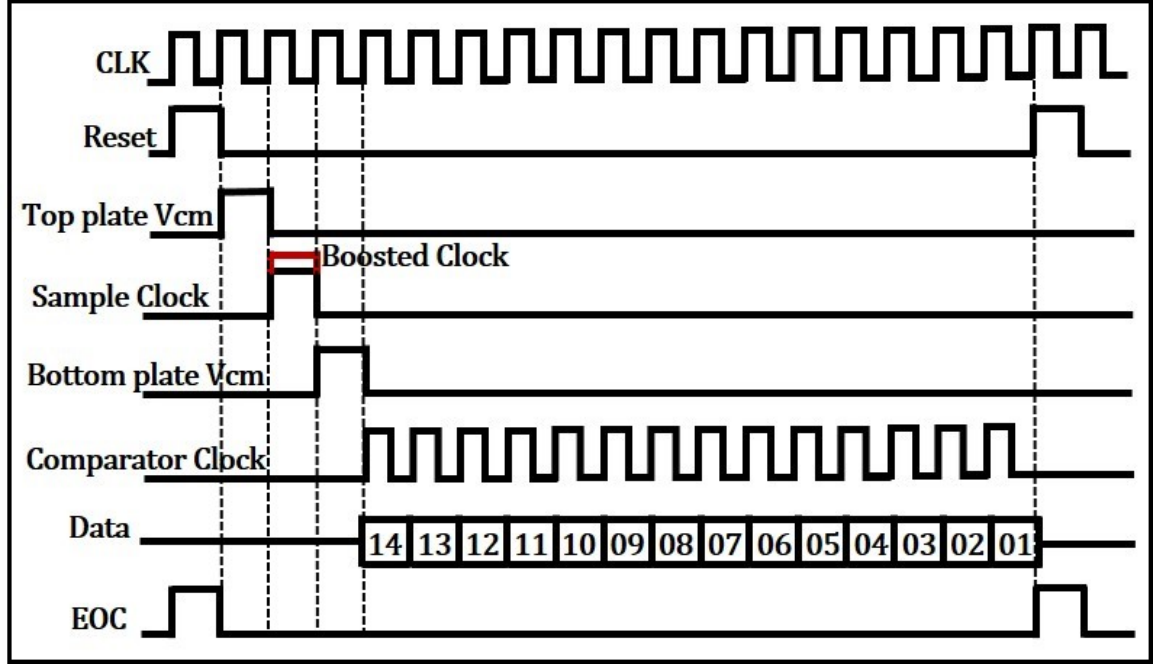


Figure 4.42: ADC operational timing diagram.

4.10 Full chip

4.10.1 I/O ring and Decoupling capacitors

The complete chip layout, including the decoupling capacitors and the I/O ring, is depicted in Figure 4.43. Decoupling capacitors are placed on each supply rail to filter out unwanted noise from the power supply and to minimise the effects of current spikes on the bondwires. Any remaining blank areas are filled with dummy metal, diffusion layer (OD), and poly (not shown in Figure 4.43 for clarity) to satisfy design rule density requirements. The die was packaged in a chip-scale-package (CSP) in a daughter card with 16 solder-balls.

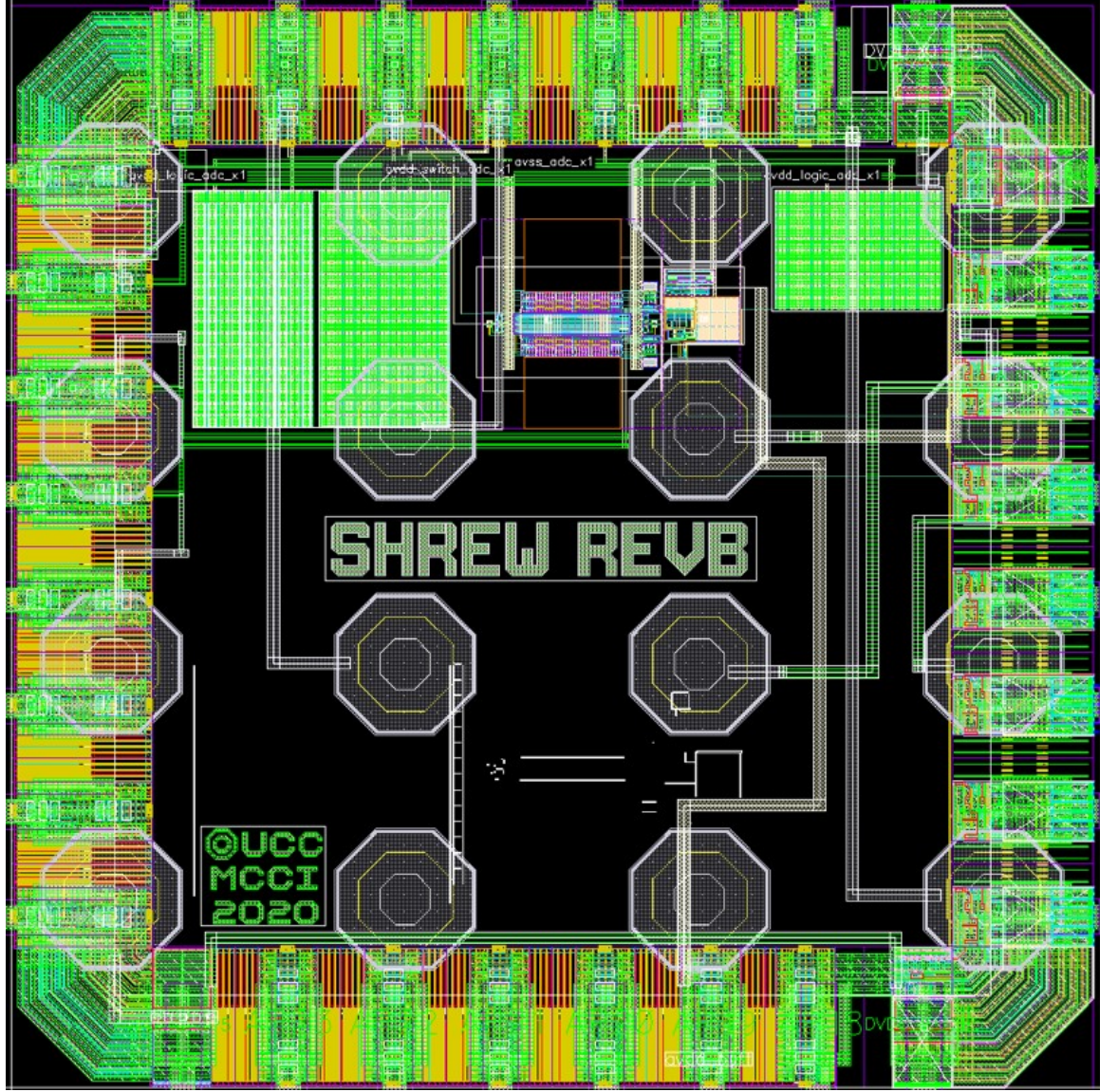


Figure 4.43: Layout of full chip.

4.11 Measured results

The measurement and evaluation setup for testing the SAR ADC is shown in Figure 4.44. A close up picture of the die in the daughter card (chip scale package) is also shown in Figure 4.44. The serial comparator data and the EOC signal (which are active low signals) are taken from the chip and converted into a parallel 14-bit word and processed in Matlab to determine the required FFT. The synchronous 14-bit ADC achieves a 500 kHz sample rate when operating from a 9 MHz clock and consumes $9.14 \mu\text{W}$ from a single 1 V supply with a full-scale range of 700 mV, with a common-mode voltage of 350 mV and an applied amplitude close to the full scale range [135].

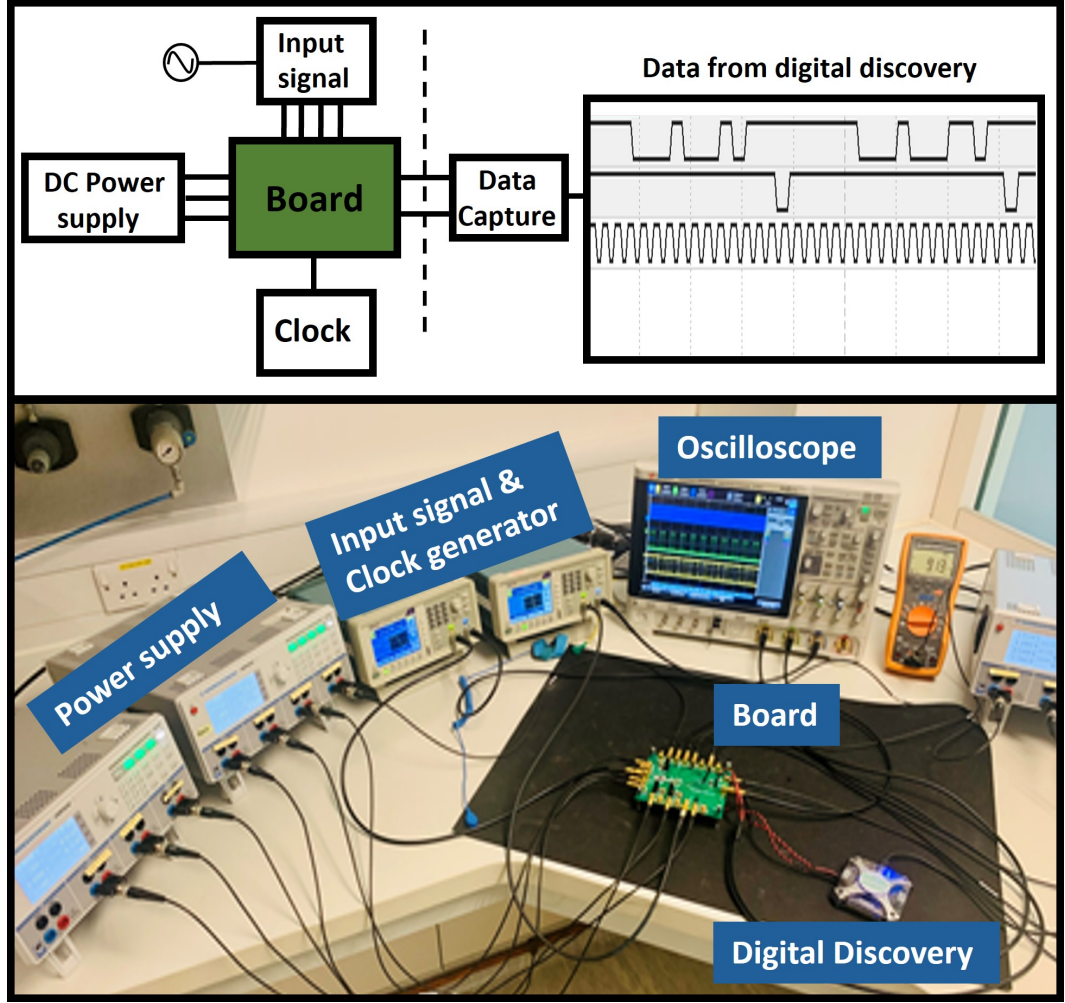


Figure 4.44: Measurement and evaluation setup for SAR ADC.

The proposed SAR ADC was implemented using a 65nm CMOS technology, and the die micrograph is shown in Figure 4.45. The SNDR remains flat across input frequencies ranging from low frequency up to the Nyquist rate as shown in Figure 4.46. This consistent performance across the input range validates the clock boosting approach, demonstrating the robustness and absence of any degradation in SNDR and SFDR. The simulated power consumption breakdown of the proposed SAR ADC is shown in Figure 4.47. The SAR control logic and the comparator consume 27% and 61% of the power consumption, respectively. Moreover, the CDAC consumes 6% power consumption and the proportion of the other analog part is about 6%. In this chip design, all the SAR core circuits share the same power supply pin, and it was not possible to measure the power of each independent block. The plot of SNDR, SFDR with respect to the sampling frequency is shown in Figure 4.48. Figure 4.49 shows the measured ADC output spectrum, using 16384 point FFT for an input frequency near DC. The ADC achieves an SNDR of 71.8 dB up to the Nyquist frequency, as shown in Figure 4.50(a). Figure 4.50(b) shows the plot of a two-tone measurement at 184.448 Hz and 189.0897 Hz. This work compares favourably to the

state-of-the-art and achieves the highest reported SNDR for a clock-boosting based design.

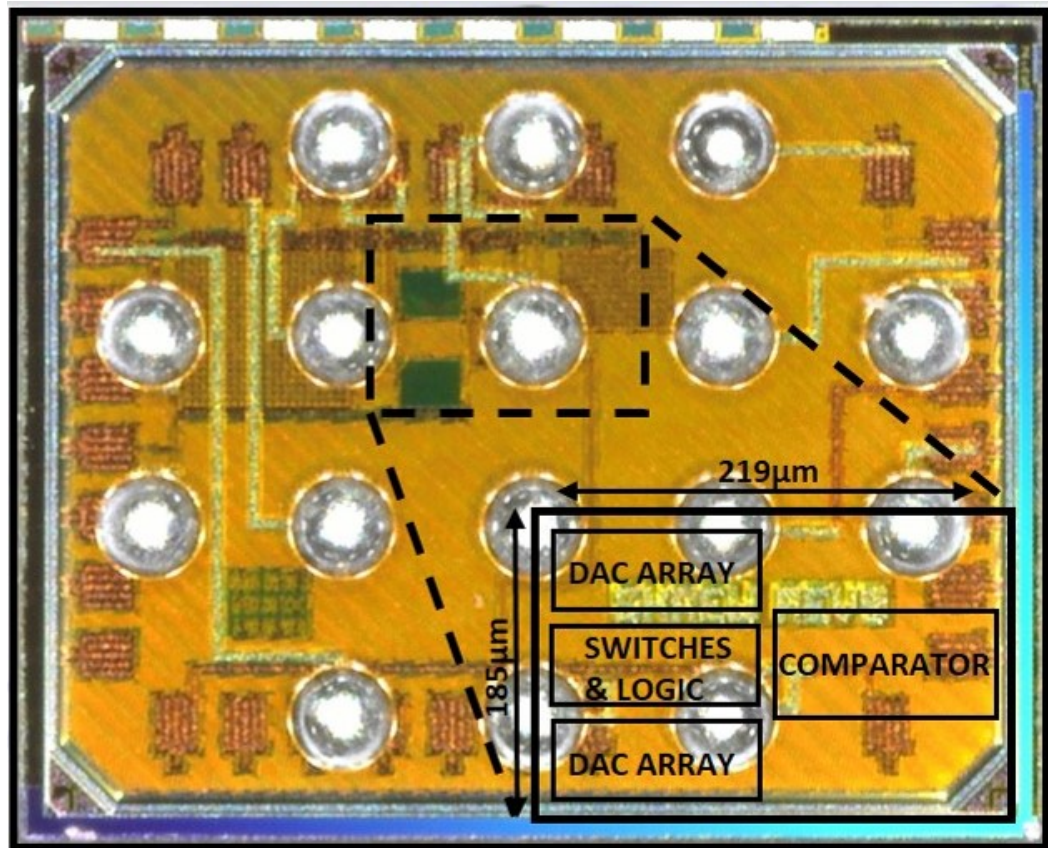


Figure 4.45: Die Micrograph.

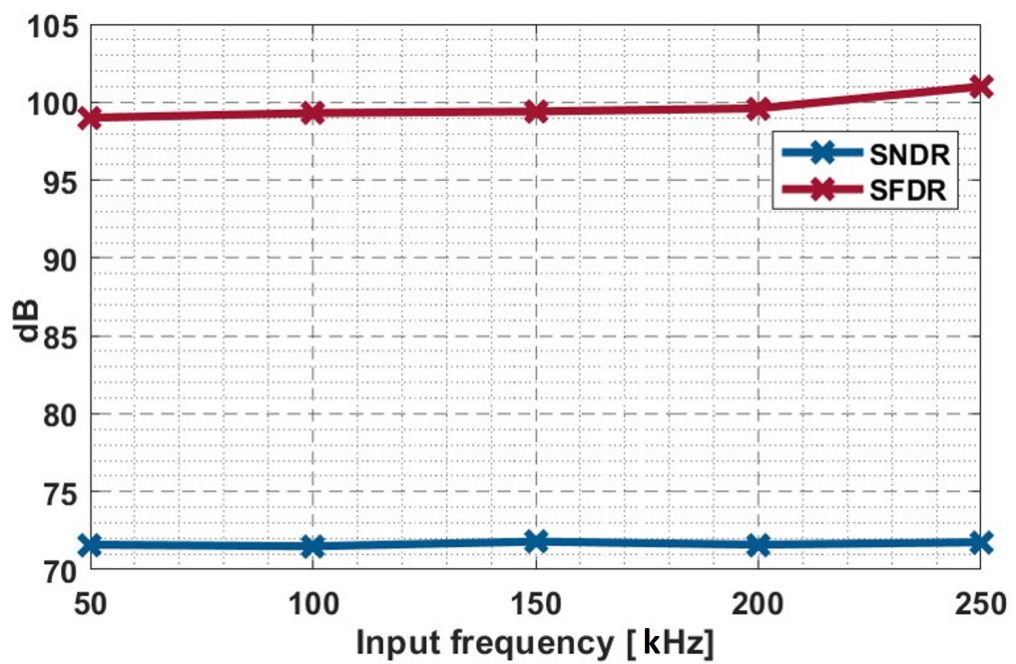


Figure 4.46: Measured plot of SNDR, SFDR vs input frequency.

This work achieves a Walden FoM of 5.7 fJ/Conv and a Schreier FoM of 176.2 dB, while operating from a single supply. This is achieved through the use of a reservoir capacitance, which reduces the effective supply voltage of the comparator, resulting in an associated noise reduction. This design is one of the first reported 1 V designs that uses clock boosting instead of a bootstrapped switch, while achieving comparable SNDR.

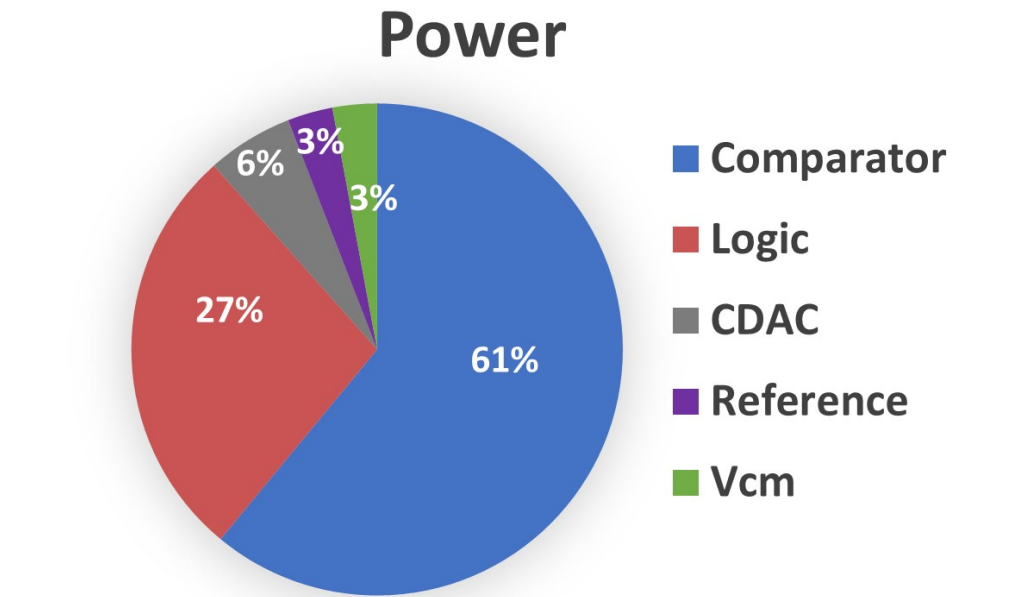


Figure 4.47: Simulated power breakdown of the proposed SAR ADC.

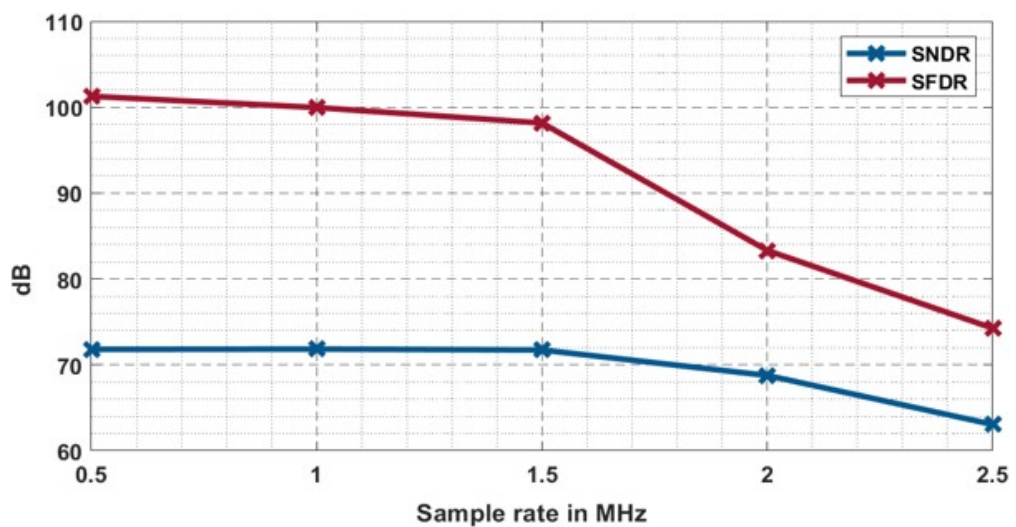


Figure 4.48: Measured plot of SNDR, SFDR vs sampling frequency.

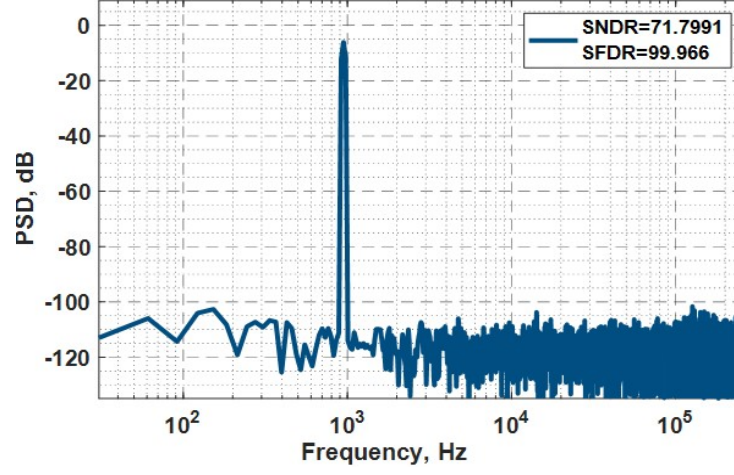


Figure 4.49: Measured ADC output spectrum, 16384 point-FFT near DC ($F_{in} = 946.00449219$ Hz) with full scale input range.

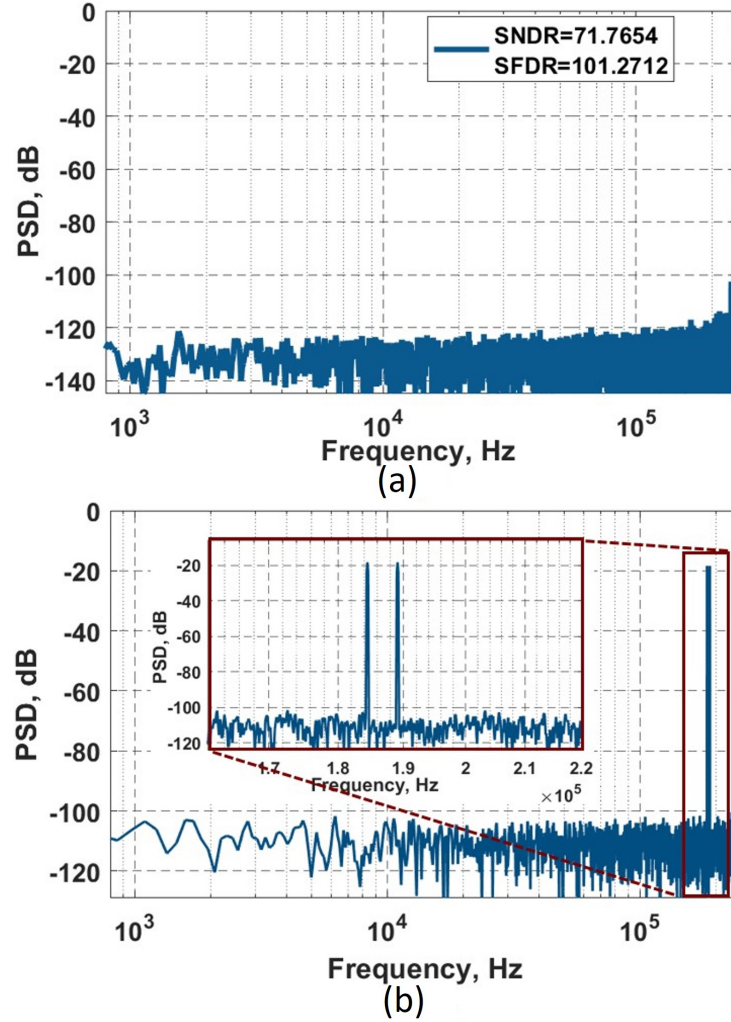


Figure 4.50: (a) Measured ADC output spectrum, 16384 point-FFT, $F_{in} = 249.9694824$ kHz with full scale input range and (b) Two-tone test, 4096 point-FFT, 184.448 Hz and 189.0897 Hz, with -4.1 dBFS each.

4.12 Summary

This chapter introduced a switched-supply dynamic comparator that, by means of a reservoir capacitor, exhibits a reduced effective supply voltage during the decision phase without requiring a dedicated DC-DC down converter or external supply rail. The proposed switched-supply comparator achieves a 28% reduction in power consumption compared to the conventional dynamic comparator design. An ultra-low power 14-bit SAR ADC was implemented using the proposed switched-supply comparator, where the bootstrap switch is also replaced with a clock-boosting switch, enabling further power consumption reduction without compromising the achievable SNDR. The ADC was fabricated in a 65 nm CMOS and consumes 9.14 μ W from a 1 V supply and achieves a constant SNDR of 71.7 dB from DC to 0.5 MS/s. The resulting resolution, speed, and state-of-the-art Walden FoM of 5.7 fJ/Conv make this ADC suitable for low-power portable biomedical devices, which was presented at the 2023 BioCAS Conference [135].

Chapter 5 will present the design and analysis of a programmable switched-supply comparator that uses a programmable reservoir capacitor. This design provides the advantage of programming the input-referred noise and power consumption at any clock cycle and can eliminate the need for coarse and fine comparators in two-comparator SAR ADCs without requiring offset calibration.

Chapter 5

Programmable switched-supply comparator

5.1 Introduction

The growing demand for wearables and battery-powered systems has spurred a need for inventive approaches to achieve ultra-low-power data converters. Amid the various architectural choices, SAR ADCs stand out for their remarkable efficiency. Moreover, the quasi-all-digital characteristics of this topology make it exceptionally adaptable to technological scaling, while its simple structure is well-suited for integration into more complex system-level designs. However, their energy efficiency is usually limited by the comparator [71] [97] [77]. Additionally, alongside the capacitive DAC, the comparator determines the overall ADC noise performance. Gaining one bit of noise reduction in the comparator typically increases the power consumption by at least a factor of 4. To address the noise and area challenges posed by the comparator, solutions have been proposed at both the circuit and system levels.

5.2 Prior Art

At the circuit level, the StrongARM latch comparator [98] benefits from strong positive feedback, enabling fast decisions, and has no static power consumption. However, due to its single-stage configuration, it requires a large voltage headroom. The dual-tail dynamic latch comparator [101] is a two-stage architecture that mitigates these issues by separating the pre-amplifier stage from the latch. This architecture suffers from suboptimal energy consumption as both the pre-amplifier and the regenerative latch start operating simultaneously, making it less suitable for low-power, medium-resolution SAR ADCs. Elzakker’s comparator [71], addresses this problem and enhances the energy consumption by delaying the conduction of the

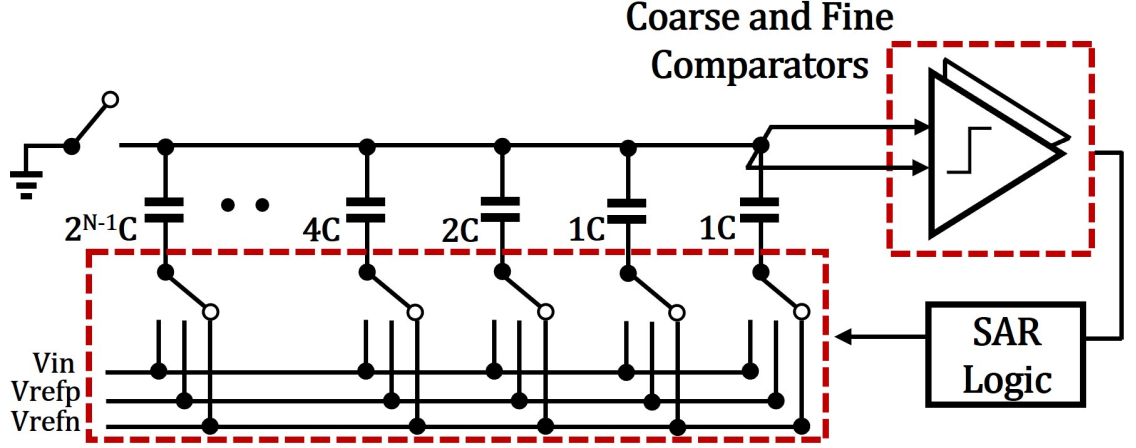


Figure 5.1: The two comparator SAR ADC architecture.

latch stage until a sufficient voltage gain has been achieved across the pre-amplifier's output. The dynamic bias comparator [103] employs source degeneration and prevents the full discharge of the integration capacitors in the preamplifier, reducing the energy per conversion compared to [71], at the cost of a larger area. The dynamic comparator presented in [105] incorporates cross-coupled devices at the input of the differential pair, preventing the pre-amplifier's internal nodes from completely discharging to ground. This design reduces energy consumption but limits the design's ability to migrate to lower power rails. The Dynamic Floating Inverter based comparator [104] uses an inverter-based input pair powered by a floating reservoir capacitor. This setup realises the dynamic bias described in [77] and employs current reuse, reducing the energy per conversion. A more detailed analysis of these comparators was presented in Section 3.4. Lastly, the switched-supply comparator discussed in Chapter 4 applies the concept of a reservoir capacitor to the dynamic comparator, lowering the effective supply voltage and power consumption of the comparator. Such a design trades off power consumption, input-referred noise, and speed.

At the system-level, one noise mitigation technique consists of the use of majority voting [70], averaging the comparator noise over multiple comparator decisions at the expense of the ADC operating frequency. Another system-level solution involves using two comparators (coarse and fine) [136] as depicted in Figure 5.1. In this approach, the comparator responsible for the MSB decisions is a low-power comparator with relaxed noise specifications, whereas the comparator in control of the LSB conversions is low-noise with increased power budget and delay time. In this way, the power-hungry and low-noise comparator has only to be used for a few conversions during the LSB decisions. However, the mismatch between the two comparators introduces new undesirable effects in the SAR ADC such as offset mismatch that

requires calibration [136]. Providing a large redundancy can help correct the offset mismatch; however, this approach leads to increased power consumption.

5.3 Programmable switched-supply comparator

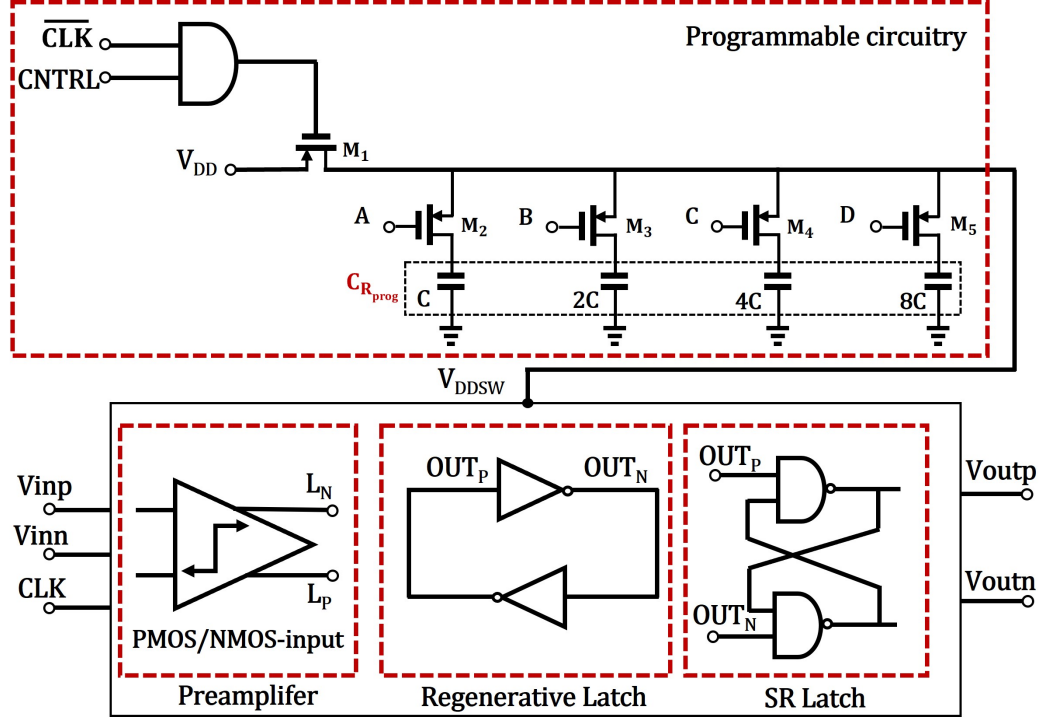


Figure 5.2: Proposed programmable switched-supply comparator.

The proposed programmable comparator solution caters to both the circuit and the system-level requirements for the two-comparator ADC. The proposed comparator employs a programmable reservoir capacitor, enabling dynamic adjustment of its input-referred noise and power during the conversion cycle. This avoids the mismatch issues inherent in the two-comparator architecture while enabling a robust comparator whose performance can be tuned as it transitions through the bit trials.

As discussed in Section 4.2, where a switched-supply comparator was presented, the introduction of C_R assists in limiting the effective voltage at which the comparator operates during the decision phase. The reduced supply voltage not only reduces power consumption, but also affects input-referred noise [99] [100] and speed, as discussed in Chapter 4.

The proposed programmable switched-supply comparator is depicted in Figure 5.2, with binary-weighted capacitors and their control signals (A, B, C, D), allowing the configuration of the comparator's power and noise parameters to be controlled in a dynamic manner.

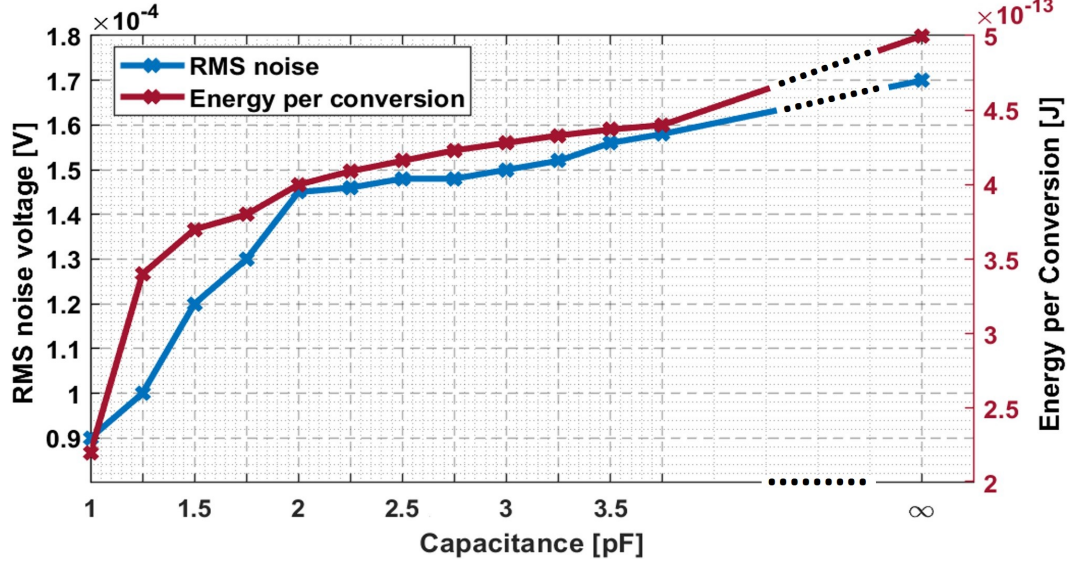


Figure 5.4: RMS noise and energy per conversion for different values of reservoir capacitance for a PMOS-input comparator (simulation procedure is explained in Appendix B.3).

the output common mode voltage and C_{total} is the total capacitance (i.e., $C_{R_{prog}} + 2C_P$). From expressions (5.1) to (5.3), it can be seen that by adjusting the number of capacitors connected to form $C_{R_{prog}}$, the energy per conversion can be adjusted, along with the input-referred noise. Interestingly, when the energy per conversion decreases, the noise also decreases. To illustrate this, transistor-level simulations were carried out. The simulated energy per conversion and input-referred noise for different values of $C_{R_{prog}}$ are depicted in Figure 5.4. Note that as $C_{R_{prog}}$ becomes smaller, the energy efficiency and the input-referred noise improve. However, this decrease has a lower limit since the reduced pre-amplifier bandwidth makes the overall amplification slower, reducing the available time for the latch to trigger.

Figure 5.5, depicts the time-domain signals at the various nodes, illustrating the increased amplification time for low values of $C_{R_{prog}}$. The analysis presented here shows that as long as the time constraints are met, the programmable comparator can be used as both a coarse and a fine comparator, where the noise levels can be adjusted at any clock cycle. This makes the programmable comparator an excellent solution for the SAR ADC architecture of [136], where the two comparators can be replaced with a single programmable one.

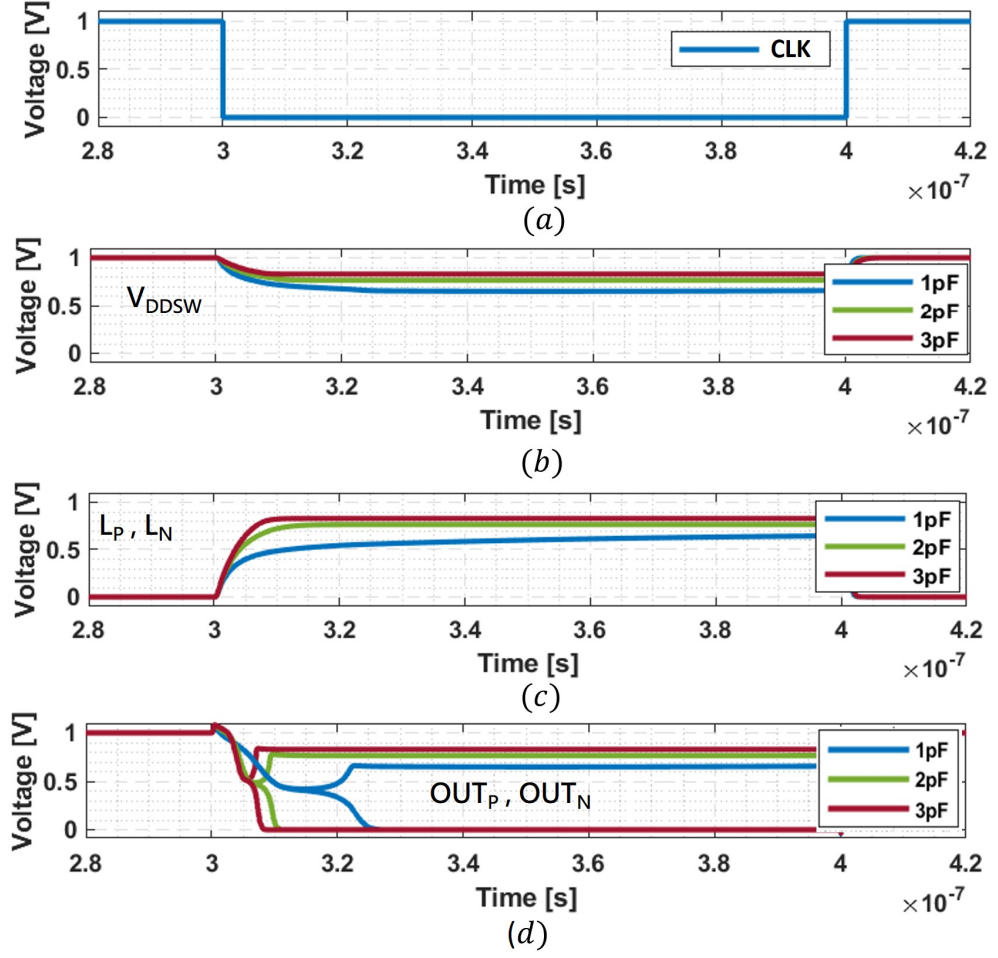


Figure 5.5: Simulated timing diagram of the PMOS-input comparator with 100 μ V input differential voltage for three different values of reservoir capacitance: (a) Applied clock, (b) Equivalent V_{DD} , (c) Pre-amplifier output, and (d) Regenerative latch output.

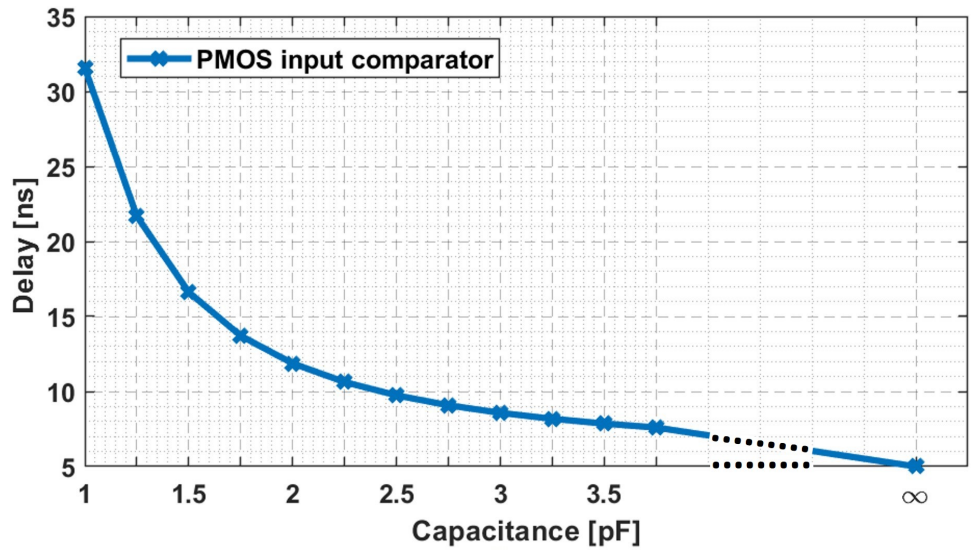


Figure 5.6: Simulated comparator delay as a function of reservoir capacitance for a PMOS-input with $V_{CM} = 0.35$ V.

The PMOS-input comparator delay is shown in Figure 5.6. The “ ∞ ” symbol on the x-axis represents the delay when $C_{R_{prog}}$ is disabled (i.e., when CNTRL = 0) and the blocks are powered directly from V_{DD} . As expected, small values of C_R lead to reduced power consumption in the proposed comparator. However, this comes at the expense of reduced operating speed. Figure 5.7 illustrates the layout of programmable switched-supply PMOS-input comparator with a size of $109.5 \mu\text{m} \times 43.73 \mu\text{m}$.

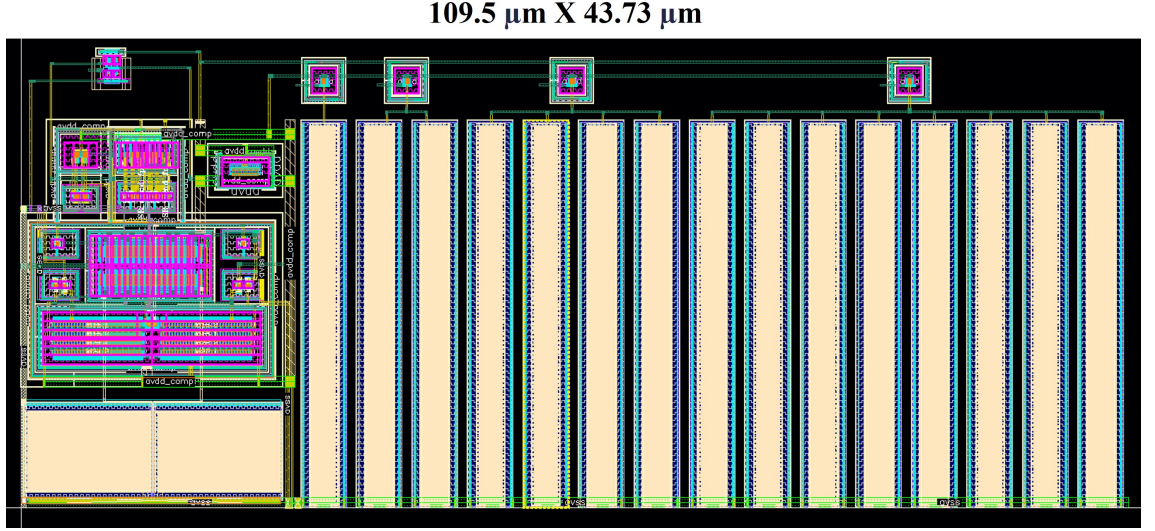


Figure 5.7: Layout of programmable switched-supply PMOS input comparator.

5.5 NMOS-input programmable comparator

5.5.1 Design and simulation

The proposed programmable switched-supply technique was also applied to the NMOS-input comparator in order to investigate its performance with respect to $C_{R_{prog}}$ as shown in Figure 5.8. The time domain simulation of the NMOS-input comparator internal nodes are depicted in Figure 5.9. It can be seen that integration ceases when the output nodes of the pre-amplifier reach $(V_{DDSW} - V_{TH})$ which is lower than $(V_{DD} - V_{TH})$. As a result, the integration gain is constrained by the bounded output common-mode voltage drop. This leads to a decreased integration gain and an increased noise bandwidth, resulting in a higher input-referred noise voltage.

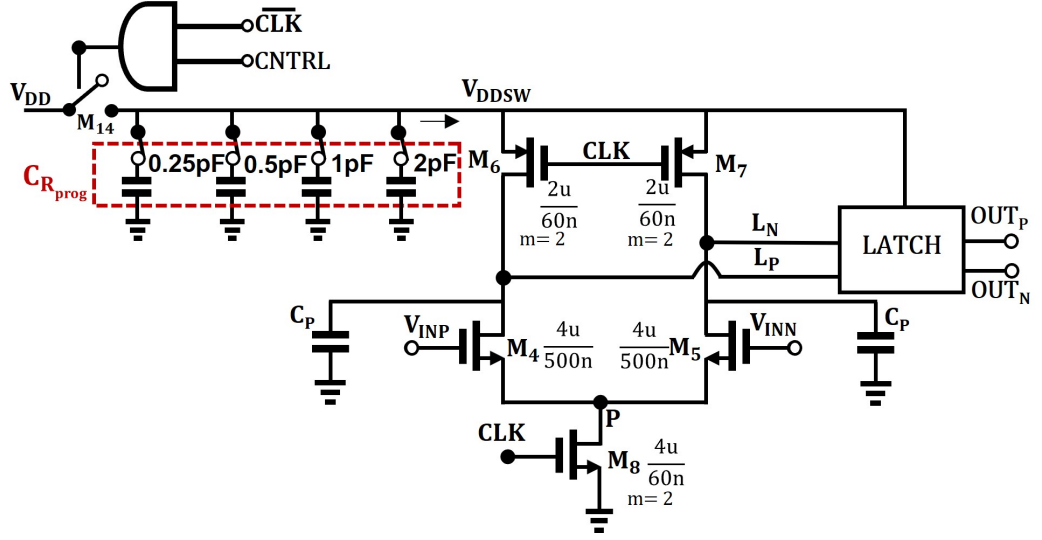
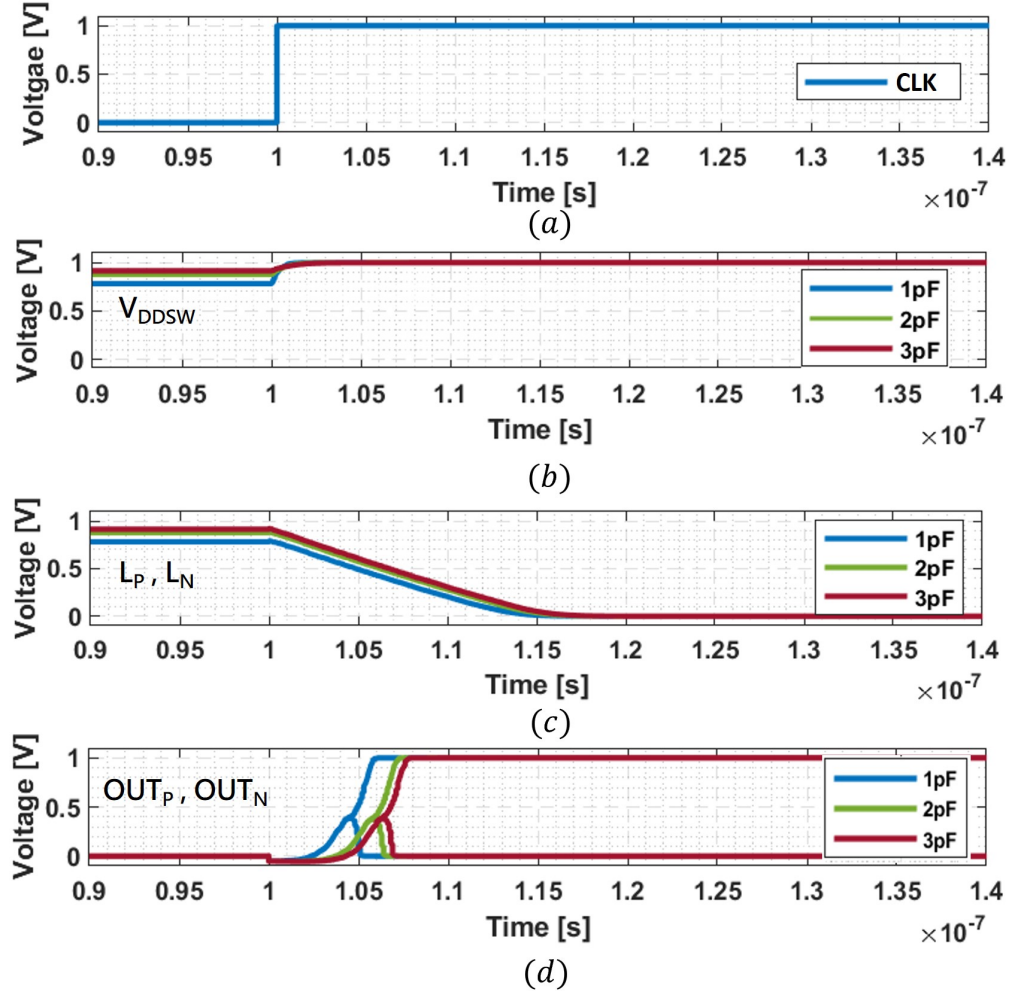


Figure 5.8: Proposed programmable comparator with NMOS-input pre-amplifier.


 Figure 5.9: Simulated timing diagram of an NMOS-input comparator with 100 μV input differential voltage for different values of reservoir capacitance: (a) Applied clock, (b) Equivalent V_{DD} , (c) Pre-amplifier output, (d) Regenerative latch output.

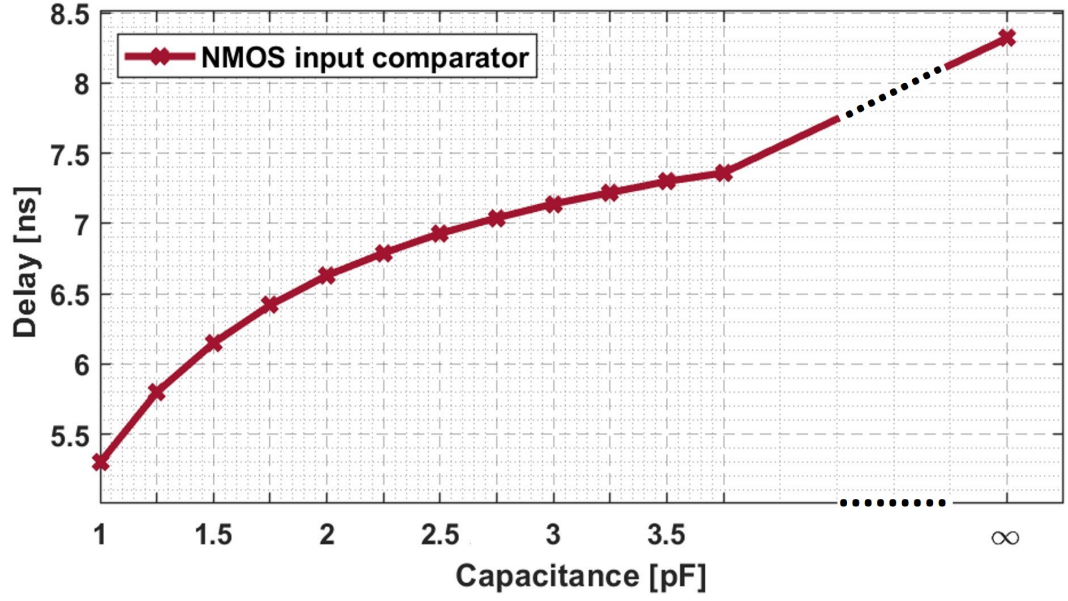


Figure 5.10: Simulated comparator delay as a function of reservoir capacitance for PMOS-input with $V_{CM} = 0.5$ V.

The NMOS-input comparator delay is shown in Figure 5.10. The " ∞ " symbol on the x-axis represents the delay when $C_{R_{prog}}$ is disabled (i.e., when CNTRL = 0) and the blocks are powered directly from V_{DD} . It is evident from Figure 5.10. that there is no significant improvement in delay for the NMOS-input comparator when V_{DDSW} is reduced during the reset phase. It can be concluded that by adding a programmable switched-supply to the NMOS-input comparator, no significant benefits can be achieved. Figure 5.11 illustrates the layout of the programmable switched-supply NMOS-input comparator with a size of $109.5\mu\text{m} \times 43.73\mu\text{m}$.

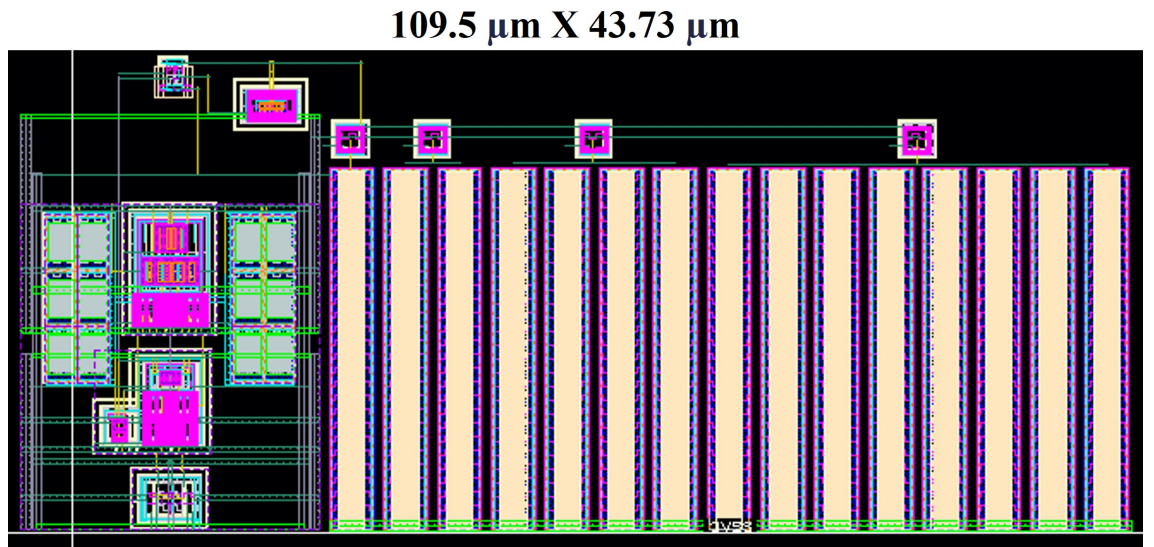


Figure 5.11: Layout of programmable switched-supply NMOS input comparator.

5.6 Full chip

Decoupling capacitors have been added to each supply rail to filter out unwanted signals from the power supply and minimise the effects of current spikes on the bondwires as shown in the full chip layout in Figure 5.12. To meet design rule density requirements, all the remaining blank space has been filled with dummy metal, OD, and poly layers (not displayed in Figure 5.12 for clarity).

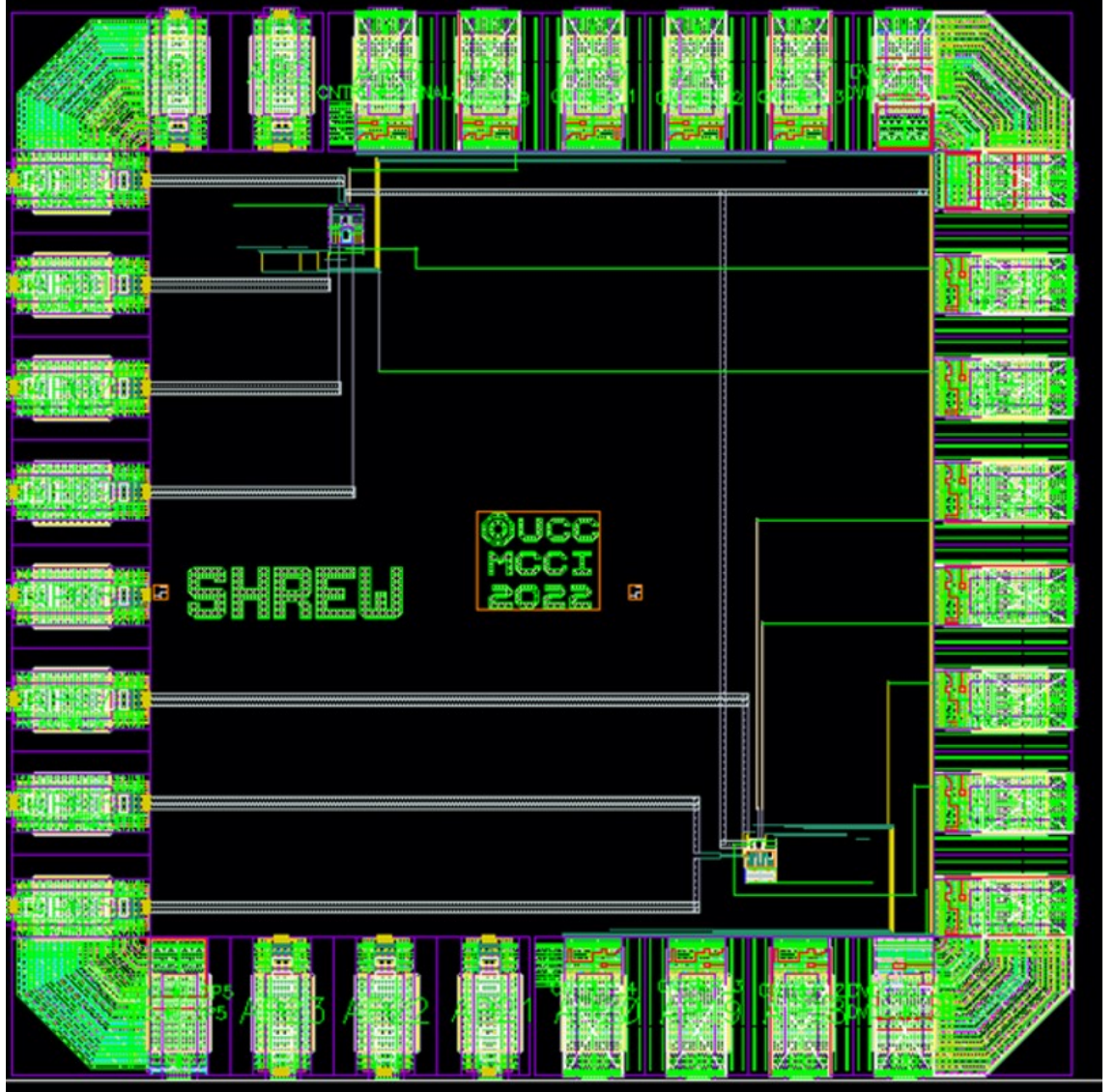


Figure 5.12: Layout of full chip (PMOS-input and NMOS-input programmable comparators) and I/O ring with bondpads.

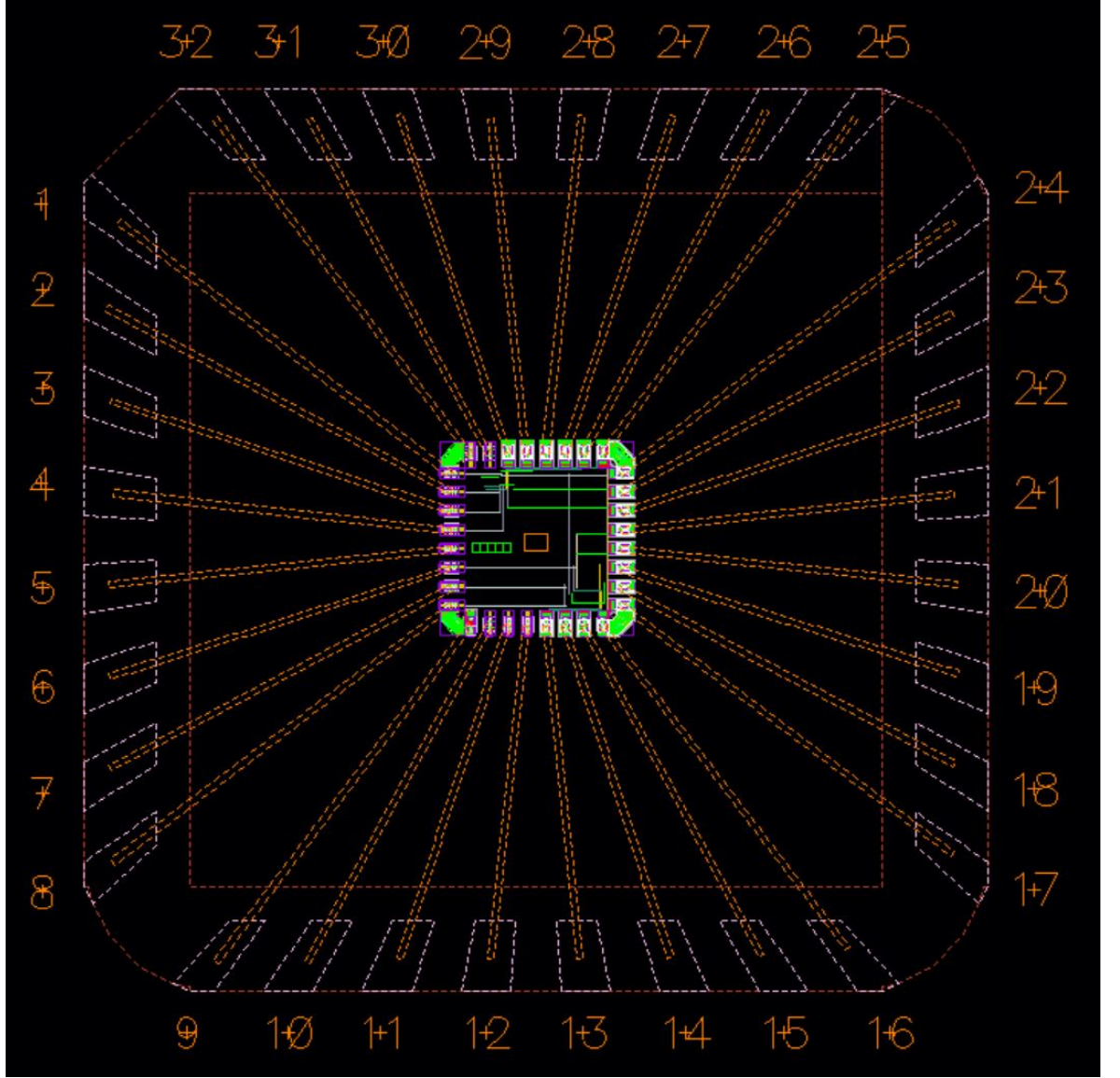


Figure 5.13: Bonding diagram of full chip (PMOS-input and NMOS-input programmable comparator) and I/O Ring with bondpads.

The completed die is packaged in a 32-pin Quad Flat No-leads (QFN) package as illustrated in the bonding diagram in Figure 5.13.

5.7 Measurement results

The programmable comparators (both NMOS-input and PMOS-input) were designed and fabricated on the same die in a standard 65nm CMOS process [137]. Figure 5.14, shows the die micrograph of the proposed comparators, with each comparator having an area of $109.5 \mu\text{m} \times 43.73 \mu\text{m}$ including $C_{R_{prog}}$. The measurement and evaluation setup for testing the switched-supply programmable comparator is shown in Figure 5.15.

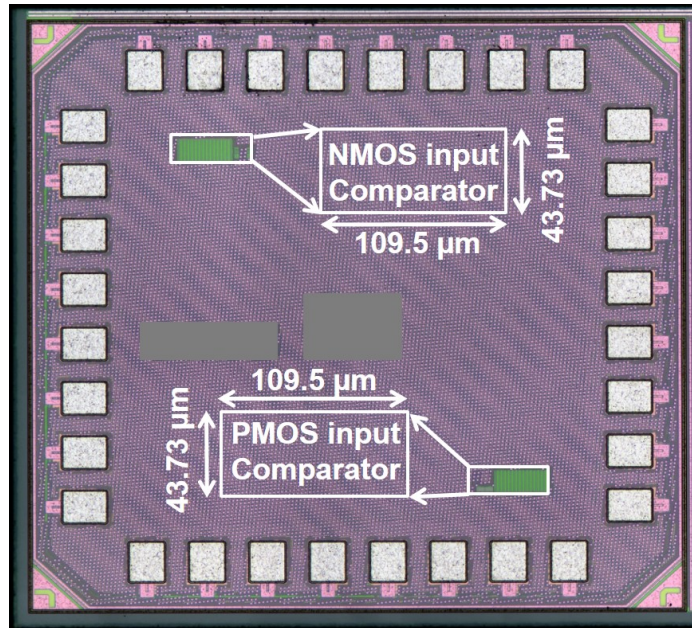


Figure 5.14: Die micrograph.

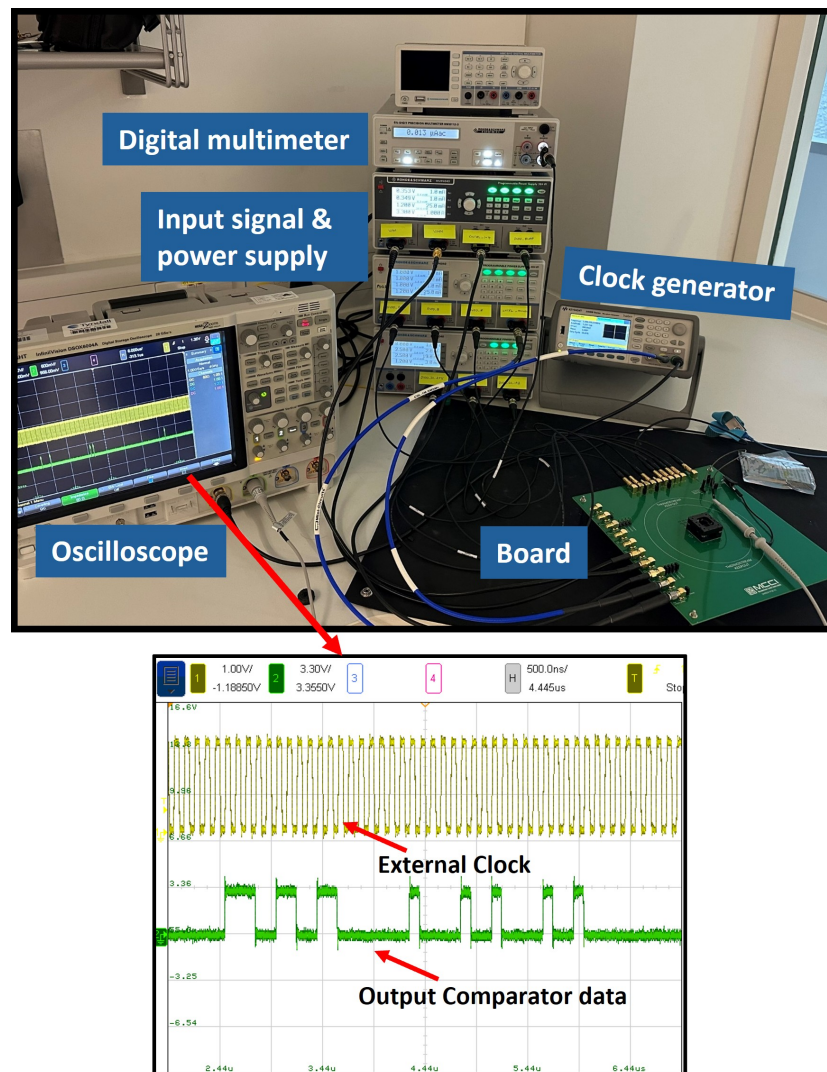


Figure 5.15: Measurement setup for programmable switched-supply comparator.

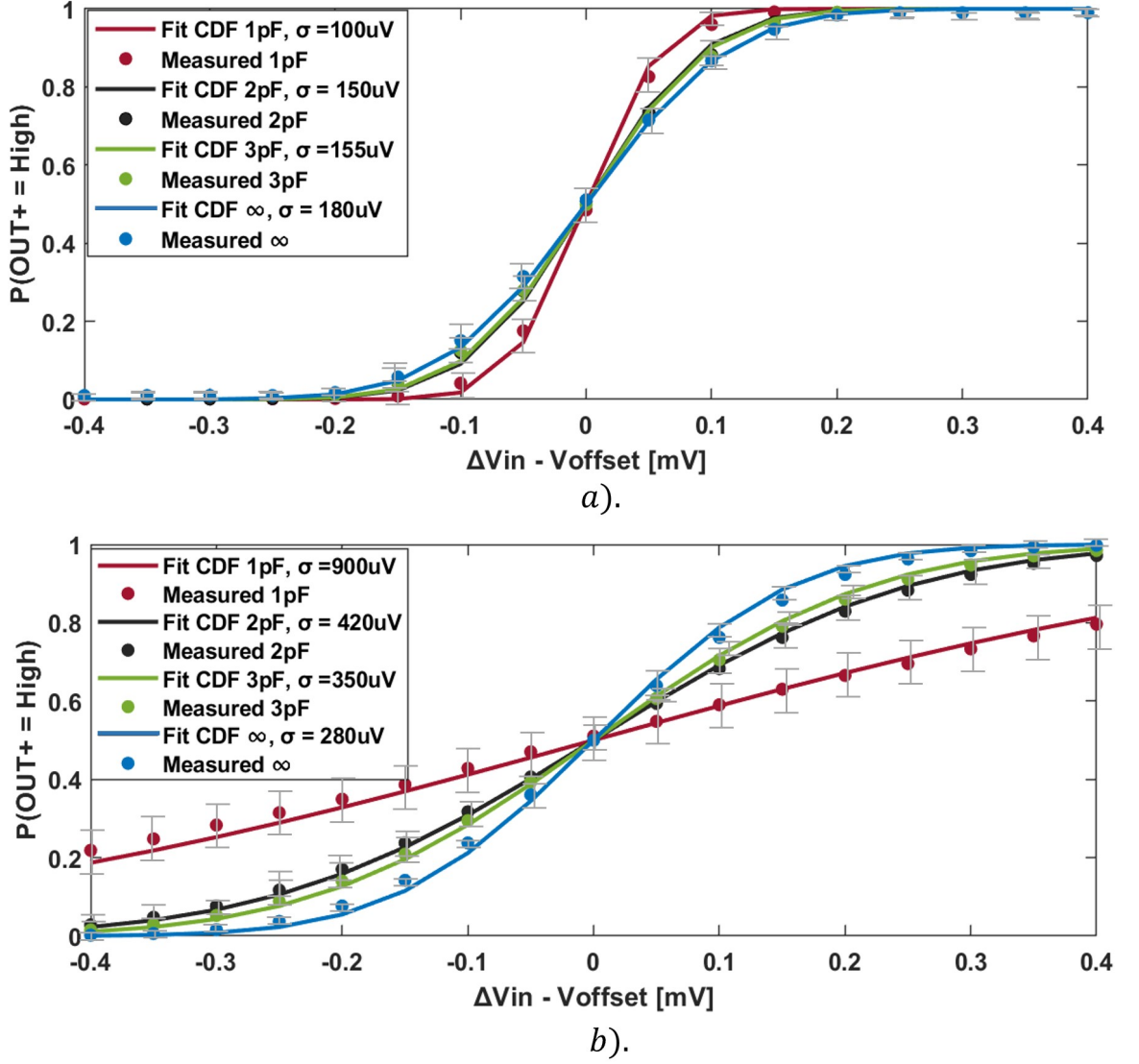


Figure 5.16: Measured cumulative probability density distribution and fit to Gaussian distribution for varying reservoir capacitor values for (a) PMOS-input switched-supply comparator $V_{CM} = 0.35$ V and, (b) NMOS-input switched-supply comparator with $V_{CM} = 0.5$ V.

Figure 5.16 shows the measured input-referred noise for both the PMOS-input and the NMOS-input comparators by measuring the average number of positive decisions against an applied ΔV_{in} . Fitting these measurements to the normal cumulative distribution function (CDF) provides the input-referred rms noise. The grey tick marks in Figure 5.16 highlight the spread of the probability of positive decisions measured at five different time instances.

The measured input-referred rms noise voltage has been tabulated for various values of $C_{R_{prog}}$ for both the PMOS-input and the NMOS-input comparators. For the PMOS-input comparator, the measured rms noise levels are 100 μ V, 150 μ V and 155 μ V for $C_{R_{prog}}$ values of 1 pF, 2 pF and 3 pF respectively and 180 μ V when powered directly from V_{DD} . This behaviour in the PMOS-input comparator arises

from the reduction in $C_{R_{prog}}$, leading to longer integration times and reduced noise bandwidth. Notably, when ΔV_{in} is equal to zero for different $C_{R_{prog}}$ values, the mean value is zero. This demonstrates that the offset is independent of $C_{R_{prog}}$. For the NMOS-input comparator, the rms noise levels are 900 μV , 420 μV and 350 μV for $C_{R_{prog}}$ values of 1 pF, 2 pF and 3 pF respectively and 280 μV when powered directly from V_{DD} . This behaviour in the NMOS-input comparator is attributed to the decrease in supply voltage as $C_{R_{prog}}$ is reduced during the reset phase.

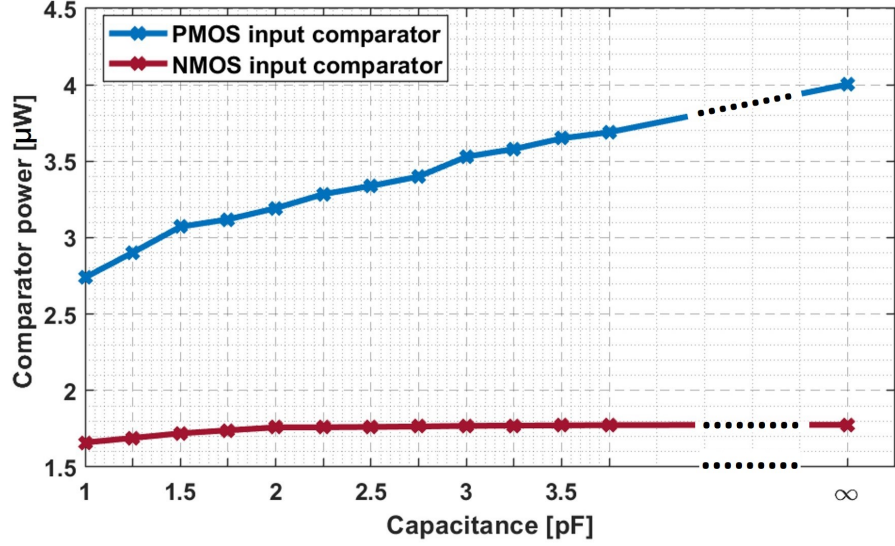


Figure 5.17: Measured plot of power dissipation with respect to reservoir capacitance for PMOS-input and NMOS-input comparators.

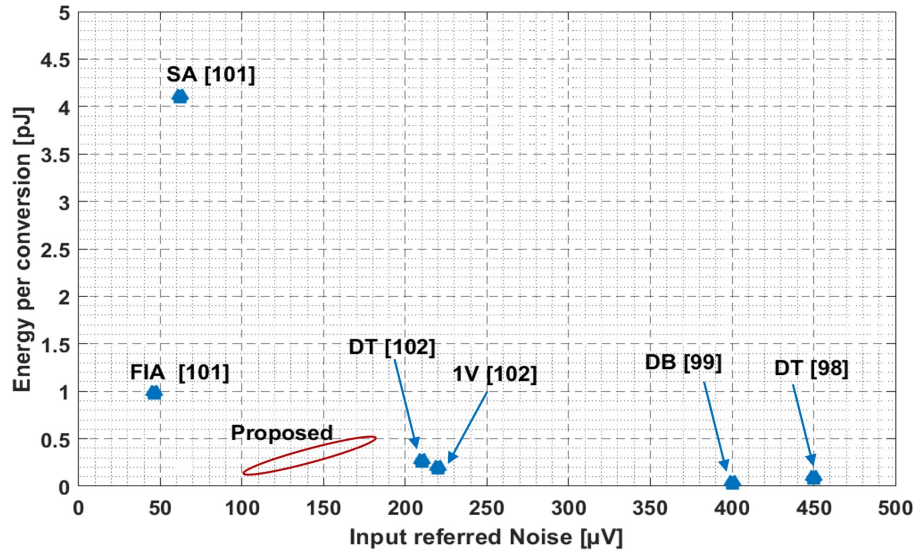


Figure 5.18: Comparison with the state-of-the-art in terms of energy per conversion and Input referred noise, with references [101], [102], [99], and [98]

Figure 5.17 illustrates the measured power dissipation for the PMOS-input and the NMOS-input comparators. The PMOS-input comparator consumes 4.1 μW

when the programmable circuitry is disabled and $2.74 \mu\text{W}$ when enabled, achieving up to a 50% reduction in power consumption. Figure 5.18. shows the input-referred noise with respect to energy per conversion in the state of art. The proposed programmable PMOS-input switched-supply comparator achieves an energy per conversion of $0.22 \text{ pJ} - 0.5 \text{ pJ}$ for an input referred noise of $100 \mu\text{V} - 180 \mu\text{V}$. Figure 5.19 illustrates the power consumption relative to reservoir capacitance for 10 dies for the PMOS-input comparator, while Figure 5.20 presents the same for the NMOS-input comparator. From Figure 5.19 and Figure 5.20, it is clear that the power consumption performance across the dies remain consistent.

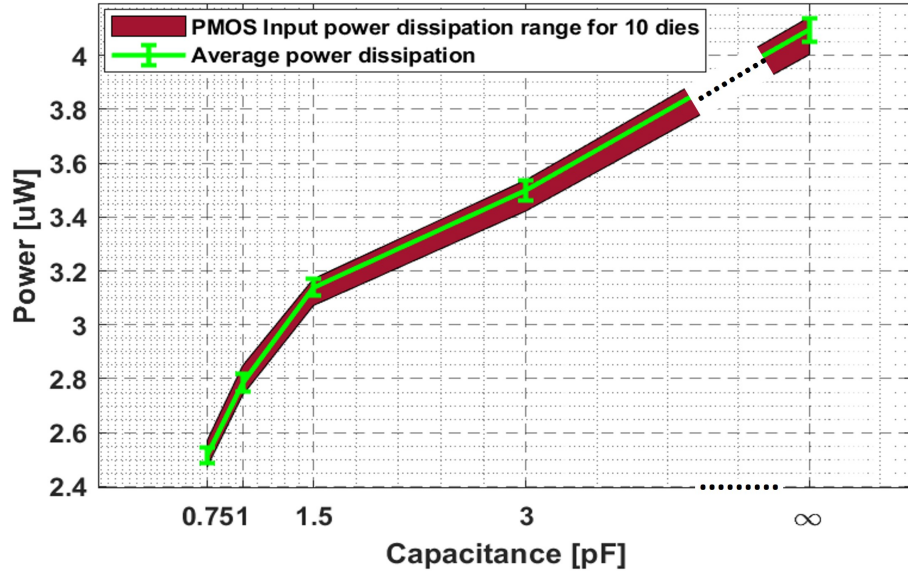


Figure 5.19: Plot of measured power for the PMOS-input comparator with respect to reservoir capacitance for a sample of 10 die samples.

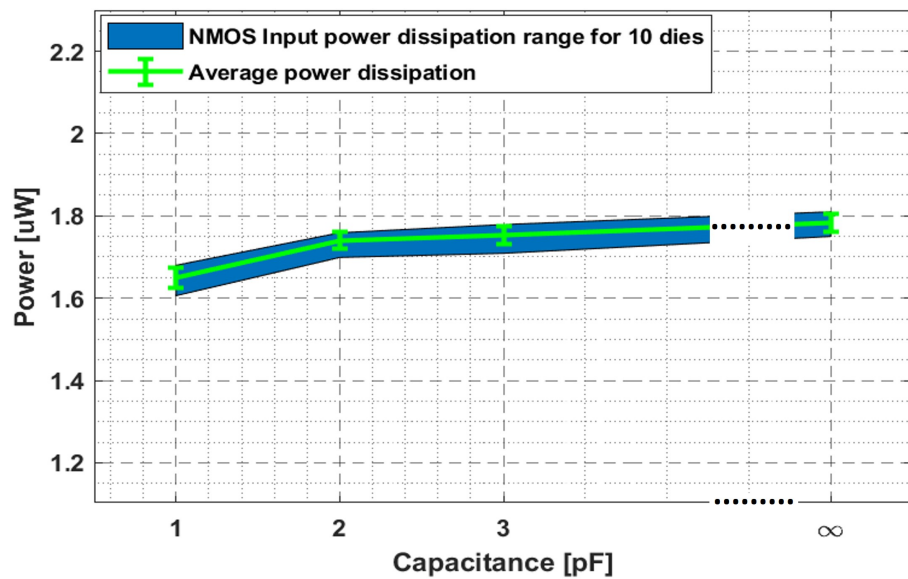


Figure 5.20: Plot of measured power for NMOS input comparator with respect to reservoir capacitance for a sample of 10 dies.

5.8 Summary

This chapter described the design and analysis of a programmable switched-supply comparator that uses a programmable reservoir capacitor to achieve a reduced effective supply voltage during the decision phase without the need for a dedicated DC-DC down converter or external supply rail. The proposed comparator achieved a reduction in power consumption of up to 50% compared to the conventional dynamic comparator. The proposed design was fabricated in a 65nm CMOS process. The silicon-based results of the PMOS-input programmable comparator show programmable power consumption and energy efficiency ranging from 2.7 - 4.1 μW and 0.22 - 0.5 pJ/Conv, respectively. Similarly, the input-referred noise can be programmed from 100 - 180 μV_{rms} , achieving an almost 2-x reduction in noise. Furthermore, power consumption and input-referred noise can be programmed at any clock cycle, making this design an ideal solution for the two-comparator SAR ADC architecture. which was presented at the 2024 ISCAS Conference [137].

Chapter 6 will present the design and simulation of the SAR ADC using a programmable switched-supply comparator, compare it with the SAR ADC without the programmable switched-supply comparator, and tabulate its performance in terms of power consumption and signal-to-noise ratio.

Chapter 6

SAR ADC based on programmable switched-supply comparator

6.1 Introduction

This chapter presents the details of a 14-bit, low-power, 277 kS/s SAR ADC using the programmable switched-supply comparator, implemented in a 65nm CMOS process. It explains the design and integration of the programmable switched-supply comparator within the SAR ADC, replacing the coarse and fine comparators in a two-comparator SAR ADC architecture to address mismatch issues and reduce power consumption.

6.2 Comparator power reduction and SAR architectural level power reduction

Recent developments in analog and mixed signal design for battery operated devices emphasise the need for cost-effective, power-efficient ADCs. SAR architectures have strong potential in delivering high power efficiency for applications requiring moderate resolution and medium bandwidth [138]. However, in SAR ADCs, where the comparator plays a crucial role in determining the overall performance, thermal noise in the comparator can significantly restrict the maximum achievable resolution.

In addition to designing an energy-efficient comparator as discussed in detail in Chapters 4 and 5, the architectural characteristics of a SAR ADC can be leveraged to decrease the overall comparator power consumption. In an N-bit SAR ADC, the comparator is activated N times, but the noise requirements for each comparison vary. When the comparator input is small, low noise is essential to ensure an accurate

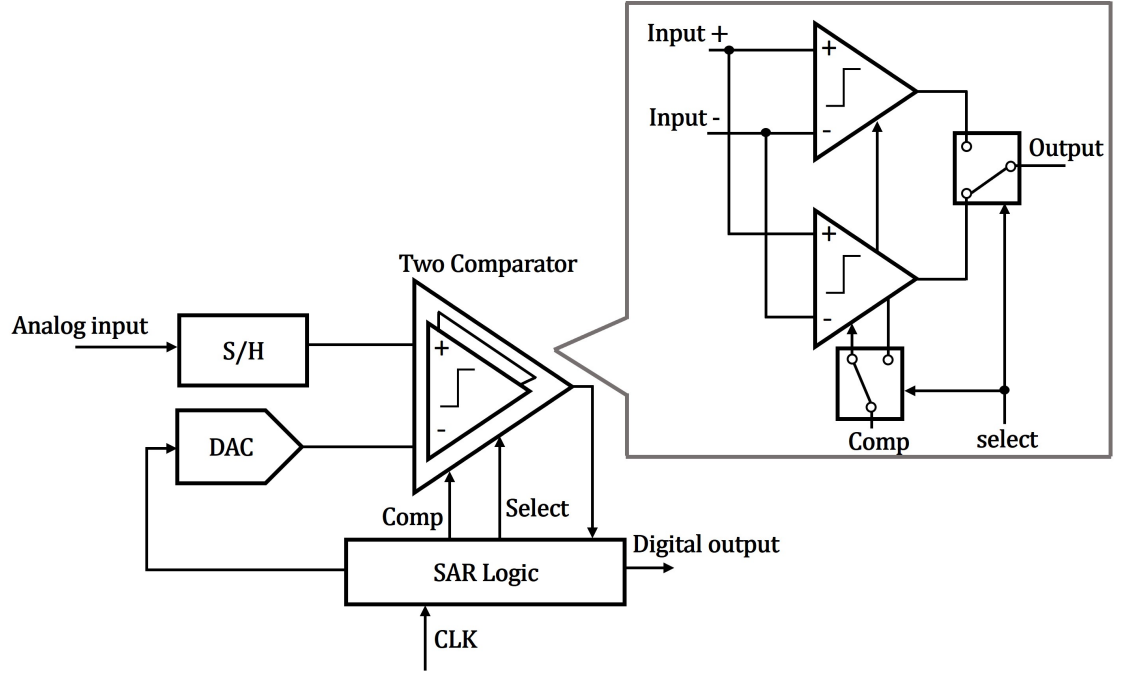


Figure 6.1: The two comparator SAR ADC architecture.

decision. Conversely, with a larger input, the noise tolerance can be significantly relaxed while still achieving the correct outcome. It is important to note that among the N comparisons, the comparator input is less than $\text{LSB}/2$ only once; for all other comparisons, the noise requirements can be relaxed to conserve energy. However, a significant challenge is that it is impossible to predict when the critical decision will occur because it depends on an unknown input.

A commonly used approach involves introducing redundancy into the SAR search algorithm, which enables corrections of earlier decision errors later during the conversion. This redundancy allows the system to tolerate a range of errors, such as comparator noise and DAC settling errors, provided that they are within the allowable redundancy range. Effectively, this shifts the most critical comparisons to the LSB decisions.

In [136], the authors introduced a two-comparator architecture that incorporates redundancy [139–142], as illustrated in Figure 6.1. In this approach, the last two bit decisions, including the redundant bit, utilise a low-noise comparator to ensure conversion accuracy, while the earlier $(N-1)$ bit decisions rely on a higher-noise, low-power comparator to conserve energy. The fine comparator is designed with input-referred noise levels that are half of those of the low-power comparator. Rough estimates suggest that the low-noise comparator consumes four times more power than the low-power comparator. In contrast to conventional designs, where all N bit decisions require a low-noise comparator, this method activates it only twice, reducing the total comparator power consumption by approximately 55% in a 9-bit

SAR ADC. However, this design faces challenges due to offset mismatches between the two comparators, which requires calibration. Although it is possible to provide greater redundancy to correct these mismatches, doing so would necessitate larger redundancy in a more significant bit, increasing the number of low-noise comparisons and ultimately reducing energy efficiency.

6.3 Schematic implementation

With the use of the programmable comparator implemented in Chapter 5 in the SAR ADC implemented in Chapter 4 those issues can be mitigated and a low power comparable performance can be achieved. The SAR ADC discussed in Chapter 4 and the programmable comparator discussed in Chapter 5 are reused in this design to implement the programmable switched-supply comparator-based ADC. The block diagram of the implemented 14-bit SAR architecture is shown in Figure 6.2, which is similar to SAR architecture discussed in Chapter 4, except that the switched-supply comparator is replaced with the programmable switched-supply comparator discussed in chapter 5.

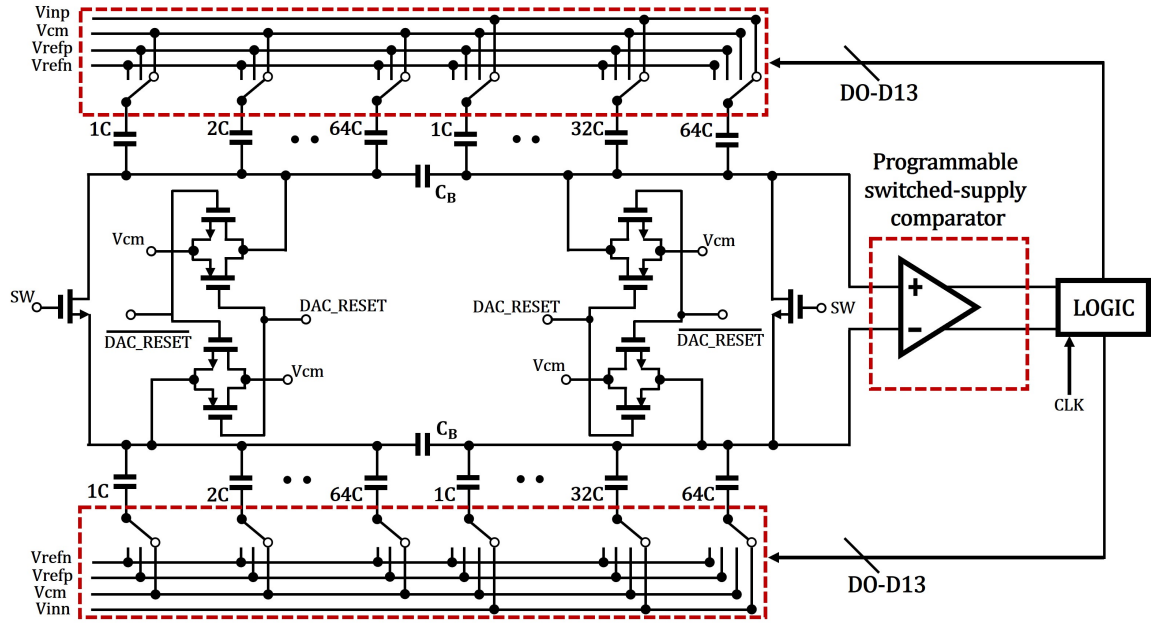


Figure 6.2: Block diagram of the implemented 14-bit SAR ADC using a programmable switched-supply comparator.

6.4 Simulation results

The timing diagram of the SAR ADC employing the programmable switched-supply comparator is illustrated in Figure 6.3. The programmable switched-supply com-

parator is disabled during the first four MSB decisions, as the comparator responsible for these MSB decisions is a standalone PMOS-input dynamic comparator with relaxed noise specifications.

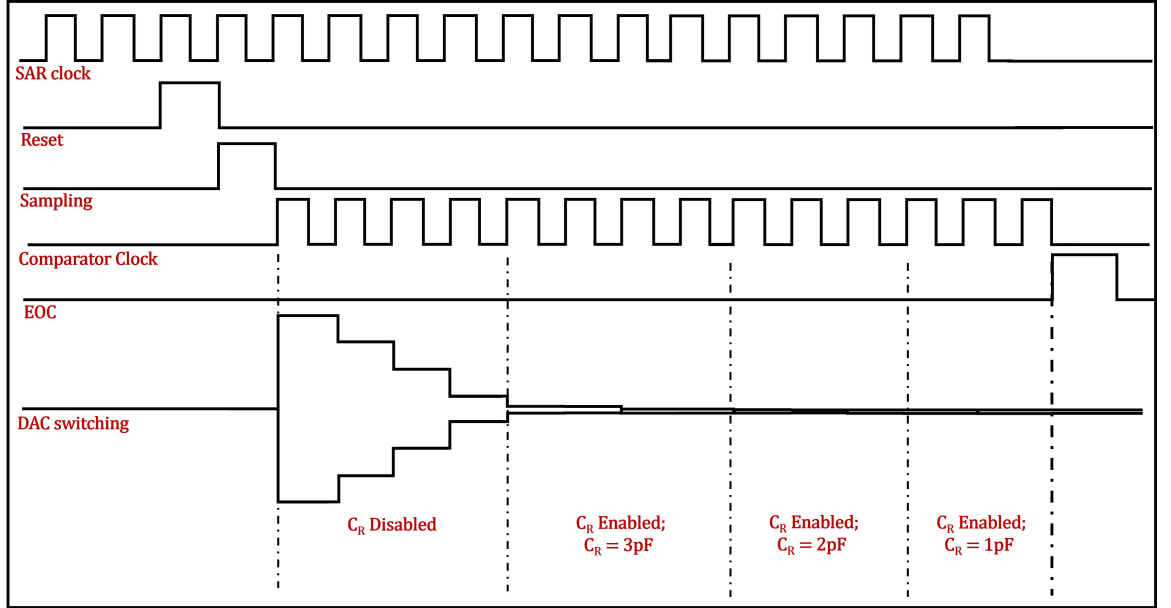


Figure 6.3: Timing diagram of the programmable switched-supply based SAR ADC

After the first four MSB decisions, the programmable switched-supply comparator is enabled to provide improved noise specifications ($C_R = 3\text{pF}$) for the next three decisions, followed by ($C_R = 2\text{pF}$) and ($C_R = 1\text{pF}$) for the remaining SAR decisions. As discussed in Chapter 5, as C_R becomes smaller, the energy efficiency and the input referred noise improve. However, this decrease has a lower limit since the reduced pre-amplification bandwidth also makes the overall amplification slower, reducing the available time for the latch to trigger. In the SAR ADC implemented, the internal SAR clock is set to 5 MHz to allow enough time to amplify signals and make the correct decisions when C_R is equal to 1pF.

Figure 6.4 shows the FFT of the simulated SAR ADC without the programmable switched-supply comparator, with the SAR clock running at 5 MHz for 4096 points. Figure 6.5 shows the FFT of the simulated SAR ADC with the programmable switched-supply comparator under the same conditions as Figure 6.4. From these two figures, it is evident that there is no degradation in the SNDR when the programmable switched supply comparator is toggled during the subsequent conversion of the SAR ADC. By utilising the programmable switched-supply comparator during the conversion process, instead of a standalone comparator, the comparator power is reduced by 30%, which subsequently reduces the overall power consumption of the SAR ADC. However, power consumption can be reduced by up to 50% (with more precise C_R selection for subsequent conversions) if the comparator is programmed

to 2 pF for the first 7 conversions and 1 pF for the remaining 7 conversions, while still maintaining similar SNR performance.

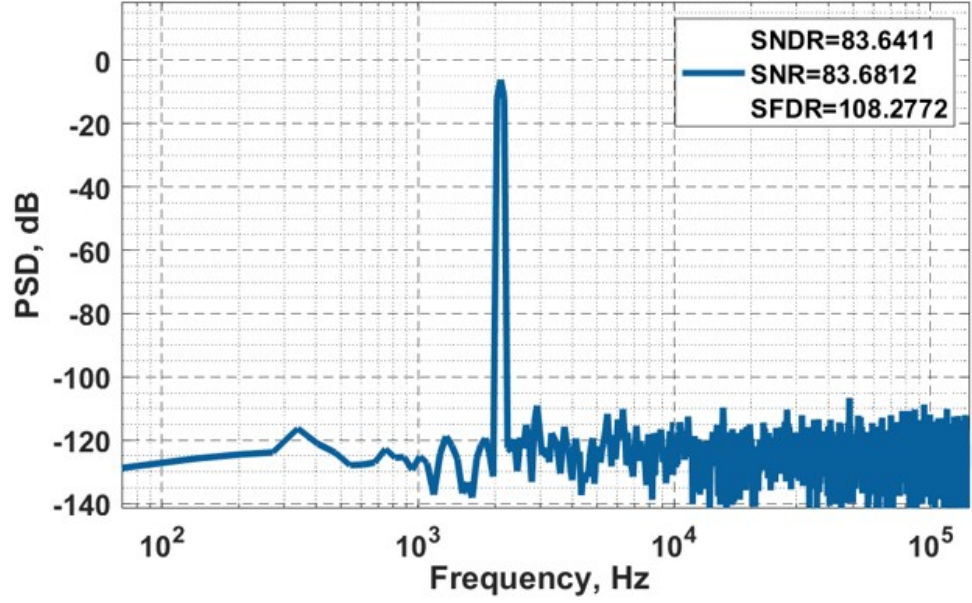


Figure 6.4: Simulated FFT of the SAR ADC without the programmable switched-supply comparator.

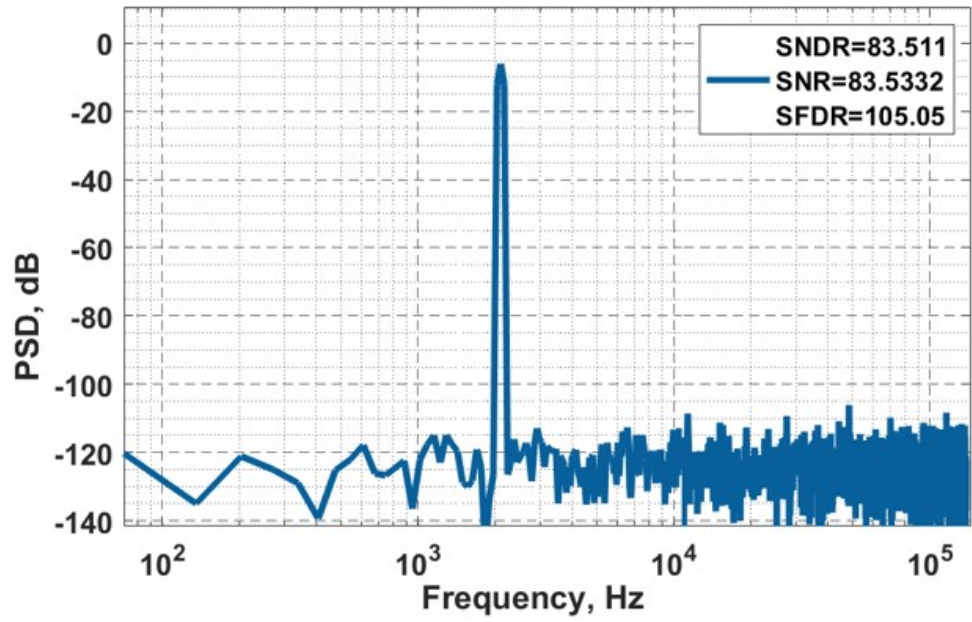


Figure 6.5: Simulated FFT of the SAR with the programmable switched-supply comparator.

6.5 Summary

This chapter presented the design and simulation of the programmable switched-supply comparator implemented in the SAR ADC and compared it to the SAR ADC

with a standalone PMOS-input dynamic comparator. It also compares performance in terms of power consumption and signal-to-noise ratio, replacing the coarse and fine comparators in a two-comparator SAR ADC architecture to address mismatch issues and reduce power consumption.

Chapter 7 presents the conclusions for the implemented SAR ADC discussed in Chapter 4, comparing it with the current state-of-the-art. It will also provide conclusions for the programmable switched-supply comparator introduced in Chapter 5, compare it with the current state-of-the-art, and outline its potential for future work.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

Analog-to-digital conversion is a critical component in sensing, signal acquisition, and data transmission systems. Over the years, the energy consumption of ADCs, particularly Successive Approximation Register (SAR) ADCs, has decreased significantly, achieving an impressively low Walden (FoM) of less than 1 fJ per conversion step.

The objective of this research was to design and implement a low-power, medium-resolution SAR ADC, and to propose design techniques aimed at reducing noise and power consumption in the key noise-contributing blocks, particularly for target resolutions exceeding 10 bits and also to achieve lowest Walden FoM.

This work demonstrates a switched-supply technique that can be used to achieve an ultra-low power SAR ADC. The switched supply technique reduces power consumption and achieves performance close to 12-bit resolution. The designed ADC has also shown comparable performance in terms of linearity, with no background calibration needed for capacitor mismatch, compared to other state-of-the-art SAR ADC's. Finally, the approach of using a clock boosting circuit instead of a bootstrapped switch on the input sampling switches has been validated, reducing power while still achieving an ENOB close to 12 bits.

The presented ADC achieves lower power consumption, comparable to the state of the art, making it a suitable option for sensor A/D interface systems. Table 7.1 summarises the specification achieved by this work, along with a comparison to the current state-of-the-art having similar sampling rates. Figures 7.1 and 7.2. illustrate how this work fits within the state-of-the-art.

Table 7.1: Performance summary and comparison table

Parameter	[71]	[143]	[144]	[95]	[94]	[145]	This Work
Technology [nm]	65	130	40	90	90	180	65
Supply [V]	1	1	1.1	0.4	0.4	1.8	1
Sample rate [S/s]	1M	0.6M	1M	0.27M	0.5M	1M	0.5M
Power [W]	1.9 μ	189n	31 μ	638n	500n	19.7m	9.14μ
SNDR [dB]	54.4	58.7	66.6	73.6	54.3	101.5	71.8
SFDR [dB]	–	70	100.4	90.6	–	–	101.2
FoMw [fJ/Conv-step]	4.42	0.4	17.7	0.6	2.4	202.8	5.7
FoMs [dB]	168.6	180.8	168.7	186.8	171.3	175.5	176.2
Input sampling	bootstrap	bootstrap	–	boosting	boosting	–	boosting

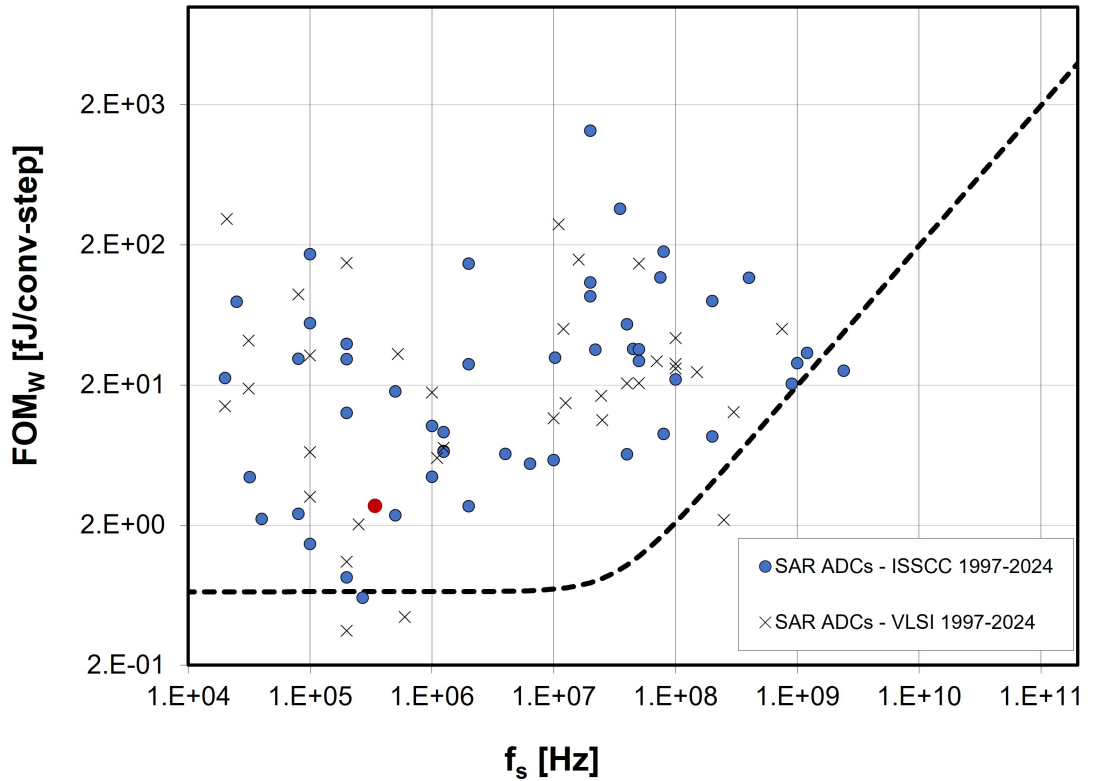


Figure 7.1: Walden FoM for recent SAR ADC publications (author's work in red).

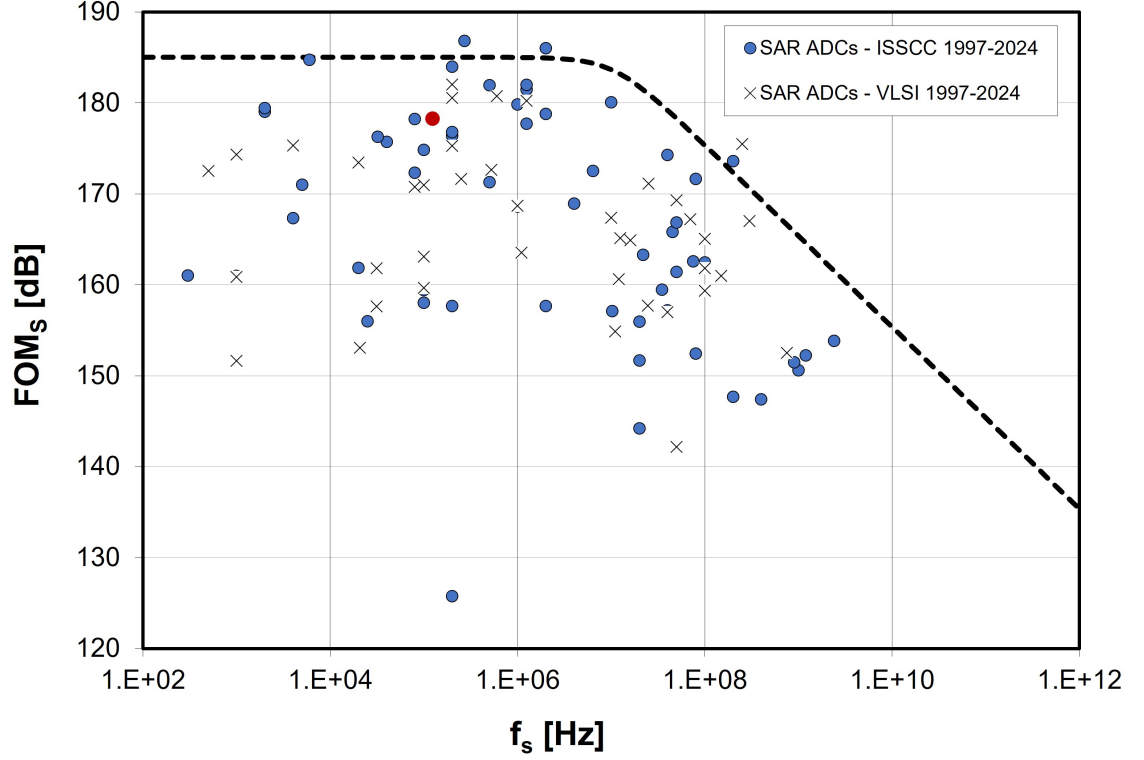


Figure 7.2: Schreier FoM for recent SAR ADC publications (author's work in red).

This work also demonstrates an energy efficient programmable switched-supply technique that can be used to achieve low power and low noise by leveraging longer integration times, which in turn results in reduced noise bandwidth, and consequently a lower input-referred noise voltage. Additionally, the proposed technique can eliminate the need for coarse and fine comparators in SAR ADCs when integrated with redundancy, addressing the issue of offset mismatch requiring calibration in the two-comparator architecture. For the first time, this work presents a comparator whose performance can be dynamically programmed from bit-to-bit-trial. These properties make programmable comparators an excellent design choice for low-power ADCs in IoT applications. Table 7.2 summarises the specifications achieved by this work, alongside a comparison to the current state-of-the-art.

7.2 Publications

The work outlined in this thesis has led to the following publications to date:

- M. Venkatesh, G. M. Salgado, K. G. McCarthy and I. O'Connell, "A 500 kS/s 71.8 dB 5.7 fJ/Conv-step Switch Supply Based Comparator SAR ADC for Biomedical Portable Devices," 2023 IEEE Biomedical Circuits and Systems

Conference (BioCAS), Toronto, ON, Canada, 2023, pp. 1-5, doi: 10.1109/BioCAS58349.2023.10388868.

- M. Venkatesh, G. M. Salgado, K. G. McCarthy and I. O’Connell, "A Low Power Programmable Switch Supply Dynamic Comparator," 2024 IEEE International Symposium on Circuits and Systems (ISCAS), Singapore, 2024, pp. 1-5, doi: 10.1109/ISCAS58744.2024.10558322.

The work listed above was also presented at the MCC’s Annual Research Technical Conference (MTC) 2024.

Table 7.2: Performance summary and comparison table

Parameter	This work		[105]		[104]		[103]		[101]
Architecture	I/P PMOS	I/P NMOS	1V	DT	FIA	SA	DB	DT	DT
Technology [nm]	65	65	65	65	180	180	65	65	90
Supply [V]	1	1	1	1	1.2	1.2	1.2	1.2	1.2
Noise [μ V]	100 - 180	280 - 900	220	210	46	62	400	450	1500
Energy [pJ]	0.22 - 0.5	0.5	0.192	0.26	0.98	4.1	0.034	0.088	0.113
Area [μm^2]	4788	4788	90	90	9800	7700	125	90	82.5
FoM* [$nJ \cdot \mu V^2$]	2.2 - 16.3	39.2 - 405	9.29	11.46	2.07	15.8	5.44	17.8	254

$$*FoM = Energy \cdot (NoisePower)$$

Due to the fundamental trade-off between energy consumption and thermal noise, a figure of merit (FoM) to represent the energy efficiency of a comparator is defined as the product of the comparator energy consumption and the input-referred noise power. The lower the FoM, the higher the efficiency that the comparator achieves. From Table 7.2 it can be seen that this work presents for the first time a comparator whose performance (noise and energy) can be dynamically programmed.

7.3 Future Work

7.3.1 Asynchronous logic

As discussed in Section 3.2.3, a SAR ADC with asynchronous logic can operate at twice the speed of a synchronous design, without increasing the power consumption of the analog blocks. Additionally, asynchronous designs reduce the complexity of the required logic, leading to lower digital power consumption compared to conventional synchronous implementations. Alternatively, it could relax the reference

settling timing constraints while maintaining the same sampling speed. These advantages, combined, would result in an improved FoM and should be investigated in the future.

7.3.2 Lower power supply voltage

The literature review of low-power SAR ADCs in Chapter 3, as shown in Table 7.1, indicates that supply voltages in the latest designs range from 1 V down to as low as 0.4 V, reflecting the current state-of-the-art. The dynamic power is proportional to V_{DD}^2 , so reducing the supply voltage from 1 V to 0.5 V would result in a 4x decrease in power consumption. Future research on this project would be to employ a clock booster to boost up each of the individual circuits to its nominal voltage, which is necessary to operate. This reduction of supply voltage would significantly improve the achievable FoM, provided that performance remains unaffected.

7.3.3 DAC digital calibration

The accuracy of the output voltage of a DAC is influenced by gain and offset errors within the DAC and other components, such as switches. Digital calibration compensates for these errors by adjusting the digital inputs sent to the DAC, effectively eliminating their impact. This approach enhances DAC performance without the need for component trimming or external solutions. Future research could explore additional methods to further improve DAC performance using this technique.

7.3.4 Ping-Pong action SAR ADC

Future work on this project would involve employing the ping-pong action Capacitive Digital-to-Analog Converter (CDAC) based SAR ADC to power up the dynamic comparator. The internally generated charge resulting from switching between two CDACs serves as a charge reservoir for the dynamic comparator during decision-making.

Appendix A

Comparator mathematical analysis

The first-order approximation from the the analysis in [99, 100] shows that integration time is approximated as:

$$T_{int} \approx \frac{C_p}{I_D} \cdot V_{TH}, \quad (\text{A.1})$$

where V_{TH} is the threshold voltage and C_p is the integrating capacitance. The integration gain A_v depends on the input transistors $\frac{g_m}{I_D}$ and the threshold voltage.

$$A_V \approx \frac{g_m}{I_D} \cdot T_{int} \approx \frac{g_m}{I_D} \cdot V_{TH} \quad (\text{A.2})$$

The controllable parameters to improve gain are the following:

- Integration time T_{int} .
- g_m of the input differential pair.
- load capacitance C_p .

Conventionally, the input transistors are biased in the strong-inversion region. A detailed analysis shows that the input-referred noise of the comparator is primarily dominated by the dynamic integrator, and this noise is inversely proportional to the $\frac{g_m}{I_D}$ ratio

$$\overline{V_{n,pre}^2} \approx \frac{I_D}{g_m} \cdot \frac{4kT\gamma}{V_{thn}C_p}. \quad (\text{A.3})$$

To minimise the thermal noise, a high $\frac{g_m}{I_D}$ ratio and a large integrating capacitor C_p are required. The noise and offset introduced by the latch are reduced by the integration gain A_V

$$\sigma_{n(os),in} \approx \sqrt{\sigma_{n(os),int}^2 + \frac{\sigma_{n(os),latch}^2}{A_{int}^2}}. \quad (\text{A.4})$$

A.1 Latch Delay calculation

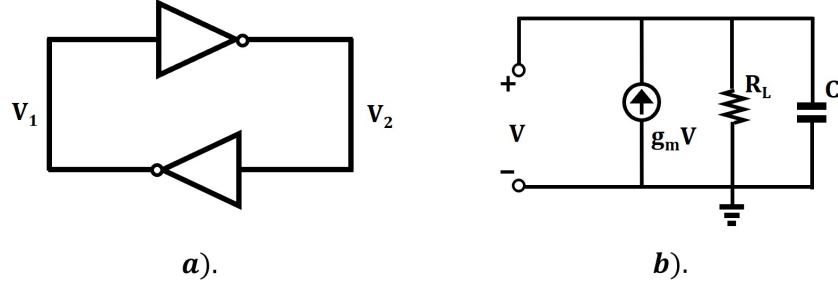


Figure A.1: a). shows the simplified circuit diagram of a regenerative latch, b). shows its respective linearised model.

The following analysis shows the determination of the comparator delay for the regenerative latch.

$$g_m V = \frac{V}{R_L} + \frac{CdV}{dt} \quad (\text{A.5})$$

$$g_m V - \left(\frac{V}{R_L}\right)dt = CdV \quad (\text{A.6})$$

$$\frac{V}{C} \left(g_m - \frac{1}{R_L}\right)dt = dV \quad (\text{A.7})$$

$$\frac{g_m}{C} \left(1 - \frac{1}{g_m R_L}\right)dt = \frac{1}{V}dV \quad (\text{A.8})$$

$$\frac{g_m}{C} \left(1 - \frac{1}{g_m R_L}\right) \int_{t_1}^{t_2} dt = \int_{V_1}^{V_2} \frac{1}{V}dV \quad (\text{A.9})$$

Assume $g_m R_L$ is much greater than 1;

$$\frac{g_m}{C} \cdot (t_2 - t_1) = \ln(V_2/V_1) \quad (\text{A.10})$$

$$\tau = \frac{C}{g_m} \cdot \ln(V_2/V_1) \quad (\text{A.11})$$

where τ is the comparator latch delay.

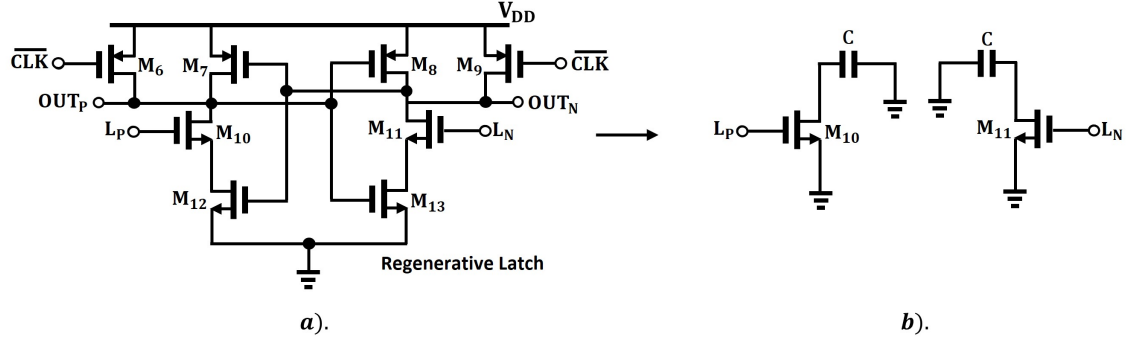


Figure A.2: a). circuit diagram of regenerative latch, b). equivalent signal model during decision phase.

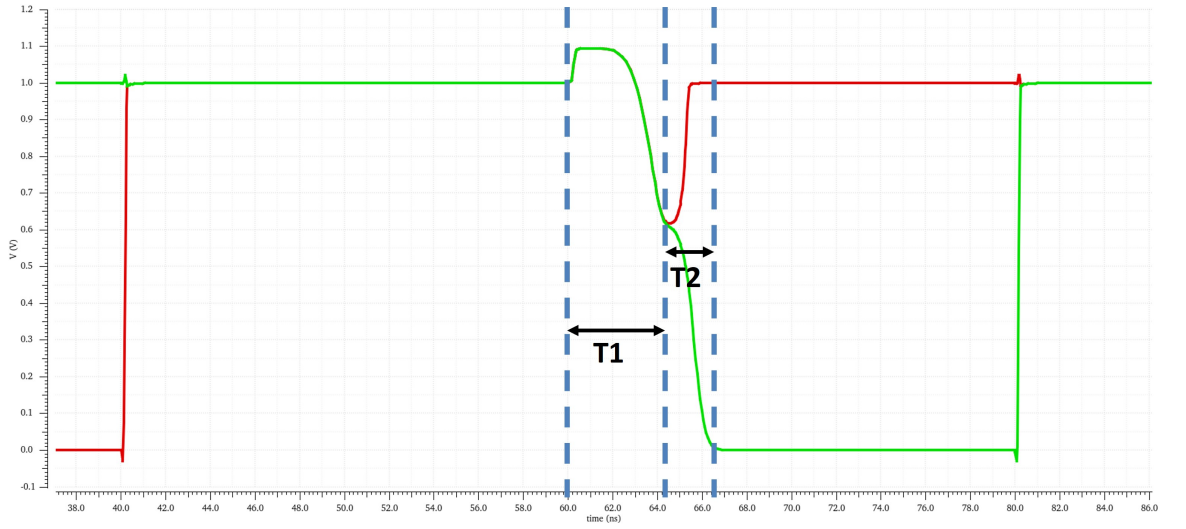


Figure A.3: Simulated output voltages of the regenerative latch

$$T_2 = V_{th} \cdot \frac{C_{fOUTp} + C_{fOUTn}}{I_D} \quad (A.12)$$

$$V_c(t) = \frac{I}{C}t \quad (A.13)$$

$$t = \frac{C}{I}\Delta V \quad (A.14)$$

$$T_1 = \frac{C}{I}\Delta V = \frac{C(V_{DD} - (V_{DD} - V_{TH}))}{\frac{\mu C_{ox} W (V_{cm} - V_{th})^2}{2L}} \quad (A.15)$$

$$T = T_1 + T_2 \quad (A.16)$$

where T is the total delay of the regenerative latch.

Appendix B

Simulation files

Spectre, a circuit simulator developed by Cadence and a part of the Virtuoso Analog Design Environment (ADE), was used for the simulation and verification of analog mixed-signal circuits in the TSMC 65nm CMOS process.

B.1 Design parameters

The design parameters - Width (W), Length (L), Fingers (F), Multipliers (M) of the circuits mentioned in Chapter 4 are discussed below. The Proposed switch-supply comparator and the conventional PMOS input Dynamic comparator, shown in Figures 4.1 and 4.2, are listed below:

- Transistor M_1 : $W = 360 \text{ nm}$; $L = 60 \text{ nm}$; $F = 4$; $M = 1$
- Transistor M_2, M_3 : $W = 1 \text{ u}$; $L = 60 \text{ nm}$; $F = 2$; $M = 16$
- Transistor M_4, M_5 : $W = 360 \text{ nm}$; $L = 60 \text{ nm}$; $F = 2$; $M = 1$
- Transistor M_{12}, M_{13} : $W = 180 \text{ nm}$; $L = 60 \text{ nm}$; $F = 2$; $M = 1$
- Transistor M_6, M_9, M_7, M_8 : $W = 360 \text{ nm}$; $L = 60 \text{ nm}$; $F = 32$; $M = 2$
- Transistor M_{10}, M_{11} : $W = 180 \text{ nm}$; $L = 60 \text{ nm}$; $F = 2$; $M = 1$
- Transistor M_{14} : $W = 200 \text{ nm}$; $L = 60 \text{ nm}$; $F = 10$; $M = 2$

Capacitor values:

- $C_P = 26 \text{ fF}$
- $C_R = 3 \text{ pF}$

The design parameters for the switches used in CDAC shown in Figure 4.20 are listed below:

- Transistor M_1 : $W = 400 \text{ nm}$; $L = 280 \text{ nm}$; $F = 2$; $M = 1$
- Transistor M_3 : $W = 200 \text{ nm}$; $L = 60 \text{ nm}$; $F = 2$; $M = 1$
- Transistor M_2 : $W = 200 \text{ nm}$; $L = 60 \text{ nm}$; $F = 2$; $M = 1$
- Transistor M_4 : $W = 200 \text{ nm}$; $L = 60 \text{ nm}$; $F = 8$; $M = 1$

The design parameters for the proposed clock boosting circuit shown in Figure 4.31 are listed below:

- Transistor M_3 : $W = 200 \text{ nm}$; $L = 60 \text{ nm}$; $F = 2$; $M = 1$
- Transistor M_2 : $W = 200 \text{ nm}$; $L = 60 \text{ nm}$; $F = 2$; $M = 1$
- Transistor M_1 : $W = 200 \text{ nm}$; $L = 60 \text{ nm}$; $F = 2$; $M = 1$
- Transistor M_7 : $W = 360 \text{ nm}$; $L = 60 \text{ nm}$; $F = 2$; $M = 1$
- Transistor M_6 : $W = 180 \text{ nm}$; $L = 60 \text{ nm}$; $F = 2$; $M = 1$
- $C_1 = 150 \text{ fF}$

The design parameters for the bootstrap circuit shown in Figure 4.30 are listed below:

- Transistor M_1, M_2, M_3 : $W = 600 \text{ nm}$; $L = 60 \text{ nm}$; $F = 2$; $M = 1$
- Transistor M_{10} : $W = 60 \text{ nm}$; $L = 200 \text{ nm}$; $F = 2$; $M = 1$
- Transistor M_9 : $W = 200 \text{ nm}$; $L = 100 \text{ nm}$; $F = 2$; $M = 1$
- Transistor M_8 : $W = 600 \text{ nm}$; $L = 60 \text{ nm}$; $F = 2$; $M = 1$
- Transistor M_6 : $W = 200 \text{ nm}$; $L = 60 \text{ nm}$; $F = 2$; $M = 1$
- Transistor M_7 : $W = 360 \text{ nm}$; $L = 60 \text{ nm}$; $F = 2$; $M = 1$
- Transistor M_5 : $W = 180 \text{ nm}$; $L = 60 \text{ nm}$; $F = 2$; $M = 1$
- $C_1 = 12 \text{ fF}$
- $C_2 = 12 \text{ fF}$
- $C_3 = 160 \text{ fF}$

The design parameters for the TSPC logic shown in Figure 4.34 are listed below:

- Transistor M_1 : $W = 250 \text{ nm}$; $L = 60 \text{ nm}$; $F = 1$; $M = 1$

- Transistor M_2 : $W = 360 \text{ nm}$; $L = 60 \text{ nm}$; $F = 1$; $M = 1$
- Transistor M_3 : $W = 180 \text{ nm}$; $L = 60 \text{ nm}$; $F = 1$; $M = 1$
- Transistor M_4 : $W = 200 \text{ nm}$; $L = 60 \text{ nm}$; $F = 2$; $M = 1$
- Transistor M_5 : $W = 300 \text{ nm}$; $L = 60 \text{ nm}$; $F = 1$; $M = 1$
- Transistor M_6 : $W = 180 \text{ nm}$; $L = 60 \text{ nm}$; $F = 2$; $M = 1$
- Transistor M_7 : $W = 300 \text{ nm}$; $L = 60 \text{ nm}$; $F = 1$; $M = 1$
- Transistor M_8 : $W = 200 \text{ nm}$; $L = 60 \text{ nm}$; $F = 1$; $M = 1$
- Transistor M_9 : $W = 180 \text{ nm}$; $L = 60 \text{ nm}$; $F = 1$; $M = 1$

B.2 Derivation of ENOB equation

When an ADC converts an analog signal to digital, the resolution is limited by the number of bits (N), and the signal is approximated to the nearest discrete level. This introduces quantization noise, which is the error between the actual analog signal and the quantized digital signal. The Power Spectral Density (PSD) of the quantization error is evaluated by assuming $0 \leq V_{in} \leq V_{FS}$, $V_{in} \gg \Delta$, N is large, e is independent of V_{in} . The quantization noise is uniformly distributed and the quantization noise spectrum is white. The mean squared noise due to Quantization is given by:

$$\sigma_e^2 = \int_{-\Delta/2}^{\Delta/2} e^2 \cdot \frac{1}{\Delta} \cdot de = \frac{\Delta^2}{12}. \quad (\text{B.1})$$

- SNDR defines the theoretical performance of an ideal N-bit ADC.
- Assume a sinusoidal input $V_{PP} = V_{FS} = 2^N \cdot \Delta$

$$\text{Signal Power } S = \frac{V}{C} (g_m - \frac{1}{R_L}) dt = dV \quad (\text{B.2})$$

$$\text{Signal Power } S = (V_{rms})^2 = (V_{FS}/2\sqrt{2})^2 \quad (\text{B.3})$$

$$\text{Signal Power } S = V_{rms}^2/8 = (2^N \cdot \Delta)^2/8 \quad (\text{B.4})$$

$$\text{Noise Power } N = \Delta^2/12 \quad (\text{B.5})$$

$$SNDR \text{ (dB)} = 10 \log_{10}(S/N) \quad (\text{B.6})$$

$$SNDR \text{ (dB)} = 10 \log_{10}\left(\frac{3}{2} \cdot 2^{2N}\right) \quad (\text{B.7})$$

$$SNDR \text{ (dB)} = 6.02N + 1.76 \text{ dB} \quad (\text{B.8})$$

$$ENOB = \frac{SNDR - 1.76}{1.76} \quad (\text{B.9})$$

B.3 Comparator noise setup

For clocked comparators, apply constant DC input voltages around the common mode voltage. The input referred noise varies with respect to the common mode voltage. When applying DC input voltages, ensure that differential voltage varies from negative to positive values.

- Transient noise analysis was performed to tabulate the noise, with F_{MAX} at least 50 times the clock frequency.
- Noise F_{min} is set to lowest noise frequency of interest.
- Noise F_{min} and Stop time are inversely related to each other.
- For each input differential voltage, the Probability of One's is tabulated. Probability of One's is the ratio of the number of times the comparator gives a decision HIGH to the total number of samples taken.
- Cumulative Distributive Function (CDF) is calculated from the following expression:

$$CDF = \frac{1}{2} \left[1 + \operatorname{erf} \left(\frac{V_{diff} - \mu}{\sigma \sqrt{2}} \right) \right], \quad (\text{B.10})$$

where μ is the mean and σ is the standard deviation

- To tabulate the CDF values, start by choosing some random values for σ , Adjust the σ value until the probability of One's and the CDF values overlap with respect to input differential voltage. The best overlap plot of probability of One's gives the value of σ
- For the Figure shown in 5.4, the above mentioned approach was used to calculate for different values of Reservoir capacitance.

Appendix C

Testing PCBs

C.1 Testing SAR ADC described in Chapter 4.

The design strategy for testing the SAR ADC described in Chapter 4 is as follows.

- Reference voltages, common mode voltages, and supply voltages are provided off-chip.
- To ensure a stable, regulated DC output voltage, low-noise Low Dropout Regulators (LDOs) are used on the PCB.
- Two clock signals are supplied to the PCB: The SAR clock, which is used for the SAR logic and to generate the internal clock for the comparator. The DAC reset clock, which resets the DAC and SAR logic after every conversion. These two signals are externally synchronised using an off-chip clock generator and are used to generate all internal control signals.
- Two signals are taken from the chip: serial comparator data and the End of Conversion (EOC) signal.
- To reduce the number of PCB pins, instead of directly taking 14-bits from the SAR logic, serial data from the comparator is taken from the PCB using digital discovery. This data is then converted to parallel using the python code shown in Figure C.1.
- The converted parallel data is processed in MATLAB to obtain the corresponding FFT spectrum.
- In this design, all SAR core circuits share the same power supply pin. The current drawn is measured using a digital multimeter to calculate the total power consumption of the SAR ADC.

```
import csv

column = []
sampleOutput=[]
with open('acq_tran_5.csv', mode='r') as csv_file:
    csv_reader = csv.DictReader(csv_file)
    line_count = 0
    for row in csv_reader:
        column.append((row["DIO 27"]))

"convert data into window size of 18"
def chunks(lst, n):
    for i in range(0, len(lst), n):
        sampleOutput.append(lst[i:i + n])

# bucket size
chunks(column,18)

"remove first 4 data points"
sampleout2 = []
sampleoutput3 = []
for i in range(len(sampleOutput)):
    for j in range(len(sampleOutput[i])):
        if j <= 3:
            pass
        else:
            sampleout2.append(sampleOutput[i][j])
    sampleoutput3.append(sampleout2)
    sampleout2 = []

"save dat containg 14 colums per row in txt"
with open('acq_tran_5_parallel.txt', mode='w') as employee_file:
    employee_writer = csv.writer(employee_file, delimiter='\t')
    for i in sampleoutput3:
        employee_writer.writerow(i)

print("done")
```

Figure C.1: Python code to convert serial data to parallel data

C.2 Testing programmable comparator described in Chapter 5.

- The supply voltage, input signal, and control signals are provided off-chip.
- The comparator noise is measured in a similar manner as mentioned in Appendix B.3 using the data collected from the board via digital discovery for different values of reservoir capacitance.

- The comparator power is recorded for different values of reservoir capacitance by measuring the current drawn when control signals are connected to the desired Reservoir capacitance.

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