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Back-gated Nb-doped MoS_2 junctionless field-effect-transistors

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Electrical measurements were carried out to measure the performance and evaluate the characteristics of MoS_2 flakes doped with Niobium (Nb). The flakes were obtained by mechanical exfoliation and transferred onto 85 nm thick SiO_2 oxide and a highly doped Si handle wafer. Ti/Au (5/45 nm) deposited on top of the flake allowed the realization of a back-gate structure, which was analyzed structurally through Scanning Electron Microscopy (SEM) and Transmission Electron Microscopy (TEM). To best of our knowledge this is the first cross-sectional TEM study of exfoliated Nb-doped MoS_2 flakes. In fact to date TEM of transition-metal-dichalcogenide flakes is extremely rare in the literature, considering the recent body of work. The devices were then electrically characterized by temperature dependent I_{ds} versus V_{ds} and I_{ds} versus V_{bg} curves. The temperature dependency of the device shows a semiconductor behavior and, the doping effect by Nb atoms introduces acceptors in the structure, with a p-type concentration 4.3×10^{19} cm^{-3} measured by Hall effect. The p-type doping is confirmed by all the electrical measurements, making the structure a junctionless transistor. In addition, other parameters regarding the contact resistance between the top metal and MoS_2 are extracted thanks to a simple Transfer Length Method (TLM) structure, showing a promising contact resistivity of 1.05×10^{-7} Ω/cm^2 and a sheet resistance of 2.36×10^2 Ω/sq. © *2016 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).*
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INTRODUCTION

One of the most promising candidates as a substitution for silicon in modern electronics devices are Transition-Metal-Dichalcogenides (TMDs). These are semiconductors in the form of MX_2, where M is a transition metal (Mo, W, Hf), and X is a chalcogen (S, Se, Te). The weak Van-Der-Waals forces between each 2D monolayer of which they are formed, allow thin multilayers to be easily exfoliated by a scotch tape technique from their bulk form, as first was shown for graphene.[1] However one of the main limitations of graphene is its zero bandgap and resulting low on/off current ratio, which limits its usefulness for field-effect-transistor (FET) applications. On the contrary, a selection of TMDs show a finite direct bandgap between 1-2 eV, predicted by density-functional-theory (DFT) calculations,[2] which makes them suitable for logic devices. Their ultra-thin nature would allow a better electrostatic control for device applications with respect to the state-of-the-art devices, and better immunity to short-channel effects, earning the attention of the electronics and optoelectronics community.

Several groups have studied processes more compatible with large area coverage than mechanical exfoliation to obtain thin film or few monolayers of TMD materials. These include Chemical Vapor Deposition (CVD) used to grow MoS_2 by sulphurization of the metal,[3–5] Molecular Beam Epitaxy (MBE) methods to grow $HfSe_2$,[6] or $MoSe_2$,[7] which can be potentially extended to other 2D

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materials, and Atomic Layer Deposition (ALD) of MoS_2.[8] Even though these kinds of processes will be needed for future applications in larger scale production, scotch tape based exfoliation is widely used because of its easiness, and fresh flakes can be obtained quickly. In addition, this method doesn't compromise device performance in terms of gate control and current on/off ratios. Often, back-gate devices are prepared with mechanically exfoliated flakes, in which the substrate is used as a control gate. Top-gated TMD films have produced an on/off ratio exceeding 10^8 and mobility of almost 200 $cm^2/V.s$ for MoS_2 based FETs.[9]

In many cases, after flake preparation, an important problem that can affect and limit device performance is the contact resistance between the metal and the TMD. A high resistance can be due to residues at the TMD-metal interface, such as moisture or oxidation states on the surface. Moreover, X-ray photoelectron spectroscopy (XPS) results have shown impurities of carbon and oxygen on geological MoS_2.[8] A cleaner TMD surface can be obtained by 15 minutes ultra-high-vacuum (UHV) annealing at 400 °C, which can burn off the unwanted contaminants. This is important because a low contact resistance can be obtained if a clean TMD-metal interface is achieved.[10]

An important role is also played by the types of metals used because Fermi level pinning may occur at the interface. This would result in a Schottky-barrier modulated current[11] instead of a more linear ohmic characteristic. It has been shown how low work function metals[12] such as Sc, may be used to improve both carrier injection and the contact resistance of the device, but other metals, such as Ti[11–13] and Ni[12,14,15] have been used as well.

In this article, we report the electrical measurements of a back-gated MoS_2 flake doped with Nb, mechanical exfoliated from a Nb-doped MoS_2 crystal. Overall, device performance shows p-type characteristics, as expected for substitutional Nb doping,[16–18] and promising results in terms of MoS_2-metal contact resistance, demonstrating that high Nb doping levels can improve MoS_2 device characteristics, much like in other doped semiconductors.[14]

EXPERIMENTAL

Using classic scotch tape techniques thin multilayer MoS_2 flakes were mechanically exfoliated from a bulk MoS_2 crystal. During formation of the synthetic MoS_2 crystal by a chemical vapor method, Nb was incorporated by the supplier. The presence of the Nb in the crystal was confirmed by time of flight secondary ion mass spectrometry (SIMS) analysis (not shown). The exfoliated flakes were gently pressed onto a surface composed of 85 nm of SiO_2 and a highly-doped Si handle wafer. The height of the flake measured using a Tencor Profiler was approximately 9.8 nm, thus the number of layers of the flake, considering each layer as 0.65 nm thick, is approximately 15. Ti/Au metal contact pads and electrodes were defined by electron-beam lithography, followed by metal evaporation and a lift off process. 15 kV beam exposures were performed with a Zeiss SUPRA SEM with a Raith Elephy Plus blanker. An adhesion layer of 5 nm of Ti and 45 nm of Au were deposited with e-beam evaporation. Before and after metal deposition the sample wasn't subjected to any process to remove surface contaminants.

For structural analysis, cross-section samples were obtained by using FEI's Dual Beam Helios Nanolab 600i system using Ga ion beam. Three layers of protective material were used, namely electron beam C, electron beam Pt, and ion beam C. Lamellas were thinned and polished at 30 kV 100 pA and 5 kV 47 pA, respectively. Cross-sectional Transmission Electron Microscopy (XTEM) imaging was carried out using a JEOL 2100 HRTEM operated at 200 kV in Bright Field mode using a Gatan Double Tilt holder. For electrical characterization, the Agilent B-1500 parameter analyser was used. Hall effect measurements were obtained using a LakeShore HMS 8404 Hall Measurement System with both DC and AC magnetic field capability.[19] We carried out Hall effect measurements on an approximetly 190 μm thick flake exfoliated from the same bulk Nb-doped MoS_2 crystal. Both DC and AC magnetic field methods were used with field reversal strength of ±1.7 T for the DC technique and +1.2 T_{rms} for the AS method using a lock-in amplifier. Geometry and current reversal methods were employed to remove error factors.

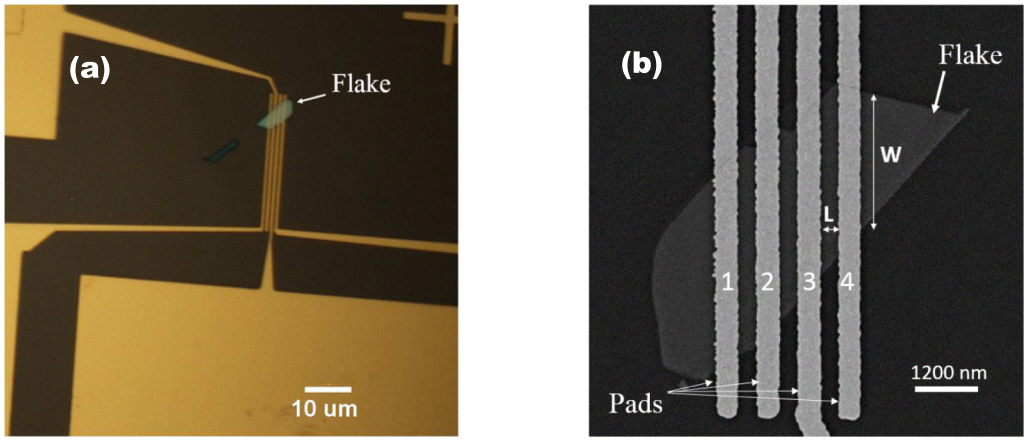


FIG. 1. (a) Optical image of the MoS_2 flake. (b) SEM image of the contacted device, with the contact tracks numbered 1 to 4.

RESULTS AND DISCUSSION

The Nb-doped MoS_2 device is shown in Figure 1(a) and 1(b). The image in Figure 1(a) was taken with an optical microscope. The large areas of metal are the contact pads, and the lines are the metal electrodes leading to the MoS_2 flake, which is labelled. In addition, a SEM image of the device is shown in Fig. 1(b), to be sure that metal deposition was successful, without any cracks or discontinuities of the metal tracks along the flake. For the sake of clarity, the pads are numbered 1 to 4 from left to right.

Representative TEM images are reported in order to have a deeper understanding of the material characteristics of the flake. Figure 2 shows a wide view of the device, where it is possible to notice the Ti/Au pads on top of the thin flake, and then the SiO_2 and the Si substrate. Interestingly, the flake is characterized by undulations along the surface of the substrate, which are most prominent around the edges of the Au/Ti metal. It is possible the weak Van der Waals forces between layers of MoS_2 allow for some bending of the thin MoS_2, which causes a bending in the MoS_2 film primarily around the edges of the Au/Ti metal electrodes, most probably occurring due to the lift off process.

Figure 3 shows four different representative TEM images with a higher magnification, taken at different locations along the flake. In Fig. 3(a) it is possible to clearly see the layered structure of the flake, composed by 16 layers, confirming the height of almost 10 nm found with the Tencor Profiler. Figure 3(b) shows another particular area of the flake, where the flake bends, even if it is not near the metal pads.

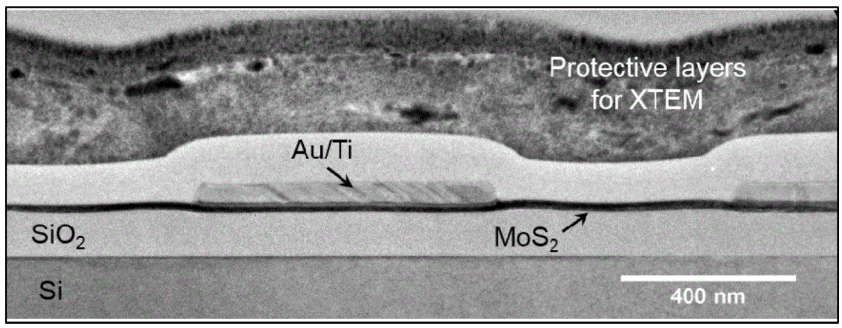


FIG. 2. Representative TEM image of the overall structure of the flake. It is possible to note the undulations of the 10 nm MoS_2 flake along the surface of the substrate.

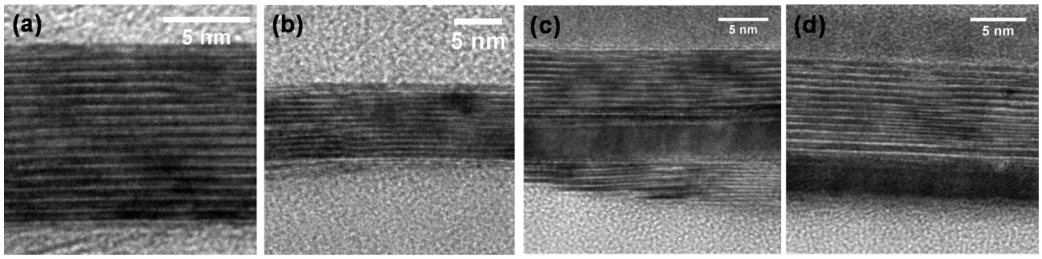


FIG. 3. Representative higher-resolution TEM images showing (a) the layered structure of the MoS_2, (b) bending of the MoS_2. Indicated by the white arrows in (c) and (d) uniformly grey regions which are crystalline but do not have the classic layered MoS_2 structure. This may be a side-effect of the mechanical exfoliation.

Figure 3(c) displays that the layered MoS_2 structure and the height are not constant along all the flake. There are regions within the MoS_2 that are crystalline, but not perfectly layered like that in Fig. 3(a). This is the uniformly grey region. This may be a side-effect of the mechanical exfoliation process, as cross sections of the bulk crystal (not shown) do not show this. This may be due to a different orientation of the MoS_2 layers in that area, so the flake may still be crystalline in that region. Moreover the height is clearly not perfectly constant, but some missing layers can be due to the stress induced on the flake through the mechanical exfoliation method. Figure 3(d) reports another region of thin MoS_2 which is crystalline but does not have the classic layered MoS_2 structure. This uniformly grey region might have a different orientation to the rest of the layered MoS_2.

Electrical measurements were carried out to characterise the electrical conductivity of the device. First of all, I_{ds} versus V_{ds} curves were measured at 25, 40 and 55 °C, considering all pad combinations to ensure that there were no open-circuits of any pad or short-circuits between pads. Figure 4(a) shows the IV characteristics between the first and the second pad, while Figure 4(b) considers the first and the last one. This effectively changes the channel length of the back-gated device. The current scales with gate length as expected. An increase in temperature corresponds to a higher current, consistent with a semiconductor behavior. The current is not linear with respect to source-drain voltage, so it is not an ohmic behavior, but it seems to be modulated by Schottky barrier between the flake and the metal, as was reported in other publications.[11,12]

In order to further demonstrate the p-type behavior of the device, I_{ds} versus V_{ds} curves were extracted for different values of V_{bg}, considering a constant drain-source voltage at 1 V. As it is clear from the plot in Fig. 5, a more negative back-gate voltage results in a higher drain current, as it would be expected from a p-type doped semiconductor. Calculating the maximum depletion region

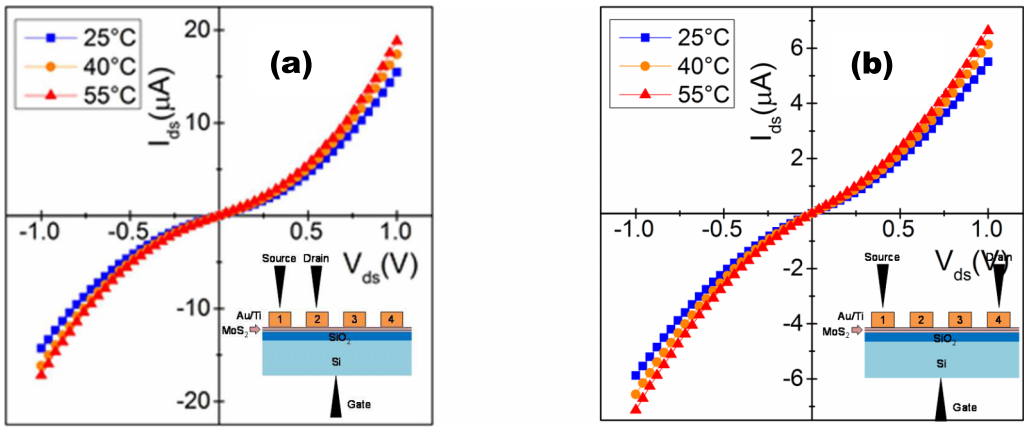


FIG. 4. IV charateristics between (a) first and second pad and between (b) first and fourth pad, as labelled in Fig. 1, for no voltage applied to the back gate. The insets show the contact scheme.

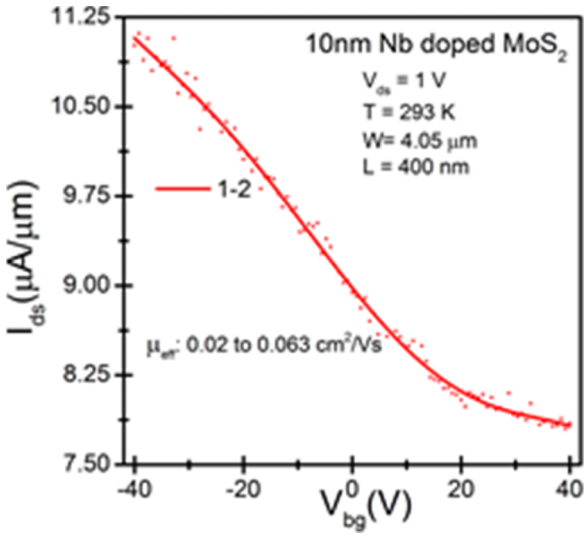


FIG. 5. I_{ds}-V_{bg} curve between the first and second electrodes as labelled in Fig. 1.

in the MoS_2 film based on the doping concentration of 4.3×10^{19} cm^{-3} and an out of plane dielectric constant of 10.5 for MoS_2, yields a value of 4.7 nm[18]. This value is lower than the thickness of the MoS_2 flake (~10 nm) and as a consequence the device cannot be fully turned off compromising its I_{on}/I_{off} ratio.

Further proof of the p-type doping of the flake are the findings of our DC and AC Hall effect measurements. From other publications, the carrier concentration reported for this type of flake was 3×10^{19}–3×10^{20} cm^{-3}.[17,18] Our Hall effect data confirm this, as the p-type doping concentration found is 4.3×10^{19} cm^{-3} with a Hall mobility of approximately 7.5 $cm^2/V.s$.

Considering the overall structure of the device and such a high doping, it can be categorized as a "junctionless transistor", whose architecture can achieve low leakage currents and very good response against short channel effects.[20,21] The importance of this is not only related to the potential of the electrical characteristics, but also to the easier process and the higher device density that could be advantageous with respect to the modern silicon-based devices in production.

Another parameter extracted from the electrical measurements is the field effect mobility. The field effect mobility was determined from the derivative of the transfer characteristic, and the results for two separate pad combinations are shown in Figure 6, with the peak mobility values for all pad combinations included in Table I.

The field effect mobility is lower than the Hall effect mobility probably due to a number of factors. The Hall effect measurement was performed on a large crystal, while the device characteristics were extracted from a 10 nm flake, with all its imperfections (see XTEM in Fig. 3) and many surfaces. These imperfections are likely to degrade the carrier mobilities. The field effect mobility values were found to be in the range 0.02 and 0.2 $cm^2/V.s$.

Previous studies have shown the thickness dependence of the mobility[12,22,23] and the improvement after high-k dielectric passivation[24,25] or vacuum annealing for removal of atmospheric adsorbates.[22] In terms of optimum TMD thickness, Das *et al.*[12] reported a systematic study on MoS_2 flakes, back-gated n-type FET devices with Sc contact metallization. Based on drive current and mobility, MoS_2 thicknesses of ~6-12 nm, which comprises the height of our flake, appears to be optimum. Also, a thickness study showed a peak of mobility of approximately 54 $cm^2/V.s$ for 8 layers. In that work electron mobility was 184 $cm^2/V.s$ without high-k overlayers, but with Al_2O_3 high-k dielectric mobility increased to 700 $cm^2/V.s$. Very recently Lee *et al.* reported field-effect mobility of 4.5 $cm^2/V.s$ measured in $MoS_2/SiO_2/Si$ back-gated transistors, based on a clean transfer of large-area MoS_2 films using deionized water.[26] Considering our process flow, there were no high-k dielectric passivation or vacuum annealing, so these could be some of the reasons for the low values of field effect mobility.

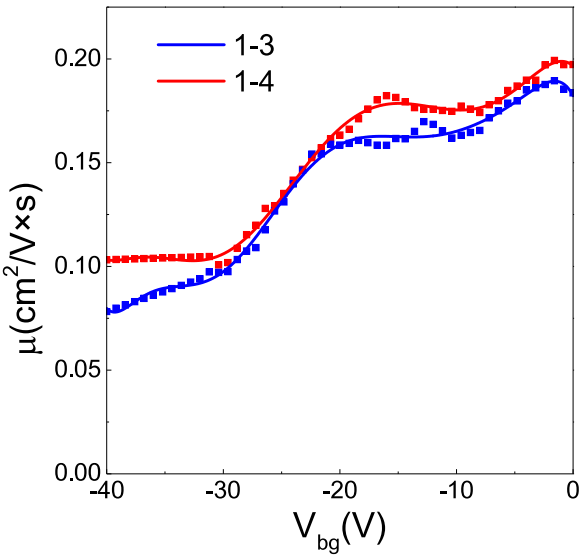


FIG. 6. Derivation of field effect mobility values versus V_{bg} for two different pad combinations: 1-3 and 1-4.

TABLE I. Voltages where peak $g_{m,max}$ values are recorded and the corresponding field-effect mobility values at those voltages for all pad combinations.

Pad combinations	Voltage (V)	μ (cm^2/V.s)
1-2	−0.8	0.06
1-4	−1.6	0.20
1-3	−1.6	0.19
2-3	−3.2	0.04
2-4	−1.6	0.08
3-4	−2.4	0.02

Even if the current is not perfectly ohmic as said before, still the promising electrical response of the flake is worthy to be further studied. Then, from the SEM image reported in Fig. 1, one can notice how the pad configuration looks like a simple Transfer Length Method (TLM) structure, where the length and the width are reported as "L" and "W", respectively. If the TLM method could be applied more parameters can be extracted from the device, allowing a deeper understanding of its characteristics.

Each track is 400 nm wide and the spacing between each track is 400 nm. In order to apply the TLM method three lengths can be considered: between first and second pad (spacing=400 nm), between first and third pad (spacing=1200 nm), and first and forth pad (spacing=1600 nm). In addition, the width "W" is approximately 4.05 μm.

We are aware that TLM layouts are usually more optimized than here. Indeed, in order to create a TLM there should be more tracks, with varied spacing. In Fig. 7 it is possible to see that the total resistance plotted against the contact separations considered before is linear at different temperatures. With the TLM, from the data in Fig. 7, it is possible to extract the contact resistance and the transfer length of the AuTi/MoS_2 contacts. Considering these values it is possible to evaluate sheet resistance (R_{SH}), specific contact resistivity (ρ_C), and contact resistance (R_C) expressed in Ω and Ω · mm. All the results are shown in Table II. The transfer length values are between 207 and 211 nm, which is almost half the width of the contact tracks. The contact resistance values are ranged between 12.34 and 12.45 kΩ, which is in agreement with other publications,[27,28] despite the fact that we did not perform optimized process recipes to minimize contact resistance. With regards to R_C expressed as Ω. mm our value reported at 25 °C is almost 6.3 times higher than previously

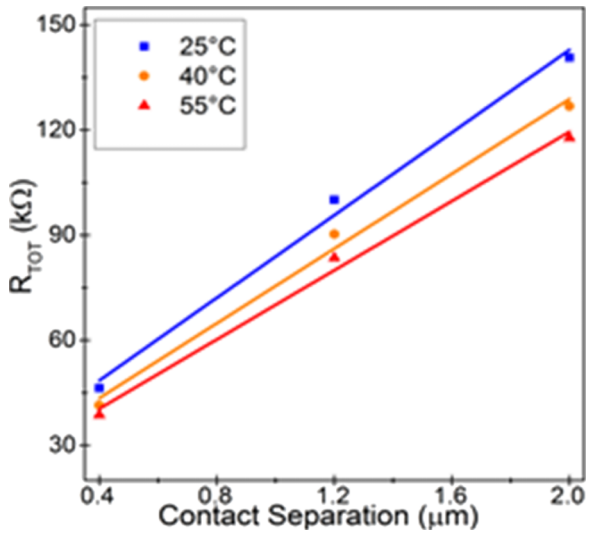


FIG. 7. Total resistance versus contact separation at different temperatures.

TABLE II. Results obtained from the MoS_2 device evaluated as a TLM structure.

Temp. (°C) :	25	40	55
1/kT	38.9	37.0	35.3
R_{SH} (Ω/sq)	2.36×10^2	2.13×10^2	1.97×10^2
L_T (nm)	211.1	207.4	209.2
ρ_C ($\Omega * cm^2$)	1.05×10^{-7}	9.18×10^{-8}	8.65×10^{-8}
R_C (kΩ)	12.4	11.0	10.3
R_C ($\Omega * mm$)	4.98	4.42	4.13

reported,[22] but it can be related to the different type of flake studied and to different process applied to the flake before testing it.

A low specific contact resistivity of 5×10^{-7} Ω. cm^2 for MoS_2 was reported by English *et al.*[10] In that work, the low contact resistivity was reached thanks to the low pressure adopted during the metal deposition by electron-beam lithography, in order to guarantee a cleaner interface between the MoS_2 and the metal. In terms of ρ_C, another relevant result of 2.2×10^{-7} Ω.cm^2 was reached by Kang *et al.*[29] through the use of Mo as metal contact, in order to form lower Schottky barrier and a high quality interface. Note that in these cases, MoS_2 flakes were mechanically exfoliated and no intentional or unintentional doping was reported. Our low value of 1.05×10^{-7} Ω.cm^2 indicates that high doping of MoS_2 is a very effective way to drive down ρ_C. Future work should combine high-doping levels with other processes such as pre-metal deposition cleaning and surface functionalisation techniques, along with dedicated TLM structures for accurate parameter extraction of ρ_C below 10^{-7} Ω.cm^2.

CONCLUSIONS

In summary, highly doped MoS_2 flakes were mechanically exfoliated and contacted. The p-type behavior of the flake, expected since it is doped with Nb atoms, was confirmed by electrical device measurements and by Hall-effect measurements that indicated a high carrier concentration of 4.3×10^{19} cm^{-3} and Hall mobility of 7.5 cm^2/V.s. The low contact resistance (12.4 kΩ and 4.98 Ω. mm) and specific contact resistivity (1.05×10^{-7}Ω.cm^2) data reported, even if extracted with a simple TLM structure, can be related to the high p-type doping of the flake, which, together with other processes widely used to improve metal contacts and obtain clean TMDs surfaces, can

be helpful in minimizing the specific contact resistance of the MoS_2/metal interface. Moreover, the high doping can be the key to the introduction of TMD-based junctionless transistors, in which the favorable characteristics of TMDs and the uncomplicated process required by this kind of device architecture may be combined.

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