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A study of capacitance-voltage hysteresis in the HfO_2/InGaAs metal-oxide-semiconductor system

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Abstract

In this work, we performed a study of capacitance-voltage (C-V) hysteresis in HfO_2/InGaAs metal-oxide-semiconductor (MOS) systems. The charge trapping density estimated from the C-V hysteresis is comparable to or even greater than the typical interface state density in high-*k*/InGaAs MOS systems. Based on an oxide thickness series, it is demonstrated that the magnitude of C-V hysteresis increases linearly with the increasing HfO_2 thickness, with the corresponding density of trapped charge being a constant value over the range of oxide thicknesses, indicating that the charge trapping is occurring in a plane near/at the HfO_2/InGaAs interfacial transition region. C-V hysteresis with a hold in accumulation was also investigated. It is observed that the C-V hysteresis has a power law dependence on the stress time in accumulation at the initial stage of stressing and tends to reach a plateau for sufficiently long stress times. Moreover, a larger gate voltage used during the stress increases the oxide field, allowing more border traps to be accessed.

Keywords – HfO_2; InGaAs; C-V hysteresis; stress

1. Introduction

High-dielectric constant (high-*k*) gate materials in conjunction with high mobility channel materials (e.g. InGaAs) are under investigation in order to improve metal oxide semiconductor field effect transistor (MOSFET) performance. However, the high-*k*/InGaAs MOS system exhibits a high density of interface states (D_{it}) and fixed oxide charges, both of which can affect device performance by degrading the subthreshold slope and shifting the MOSFET threshold voltage (V_t), and have been examined in some detail [1-5]. Charge trapping sites (referred to as "slow states" or "border traps") can also be located within the interfacial transitional region between the high-*k* oxide and the crystalline InGaAs. These border traps can cause device instability, and now represent the main challenge for the development of the high-*k*/InGaAs gate stacks. Border traps have been examined based primarily on the frequency dispersion of the accumulation capacitance for high-*k*/InGaAs MOS structures [6-8]. However, this accumulation frequency dispersion can also include the contribution of interface states which have short time constants and energy levels inside the conduction band [9-11]. An alternative way in which border traps manifest themselves in device behavior, is that they will induce hysteresis exhibited in the capacitance-voltage (C-V) response, and an analysis of C-V hysteresis presents as alternative method to characterize the density and charge trapping dynamics of high-*k*/InGaAs border traps. In the literature, very little attention has been paid to the issue of C-V hysteresis exhibited in high-*k*/InGaAs MOS systems [12-14]. In this study, we extend the work reported in [12] to study C-V hysteresis in HfO_2/InGaAs MOS capacitors with an emphasis on the charge trapping distribution in the HfO_2 film and a study of the charge trapping dynamics through analysis of the C-V hysteresis evolution with the hold in accumulation.

2. Experimental

The samples used in this work were *n*-doped and *p*-doped InP (100) substrates with 2 μm *n*-type (S at 4 $x10^{17}cm^{-3}$) and *p*-type (Zn at 4 $x10^{17}cm^{-3}$) InGaAs (indium concentration = 53%) epitaxial layers, respectively, grown by metal organic vapour phase epitaxy (MOVPE). Prior to oxide deposition, all the samples were immersed in $(NH_4)_2S$ solutions (10% in deionized H_2O) for 20 min at room temperature (~295 K) [15]. The samples were then introduced to the atomic layer deposition (ALD) chamber within a minimum transfer time (~3 min) after the removal from the 10% $(NH_4)_2S$ solution to minimize the formation of InGaAs native oxide due to air exposure. HfO_2 was deposited as the high-*k* oxide on the InGaAs surface. The HfO_2 dielectric has a series of thicknesses (10 nm, 15 nm, 20 nm, 25 nm, 30 nm) deposited by ALD at 250 ^{0}C using $Hf[N(CH_3)C_2H_5]_4$ (TEMAH) and H_2O as precursors. Pd (160 nm) was used as the metal contacts and formed by electron beam evaporation and a lift-off process. During the measurements, the samples were placed in a Cascade Microtech probe station (model Summit 12971B) in a dry air, dark environment. The C-V hysteresis measurements were recorded using either an Agilent CV-enabled B1500A semiconductor device analyser or an E4980 LCR meter. The C-V hysteresis responses were measured starting from inversion and sweeping towards accumulation, and subsequently sweeping back towards inversion. All the C-V hysteresis sweeps were recorded at room temperature and a high frequency of 1 MHz to minimize the D_{it} contribution to the C-V. The charge trapping density is quantified using equation (1).

$$Q_{trapped} = (\Delta V \times C_{ox})/q \ (cm^{-2}) \quad (1)$$

where $Q_{trapped}$ is the density of trapped charge in cm^{-2}, ΔV is the C-V hysteresis in V, C_{ox} is the oxide capacitance in F/cm^2, and q is the elementary charge in C. Equation (1) assumes the charge trapping is taking place predominantly near/at the high-*k*/InGaAs

interfacial transition region, as reported in [12] for HfO_2/InGaAs and Al_2O_3/InGaAs MOS systems. The validity of this assumption for the HfO_2/InGaAs structure is explored further in this paper.

3. Results and Discussion

Fig.1 shows double C-V hysteresis sweeps for HfO_2(15nm) over (a) *n*-InGaAs and (b) *p*-InGaAs MOS capacitors. The ΔV estimated from the first C-V hysteresis sweep corresponds to an electron trapping level of 2.4 x10^{12} cm^{-2} for the *n*-InGaAs, and a hole trapping level of 8.9x10^{12} cm^{-2} for the *p*-InGaAs, both of which are comparable to or even greater than the typical D_{it} integrated across the energy gap in high-*k*/InGaAs MOS systems, indicating that C-V hysteresis is an important problem to resolve. In addition, it is noted that the relaxation process for trapped charges in the InGaAs MOS structure is very fast when compared to silicon based MOS devices, with significant recovery occurring at time scales < 0.1 s [16]. As a consequence, the total trapped charge density could exceed the values quoted above when using fast pulse measurements on MOSFET structures. From Fig.1, it is also evident that the majority of the charge trapping is a reversible process as indicated by the almost overlapping 1st and 2nd sweeps in the inversion to accumulation (upwards) direction. There is a large shift between the 1st and 2nd upward C-V sweeps in the case of *p*-InGaAs, which is due to the charges being trapped in the defect sites which cannot be removed even when pushing the MOS capacitor back into inversion. More details are discussed in [12].

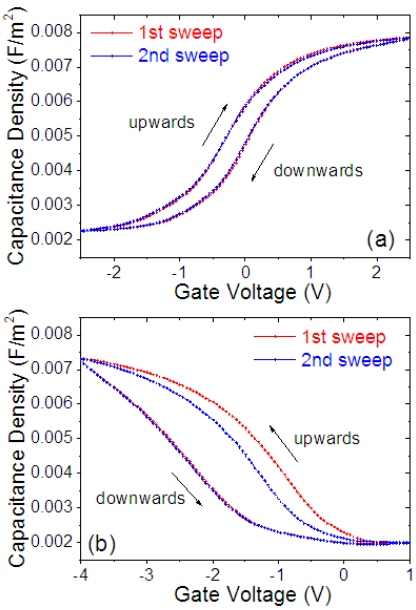


Fig.1 : Double C-V hysteresis for (a) Pd/HfO_2(15nm)/n-InGaAs and (b) Pd/HfO_2(15nm)/p-InGaAs MOS capacitors. The charge trapping density estimated from the C-V hysteresis (measured at the mid-point along the C-V) is comparable to or even greater than the typical D_{it} in high-k/InGaAs MOS systems.

The use of a HfO_2 thickness series allows for an investigation of the distribution of trapped charge in the HfO_2 film. The maximum electric field, as determined by the maximum voltage (V_{max}) in accumulation, is kept at the same value for all thicknesses for both the *n*-InGaAs and *p*-InGaAs, neglecting the effect of different oxide electric fields due to small variations in oxide thickness. It is observed in our experiments that the C-V hysteresis window increases for the samples with a thicker HfO_2 film. It is expected that, for a trapped charge located in a plane (in unit of cm^{-2}) near/at the oxide/semiconductor interface, ΔV is proportional to oxide thickness. This linear relation can be expressed using equation (2).

$$\Delta V = (q \times Q_{trapped} \times t_{ox})/(\varepsilon_0 \times k) \qquad (2)$$

where t_{ox} is the oxide thickness, ε_0 is the vacuum permittivity, and *k* is the relative permittivity of the oxide. For a trapped charge distributed throughout the oxide layer (in unit of cm^{-3}), ΔV will be proportional to the square of the oxide thickness [12, 17].

The C-V hysteresis magnitude (ΔV) and the corresponding charge trapping density are plotted as a function of oxide thickness as shown in Fig.2 for (a) *n*-InGaAs and (b) *p*-InGaAs MOS capacitors, which demonstrates a linear dependence of the C-V hysteresis magnitude on the HfO_2 thickness with the corresponding $Q_{trapped}$ being a constant value for all HfO_2 thicknesses. This is consistent with charge trapping occurring in a plane (in cm^{-2}) at the HfO_2/InGaAs interfacial transition region.

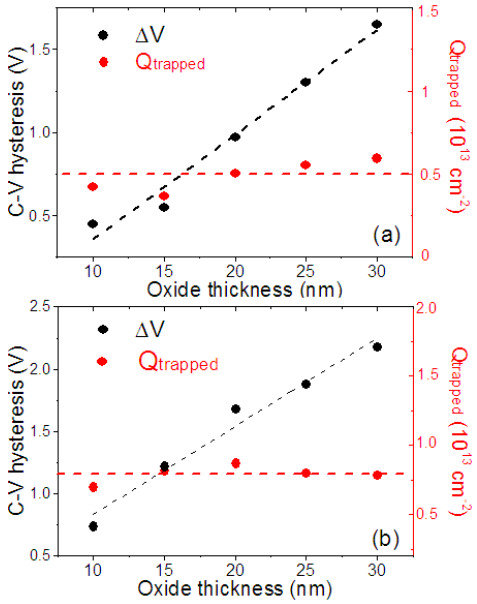


Fig.2 : C-V hysteresis (ΔV) and charge trapping density ($Q_{trapped}$) as a function of HfO_2 thickness for (a) Pd/HfO_2/n-InGaAs and (b) Pd/HfO_2/p-InGaAs MOS capacitors. The maximum electric field is kept at the same value for all thicknesses. C-V hysteresis is estimated at either the flatband capacitance or half the maximum capacitance. ΔV increases linearly with increasing HfO_2 thickness and the corresponding $Q_{trapped}$ is a constant value over the range of oxide thicknesses used, consistent with charge trapping occurring in a plane near/at the HfO_2/InGaAs interfacial transition region.

Extracting the gradient of ΔV versus the oxide thickness from Fig.2 and using equation (2) yield an electron trapping density of 7.0 x 10^{12} cm^{-2} for the *n*-InGaAs and a hole trapping density of 8.1 x 10^{12} cm^{-2} for the *p*-InGaAs. The linear dependence of C-V hysteresis on oxide thickness has also been observed in other high-*k* oxides (e. g. Al_2O_3, ZrO_2, HfAlO, HfSiO, etc) measured on InGaAs MOS systems as reported previously in [12, 18], all of which indicate that the trapped charge is localized in a plane and not distributed throughout the high-*k* oxide.

C-V hysteresis with a hold in accumulation (at V_{max}) was also investigated in this work. The measurements were performed using an E4980 LCR meter through labview which is capable of measuring C-V from inversion to accumulation at a gate voltage (V_g) equals to V_{max} and holding MOS capacitor at V_{max} for a period of time (t_{stress}) before sweeping the C-V back towards inversion. Measurements with different stress times were performed on different sites in order to minimize the possible contribution of stress induced interface states to the measured value of ΔV. The behavior of these sites has been confirmed to be similar by comparing the double C-V hysteresis measured on them prior to the stress measurements. Fig.3 shows the evolution of the C-V hysteresis with increasing stress hold time in accumulation for a Pd/HfO_2(15nm)/*n*-InGaAs MOS capacitor. It is important to emphasize that $\Delta V \neq 0$ V even without a hold time at V_{max} (see Fig.1 and Fig.3), and this ΔV value is denoted as ΔV_0. ΔV-ΔV_0 is plotted as a function of stress time for HfO_2(15nm) over (a) *n*-InGaAs and (b) *p*-InGaAs MOS capacitors using different values of V_{max} as shown in Fig.4 in log-log scale. It is observed that ΔV-ΔV_0 increases with a power law dependence with the increasing stress time at the initial stage of stressing and tends to reach a plateau when the stress time is sufficiently long. This relation is similar to the previous model proposed by S. Zafar et al [19], who performed positive bias stress pulses on HfO_2 and Al_2O_3 on Si substrate *n*-channel MOSFET and demonstrated that the threshold voltage shift (ΔV_t) increases with a power law dependence on the stress time at the initial stage of stressing. This model also predicts that the ΔV_t will eventually reach a plateau if the *n*-channel MOSFET is stressed at positive gate bias for a sufficiently long time providing that no new border traps are created during the stress. The relation between ΔV-ΔV_0 and stress time (t_{stress}) can be expressed using equation (3) on the premise that no new traps are generated during the stress.

$$\Delta V - \Delta V_0 = \Delta V_{max0} \times \{1 - \exp(-(t_{stress}/\tau_0)^{\gamma})\} \quad (3)$$

where τ_0 and γ are fitting parameters associated with the gate leakage current and the capture cross section of the traps, and ΔV_{max0} is associated with the maximum trapping density [19]. For $t_{stress} \ll \tau_0$, ΔV-$\Delta V_0 \approx \Delta V_{max0} \times (t_{stress}/\tau_0)^{\gamma}$ (i.e. a power law dependence of ΔV-ΔV_0 on t_{stress}), and for $t_{stress} \gg \tau_0$, ΔV-$\Delta V_0 \approx \Delta V_{max0}$ (i.e. a plateau). Once ΔV_{max0} is obtained (i.e. the saturation value of ΔV-ΔV_0 in Fig.4), the maximum trapping density corresponding to a certain value of V_{max} used, can be calculated using equations (1) and (3).

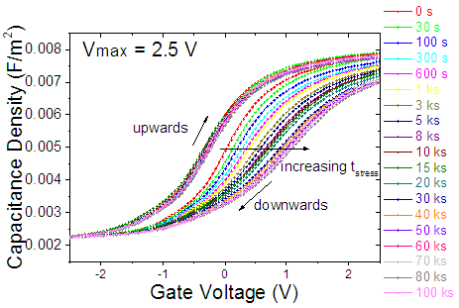


Fig.3 : C-V hysteresis responses with an increasing stress time in accmulation (at V_{max} = 2.5 V) for a Pd/HfO_2(15nm)/n-InGaAs MOS capacitor.

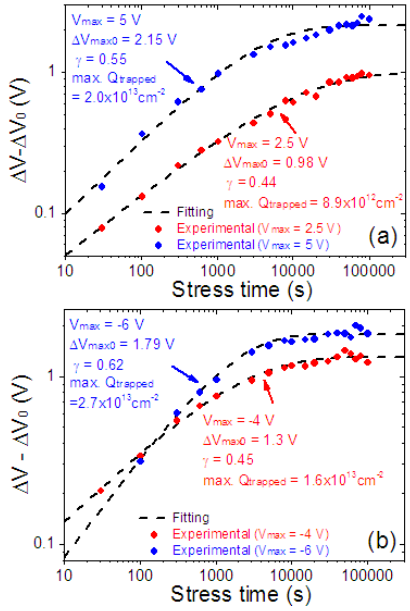


Fig.4 : ΔV- ΔV_0 as a function of stress time for (a) Pd/HfO_2(15nm)/n-InGaAs and (b) Pd/HfO_2(15nm)/p-InGaAs MOS capacitors. ΔV- ΔV_0 increases with a power law dependence with the increasing t_{stress} at the initial stage of stressing and tends to reach a plateau at sufficiently long stress times.

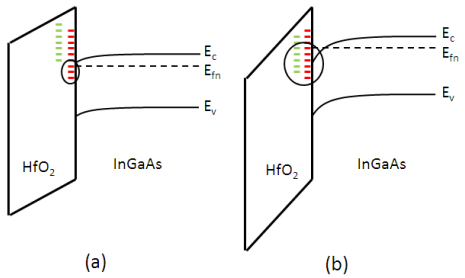


Fig.5 : Simplified band diagrams of HfO_2/n-InGaAs MOS capacitor which have (a) smaller E_{ox} and (b) larger E_{ox}. The border traps that are involved in the trapping process leading to C-V hysteresis are circled. Using a larger V_{max} thus a larger E_{ox} allows more border traps to be accessed, resulting in a larger ΔV.

It is noted in Fig.4 that using different V_{max} results in different saturation values at the plateau. Border

traps can be distributed at different energy levels and also at different depth into the oxide near/at the high-*k*/InGaAs interface (Fig.5). Firstly, using a larger V_{max} pushes the Fermi level further into the InGaAs conduction/valence bands, thus accessing border traps over a wider energy range resulting in a larger ΔV. Secondly, a larger V_{max} increases the electric field across the oxide (E_{ox}), which can result in additional oxide traps being aligned with the Fermi level at the high-*k*/InGaAs interface during the stress (see Fig.5).

5. Conclusion

C-V hysteresis measurements were performed on Pd/HfO_2/InGaAs/InP MOS capacitors. The C-V hysteresis corresponds to a charge trapping level comparable to or even greater than the typical D_{it} in high-*k*/InGaAs MOS systems, indicating the importance of C-V hysteresis behavior. The results indicated that the trapping occurs primarily in a plane near/at the HfO_2/InGaAs interface and not distributed throughout the oxide, indicating that the engineering of the interface transition region between the HfO_2 and the InGaAs is central to minimizing C-V hysteresis and thus device instabilities. In addition, $\Delta V - \Delta V_0$ increases with a power law dependence on stress time in accumulation and approaches to a plateau at sufficiently long stress times, consistent with trapping in pre-existing border traps which have a wide range of capture cross sections. A larger V_{max} used in the study of C-V hysteresis with a hold at V_{max} in accumulation results in a larger ΔV. This is because a larger V_{max} results in a larger E_{ox} which allows more border traps to be assessed.

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