# Packaging Design Challenges of High-Density High-Speed Silicon Photonic Receiver

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ABSTRACT:
We report on the first optically and electrically packaged prototype of the 48-channels silicon photonic single mode receiver device. The receiver device, measuring 11.8 mm x 32 mm, has 48 monolithically integrated Ge p-i-n photodetectors, 144 Al bond pads along three edges and 50 input grating couplers (including alignment shunts) located in the middle. The first receiver package prototype utilised short-length Au wire bonding from device bond pad to high speed board with edge SMP terminations. A 64-channel angle-polished fibre array was coupled permanently, with fibre-to-fibre transmission loss of 8.15 dB recorded through the alignment shunt. The current prototype package was able to conservatively support an aggregated data rate up to 480 Gbps (10 Gbps per photodetector). This paper discusses the design, process and materials integration of the prototype package, as well as the challenges encountered with respect to packaging. Results and analyses of the current prototype are also discussed.

## INTRODUCTION

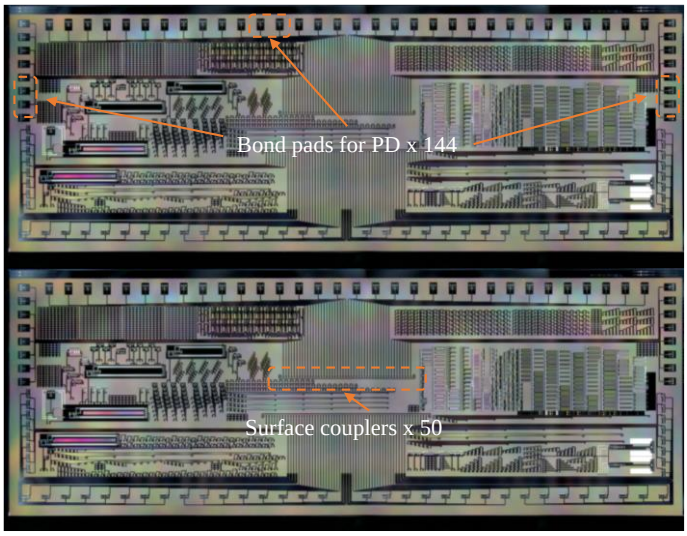


Fig. 1. Receiver device with locations of bond pads and surface couplers respectively. The device consists of 50 optical I/Os and 144 electrical I/Os.

Silicon photonics have grown by leaps and bounds since its first demonstration three decades ago [1], with more applications being developed and applied each day. For instance, the optical transceiver market "was valued at US$ 2.71 B in 2015 and is expected to reach US$ 6.87 B by 2022, driven by the rise in Internet penetration and data traffic" [2]. At the same time, monolithically integrated silicon photonics has become increasingly attractive due to its potential to lower fabrication cost while packing more functionalities on a single chip [3]-[5]. An example that had been demonstrated was the receiver device that was being used in this packaging prototype and its transmitter sibling [6]. The receiver device, measuring 11.8 mm x 32 mm, has 48 monolithically integrated Ge p-i-n photodetectors, 144 Al bond pads along three edges and 50 input grating couplers (including alignment shunts) located in the middle. The transmitter device, on the other hand, has 48 Mach-Zehner modulators, 336 Al bond pads (48 differential pairs, 96 thermal phase tuners, 2 grounds) along all edges and 62 input grating couplers on a compact size of 13.2 mm x 32 mm. In this article, the authors first described the packaging design, process flow and assembly challenges of the receiver device before proposing some new concepts that can be adopted for the transmitter device in the future.

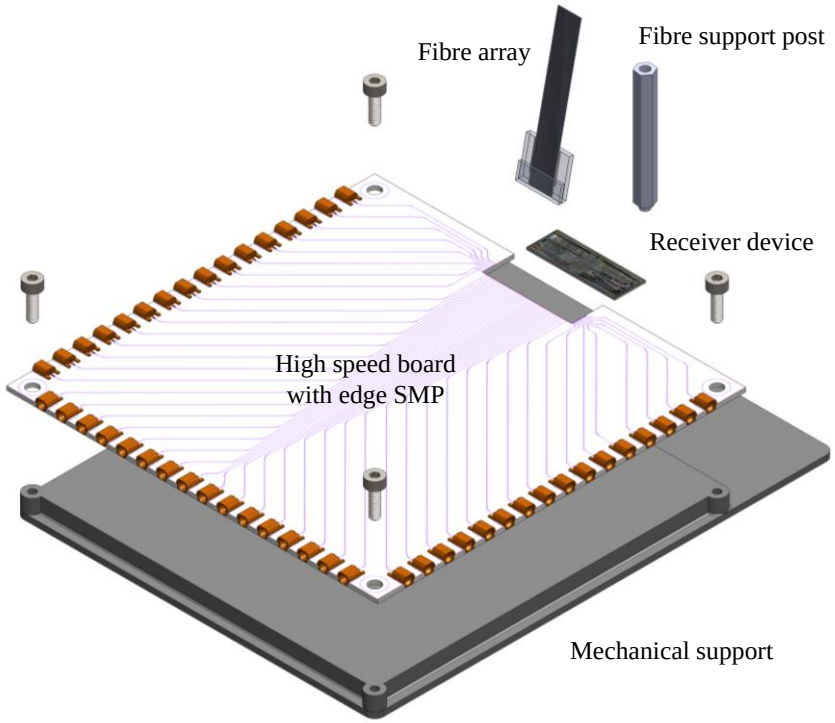


Fig. 2. 3D model of prototype 1 receiver package assembly.

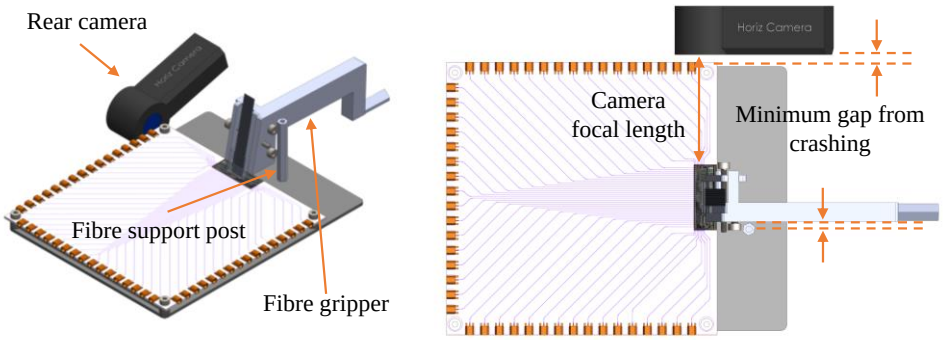


Fig. 3. Assembly design rule check (equipment constraints) for fibre alignment to confirm that no obstruction occurs during fibre alignment and epoxy dispensing.

In this first packaging prototype, the authors proposed that direct wire bonding (Fig. 2) rather than flip chip bonding to high speed board or interposer to be used for the following reasons. First of all, due to the location of the optical I/Os in the middle of the device, a punched hole on the board or interposer will be required under the flip chip configuration. Silicon photonic devices that had been flip chip packaged had their optical ports arranged at the edges and away from electrical bond pads, such as that found in [7], [8]. Alternatively, a pluggable approach such as that proposed in [9] can be adopted but it will have to be flip-chip configured. Secondly, the device bond pads came in aluminium metallization, meaning that post-processing such as gold-stud bump, copper pillar with solder cap or electro-less plating in the form of ENIG is required. At the same time, assuming that the above can be done, the total number of solder joints on the device is unlikely to be able to support such a large device without the use of underfill, which has to be properly dispensed and cured in order to not cover the optical I/Os. Lastly, a flip chip configuration for this device will also block the field of view during fibre alignment and fixing.

Fig. 3 further shows the additional challenges and considerations in designing the prototype package, in the form of fibre alignment equipment constraints such as camera focal length and travel distance of the camera and fibre alignment arm. Other items that were considered but not shown include (a) length of wire bond from device to board, (b) packaging process sequence, (c) overall board size to cater for 48 edge SMPs while meeting

both equipment, process and electrical performance constraints, (d) location of fibre support post, (e) ease of testing and also (f) the ability to survive shipment. Ultimately, the size of the board was fixed at 129 mm x 128 mm, a 64-channel 12 ° polished fibre array was used and a raised step on the mechanical support whereby device will be located was added to level the surface of the device with the board. Designs for components were then sent to the supply chain for fabrication.

## PACKAGING AND ASSEMBLY PROCESSES

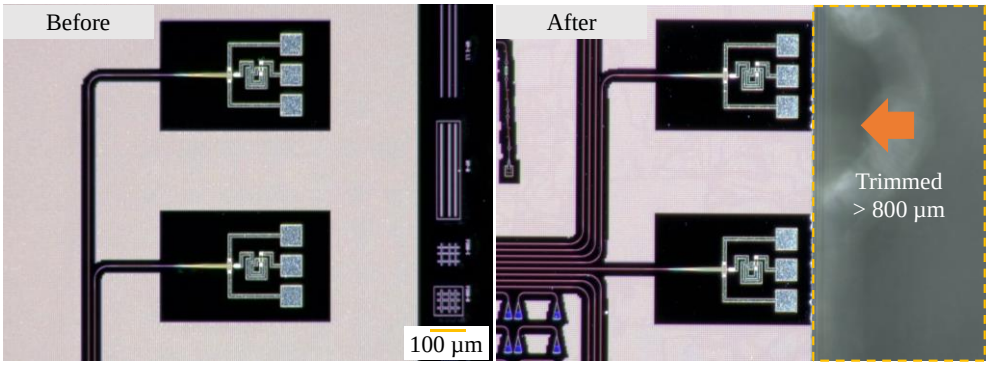


Fig. 4. Trimming of unnecessary silicon material from PD bond pads to minimise bond wire length.

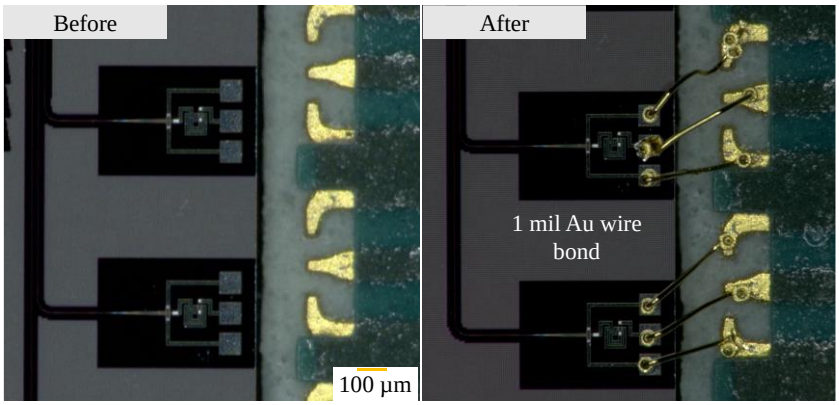


Fig. 5. Minimizing gap between device and test board for Au wire bonding. There is a slight mismatch on the board bond pads due to fabrication tolerances.

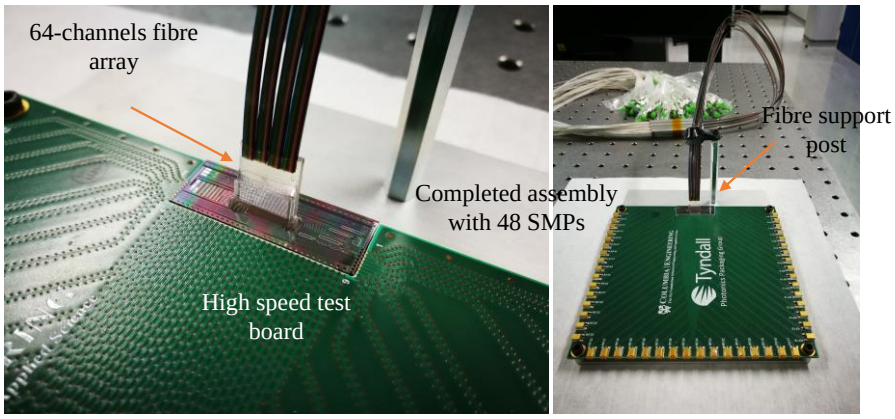


Fig. 6. Completed prototype receiver package, ready for testing.

Prior to packaging and assembly, excess silicon material beyond bond pads were trimmed in order to minimise the bond wire length (Fig. 4). The two rounded corners of the slot on the test board, whereby the device will be located were also carefully polished to make sure that the device can be placed as close to the board edge as possible. The packaging was then performed in the following order – (a) board mounting onto mechanical support, (b) device mounting on the raised step of mechanical support, (c) gold wire bonding (Fig.

5), (d) fibre alignment and fixing and (e) fibre support post mounting and fixing fibre ribbons. The final assembled prototype package is shown in Fig. 6 and ready for testing.

## EXPERIMENTAL SETUP AND PERFORMANCE EVALUATION

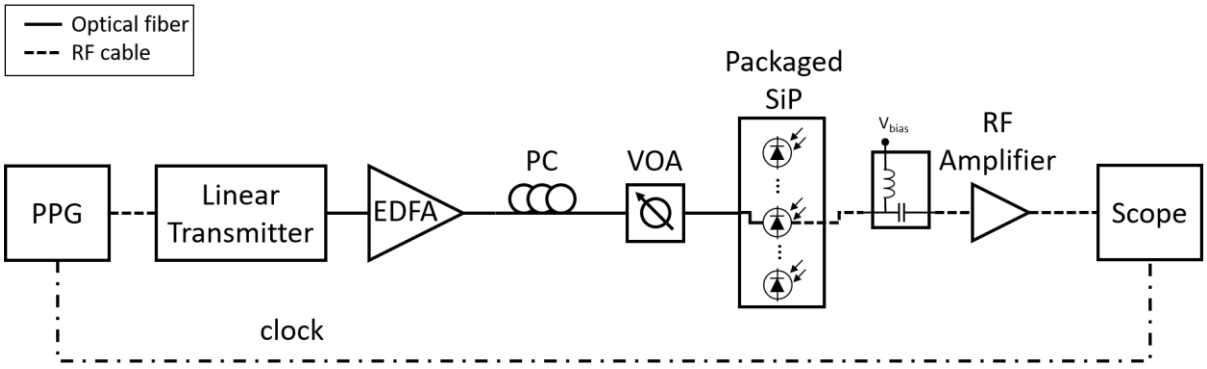


Fig. 7. Schematic of the experimental setup.

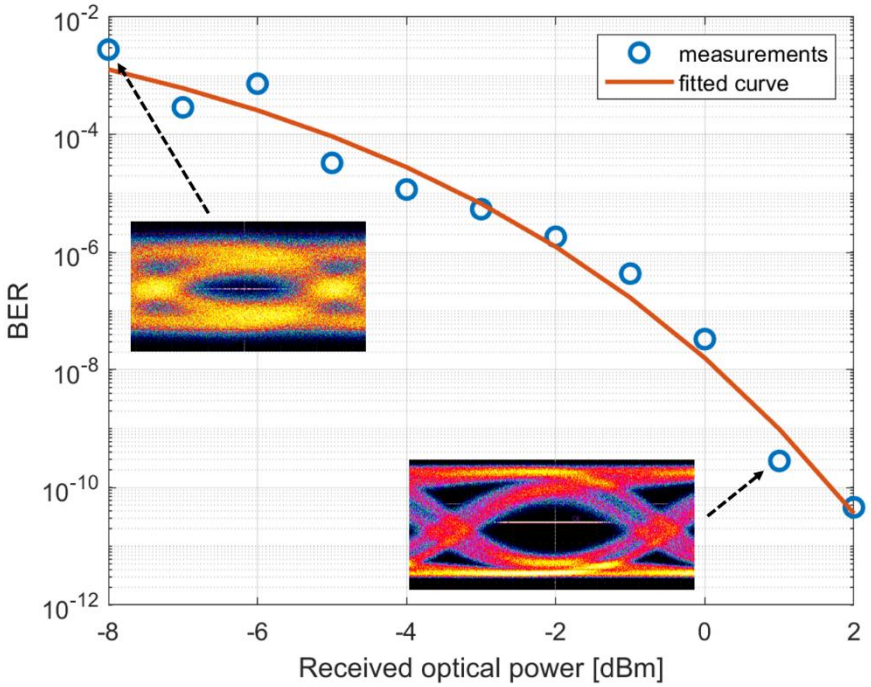


Fig. 8. The sensitivity measurements of the packaged receiver. Insets: eye-diagrams of the received signal.

A schematic of the experimental setup to test the packaging performance of the silicon photonics (SiP) device is shown in Fig. 7. A pulse pattern generator (PPG) (Anritsu MU181020B) is used to generate a 10 Gbps on-off-keying non-return to zero (OOK-NRZ) pseudo random bit sequence (PRBS) at a length of $2^{31}$-1. 10 Gbps was also previously found to be the optimum speed for energy transfer [10]. The electrical signal is injected into a linear reference transmitter (Thorlabs MX35E) to convert the electrical signal into the optical domain at a carrier at a wavelength of 1550.11 nm. The optical signal is then amplified by an erbium doped fiber amplified (EDFA) to overcome fiber coupling losses of 4.1 dB per grating facet. A polarization controller (PC) is used to set the optical carrier to the TE mode supported by the integrated grating coupler.

To measure the signal integrity in terms of eye-opening quality and estimated bit-error rate (BER) performance of the packaged silicon photonics receiver, a variable optical attenuator (VOA) is used to control amount of the received optical power. Following the characterization of the integrated photo-diodes, a reverse bias voltage of 1.5 V is applied to decrease the junction capacitance to ~0.6 fF/μm$^2$ resulting in a higher 3dB cut-off frequency performance [11]. The electrical output of the receiver is then amplified by an external limiting RF amplifier to increase the dynamic range. The amplified signal is measured by a sampling oscilloscope (Tektronix DSA8300), which is synchronized with the clock from the PPG.

The BER is estimated from the measured Q-factor using the mapping equation $BER = 0.5 \cdot \mathrm{erfc}(Q/\sqrt{2})$. Figure 8, shows the sensitivity measurements of the packaged receiver with the blue circles

indicate measured results and the red curve is the fitted sensitivity. The eye-diagrams in the insets of Fig. 8 show the received signal at -8 dBm and 1 dBm measured at the output of the VOA and the corresponding injected power to the receiver is –12.1 dBm and –3.1 dBm, respectively.

## FUTURE WORKS

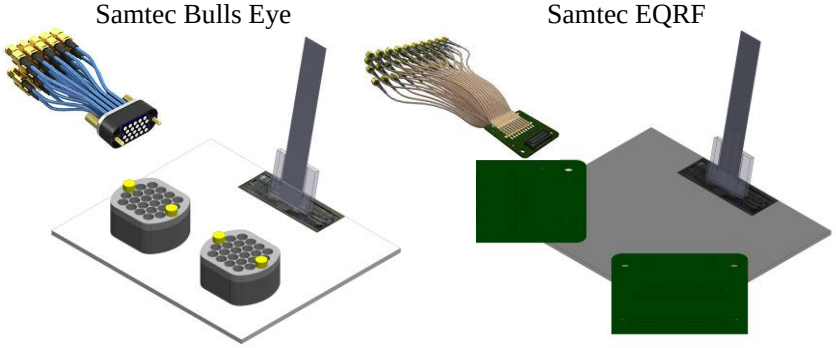


Fig. 9. Future packaging prototype using Samtec's Bulls Eye and EQRF components.

In the future, the authors plan to further reduce the size of the high-speed board as well as the transmission line length. The two proposed prototype concepts (Fig. 9) will swap edge SMPs with Bulls Eye [12] and EQRF [13] cables from Samtec in order to achieve higher data than the current 10 Gbps per channel demonstrated. Non-optimized design has found that the length of transmission line on high-speed board can be reduced by 50%. Secondly, these approaches will also allow the subsequent demonstration of the transmitter device that was developed concurrently with the receiver using the same platform. The transmitter device came with 48 differential pairs (GSGSG) for the modulators and additional DC connections that have to be connected to a board. Using the current edge SMP design, the board will have to be designed to accommodate 96 edge SMPs and becoming unrealistically large, therefore a more compact packaging solution such as that proposed is needed.

## CONCLUSION

In this work, the authors had designed, packaged and tested the first 48-channels silicon photonic single mode receiver device prototype through the use of direct wire bonding between the device and high-speed board populated with edge SMPs. The developed prototype is capable of receiving at least 480 Gbps. The processes and challenges involved in this development were discussed and elaborated. Future designs for a more compact high-speed silicon photonics packaging were also proposed.

## ACKNOWLEDGEMENT:

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