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Design and Analysis of a Photon Counting System using Covered Single Photon Avalanche Photodiode

Shijie Deng, Xiang Li, Alan Morrison, Ming Chen, Hongchang Deng, Chuanxin Teng, Houquan Liu, Ronghui Xu, Yu Cheng and Libo Yuan

***Abstract*—A photon counting system using covered single photon avalanche diode (SPAD) based on a standard IC process (0.18 μm) is designed and analysed in this work. The SPAD is formed using the medium voltage (MV) doping layers of the process. To reduce the dark count rate (DCR) in the SPAD, a shaded SPAD with the same structure is fabricated on the same chip which is covered by a metal layer and only providing DCR for the DCR correction. This DCR provided by the shaded SPAD can be also used for the real-time on chip monitoring of some other parameters such as temperature, breakdown voltage and afterpulsing probability. Experimental results show that the SPAD developed is able to detect the visible light from 450 nm to 850 nm with a 35 % peak photon detection probability achieved at around 550 nm with bias voltage of 16 V (excess voltage of 3 V). A timing jitter of 176 ps is measured with an excess voltage of 3 V. The dark count rate in the SPAD tested is about 1.38 cps/μm^2 with excess bias voltage of 1 V and 14.62 cps/μm^2 with the excess bias voltage of 3 V without the DCR correction. Results also show that a reduction of more than 85 % in the DCR (background noise) can be achieved when the DCR correction is applied resulting in a DCR of 1.68 cps/μm^2 with excess bias voltage of 3 V. By monitoring the DCR of the shaded SPAD, the breakdown voltage and temperature of other on chip SPAD can be measured. The potential usefulness of the afterpulsing probability monitoring using the shaded SPAD and the crosstalk probability between SPADs on the chip are analyzed. In addition, the effects of process variations on the SPAD performance is investigated by testing 10 chips with the same SPADs fabricated and potential method is proposed for alleviating the process variations in the SPAD arrays.**

***Index Terms*—Dark count rate correction, temperature monitoring, breakdown voltage, afterpulsing effect, SPAD arrays.**

I. Introduction

SINGLE photon detection technology is widely used in low light sensing applications such as laser ranging [1], DNA sequencing [2], quantum key distribution [3] and medical imaging [4]. In recent years, the single-photon avalanche diode has been used to replace photomultiplier tube (PMT) or micro-channel plate (MCP) in photon counting applications because of its low bias voltage, low power consumption and easy integration with electronic circuits [5-7]. Since 2003, various SPADs based on standard IC processes (such as the CMOS process) have been developed making it possible to integrate the SPAD, avalanche event sensing circuit, quenching circuit and back-end signal processing circuit on the same chip and highly integrated and low-cost single photon detection systems based on the CMOS process can be realized [8-12]. One of the major drawbacks in CMOS SPADs is the high dark count rate which is mainly caused by its fixed doping profile, the injection depth of each layer, as well as the limitation of the design rules (such as metal density), which means the CMOS SPAD can be easily affected by thermal carrier excitation and tunneling effects. Since the high DCR reduces the signal-to-noise ratio (SNR), increases the bit error rate and reduces the detection sensitivity of a photon counting system, the DCR in a SPAD needs to be minimised. In the comparison of SPADs fabricated by different IC process technologies, larger process geometries (such as 0.13 μm, 0.18 μm and 0.35 μm) have a lighter doping profile and a more stable fabrication process, which make the SPADs developed in those processes show relatively better performance in terms of reliability and noise [21-25]. Nevertheless, those SPADs with low dark count rates require high voltage to operate, and their dark count rates are still in the tens to hundreds of counts per second (counts/s) for a single SPAD, which makes the overall dark count rate still considerable when they are used in SPAD arrays. In addition, parameters such as chip temperature, breakdown voltage and afterpulsing probability are important to the SPAD's performance and real-time monitoring of those parameters can be very useful for optimization of the photon counting system's overall performance.

In this work, an optimised photon counting system using covered SPAD is designed and analysed. The SPAD can achieve the peak detection efficiency of 35 % at around 550 nm, and the detectable spectral range of the SPAD is from 450 nm to 850 nm. The breakdown voltage of the SPAD is around 13 V and its timing jitter measured is 176 ps when the SPAD operates at an excess bias of 3 V. The DCR are 1.38 cps/μm^2 (counts/s · μm^2) with an excess bias voltage of 1 V and 14.62

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cps/μm^2 with an excess bias voltage of 3 V respectively. In order to further reduce the DCR and monitoring important parameters of the SPAD, identical SPADs are fabricated on the same chip, with one covered by a metal layer to be kept in the dark. Both SPADs are connected to the same bias voltage and for counting avalanche events. Since the identical SPADs have similar performance characteristics in terms of breakdown voltage, dark count rate and afterpulsing probability. The dark count rate recorded from the shaded SPAD can be used to estimate, in real time, the dark count of the other SPADs, thereby to be used to reduce the dark count rate of the whole chip. Results show that more than 85 % DCR reduction can be achieved, resulting in a DCR of 1.68 cps/μm^2 at an excess bias voltage of 3 V. By analyzing the DCR of the shaded SPAD, the breakdown voltage and temperature of the on chip SPAD can be measured which can be very useful for the optimization of the whole photon counting system. The potential usefulness of the afterpulsing probability monitored using the shaded SPAD and the crosstalk probability between SPADs on the chip are analyzed. In addition, the effects of process variations on the SPAD performance is investigated by testing 10 chips with the same SPADs fabricated and potential method is proposed for alleviate the process variations in the SPAD arrays.

The structure of the paper is as follows: the design of the system is described in Section II, Section III presents the measurement method for estimating the system's performance parameters, and the experimental results and the analysis are shown in Section IV. The comparison of the designed system with the state of art SPAD and the commercial SPADs is also added in Section V.

II. Design Description

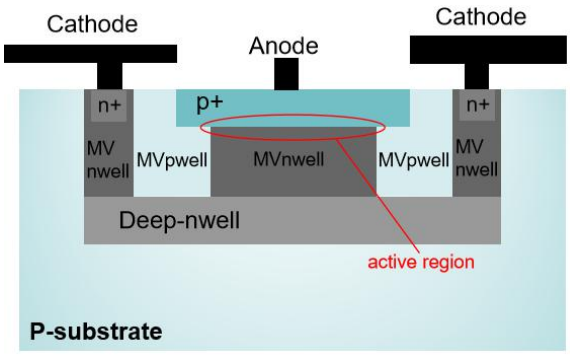


Fig. 1. Cross section of the developed SPAD.

The cross section of the developed SPAD can be seen in Fig. 1. In the standard 0.18 μm BCD (Bipolar-CMOS-DMOS) process used, there are 3 different kinds of doping layer available: low voltage (LV), medium voltage and high voltage (HV) process for the MOS transistors operate up to 1.8 V, 5 V and 60 V. In this design we chose the medium voltage process for forming the SPAD, since it can lower the breakdown voltage compared to the high voltage process, which makes the SPAD has lower power dissipation and it will be easier to design its back end circuitry. In the meantime, its lighter doping profile (compared to the standard voltage process) makes it possible to achieve a relatively low dark count rate in the SPAD. In the device, a p+ implant layer forms the central active area and the depletion region with the MV-nwell layer. An MV-nwell layer is also used with the Deep-nwell and n+ implant layers to form the cathode of the SPAD. MV-pwell layers are used as the guard-ring to prevent the edge breakdown surrounding the p+ active area. The small geometries process geometries (e.g. deep-submicron process) will result in higher doping profile layers, which will make the SPAD designed based on those process have higher dark count rate performance [31, 32]. However, if the geometries process used is too large, when the related circuits (avalanche events sensing circuit, quenching circuit and back-end signal processing circuit) are integrated with the SPAD, the overall layout of the chip would be very large and the fill factor would be affected. This would also limit the usefulness for the design to be used in large SPAD arrays systems. As a trade-off between the performance of the SPAD and the integration possibility of the whole system, we selected the 0.18 μm process.

To further reduce the noise in the SPAD and makes the real-time breakdown voltage and on chip temperature monitoring available, a shaded SPAD with the same structure is fabricated on the same chip which is covered by a metal layer and only measures dark count rate, see Fig. 2. As the SPADs are fabricated on the same chip with the same structure, their performance is similar and the DCR from the shaded SPAD can be used to correct the noise performance of other normally operating SPADs.

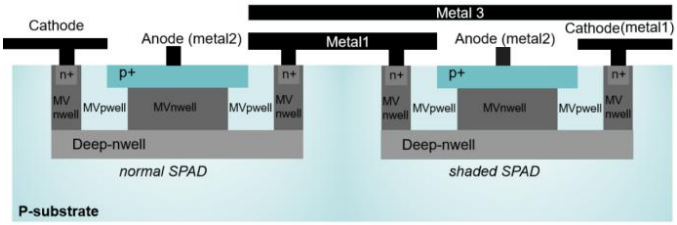
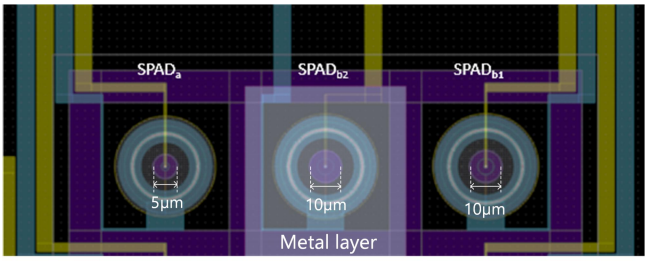
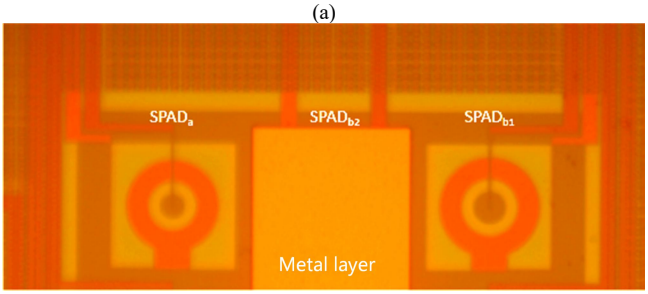


Fig. 2. Cross section of two identical SPADs with one is shaded.



(a)



(b)

Fig. 3. (a) layout and (b) die photograph of the developed SPADs.

The layout and the die photograph of the developed SPADs are presented in Fig. 3. Three SPADs with the same structure

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are fabricated. $SPAD_a$ is with 5 μm diameter active region, $SPAD_{b1}$ is with 10 μm diameter active region and $SPAD_{b2}$ is the same size as $SPAD_{b1}$ but covered by a metal layer. The performance characteristics of $SPAD_a$ were firstly evaluated. Then the $SPAD_{b2}$'s DCR is used for the dark count rate correction in $SPAD_{b1}$. 10 SPAD Chips are measured to evaluate the effects of process variations on the SPAD's performance.

III. Experimental Measurement Method

Photon Detection Probability

In the Photon detection probability (PDP, described as the ratio of the number of detected photons and the number of photons incident on the photoactive area) measurement, a broad-spectrum light source is used to provide the incident light to the SPAD through one port of an integrating sphere. Optical band-pass and attenuation filters are used to select the specific wavelength and alter the incident light power intensity. An optical power meter is used to monitor the incident power from another port of the integrating sphere. This monitored power together with the photoactive area of the optical power meter's detector head will be used to calculate the photons intensity directed to the active area of the SPAD. For each selected wavelength, the incident photons per second and the photon counting rate (overall counting rate - dark count rate) at the output of the SPAD are measured and the PDP is calculated.

Timing Jitter

To measure the timing jitter of the SPAD, a pulsed laser (660 nm) is used to generate pulsed incident light to the SPAD and its synchronized pulse is sent to a time correlated single photon counting (TCSPC) instrument. The time delay between the laser's synchronized pulses and the pulses from the SPAD's readout circuit are recorded by the PC through the TCSPC (see Fig. 4). The delay time histogram distribution is built for the timing jitter calculation.

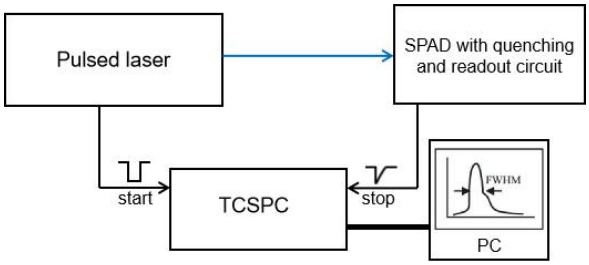


Fig. 4. Experimental setup for measuring the timing jitter of the SPAD.

Dark count rate

The SPAD's DCRs is as a Poisson distribution, which can be expressed as [13, 14],

$$P(X=k) = -\lambda^k e^{-\lambda} / k! \quad (1)$$

where X is the random variable representing DCRs of SPAD, P is the probability to have a DCR of K, and λ is the mean of DCRs. The DCR of SPAD is not a fixed value, but fluctuates in a range, therefore, the mean value of DCRs is used. Because $SPAD_{b1}$ and $SPAD_{b2}$ (metal covered SPAD) have the same structure, the performance of DCR of $SPAD_{b1}$ and $SPAD_{b2}$ should be the similar. When the DCR of $SPAD_{b1}$ (DCR_{b1}) and DCR of $SPAD_{b2}$ (DCR_{b2}) are measured, the corrected DCR of $SPAD_{b1}$ (DCR_{cb1}) can be calculated by the following formula,

$$DCR_{cb1} = DCR_{b1} - DCR_{b2} \quad (2)$$

Breakdown Voltage

The breakdown voltage has a linear relationship with temperature, which can be described as [15, 16],

$$V_B = V_{B0}\left[1 + \beta(T - T_0)\right] \quad (3)$$

where V_{B0} is the breakdown voltage at T_0, and β is the temperature coefficient.

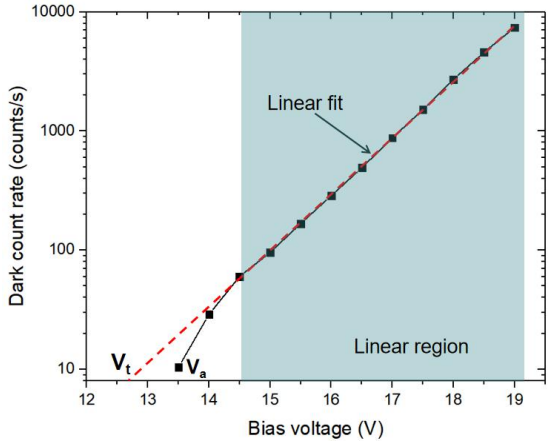


Fig. 5. Measurement and calculation of the breakdown voltage.

As can be seen form Fig. 5, the measurement of the breakdown voltage can be achieved using the following steps:

1. Identify the "bias voltage" vs "DCR" linear region of the shaded SPAD in advance. Chose at two points (V_{b1}, DCR_1) and (V_{b2}, DCR_2) in the plot and calculate the breakdown voltage as by using these data points, a linear expression for the DCR:

$$DCR = a \times V_b + b \quad (4)$$

And the breakdown voltage (Vt) can be derived, by setting the DCR to 0 in the expression, the breakdown voltage can be calculated:

$$V_t = -b/a = V_{b1} - (V_{b1} - V_{b2})/(1 - DCR_2/DCR_1) \quad (5)$$

2. Sweep the bias voltage and recorded the DCR in the shaded SPAD. Applied the linear fit region by region (e.g. every 1 V range of the bias voltage) and find the linear expression for the linear region (if the fitting is in the linear region, the fitting results would be very similar). Finally derive the breakdown voltage by using the linear expression. For the on-chip temperature monitoring, a series of temperature versus true breakdown voltage data will be recorded and plotted. A linear fit to the data will be produced. By using this linear fitting data together with the real time measured breakdown voltage, the real-time on chip temperature can be achieved.

Crosstalk

When an avalanche event is triggered, a large number of carriers are generated in the SPAD (source pixel), and these carriers may recombine and emit photons. These photons can cause an avalanche event in the adjacent SPAD (detector pixel), which is called crosstalk,the process of crosstalk can be described by the equation [18],

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$$P_{crosstalk} = P_{generation} \times P_{pass} \times P_{absorb} \times P_{avalanche} \quad (6)$$

in which $P_{generation}$ is the recombination probability of multiplied photo-carriers in the source pixel, P_{pass} is the probability of a photon propagating to the adjacent detector pixel, P_{absorb} is the absorption probability of photons by the detector pixel and $P_{avalanche}$is the probability that a photon could trigger an avalanche event. $P_{generation}$ and $P_{avalanche}$ are related to the bias voltage of SPAD. To study the influence of crosstalk on the DCR in SPAD, the crosstalk probability (CTP) is measured in the following two cases: (1) CTP_1, $SPAD_{b2}$ is used as the source pixel and $SPAD_{b1}$ as the detection pixel; (2) CTP_2, $SPAD_{b1}$ is used as the source pixel and $SPAD_{b2}$ as the detection pixel. First, the source pixel and the detector pixel are biased by the same voltage, and the DCR_1 of the detector pixel is measured. Then, the source pixel is closed, and the DCR_2 of the detector pixel is measured. The crosstalk count rate is obtained by DCR_1 - DCR_2, and the crosstalk probability is (DCR_1 - DCR_2) / DCR_1.

Afterpulsing probability

When avalanche occurs in SPAD, any trap in the multiplier region will become the carrier trapping center and when a large number of charges pass through SPAD, some carriers will be trapped by these traps. If the avalanche process is suppressed, these traps begin to release carriers. If they are accelerated by the electric field, they will trigger the avalanche again and generate pulses independent of photon incidence.

In avalanche process, some carriers will be captured by the traps in SPAD, and the trapped carriers are released to the avalanche events, which is called afterpulsing. The afterpulsing probability can be described as [19],

$$P_{ap}(t) = B + A_1 \exp(-t/\tau_1) + A_2 \exp(-t/\tau_2) + \cdots \quad (7)$$

in which B is the DCR; A_1, A_2, … are the initial values of amplitudes of the different exponential components; τ_1, τ_2, … are the lifetime of different traps, and τ_i can be described by the Arrhenius equation [20],

$$\tau_i = C \cdot \exp(E_a / kT) \quad (8)$$

where E_a is the activation energy of the i-th trap, k is the Boltzmann constant, T is the temperature and C is related to trap cross section, the relevant effective state density and temperature. Different traps in SPAD have different lifetime, and each trap's lifetime is related to temperature. The carrier generated by photon count and dark count will be captured by these traps and will cause complex afterpulsing effect. To evaluate the afterpulsing probability of the designed SPADs, we applied a laser (660 nm) with a power of 400 nW to $SPAD_{b1}$ and $SPAD_{b2}$, and measured the afterpulsing probability for different bias voltages.

The measurement method of afterpulsing probability we used is similar to the typical measurement method in the literature [19, 26, 27]. The SPAD's output is connected to two channels (start channel and stop channel) of a time to digital converter (TDC, Tektronix FCA3100), the TDC records the time delay between adjacent output pulses of SPAD. A large number of data are used to establish the histogram, and the afterpulsing probability is calculated by formula,

$$P_h(n) = [1 - e^{-\mu s \Delta t} e^{-\mu d \Delta t} (1 - p_a(n)] \times \prod_{i=1}^{n-1} [e^{-\mu s \Delta t} e^{-\mu d \Delta t} (1 - p_a(i))] \quad (9)$$

where n and i are the sampling interval index (the time delay is divided into n or i sampling intervals); $P_h(n)$ denote the probability of an event to occur n sampling intervals; $P_a(i)$ is the probability to detect an afterplusing count in the i-th sampling intervals. μs is the detected photon count rate, μd is the dark count rate. Δt is the width of the sampling interval [26].

IV. Experimental Results

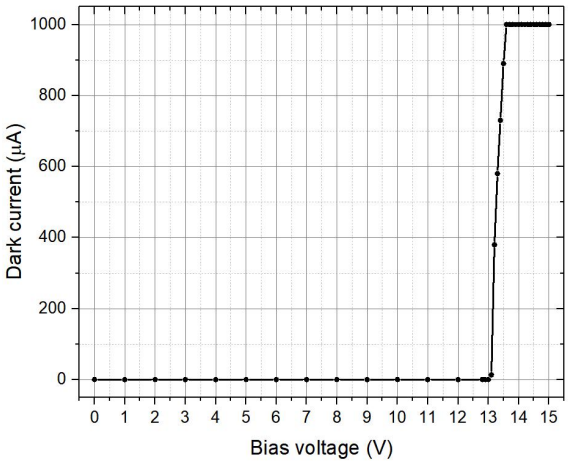


Fig. 6. IV plot of the dark current and breakdown voltage of the SPAD developed.

The IV plot of the dark current and breakdown voltage of the SPAD developed can be seen in Fig. 6. Results show that the SPAD is with a breakdown voltage of around 13 V. The $SPAD_a$'s dark count rate as a function of the bias voltage applied to its cathode, see Fig. 7. In the measurement, the SPAD's anode is connected in series with a resistor of around 100k ohm for passive quenching. Results show that when the excess bias voltage is 1 V (bias voltage is 14 V), the SPAD can maintain a low dark count rate of about 27 counts/s, corresponding to about 1.38 cps/μm^2. With the excess bias voltage of 3 V (bias voltage is 16 V), the dark count rate in the SPAD is about 287 counts/s, corresponding to a DCR of 14.62 cps/μm^2. Results also demonstrate that the device is able to operate at an excess bias voltage of up to 6 V (bias voltage is 19 V) with a DCR of about 7.4k counts/s.

The measured photon detection probability of the SPAD for different incident light wavelengths and reverse bias voltages are presented in Fig. 8, the SPAD developed can detect the visible light from 450 nm to 850 nm with a peak PDP of about 35 % at 550 nm when the bias voltage is 16 V.

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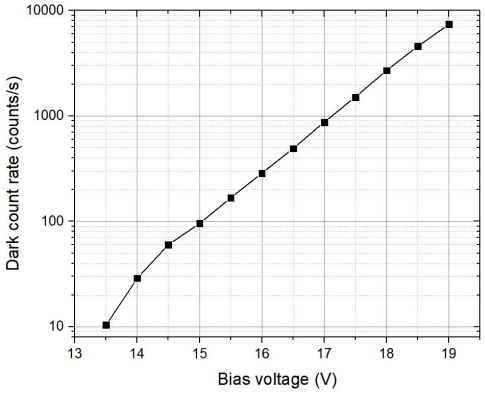


Fig. 7. $SPAD_a$'s dark count rate as a function of the bias voltages.

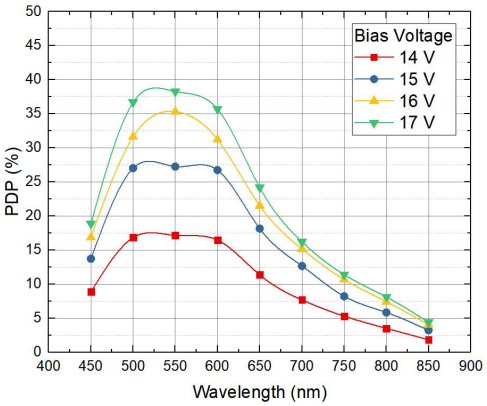


Fig. 8. Photon detection probability of the SPAD for different incident light wavelengths and reverse bias voltages.

The measured delay time histogram distribution of the SPAD is presented in Fig. 9, a short timing jitter of 176 ps at 3 V excess bias is achieved and a timing jitter of 190 ps is measured with an excess bias voltage of 1 V. These timing jitters measured are including the internal jitter of the TCSPC instrument which is about 60 ps.

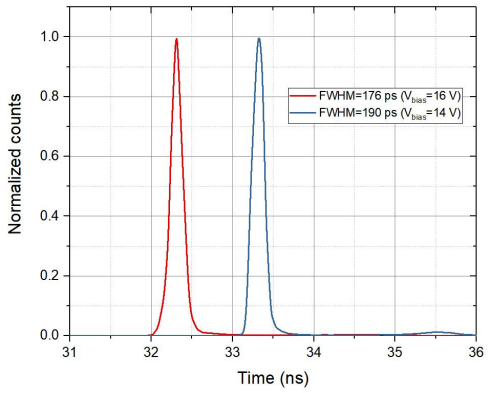


Fig. 9. Timing responses of the SPAD for different bias voltages.

As can be seen from Fig. 10, the measured DCR of $SPAD_a$ (5 µm diameter active area), $SPAD_{b1}$ (10 µm diameter active area) and$SPAD_{b2}$ (10 µm diameter active area with metal covered) for different bias voltages. In the experiments, 10 fabricated chips with the same design were tested. It is clear that the fabricated SPADs of the same structure and size show similar DCR performance with the maximum standard deviations of 584 counts/s, 3.6k counts/s and 3.1k counts/s for $SPAD_a$, $SPAD_{b1}$ and $SPAD_{b2}$ (over the bias voltage range from 13 V to 19 V), respectively.

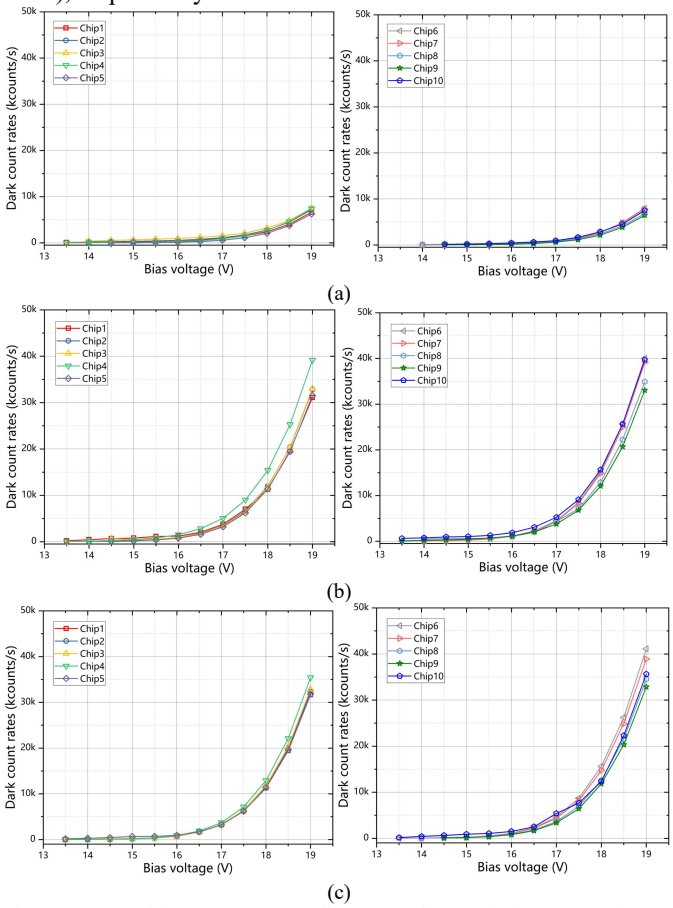


Fig. 10. DCR of (a) $SPAD_a$ (5 µm diameter active area), (b) $SPAD_{b1}$ (10 µm diameter active area) and (c) $SPAD_{b2}$ (10 µm diameter active area with metal covered) for different bias voltages.

The corrected DCR of $SPAD_{b1}$ by using the DCR measured in $SPAD_{b2}$ for different bias voltages, see Fig. 11. Results show that for most of the chips tested, the DCR in $SPAD_{b1}$ can be reduced to nearly 0 (near 90 % of the DCR reduction). Results also show that the corrected DCR in chip4 and chip10 show some increment when the bias voltage is above 17 V (this may due to the process variations), but more than 80 % DCR reductions can still be achieved. When this DCR reduction technology to be applied to SPAD arrays, to alleviate the process variation issue, a few shaded SPADs (with metal covered) may need to be used which should be distribute in different locations in the arrays chip and their average DCR can be used for the SPAD arrays overall DCR correction.

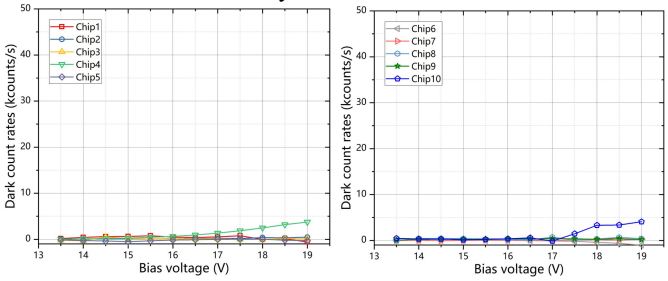


Fig. 11. Corrected DCR of $SPAD_{b1}$ by using the DCR measured in $SPAD_{b2}$ for different bias voltages.

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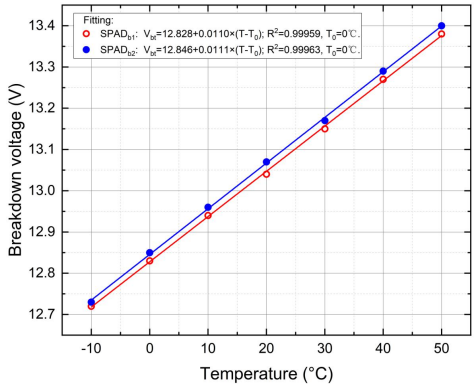


Fig. 12. Measured breakdown voltage of $SPAD_{b1}$ and $SPAD_{b2}$ for different temperature.

The measured breakdown voltage of $SPAD_{b1}$ and $SPAD_{b2}$ for different temperatures, see Fig. 12. In SPAD, the relationship between DCR and temperature can be described as [17],

$$DCR = A\exp\left(-E_A / K_B T\right) \tag{10}$$

where K_B is Boltzmann's constant, A is a constant and T is the absolute temperature in Kelvin. It can be seen that the DCR of SPAD depends on temperature, which makes it very necessary to monitor the temperature of SPAD. Linear fitting are used and the relationship between the breakdown voltage and the temperature is established and the results show that the relationship between breakdown voltage and temperature of $SPAD_{b1}$ and $SPAD_{b2}$ are very linear and consistent. In this way, the breakdown voltage of SPADs on the same chip can be monitored in real time. In addition, by using the fitting relationship, the temperature of the chip can be also monitored in real time.

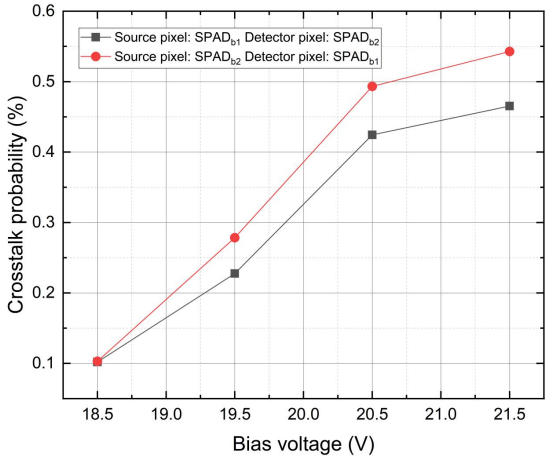


Fig. 13. Measured CTP_1 and CTP_2 for different bias voltage.

The measured CTP_1 and CTP_2 for different bias voltage are shown in Fig. 13, CTP_1 is 0.103 % and CTP_2 is 0.102 % as the bias voltage is 18.5 V, and CTP_1 is 0.543 % and CTP_2 is 0.465 % as the bias voltage is 21.5 V. It can be seen that the crosstalk effect in the designed SPADs is weak, when the SPAD's bias voltage is set at a high level, the crosstalk will have a slight impact on the SPAD's dark count noise.

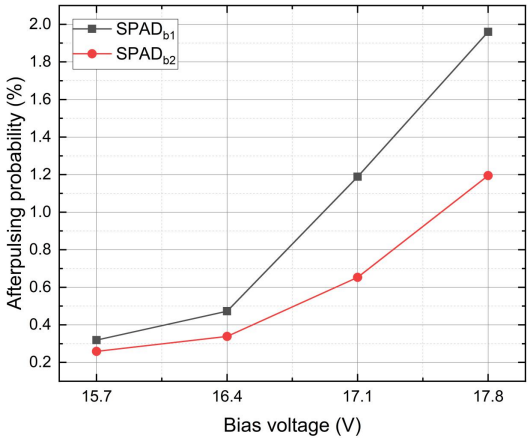


Fig. 14. Measured afterpulsing probability of $SPAD_{b1}$ and $SPAD_{b2}$ for different bias voltage.

Fig. 14 shows the results of the measurement, the afterpulsing probability of $SPAD_{b1}$ is 1.96 % as the bias voltage is 17.8 V, and the afterpulsing probability of $SPAD_{b2}$ is 1.195 % as the bias voltage is 17.8 V. The afterpulsing probability of $SPAD_{b1}$ is higher than that of $SPAD_{b2}$, which means that in the case of light incident, the carriers caused by photon counts will increase the afterpulsing effect, and afterpulsing caused by photon incidence cannot be corrected by $SPAD_{b2}$.

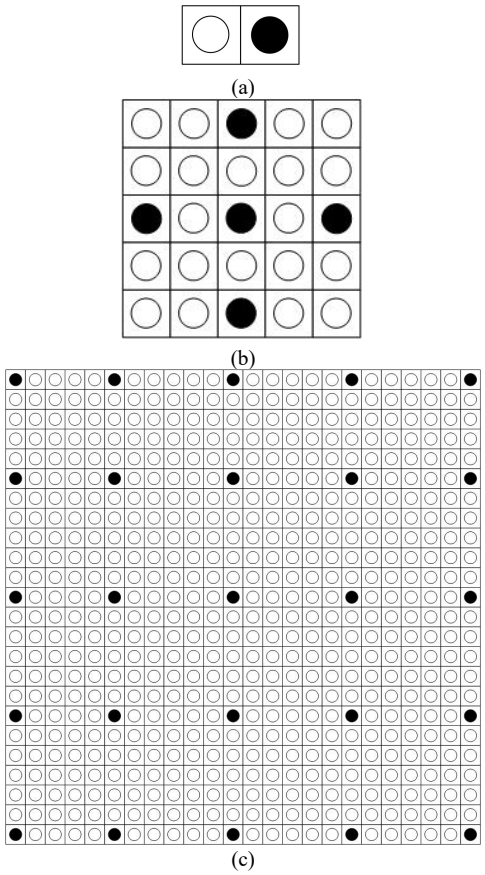


Fig. 15. Configuration of the proposed technology when it's used in SPAD arrays.

When the technology proposed in the SPAD arrays, some shaded SPAD will be selected which should be distributed around the whole SPAD arrays chip as shown in Fig.15 (b) and

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(c) to alleviate the affection of the process variations in CMOS process (since the process variations in CMOS process follows a circular profile). The shaded SPADs' dark count rates will be recorded, averaged and used for the noise reduction of the overall SPAD arrays chip. In addition, since the dark count rates of the shaded SPAD is only responding to the bias voltage and temperature, real-time monitoring of the SPAD chip's parameters such as on-chip temperature and breakdown voltage will be possible.

The PDP won't be affected by proposed DCR reduction technology, but, the PDE (photon detection efficiency, described as PDP × "fill factor") will be affected. The shaded SPADs won't response to the light illuminated which will lead to a reduction of the fill factor and thus the PDE. When the number of the on chip SPADs is small, even one or few SPADs covered in dark will significantly affect the overall PDE. For example, as shown in Fig. 15 (a) and (b), in the dual-SPAD chip, the fill factor will be reduced by 1/2 and in a 5×5 SPAD arrays, the fill factor will be reduced by 20 %. One solution might be useful is to place the un-shaded SPADs in the centre of the SPAD chip and use micro-lens to focus the incident light to them. However, for the larger SPAD arrays, for example a 24× 24 SPADs arrays shown in Fig. 15 (c), the fill factor will be only reduced by about 2.8 %.

The DCR reduction mechanism in the proposed technology can be used for the intensity measurement of the SPAD based photon counting system and it's not suitable for the time-resolved detection noise reduction. However, the ability of the real-time monitoring of the important parameters such as breakdown voltage, on chip temperature and afterpulsing that would make this technique very useful for the performance optimization of the whole photon counting system when it's used in varying environments.

V. State of the Art Comparison

TABLE I Performance comparison of the SPAD developed with state-of-the-art SPADs fabricated in standard IC technologies and commercial SPADs.

	[22]	[23]	[24]	[33]	[28]	[29]	[30]	This work
Process Technology	180 nm	160 nm	140 nm	65 nm	Hamamatsu	Laser components	Thorlabs	180 nm
Breakdown voltage (V)	47.5	36	11.3	9.6	42	125	-	13
Dark count rate (cps)	3.18 cps/μm²	0.2 cps/μm²	1.2-396.1 cps/μm²	73 cps/μm² (Vex=2V)	0.26-0.69 cps/μm² (Vex=5V)	0.051 cps/μm² (Vex=2V)	0.19 cps/μm²	1.38 cps/μm² (Vex=1 V) ***0.179 cps/μm² (Vex=1 V, with DCR correction)*** 14.62 cps/μm² (Vex=3 V) ***1.68 cps/μm² (Vex=3 V, with DCR correction)***
Maximum PDP (%)	17.5 % @600 nm	31-58 % @450 nm	26 % @500 nm	9.2 %@480 nm	40 % @600 nm	65 % @830 nm	35 % @500 nm	17 % @550 nm,Vex=1 V 35 % @550 nm,Vex=3V
Timing jitter	152 ps	39 ps	119 ps	158 ps	-	-	-	176 ps

Table I shows the performance comparison of the SPAD developed in this work with other state-of-the-art SPADs [22-24, 33] fabricated in standard IC technologies and commercial SPAD [28-30]. The table shows that the SPAD developed in this work can produce a comparable performance in terms of PDP, timing jitter and DCR with relatively low bias voltage (the low operation voltage makes it easier for designing the driving and controlling circuitry). Moreover, with the DCR reduction technology proposed, the DCR in the SPAD can be reduced by nearly 90 % which makes it comparable to those SPADs fabricated using high-voltage processes and also the commercial SPADs. In addition, this design enables the breakdown voltage and the temperature monitoring capability that makes it possible for adding the intelligent control for the optimization of the photon counting system's overall performance.

More important, this technology proposed does not have conflicts with the existing technology and can be applied to any other types of SPAD or SPAD arrays system to further improve their DCR performance and monitoring the key parameters of the system.

VI. Conclusion

In conclusion, an optimised photon counting system using covered SPAD is designed in this work. The SPAD is based on a standard 0.18 μm process and formed using the medium voltage doping layers. Results show that the SPAD is able to detect the visible light from 450 nm to 850 nm with a 35 % peak photon detection probability achieved at around 550 nm with bias voltage of 16 V. A narrow timing jitter of 176 ps is measured at an excess voltage of 3 V. The dark count rate in the SPAD tested is about 14.62 cps/μm² with excess bias voltage of 3 V. To real-time monitor the important parameters in the SPAD, a shaded SPAD with the same structure is fabricated on the same chip which is covered by a metal layer and only measures the DCR for the correction. Results show that nearly 90 % DCR reduction can be achieved which makes it very useful for the DCR corrections in SPAD arrays. By monitoring the DCR of the shaded SPAD, the breakdown voltage and on-chip temperature of the SPADs on the same chip can be obtained and the results show that the temperature measurement range can be from -10 ℃ to 50 ℃. The potential usefulness of the afterpulsing probability monitored using the shaded SPAD and the crosstalk probability between SPADs on the chip are analyzed. In addition, the effects of process variations on the SPAD performance is investigated by testing 10 chips with the same SPADs fabricated and potential method is proposed for alleviate the process variations in the SPAD arrays.

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