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128 x 128 Silicon Photonic MEMS Switch Package using Glass Interposer and Pitch Reducing Fibre Array

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Abstract

We design and fabricate the packaging of 128 x 128 silicon photonic MEMS switch device using through glass via (TGV) interposer and pitch reducing fibre array. The switch device contains 16384 MEMS switch cells and 272 grating couplers spaced at 63.5 µm in a compact footprint of 17.4 mm x 16 mm. The apodised grating couplers designed for 1300 nm have an insertion loss of 2.5 dB/facet at 10˚ coupling angle. The 0.5 mm thick glass interposer contains 512 electrical vias while the pitch reducing optical coupling array is polished to 40° for planar coupling.

Introduction

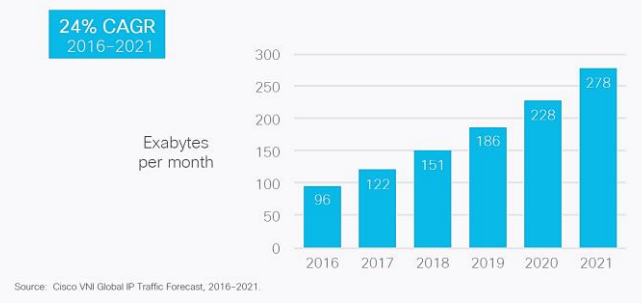


Fig. 1. Cisco VNI forecasts 278 exabyte per month of IP traffic by 2021 [1].

The growth in data traffic (Fig. 1), which is projected to increase at a compound annual growth rate (CAGR) of 24 % over the next 5 years [1] has warranted higher capacity and energy efficient optical network switching system, with silicon photonic platform as an attractive candidate. Existing data centre networks typically use a multi-stage folded Clos topology and electronic packet routers between servers, increasing cost, cabling and thermal management complexity [2]. Silicon photonic on the other hand allows the integration of highly dense optical and electronic structures and mass production through the use of existing complementary metal-oxide semiconductor (CMOS) architectures, making all optical switching possible on a single chip. Various switching architectures based on silicon photonic have been proposed such as electro-optic [3], thermo-optic [4] and MEMS [5] switching mechanisms. In this paper, the authors discuss in detail the packaging components of the 128 x 128 MEMS-actuated silicon photonic switching device that can address the future data traffic requirement.

Silicon photonic MEMS switch architecture and packaging

The operating principle of the MEMS switch mirrors classical parallel plate electrostatic actuators. A switching element (N) consists of a movable 90 ° bend coupler waveguide that is suspended above the intersections of horizontal and vertical bus waveguides when the cell is under OFF state. When a potential difference is applied (ON state), the movable coupler waveguide is brought into close vicinity of the bus waveguide, allowing a 90 ° turn in the optical signal's propagation path. This switching architecture is thus scalable to N x N ports as the optical switching loss is independent of the number of switching elements. The operating principle is illustrated in Fig. 2 and more details about the architecture can be found in [6].

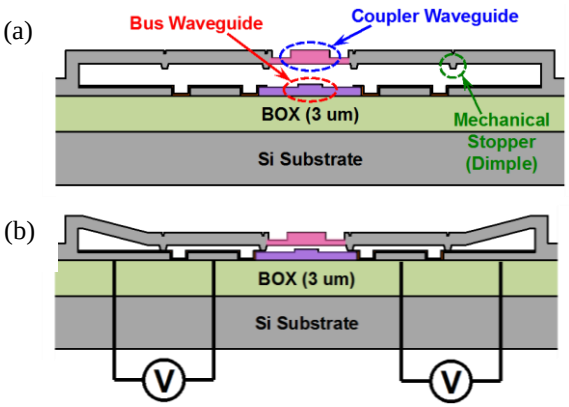


Fig. 2. Illustration of MEMS architecture and actuation under the influence of potential difference – (a) OFF and (b) ON.

The challenge in packaging and integrating a switch device consisting of N x N switching elements at sub-system level however is the large number of electrical interconnects that has to be addressed. For an N x N switch device, N^2 electrical interconnects is needed. The authors have previously demonstrated the packaging of 12 x 12 switch array that has N^2 electrical interconnects through the use of single metal layer aluminum nitride interposer with 25 µm line width and space (L/S) [7]. Increasing the number of packaged ports will require either a reduction in L/S, increasing the number of transmission lines layers or a combination of the two.

By exploiting the hysteresis of the electrostatic actuators however, the N^2 electrical interconnects can be reduced to 2N through row / column addressing scheme [8]. Fig. 3 illustrates the difference between individual (N^2) and row / column (2N) addressing schemes. Assuming the current device is fabricated using individual addressing scheme, the number of electrical interconnects that has to be connected will be 16384. On the other hand, with row / column addressing scheme, a minimum of only 256 electrical interconnects is required. With this approach, the authors are able to expand the number of packaged ports from 12 x 12 previously to 128 x 128 ports while keeping the design of electrical interconnects on interposer and test board manageable. While row / column addressing would require only 256 electrical pads for 128 x 128 switching elements, the current version of MEMS switch has a

total of 512 electrical bond pads to allow for symmetrical bonding configuration. The fabricated switch device is shown in Fig. 4.

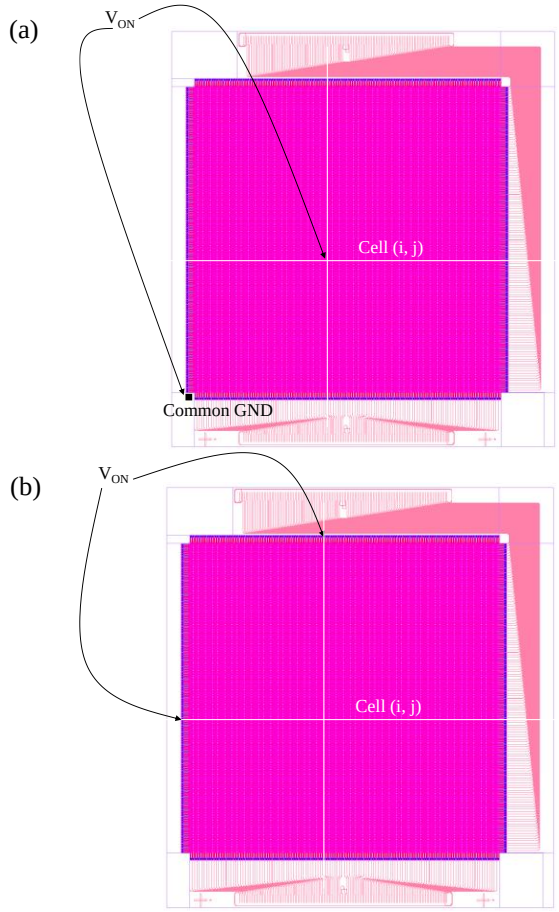


Fig. 3. Difference between (a) individual and (b) row / column addressing schemes. The latter approach reduces the number of electrical interconnects from N^2 to 2N.

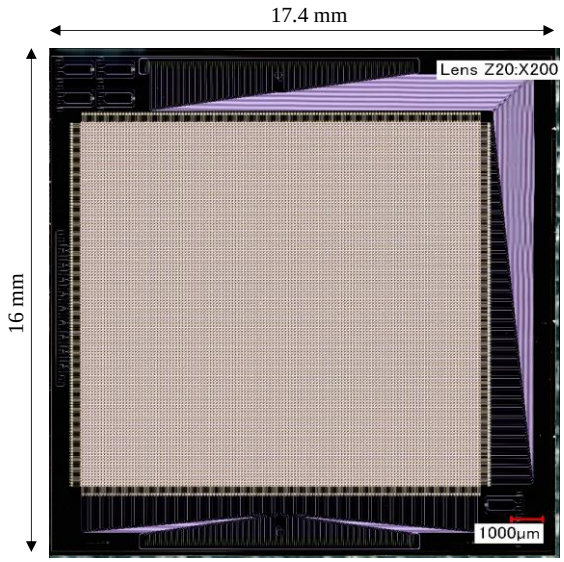


Fig. 4. The 128 x 128 MEMS switch device to be packaged. 272 optical couplers (input and drop ports) are evenly distributed on the north and south of the image.

In this paper, the authors propose the packaging of a high density MEMS-based silicon photonic switch through full flip-chip assembly. Through glass via (TGV) interposers and pitch-reducing optical coupling array are used as the electrical and optical interfaces between switch device and sub-system respectively. An overview of the proposed packaging is shown in Fig. 5.

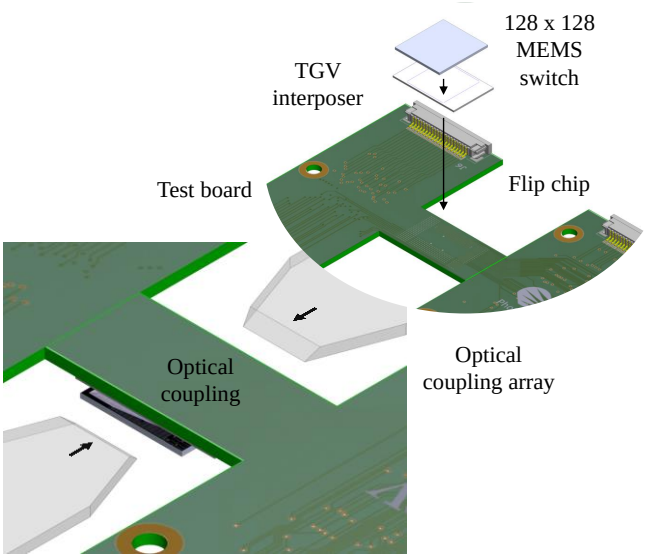


Fig. 5. Overview of the MEMS switch packaging and flip-chip assembly approach.

Solder bumps are first formed on the device and test board bond pads. The glass interposer and MEMS device are then flip-chip onto the test board and interposer sequentially and reflowed. As the fabricated MEMS device is not capped, solder flux and underfill will not be used between the device and interposer to prevent flux residue contamination or resin filling the gap between coupler and bus waveguides. The board assembly is then flipped and assembled on a mechanical sub-mount for optical coupling from both sides, one at a time as alignment can be done using the optical shunts. The waveguide arrays are finally secured using UV resin and transferred to a casing, ready for testing.

Electrical packaging design and materials

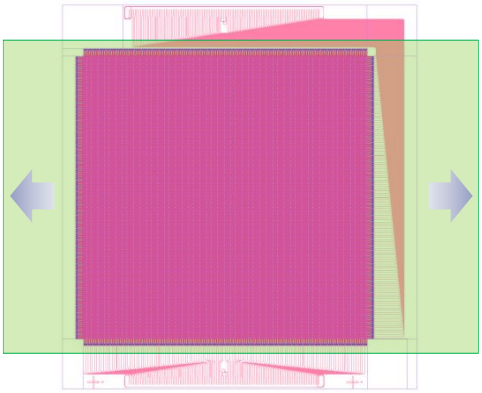


Fig. 6. Only two sides of the device are available for electrical transmission lines routing due to optical coupling requirements.

Unlike typical electronic packaging, in which 4 sides of an interposer or test board can be used for electrical transmission lines fan-out, additional optical coupling requirement on silicon photonic reduces this freedom to three or fewer sides. For the current MEMS switch device, there are only two available sides for transmission lines routing on the interposer (Fig. 6). Due to

this limitation, the interposer is designed based on two layer redistribution lines (2L-RDL) with 25 µm line width and space (Fig. 7). While a smaller line width and space, for example 15 µm would allow all 512 transmission lines to be routed within a single layer, the authors decided to proceed with 2L-RDL as part of an ongoing effort to demonstrate the process capability as well as for future applications.

The interposer has rows of ϕ 50 µm bond pads mirroring the device on one surface, with ϕ 200 µm bond pads matching the test board on the other. Layer 1 and 2 are on the same surface interfacing the switch while layer 3 interfaces with the test board. These two surfaces are connected via ϕ 40 µm copper-filled vertical vias through the 500 µm thick glass. The glass interposer has been fabricated through the following sequence on an 8" glass wafer - via drilling, via filling, chemical-mechanical polishing, redistribution lines (RDL) patterning, electroplating and dicing.

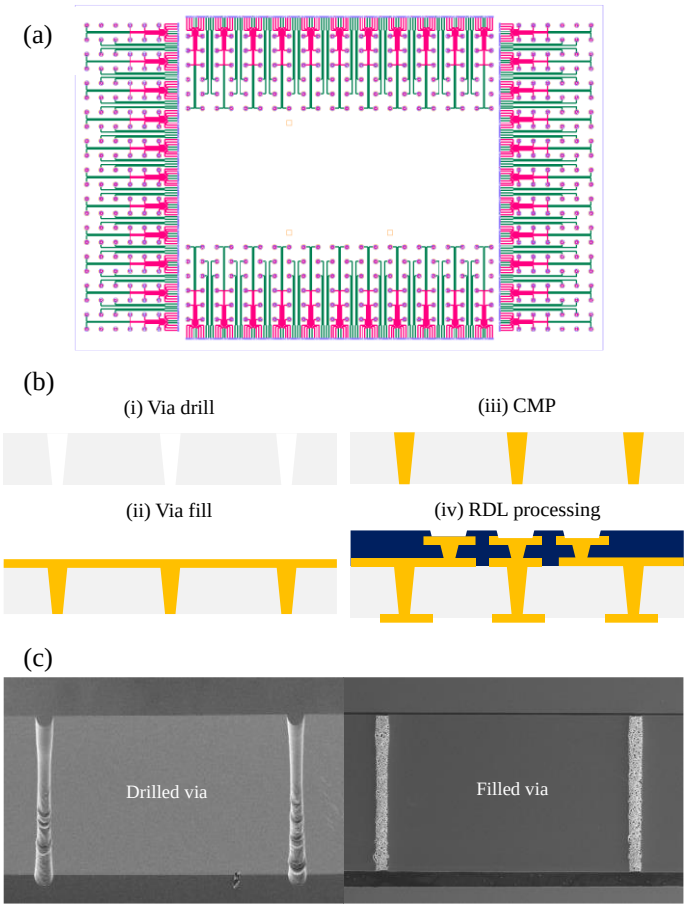


Fig. 7. (a) Design of the TGV interposer, in which the red denotes layer 1 and green layer 2 RDLs, (b) TGV interposer fabrication flow and (c) SEM images of drilled and filled TGVs.

The second component that has to be designed in order to address 512 electrical interconnects is the test board. Similar to the interposer, only two directions of the test board can be used to route the transmission lines as the remaining two has to be kept clear for optical coupling. A five-layer test board is used to route the minimum amount of 256 electrical interconnects to actuate the MEMS switch. Fig. 8 shows the dense transmission lines within the test board and the fabricated board.

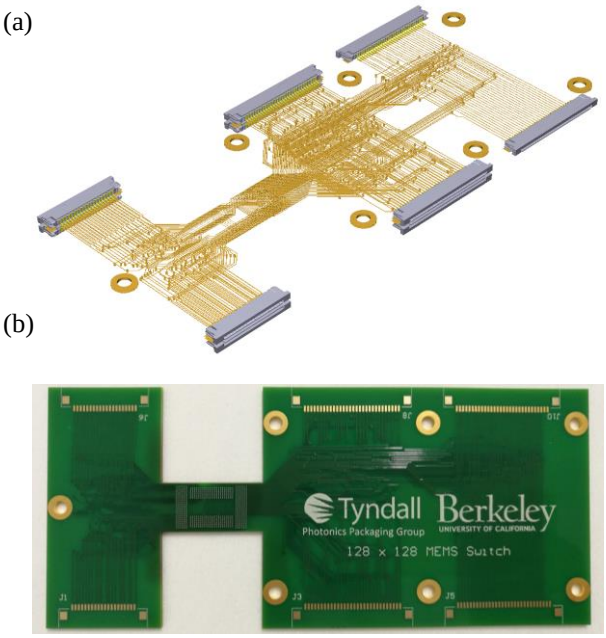


Fig. 8. (a) The 3D model illustrating the electrical transmission lines within and (b) the test board fabricated.

Optical packaging design and materials

Aside from 2N electrical interconnects, there are also 2N optical interconnects that has to be addressed. On the switch device, a total of 276 grating couplers are evenly distributed in linear fashion on two opposite sides of the device (Fig. 4). The couplers have a pitch of 63.5 µm in order to reduce the length of waveguides and thus overall size of the device. The fibre insertion loss of these apodised grating couplers are 2.5 dB/facet at 10° angle of incident and 1310 nm wavelength.

Instead of conventional fibre array unit, the authors have opted to use ion-exchanged waveguide array in order to address the smaller than conventional optical coupler pitch of 63.5 µm on the device. From packaging integrity point of view, a planar coupling approach is better than vertical coupling at 10 ° due to the size of the coupling array and the number of fibre pigtails that has to be managed but this often comes at the expense of additional transmission loss of approximately 0.8 dB per facet.

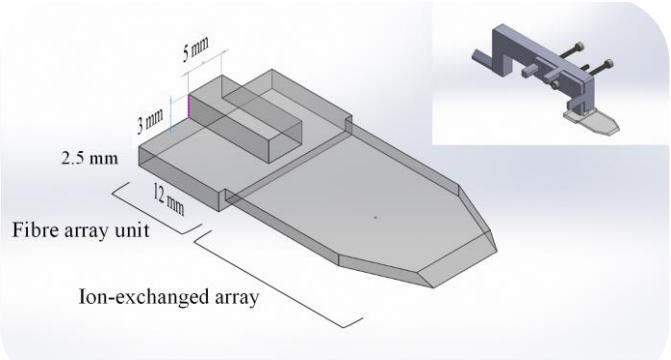


Fig. 9. Design of the ion-exchanged waveguide array and fibre array units. The device coupling facet is polished to 40 ° and deposited with aluminum.

The specifications of the ion-exchanged waveguide array are shown in Fig. 9. The pitch of the ion-exchanged waveguides

increases gradually from 63.5 µm to 127 µm from one end to another. The smaller waveguide pitch facet is polished to 40 ° and coated with aluminum while the larger waveguide pitch facet is polished to 8 ° for regular fibre array butt coupling. The reason for using additional aluminum coating on the 40 ° facet instead of relying on just total internal reflection is due buried depth of the waveguides. Unlike typical fibre array meant for planar coupling in which the fibre cores are approximately 65 µm from the coupling surface, the waveguides here are buried only 10 µm away. Any unintentional optical epoxy climb at the 40 ° polished facet would render the unit useless.

The butt coupling of the fibre array unit onto the ion-exchanged waveguide array unit also proves to be challenging due to its large size. With 136-channels and 127 µm pitch, both units have a width of approximately 20 mm, exacerbating rotational axes alignment. The authors also observed uneven insertion losses across the channels due to the bowing of fibre array unit (Fig. 10). After multiple fabrication improvements, the final array developed (Fig. 11) showed consistent insertion losses between 0.6 to 1.2 dB across all 136-channels.

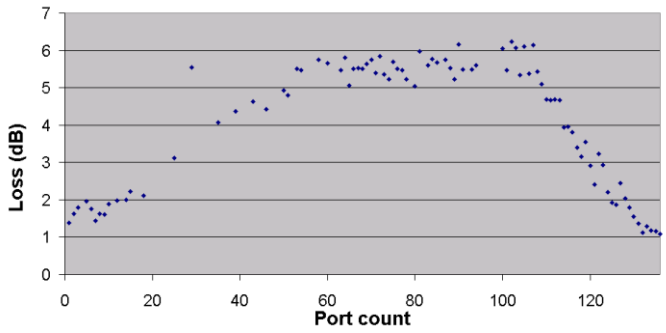


Fig. 10. Large variation of insertion losses between fibre array unit and ion-exchanged waveguide array due to bowing of fibre array unit.

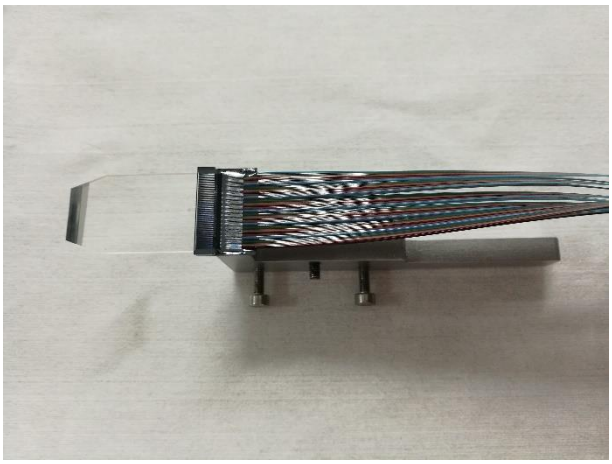


Fig. 11. The final 136-channels ion-exchanged waveguide array unit. Channel to channel insertion losses varied between 0.6 to 1.2 dB.

Conclusions

We have proposed, designed and fabricated all the necessary components to demonstrate the largest digital silicon photonic MEMS switch at the moment (to our best knowledge). Testing and characterization of the package are ongoing at the point of writing and results will be available in future publications.

Acknowledgments

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