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Control Circuits for Avalanche Photodiodes

A thesis presented to the
National University of Ireland, Cork
in Fulfillment for the Requirements for
the Degree of
Doctor of Philosophy

by

Shijie Deng

Supervisor: Dr. Alan P. Morrison

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December 2013

Abstract

Avalanche Photodiodes (APDs) have been used in a wide range of low light sensing applications such as DNA sequencing, quantum key distribution, LIDAR and medical imaging. To operate the APDs, control circuits are required to achieve the desired performance characteristics. This thesis describes the development of three control circuits including a bias circuit, an active quench and reset circuit and a gain control circuit all of which are used for control and performance enhancement of the APDs.

The bias circuit is used to bias planar APDs for operation in both linear and Geiger modes. The circuit was designed and simulated using AMS 0.35 μm and L-Foundry 0.15 μm CMOS process. The circuit is based on a dual-rail charge pump configuration and operates from a 5 V supply. Simulations shows that it is capable of providing milliamp load currents for shallow-junction planar APDs that operate up to 40 V. Novel voltage regulators allow the bias voltage provided by the circuit to be accurately controlled and easily adjusted by the end user. The circuit is highly integrable requiring only 2 external capacitors thereby enabling a single package APD solution that operates from a single system supply (e.g. 3.3 V, 5 V). This is a very attractive solution for applications requiring a compact integrated APD device.

The active quench and reset circuit is designed for APDs that operate in Geiger-mode and are required for photon counting. The circuit was designed and simulated using L-Foundry 0.15 μm and AMS 0.35 μm CMOS process. The chip was fabricated with AMS 0.35 μm CMOS process. The circuit enables

linear changes in the hold-off time of the Geiger-mode APD (GM-APD) from several nanoseconds to microseconds with a stable step size of 6.5 ns. This facilitates setting the optimal 'afterpulse-free' hold-off time for any GM-APD via user-controlled digital inputs. In addition this circuit doesn't require an additional monostable or pulse generator to reset the detector, thus simplifying the circuit. Compared to existing solutions, this circuit provides more accurate and simpler control of the hold-off time while maintaining a comparable maximum count-rate of 35.2 Mcounts/s.

The third circuit designed is a gain control circuit. This circuit is based on the idea of using two matched APDs to set and stabilize the gain. The circuit was designed and simulated using L-Foundry 0.15 μm high voltage CMOS process and implemented with discrete components (PCB). Experimental results show that the circuit can provide high bias voltage (up to 40 V) for operating the planar APD, precisely set the APDs gain (with errors of less than 3%) and compensate for changes in the temperature to maintain a more stable gain. The circuit operates without the need for external temperature sensing and control electronics, thus lowering the system cost and complexity. It also provides a simpler and more compact solution compared to previous designs.

This thesis presents the circuit design, simulations and development of the three circuits. These circuits were developed independently of each other and are used for improving different performance characteristics of the APD. Further research on the combination of the three circuits will produce a more compact APD-based solution for a wide range of applications.

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• Shijie Deng and Alan P. Morrison, "A dual-rail charge pump bias circuit for avalanche photodiodes", The 22nd Irish Signals and Systems Conference (ISSC 2011), pp. 56-58, Dublin, Ireland, Jun. 2011.

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• Shijie Deng and Alan P. Morrison, "High-resolution hold-off time control circuit for Geiger-mode avalanche photodiodes", The 19th International Conference Mixed Design of Integrated Circuits and Systems (MIXDES2012), pp. 269-272, Warsaw, Poland, May. 2012.

• Shijie Deng and Alan P. Morrison, "Design of an adjustable bias circuit using a single-sided CMOS supply for avalanche photodiodes", The 10th IEEE International NEWCAS Conference (NEWCAS2012), pp. 65-68, Montreal, Canada, Jun. 2012.

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Chapter 1

Introduction

1.1 Introduction

Advances in avalanche photodiode (APD) technology including higher sensitivity, faster response time, lower operation voltage and lower costs have allowed APDs to replace PIN photodiodes or photomultiplier tubes (PMTs) in many low-light sensing applications.

In fibre communication systems, APDs have been the frequently choices as they can provide higher sensitivity in optical receivers than PIN photodiodes. Thanks to the high internal gain and fast response time, APD can achieve 5∼10 dB better sensitivity than PINs and provide higher signal to noise ratio (SNR) that make it more suitable for long haul communications as a high speed receiver in high bandwidth applications [1-3]. In single-photon counting and time-correlated single-photon counting (TCSPC) applications, APDs have been alternatives to photomultiplier tubes (PMTs). APDs can provide higher detection efficiency meanwhile give an excellent photon timing performance. More importantly, the APDs fabricated in planar technology compatible with CMOS circuits have enabled smaller size, lower operating voltage and lower power dissipation than the use of PMTs [4-6]. APDs are also well suited in some other applications including astronomy [7], fluorescence correlation spectroscopy [8], DNA sequencing [9, 10], quantum cryptography [11], LIDAR

[12-14], laser range finders [15, 16], metrology [17], confocal microscopy [18], particle detection [19] and nuclear medicine [20, 21].

Avalanche photodiodes operate in different modes under different bias voltages. The APD operates in linear mode with the bias voltage below its breakdown voltage. In this mode, APDs have their performance characterized by gain, noise, and bandwidth. The APD operates in Geiger-mode or single photon mode with the bias voltage above its breakdown voltage and in this mode have their performance characterized by dark count, hold-off time, afterpulsing, response time, jitter and responsivity. Performance characteristics such as quantum efficiency and spectral response are common to both modes of operation. To operate an APD in low light sensing applications, control circuits are required to bias it and also to optimize the APD to achieve the desired performance characteristics.

A number of control circuits have been designed by research groups to operate the APDs and improve their performance. S. Cova *et al* have developed a number of quenching circuits for optimising the performance of GM-APDs. Those works were described in [22-24]. J. Kataoka *et al.* have developed a radiation detector consisting of APDs, an active gain control system and readout circuitry that has been used in a satellite to monitor the distribution of low energy particles [25, 26]. D. Cronin and D. P. O'Connell have also developed some control circuits for the APDs developed by the Photodetection and Imaging Group at University College Cork [27]. These circuits allow the user control of the APD characteristics such as gain and hold-off time [28, 29]. In some commercial organizations, APD control circuits have also been developed. At Hamamatsu, circuits consisting of photodiodes and custom signal processing circuits have been developed which can be used for X-ray detection [30]. PerkinElmer have developed APD/preamplifier hybrid modules which

are used for confocal microscopy, range finding and LIDAR applications [31]. Some other organizations such as PicoQuant [32], ID Quantique [33] and Sensl [34] have also developed a number of systems that consist of APDs and control electronics for low light detection.

In this work, the design and development of three APD control circuits is described. These circuits were developed independently of each other. However the combination of the three circuits results in a system that is capable of providing a more compact APD-based solution for a wide range of applications.

The first circuit designed is a bias circuit for an APD that can operate in both linear mode and Geiger-mode. The circuit was designed using AMS 0.35 μm and L-Foundry 0.15 μm CMOS process and post-layout simulations are presented. Simulation results show that the circuit is capable of sourcing milliamp range load currents for shallow-junction planar APDs that operate up to 40 V. The layout of the circuit designed with the L-Foundry 0.15 μm process shows a small footprint of 1.55 mm $\times$ 1 mm, making it suitable for hybrid integration with two external capacitors and an APD in a single package to operate seamlessly from a 5 V supply. This removes the requirement for a separate APD bias supply, employing the same supply for both signal conditioning and bias. Moreover, the circuit is capable of full integration for APD-based devices. Compared with the existing solutions including external high-voltage supplies, DC-DC converter chips and other reported designs (requiring several external components to function correctly), this design provides a more compact solution that can be used to reduce size, weight and power consumption for APD-based applications.

The second circuit designed is an active quench and reset circuit (AQRC) for the APD that operates in Geiger-mode. This circuit is designed with the aim of

overcoming the difficulties of hold-off time adjustment that remain in existing quench circuits. The circuit is simulated and layout designed in the Cadence design environment with L-Foundry 0.15 μm and AMS 0.35 μm CMOS process. The integrated circuit was fabricated using AMS 0.35 μm CMOS process and tested with a GM-APD. Results show that this design is capable of linear changes to the hold-off time from several nanoseconds to microseconds with a reasonable step of 6.5 ns that allows setting of the optimal 'afterpulse-free' hold-off time for any GM-APD through digital inputs or additional signal processing circuitry. A minimum dead time of 28.4 ns was observed from the measurement, demonstrating a saturated photon-counting of 35.2 Mcounts/s with this AQRC.

The third circuit designed is a gain control circuit for APDs that operate in linear-mode. This circuit uses a matched APDs arrangement which has the advantages of controlling and stabilizing the gain without the need for external temperature sensing and control electronics thereby lowering the system cost and complexity. Meanwhile this design provides a simpler and more compact solution. The circuit was simulated in the Cadence environment with L-Foundry 0.15 μm high voltage CMOS process, fabricated with discrete components (PCB) and measured with packaged APDs. Results show that the circuit can provide in excess of 40 V bias voltage for the planar APD and allow for the setting and stabilization of its gain independent of variation in the ambient temperature or power supply fluctuation.

1.2 Thesis Outline

This thesis is divided into a number of chapters. Chapter 2 introduces the theory of photodetection and the operation of avalanche photodiodes biased in linear mode and Geiger-mode. Chapter 3 describes a bias solution that is

used for APDs operating in both linear and Geiger modes. Chapter 4 presents the design and development of a new active quench and reset circuit (AQRC) for Geiger-mode avalanche photodiodes (GM-APDs). Chapter 5 describes a novel gain control and stabilization circuit for avalanche photodiodes (APDs) biased in linear mode. In Chapter 6, the conclusions of this thesis are made and future work is proposed.

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Chapter 2

Introduction to avalanche photodiodes (APDs)

This chapter briefly introduces the theory of photodetection and the operation of avalanche photodiodes (APDs). The APD's physical processes and key performance characteristics are explained. The backgrounds of some external control circuits required for the APDs' operation are described. The design of the planar APD used throughout this project is illustrated.

2.1 Photodetection

Based on photon absorption in semiconductor materials, a photodetector absorbs light via three processes including intrinsic band-to-band absorption, free carrier absorption and band-to-impurity absorption, see Figure 2.1. Intrinsic band-to-band absorption occurs when the photon energy ($h\nu$) is greater than the material bandgap energy E_g. In this case, a photon is able to excite an electron from the valence band up into the conduction band to create an electron-hole pair. The hole and electron each constitute a charge carrier. The electric field applied to the semiconductor will cause the hole and electron to be transported into the external circuit through the material. When the electron-hole pair makes its way to the external circuit their combined effect will lead to a flow of charge q in the circuit where q is the charge of a single

electron [1], [2].

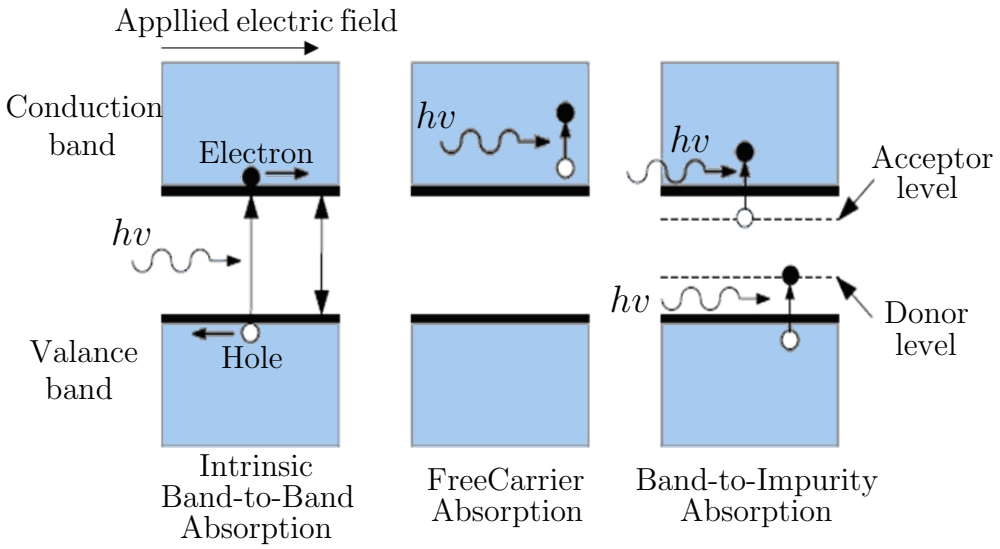


Figure 2.1: Photon absorption mechanisms.

Intrinsic band-to-band absorption is the dominant absorption mechanism in most semiconductors used for photodetection. To create an electron-hole pair, it requires that the photon energy, E = $h\nu$, is greater than the material bandgap energy, E_g: this can be expressed as

$$h\nu > E_g \; or \; h\frac{c}{\lambda} > E_g \tag{2.1}$$

This yields a maximum allowable wavelength

$$\lambda_{max} = \frac{hc}{E_g} \; or \; \lambda_{max}\,(nm) = \frac{1240}{E_g\,(eV)} \tag{2.2}$$

Where E_g (eV) = bandgap energy in electron-volts.

Table 2.1 lists the bandgap, the corresponding maximum usable wavelength, and typical operating wavelengths for common semiconductor materials.

Free carrier absorption occurs when the photon energy is absorbed by free carriers in either the conduction band or the valence band which corresponds to the "heating" of the semiconductor material. It is a secondary effect at the near infrared wavelengths used for optical communications. Band-to-impurity

Material	Bandgap	Maximum wavelength (nm)	Typical operating range (nm)
Si	1.12	1110	500 - 900
Ge	0.67	1850	900 - 1300
GaAs	1.43	870	750 - 850
$In_xGa_{1-x}As_yP_{1-y}$	0.38 - 2.25	550 - 3260	1000 - 1600

Table 2.1: Characteristics of various semiconductors [1].

absorption is another secondary effect at near-IR wavelengths. It is used to construct photodetectors responsive at mid-IR wavelengths as long as 30 μm [1].

An important parameter for a photodiode is the quantum efficiency (QE). The quantum efficiency is defined as the probability that a single photon incident on the detector generates an electron-hole pair and is given by [1]:

$$\eta = \frac{number\,of\,e\,-\,h\,pairs\,produced}{number\,of\,incident\,photons} \tag{2.3}$$

where $0 \leq \eta \leq 1$. A signal with photon energy sufficient to generate photocarriers will continuously lose energy to the semiconductor crystal lattice as the optical field propagates through the semiconductor. As can be seen from Figure 2.2, there is a reflection loss at the interface of the air and the semiconductor due to differences in the index of refraction. The Fresnel reflectivity for an optical signal at normal incidence to an interface between two materials is given by

$$R = \frac{(n_1 - n_2)^2}{(n_1 + n_2)^2} \tag{2.4}$$

where n_1 = index of refraction of first material and n_2 = index of refraction of second material. For many semiconductors used in the 800 nm to 1500 nm region, n is between 3.2 and 3.6 and the reflectivity can be as high as 32 %. Reflection losses can be reduced with antireflection coatings to less than 1 %.

Inside the semiconductor, the field decays away exponentially as energy is transferred to the semiconductor. The material can be characterised by an

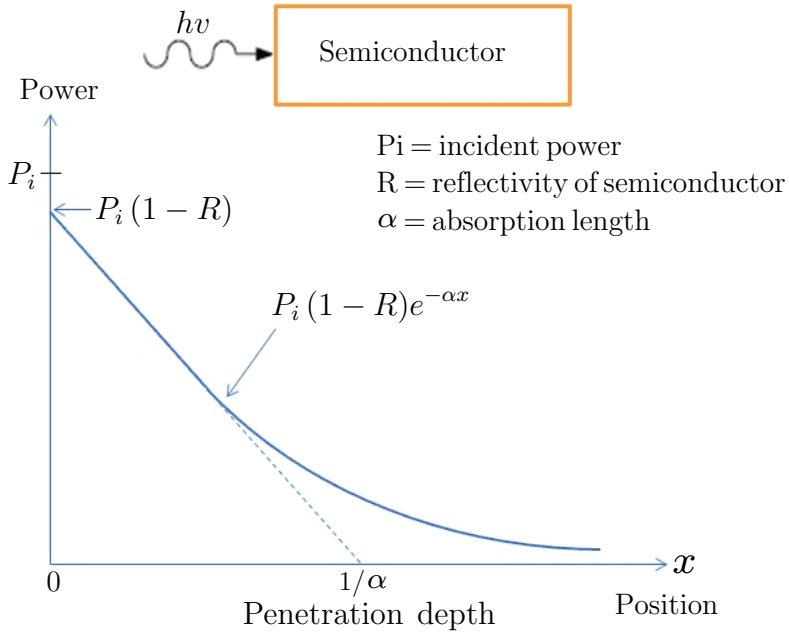


Figure 2.2: Optical absorption in a semiconductor [1].

absorption constant α and a penetration depth $1/\alpha$. Penetration depth is the point at which $1/e$ of the optical signal power remains. The power in the optical field decays with distance. The amount of power absorbed in the semiconductor is as a function of position within the material and can be expressed as

$$P_{abs} = P_i\,(1-R)\left(1-e^{-\alpha x}\right) \tag{2.5}$$

The number of photons absorbed per second is the power in watts divided by the photon energy (E = $h\nu$). If each absorbed photon generates a pair of photocarriers (i.e. an electron-hole pair), the number of photocarriers generated per photon for a specific semiconductor with reflectivity R and absorption constant α is given by

$$\eta\,(x) = (1-R)\left(1-e^{-\alpha x}\right) \tag{2.6}$$

Where $\eta(x)$ is the quantum efficiency of the photodetector.

Responsivity is defined as the ratio of the photocurrent to the optical power and is given by [2]

$$R = \frac{I_{photo}}{P_{opt}} = \frac{\eta q}{hv}\,(A/W) \tag{2.7}$$

Where I_{photo} = photogenerated current, P_{opt} = incident optical power, η = quantum efficiency, q = electronic charge, h = Planck's constant, v = optical frequency. For an ideal photodiode each incident photon would generate the charge of one electron flowing in the external circuit. In reality, there are several physical effects that tend to reduce the responsivity, including incomplete absorption, recombination, reflection from the semiconductor surface and contact shadowing.

The responsivity of a semiconductor will also vary with wavelength [1]. Responsivity increases as the wavelength increases because there are more photons per watt at long wavelengths than there are at short wavelengths. This is a direct result of the photon energy decreasing with wavelength. Since the amount of photocurrent is determined by the number of photons instead of the energy of the photons, longer wavelengths generate more photocurrent per watt than the short wavelengths.

2.2 Avalanche photodiodes

An avalanche photodiode (APD) is a very sensitive photodetector. The advances in APDs such as low operating voltages, low-cost, higher sensitivity and small-size make it very attractive for use in photodetection [1]. It has been used in a wide range of lowlight sensing applications including astronomy [3], DNA sequencing [4], light detection and ranging (LIDAR) [5] and medical sensing [6].

2.2.1 Avalanche effect in APDs

In Figure 2.3, the structure of a typical avalanche photodiode is illustrated [1]. The APD consists of four sections of semiconductor with different doping profiles as shown in Figure 2.3(b). The leftmost section is a p-type semiconductor doped to a density of N_{accept}, while the rightmost section is an n-type semiconductor doped to a density N_{donor}. The middle region is an intrinsic region in combination with a second p-type region. The energy diagram of the APD is shown in Figure 2.3(c) while the electric field profile of the space charge region is shown in Figure 2.3(d). When a p-n junction is subjected to a high reverse bias there are two breakdown mechanisms that can occur. The first mechanism involves the atoms being directly ionized by the applied field which is known as zener breakdown and is commonly used to make voltage regulating diodes. The second mechanism is called avalanche breakdown which is caused by high velocity carriers causing impact ionisations within the semiconductor that generates additional carriers.

In the absorption region shown in Figure 2.3(d), photons are absorbed in the lightly doped semiconductor material, generating electron-hole pairs. The carriers rapidly travel through the lower field drift region at their saturation velocity (1×10^7 cm/s for electric field $> 10^4$ V/cm [7]) to the edges of the region. Carriers that reach the gain region are further accelerated by an even higher electric field. Avalanche breakdown then begins to occur with very high velocity carriers causing impact ionisations within the semiconductor that will further generate additional carriers. These additional carriers can then undergo additional impact ionisations causing an avalanche effect.

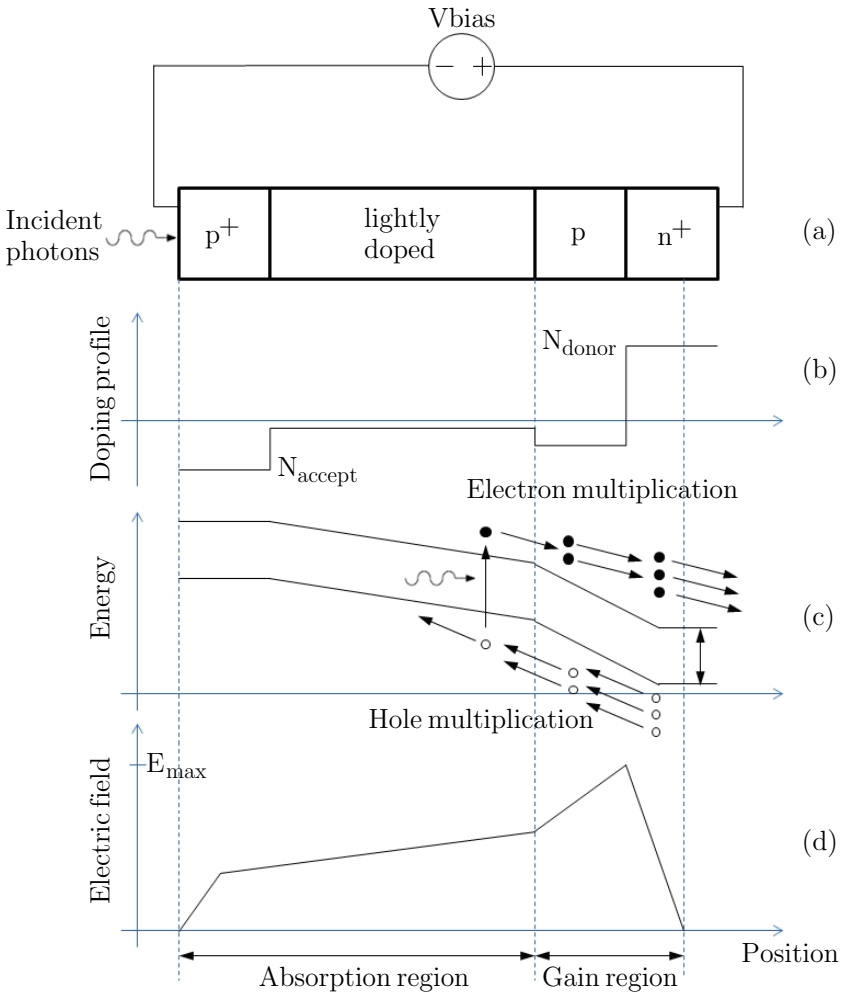


Figure 2.3: Example of an avalanche photodiode. (a) Diode structure. (b) Doping profile. (c) Energy band diagram. (d) Electric field profile. [1]

2.2.2 Impact ionisation

The impact ionisation or multiplication process in the gain region is demonstrated in Figure 2.4. The avalanche current flowing in the APD is caused by this mechanism. The impact ionisation can be characterised by the ionisation coefficients, α_e and α_h, for electrons and holes respectively. α_e and α_h can also be defined as the number of secondary electron-hole pairs generated in a unit distance with the applied electric field. For a given temperature, the ionization coefficients are exponentially dependent on the electric field and can

be defined as

$$\alpha_{e,h} = a.exp\left(-\left[\frac{b}{E}\right]^{c}\right)\left(cm^{-1}\right) \tag{2.8}$$

where a, b and c are experimentally determined constants, E = magnitude of the electric field.

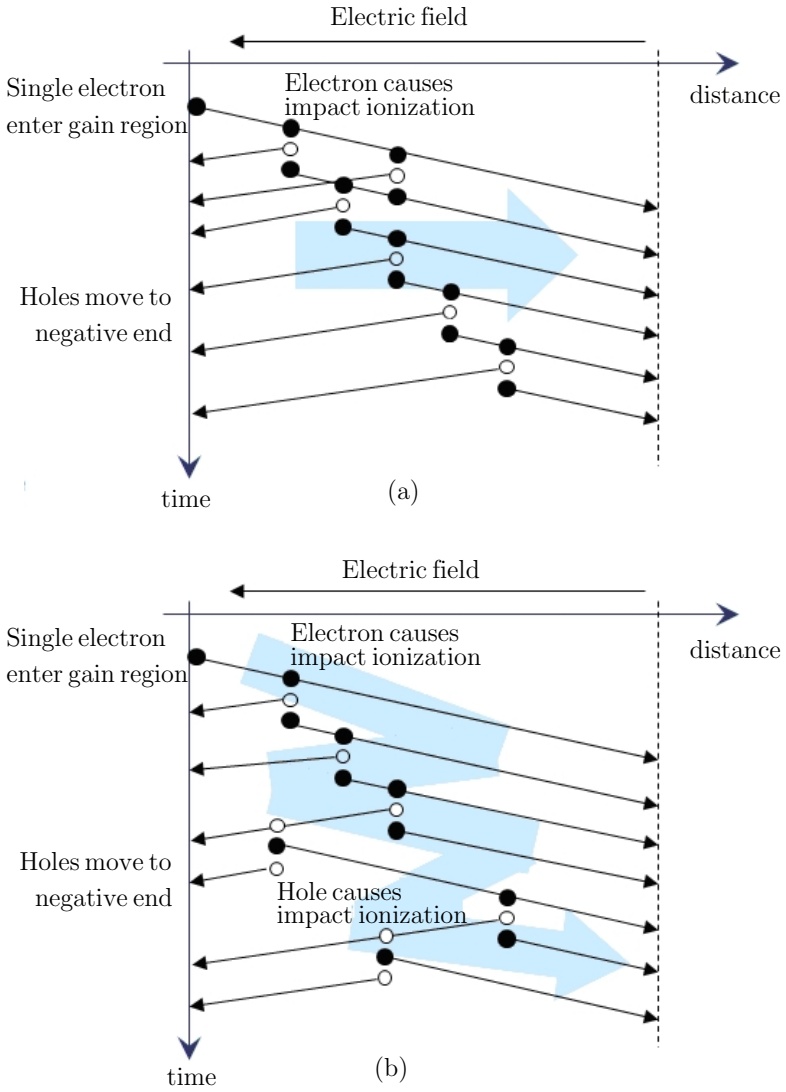


Figure 2.4: (a) Impact ionisation process with electrons only contributing (b) Impact ionisation process with both holes and electrons contributing; note the avalanche direction indicated by the blue arrow [1].

If the temperature of the detector is increased, there will be an increase in both

the number of non-ionising collisions with thermally excited atoms and the phonon energy as shown in Eqn. 2.9. The additional phonon collisions reduce the carrier velocity and decreases their probability of gaining sufficient energy to initiate impact ionisations and the generation of the number of secondary electron-hole pairs will be decreased [8-13].

$$\alpha_{e,h} = \frac{q\varepsilon}{E_i} exp\left(-\frac{3E_{phonon}E_i}{(q\varepsilon\lambda)^2}\right) \tag{2.9}$$

where q = electronic charge, E = electric field, E_{phonon} = phonon energy, E_i = ionisation threshold energy (minimum energy for impact ionisation to occur), λ = mean free path for phonon scattering.

To determine the ionising carrier in an APD, an ionisation ratio is defined as:

$$k = \frac{\alpha_h}{\alpha_e} \tag{2.10}$$

The APD structure is optimised for the more ionising carrier depending on this ratio k. For materials where $\alpha_e \gg \alpha_h$, (i.e. where electrons are much more ionising than holes such as in silicon) it is required that photons are absorbed in the p-region (see Figure 2.3). Values of k between 0.01 and 0.003 can be achieved to produce high quality Si APDs. Similarly, for materials where holes are more ionising than electrons ($\alpha_h \gg \alpha_e$, e.g. Germanium), photons should be absorbed at the n-region of the junction. Figure 2.4(a) shows the impact ionisation process for silicon ($k \ll 1$), where holes do not contribute. When a photoelectron enters into the gain region, it is accelerated by the applied electric field and then gains enough kinetic energy from the field to generate a series of impact ionisations. In this example, it results in six extra electrons and the avalanche proceeds in a well defined manner from left to right. It is assumed that only holes contribute to the impact ionisations when $k \gg 1$. Figure 2.4(b) demonstrates an undesirable case where $k \cong 1$ and both electrons and holes contribute to the impact ionisations. In this example,

an electron initiates the first ionisation but the subsequent ionisations can be caused by high energy electrons or holes. This avalanche process behaves in an uncontrolled manner, moving back and forth in the gain region depending on which carrier is causing the ionisation. This leads to an undesirable uncertainty associated with this type of process as there is no clearly defined end point until all possible impact ionisations are completed [1, 2]. The net result of this is an undesirable noise contribution due to the stochastic nature of impact ionisation called excess noise.

2.2.3 Multiplication gain

The gain or multiplication factor of an APD is given by [2, 7]

$$M = \frac{I_{photo}}{I_{primary}} \tag{2.11}$$

Where I_{photo} = observable photocurrent at APD terminals, $I_{primary}$ = internal photocurrent before multiplication. The primary current is defined by

$$I_{primary} = \frac{\eta q}{h\upsilon} P_{rcvd} \tag{2.12}$$

Where η = quantum efficiency, P_{rcvd} = received optical signal power. Typically, multiplication gains of a few tens to a few hundreds are applied, even though it is possible for the multiplication factor to be as high as 10^3 or 10^4 [1, 14]. The expressions for electron multiplication (M_e) and hole multiplication (M_h) in a gain region of length l_g are [1, 2, 7]

$$M_e = \frac{1}{1 - \int_{l_0}^{l_g} \alpha_e exp\left(-\int_0^x (\alpha_e - \alpha_h)\, dx\right) dx} \tag{2.13}$$

$$M_h = \frac{exp\left(-\int_0^{l_g} (\alpha_e - \alpha_h)\, dx\right)}{1 - \int_{l_0}^{l_g} \alpha_e exp\left(-\int_0^x (\alpha_e - \alpha_h)\, dx\right) dx} \tag{2.14}$$

As both α_e and α_h in most devices are functions of position within the gain region, exact solutions to Equations 2.13 and 2.14 are difficult to obtain. In certain cases closed form solutions are available. One is for the case where $\alpha_e = \alpha_h$, only electrons are being injected into the gain region, the electric field in the gain region is uniform and the number of ionising collisions per primary carrier is large. In this case, the electron multiplication is given by

$$M_e = \frac{1-k}{exp\left(-\left(1-k\right)\alpha_e l_g\right) - k} \tag{2.15}$$

Where l_g = length of gain region. For the case where k = 0, Equation 2.15 can be reduced to

$$M_e = \frac{1}{1-\alpha_e l_g} \tag{2.16}$$

Instability occurs for $l_g = 1/\alpha_e$ and this condition must be avoided. In a practical device, the maximum achievable DC multiplication is limited by the series resistance and space charge effect (these factors can be combined into a single series resistance R). The multiplication for photogenerated carriers can be described as [2, 15]

$$M_e = \frac{I - I_{MD}}{I_P - I_D} = \frac{1}{\left[1 - \left(\frac{V_R - IR}{V_B}\right)^n\right]} \tag{2.17}$$

Where I = total multiplied current, I_P = total primary (unmultiplied) current, I_D = primary dark current, I_{MD} = multiplied dark current, V_R = reverse bias voltage, V_B = zener breakdown voltage, n = constant depending on the semiconductor material, doping profile and radiation wavelength. For high light intensity, $I_P \gg I_D$ and $IR \ll V_B$, the maximum value of the multiplication is given by

$$\|\| \left(M_{ph}\right)_{max} \cong \frac{I}{I_P} = \frac{1}{\left[1 - \left(\frac{V_R - IR}{V_B}\right)^n\right]} \mid V_R \to V_B \approx \frac{1}{nIR/V_B} \tag{2.18}$$

or

$$(M_{ph})_{max} = \sqrt{V_B/nI_PR} \tag{2.19}$$

When the photocurrent is smaller than the dark current, the maximum multiplication is limited by the dark current and is given by an expression similar to Equation 2.19, with I_P replaced by I_D. It is important that the dark current is made as low as possible so that it does not limit $(M_{ph})_{max}$.

2.3 APD operation modes

With different bias voltages, avalanche photodiodes operate in different modes. APDs that are biased below the breakdown voltage (linear mode) have their performance characterized by gain, excess noise, responsivity and bandwidth while APDs biased above the breakdown voltage (Geiger-mode) have their performance characterized by photon detection probability, dark count rate, hold-off time, afterpulsing effect, and response time jitter. Some performance characteristics such as quantum efficiency and spectral response are common to both modes of operation.

2.3.1 Linear mode

Linear mode applies to APDs biased below the breakdown voltage. In linear mode, the current output varies linearly with the incident optical power and the gain to the incident photo-generated carriers can be from one up to several hundred.

The bandwidth associated with avalanche photodiodes is limited by three main factors including RC time constant, transit time and avalanche multiplication build-up time. The RC time constant is determined by the parallel plate capacitor which shunts current away from the external circuit and the junction

resistance. The junction capacitance is determined by the APD geometry, the fabrication process and applied bias. Since the duration of the photocurrent depends on the lifetime of the longest lived carrier, any fluctuations in the received optical field faster than the carrier lifetime will not be clearly observed. An overall estimate for the APD bandwidth is given by the root-sum-square of the two individual bandwidths [16].

$$B = \frac{1}{\sqrt{\left(\frac{1}{f_{RC}}\right)^2 + \left(\frac{1}{f_t}\right)^2}} \tag{2.20}$$

Where f_{RC} = RC bandwidth, f_t = transit time bandwidth. The time delay due to avalanche multiplication build up can also affect APD bandwidth. The bandwidth of an avalanche photodiode has been shown to be independent of avalanche multiplication when the DC multiplication is less than α_e/α_h [17]. In this circumstance the bandwidth is given by Equation 2.20. Other factors that affect response speed are carrier diffusion current from outside the gain region and the space charge effect. The time delay of carriers generated outside the gain region occurs when the absorption region is not wide enough with respect to the penetration depth of the incident light. The space charge effect is evident when the incident light level is high and the resulting photocurrent is large, with the attractive power of the electron-hole pairs diminishing the electric field effect.

Similar to a passive component, the APD generates signal noise that can be characterised into a number of types. Thermal noise is a temperature dependent white noise source. The thermal noise generated by an APD is given by

$$\bar{v_R^2} = 4kTR_LB \tag{2.21}$$

Where k = Boltzmann's constant, T = the absolute temperature, R_L = the

load resistance, B = the bandwidth. The load resistance is the series resistance connected to the APD as well as the APD resistance itself.
Shot noise is a current dependent white noise source. The total shot noise generated by an APD is given by Equation 2.22:

$$\bar{i^2} = 2qIB \tag{2.22}$$

Where q = electron charge, I = total APD current, B = the bandwidth. The total current is made up of the dark current and the photocurrent. The dark current has a surface leakage component, I_{DS}, that does not flow through the gain region and so does not take part in the multiplication process. On the other hand the internal dark current component, I_{DG}, flow through the gain region and adds to the gain current.

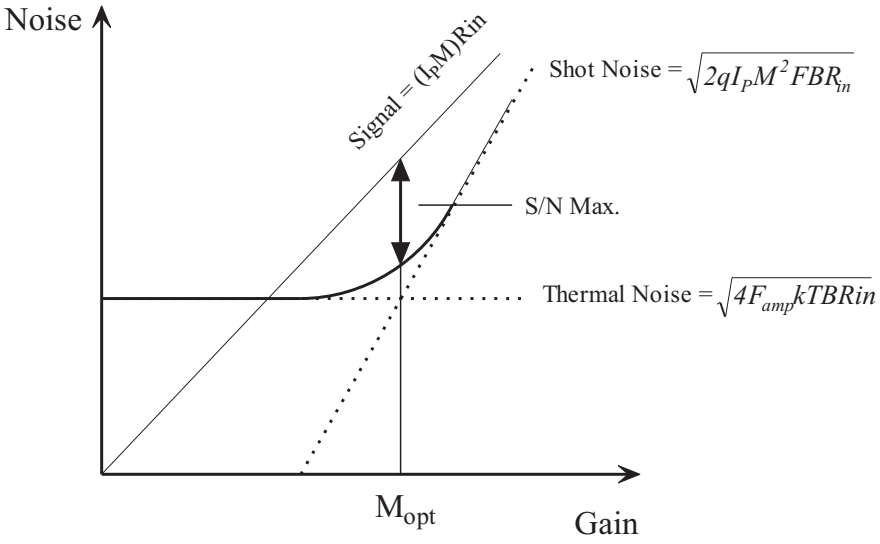
The ionization of individual carriers is not uniform and so the multiplication process contains statistical fluctuations known as excess noise. The excess noise factor, F, can be expressed by the multiplication ratio, M and the ratio of the electron/hole ionization rate, k, and is defined as [16, 18]:

$$F = Mk + \left(2 - \frac{1}{M}\right)(1 - k) \tag{2.23}$$

Equation 2.23 is the noise factor when electrons are injected into the avalanche region. To evaluate the excess noise factor when holes are injected into the avalanche region, k in Equation 2.23 should be substituted by 1/k. In the ideal case noise is minimized, k should equal zero for electron injection and k should be infinite for hole injection. Silicon APDs are usually used when electrons are injected into the avalanche region. When the thermal effects and total current noise are taken into account the final expression for APD noise is given as:

$$\bar{I_D^2} = 2q\left(I_P + I_{DG}\right)M^2FB + 2qI_{DS}B + \frac{4kTB}{R_L} \tag{2.24}$$

Where I_P is the photocurrent for M=1. From Equation 2.24 it can be seen that excess noise increases as the gain increases. The photocurrent generated by the optical signal is also amplified by the gain and as a result there is an optimum gain value which maximizes APD signal to noise performance. This optimum gain is achieved when the shot noise equals the thermal noise, as shown in Figure 2.5 [16, 19].



F_{AMP}: Noise figure of next stage amplifier
R_{in}: Input resistance of next stage amplifier

Figure 2.5: Signal and Noise versus gain [19].

The signal to noise ratio for an APD can be calculated as follows:

$$S/N = \frac{I_P^2 M^2}{2q\left(I_P + I_{DG}\right) BM^2 F + 2qI_{DS} + \frac{4kTB}{R_L}} \tag{2.25}$$

Operating conditions such as temperature and bias voltage play a large part in determining the APDs performance. The APD gain has a temperature dependent characteristic [16, 20]. The gain at a certain bias voltage decreases with increasing temperature. These effects can be seen in Figure 2.6.

To achieve maximum signal to noise ratio in the APD, it is necessary to set

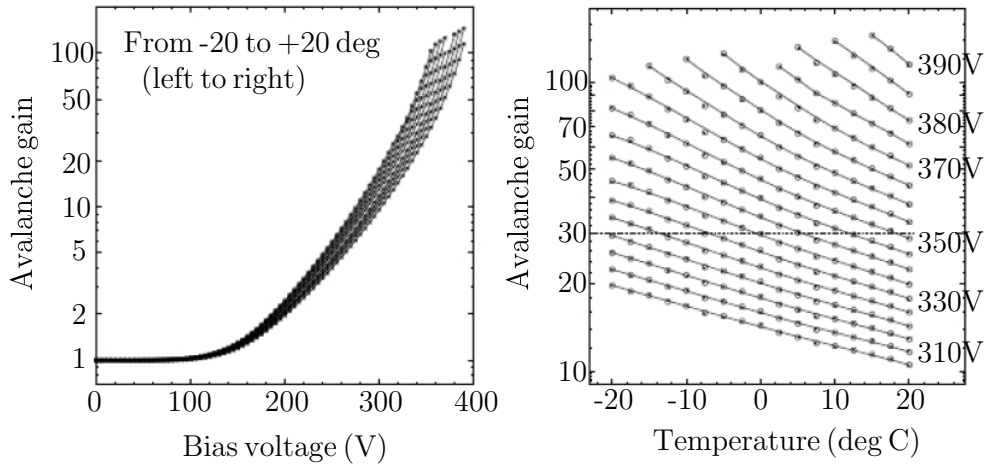


Figure 2.6: Gain variations of APD as a function of bias voltage and temperature [20].

the APD gain close to the optimum gain and stabilize it. This is accomplished by maintaining a constant temperature or adjusting the bias voltage according to the changes in temperature using appropriate control circuits. Those circuits will be introduced in more detail in Chapter 5 and a new bias and gain control circuit will be presented which can be used to maintain the APD gain independent of environmental conditions.

2.3.2 Geiger-mode

Geiger-mode avalanche photodiodes are capable of operating as single photon counting diodes or single photon avalanche diodes (SPAD). In Geiger-mode, the APD is biased above its breakdown voltage. When a photon is absorbed by the APD, an avalanche event is triggered and registered as a photon count. External circuitry, known as a quench circuit, senses this event and reduces the bias across the APD to allow it to recover. After the current dissipates, the voltage is reset, and the diode can count another avalanche event [21].
In contrast to the APD operating in linear mode, the output of a Geiger-mode

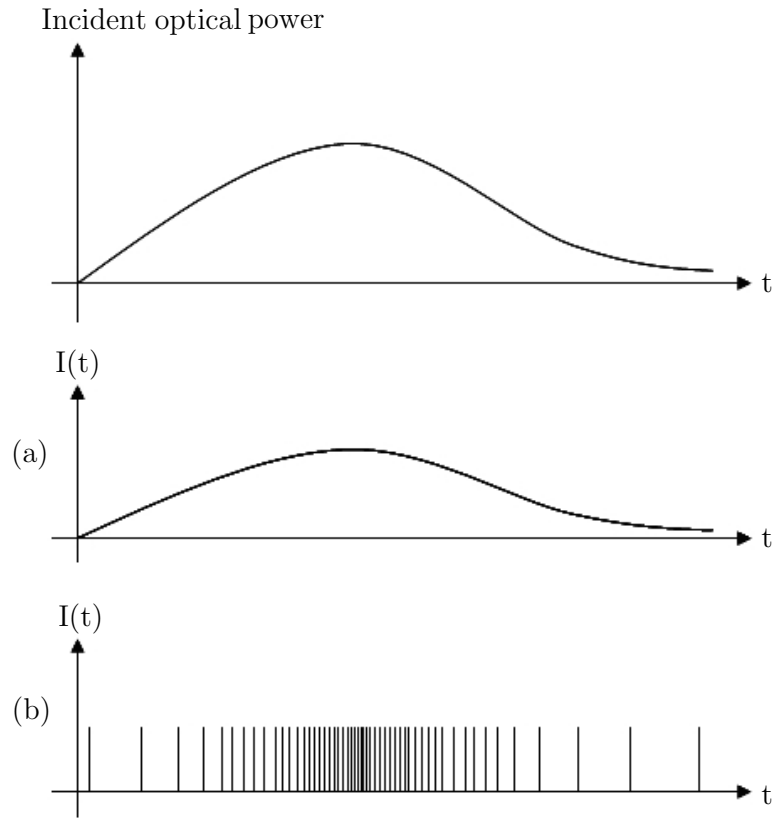


Figure 2.7: Photocurrent when APD operates in (a) linear mode and (b) Geiger-mode.

APD is not a linear current, but current pulses. The difference between operating an APD in the linear-mode and the Geiger-mode can been seen in Figure 2.7, where the photocurrent of the former is proportional to the incident optical power while the light intensity on a Geiger-mode APD gives a corresponding change in the number of current pulses per second [12]. Operating the APD in Geiger-mode eliminates many of the current fluctuations present in the linear mode. The output current pulses are sufficiently high so that variations between pulses do not matter. The external circuitry only detects that a pulse has occurred [21].

Dark count

When counting photons, the GM-APD detects the avalanche events created in the APD. The avalanche breakdowns are not only generated by photon absorption but also by other means such as thermal generation of electron-hole pairs and carriers tunnelling across the depletion region [7, 12, 21, 22, 23]. These pulses result in a noise source for the Geiger-mode detector and are referred to as dark counts due to the detection of events in the absence of a light source. The dark count rate of a GM-APD is an important parameter that should be minimised. Shockley-Reed-Hall (SRH) generation and recombination theory describes the thermal excitation of carriers in semiconductors. If an electron-hole pair is thermally generated in the depletion region, an avalanche event may occur as outlined in Section 2.2.1. If these are generated in the p-epilayer region of the GM-APD, these carriers may drift to the depletion region and cause an avalanche [12, 24]. Band-to-band tunnelling contributes to the number of dark counts if the electric-field strength is high (5×10^5 V cm^{-1}) [24, 25]. However, high electric-fields are required in GM-APDs to maximise the photon detection probability [21]. Due to these high electric-fields, an electron may tunnel from the valence band to the conduction band, thus leaving a hole behind in the valence band. As a result, the electron-hole pair may generate an avalanche event and hence a dark count. When the acceptor concentration of the p-region of the GM-APD's pn junction is increased, i.e. $N_a \geq 5 \times 10^{15}$ cm^{-3}, and hence the breakdown voltage, V_{br}, is less then 25 V, the field strength in the junction is increased such that the dark count rate due to tunnelling is increased. When operating the GM-APD, the dark count rate will increase as the following parameters increase: excess bias voltage (the bias voltage above the breakdown voltage), detector area and temperature [21, 26-30]. Decreasing the excess bias will decrease the dark count but unfortunately the photon detection probability will also be reduced. Decreasing the

active area is possible but may not suit all applications such as imaging. The temperature dependence of the dark count can be minimised by cooling the GM-APD using a thermoelectric cooler (TEC) [12].

Afterpulsing

During an avalanche event, some of the charge carriers will be captured by trapping centres in the space charge region when the avalanche current flows through the device and there are released after a period of time. These carriers could trigger a new avalanche event, which in turn can lead to further carrier trapping. The avalanche events triggered by trapped carriers are not related to new photon arrivals and are thus an unwanted source of noise called afterpulsing. Afterpulsing intensity depends on the type and number of trapping centres present in the device and the amount of charge that flows through the junction during an avalanche. Afterpulsing introduces correlation between consecutive avalanches, and limits the maximum repetition rate and so needs to be minimised.

The afterpulsing phenomenon can be minimized by allowing sufficient time for all trapped charge to dissipate before resetting the GM-APD. This is achieved using an appropriate control circuit that quenches the APD avalanche current by lowering the bias voltage below the breakdown voltage, holding the bias below breakdown for a period of time before resetting the device to its original bias voltage to await the next avalanche event. The period of time that the device is held below its breakdown voltage is known as the hold-off time. During the hold-off and reset process, no incoming photon can be detected and this leads to a reduction of the maximum achievable count-rate of the GM-APD. As a result, a trade-off needs to be made between the count-rate and an acceptable level of afterpulsing. The control circuits used to minimize the afterpulsing phenomenon and setting the hold-off time will be discussed

in detail in Chapter 3 and a quenching circuit with improved hold-off time control logic for the GM-APD will be introduced.

Jitter

Timing jitter is the delay between a photon being absorbed by the detector and the detector sending out a measurable response. It can be described as the full-width half-maximum measure of the temporal variation in the avalanche breakdown pulses resulting from an incident photon. Among the timing-resolution components are the variation caused by the generated carrier transit time from the depletion layer to the multiplication region, which is dependent on the depth of absorption of the incident photon and the statistical build up of the avalanche current itself [21, 26, 32].

2.4 Planar APD

The APD used throughout this research is the planar junction APD developed by the Photodetection and Imaging Group at University College Cork [33, 34]. A cross section of the APD can be seen in Figure 2.8. The APD can be fabricated with CMOS compatible process steps with the p-epitaxy common to the CMOS process that allows the APD to be monolithically integrated with CMOS circuitry. The central p-implant is the enrichment implant that increases the p-doping compared to the epi-layer. The overlap of the p and n layers defines the active area of the detector. The high field region is the depletion region that occurs around the pn junction where the photoelectron impact ionisation takes place. The n+ layer overlaps the high-field region into the p-epitaxial substrate, forming a virtual guard ring. The guard ring eliminates edge breakdown of the diode caused by the junction curvature effects, allowing a uniform breakdown across the surface of the junction. The n+ layer forms the diode's cathode. The annular p+ sinkers allows top contact to the

anode which aid in the removal of metallic contaminants from the high-field region [16, 35, 36]. The shallow junction of the planar APD gives the detector increased sensitivity to short wavelength light (400 to 650 nm). The doping of the junction is engineered to allow for low voltage operation (< 50 volts).

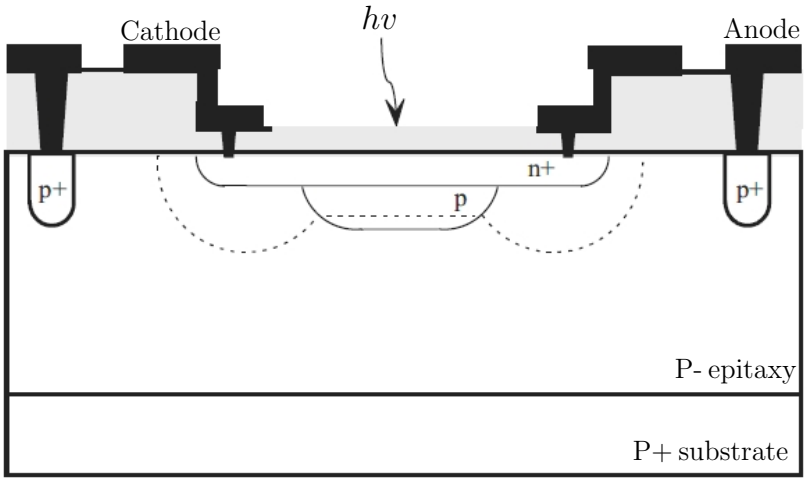


Figure 2.8: Cross section of planar shallow junction APD developed by the Photodetection and Imaging Group at University College Cork [2, 33, 34].

Planar APDs have a number of advantages over Large Area APD (LAAPD) bevelled edge structures and reach-through APD structures. In LAAPDs the impact ionisation takes place in the p-region where the electric field is low. It takes substantial time, 10ns-30ns, for multiplication and charge collection to take place. LAAPDs need a large operating voltage of between 1000 and 2000 volts. Cooling systems, such as liquid nitrogen, are needed for LAAPDs to operate in photon counting applications. Reach through APDs have high operating voltages of between 300 - 450 volts. Also, placing the high field region deep inside the detector structure and the use of a pi region requires specialised processing steps. These steps increase fabrication costs and are not CMOS compatible [2, 16]. The planar APD has a simple structure requiring fewer process steps. This leads to fewer defects and higher performance detectors. Moreover, the low operation voltage (< 50 V) makes it possible to design an on-chip bias circuit to power the APD. As will be seen in Chapter 3, an

intergrable bias solution is designed for biasing the planar APD that can be used to reduce the size, weight and power consumption of the APD-based applications.

2.5 Conclusion

This chapter has introduced the theory of photodetection and some background detail of APDs that operate in both linear and Geiger modes. The performance characteristics of the APD such as quantum efficiency, multiplication gain, bandwidth, dark count and afterpulsing have been discussed. The APD requires many external control circuits for enhancing its performance. In the following chapters, some of these control circuits will be introduced and improved circuit designs will be presented. These circuits include a bias circuit, a gain stabilization circuit and a quenching circuit. The bias circuit is used to provide the high bias voltage for powering the APDs that operate in both linear and Geiger modes. The quenching circuit is used to perform photon counting while minimising the afterpulsing phenomenon in the Geiger-mode APDs. The gain stabilization circuit is designed for the APD that operates in linear mode to control and maintain its gain independent of temperature and power supply fluctuations.

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Chapter 3

Biasing Avalanche photodiodes

It was shown in Chapter 2 that high bias voltages and mA range load currents are needed for the operation of APDs. This chapter presents a bias solution that meets these requirements and can be used for APDs operating in both linear and Geiger modes. In this chapter, the bias requirements for APDs and APD-based applications are introduced. A number of bias solutions are reviewed and discussed. The design and development of a dual-rail charge pump based bias circuit is described. The operation of this circuit is evaluated experimentally and its drawbacks identified. An improved bias circuit which simplifies the overall control of the bias voltage and eliminates the need for a negative voltage rail was developed and implemented. A layout of the circuit was designed using the L-Foundry 0.15 μm process and post layout simulations are presented.

3.1 Introduction to APD Bias solutions

The bias voltage needed for the APD's operation is determined by its architecture. In this work, the APDs used are the planar shallow junction APDs developed by the Photodetection and Imaging Group at University College Cork [1]. These planar APDs operate with a much lower bias voltage (< 50 V) [2, 3] than that needed for Large Area APDs (1000 V $\sim$ 2000 V) [4-6] and reach through APDs (300 V $\sim$ 500 V) [7-9]. However, it's still difficult to bias

these at voltages that are in excess of the voltage requirements for the rest of the sensing system which is typically 3.3 V or 5 V [10-13].

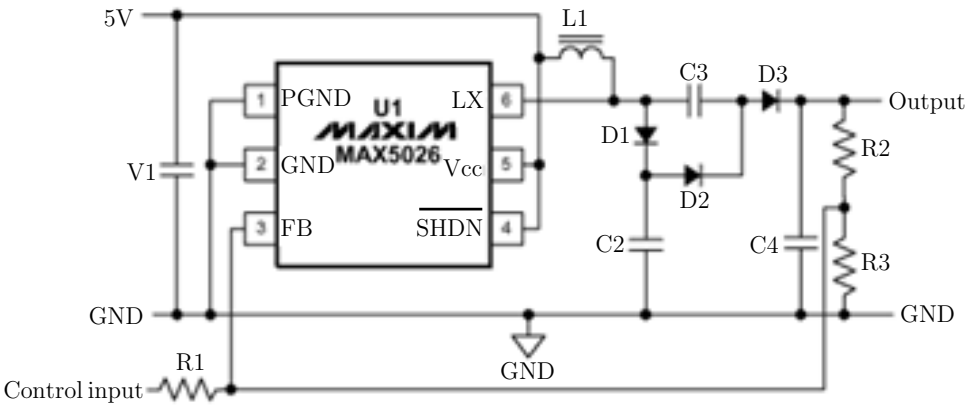
An external high-voltage supply such as that shown in Figure 3.1 is normally used to bias the APDs. This kind of supply is bulky, expensive and can not be used in portable devices.



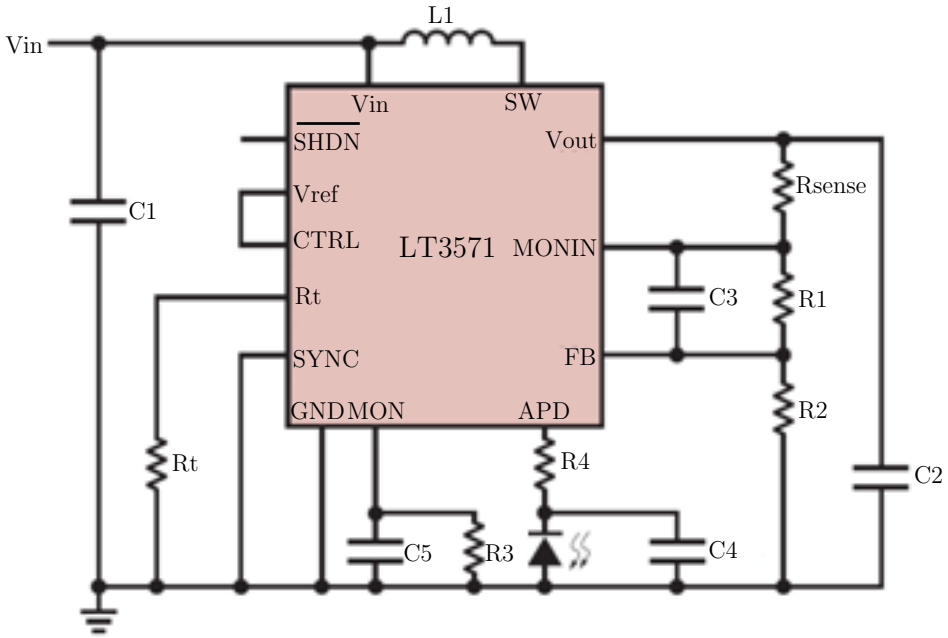
Figure 3.1: Bench top power supply (Keithley 2400 digital sourcemeter)

Many step-up DC-DC converter chips are available in the market for biasing APDs. These chips are designed to have a high output voltage to bias the APD [14, 15]. However, several external discrete components are required for them to function correctly, as shown in Figure 3.2, thereby limiting their usefulness in compact or integrated applications. The step-up DC-DC chips are mostly based on boost converters which are traditional high voltage generation circuits and widely used in discrete circuits [16, 17]. A basic schematic of a boost converter is shown in Figure 3.3.

The main drawback of these circuits is the use of inductors which lead to a large board area and height such as in [18]. When implementing an integrated circuit, the fabricated on-chip inductors are normally large and have low inductance and quality factors [19-21]. For example, the chip area required for



(a)



(b)

Figure 3.2: Commercial bias solutions for APDs: (a) MAXIM MAX5026, 5 V to 71 V APD power supply [14] and (b) LINEAR TECHNOLOGY LT3571, 5 V to 45 V APD bias power supply [15]

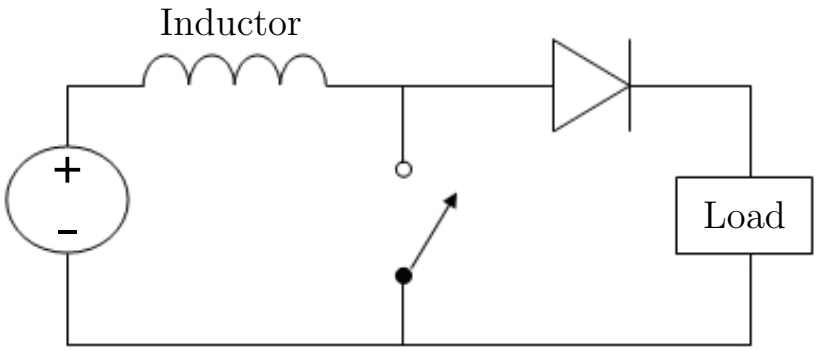


Figure 3.3: Basic schematic of a boost converter

a 58 nH inductor in [20] is 4 mm^2 and a 13.1 nH inductor in [21] occupied 0.8 mm^2 chip area. This drawback limits the boost converter's usefulness in on-chip step-up DC-DC converters which usually require large value inductors. Moreover, for most conventional CMOS processes, there is no standard inductor available in the libraries which makes designing an integrated boost converter with conventional CMOS processes difficult [22]. In [23], Yao-Yi Yang *et al.* presented a boost converter based bias circuit for APDs. The design can provide up to 80 V bias voltage for APDs with low output voltage ripple (after an external RC low pass filter). However, the use of a high value inductor (3.3 μH) makes it incapable of being fully integrated.

Compared with boost converters, charge pump DC-DC converters are inductorless and the main components needed are capacitors and switches (diodes or transistors) which can be easily integrated on chip with currently available CMOS technologies. In [24, 25], charge pumps are used to provide on-chip power supply for biasing the APDs. With those solutions, the size, weight and power consumption of the APD-based systems are reduced. However, there are several drawbacks remain in those designs. Firstly, the bias voltages produced are not high (11 V in [24] and 25 V in [25]) that limit their usefulness for the APDs that require higher bias voltages (e.g. in this project the APD used

has a breakdown voltage of 27 V and operates with the bias voltage from 25 V to 35 V). Moreover, in [24, 25], the maximum load current the bias circuits can provide are not mentioned which is a very important aspect for the bias circuits. If the maximum load current provided is small, when the illumination level to the APD is high or the APD arrays are used, the circuit will not be able to maintain the high bias voltage required. With the aim of developing an integrable bias circuit with high bias voltage and load current, as will be shown, a new regulated charge pumps are designed.

3.2 Design of an integrable bias circuit

For generating high output voltages and load current, regardless of the types of charge pumps, a large number of stages are required [26-29]. As the number of stages is increased, the threshold voltage of the MOS devices increases due to the body effect and the energy losses in each stage can significantly reduce the pumping gain and limit the circuit's performance [30]. With the same structure, fewer stages gives lower energy losses for each stage and less area occupation for the charge pumps. As will be shown, the dual-rail charge pump circuit proposed is utilized to generate a high potential between the positive and negative output with a small number of stages.

3.2.1 Circuit description

An overview of the proposed bias circuit is shown in Figure 3.4 and consists of two main parts: (i) A dual-rail charge pump which provides the high bias voltage for the load. (ii) Two shunt regulators which are used to control the output voltage for the positive and negative nodes of the load.

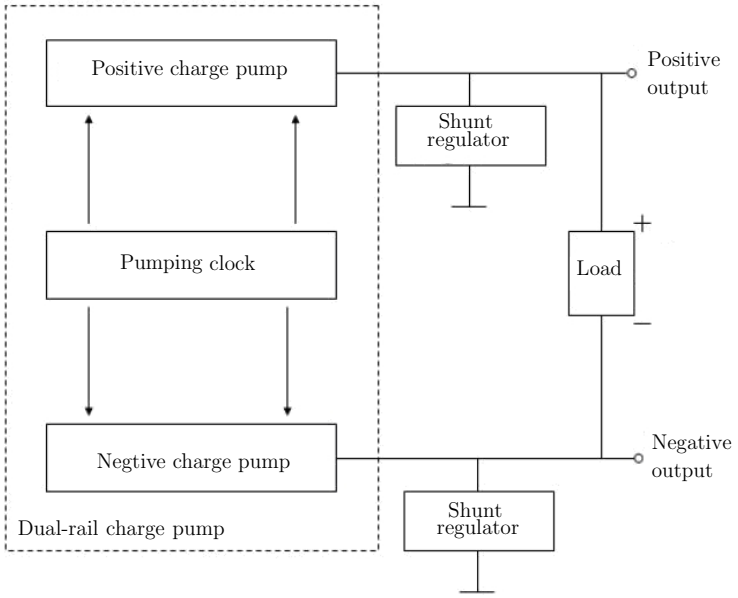


Figure 3.4: Block diagram of overall bias solution

Charge pumps

Figure 3.5 shows the schematic of the dual-rail charge pump. The positive and negative charge pumps used in Figure 3.5 are Dickson pump circuits [31]. The MOS transistors in the circuit are connected in diode fashion. The neighbouring pumping capacitors are connected to two inverse pumping clocks. NMOS is used for the positive charge pump to transfer the positive charge to the positive output. PMOS is used for the negative charge pump to transfer the positive charge away from the negative output [30].

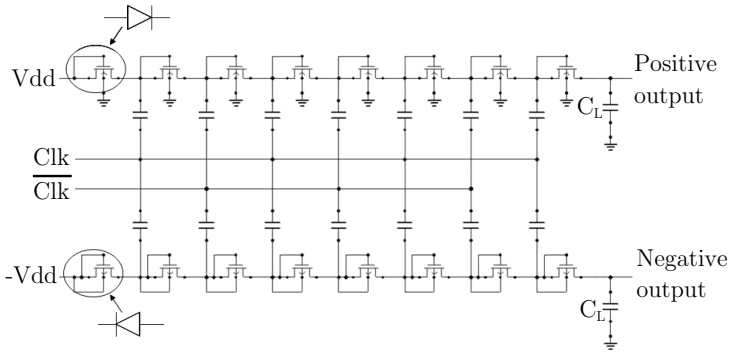


Figure 3.5: Schematic of dual-rail charge pump

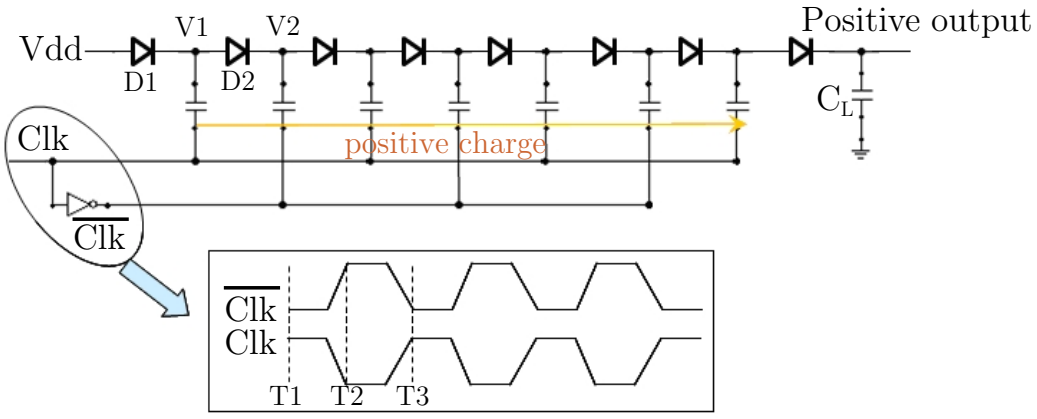


Figure 3.6: Positive charge pump

The charge pump shown in Figure 3.6 boosts the voltage at the positive output by the pumping clocks Clk and $\overline{Clk}$. At T1 when Clk is high and $\overline{Clk}$ is low, diode D1 is forward biased and V1 is (V_{dd} - V_d), where V_d is the forward voltage of the diode. Next, at time T2 when Clk is low and $\overline{Clk}$ is high, V1 is pushed up to ($2V_{dd}$ - V_d). D2 is forward biased and V2 is ($2V_{dd}$ - $2V_d$). At time T3 when Clk is high and $\overline{Clk}$ is low, V1 is pushed up to ($3V_{dd}$ - $2V_d$). In the same way, through every stage that consists of a capacitor-diode pair, the voltage is boosted stage by stage and at the output a high potential exceeding the power supply voltage can be obtained.

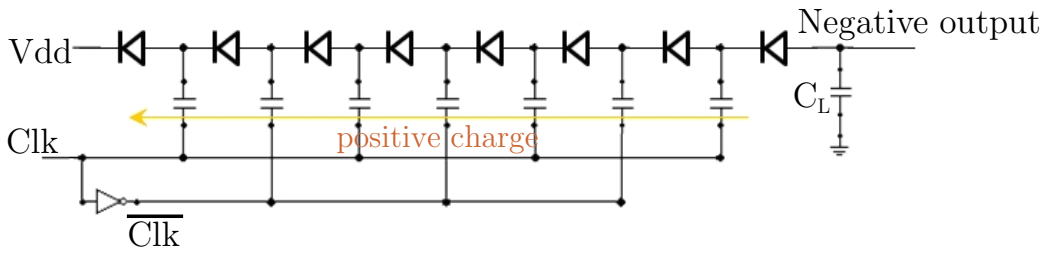


Figure 3.7: Negative charge pump

Similar to the positive charge pump, the negative charge pump is built on

capacitor-diode pairs. To achieve a negative output, the direction of the charge movement in the negative charge pump shown in Figure 3.6 is opposite to the positive charge pump. Through every stage, the positive charge is removed from the negative output that reduces its voltage from the initial level (here it is V_{dd}) to a negative level.

Shunt regulator

For the control of the charge pump's outputs, shunt regulators are used. With the shunt regulators, the charge pump operates continuously. Figure 3.8 shows the schematic of the shunt regulator. This regulator uses a MOS transistor (NMOS for positive output and PMOS for negative output) in parallel with the load and behaves functionally like a variable current divider to obtain load voltage regulation [32]. R1 and R2 are used to decrease the output voltage to a comparable level, V1.

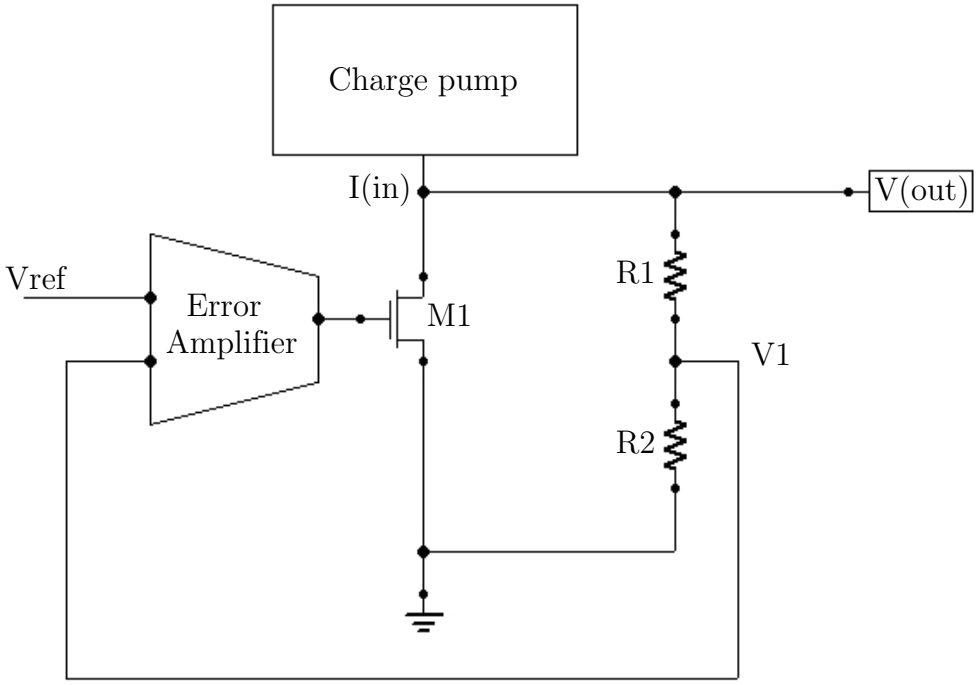


Figure 3.8: Schematic of shunt regulator

A two-stage op-amp is used as the error amplifier (see Figure 3.9) [33]. The first stage is a differential input stage; the second stage is a common-source stage with an active load. The differential pair transistors have equal dimensions and are biased by a current mirror with one diode connected PMOS transistor as the load. All the transistors have a minimum length of 0.35 μm. The widths of M1, M2, M3, and M4 are set to 25 μm, M5 and M8 are set to 16 μm, M6 is set to 15 μm, M7 is set to 8 μm and M9 is set to 2 μm. A power supply of V_{dd} and GND are used for amplifying the positive error, a power supply of GND and -V_{dd} is used for amplifying the negative error. Simulations show the DC Gain and GBW can reach 48dB and $>$ 100MHz with a 20 pF load capacitor. The Phase Margin was simulated to 60 degrees that guarantees the stability of the amplifier (see Figure 3.10).

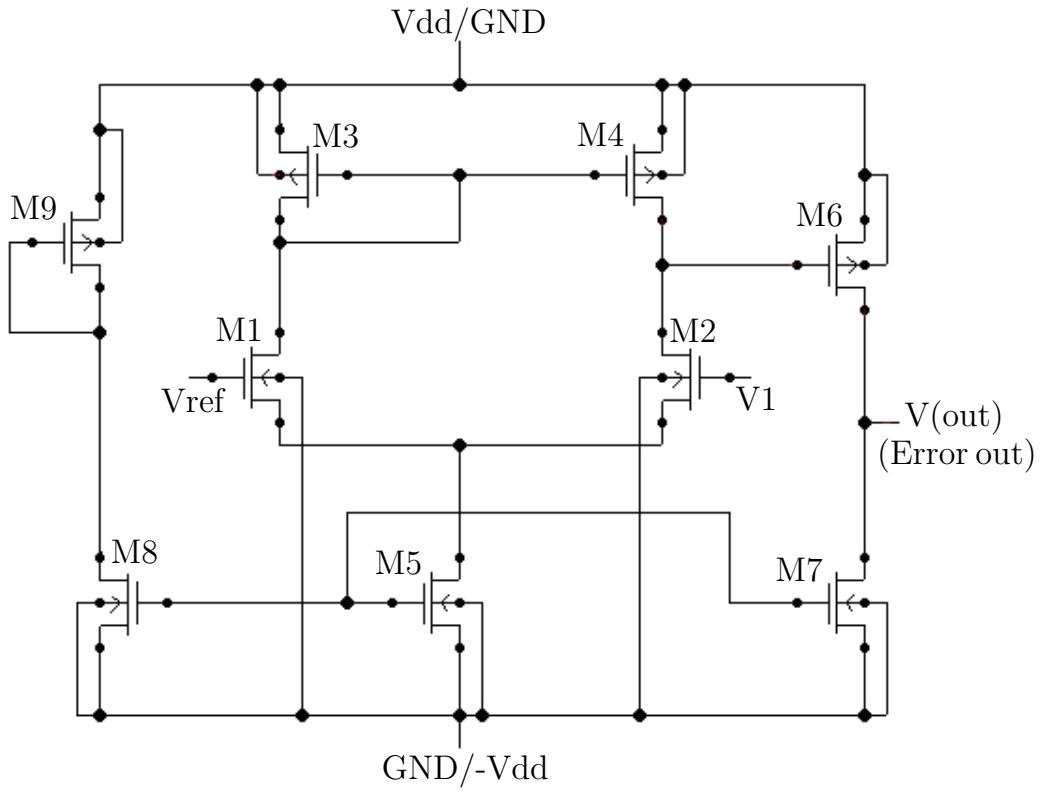


Figure 3.9: Schematic of two-stage op-amp

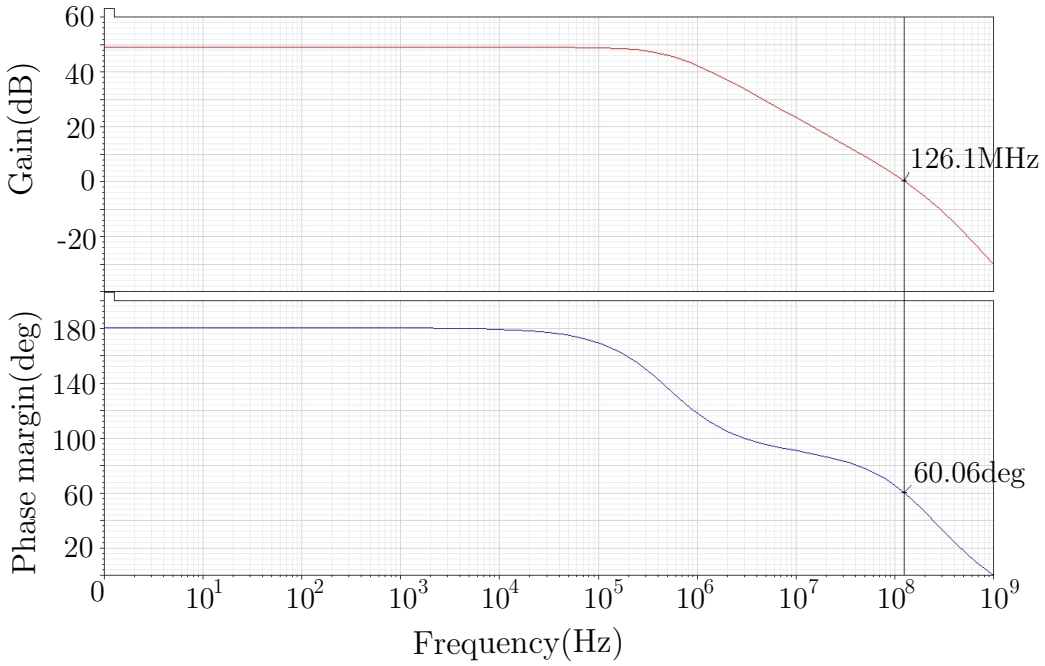


Figure 3.10: AC sweep of the 2-stage op-amp

With the error amplifiers, the operation of the shunt regulation shown in Figure 3.8 is described as follows: If V1 exceeds the regulation level V_{ref}, the error amplifier generates an output voltage proportional to the difference between V_{ref} and V1 and the MOS transistor will be biased to divide the output current. If the output falls below the regulation level, the MOS transistor will be turned off, and the output can be continuously charged up. In this way, V1 can be set equal to V_{ref}. By setting the reference voltage V_{ref}, the output voltage can be altered.

3.2.2 Simulations

The circuit was simulated using Austria Microsystem's 0.35 μm CMOS process [34] running in the Cadence design environment. A 7-stage dual-rail charge pump with shunt regulators was used. The pumping capacitors are 20 pF. The two load capacitors are 3 nF each and are the only external components required for this design. The clock frequency is 50 MHz with $V_{dd} = V_{clk} = 5$ V.

Figure 3.11 demonstrates the regulation of the positive output voltage at 15 V. As can be seen from the figure, when the positive output reaches the regulation level, the error amplifier generates an output voltage to bias the NMOS transistor. The excess current to the output is divided by the NMOS transistor that maintains the positive output voltage equals to the regulation level.

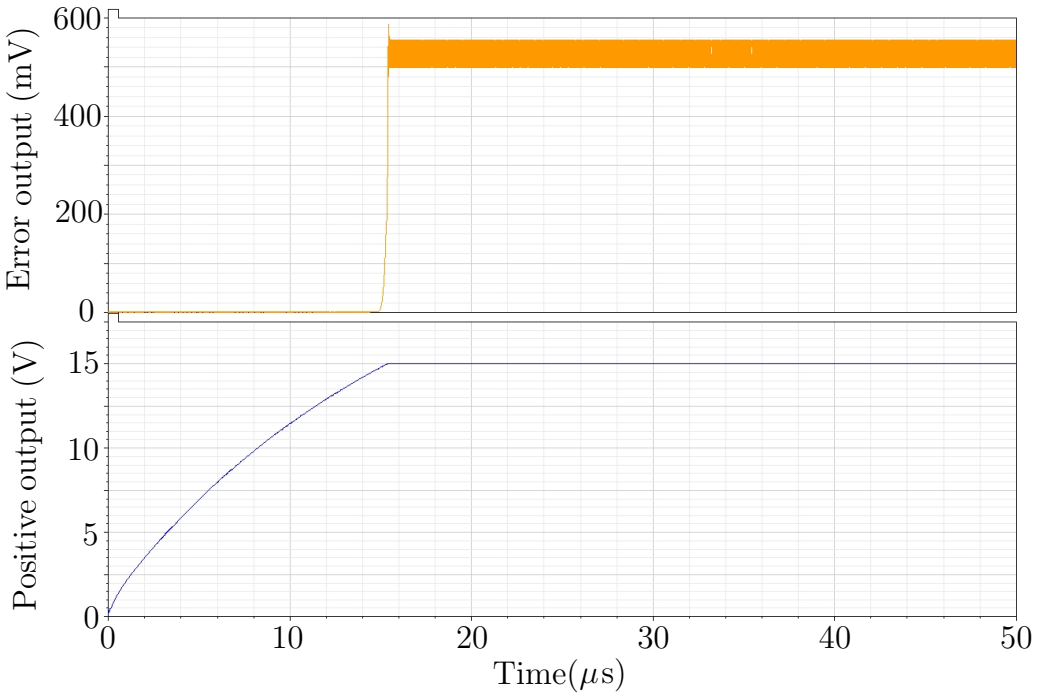


Figure 3.11: Regulation of positive output to 15 V

Similar to the regulation of the positive output, the error amplifier in the negative charge pump circuit generates a negative voltage to bias the PMOS transistor. The excess negative current to the negative output is divided by the PMOS transistor that makes the negative output voltage equals to the regulation level (see Figure 3.12).

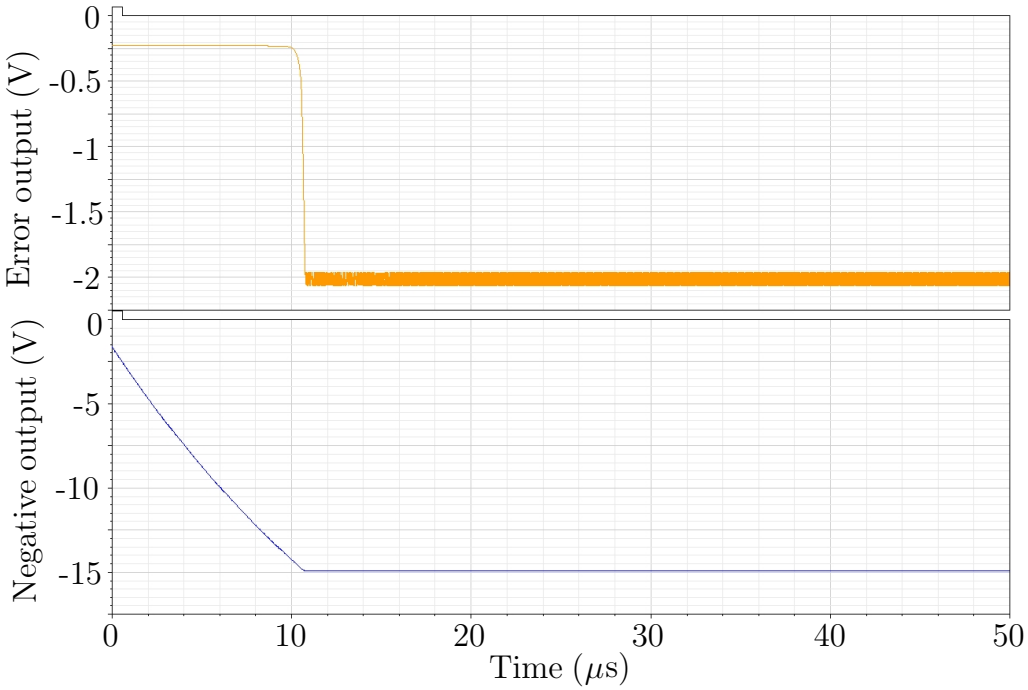


Figure 3.12: Regulation of negative output to -15 V

In Figure 3.13, Figure 3.14 and Figure 3.15, the bias voltages and the output voltages of the positive node and the negative node when the bias voltage is regulated at 25 V, 30 V and 35 V are illustrated. Simulation results show that the bias voltage can be regulated accurately with a peak-peak ripple of less than 25 mV.

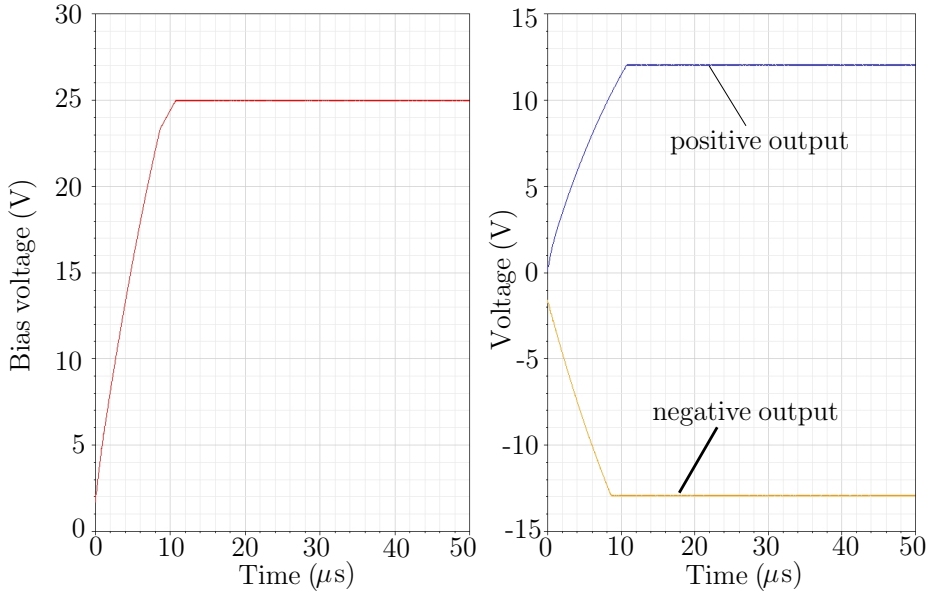


Figure 3.13: Simulation results when the bias is regulated to 25 V

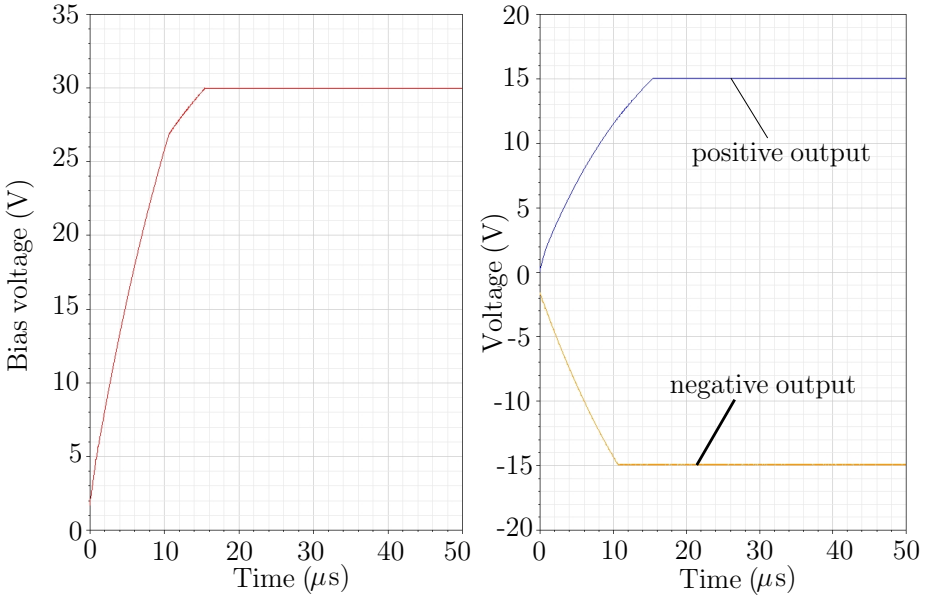


Figure 3.14: Simulation results when the bias is regulated to 30 V

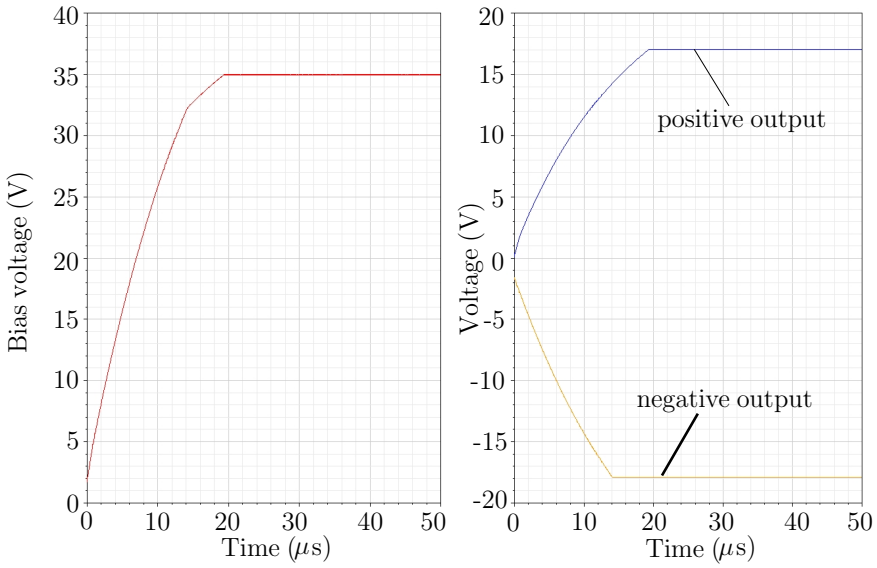


Figure 3.15: Simulation results when the bias is regulated to 45 V

Figure 3.16 shows the maximum load current and output power for different bias voltages. From the simulations it is clear that the circuit is capable of meeting load current demands in excess of 1 mA at bias voltages up to 45 V.

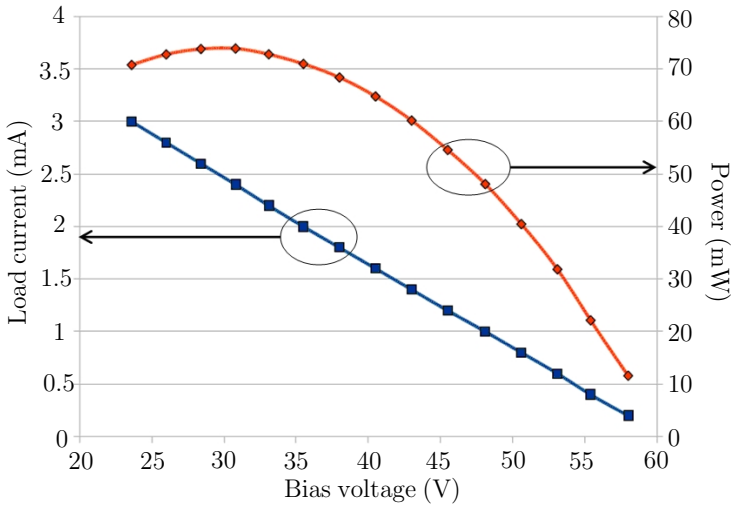


Figure 3.16: Simulation results of maximum load current and output power for different bias voltages

3.2.3 Printed circuit board (PCB) implementation

With discrete components, the circuit was implemented on a printed circuit board (PCB). Due to large parasitics and speed limitations of a discrete implementation, larger capacitors are used. The pumping capacitors are 0.1 μF and the load capacitors are 1 μF. The N-transistors and P-transistors used are ZVN3306F and ZVP3306F, respectively. A TLE2021IP low-power precision op-amp is used as the error amplifier. The clock frequency is 100 kHz with V_{dd} = V_{clk} = 5 V.

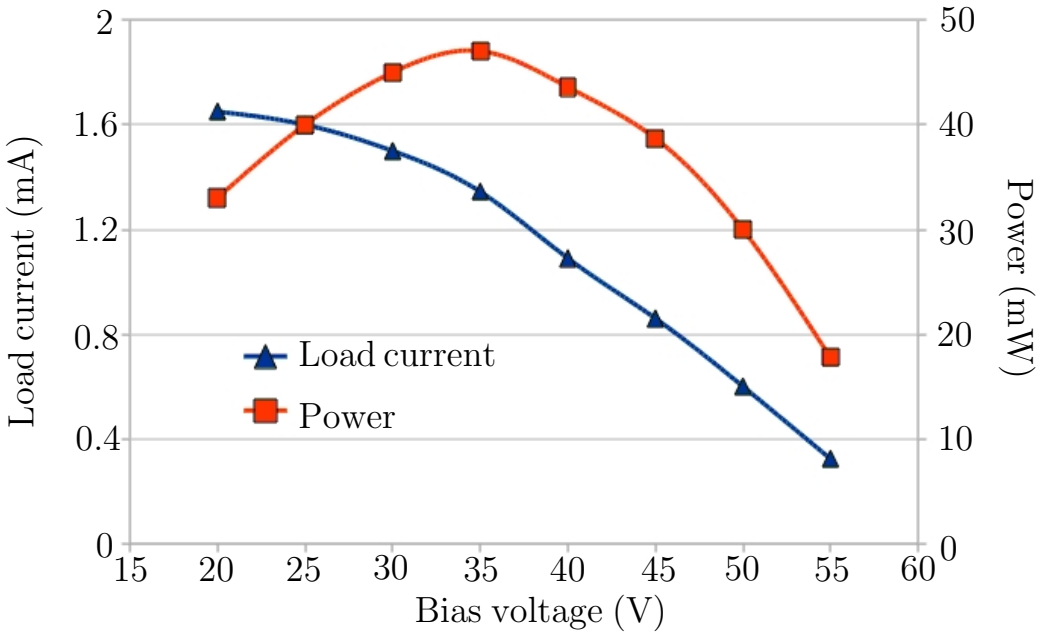


Figure 3.17: Plots of maximum load current and output power for different bias voltages

In Figure 3.17, the maximum load current and output power for different bias voltages are demonstrated. It shows the circuit is capable of delivering greater than 1 mA at a bias voltage up to 40 V.

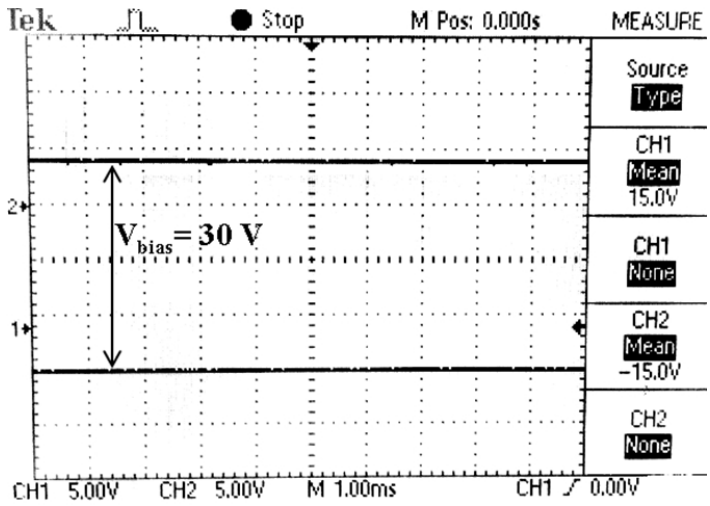


Figure 3.18: Oscilloscope trace when the bias voltage is regulated to 30 V.

Figure 3.18 shows the bias voltage when it is regulated at 30 V. The voltage ripples on the positive and negative output are 120 mV and 180 mV respectively; see Figure 3.19.

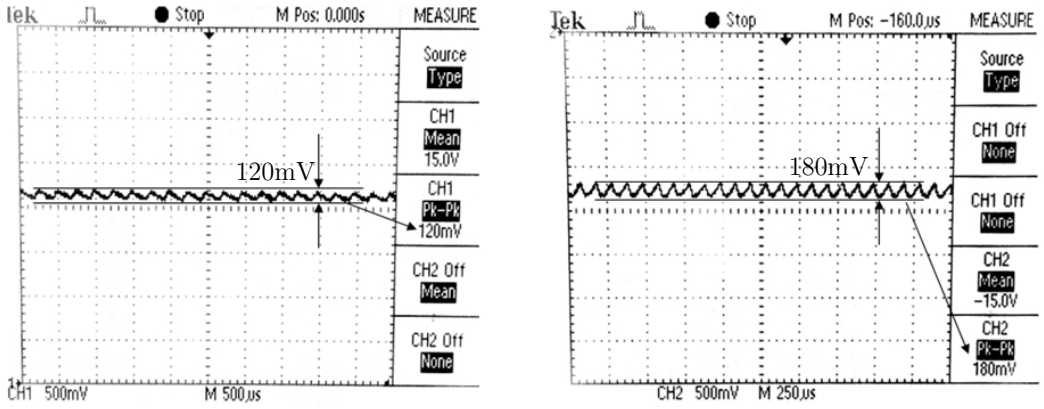


Figure 3.19: Voltage ripples on the positive and negative output.

This is mainly caused by two factors: (i) Noise due to the discrete implementation. (ii) Low speed of the amplifier, which means the amplifier cannot generate the error voltage quick enough when the output voltage exceeds the regulation level. The ripples can be reduced with an integrated circuit implementation or a faster amplifier [35, 36].

In summary, the circuit introduced is based on a dual-rail charge pump and was simulated in Cadence. A PCB module was fabricated and measured to verify the circuit function. Both simulations and experimental measurements show the circuit proposed is capable of providing in excess of 50 V for biasing planar APDs. Results also show that the output bias voltage can be adjusted precisely and can sustain mA output current up to 40 V bias voltage. However, there are several drawbacks to this circuit. In this design, two control voltages require adjusting by the end user to provide the required output voltage and a negative supply rail is needed to control the negative output, which adds to the complexity of the circuit. As will be seen in the next section, a new approach is designed to overcome these drawbacks.

3.3 New approach to the bias circuit

To overcome the limitations of the old design, a new approach was designed. In this circuit, pass-gate based voltage regulators replace the shunt regulators and the negative voltage regulator is now linked to the positive output, which links the bias voltage to the reference voltage of the positive voltage regulator. This simplifies the overall control of the bias voltage and eliminates the need for a negative voltage rail in the circuit. The layout of the circuit was designed using the L-Foundry 0.15 μm process and the final design has a small footprint of 1.55 mm $\times$ 1 mm.

3.3.1 Circuit description

Figure 3.20 shows the schematic of the new approach of the bias circuit which consists of: (i) Positive and negative charge pumps to provide the high bias voltage for the APD. (ii) Positive and negative voltage regulators that control the voltage of the positive and negative output.

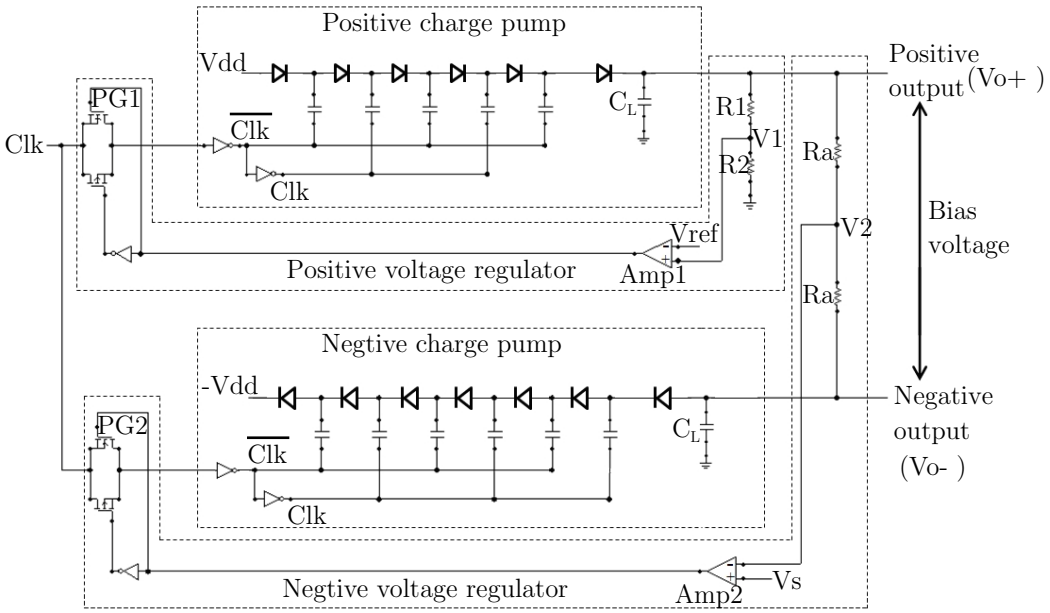


Figure 3.20: Schematic of new bias circuit

The positive and negative charge pumps used are the same as described in Section 3.1. For the bias voltage regulation, pass-gates (PG1 and PG2) are connected between the input clocks and the charge pumps and controlled by the output of the operational amplifiers (Amp1 and Amp2). R1, R2 and Ra are potential dividers used to limit the input voltage range at nodes V1 and V2. V1 is connected to the non-inverting input (+) of Amp1 and V2 is connected to the inverting input (-) of Amp2.

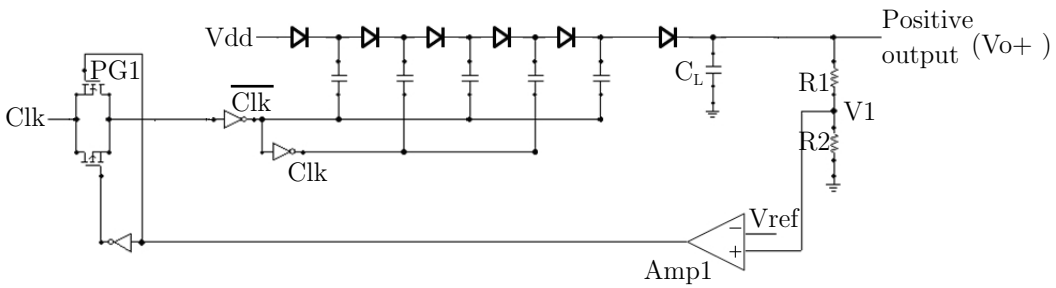


Figure 3.21: Positive charge pump and regulation circuits

The regulation circuit for the positive output is shown in Figure 3.21. In the circuit, if V1 exceeds the regulation level, V_{ref}, the amplifier Amp1 generates an output voltage proportional to the difference between V_{ref} and V1. The pass-gate PG1 is turned off to block the input clocks and the positive output is decreased. If the output falls below the regulation level, the pass-gate will be turned on and the output can be charged up. In this way, V1 can be set equal to V_{ref} and the positive output voltage can be altered and V_{o+} can be calculated using

$$V_{o+} = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \tag{3.1}$$

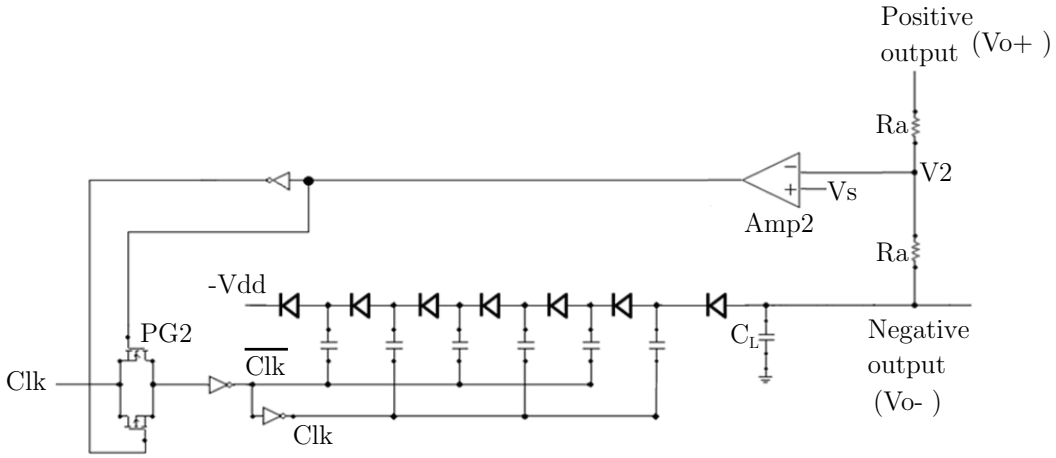


Figure 3.22: Negative charge pump and regulation circuits

The regulation circuit for the negative output is shown in Figure 3.22. In the circuit, if V2 is less than the set voltage, Vs, the amplifier Amp2 generates an output voltage proportional to the difference between Vs and V2. The pass-gate PG2 is turned off to block the input clocks to the negative charge pump, the amplitude of the negative output is decreased and V2 is increased. If V2 exceeds Vs, the pass-gate PG2 will be turned on, the amplitude of the negative output can be charged up and V2 will be decreased. In this way, V2 can be set equal to Vs and V_{o-} can be calculated using

$$V_{o-} = 2V_s - V_{o+} \tag{3.2}$$

The bias voltage Vbias is the difference between V_{o+} and V_{o-}

$$V_{bias} = V_{o+} - V_{o-} \tag{3.3}$$

Replace V_{o+} and V_{o-} using (3.1) and (3.2), gives

$$V_{bias} = 2V_{ref} \times \left(1 + \frac{R1}{R2}\right) - 2V_s \tag{3.4}$$

In this circuit, the ratio of R1 and R2 is set to 9/1 and Vs is set to 1 V that gives

$$V_{bias} = 20 \times V_{ref} - 2 \tag{3.5}$$

As can be seen from (5), the bias voltage of the circuit can be regulated linearly by setting the reference voltage V_{ref}.

3.3.2 Layout and simulations

The layout was designed with L-foundry 0.15 μm CMOS process [37]. A 5-stage positive charge pump and a 6-stage negative charge pump are used. The pumping capacitors are set to 20 pF. Except for the 2 load capacitors, all the other components of the circuit are implemented on the chip.

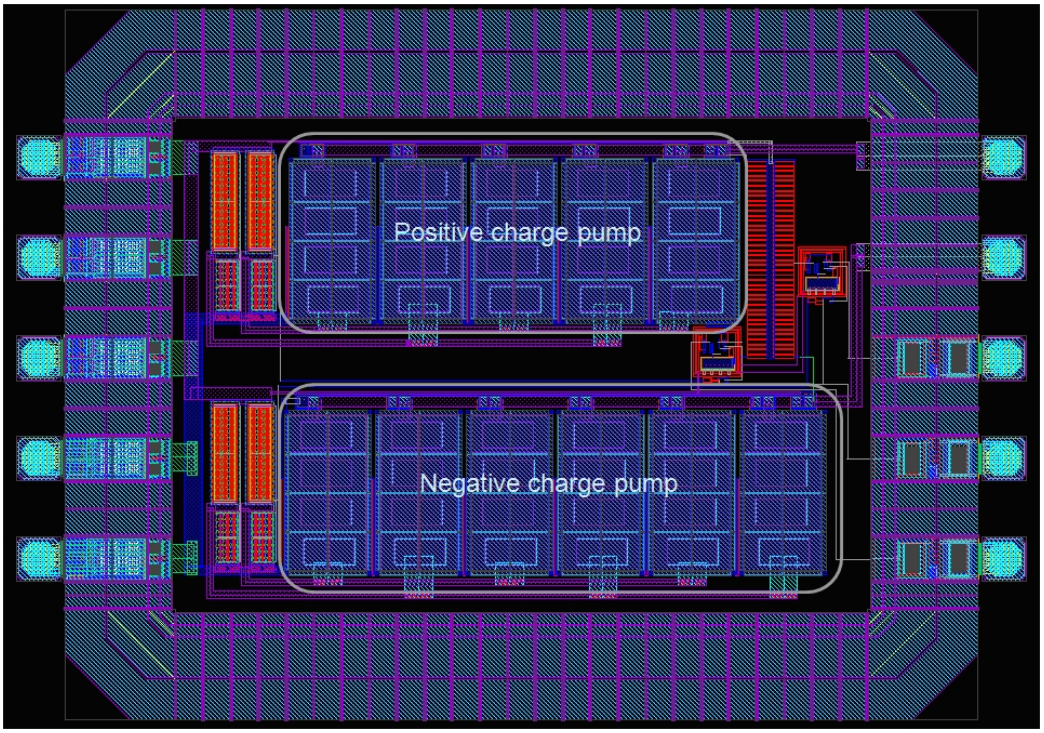
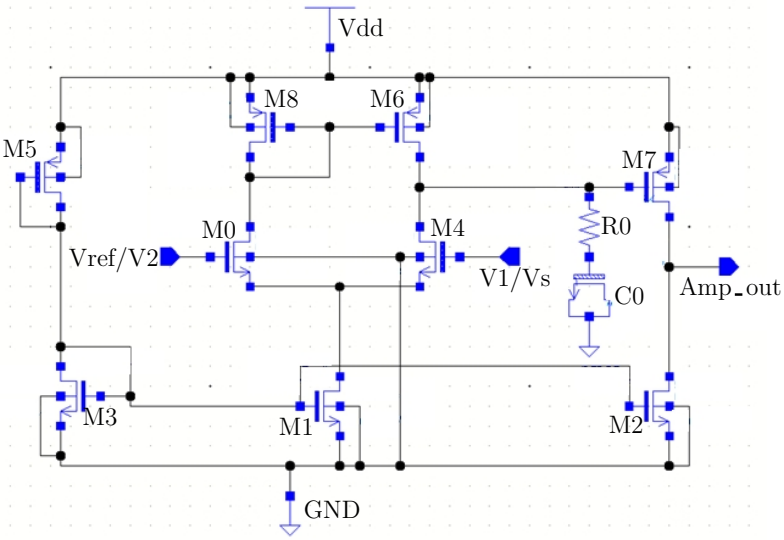
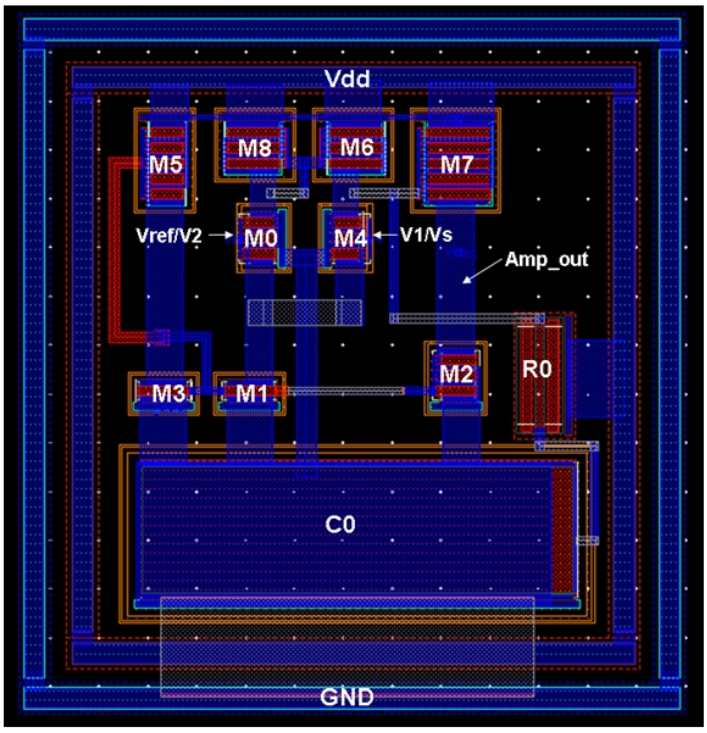


Figure 3.23: Layout of the designed circuit

The op-amp schematic is shown in Figure 3.24(a) and the layout is shown in Figure 3.24(b). The pass-gate regulator schematic is shown in Figure 3.25(a) and the layout is shown in Figure 3.25(b). The completed circuit layout is shown in Figure 3.23 which has dimensions of 1.55mm $\times$ 1mm. All the simulations reported are post-layout simulations.

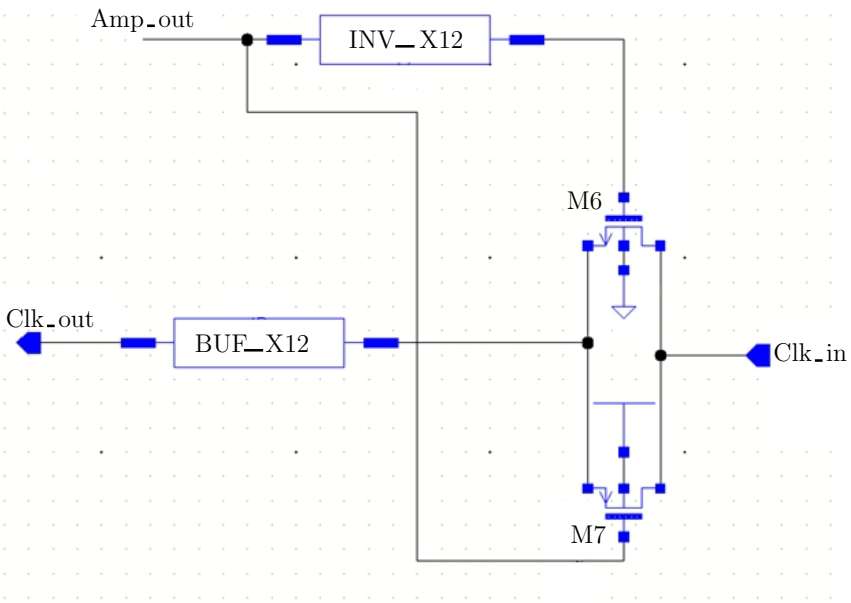


(a)

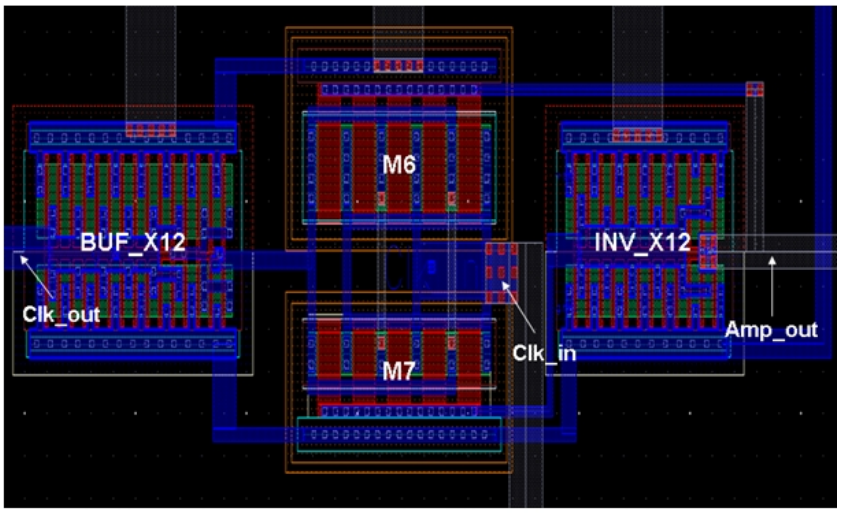


(b)

Figure 3.24: (a) Schematic of the op-amp; (b) Layout of the op-amp.



(a)



(b)

Figure 3.25: (a) Schematic of the pass-gate regulator; (b) Layout of the pass-gate regulator.

For the simulations, the two load capacitors, set to 5 nF each, are the only external components of the circuit. The simulations were completed in the Cadence design environment. The clock frequency is 50 MHz with $V_{dd} = V_{clk}$ = 5 V.

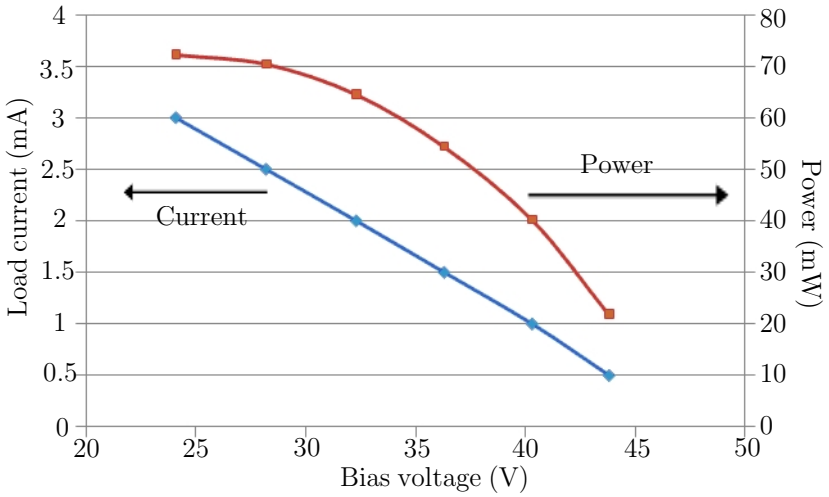


Figure 3.26: Simulation results of maximum load current and output power for different bias voltages

Figure 3.26 shows the maximum load current and output power for different bias voltages. It is clear that the circuit is capable of meeting load current demands in excess of 1 mA for bias voltages up to 40 V.

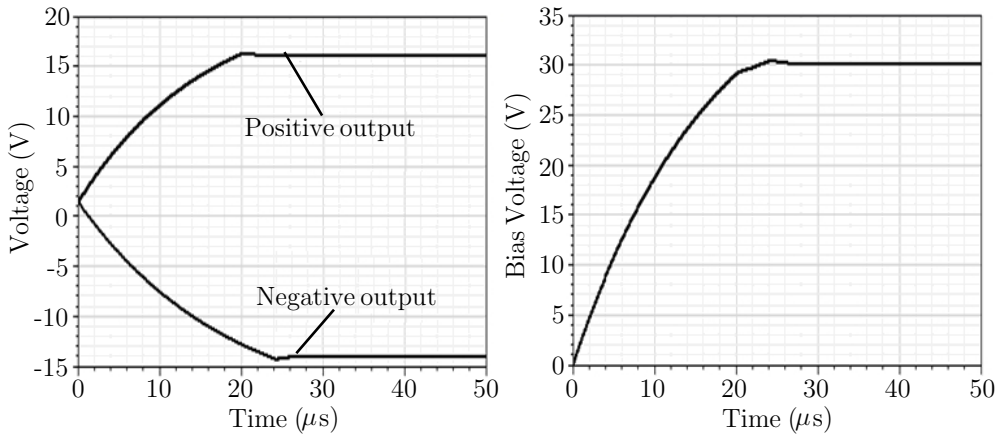


Figure 3.27: Positive and negative output when the bias voltage is regulated to 30 V

Figure 3.27 shows the Positive and negative output when the bias voltage is regulated to 30 V. Here V_{ref} is set to 1.6 V that makes the positive output voltage equal to 16 V and the negative output voltage equal to -14 V (2 V - Positive output). As can be seen from the figure, with the voltage regulators, the bias voltage is precisely set to 30 V. With the accurate control of the bias voltage, the excess bias (bias voltage above the breakdown voltage of the APD) can be stabilized by using the "Time over Threshold" introduced in [25]. This method measures the dark photon count pulse width which is as a function of the excess bias, then adjusts the bias voltage to achieve a constant pulse width that makes the excess bias stable.

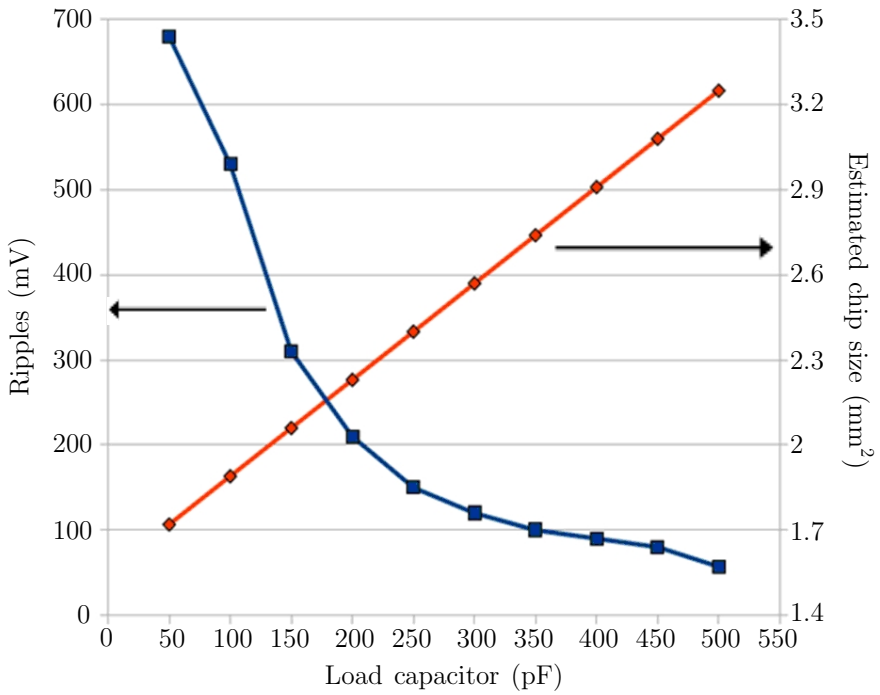


Figure 3.28: Bias voltages ripple and estimated chip size for different load capacitors

Figure 3.28 shows the bias voltage ripple for different load capacitors when the bias voltage is regulated at 30 V with a load current of 1 mA. The estimated chip size when the load capacitors are integrated on the chip is also illustrated. As can be seen from the figure, the ripple can be decreased to around 70 mV

when the values of the load capacitors are set to more than 500 pF. That means this circuit is capable of full integration if the bias voltage's ripple requirement of the devices is not very stringent (e.g. < 100 mV). [38]

3.4 Conclusions

This chapter has described the development of a bias circuit for avalanche photodiodes (APDs). The circuit design was explained and simulations were performed. A discrete version of the circuit was fabricated and tested. A layout of this circuit was also implemented with a conventional CMOS process. Results show that the circuit is capable of sourcing mA range load currents for shallow-junction planar APDs that operate up to 40 V. The layout of the circuit designed with the L-Foundry 0.15 μm process shows a small footprint of 1.55 mm $\times$ 1 mm, making it suitable for hybrid integrated with the 2 external capacitors and an APD in a single package to operate seamlessly from a 5 V supply, thereby taking the additional responsibility for biasing the APD from the end-user. In the end, the possibility of developing a full integration version of this circuit was also discussed which shows the circuit is capable of fully integrated for the devices with voltage ripple tolerance of greater than 70 mV. Compared to the existing solutions that include external high-voltage supplies, DC-DC converter chips and reported designs [14, 15, 23], this bias solution is inductorless, highly integrable and provides a more compact solution that can be used to reduce size, weight and power consumption for APD-based applications.

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Chapter 4

Active quench and reset circuit (AQRC) for Geiger-mode avalanche photodiodes

As described in Chapter 2, the afterpulsing phenomenon is an unwanted source of noise for the GM-APD which needs to be minimized. This is accomplished by properly setting the hold-off time using a quenching circuit. This chapter introduces the design and development of a new active quench and reset circuit (AQRC) for Geiger-mode avalanche photodiodes (GM-APDs). Firstly, several previously reported quenching circuits and hold-off time control techniques are reviewed. The merits and drawbacks for each circuit are discussed. Next, a new AQRC with high-resolution hold-off time control logic is designed to overcome the drawbacks in the existing AQRCs. A layout of the circuit is designed and post-layout simulations are performed to evaluate the operation of the circuit. Following that, an improved approach is presented that simplifies the end-user control. The circuit was fabricated using AMS 0.35 μm CMOS process and tested with a GM-APD.

4.1 Quenching circuits and hold-off control techniques

In APD-based photon counting applications, the photo current generated in the GM-APDs must be eliminated after an avalanche event. This is accomplished by using passive or active quenching circuitry. A passive quenching circuit is the simplest way to quench the avalanche in a GM-APD. In passive quenching, the GM-APD is connected in series with a high value resistor. The operation of a passive quenching circuit is illustrated in Figure 4.1.

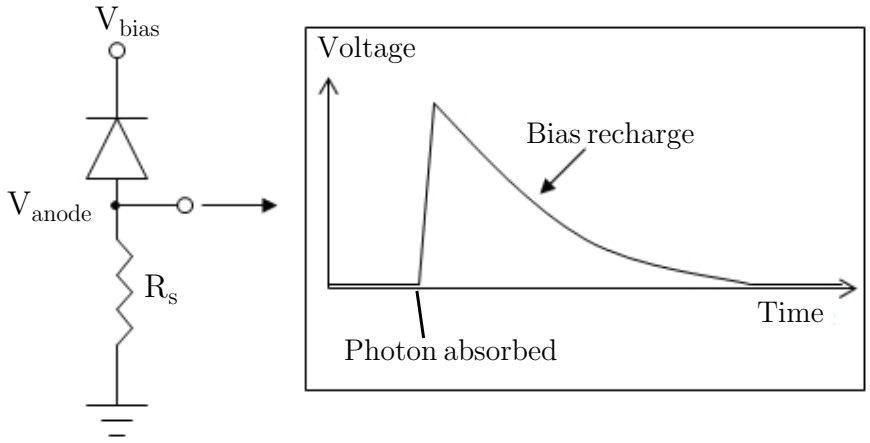


Figure 4.1: Passive quenching circuit

When an avalanche event happens in the GM-APD, a large voltage increases by the large series resistor at the GM-APDs anode and the bias across the GM-APD is quenched to its breakdown voltage. During this process, the diode current rises to its peak value which determined by the values of excess bias voltage and the series resistor. The quenching time can be defined as:

$$t_q \cong (C_j + C_p)\, R_d \tag{4.1}$$

Where C_j is the junction capacitance of the APD, Cp is the parasitic capacitance at the anode of the APD and Rd is the equivalent resistance in the

APD. Typically, the APD is connected in series with an external resistor and the parasitic capacitance C_p can be from several pF up to tens of pF which results in a quenching time of > 100 ns as reported in [1], [2] and [3]. Many passive quenching circuits reported integrate the series connected external resistor directly with the APD that makes the parasitic capacitance much smaller to reduce the quenching time [4-6]. After the GM-APD has been quenched, the bias voltage slowly reset to its original voltage with a RC time constant determined by the parasitic capacitance and the series connected resistor. For most passive quenching circuits reported in the literature, such as in [7-11], the reset time is typically in the microsecond region. The reset time can be reduced to tens of nanoseconds, but it requires integration of the APD and quenching circuit together to decrease the parasitics [4-6]. In addition to the long quench and reset times, there is another disadvantage of using the passive quenching circuit. During the reset process, the bias voltage is above the breakdown voltage and the avalanche events can be triggered before the bias returns to the original voltage. When the counting rate is high, this will significantly affect the APDs performance such as detection efficiency, timing response, etc.

In summary, the passive quenching circuit is simple, low cost and occupies a small area that makes it useful in applications such as the fabrication of large APD arrays such as in [12-17]. However, it has the drawback of very slow quench and reset times (in the microsecond range) that limit the photon counting rate. Moreover, the ill-defined dead time leads to the possibility of avalanche retriggering and thus increased afterpulsing.

To overcome these drawbacks, active quench and reset circuits (AQRCs) are used. The AQRC quenches the avalanche current by lowering its bias voltage below the breakdown voltage after an avalanche event. The GM-APD is then kept in the OFF state for fixed period of time, called the hold-off time, before

resetting the device to its original bias voltage to await the next avalanche event. With the AQRC, the dead time of the GM-APD can be controlled to effectively reduce the afterpulsing phenomenon. Moreover, the stable well defined hold-off time (dead-time) make it possible to apply dead time correction to account for photons absorbed during hold-off time when an avalanche can't be triggered [18].

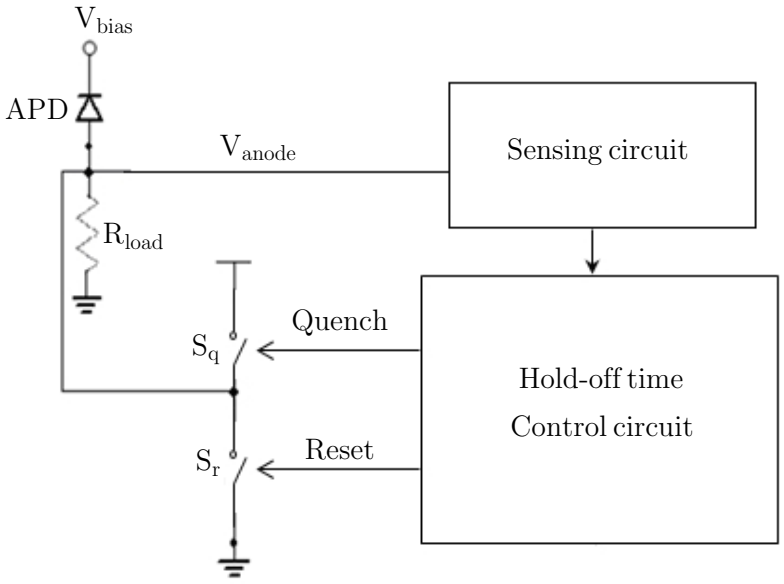


Figure 4.2: Typical structure of an active quench and reset circuit

Figure 4.2 shows the typical structure of an AQRC. The sensing circuit is used to sense the avalanche current in the GM-APD. This is typically a comparator or a simple inverter. The hold-off time control circuit receives a signal from the sensing circuit and generates pulses to control the quench and reset switches for holding the GM-APD in the OFF state for a period of time and then resetting it. The first AQRC was introduced in 1975 and was built using discrete components to enhance the performance of GM-APDs [19]. This circuit is designed with the aim of shortening the bias voltage reset time and providing a well defined hold-off time (dead time). In 1996, a compact discrete AQRC module was developed [20] which employed monostables to set the hold-off time. Progress in AQRCs made by the same research group led

to hybrid/integrated versions of the AQRC [21, 22], enabling the possibility of developing miniaturized detector modules.

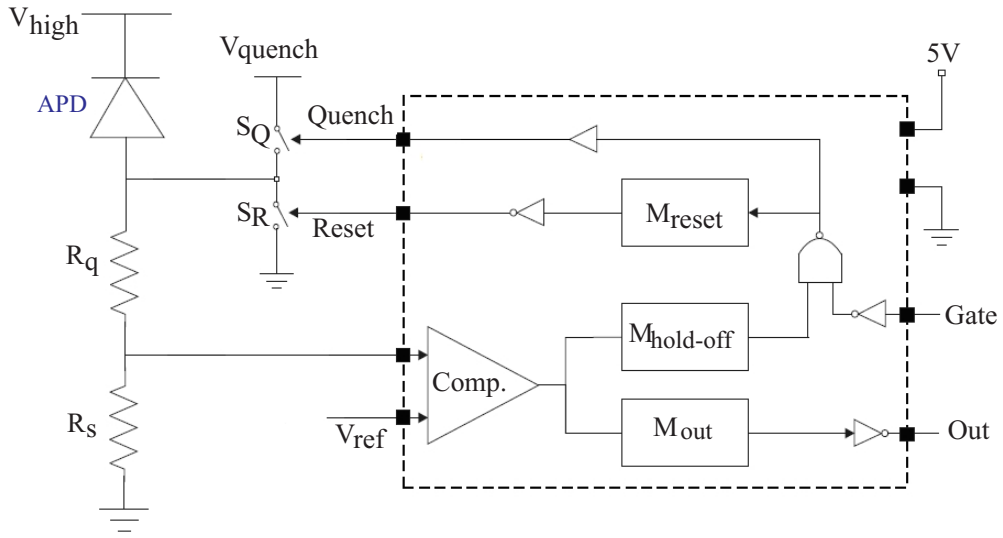


Figure 4.3: Diagram of AQRC in [21]

The AQRC [21] shown in Figure 4.3 consists of: 1) a comparator that senses the avalanche event; 2) monostables that generate the pulses for quenching and resetting the APD. As shown in Figure 4.3, the GM-APD is biased above its breakdown voltage. The excess bias voltage is about 10% of the breakdown voltage. When an avalanche event occurs a voltage is generated across the resistor Rs and sensed by a fast comparator. The comparator is used to provide an output pulse to external counters and to trigger a monostable multivibrator, $M_{hold-off}$.

The schematic of the monostable is shown in Figure 4.4. An RC delay circuit is used to generate a pulse for quenching or resetting the APD. With the monostable, the hold-off time can be adjusted by setting the value of the external resistor. As soon as the monostable is triggered, the QUENCH goes low, the quench switch (S_Q) is closed and this increases the anode voltage to Vquench. Vquench is higher than the excess bias voltage and thus brings the APD bias

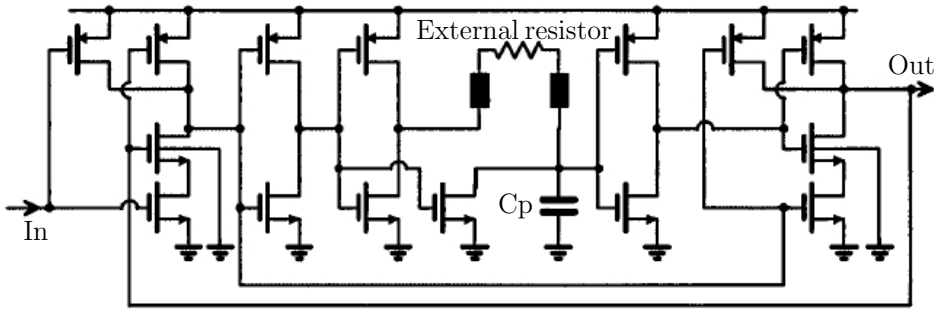


Figure 4.4: Schematic of a monostable

below its breakdown voltage. During the hold-off time period, the GM-APD remains quenched and no avalanche can be detected. When $M_{hold-off}$ resets (QUENCH goes high), the quench switch S_Q is opened and the monostable M_{reset} is triggered. The signal RESET goes high to close the switch S_R and this lowers the anode potential back to ground. After the transition of the M_{reset} monostable, the switch S_R is opened and the GM-APD is ready to detect another photon. This circuit achieved a dead-time of 40 ns between consecutive avalanche breakdowns (giving a maximum count-rate of 25 Mcounts/s) and shows the capability of providing a user-controllable hold-off time to reduce afterpulsing.

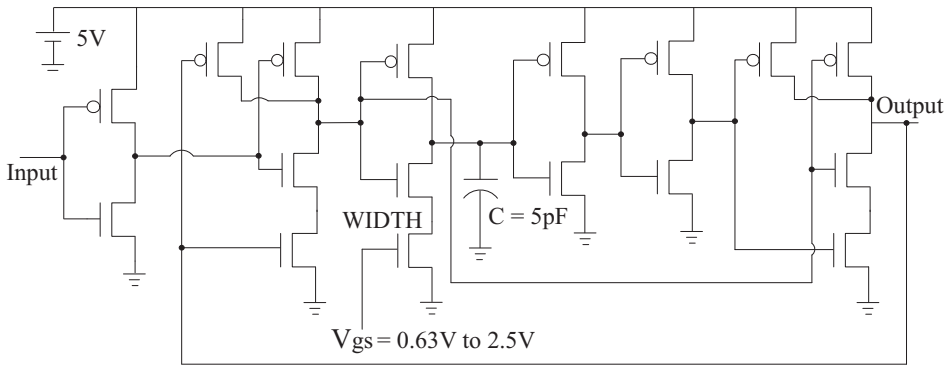


Figure 4.5: Modified monostable proposed in [23]

A modified monostable was proposed in [23], see Figure 4.5. In this circuit,

a WIDTH transistor is used to replace the resistor. The hold-off or reset monostable pulse widths can be adjusted by varying the input voltage of the WIDTH transistor. As reported in [23], this design is capable of setting the hold-off time between 4.6 μs and 4 ns by varying the input voltage between 0.635 V and 2.5 V. This makes it easier to adjust the hold-off time for an AQRC. Up to now, the use of monostables remains the most popular method for setting the hold-off time [24-27] with circuits still using this technique reported recently [28].

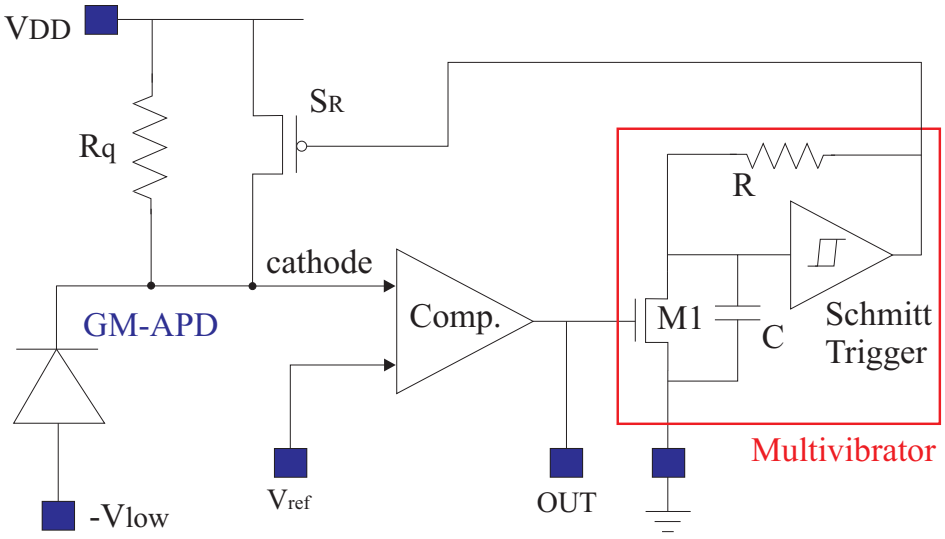


Figure 4.6: Schematic of AQRC reported in [29] and [30].

Figure 4.6 shows another AQRC reported by Rochas *et al* in which the GM-APD and the control circuit are integrated together. This circuit was implemented in both discrete and integrated formats reported in [29] and [30] respectively. Similar to the design in [21], this circuit uses a comparator to sense the avalanche events and a monostable multivibrator for controlling the hold-off time. Thanks to the monolithic integration, the parasitics of this circuit are greatly reduced and a dead-time of just 10 ns between adjacent events was achieved that leads to a very high maximum count-rate of 100 Mcounts/s. Some other designs that integrate the quenching circuit and the APD together

can be seen in [31, 32] in which maximum count-rates of excess 150 Mcounts/s are achieved. The monolithic integration gives a high maximum count-rate but it makes it difficult for users to interchange the sensor.

One drawback that remains in the AQRCs described is the hold-off time setting with monostables. With monostables, the adjustment of the hold-off time is non-linear and it's difficult to select the optimal hold-off time digitally or via additional signal processing circuitry. To overcome this drawback, the delay line technique can be used to set the hold-off time in AQRC. Figure 4.7 shows the schematic of an AQRC using a delay line technique to set the hold-off time proposed in [33].

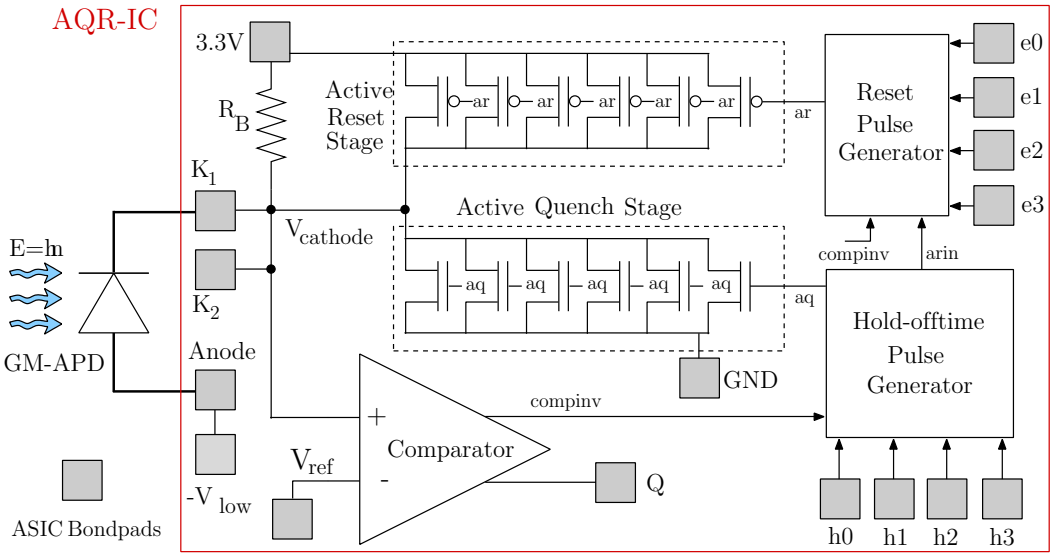


Figure 4.7: Diagram of AQRC in [33]

In this circuit, a comparator is used to sense the avalanche event in the GM-APD and send signals to a pulse generator. The pulse generators are based on a silicon delay line with additional combinational logic that is used to create pre-defined pulse-widths for setting the hold-off time.

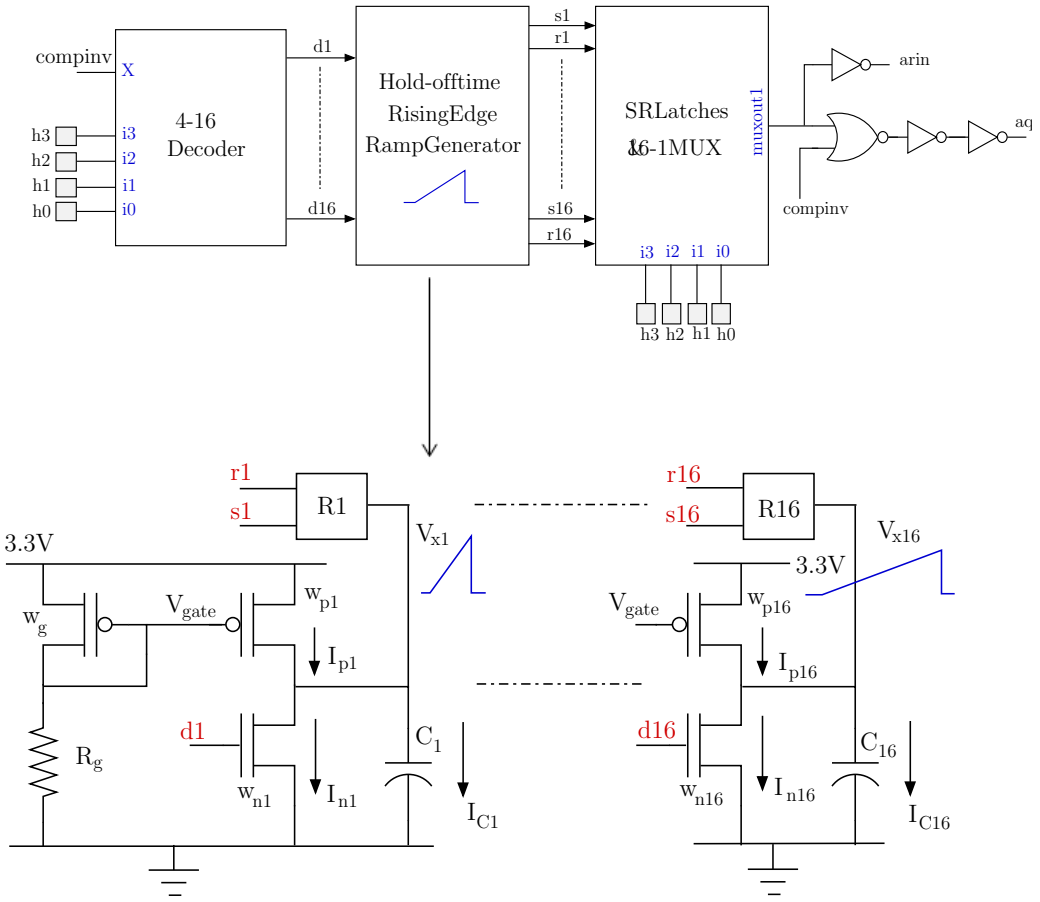


Figure 4.8: Diagram of delay line technique in [33]

A diagram of the delay line technique used in [33] is shown in Figure 4.8. The rising-edge ramp generator in the figure is a current source connected through a capacitor to ground. A current source/current mirror configuration is used to create the rising ramp voltage V_{x1} when the gate voltage, d1, of the NMOS transistor W_{n1} is set low. 16 discrete current mirrors were used with each having an individual capacitor to generate 16 predefined delays. The delay can be selected using a 4-16 decoder via inputs h3 to h0. The outputs of the 16 SR-latches are connected to a 16-1 multiplexor and the same inputs h3 to h0 selected for the decoder are used to determine the SR-latch output sent to the next stage. This output is then connected to a logic stage to create one of

h3 h2 h1 h0	Hold-off time	h3 h2 h1 h0	Hold-off time
0000	9.5 ns	1000	276 ns
0001	17.5 ns	1001	317 ns
0010	42.5 ns	1010	363 ns
0011	71 ns	1011	375 ns
0100	101 ns	1100	444 ns
0101	142 ns	1101	486 ns
0110	187 ns	1110	588 ns
0111	224 ns	1111	683 ns

Table 4.1: Available hold-off times with AQRC in [33]

the selected 16 predefined high hold-off time pulse widths between 5 and 660 ns, ultimately determined by the size of the capacitors C1-C16 and the current flowing through them. After the hold-off time is completed, the active quench stage is deactivated (parallel NMOS transistors of Figure 4.7) and the parallel PMOS transistors are turned on using a logic low pulse. This is provided by a similar pulse generator operating in 16 discrete steps between 2.5 and 100 ns.

4.2 High-resolution hold-off time control circuit

As discussed in Section 4.1, the adjustment of the hold-off time in previously reported quenching circuits are either non-linear or complicated. To overcome the drawbacks, a simplified high-resolution hold-off time circuit is designed.

4.2.1 Circuit Design

Figure 4.9 shows the block diagram of the proposed circuit. The non-inverting input of the comparator is connected to the anode of the APD, which is biased at the voltage between the avalanche breakdown voltage, V_{break}, and $(V_{break} + V_{dd})$. The comparator is used to sense the avalanche current at the

anode of the APD which also has an inverse output, $\overline{compo}$, that is connected to an external bond pad for readout. One PMOS and one NMOS transistor are used as the switches for quenching and resetting the APD. An external clock signal provides the counting clock during the hold-off period and a counter is used to control the hold-off time.

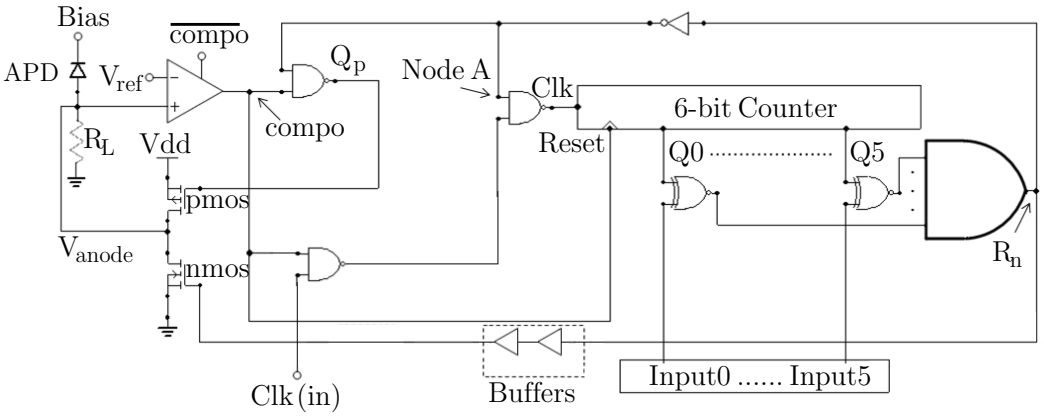


Figure 4.9: Block diagram of high-resolution hold-off time control circuit

Initially, when there is no avalanche current, compo is low, the external clock is blocked, the 6-bit counter is reset to 0 ("000000") and both PMOS and NMOS transistors are turned off. When an avalanche event happens in the APD, current flows through the load resistor, R_L, and the voltage increases at the anode of APD. The comparator senses the voltage rise and compo goes from low to high. Qp goes low to turn on the PMOS transistor and the anode of the APD is connected to V_{dd} for quenching. Meanwhile, the counter receives clocks from the external clock, Clk(in).

The counter used here is a 6-bit synchronous binary counter which consists of 6 J-K flip-flops with the clock signal connected to the clock input of every flip-flop with the J and K inputs tied together; see Figure 4.10. The J and K inputs of the first flip-flop are connected to V_{dd}; the J and K inputs of the other flip-flops are connected to the output, Q, of each front end. When the

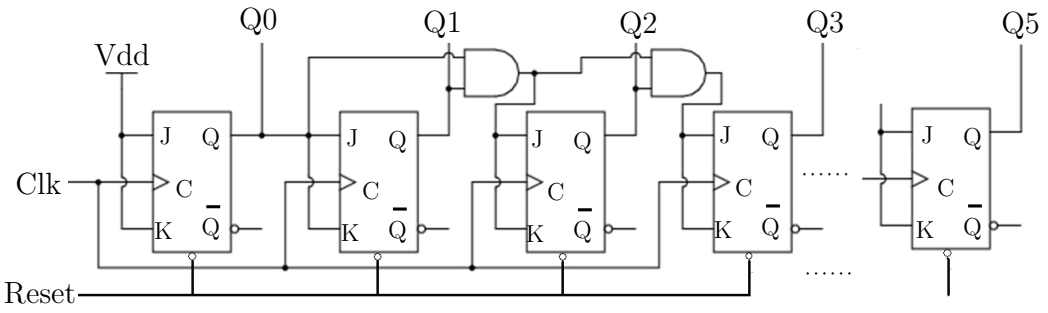


Figure 4.10: 6-bit synchronous binary counter

reset signal compo is high, the counter receives clocks from Clk(in) and counts upwards from 0 ("000000") to 63 ("111111"). Each output of the counter is connected to one input of an XNOR gate. The other input of the XNOR is connected to an external input (controlled by the end user). When the output of the counter is equal to the external inputs, all the outputs of the XNOR gates go to logic "1" (high). Then Rn goes high which makes Qp go high to stop the hold-off process and turn on the NMOS transistor to reset the APD (two buffers are used here to make sure the reset process starts after the hold-off process is finished). At this time, the Node A' goes low to stop the clock to the counter and the counter is stopped. This then makes Rn remain high for resetting. When the anode of the APD is reset back to ground, compo is low, the Clk(in) is blocked again and the counter is reset to 0 ("000000"). Now the outputs of the counter do not match the external inputs, Rn goes low and the NMOS transistor is turned off to complete the reset process. The APD is then ready to detect the next photon. By setting the external inputs, the counting number can be determined and the hold-off time can be altered. The step resolution is decided by the counting speed, which depends on the period of the external clock Clk(in).

4.2.2 Layout and simulations

The layout of the proposed circuit was completed using L-Foundry 0.15 μm CMOS process [34] and is illustrated in Figure 4.11. The overall chip dimension is about 700 μm $\times$ 700 μm which is mostly occupied by the bond pads and the I/O standard cells. The dimensions of the IC core (without bond pads) are 95 μm $\times$ 55 μm. All the simulations reported are post-layout simulations.

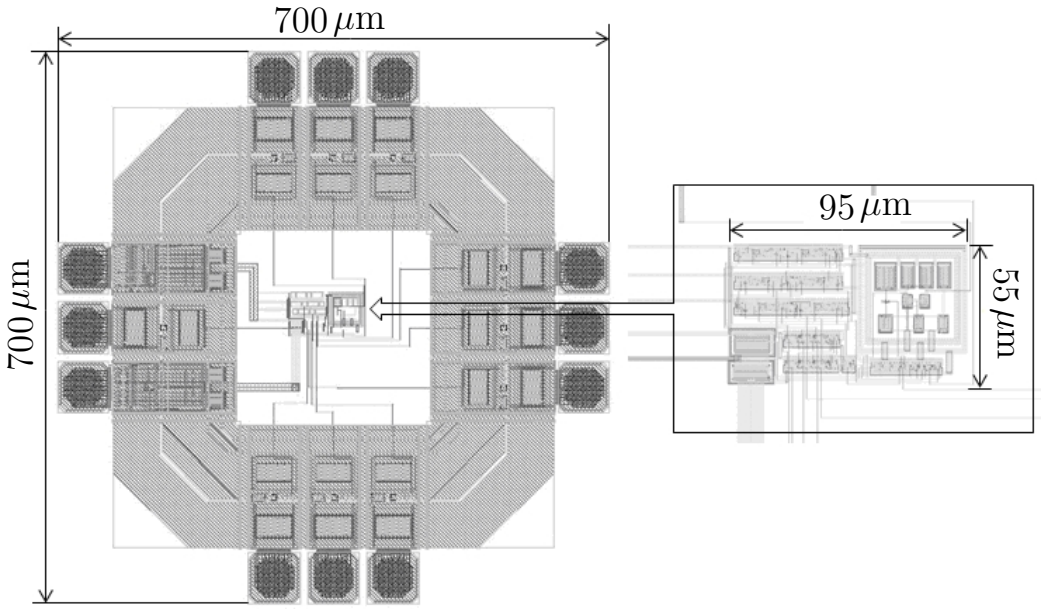


Figure 4.11: Layout of the proposed circuit

For circuit simulations, a linear model of the GM-APD is used, as illustrated in Figure 4.12 [20]. V_b is a voltage source that represents the breakdown voltage, which is set at 27 V. The bias voltage is set to 30 V. R_d is the internal resistance, which is set to 250 Ω. C_d is the junction capacitance, which is set to 2 pF. The simulations were run in the Cadence design environment with V_{dd}=3.3 V.

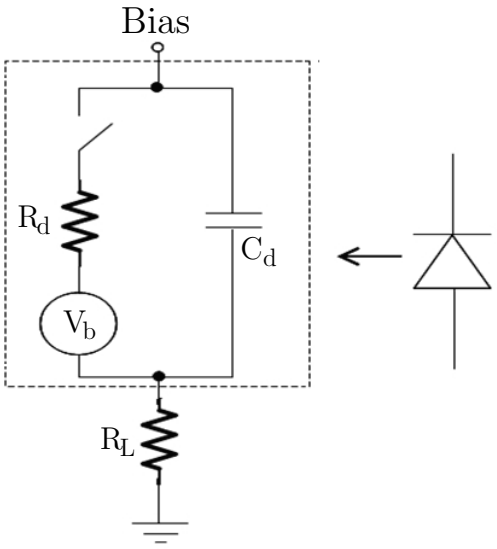


Figure 4.12: Simulation model of the GM-APD

Figure 4.13 shows an example of the circuit operation when the external inputs are set to 30 ("011110"). The period of the external clocks is set to 2 ns. As can be seen from the figure, at 5 ns when a photon absorbed, the comparator senses the voltage change from the anode of the APD and Qp goes low for quenching. Meanwhile, the external clock is not blocked and provides the clock pulses to the counter. The 6-bit counter counts upwards from 0 ("000000") at a rate set by the external clocks (here the period is set to 2 ns). When the outputs of the counter match the external inputs, which in this case are set to 30 ("011110"), Rn goes high which makes Qp go high to stop the hold-off process and turn on the NMOS transistor to reset the APD. At this time, the clocks to the counter are blocked and the counter is stopped thereby keeping Rn high for resetting the APD. When the anode of the APD is set back to ground, the counter is reset to 0 ("000000") and Rn goes low to stop the reset process. In this way, with the external inputs of 30 ("011110"), the hold-off time is set to around 60 ns.

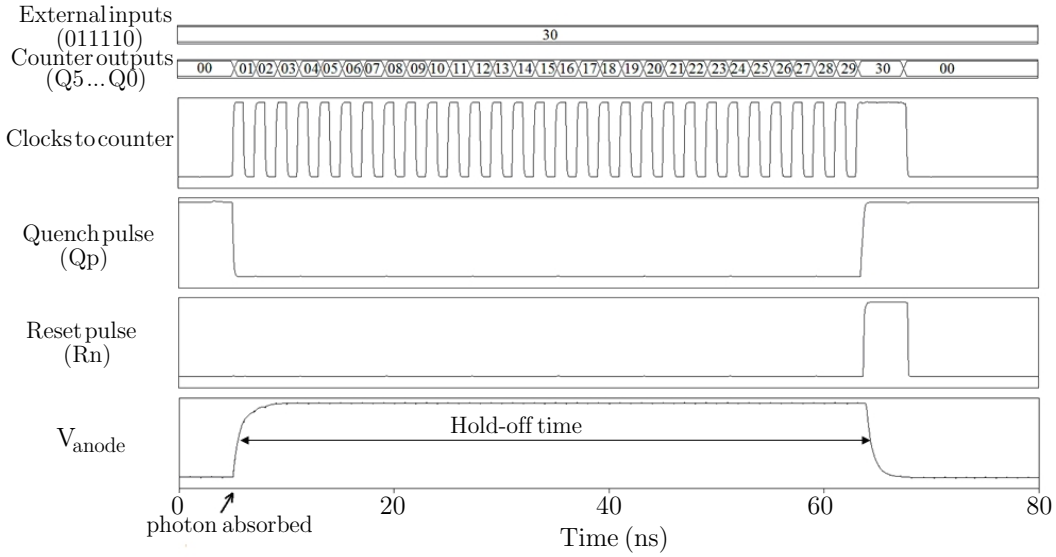


Figure 4.13: Example of the circuit operation when the external inputs are set to 30 ("011110")

Figure 4.14 shows the simulation results of varying the external input codes versus the resultant hold-off time. It shows when the input code increases from 1 ("000001") to 63 ("111111") the hold-off time linearly increases to more than 120 ns with a step resolution of about 2 ns.

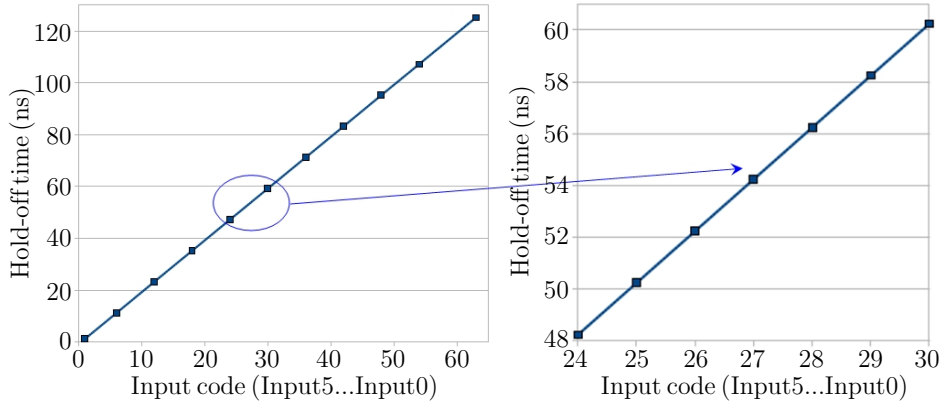


Figure 4.14: Hold-off times versus external input codes when the step resolution is set to 2 ns

Figure 4.15 shows the setting range of the hold-off time for different step resolutions. As can be seen from the figure, when the step resolution is varied

from 2 ns to 20 ns, the range of the hold-off can be altered by more than a microsecond.

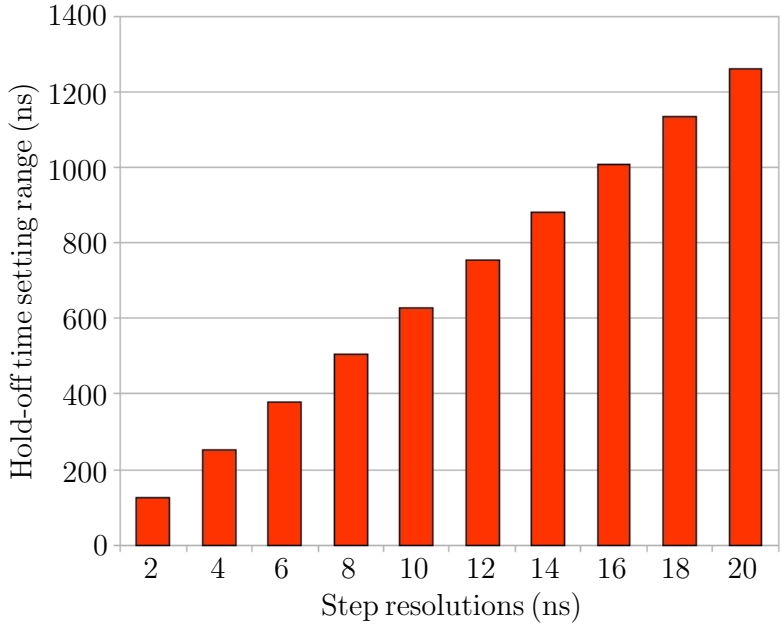


Figure 4.15: Setting range of the hold-off time for different step resolutions

In summary, this section has introduced a high-resolution hold-off time control circuit for GM-APDs. Circuit design, layout and simulations were presented. With this circuit, the hold-off time can be linearly varied from several nanoseconds to microseconds with a user-set resolution. The optimal 'afterpulse-free' hold-off time for any GM-APD can be easily set through the circuit's digital inputs or via an additional signal processing circuit. The layout of this circuit was completed using a conventional CMOS process, resulting in a small layout area that makes it suitable for integration with arrays of GM-APDs. The circuit also incorporates a facility designed to reset the APD automatically at the end of the hold-off time that further simplifies the control for the end-user. However, the use of the external clock increases the user control complexity. In the next section the external clock is replaced by a ring-oscillator. With that configuration, the clock pulses to the counter can be generated locally and this simplifies the end-user control. [35].

4.3 Improved approach and ASIC development of the active quench and reset circuit

To simplify the user control of the design described in Section 4.2, an improved circuit was developed. In this new approach, a ring-oscillator replaces the external clock to simplify the end-user control. This circuit was fabricated using Austria Microsystems (AMS) 0.35 μm CMOS process and tested with a planar silicon GM-APD having a 27 V breakdown voltage.

4.3.1 Circuit description

Figure 4.16 shows the block diagram of the proposed circuit. The inverting input of the comparator is connected to the cathode of the APD which is biased at a voltage determined by V_{dd} and -V_{low}. A comparator is used to sense the avalanche current at the cathode of the APD. One PMOS and one NMOS transistor are used as the switches for quenching and resetting the APD. A ring-oscillator is used to generate clock pulses during the hold-off period and a counter is used to count the clock pulses to adjust the hold-off time.

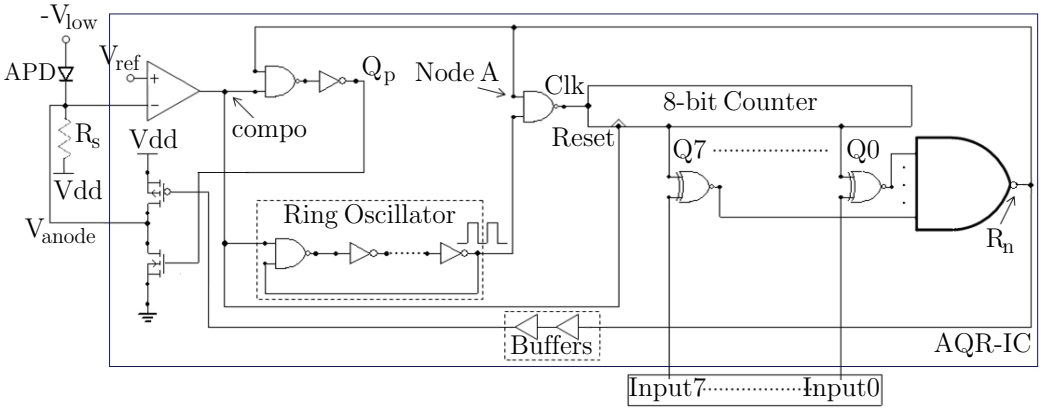


Figure 4.16: Block diagram of the new approach

When there is no avalanche current, compo is low, the ring-oscillator is inactive, the 8-bit counter is reset to 0 ("00000000") and the PMOS and NMOS

transistors are turned off. When an avalanche event occurs, current flows through the sensing resistor Rs and a voltage drop is observed at the cathode of the APD. The comparator senses the voltage drop and compo goes from low to high. Qp goes high to turn on the NMOS transistor and the cathode of the APD is connected to GND for quenching. Meanwhile, the ring oscillator is active and provides the clock to the counter. The counter used is an 8-bit synchronous binary counter which has the same architecture as that was described in Section 4.2.1. When the reset signal compo is high, the counter receives clocks from the ring-oscillator and counts upwards from 0 ("00000000") to 255 ("11111111"). Each output of the counter is connected to one input of an XNOR gate. The other input of the XNOR is connected to an external input (controlled by end user). When the outputs of the counter equal the external inputs, all the outputs of the XNOR gates go to logic "1" (high). Then Rn goes low which makes Qp go low to stop the hold-off process and turn on the PMOS transistor thereby resetting the APD (buffers are used here to make sure the reset process starts after the hold-off process is finished). At this time, Node A goes low to block the clock from the ring-oscillator to the counter and the counter is stopped. This makes Rn remain low for resetting. When the cathode of the APD is reset back to V_{dd}, compo is low, the ring-oscillator is inactive and the counter is reset to 0 ("00000000"). Now the outputs of the counter do not match the external inputs, Rn goes high and the PMOS transistor is turned off to complete the reset process. The APD is then ready to detect the next photon. By setting the external inputs, the counting number can be determined and the hold-off time can be altered. The hold-off time setting step is determined by the counting speed that depends on the number of the stages of the ring-oscillator. A 41-stage ring-oscillator occupying approximately 25% of the IC core is used here to give a stable setting step of 6.5 ns for the hold-off time.

4.3.2 ASIC development and measurements

The circuit layout was designed with 0.35 μm AMS CMOS process [36] and submitted to Europractice-IC [37] for fabrication. Figure 4.17 shows a photograph of the fabricated chip; the overall chip dimensions are 1.7 mm $\times$ 1.4 mm which mostly occupied by the bond pads and decoupling capacitors. The dimensions of the IC core are 260 μm $\times$ 150 μm.

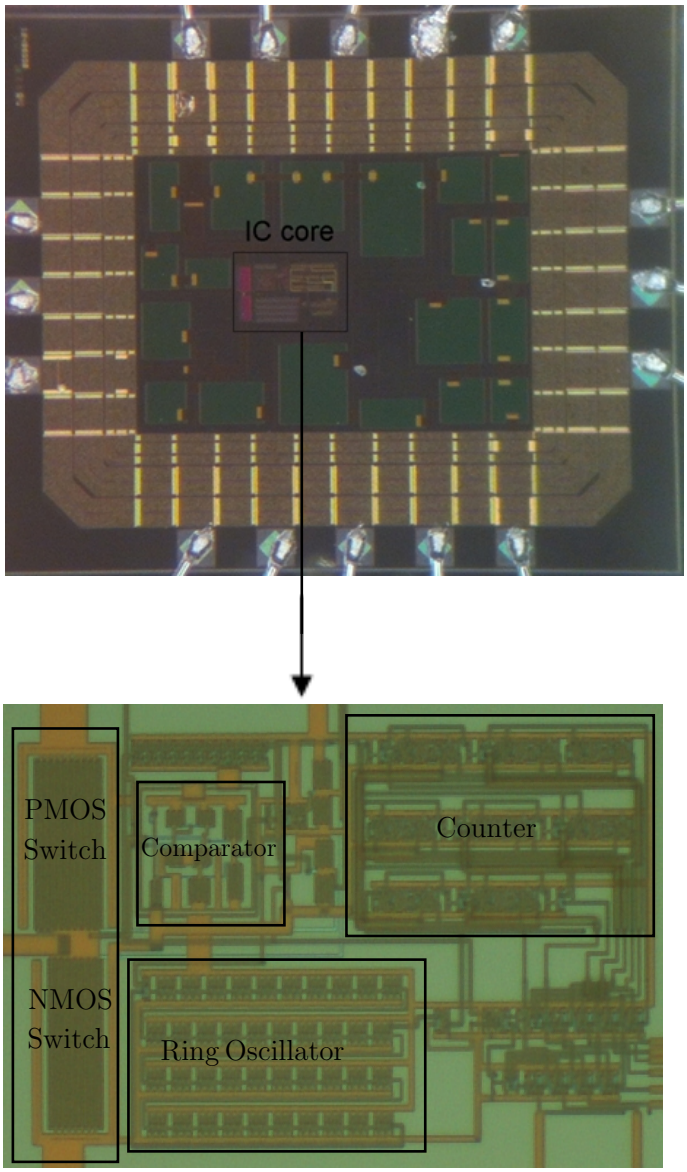


Figure 4.17: Photograph of the fabricated chip

For the measurements, the AQR-IC is connected to a 20 μm diameter circular GM-APD developed by the Photodetection and Imaging Group at University College Cork [38-40]. The fabricated PCB can be seen in Figures 4.18 and 4.19.

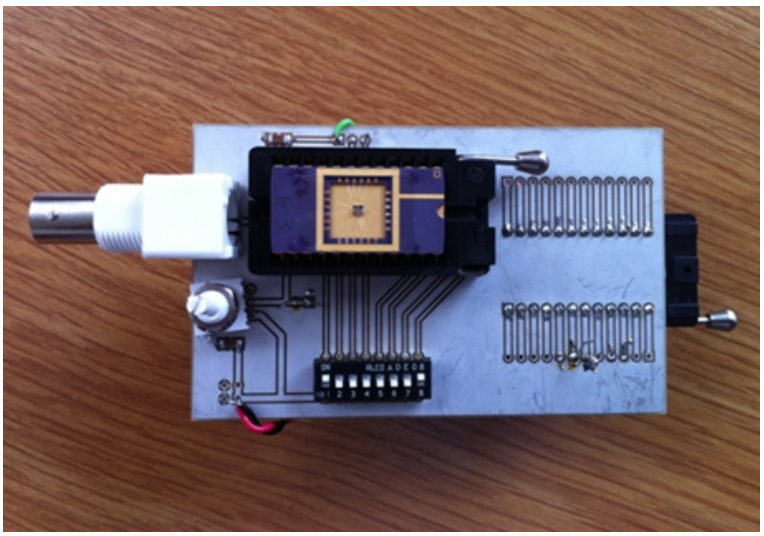


Figure 4.18: Top-side of the test PCB (holds the fabricated chip)

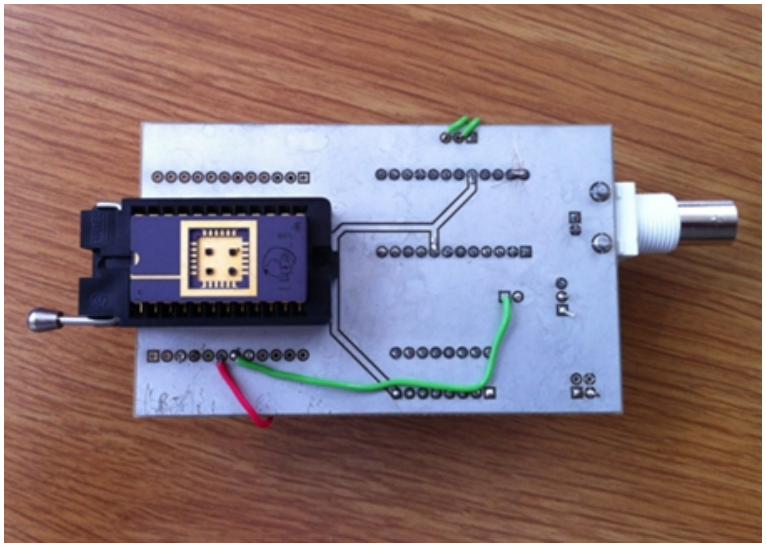


Figure 4.19: Bottom-side of the test PCB (holds the tested APDs)

In Figure 4.20, the experimental setup for the hold-off time test is demonstrated. A He-Ne laser source operating at 632.8 nm was used as the light source that was directed to the GM-APD using an integrating sphere. An external power supply was used to provide -V_{low} and V_{dd} for biasing the GM-APD and powering the AQR-IC. The APD is biased at 30 V (-V_{low} = -26.7 V, V_{dd} = 3.3 V) which is around 3 V in excess of the breakdown voltage. The hold-off time is controlled by the 8 way switch on the PCB. An oscilloscope was used to observe the quench pulse (Qp) and the voltage at the cathode ($V_{cathode}$) of the APD.

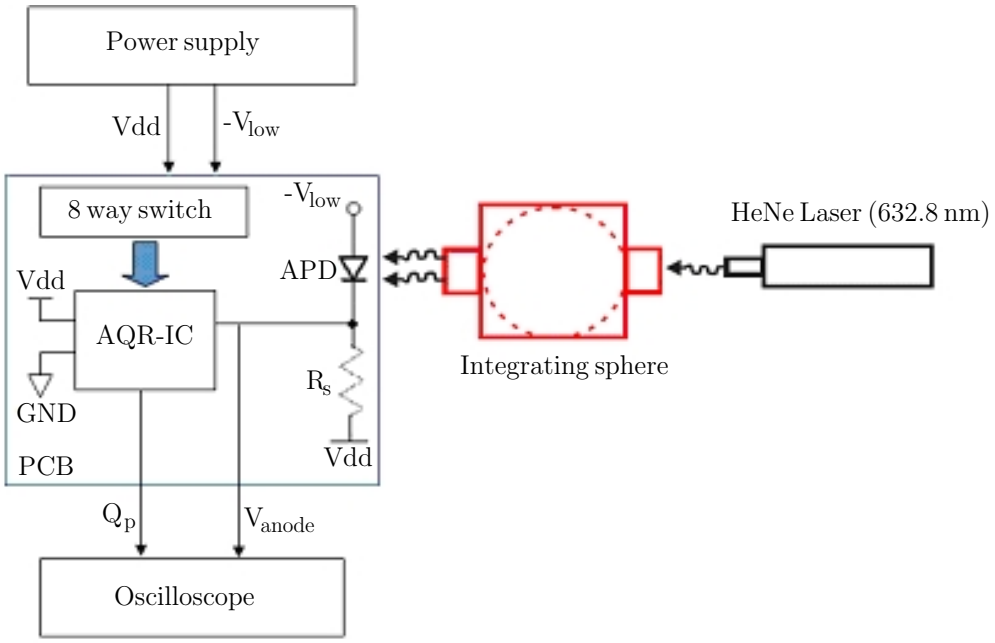


Figure 4.20: Experimental setup for testing the AQR-IC

In Figure 4.21(a), the oscilloscope traces of the quenching pulse (Qp) and the cathode voltage ($V_{cathode}$) are demonstrated with the hold-off time kept at 190 ns by setting Input7 to Input0 to 00011101. Figure 4.21(b) and Figure 4.21(c) show the cathode voltage ($V_{cathode}$) of the APD with the hold-off times set to 326 ns and 1.18 μs. The results demonstrate the accurate control of the hold-off time using external switches.

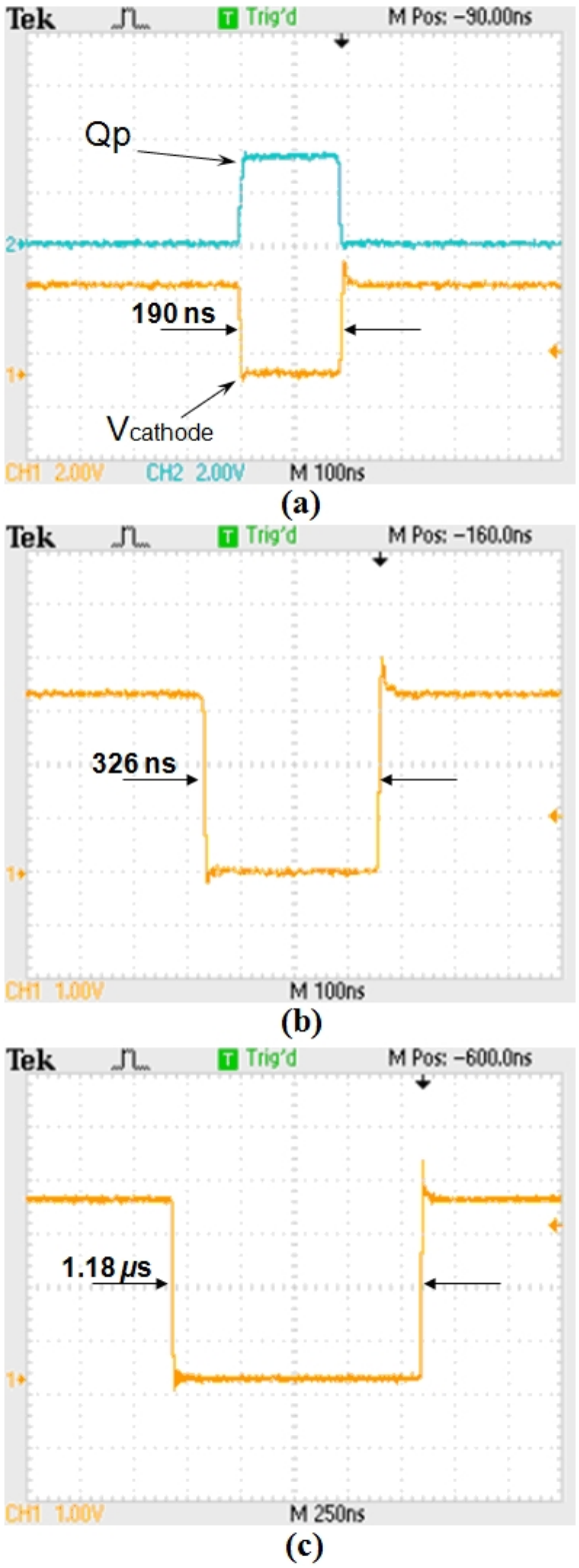


Figure 4.21: a) Quenching pulse (Qp) and APD's cathode voltage ($V_{cathode}$) with a hold-off time of 190 ns (00011101), (b) $V_{cathode}$ with hold-off time = 326 ns (00110010) and (c) $V_{cathode}$ with hold-off time = 1.18 μs (10110101).

Figure 4.22 shows the results of varying the external input codes versus the resultant hold-off time. It shows when the input code increases from 1 ("00000001") to 255 ("11111111") the hold-off time linearly increases from several nanoseconds to more than 1.6 μs with a setting step of about 6.5 ns.

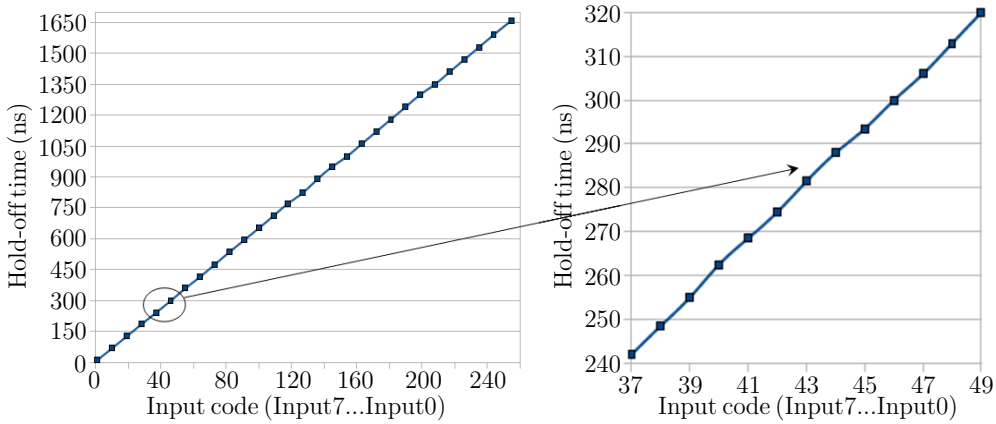


Figure 4.22: External input codes versus hold-off time

In Figure 4.23, a plot of $V_{cathode}$ is shown with Input7 to Input0 set to "00000001" when saturating light is directed at the APD; this demonstrates the minimum dead-time between adjacent avalanche events in the GM-APD. It can be seen that the minimum dead-time is 28.4 ns corresponding to a saturated count-rate of 35.2 Mcounts/s with this AQR-IC.[41, 42].

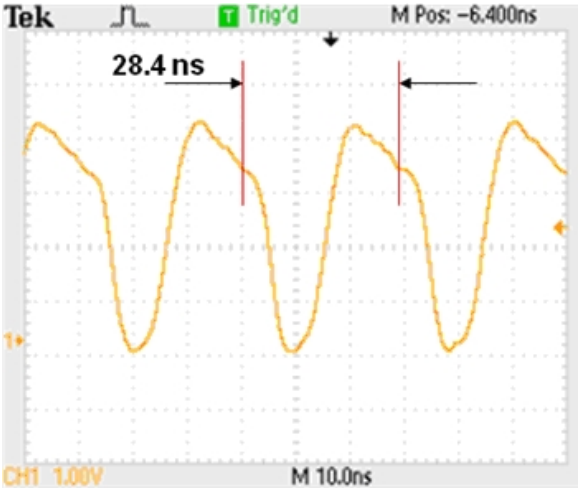


Figure 4.23: Plot of $V_{cathode}$ for saturated count-rate

4.4 Conclusion

This chapter described the design and development of an active quench and reset circuit with high-resolution hold-off time control logic. The circuit operation was explained, layout design and simulations were presented. The integrated circuit was fabricated using a conventional CMOS process and tested with a GM-APD.

Results show that this design is capable of linear changes to the hold-off time from several nanoseconds to microseconds with a reasonable step of 6.5 ns that allows setting of the optimal 'afterpulse-free' hold-off time for any GM-APD through digital inputs or additional signal processing circuitry. A minimum dead time of 28.4 ns was observed from the measurement, demonstrating a saturated photon-counting of 35.2 Mcounts/s with this AQRC.

A comparison of existing active quench and reset circuits and the circuit designed in this work is shown in Table 4.2. Monostables were used by many research groups to select the hold-off time and reset pulse. The main disadvantage of using monostables is the difficulty in accurately adjusting the hold-off time. The monostable adjusts the hold-off time by setting the value of an external resistor or varying the input voltage of a WIDTH transistor that leads to a non-linear change in the hold-off time, thereby making it difficult to select the optimal hold-off time digitally. Delay line techniques provide a more advanced way to set the hold-off time. The digitally controlled hold-off time makes it easier to interface with other signal processing circuitry. However, there are limited hold-off times available with the circuit and an increased chip areas needed if additional hold-off times are required. The circuit designed in this work allows digital control of the hold-off time while maintaining a comparable maximum count-rate to previous designs (as presented in [28,29], monolithic

integration of the APD and the quench circuit would produce a much higher saturated count-rate). Moreover, it eliminates the requirement of using an additional monostable or pulse generator to reset the detector, thus simplifying the circuit.

	[2]	[21, 22]	[31, 32]	[33]	This work
Integrated	No	Yes	Yes	Yes	Yes
Connection to the APD	not integrated	not integrated	Monolithic integrated	PCB	PCB
Min. Deadtime	39 ns	50 ns	5.4 ns	40 ns	28.4 ns
Max. Count-rate (Mcounts/s)	25.6	20	185	25	35.2
Hold-off time control logic type	Monostable	Monostable	Monostable	Delay line	Novel control logic
Hold-off time adjustment	External resistor	External resistor	Fixed	Digitally	Digitally
Additional control needed for resetting APD	Yes	Yes	Yes	Yes	No

Table 4.2: Comparison of existing active quench and reset circuits

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Chapter 5

Bias and gain control circuit for avalanche photodiodes

It was shown in Chapter 2 that the APD's multiplication gain is needs to be accurately controlled under varying environmental conditions for some APD-based applications. To accomplish this, a novel bias and gain control circuit is developed in this chapter for avalanche photodiodes (APDs) biased in linear mode. In the first section, some gain control and stabilization circuits for APDs are reviewed and the advantages and disadvantages for each circuit are discussed. Next, a bias and gain control circuit is designed and developed. This circuit is based on the idea of using two matched APDs to set and stabilize the gain which operates without the need for external temperature sensing and control electronics thereby lowering the system cost and complexity. With discrete components, a printed circuit board (PCB) module of the proposed circuit was fabricated and measured using packaged APDs. Results show that the circuit is capable of providing bias voltages up to 40 V for the APDs, precisely setting its gain and compensating for the changes in the temperature to maintain a stable gain.

5.1 Introduction to gain control circuit for avalanche photodiodes

In Chapter 2, it was seen that the APD gain is affected by many factors including reverse bias voltage and temperature. A number of reports have shown that APDs have significant temperature-dependent gain [1-5] which leads to a problem for the stability of APD-based systems. Therefore, it is necessary to precisely set the intended APD gain and maintain that gain for long periods of time under varying environmental conditions to ensure accurate performance in some APD-based applications such as those in nuclear medicine and astronomy [6-9].

Much research has focused on using temperature stablilization systems (thermal chambers or cooling systems) to provide a stable low APD temperature for APD gain stabilization as shown in [10-14]. However these solutions are usually very expensive in terms of initial and maintenance costs, thus limiting their usefulness to laboratory experiments. Figure 5.1 shows a more advanced temperature control system used for APD gain stabilization [15, 16]. This system uses a high frequency switching power regulator and a temperature control system to guarantee a low and extremely constant temperature in an APD. A temperature sensor in the thermal block is used to detect any variation of the temperature. The system receives feedback from the temperature sensor, compares it with an external reference signal and sends a control signal to the "Peltier cell" through the regulator to adjust the temperature of the APD. However, the use of the thermal block in this system makes it bulky, expensive and power intensive. Moreover, this system does not compensate for drift in the supply voltage that increases the inaccuracy of the APD gain stabilization.

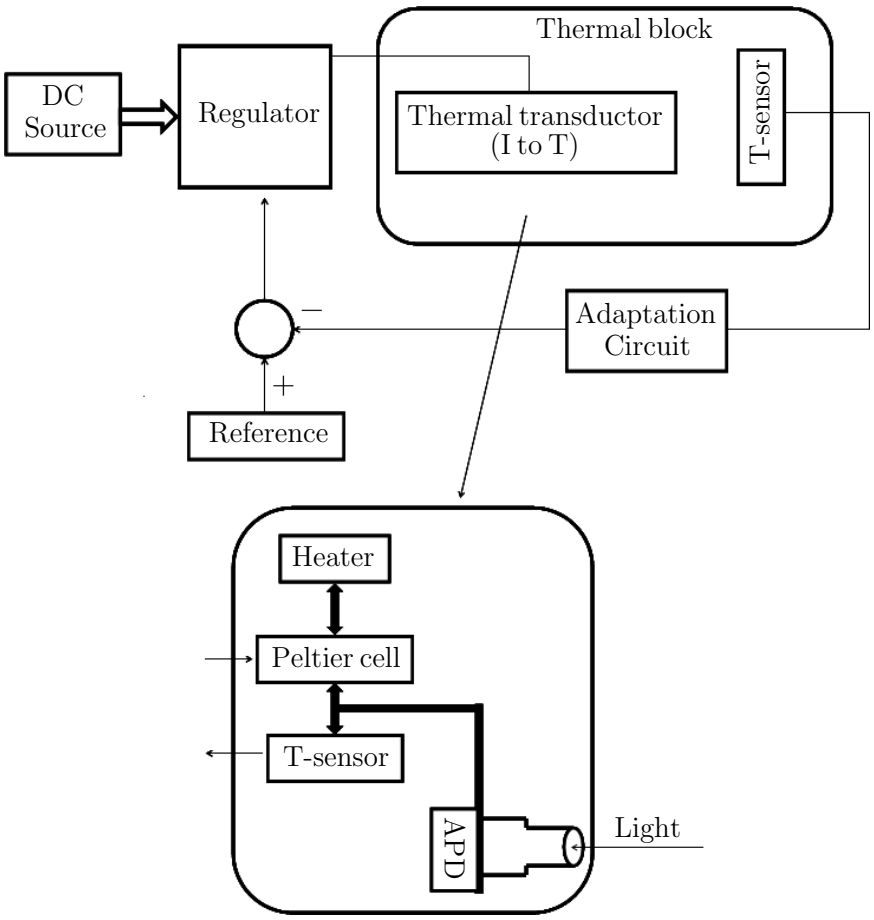


Figure 5.1: Temperature control system in [15, 16].

A CPU-based gain stablilization system is proposed [8, 17] as shown in Figure 5.2. This design also uses a temperature sensor to detect the temperature variation in the APD. Unlike the system described in [15, 16], this system adjusts the APD's bias voltage instead of its temperature according to the feedback from the temperature sensor to keep the APD gain stable under moderate temperature variations. Results show that the circuit operates well over a temperature variation of 20^oC. The active control of the APD gain by varying its bias as a function of the temperature has been used in a number of APD-based systems to operate the APDs independent of the temperature. Those designs can be seen in [7, 9, 18-20]. However, this method suffers from several drawbacks. The required bias voltages for the APD at different temperatures

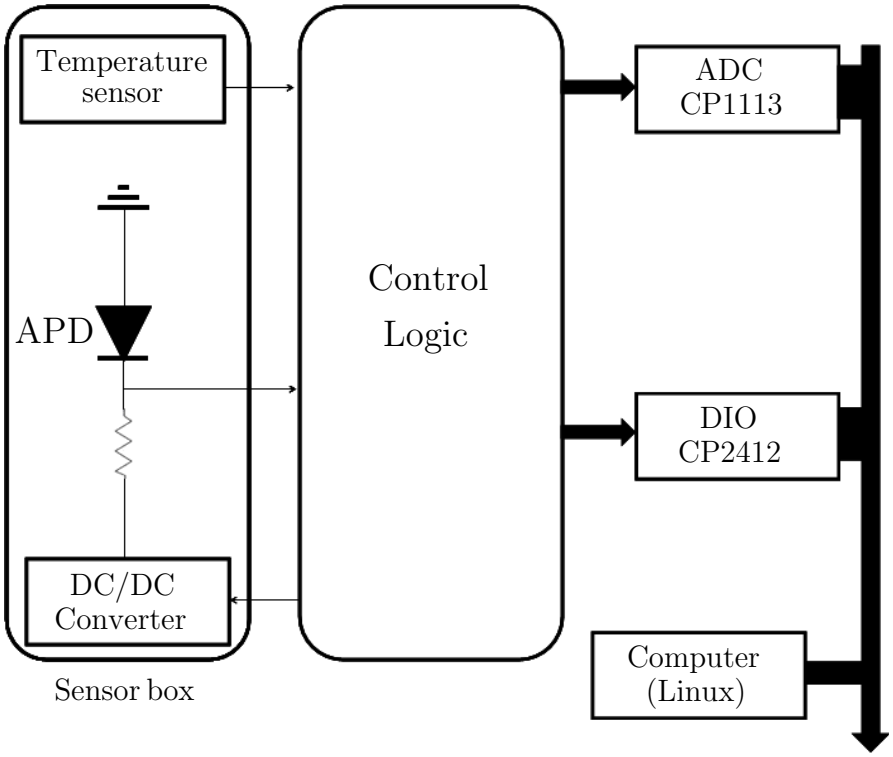


Figure 5.2: Gain stabilisation system in [8, 17].

need to be measured in advance by the end user thus increasing the control complexity. Moreover, the temperature compensation elements suffer from temperature coefficient mismatches that further limit their operation accuracy.

An alternative control solution to set the APD gain is to use two matched APDs where one is biased at unitary gain (unmultiplied) and the other one is biased at a high gain (multiplied) [21, 22]; see Figure 5.3. Since the two matched APDs have near identical performance, the gain is simply the ratio of the currents flowing in the two APDs. In principle this technique can be used to set the gain and modify the bias voltage to compensate for the changes in the environment without the need for external temperature sensing and control electronics.

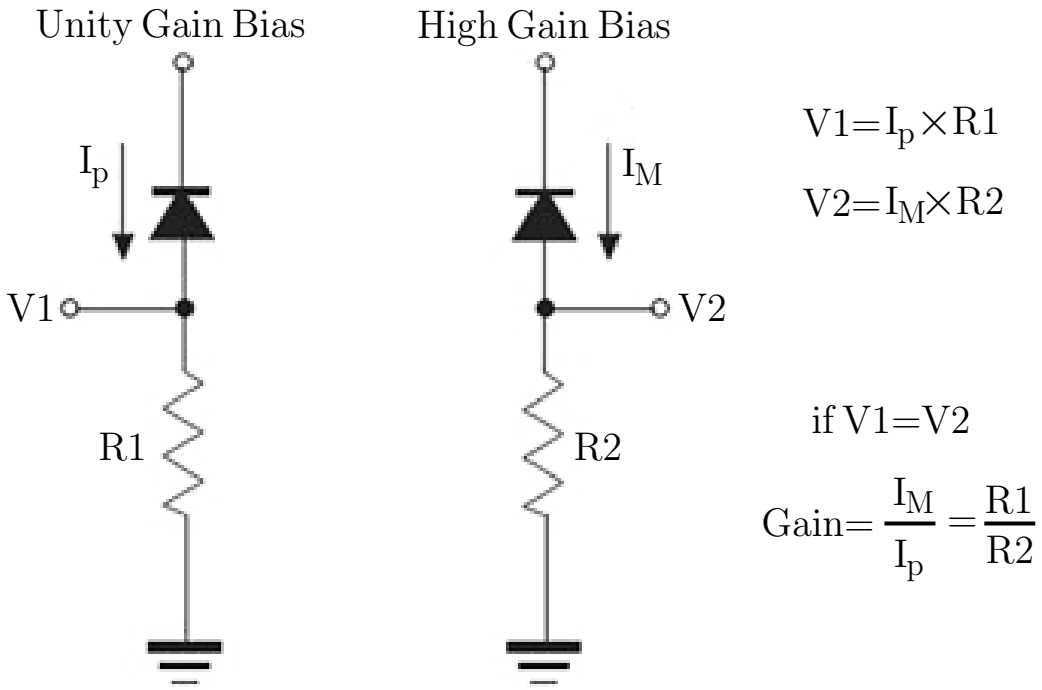


Figure 5.3: APD bias arrangement using two matched devices.

Based on this idea, many circuits have been designed. Figure 5.4 shows one of the APD gain control and stablilization circuits using this idea developed by the Photodetection and Imaging Group at University College Cork [22, 23].

In the circuit, APD1 is biased at unity gain which is independent of room temperature variations. APD2 is biased at high gain by an opto-coupler circuit which consists of an LED irradiating, an isolated feedback and an output PIN photodiode. A comparator is used to receive the feedback from the two matched APDs and send a signal to the FPGA for further processing. The FPGA receives the signal from the comparator and adjusts the high gain bias circuit through a digital-to-analogue converter to maintain V1 equal to V2 and thus maintain a stable multiplication gain in the APD2. This design operates without the need for external temperature sensing and control electronics. However, the control logic in this design is complicated and its bias solution

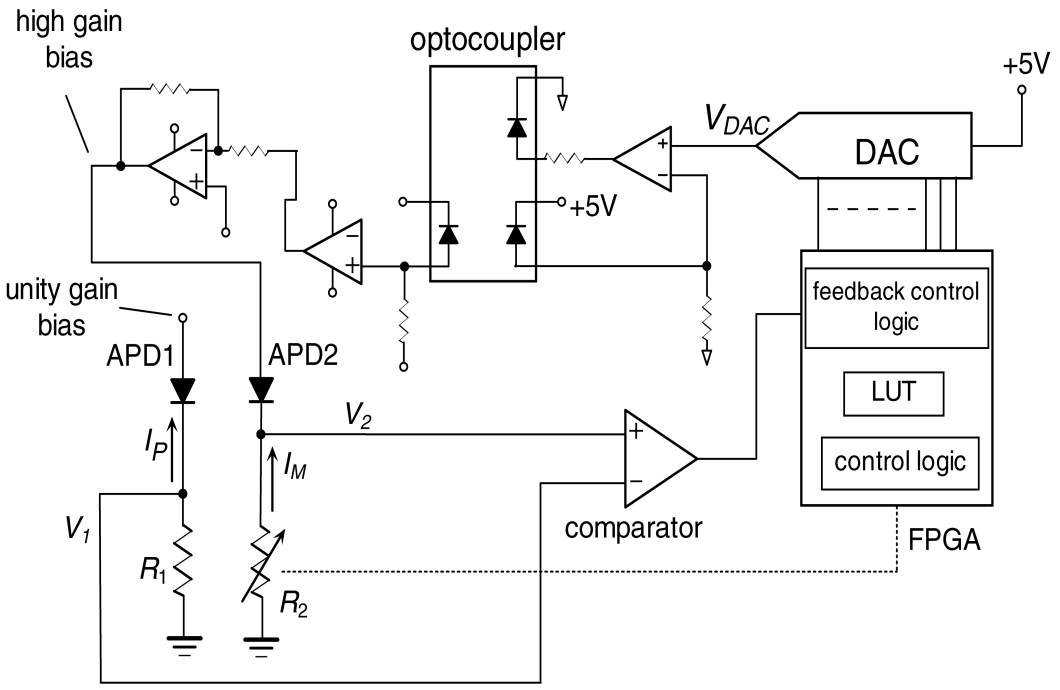


Figure 5.4: APD gain control and stablilization circuits in [22].

is not compact. As will be seen in the next section, a bias control and gain stabilization circuit is designed which has the advantages of using the matched APDs while providing a simpler and more compact solution.

5.2 Circuit description

Figure 5.5 shows the block diagram of the proposed circuit. A 5 V charge pump DC-DC converter is used to provide the high bias voltage up to 40 V. A gain control circuit is used with the bias circuit and the two matched APDs to set and stabilize the gain in the high gain APD.

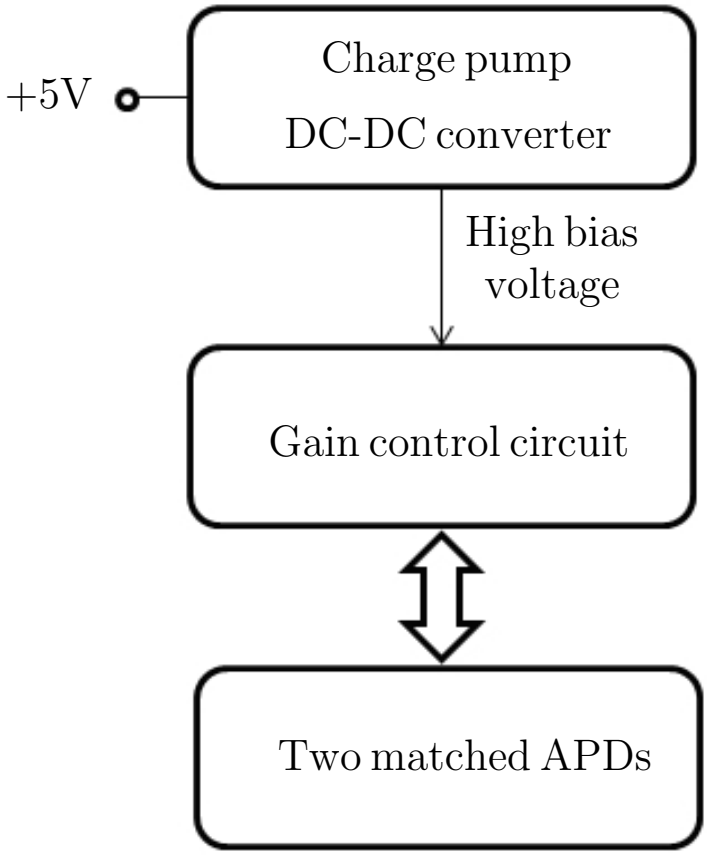


Figure 5.5: Block diagram of proposed circuit.

5.2.1 Charge pump DC-DC converter

The DC-DC converter used is Dickson charge pump circuit [24], see Figure 5.6. In the circuit, an inverter is used to invert the phase of the input clocks. The neighbouring pumping capacitors are connected to these two inverse clocks. A load capacitor is used to smooth the output voltage which will be the only external component needed if the circuit is integrated on a chip. Through every stage, the positive charge is transferred by the diodes and pumping clocks to the output. At the output, a high voltage is obtained to bias the APD.

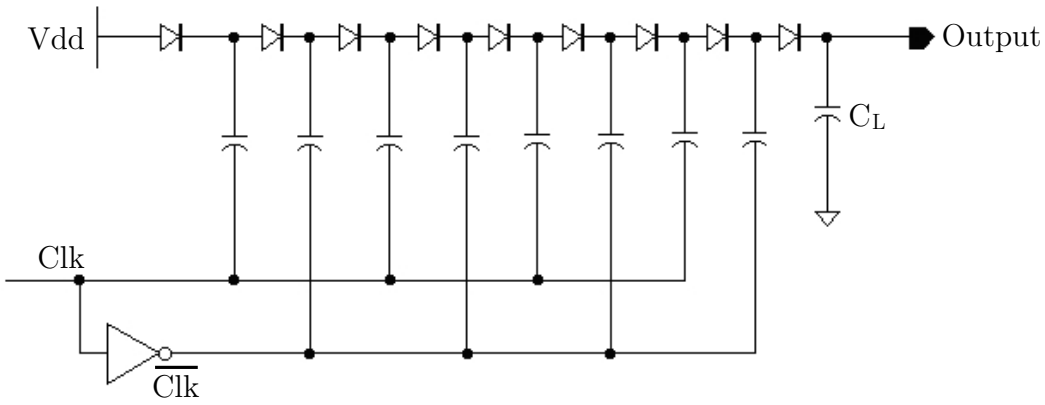


Figure 5.6: Charge pump DC-DC converter.

5.2.2 Gain control and stabilization

The schematic of the gain control circuit with two matched APDs is shown in Figure 5.7. APD2 is biased by the charge pump to generate a multiplied current, I_{MPh}. The other photodiode APD1 is biased to give an unmultiplied current, I_{Ph}.

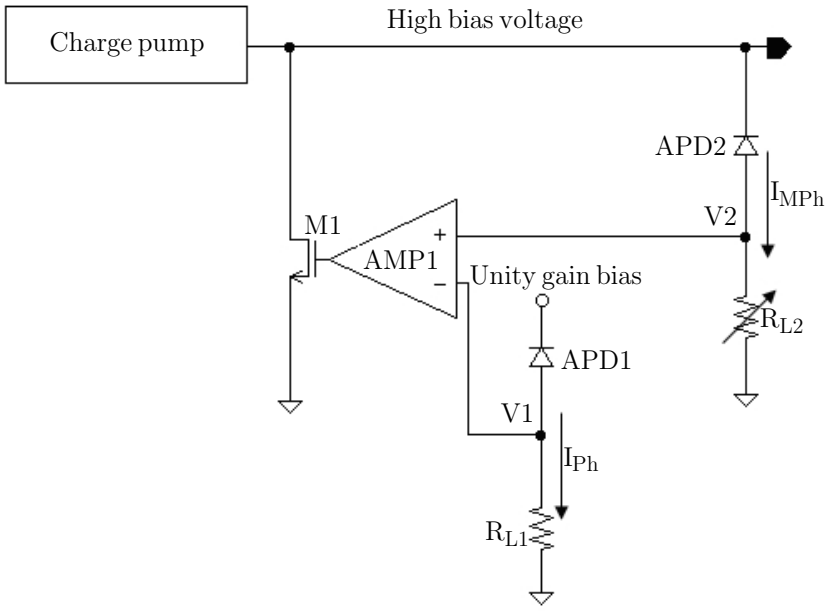


Figure 5.7: Schematic of gain control circuit with two matched APDs.

In the gain control circuit, an op-amp and an NMOS-transistor are used to sense the voltage feedback from both photodiodes and control the bias voltage from the charge pump to adjust the gain of APD2. The bias voltages generate the unmultiplied and multiplied currents in APD1 and APD2 which flow through the load resistors R_{L1} and R_{L2}. Voltages V1 and V2 can be seen at the anode of both photodiodes. V1 is connected to the inverting input of an op-amp, Amp1 and V2 is connected to the non-inverting input of Amp1. If V2 exceeds V1, the op-amp generates an output voltage proportional to the difference between V2 and V1 and the NMOS-transistor M1 will be biased to divide the output current. The bias voltage of APD2 will be decreased and V2 will decrease. If V2 falls below V1, M1 will be turned off, the bias voltage of APD2 can be continuously charged up and V2 will increase. In this way, V2 can be set equal to V1 which makes the multiplication gain in APD2 equal to the ratio of R_{L1} and R_{L2}. When R_{L1} is fixed, the gain of APD2 can be altered by setting the value of the load resistor R_{L2}.

5.3 Simulations

For the simulations, an avalanche photodiode model shown in Figure. 5.8(a) is used. In the model, R1 and R2 represent the internal resistance when the APD is reversed biased far from and near the breakdown voltage which are set to 3 MΩ and 25 kΩ respectively. The voltage source V1 (set to 23 V) and diode D1 is used to model the large increase in gain when the APD is biased close to breakdown voltage. Figure 5.8(b) shows the simulation result of this model when the reverse bias is varied from 0 to 30V, demonstrating an approximate I-V characteristic for a planar APD with increasing gain approaching breakdown.

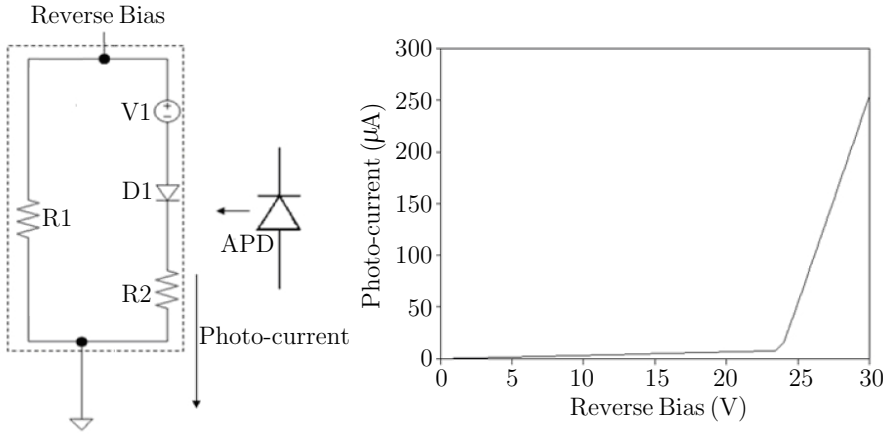


Figure 5.8: APD model and its simulation result.

The simulations of the proposed circuit were completed using the L-foundry 0.15 μm CMOS process in the Cadence design environment [25]. An 8-stage charge pump is used with the pumping capacitors and load capacitor set to 20 pF and 1 nF, respectively. The clock frequency is 50 MHz with $V_{dd} = V_{clk} =$ 5 V. APD1 is biased at V_{dd} to give unity gain and R_{L1} is set to 500 kΩ.

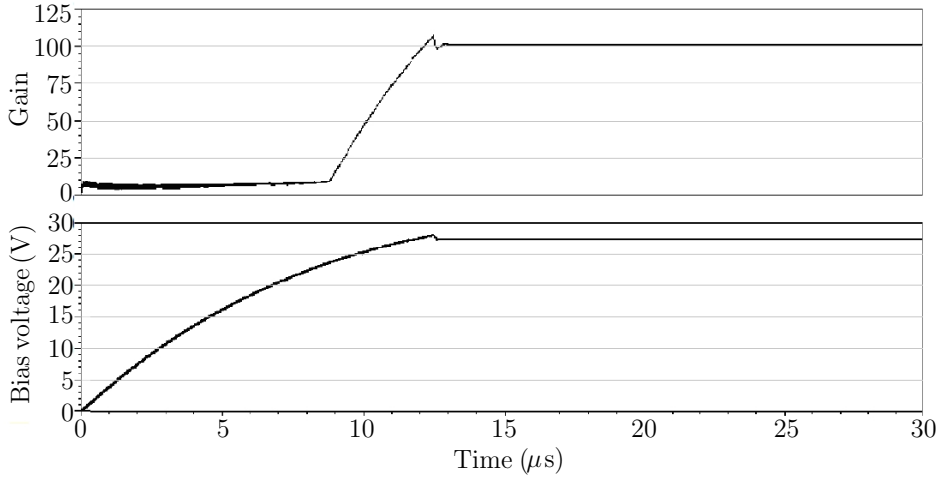


Figure 5.9: Gain and the bias voltage of APD2 when its gain is set to 100.

Figure 5.9 shows the gain and the bias voltage of APD2 when its gain is set to 100 ($R_{L2} = 5$ kΩ). As can be seen from the figure, the op-amp adjusts the bias voltage according to the feedback from the two photodiodes and control the gain precisely.

5.4 Development of PCB module and experimental results

With discrete components, a printed circuit board (PCB) was fabricated. Due to large parasitics and speed limitations of a discrete implementation, a larger load capacitor is used which is set to 47 nF to smooth the output voltage of the charge pump. The pumping capacitors are 22 pF and the diodes are Schottky diodes BAS40. The NMOS-transistor used is ZVN3306F and the op-amp is MCP6041. This circuit operates with clock frequency of 50 MHz and $V_{dd} = V_{clk} = 5$ V. A photograph of the fabricated PCB can be seen in Figure 5.10.

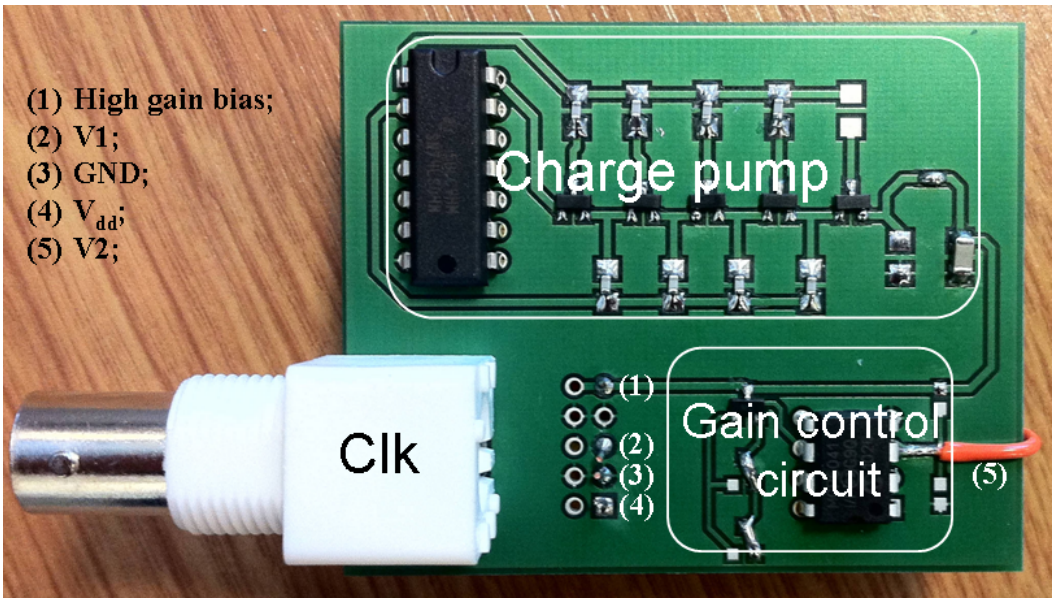


Figure 5.10: Photograph of the fabricated bias and gain control circuit gain.

Figure 5.11 illustrates the measured output voltages of the charge pump for different load currents. It shows the circuit is capable of providing up to 40 V bias voltage and delivering more than 1mA load current at a bias of 27 V.

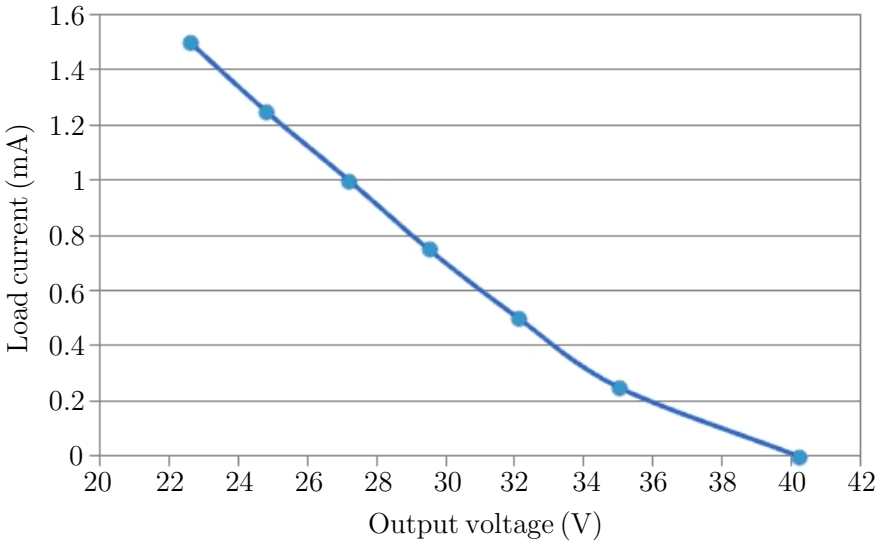


Figure 5.11: Output voltages of charge pump DC-DC converter for different load currents.

For the measurement, two 400 μm diameter circular planar shallow junction APDs developed by the Photodetection and Imaging Group from University College Cork were wire bonded in a dual in line (DIP) package; see Figure 5.12.

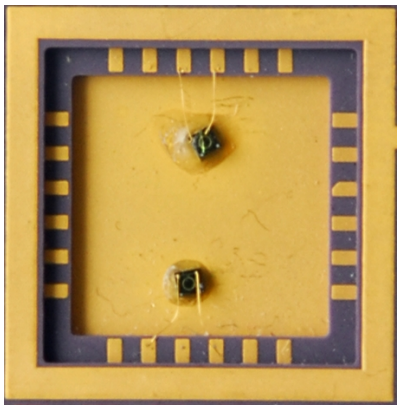


Figure 5.12: Packaged two matched avalanche photodiodes.

The block diagram of the experimental setup can be seen in Figure 5.13. A He-Ne laser source operating at 632.8 nm with the optical power of 330 nW was used as the incident light that was directed to the packaged diodes through an integrating sphere.

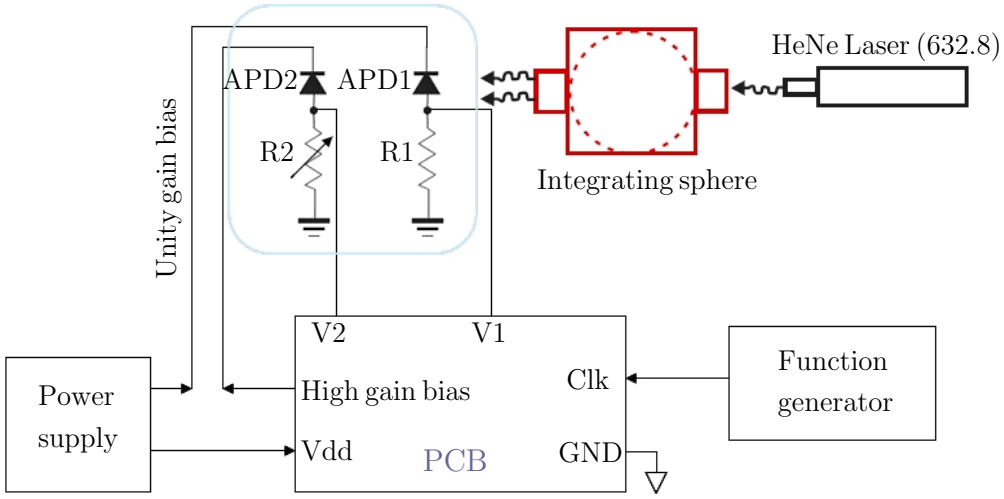


Figure 5.13: Block diagram of the experimental setup.

In the experiments, gain values of 20, 50 and 100 ($R1/R2$) were chosen to be the required gain values. Figure 5.14 shows the gain variation over a period of time. As can be seen from the figure, for the gains set to 20, 50 and 100, the mean gains measured are 20.55, 51.49 and 102.69 respectively. The gain offset errors are similar and close to 3% with standard deviations of less than 0.1. The gain offset error is mainly caused by the input bias current of the amplifier. Corrections can be made (Measured gain - 3% Set gain) to the measured gain so that it can demonstrate the intended set gain more accurately. Figure 5.15 shows the photo-current in the APD when the ambient temperature is changed. As shown in the figure, with the proposed circuit, the APD shows a more stable performance than that without the circuit. [26, 27].

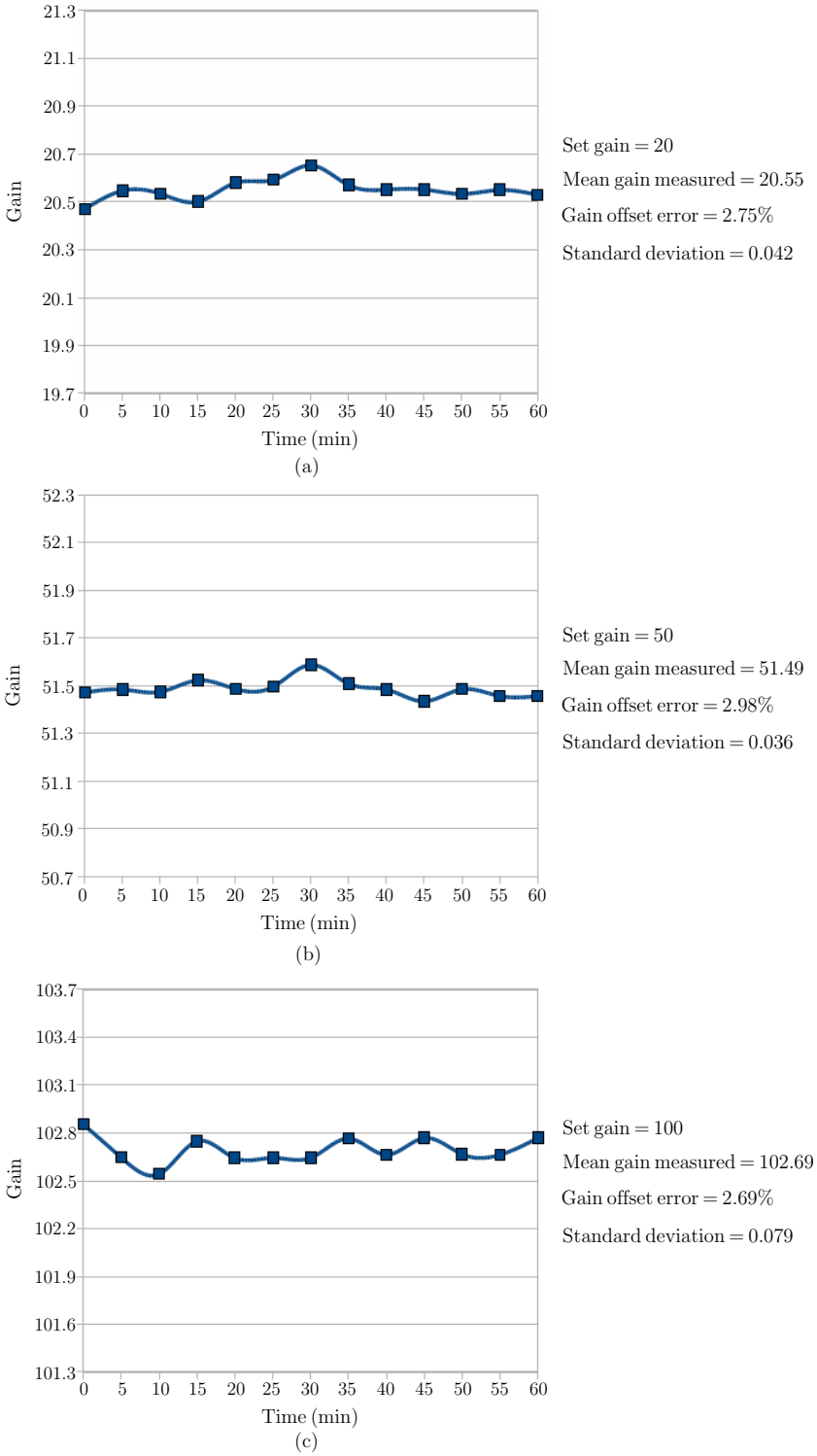


Figure 5.14: Gain variation over a period of time under the control of the proposed circuit: (a) Gain set to 20; (b) Gain set to 50; (c) Gain set to 100.

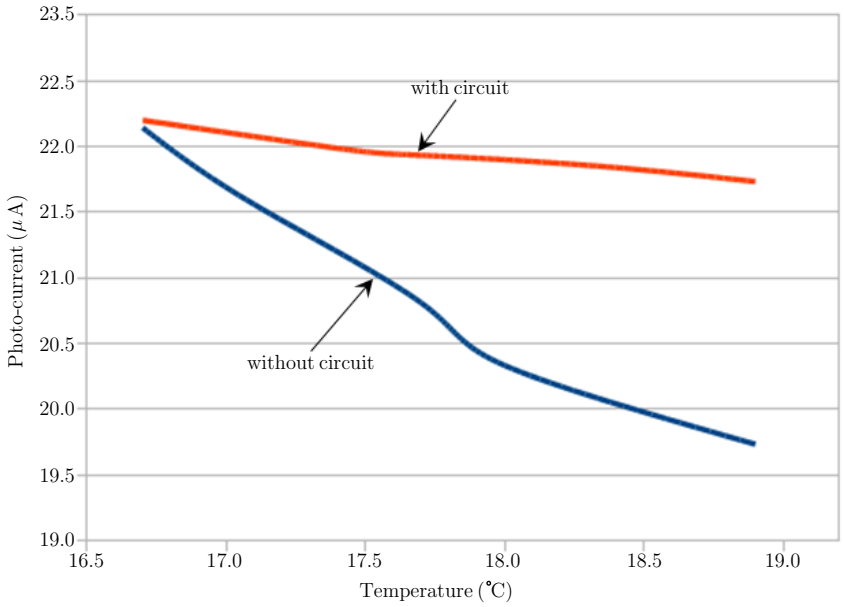


Figure 5.15: APD's performance when ambient temperature is changed.

5.5 Conclusions

In this chapter, the development of a bias control and gain stabilization circuit has been described. Existing solutions in the literature were reviewed. The proposed circuit operation was explained; and simulations and measurements were presented. Temperature stablilization systems are used by many research groups to provide a stable low APD temperature for APD gain stabilization. These are expensive in terms of initial and maintenance costs and this limits their usefulness to a laboratory environment. Active control of the APD gain by varying its bias as a function of temperature is another way to operate the APDs with a stable gain, independent of the temperature. However, the required bias voltages for the APD at different temperatures must be measured in advance by the user. Moreover, the temperature compensation elements suffer from temperature coefficient mismatches that further limit their operational accuracy. The circuit developed in this work is capable of providing a

high bias voltage for planar APDs, controlling and stabilizing their gain without the need for external temperature sensing and control elements thereby lowering the system cost and complexity. The circuit was simulated in the Cadence environment, fabricated with discrete components and tested using packaged APDs. Results show that the circuit can provide in excess of 40 V bias voltage for the planar APD and set the gain to within 3% of the desired gain with a standard deviation of less than 0.1.

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Chapter 6

Conclusions and future work

This chapter summarises the contributions achieved in this work and research ideas that could be pursued in the future are described.

6.1 Conclusions

In this thesis, three circuits have been designed and developed for control and enhancing the performance of the APD.

A bias solution that is used for the APDs operating in both linear and Geiger modes has been presented. The design consists of a dual-rail charge pump bias circuit and novel output voltage regulators. The operation of this circuit is evaluated experimentally and a layout of the circuit was designed using the L-Foundry 0.15 μm process and post layout simulations are presented. Results show that the circuit is capable of sourcing mA range load currents for shallow-junction planar APDs that operate up to 40 V. The layout of the circuit designed using L-Foundry 0.15 μm CMOS process shows a small footprint of 1.55 mm $\times$ 1 mm, making it suitable for hybrid integration with 2 external capacitors and an APD in a single package. This would operate seamlessly from a 5 V supply, thereby taking the additional responsibility for biasing the APD from the end-user. The possibility of developing a fully integrated version

of this circuit was also discussed which shows that the circuit is capable of full integration for the devices with voltage ripple tolerance of greater than 70 mV.

A new active quench and reset circuit (AQRC) with novel hold-off time control logic for Geiger-mode avalanche photodiodes (GM-APDs) has been described. The circuit was designed and simulated in Cadence and sent for fabrication using a conventional 0.35 μm CMOS process and tested with a GM-APD. Results show that this circuit is capable of linear changes to the hold-off time from several nanoseconds to microseconds with a reasonable step of 6.5 ns that allows setting of the optimal 'afterpulse-free' hold-off time for any GM-APD through digital inputs or additional signal processing circuitry. A minimum dead time of 28.4 ns was observed from the measurement, demonstrating a saturated photon-counting rate of 35.2 Mcounts/s with this AQRC.

A gain and stabilization control circuit has been demonstrated. This circuit is based on the idea of using two matched APDs to set and stabilize the gain which operates without the need for external temperature sensing and control electronics and thus lowers the system cost and complexity. A printed circuit board (PCB) module of the proposed circuit was fabricated with discrete components and measured with packaged APDs. Results show that the circuit is capable of providing bias voltages up to 40 V for the APDs, precisely setting its gain and compensating for the changes in the temperature to maintain a stable gain.

6.2 Future work

Following the developments from this thesis, some improvements could be made to the designed circuits and a number of areas could be pursued in the future research.

Firstly, an on-chip clock generator could be designed and used in the bias circuit that will eliminate the need for the external clock signal. Filters can be applied at the output of the bias circuit that will decrease the ripples on the output bias voltage. The layout of the bias circuit should be submitted for fabrication. A hybrid package of the fabricated chip, an APD and several external components can provide a compact, single package solution (as shown in Figure 6.1) for APD-applications. A fully integrated bias circuit can be further developed for biasing the APD from a system power supply such as 5 V or 3.3 V.

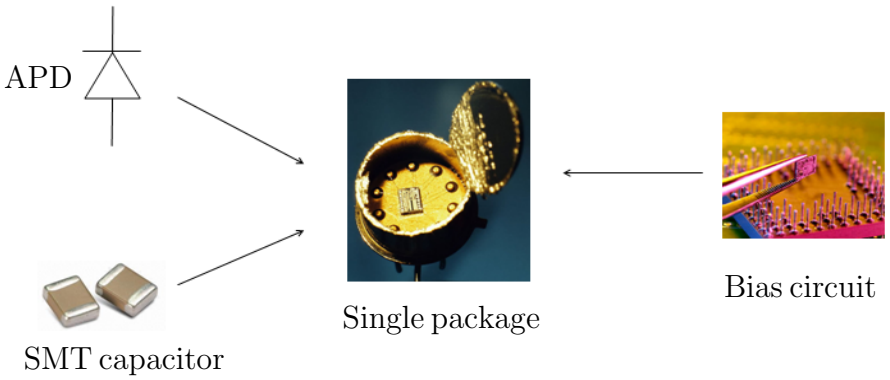


Figure 6.1: Single package APD solution with bias circuit.

Secondly, there are potential improvements that can be made to the active quench and reset circuit. Integrating the active quench and reset circuit and the GM-APD would reduce the parasitics and the deadtime to achieve a higher saturated photon counting rate as discussed in Chapter 4. Newer CMOS processes can be used to design the circuit that will reduce the total chip area and give a faster speed response to the sensing circuit. Moreover, combining the bias circuit and active quench and reset circuit would produce a GM-APD system which is a highly compact solution with adjustable bias voltage and digitally controlled hold-off time. Signal processing circuitry could be added

to the system for intelligent control of the bias voltage as well as the hold off time. In addition, this circuit could be also implemented with arrays of GM-APDs and some other circuitry to produce a complete imaging solution. When implementing the circuit with APD arrays, only one ring-oscillator is needed to provide the clocks which can be shared by the control logics for each pixel's hold-off time control that will simplify the design and reduce the circuit size.

Last but not least, the three circuits designed (bias circuit, active quench and reset circuit and gain stabilization circuit) can be combined. An interface logic needs to be designed. By controlling the bias voltage of the APD using the bias circuit, the APD's operation mode can be decided. When the APD is biased in linear mode then the gain control and stabilization circuit should be active to set the gain in the APD. When the APD is biased in Geiger-mode then the active quench and reset circuit should be active to enhance the GM-APD's performance. This system can be developed using existing circuits and implemented on a PCB module. It can also be designed into an integrated circuit that will decrease parasitics, improve speed response and reduce size, weight and power consumption. Read-out circuits and other signal processing circuitry also can be designed to process the results for each mode. Similarly, the circuit could be also implemented with APD arrays. The connections could be made in either hybrid or monolithic form.