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Low-temperature conductance oscillations in junctionless nanowire transistors

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Junctionless nanowire transistors show more marked oscillations conductance oscillations than inversion-mode devices. These oscillations can be observed at higher temperature, drain voltage, and gate voltage than in surface-channel, inversion-mode multigate metal-oxide-semiconductor field-effect devices. Clear oscillations are observed at 77 K at a drain voltage of 100 mV in devices with a 10×10 nm^2 cross section. © *2010 American Institute of Physics*. [doi:10.1063/1.3506899]

The junctionless nanowire transistor (JNT) is a metal-oxide-semiconductor MOS device consists of a heavily doped silicon-on-insulator (SOI) nanowire and a trigate (pi-gate) electrode. The channel region of the device has the same doping polarity and concentration as the source and the drain. There are, therefore, no junctions and the device basically behaves a resistor that can be pinched off through "electrostatic squeezing" of the channel region. The electrical characteristics of the JNT are similar to those of a regular metal-oxide-semiconductor field-effect transistor (MOSFET), with a subthreshold slope close to k_BT/q ln(10), where k_B is Boltzmann's constant and q is the electron charge. Both n- and p-channel JNTs have been demonstrated.[1] Oscillations of the drain current I_D have been observed in trigate MOS transistors as gate voltage V_G is increased. This is attributed to the successive filling of subbands and to intersubband scattering effects. As a rule of thumb, oscillations can be observed if the temperature T at which the measurement takes place is not too large compared to $\Delta E/k_B$ where ΔE is the energy difference between subbands, and if the drain voltage is lower than $\Delta E/q$.[2–6]

In inversion-mode trigate MOSFETs with a small cross section, conduction around threshold occurs in the center (bulk) of the device. This effect is called "volume inversion."[7] At higher gate voltages, three surface channels are formed, two along the sidewalls and one at the top of the nanowire (the corner effect is here neglected).[8] In heavily doped junctionless transistors, the current is always flowing in the center (bulk) of the nanowire. Above threshold, the carriers are confined within a thin "filament" channel from source to drain. The diameter if the filament increases as the gate voltage is increased, until flatband is reached, in which case the cross section of the filament becomes equal to the physical cross section of the nanowire.[1] Thus, unlike in inversion-mode devices, the cross section of the conduction path of a junctionless device is smaller than its physical cross section. This field-induced carrier confinement adds to the physical confinement, which should give rise to well separated energy subbands, and, as a result, to clearly observable oscillations in the $I_D(V_G)$ curves.

N-channel JNTs with a gate length of 1 μm, a cross section of approximately 10×10 nm^2, an N-type doping concentration of 3×10^{19} cm^{-3} and a gate oxide thickness of 7 nm were measured at cryogenic temperatures. A typical transmission electron microscope cross section of such a device can be found in Ref. 9.

Figure 1 shows the conductance g versus gate voltage measured at a temperature of 8 K for different values of the drain voltage. The conductance is defined as $g=I_D/V_D$. Clear "ripples" can be seen in Fig. 1. These are indicative of successive subband filling as the gate voltage is increased. Clear oscillations can be seen for drain voltage values up to 100 mV. As the drain voltage is increased above that value, the oscillations dampen but weak oscillations can still be observed up to $V_D=700$ mV. Junctionless transistors have a larger source and drain resistance than conventional MOSFETs, because of lower doping concentration. This could affect results at high drain current, but does not seem to impact the measurements for drain voltages up to 100 mV, since the conductance g increases with V_{DS} (Fig. 1).

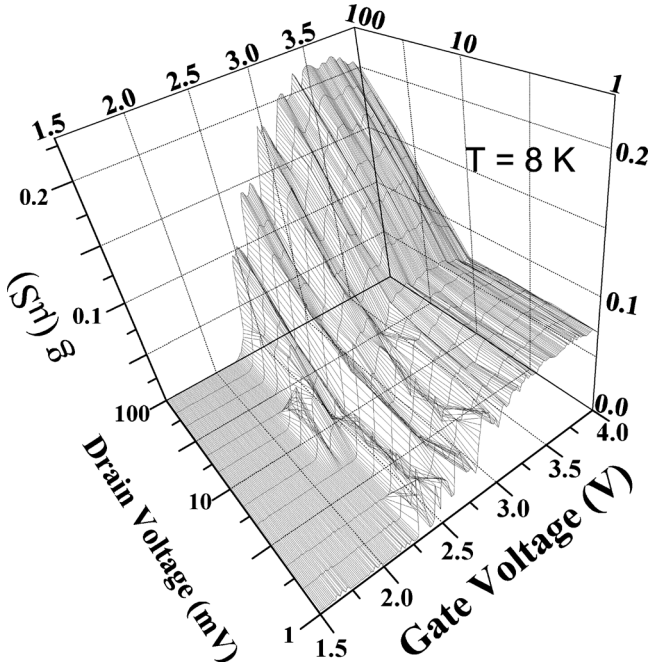


FIG. 1. Measured conductance in a junctionless n-channel transistor as a function of gate and drain voltages.

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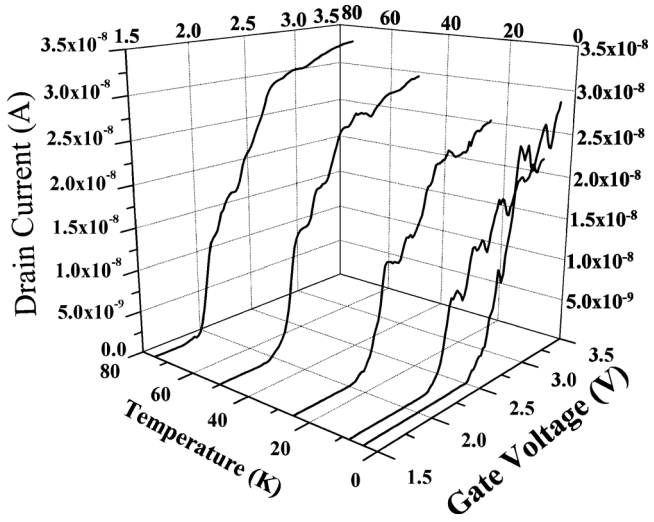


FIG. 2. Measured drain current in a junctionless n-channel transistor as a function of gate voltage and temperature. Drain voltage is 100 mV.

Figure 2 shows the drain current versus gate voltage at $V_D = 100$ mV for different temperatures. Oscillations are observed up to liquid nitrogen temperature (77 K), but are not present at room temperature. Figure 3 shows the drain current measured on an inversion-mode (p-type doped channel) devices with the same dimensions and fabrication parameters as the junctionless transistor. The oscillations are much less pronounced than in the junctionless device under the same measurement conditions (Fig. 1).

In inversion-mode trigate devices, "volume inversion" can sometimes be observed right above threshold. In that case, carrier confinement is observed and the presence of one-dimensional density of states (DoS) can manifests itself in the form of current oscillations as the gate voltage is increased. Above threshold, conduction takes place in three channels located at the top interface and the two sidewalls of the nanowire, and the high electric field present in those channels result in surface scattering. As a result, oscillations are usually visible only near threshold, and not at higher gate voltages. Because the carriers are spread over the entire cross section of the device (e.g., approximately 10×10 nm^2 in our case), confinement effects can only be seen at very low temperature and drain voltage, such as $T = 37$ K, $V_D = 50$ mV for a nanowire diameter of 7 nm in Ref. 3. In junctionless transistors, the entirety of the current at and above threshold flows in a bulk channel in the middle of the nanowire. Above threshold and below flatband voltage, the diameter of this channel increases with gate voltage, but is always smaller than the cross section of the nanowire. Furthermore, the electrons in the channel are exposed to little or no electric field perpendicular to carrier transport.[9] These two effects allow for the production of more marked oscillations than in inversion-mode devices; furthermore, these oscillations can be observed at higher temperature, drain voltage, and gate voltage than in surface-channel devices.

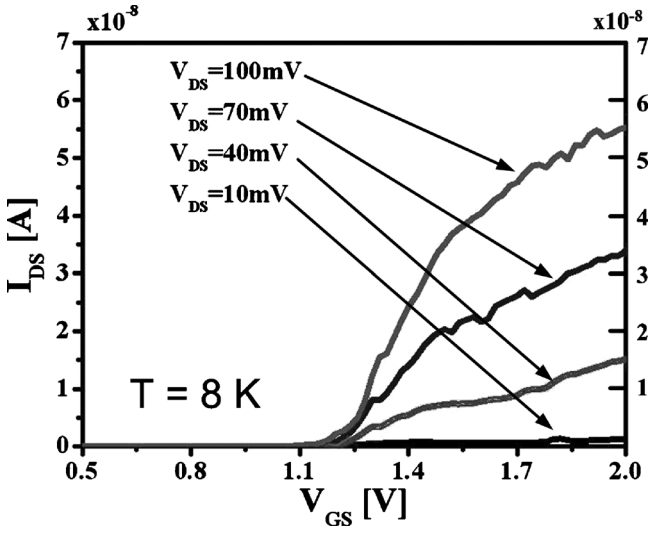


FIG. 3. Measured drain current in an inversion-mode n-channel trigate transistor as a function of gate and drain voltages.

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