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A Dual-rail Charge Pump Bias Circuit for Avalanche Photodiodes

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Abstract — **In this paper, a dual-rail charge pump bias circuit for avalanche photodiodes is presented. The proposed circuit was fabricated and measured on a printed circuit board (PCB). Experimental measurements show that it is capable of providing up to 50 V bias voltage and delivering more than 40 mW of power for shallow-junction planar APDs that operate between 25 V and 40 V, allowing avalanche currents in the mA range. The circuit requires only a dual supply rail at ± 5 V which makes it useful for reducing the system complexity and the cost of using additional external power supplies in an APD-based sensing system. With the shunt regulators in the circuit, the bias voltage can be accurately controlled and easily adjusted.**

Keywords — **Avalanche photodiodes, Bias voltage, Dual-rail Charge pump, Shunt regulator.**

I Introduction

Avalanche photodiodes are used in wide range of low-light sensing applications such as astronomy, DNA sequencing, quantum key distribution, LIDAR and medical sensing. Planar APDs have been developed over a number of years for low-light sensing applications requiring both linear, multiplicative and Geiger-mode operation [1], [2]. Typically these APDs are designed with a breakdown voltage less than 30 V and operate with a bias more than 25 V which makes it difficult to bias them without additional external high-voltage supplies separate from the rest of the APD-based sensing system. The additional supplies, however, add cost and complexity to the system, thereby limiting their usefulness in APD-based applications.

This paper describes a bias circuit for avalanche photodiodes. In the circuit, a dual-rail charge pump is used (positive and negative charge pump) to generate the high bias voltage and two shunt regulators are included to control the magnitude of the voltage. Experimental measurements of the PCB implementation of this circuit show its capability to deliver more than 40 mW output power in the bias range from 25 V to 40 V. The circuit operates from a dual supply rail at ± 5 V which is readily available to power the other parts of the APD-based sensing system. This approach lowers the system cost and complexity. Moreover, this circuit has potential for integration which is also attractive for applications requiring a compact integration APD device solution [3].

II Circuit Description

Fig. 1 shows the block diagram of the bias voltage circuit which consists of two main parts: (i) A dual-rail charge pump which provides the high bias voltage for the load. (ii) Two shunt regulators which are used to control the output voltage for the positive and negative outputs of the load.

a) Dual-rail charge pump

Fig. 2 shows the schematic of the dual-rail charge pump. The positive and negative charge pumps used in Fig. 2 are Dickson pump circuits [4]. An inverter is used to invert the phase of the input clocks. The MOS transistors in the circuit are connected in diode fashion. The neighbouring pumping capacitors are connected to these two inverse

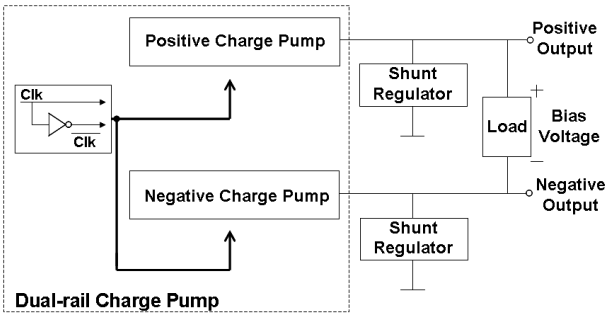


Fig. 1: Block diagram of bias voltage circuit

clocks. NMOS is used for the positive charge pump to transfer the positive charge. PMOS is used for the negative charge pump to transfer the negative charge [5]. The charge is sourced from the system power supply, V_{dd} or -V_{dd}. Through every stage, the output voltage is increased or decreased by the pumping clock. At the output, a higher potential exceeding the magnitude of the system supply is obtained.

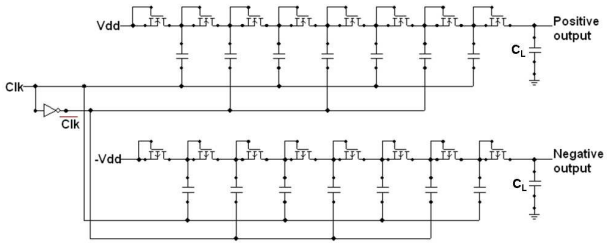


Fig. 2: Schematic of Dual-rail Charge Pump

b) Shunt Regulator

For maximizing output current, shunt regulators are needed to control the output of the charge pump. With the shunt regulator, the charge pump operates continuously. Fig. 3 shows the schematic of the shunt regulator. This regulator uses a MOS transistor (NMOS for positive output and PMOS for negative output) in parallel with the load and behaves functionally like a variable current divider to obtain load voltage regulation [6]. R1 and R2 are used to decrease the output voltage to a comparable level V_1. An op amp is used as the error amplifier. A power supply of V_{dd} and GND are used for amplifying the positive error, a power supply of GND and -V_{dd} is used for amplifying the negative error. If V_1 exceeds the regulation level V_{ref}, the error amplifier generates an output voltage proportional to the difference between Vref and V_1 and the MOS transistor will be biased to divide the output current. If the output falls below the regulation level, the MOS transistor will be turned off, and the output can be continuously charged up. In this way, V_1 can be set equal to V_{ref}. By setting the reference voltage V_{ref}, the output voltage can be altered.

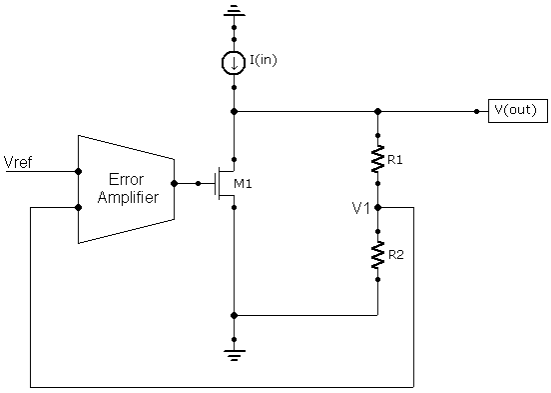


Fig. 3: Schematic of Shunt Regulator

III Simulations

In [3], the simulations were completed in Cadence design environment using Austria Microsystems 0.35 μm CMOS process. The clock frequency is 50 MHz with $V_{dd} = V_{clk} = 5$ V. Here, a 7-stage dual-rail charge pump is used with pumping capacitors of 20 pF. The two load capacitors are 3 nF each. Simulation results show that the bias voltage can be regulated accurately with a peak-peak ripple of less than 25 mV. Fig. 4 shows the maximum load current and output power for different bias voltages. It is clear from the figure that the circuit is capable of meeting load current demands in excess of 1 mA at bias voltages up to 45 V.

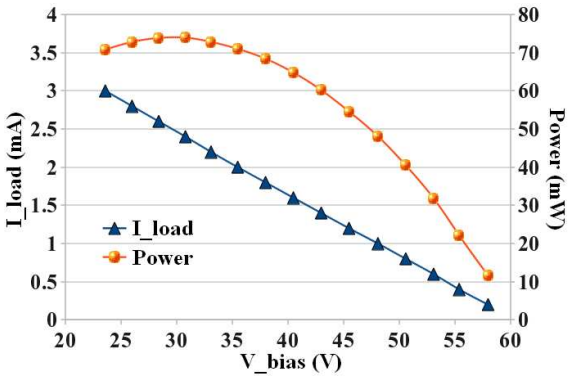


Fig. 4: Simulation results of Maximum load current and output power for different bias voltages

IV Experimental Measurements

With discrete components, the circuit was implemented on a printed circuit board (PCB). Due to large parasitics and speed limitations of a discrete implementation, larger capacitors are used. The pumping capacitors are 0.1 μF and the load capacitors are 1 μF. The N-transistors and P-transistors

used are ZVN3306F and ZVP3306F, respectively. A TLE2021IP low-power precision op-amp is used as the error amplifier. The clock frequency is 100 kHz with $V_{dd} = V_{clk} = 5$ V.

In Fig. 5, the maximum load current and output power for different bias voltages are demonstrated. It shows the circuit is capable of delivering greater than 1 mA at bias voltage up to 40 V. Fig. 6 shows the bias voltage when it is regulated at 30 V. The voltage ripple on the positive and negative output are 120 mV and 180 mV respectively. This is mainly caused by two factors: (i) Noise due to the discrete implementation. (ii) Low speed of the amplifier, which means the amplifier can not generate the error voltage quick enough when the output voltage exceeds the regulation level. The ripples can be reduced with an integrated circuit implementation or a faster amplifier.

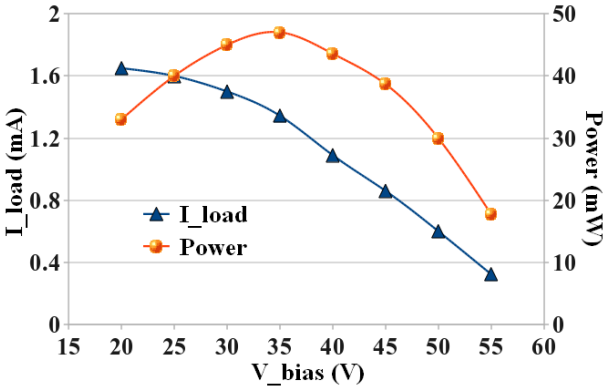


Fig. 5: Plots of Maximum load current and output power for different bias voltages

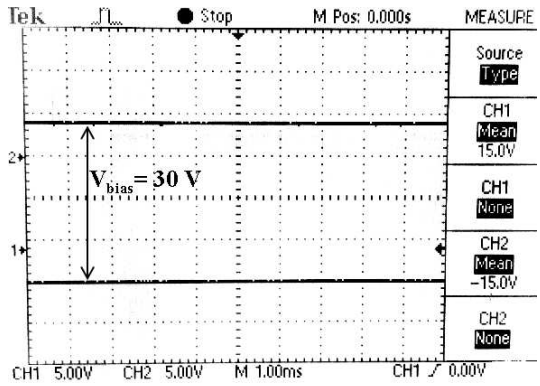


Fig. 6: Bias voltage when the charge pump is regulated at 30 V

V Conclusions

This paper describes an adjustable bias circuit which can provide in excess of 50 V for biasing planar APDs. The experimental measurements of the fabricated PCB module show the output bias voltage can be adjusted precisely and can sustain mA current output when operating between 25 V and 40 V. This circuit can be used in an APD-based sensing system to provide the bias voltage for the APD thereby reducing the complexity and additional cost of using external high-voltage power supplies. Moreover, this circuit has potential for integration. The circuit, if fabricated on chip, can be hybrid integrated with the APD and 2 surface mount external capacitors in a single package (TO-can or Dual-in-line) which is very attractive for applications requiring a compact integrated APD device solution.

VI Acknowledgments

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