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Characterizing stress in ultrathin silicon wafers

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The aim of this letter is to calculate the mechanical grinding induced bow and stress in ultrathin silicon wafers. The reverse leakage current of a *p-n* junction diode fabricated on a 4 in. silicon wafer was measured for wafers thinned to various thicknesses. A correlation with the residual stress was obtained through band gap narrowing effect. The analytical results were compared with experimental bow measurements using a laser profiler. The bow in 50 μm thick wafer was found to be less than 2 mm using the current grinding process. © *2006 American Institute of Physics*.
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The demand to miniaturize products for ambient system applications continues to drive the evolution of electronic packaging and assembly methods.[1] One of the key approach towards miniaturization is the incorporation of ultrathin chips (i.e., silicon chips thinned down to 50 μm or less in total thickness) for the final packaged device. During the wafer thinning process, the backside of the wafer is ground with an abrasive material (diamond). Silicon is continuously scratched by diamond particles embedded in the base plate. The particles result in a uniform pressure on the back surface of the wafer.[2] This causes a compressive stress on the backside, and correspondingly, the upper surface is under tension [Fig. 1(a)]. Therefore, when the silicon wafer is released from the chuck, it becomes concave upward with a positive radius of curvature. The equibiaxial tension along the [110] direction can be equated with a uniform hydrostatic stress and a compressive stress along the [001] direction. The resulting residual stress and wafer bow cause problem during wafer level assembly processes,[3] and therefore require detailed characterization.

The valence and conduction band edges of Si get displaced due to the external stress. This results in a modification of the band gap energy levels as shown in Fig. 1(b). The hydrostatic part of the stress results in an equal shift of the valence and conduction bands, whereas the compressive stress results in band splitting.[4] The six degenerate conduction levels (Δ_6) split into a low energy band of four degeneracies (Δ_4) and a high energy level (Δ_2). Similarly, the valence band degeneracy at $\mathbf{k}=\mathbf{0}$ gets destroyed into three levels, with the light holes (LHs) moving through the heavy hole valence band. The shift in valence band edge $\Delta E_v^{(\mathrm{lh})}$ and conduction band edge $\Delta E_c^{(\Delta_4)}$ is given by

$$\Delta E_c^{(\Delta_4)} = \Xi_d(\epsilon_{xx}+\epsilon_{yy}+\epsilon_{zz}) + \Xi_u \epsilon_{\Delta_4}, \tag{1}$$

$$\Delta E_v^{(\mathrm{LH})} = a(\epsilon_{xx}+\epsilon_{yy}+\epsilon_{zz}) + 2|b\times(\epsilon_{xx}-\epsilon_{zz})|, \tag{2}$$

where (Ξ_d, a) are hydrostatic deformation potentials (cause an equal band shift) and (Ξ_u, b) are shear deformation potentials (result in band splitting). The above equations are written considering an equibiaxial in-plane stress wherein the strain tensor is related to the stress σ, by compliance tensor S_{ij}, as given by $\epsilon_{xx}=\epsilon_{yy}=(S_{11}+S_{12})\sigma$, $\epsilon_{zz}=2S_{12}\sigma$, and $\epsilon_{xy}=\epsilon_{xz}=\epsilon_{yz}=0$. The deformation potentials, calculated using nonlocal empirical pseudopotentials by Fischetti and Laux[5] as shown in Table I, were used for further calculations. Using these values, the change in band gap energy $[\Delta E_g = \Delta E_c^{(\Delta_4)} + \Delta E_v^{(\mathrm{lh})}]$ as calculated using Eqs. (1) and (2) is given by

$$\frac{\Delta E_g}{\Delta\sigma} = -0.13 \text{ meV/MPa}. \tag{3}$$

To quantify the thinning process induced change in band gap, the reverse leakage current of a *p-n* junction diode present on the test wafer was measured. The reverse leakage current of a junction diode is given by[6]

$$I_R = K_1 \frac{n_i^2}{\sqrt{\tau_p N_D}} + K_2 \frac{n_i}{\tau}\left(\frac{V_R}{N_D}\right)^m, \tag{4}$$

where K_1 and K_2 are constants related to junction physical parameters; n_i, N_D, τ_p, τ, and V_R are carrier intrinsic concentrations, effective doping density in the diode base, minority carrier lifetime, effective lifetime for the space charge region, and applied reverse voltage, respectively. For low reverse bias, the effect of generation current was ignored due to extremely low values.[6] Also, the intrinsic carrier concentration is a function of band gap energy, $n_i=\sqrt{N_c N_v}\exp(-E_g/(2k_BT))$, where N_c and N_v are the effective density of states in the conduction and valence bands. Hence, using Eqs. (3) and (4), the following relation is obtained:

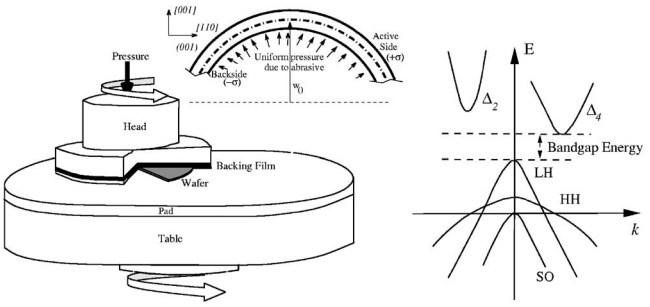


FIG. 1. (a) Mechanical grinding process, and its effect on silicon wafer bow w_0, and stress distribution σ are shown. (b) Effect of compressive stress along [001] on Si band energy.

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TABLE I. Silicon parameters used in this calculation.

Ξ_d (eV)	Ξ_u (eV)	a (eV)	b (eV)	S_{11} (10^{-12} m^2/N)	S_{12} (10^{-12} m^2/N)
1.1	10.5	2.1	−2.33	7.68	−2.14

$$\frac{\Delta I_R}{I_R} = -\frac{\Delta E_g}{k_B T}. \tag{5}$$

A simple method, based on nonlinear Von Kármán equations [(6) and (7)], was used to calculate the approximate bow in the ultrathin wafers. The stress value σ, calculated in the chips diced from locations around the center of the wafer, was considered as an average of the meridional and circumferential stresses at the center of the wafer. For derivation, azimuthal symmetry was assumed due to uniform loading condition:

$$\nabla_r^4 w = \frac{p}{D} + \frac{h}{rD}\frac{d}{dr}\left(\frac{d\Phi}{dr}\frac{dw}{dr}\right), \tag{6}$$

$$\nabla_r^4 \Phi = -\frac{E}{r}\frac{dw}{dr}\frac{d^2w}{dr^2}, \tag{7}$$

where ∇_r^4 is the biharmonic operator in polar coordinates, Φ is the Airy stress function, w is the radial deflection of the wafer $[w=w_a f(r)]$, p is the assumed uniform pressure due to the grinding process, D is the flexural rigidity, r is the radial component, h is the wafer thickness, and E is Young's modulus. The relation between average stress and deflection at the center of the wafer is given by

$$w_0(\text{in } m) = \frac{6hE(1-\nu) - \sqrt{6}\sqrt{E(-1+\nu)(6h^2E(-1+\nu) + a^2(1+\nu)^2(-5+3\nu)\sigma)}}{E(1+\nu)(-5+3\nu).} \tag{8}$$

The experiments for wafer stress and bow were carried out on test chips[7] of thicknesses 525, 250, 100, and 50 μm and lateral dimensions of 10×5 mm^2. The test chips were fabricated in-house and contain a diffused heater resistor covering 85% of the chip area and three *p-n* junction diodes. The wafers were mounted onto the grinding chuck, with the active side protected by UV film from the chuck, and the blank side of the wafer was ground using rotational force from the different sizes of grit paper. This process allowed an easy processing for removal of bulk silicon at a relatively low cost, but backgrinding could cause a large amount of damage to the back of a sample. A large percentage of this damage was done to the crystal structure, which could lead to degradation of the electrical characteristics of the final device. For this reason the initial grinding was limited to 250 μm; below this, considerable yield loss could occur due to wafer breakage. To reduce the thickness further, fine grinding followed by a polishing step was used to obtain 50 μm thick wafers. The fabrication related stress in all the wafers before thinning was considered equal due to the same fabrication process. However, the 525 μm thick chip was used without any grinding, and hence, the change in leakage current after thinning was calculated with reference to the leakage current in a 525 μm thick wafer. *I-V* characteristics of the junction diode located at the center of the chip was measured with a Wentworth probe station using a Hewlett-Packard semiconductor parameter analyzer (model 4156A, having a resolution of 1 fA). Six specimens from locations around the center of the wafer were tested for each wafer thickness to remove any local errors in the measured values. Each *I-V* characterization was performed five times to neglect the effect due to variation in ambience and random errors. All the experiments were done under ambient conditions of 295 K and 60% humidity.

The reverse-bias junction leakage current for the diode with different chip thicknesses is shown in Fig. 2. The stress and bow in the wafer calculated using Eqs. (3), (5), and (8) are shown in Table II. The active surface is in tensile stress which generates a compressive out-of-plane strain. It must be also considered that in ultralarge scale integration process flow, the multiple layers of metal lines and nitride layers cause a compressive in-plane stress (along [110] direction). Hence, the positive stress values shown in Table II are attributed to the mechanical thinning process. The stress in the wafer is increased as the wafer is thinned, due to the damage in the crystalline structure of the backside of the wafer. How-

TABLE II. Reverse saturation current, stress, and bow.

Thickness (μm)	I_s (fA)	σ (MPa)	w_0 (mm)
525	290	⋯	⋯
250	353	63	0.937
100	470	122	1.48
50	415	84	1.26

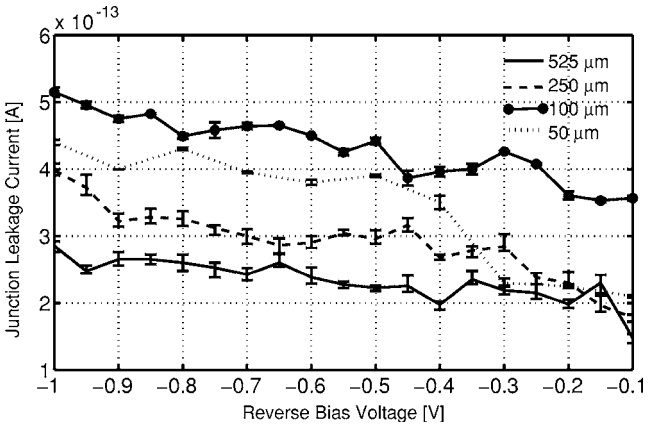


FIG. 2. Reverse-bias junction characteristics of junction diodes with varying chip thickness.

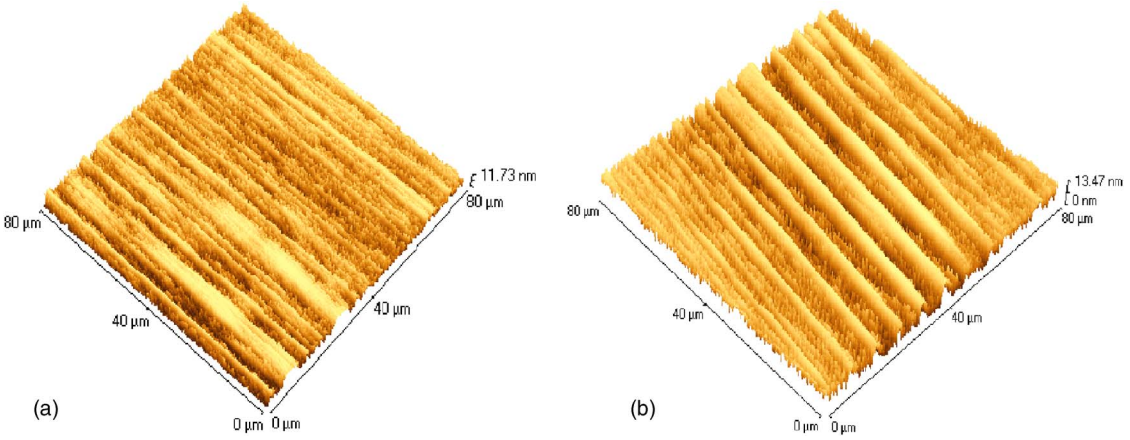


FIG. 3. (Color online) AFM image of the back surface of thinned silicon chips: (a) 50 and (b) 100 μm.

ever, from the magnitude of the stress observed in the different chip thicknesses, it is concluded that the final polishing step removes most of the damage layer leaving wafers in a very low stress state. The slightly higher stress value of 100 μm chip compared to 50 μm chip is attributed to the larger back surface area of 100 μm chips after thinning. The thinning process leaves its fingerprint on the backside of the wafer, creating modified surfaces. This was corroborated by atomic force microscopy (AFM) images of the backside of 100 and 50 μm chips [Figs. 3(a) and 3(b)]. Silicon dioxide forms on these surfaces, which is more voluminous and leads to higher compressive stress values on the backside. It must be considered that the stress values calculated here are much lower than the fracture stress of the chip ($\approx$400–600 MPa depending on wafer thickness[8]).

The bow values for ultrathin wafer was considerably higher than for the 250 μm thick wafer as given in Table II. This was attributed to the lower flexural rigidity of the ultrathin chips, and even for lower stress values for the 50 μm chips, the bow was comparatively higher. Figure 4 shows the bow for 50 μm wafer as measured with a laser profiler. The surface profile of the wafer is typically dome shaped after the thinning process. Further, the wafer bow w_0 as calculated in Table II is in accordance with data available for similar process in literature,[9,10] wherein optical and mechanical techniques were used.

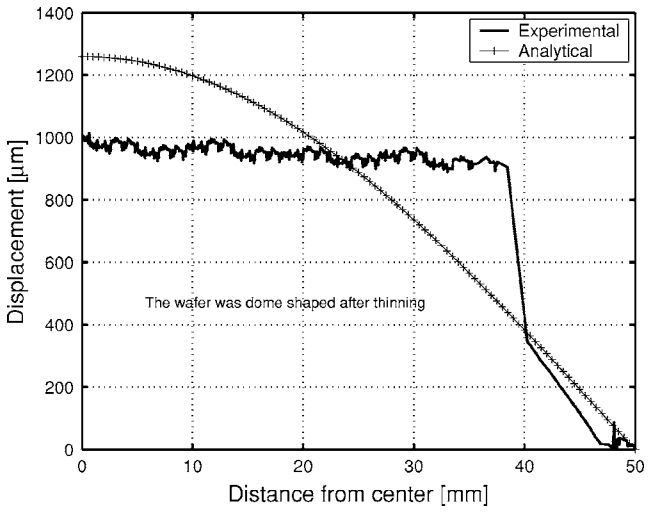


FIG. 4. Comparison of bow values for 50 μm wafer.

A simplified approach to characterize the process induced stress during thinning based on band gap narrowing effect was investigated. The active surface of the wafer was found to be in tensile stress and the stress values are significantly lower than their fracture strength. The difference in stress values between wafers of different thicknesses was correlated with the thinning process and the growth of silicon dioxide on the back surface of the wafer. Nonlinear plate theory based analytical calculations were undertaken to determine the bow at wafer level. The calculated bow for the wafers is in accordance with those from experiments and also with data available for similar process in literature. So, it can be concluded that accurate *I-V* measurements and nonlinear plate theory can be used to approximately calculate the stress and bow in the wafer.

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