# Micro-Transfer-Printing for III-V/Si PICs

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**Abstract:** Micro-transfer-printing ($\mu$TP) enables the intimate integration of a variety of III-V opto-electronic components on silicon photonic integrated circuits (Si PICs). It allows for the scalable manufacturing of complex III-V/Si PICs at low cost. 

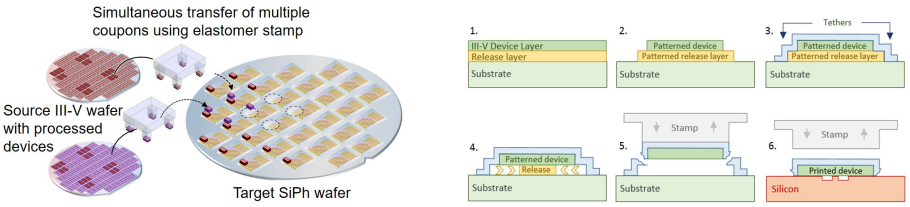
## 1. Introduction

Silicon photonics (SiPh) has the advantages of CMOS compatibility, small footprint, low cost, etc. over other photonic integration platforms. By leveraging the well established CMOS infrastructure and mature fabrication processes, complex Si PICs can be produced in high volume on 200 mm or 300 mm wafers. Following a rapid development over the last two decades, the performance of the key components is significantly improved and the integrated functionalities become more diverse. The increasingly maturing of SiPh technology enables Si PICs to serve a wide range of application fields, including telecommunication [3], gas and biomedical sensing [1,2], signal processing [5], computing [4], etc. However, the absence of wafer-scale realized on-chip optical gain elements and light sources remains an obstacle for the proliferation of SiPh due to the costly assembly processes that are used today for the integration of III-V devices on the SiPh platform. Amongst the explored methods, pick-and-place micro-assembly is the most mature solution, which allows for the pre-fabrication and pre-testing of the III-V standalone devices prior to the assembly process, however the required active alignment and sequential assembly process is time-consuming and costly. Flip-chip technology is the other widely adopted solution, but it has similar drawbacks. Die-to-wafer and wafer-to-wafer bonding has the potential for scalable integration of III-V devices on a SiPh platform. A milestone has been made by Intel, who released the first 100G transceiver with integrated III-V-on-Si lasers in 2016. The laser integration is realized through a multi-die-to-wafer bonding step after the silicon front-end processing, followed by III-V post-processing and back-end processing on the silicon wafer. However substantial modification of the back-end process flow is required to accommodate the thick III-V epitaxial layer stack. The monolithic integration of III-V semiconductors on the Si substrate through hetero-epitaxial growth is considered to be the ultimate solution, as it allows for intimate and wafer-scale integration of III-V semiconductors. Although significant progress has been made in recent years, it is still in an early stage and many issues still need to be overcome. Micro-transfer-printing is a new player in the field of III-V-on-Si PICs. It combines the advantages of die-to-wafer bonding (high throughput) and flip-chip integration (pre-fabrication and pre-testing of the devices prior to their integration). It does not affect the SiPh back-end process flow, showing great potential in the heterogeneous integration of sub-millimeter III-V opto-electronic components on SiPh platforms. In this paper we discuss micro-transfer-printed III-V opto-electronic devices on different SiPh platforms.

## 2. Micro-transfer-printing process

The concept of $\mu$TP is schematically depicted in Fig. 1. A patterned polydimethylsiloxane (PDMS) stamp with a single (or multiple posts) is used to pick-up one (or an array of) pre-fabricated device(s) from the III-V source wafer. In the transfer printing process, the device (device array) can be aligned to the target PIC with sub-micrometer alignment accuracy. As shown in Fig. 1(a), this approach also allows for the intimate co-integration of different III-V opto-electronic devices on a single SiPh chip. To enable the transfer-printing of the III-V devics, a sacrificial layer which can be selectively etched is incorporated underneath the device layer stack. InAlAs

is found to be the best release material for the InP material system. As depicted in Fig. 1(a), the preparation of the source wafer starts with the patterning of the device layer to fabricate the devices of interest in dense arrays, followed by an etch of the release layer down to the substrate. These devices are then covered by a photoresist (or a dielectric) layer, which is then patterned in a way that the devices are encapsulated and at the same time a set of tether structures are defined to anchor the devices onto its native substrate during and after the following release etch. After the release etch, the devices are ready for the transfer printing process. By arranging the III-V opto-electronic devices on the source wafer in dense arrays, the efficiency of the use of expensive III-V materials is significantly improved and very simple post-printing processes are needed to finalize the integration. Fig. 2 shows the microscope images of pre-fabricated III-V photodetectors (PDs) and SOAs on the native substrates.




(a) (b)

Fig. 1. (a) The $\mu$TP process for the integration of III-V devices on a silicon photonic wafer in a parallel manner.(b) Prefabrication of III-V devices on the source wafer and the transfer printing operation.

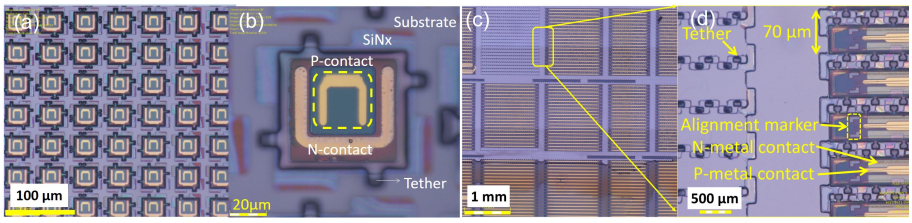



Fig. 2. Microscope images of (a) a pre-fabricated PD array on III-V source wafer, (b) a zoom-in image of a single PD on the source wafer, (c) microscope image of a pre-fabricated SOA array on the III-V source wafer (d) a zoom-in image of the SOA array showing the SOA coupon design.

## 3. Micro-transfer printing of III-V opto-electronic devices onto SiPh PICs

$\mu$TP of a variety of III-V PDs on different SiPh platforms have been investigated. Fig. 3(a) shows an array of transfer-printed C-band III-V PDs on passive Si PICs. A PDMS stamp with 4 posts was used in this process. The responsivity of the resulting devices is around 0.45 A/W at 1550 nm and the printing yield is demonstrated to be 98.8%. Fig. 3(b) shows a transceiver array with transfer-printed O-band III-V PDs realized on the imec iSiPP25G platform. These III-V PDs were sequentially transfer-printed on the target C-band grating couplers. 10 Gbit/s bidirectional data back-to-back operation was demonstrated using this PIC. The $\mu$TP of GaAs PDs (in the NIR) on SiN PICs was also demonstrated, including GaAs metal-semiconductor-metal photoconductors (Fig. 3(c)) and GaAs p-i-n PDs (Fig. 3(d)).

On the other hand, $\mu$TP of III-V SOAs has also been demonstrated (Fig. 4). Fig. 4(a) shows an array of transfer-printed C-Band SOAs, which exhibit up to 17 dB small signal gain and 15 mW output saturation power. Fig. 4(b) shows a transfer-printed C-band Fabry-Pérot laser on a Si PIC, butted coupled to 220 nm thick Si waveguides through a trident spot-size converter. More evanescently coupled III-V-on-Si integrated lasers were realized on 400 nm Si PICs, including widely tunable lasers (Fig. 4(c)), DBR lasers (Fig. 4(d)) and DFB lasers (Fig. 4(e)). Single mode operation was obtained for all these demonstrated devices. The tunable lasers exhibited over 40 nm tuning range in the C-band and mW-level waveguide-coupled output power. The maximum waveguide coupled output power of the DBR and DFB lasers are 6 mW and 3.5 mW, respectively. $\mu$TP of amplifiers/lasers on SiN PICs was investigated recently. A thin amorphous silicon (a-Si) layer is incorporated between the III-V and SiN device layer to allow for an efficient optical mode coupling between the III-V layer and the SiN waveguide. Over

13 dB on chip gain was demonstrated for the III-V-on-a-Si/SiN SOAs. Fig. 4(f) shows a microscope image of a transfer-printed SOA on a SiN waveguide circuit.

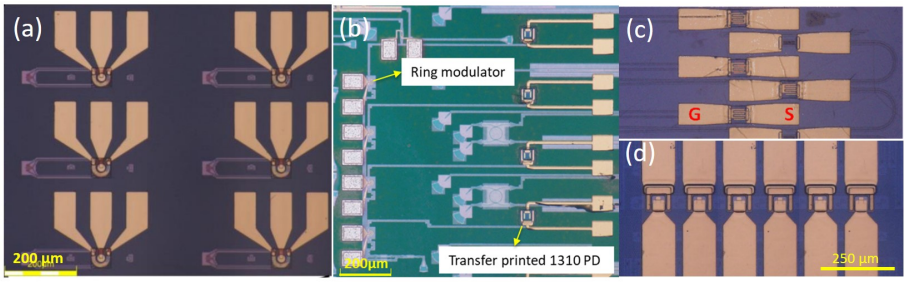



Fig. 3. Microscope images of different types of micro-transfer-printed PDs on different photonics platforms.(a) C-band III-V-on-Si PD array on a 220 nm thick Si PIC; (b) O-Band III-V PD array on an imec iSiPP50G PIC; (c) GaAs MSM PDs and (d) GaAs p-i-n PD array on a SiN PIC.

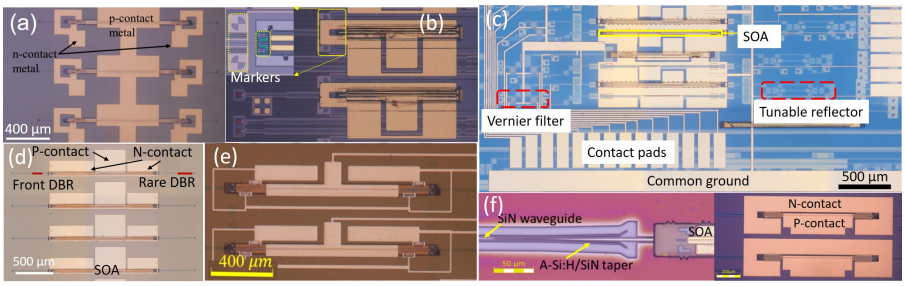



Fig. 4. Microscope images of micro-transfer-printed C-band SOAs and lasers on different photonic platforms. (a) III-V-on-Si SOAs on a 400 nm thick Si PIC; (b) III-V Fabry-Pérot lasers on a 220 nm thick Si PIC; (c)-(d)-(f) Widely tunable lasers, III-V-on-Si DBR lasers and DFB lasers on a 400 nm Si PIC and (f) III-V-on-a-Si/SiN SOAs.

## 4. Conclusions and Acknowledgements

$\mu$TP is a young technology, whereas it exhibits enormous potential for heterogeneous integration of non-inherent functionalities and materials on SiPh PICs. In this paper we summarized a variety of transfer printed III-V opto-electronic components on different target SiPh platforms, which showcase that complex PICs that can be realized using $\mu$TP technology.

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