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Coláiste na hOllscoile Corcaigh

Chapter 16

Carbon Nanotube Composites for Electronic Interconnect Applications

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Additional information is available at the end of the chapter

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1. Introduction

1.1. Electronic interconnect

In the electronics industry interconnect is defined as a conductive connection between two or more circuit elements. The interconnect connects elements (transistor, resistors, etc.) on an integrated circuit or between components on a printed circuit board. The main function of the interconnect is to contact the junctions and gates between device cells and input/output (I/O) signal pads. These functions require specific material properties. For performance or speed, the metallization structure should have low resistance and capacitance. For reliability, it is important to have the capability of carrying high current density, stability against thermal annealing, resistance against corrosion and good mechanical properties.

Over the past 40 years the continuous improvements in microcircuit density and performance predicted by Moore's Law has led to reduced interconnect dimensions. According to Moore's law the number of transistors incorporated in a chip will approximately double every 18-24 months. The interconnect length increases with each generation, leading to higher resistances, while the distance between the adjacent interconnects decreases, leading to increase capacitance. Previously Al interconnect was used for VLSI processing [1]. Al and its alloys, suffer from the problems of high resistance-capacitance (RC) delay (a "time-delay" between the input and output, when a signal or voltage is applied to a circuit), poor electromigration resistance and poor mechanical properties for application in ultra-large-scale integrated (ULSI) circuits [2].

Table 1 shows the comparison of different metals resistivity at room temperature. It can be seen from the table that only three metals have lower resistivity than Al, namely Ag, Au and Cu. Ag has the lowest resistivity but it has poor electromigration reliability. Electromigra-

tion is the transport of material caused by the gradual movement of the ions in a conductor due to the momentum transfer between conducting electrons and diffusing metal atoms. The resistivity of Cu is 1.67 μΩ.cm, which is about 40% better than Al. The self-diffusivity (the spontaneous movement of an atom to a new site in a crystal of its own species) of Cu is also the smallest among the four metals, resulting in improved reliability [3, 4].

Metal	Bulk resistivity μΩ.cm
Ag	1.63
Cu	1.67
Au	2.35
Al	2.67
W	5.65

Table 1. Comparison of the bulk resistivity for different metals.

Table 2 shows a comparison of the activation energy (the minimum energy required for movement of an atom from a lattice position in a crystal) and melting temperature of Al vs. Cu. It can be seen from this table that Cu is a more reliable metal than Al with more energy required for diffusion of Cu atoms. The reason that Cu had not been used much earlier than its introduction in 1997 was because of device reliability concerns and processing difficulties. Cu diffuses rapidly through SiO_2 in the presence of an electric field [5]. This causes degradation of transistor reliability by increasing metallic impurity levels in the Si. Another problem with Cu is that it oxidises at low temperatures but without self-passivation [6]. Cu is also difficult to etch unlike Al. This means that the classical approach where metal is deposited over the entire surface, structures created in the metal and finally infilled with dielectric (oxide) cannot be followed with Cu.

Interconnect Metal	Melting Point °C	Ea for lattice diffusion eV	Ea for grain boundary diffusion eV
Al	660	1.4	0.4 – 0.8
Cu	1083	2.2	0.7 – 1.2

Table 2. Comparison of the active energy for diffusion of Al vs. Cu.

To overcome the problems of Cu integration the inter-level dielectric (ILD) is first deposited and patterned to define "trenches" into which the metal lines of the interconnect will be placed. A thin layer of barrier material (typically refractory metals or their alloys) is deposited generally using a physical vapour deposition (PVD) process. This layer covers the entire surface to act as a barrier to Cu diffusion. After the deposition of the barrier layer the Cu

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interconnect is deposited. This can be achieved by conventional methods such as physical vapour deposition (PVD) [7] and chemical vapour deposition (CVD) [8]. However, PVD presents poor step coverage in sub-micrometer dimension vias and trenches. This technique deposits blanket films which would require further patterning. CVD also requires the use of combustible and toxic precursors at elevated temperatures which has limited the development of Cu deposition by CVD. In 1997 IBM developed the electrodeposition technique (dual damascene) for Cu metallization [9]. Electrodeposition has become the standard method for Cu metallization with demonstrated uniformity, gap filling ability and low processing temperatures. In the dual damascene technique, lines and vias can be filled with electrodeposited Cu at the same time. Fig. 1 shows a schematic diagram of via filling with Cu and the requirement to achieve superfilling or bottom up deposition through the use of suitable additives in the plating bath rather than subconformal or conformal which result in voids or seams in the Cu. [10-12].

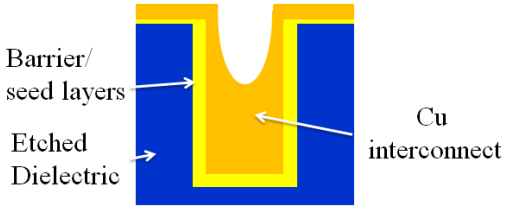

Figure 1. Cross section schematic of interconnect trench or via showing 'super-filling' or 'bottom-up filling' of features through the use of specific plating bath additives for optimum void-free profile evolution in damascene processing [9].

Semiconductor manufacturers have adopted the electroplating technique for Cu interconnect deposition in electronic devices and continue to work on miniaturization of device and feature sizes. Fig. 2 shows cross-sections from the International Technology Roadmap for Semiconductors (ITRS) of a typical microprocessor and application specific integrated circuit where the interconnect of different lines and vias between two adjacent layers are filled with Cu. As the feature sizes decrease and consequently the operating currents increase, electromigration becomes a serious issue once more [13].

The effect is important in applications where high direct current densities are used, such as in high performance processors. Grain boundaries are the fastest diffusion path for Al electromigration (activation energy 0.6 eV for grain boundary diffusion and 1 eV for interface diffusion) but an interface is the fastest diffusion path for Cu (activation energy 1.2 eV for grain boundary diffusion and 0.7 eV for interface diffusion) [14, 15]. The difference in electromigration mechanism drives different focus areas for Cu and Al reliability improvement. The damascene process requires the removal of overdeposited Cu by chemical mechanical polishing (CMP). The CMP produced top Cu surface is the fast Cu diffusion path which needs to be reliably capped. A nonconductive barrier layer is generally applied as the cap layer (silicon nitride, silicon carbide, nitride silicon carbide etc) is used to cover the top surface of the Cu line. However, there are some issues with using dielectric caps to passivate

Cu. As devices become smaller, the current density through the interconnect increases leading to the requirement for better electromigration resistance. The dielectric cap generally has a higher dielectric constant than the interlevel dielectric, resulting in an increase in line-to-line capacitance. Improved Cu electromigration resistance was reported when Cu lines were protected with thin conductive surface capping layers of self-aligned electrolessly deposited CoWP or CoSnP etc [16, 17]. Diffusion barrier layers such as Ta or TaN for Cu metallization act as redundant layers for current shunting as well as for uniform Cu seed deposition. It was reported that Cu vias are the weak link in the interconnect metallization [14]. The Cu via connects directly to the Cu metal below. If a void forms in the Cu underneath the via, there is no redundant layer available for current shunting. This is the primary cause of early failure distribution in Cu interconnects. For the 22 nm technology node or below, the interconnect metal should have current carrying capability of more than 10^7 A/cm^2 to overcome the electromigration issue but Cu is limited to 10^7 A/cm^2.

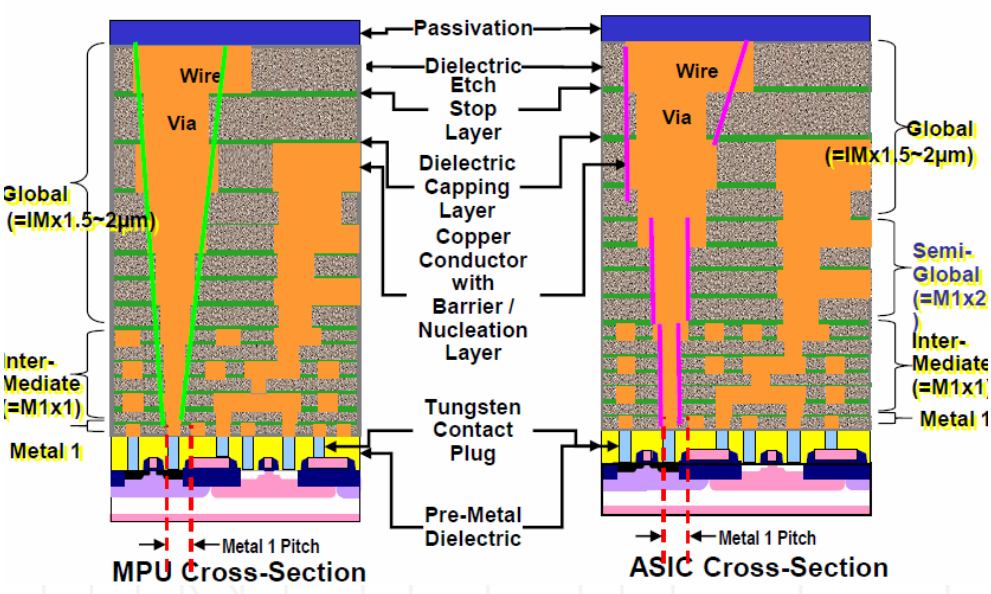

Figure 2. Typical cross section illustrating hierarchical scaling methodology [ITRS technology road map, 2011 update].

1.2. Carbon nanotubes

Carbon nanotubes (CNTs) have unique electrical, thermal and mechanical properties [18]. They can carry an electrical current density of ~ 4×10^9 A cm^{-2}, which is three orders of magnitude higher than Cu [19]. CNT's have high aspect ratio and the mean free path of the carriers (or the probability of an electron transmitted from at one end of the CNT to the other without phonon scattering or other thermal effects) in the CNT at 10 µm is much longer

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than any metal (e.g. 40 nm for Cu). In addition the covalent C-C bonding between the neighbouring atoms in the CNT is one of the strongest bonds reported in the literature [20] and C atoms will not migrate even under very high current density (activation energy 7.7 eV for atom movement). Thus the electromigration resistance of CNT is much better than other interconnects material such as Al and Cu. Because of these advantages over Cu, CNTs require consideration as the next generation interconnect material for specific applications, such as through silicon vias (TSV) for stacked die.

However there are still significant scientific and engineering challenges to incorporate CNTs in devices. CNTs can deposit inside of vias on suitable catalyst like zeolite [21]. It is necessary to ensure the selective growth of metallic CNTs in vias and lines to achieve better electrical conductivity. Alternatively CNTs can be first synthesized in a powder form and metallic CNTs separated from bulk growth CNTs (mixture of metallic and semiconducting). After that metallic CNTs would need to be transferred onto specific wafer locations. The scale of this task is obvious when considering that there are billions of transistors in a microprocessor and the placement of CNTs inside of all vias and trenches on the wafer is unlikely.

	Single CNT	**Cu at 22 nm node**
Maximum Current density (A/cm^2)	1 x 10^9	1 x 10^7
Electrical conductivity (S/m)	10^6-10^7	6 x 10^7
Thermal coefficient of resistivity (/^{o}C)	-1.5 x 10^{-3}	4 x 10^{-3}
Thermal conductivity (W/m K)	6,000	400
Coefficient of thermal expansion (ppm/^{o}C)	-1.5	17
Activation energy (eV)	7	2

Table 3. Comparison of the properties of single walled CNTs vs. Cu.

The contact resistance between CNTs and metal is large (≥1 kΩ). The minimum resistance for a ballistic single-walled CNT is ~ 6.5 kΩ, Therefore, relatively dense arrays of nanotubes will be needed to replace Cu interconnects and these arrays will still only show reduced resistance by comparison with Cu interconnect for line lengths ≥ 1 μm. The ITRS [22] therefore predicts for the 22 nm node an estimated resistance for a 17 nm x 38.5 nm x 1.5 μm Cu interconnect is R_{Cu} 145 Ω. An ensemble of ~ 45, 1 nm diameter defect-free metallic CNTs with mean inter-tube separations ~ 4 nm in a trench of these dimensions would have the same total resistance as the Cu line.

Intrinsic voids between CNTs significantly reduce the electrical and thermal conductivity and bring reliability challenges for the use of CNTs as interconnects. Contact resistance between CNTs and interconnect metal like Cu becomes the dominant source of electrical and thermal resistance which significantly reduces the benefits of CNTs. The potential use of CNTs alone as interconnect in semiconductor manufacturing is still open to debate at this time.

1.3. Metal CNT composites

To overcome some of the interconnect issues described above metal-CNT composites can be an alternative candidate material for future interconnects. The composite material would increase the contact area between vias and interconnect lines. There is also less chance of intrinsic voids between CNTs as they would be metal filled. Among the different metals Cu is the best choice at this moment to use as a composite material with CNTs for interconnects applications because of superior electrical and thermal conductivity. Chai et al [23,24] and Yoo et al [25] reported that Cu fills the voids between neighbouring CNTs which results in a more densely packed structure. They reported that the addition of Cu increases the contact area between the nanotube (1 D) and the substrate (3 D contact) making it a mechanically strong material that can sustain high electrical or thermal stress cycling. To obtain superior properties of metal-CNT composites, it is necessary to achieve a homogeneous dispersion of CNT throughout the metal matrix. It is also necessary that the composites should be void free to obtain better electrical and thermal conductivity.

Cu/CNT composites can be prepared by powder metallurgy, electroless plating or electrodeposition techniques [25, 26]. Among these methods electrochemical routes are relatively straightfoward methods to produce defect free nanocomposites [24, 25]. Powder metallurgy requires sintering at elevated temperatures that may damage CNT's and the difficulty of composite placement remains an issue. Chen et al [26] observed a clear separation of CNTs and Cu matrix composites deposited by powder metallurgy. To achieve optimum performance, CNTs need to be well-dispersed and aligned parallel rather than randomly oriented in the Cu matrix. Hjortstam et al [27] estimated the increase of effective conductivity as a function of the volume fraction of CNT in a Cu matrix. Their calculation showed that 30-40% CNT is needed in the composite with a resistivity 50% lower than for Cu. Liu et al [28] found that electrical sheet resistance is lower in Cu/CNT composite films than Cu and also decreases due to annealing at 200 - 300ºC.

Improved electromigration resistance is expected to result from the location of the alloy element at grain boundaries to prevent movement of Cu at those vulnerable points, which may lead to wiring voids (opens) or hillocks (shorts) during operation [25]. Cu/CNT composites may also improve thermal conductivity of lines and vias which also increases electromigration resistance. Chai et al [24] reported that the Cu/CNT composite vias have lower electrical resistance than that of vias with CNT only. Their electromigration test results showed that the void growth rate for a Cu/CNT composite strip was four times lower than that of pure Cu strip. Their electromigration test of Cu and Cu/CNT composites which were carried out in the temperature range of 100 to 250ºC and current density from 5×10^5 to 2×10^6 A/cm^2 using a conventional Blech-Kinsborn test structure showed that longer strips had larger void length, while no void formation was detected in the strips below 40 μm. Below the critical length the electromigration flux is balanced by the opposing backflow generated by the stress gradient in the test strip.

Yoo et al [25] fabricated Cu/MWCNT composite films by a pulsed electrodeposition technique with additives and obtained a dense structure without any voids. Their microstructure analysis showed that most of the MWCNTs exist at the Cu grain boundaries and cross-linked

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each other. They reported that C content in the composite increased by increasing CNT concentration in the bath but it decreased with annealing. Chai [29] et al reported that the mechanical strength of Cu/CNT nanocomposite was three times higher than that of pure Cu. Chen et al [26] observed good interfacial bonding between CNT and Cu when the nanocomposites were codeposited by electrodeposition. They reported that for Cu/SWCNT nanocomposites, the radial breathing mode (RBM) in the Raman was absent and the tangential or G-band had shifted and widened. Recently several patents on the metal/CNT composites codeposited by electrodeposition have been filed [30-32]. The comparison of electrical resistivity of Cu and Cu/SWCNT film which was reported by Chan [30] are shown in table 4.

	electrodeposited Cu (thickness = 10.5 μm)	**Cu/CNT composite (thickness = 22 μm)**
Resistivity (μΩ.cm)	1.72	1.22
Sheet resistance (mΩ/sq)	1.64	0.56

Table 4. Comparison of the electrical resistivity of electrodeposited Cu/SWCNT composite film vs. Cu alone [30].

1.4. Chlorosulphonic acid for CNT dissolution

Recently Davis et al [33] reported that CNTs can dissolve spontaneously in chlorosulphonic acid solution up to 0.5 wt % [5 g/l], which is much higher than previously reported in other acids (up to 80 mg/l). They reported that at higher concentrations, they form liquid-crystal phases that can be processed into fibres and sheets of controlled morphology. Their proposed phase diagram helps to identify the optimal starting fluid composition and determine micro and macrostructure of fibres and films such as plated fibres, straight fibres and smooth films. Plated fibres have potential application for hydrogen storage and sensors because of high surface area. Straight fibres are of interest for structural reinforcement and smooth, dense films for electrical applications such as electrically conductive thin films.

1.5. Purification and functionalization of carbon nanotubes

A significant problem in dealing with CNTs is the difficulty to separate them as the individual CNTs form bundles due to van der Waals attractive forces. Also in all of the synthesis techniques several impurities like catalyst particles, amorphous carbon etc. are also present in the bundles of CNTs. These impurities may deteriorate the properties of CNTs. To prepare stable and homogeneous dispersions of CNTs considerable efforts have been made [34-39] but the solubility of CNTs in water or organic solvent is relatively low. At room temperature the solubility of CNTs is in the range of 60 to 80 mg/l [34]. In order to achieve better stabilization, CNTs require additional hydrophilic groups directly on the CNT walls or provided by surfactant molecules to impart ionic charge on the CNTs [40-42]. The most common hydrophilic groups are –OH-, -COOH-, -SO_3-, -NH_2-. Functionalization of CNTs can be an important factor to manipulate the properties of CNTs. With functionalization CNTs mau be more easily separated. Several methods have been suggested for the purification and

functionalization of CNTs mainly based on covalent and noncovalent functionalization. Functionalized CNTs are easily dispersed and highly ionized in contract with water [43].

1.5.1. Covalent functionalization of carbon nanotubes

Several methods have been suggested for covalent functionalization of CNTs. The most common technique is to functionalize CNTs in concentrated acid by refluxing. In this process raw materials are sonicated followed by refluxing at 120-130°C. This process requires long processing times. After cooling at room temperature, the mixture is then centrifuged, leaving a black precipitate and a clear brownish yellow supernatant acid. Ko et al [44] reported that the presence of metal impurities in the MWCNTs is reduced significantly using this method. The purification process usually requires two repeat processing steps. The first step is acid reflux which washes metal catalyst and carbon impurities and the second step is annealing which burns the defective tubes and carbon particles. Ko et al [44] also used a microwave oven technique to purify MWCNTs. Chen and Mitra [45] reported that MWCNTs were less reactive and had lower solubility than the SWNTs. Li and Grennberg [46] also found that microwave heating is highly useful for side wall functionalization of MWCNTs.

Lau et al [47] reported that the electrical conductivity of MWCNTs increased with different functionalization techniques such as oxidation, acid reflux, dry UV-ozonolysis. They explained that the new functionalized groups increase the number of bands near the Fermi level, promoting electron transfer between the carbon atoms. They have claimed that CNT functionalization by UV-ozonolyzed technique significantly increases the electrical conductivity of CNTs. Agarwal et al [48] reported that controlled defect creation could be an attractive strategy to induce an electrical conductivity increase in MWCNTs. They reported that the outermost shell of MWCNTs is semiconducting so it is difficult to make electrical contacts to the inner shells of MWCNTs. Functionalization of CNTs may promote cross-shell bridging via sp^3 bond formation. They proposed that intershell bridging facilitates charge carrier hopping to inner shells which can serve as additional charge carrier transport pathways. Tantang et al [49] also reported that acid treatment increases the conductivity of CNT electrodes.

1.5.2. Non-covalent functionalization of carbon nanotubes

Covalent functionalization may deteriorate the unique ionic properties of CNTs by the formation of new covalent bonds on the CNTs wall. To overcome this disadvantage non-covalent functionalization mainly based on polymer surfactant interaction was developed that can disperse nanotubes easily but not degrade the CNT's unique properties [50]. The proposed mechanism for this solubilisaiton is through an individual CNT being wrapped by the polymer which acts as a surfactant in the solution to achieve separation. A surfactant is a wetting agent which lowers surface tension of liquids. It is usually an organic compound that contains both hydrophobic and hydrophilic groups. As a result, they are soluble both in organic solvents and water. Surfactants are classified based on the presence of a charged group. The head of an ionic surfactant carries a net charge. If the charge is negative, the surfactant is more specifically called anionic; if the charge is positive, it is cationic. Ionic surfac-

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tants not only separate individual CNTs but also carry charge to the surface of CNTs so that the CNTs can be codeposited with Cu by electrodeposition. Examples of surfactants which have been investigated are given below.

1. Nafion® as a surfactant

In our study we primarily used nafion, a polymer surfactant for the dispersion of CNT bundles. It is a sulfonated tetrafluorethylene co-polymer with ionic properties which bears a polar side chain (-SO_3H) and hydrophobic backbone (-CF_2-CF_2). It has unique ionic properties because of the incorporation of perfluorovinyl ether groups terminated with sulfonate groups onto a tetrafluoroethylene (Teflon) backbone. The hydrophobic backbone strongly anchors to the hydrophobic side-wall of CNTs. On the other hand the polar side-chain of the polymer imparts sufficient ionic charge to the CNT surface which enhances the solubility of CNTs in liquid solvents. Fig. 3 shows the chemical structure of nafion.

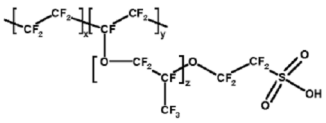

Figure 3. Chemical structure of Nafion.

2. CTAB as a surfactant

Cetyl trimethyl ammonium bromide (CTAB) is a cationic surfactant. Chen et al [51, 52] used CTAB for the dispersion of CNTs to prepare CNTs/Ni composites by an electroless deposition technique. The chemical structure of CTAB is shown in fig. 4 (a). As a cationic surfactant it can make the CNT surface positively charged to assist the codeposition of CNT on the cathodic surface [52]. The CNT with negative charge readily adsorbs the cationic surfactant. This adsorption develops a net positive charge on the CNT, which prevents them from agglomerating and leads to electrostatic attraction to the cathode surface with negative potential [51]. The net positive charge on the CNT increases the amount of CNT in the deposits. To calculate the volume fraction of CNTs, they dissolved the deposits in nitric acid. The CNTs in the deposits were filtered and the quantity of the CNTs in the deposits determined [52]. They reported that the content of CNTs in the deposit increases with an increase of CNT concentration in the bath, up to a maximum value at the CNT concentration of 1.1 g/l and then decreases. They explained this as a result of the CNT agglomeration in solution at higher concentration which reduces the content of CNT in the deposit. They also reported that the saturation concentration increases with decrease of length of CNTs because the longer CNTs tend to agglomerate more readily.

3. SDS as a surfactant

Sodium dodecyl sulfate (SDS) is an anionic surfactant used to improve the surface uniformity of the composite deposit [53]. The chemical structure of SDS is shown in fig. 4 (b).

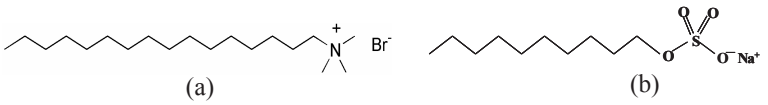

Figure 4. Chemical structure of (a) CTAB and (b) SDS.

A comparison of hardness and XRD patterns of Ni/CNT composites by using SDS and CTAB surfactant in the bath with Ni was performed [53]. The hardness changes for the composite films and depends on the concentration of CNTs in the bath as well as surfactant. The composite from the CTAB bath showed an increase of hardness unlike that of the composite from the SDS containing bath. It can be also seen from the XRD data that (111) is the preferred plane of Ni when the bath contains CTAB like pure Ni deposition. On the other hand, SDS in the bath reduces the preferred Ni (111) orientation significantly in the composite. A summary of surfactants which are commonly used for the dispersion of CNTs are reported in table 5.

CNT	CNT: g/l	Surfactant	Surfactant: g/l	Composites	References
MW	0.3	CTAB	0.6	Ni/CNT	[53]
MW	0.1	$Mg(NO_3)_2$		Cu/CNT	[26]
MW	6	PA	0.5	Cu/CNT	[23]
SW	3	CTAC	3	Cu/CNT	[54]
MW	1	CTAB	4	Cu/Zn	[55]
SW	0.002	Nafion	0.4	Nafion/CNT	[56]
MW	0.6	Gelatine	0.4	CNT/Cu	[57]
MW	2	CTAB		Ni/CNT	[58]
SW	2			Cu/CNT	[24]
MW	1	Nafion	0.01	Nafion/CNT	[59]
MW	6	PA	0.1	Cu/CNT	[60]
MW	1			Ni-Co/CNT	[61]
MW	1	Nafion	5	Nafion/CNT film	[62]
SW	0.2	Nafion		Nafion/CNT	[63]
SW	0.05	SDS	0.1	PVP/CNT	[50]

Table 5. Literature review of CNT dispersion surfactants.

1.6. Analysis of carbon nanotubes in deposit

There is very little in the literature on quantifying CNT content in the deposits [48, 51, 52]. Arai et al [60, 64, 65] measured the content of multi-walled CNTs in the electrodeposited

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composite film by dissolving the deposit in hot nitric acid. The CNTs in the nitric acid solution were filtered, dried and weighed. Osaka et al [66] reported the carbon content in the deposit was analyzed by the combustion infrared absorption method (CS 444, LECO) as this element analyzer is capable of analysing for carbon. The summary of CNT content in the deposit obtained from the literature is shown in table 2.5.

Bath	Surfactant	CNT g/l	Weight % CNT in deposit	Reference
Ni	PA	6	Up to 1	[64]
Cu	PA	2	0.4	[60]
Ni	SDS	0.3	Up to 7	[53]
Cu	PA	Up to 6	Up to 2.5	[25]

Table 6. Literature data of CNT content in the plating bath and deposit.

2. Cu and Cu/CNT pillars for flip chip interconnect assembly

Historically, IC chips have been electrically connected to the substrate by a wire bond method. In this method, the chip faces up and is attached to the package via wires. This connection has limited electrical performance and reliability problems in addition to requiring pad location at the edge of the die. Flip chip, also known as 'Controlled Collapse Chip Connection, C4', replaced the traditional wire bond method. In this method, solder bumps are deposited on the chip pads over the full area of the top side of the wafer during the final wafer processing step. In order to mount the chip to external circuitry (e.g., a circuit board or another chip or wafer), it is flipped over so that its top side faces down, aligned to the substrate and then the solder is reflowed to complete the interconnect. Generally, Sn-Pb based solder bumps have been used in flip chip packaging to connect chips to external circuitry. According to the International Technology Roadmap for Semiconductors the total number of I/Os will reach up to 10,000 cm^2 chip area by 2014 which require finer interconnect with a pitch size less than 20 μm. To fabricate such fine pitch interconnect, conventional solder bump requires fine solder deposition or paste particle which are not readily available [67]. It is also important to reduce lead-based solders for environmental concerns (RoHS compliance). As circuit density increases, devices are also more vulnerable to non-uniform thermal distribution.

Cu has higher thermal conductivity than most binary or ternary solders. Cu bumps in flip chip assembly offer increased reliability, extended temperature range capability, greater mechanical strength, higher connection density, improved manufacturability, better electrical and heat dissipating performance over Pb-Sn solder. It is also less expensive and decreases the amount of solder needed to create bumps. Cu pillars do not change shape during reflow so they do not encounter any volumetric redistribution which can lead to voids in the sol-

der. Because of these advantages the semiconductor industry is adopting Cu pillar bump by electrodeposition for flip-chip attachment to replace the typical Pb solder [67, 68]. Power and thermal non-uniformity in devices are increasing steadily with each new device generation leading to serious concerns for the industry regarding thermal issues. Mechanical stress on Cu bumps generated by the difference in thermal expansion coefficients between the chip and the substrate materials can lead to device failures. This differential thermal expansion also creates shearing forces at the bump. As a result bumps are most vulnerable to damage. Repeated thermal expansion and contraction leads to fatigue cracking of the bump.

Cu/CNT composites could be a suitable candidate material to resolve these issues for next generation flip chip assembly. CNTs have high mechanical strength (10-60 GPa, c.f. Cu 70 MPa) and thermal conductivity (>3000 W/m.K, c.f. Cu 400 W/m.K) which may alleviate the issues related to die degradation and non-uniform temperature distribution in the pillars. CNTs have a negative temperature coefficient of resistivity (- 1.5 $x10^{-3}$/ºC, c.f. Cu + 4 $x10^{-3}$/ºC) and low coefficient of thermal expansion (- 1.5 ppm/ºC, c.f. Cu + 17 ppm/ºC) which can make the Cu/CNT composites material more reliable against thermal cycling and fatigue with less risk of stress induced failure. Typical photolithography techniques can be utilised to fabricate Cu/CNT pillar bumps on chip. Arai et al [64] recently demonstrated Cu/CNT pillar emitters deposited by electrodeposition on a patterned substrate.

3. Cu and Cu/CNT in through Si via (TSV) for 3D interconnect

Cu electrodeposition in TSV features is a key component of new 3D integration approaches that are of great interest in the semiconductor industry [69]. 3D integration increases performance and lowers power consumption due to reduced length of electrical connections. Cu has been selected as the TSV interconnect because of its low electrical resistance and compatibility with conventional multilayer interconnection in large-scale integration (LSI) and back-end processes. The key challenges for TSV plating processes are to fill the vias across the entire wafer and to complete the fill as fast as possible to minimize cost. TSV interconnect shortens the interconnect requirements and reduces signal delay. However, it is difficult to fill high aspect ratio vias without voids through conventional damascene electroplating. Perfect filling without voids is required to minimise interconnect failure and reliability issues. TSVs have been extensively studied because of their ability to achieve chip stacking for enhanced system performance. This is a very promising technology that may replace wire bonding in chips or single chip solder bumping. Metal filled TSVs allow devices to be connected using a 3D approach [69]. Cu is the best low cost conductor for TSV interconnect and an extension of the damascene plating in smaller features. Recently enormous attention has been given to bottom up filling of TSVs to fill high aspect ratio vias without voids like conventional damascene electroplating [70-72]. However, there are key issues that need to be resolved, such as process reliability, electrical continuity and thermal management. TSVs should have the ability to maintain operation over a wide range of temperatures and to withstand these temperatures in a cyclic manner. The TSV material proper-

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ties must include mechanical strength, good thermal conductivity and stability with thermal cycling.

The key issues for 3D integration are process reliability, die degradation, electrical continuity, bump to pad electrical contact and thermal management. Temperature cycling and thermal shock accelerate fatigue failures. Also, non-uniform temperature distribution may influence the operation of circuits and sensing elements dramatically. Stress fields resulting from differential thermal expansion of Cu-based TSV may cause serious problems. The reliability problems of high aspect ratio TSV interconnect may be alleviated by the codeposition of carbon nanotubes (CNTs) with Cu as a suitable composite material. CNTs have high mechanical strength, thermal conductivity and low coefficient of thermal expansion which may alleviate the issues related to die degradation and non-uniform temperature distribution in the TSVs.

4. Experimental methods

In this work the Cu/CNT composites codeposition process was assessed and the deposited materials characterised. Electrochemical analysis of the deposition requires an analysis of the nucleation and growth characteristics for the candidate materials. MWCNTs have been added to the typical Cu sulphate plating bath to achieve homogeneous Cu/MWCNT composites. Here, we will report electrochemical analysis and kinetics of electrodeposited Cu when MWCNTs were present in the bath. Solubilisation or suspension of the CNTs in the Cu bath is also a key requirement. Composite plating bath chemistries for Cu/CNT deposition were investigated. The influence of typical additives in the Cu bath on the deposit characteristics was determined for optimised electrodeposition in vias and trenches. The influence of different surfactants on the deposition and electrical properties of composite films was also analyzed. Cu and Cu/CNT composites were electrodeposited on planar and structured substrates. Microstructure characterization of the deposit employed scanning electron microscopy (SEM), focussed ion beam microscopy (FIB) and x-ray diffraction (XRD). The sheet resistance of Cu/CNTs film and changes due to self-annealing and high temperature annealing were monitored by 4 point probe resistivity techniques. Cu/CNT composites were also deposited in test structures. After chemical mechanical polishing of the test structures, the line resistance was measured using a Cascade probe station.

The amount of CNTs in the deposit was determined by dissolving the deposit in a concentrate HNO_3 solution. The Cu/CNT films were deposited on 1 cm X 1 cm thin film sputtered Cu on Si. The deposition current was 1 A and deposition time was 1 h. The concentration of CNTs in the bath was 10 or 100 mg/l. After deposition, the sample was dipped in hot concentrate acidic solution (65% HNO_3, 65°C). The diluted acid solution was then vacuum filtered using PTFE filter paper. The filtration process was repeated at least 5 times to ensure all CNTs were left on filter residue. After filtration, the PTFE membrane was dried in an oven at 80°C for at least 30 minutes to ensure the membrane was completely dried. The weight difference of the PTFE membrane before and after filtration gives the amount of

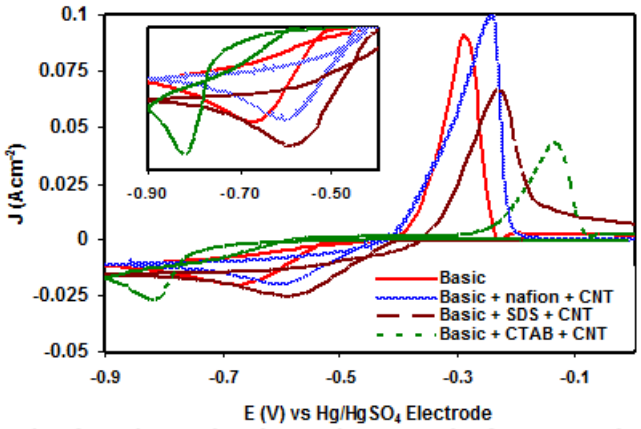

Figure 5. CVs of Cu and Cu/CNTs deposition on a glassy carbon electrode (scan rate: 0.1 V/s) from 0.24 mol dm^{-3} $CuSO_4$ + 1.8 mol dm^{-3} H_2SO_4 with/without CNTs and different surfactants in the bath.

CNTs in the deposit. The amount of CNTs in the deposit was approximately 2% by weight by using long CNTs (length 5-9 μm, diameter 110-170 nm) or short CNTs (length < 1 μm, diameter 9.5 nm) in the bath. The density of CNTs is close to 1.3 gm/cm^3 and pure Cu is 8.89 gm/cm^3 which indicates the CNTs in the deposit are up to 12% by volume.

5. Results

To utilise CNTs as a composite with Cu for interconnect applications it is necessary to verify the influence of the materials on the Cu plating chemistry. Fig. 5 shows the comparison of cyclic voltammetry of Cu and Cu/CNTs co-deposition from a simple $CuSO_4/H_2SO_4$ bath (hereafter referred to as the basic bath) with/without CNTs and surfactant at a scan rate of 0.01 V/s. It can be seen that the addition of CTAB and CNT results in a cathodic peak potential shift to a more negative value which represents a suppression influence on Cu deposition. On the other hand the Cu deposition occurs at lower overpotential when the bath contains either nafion or SDS which represents an acceleration influence. The diffusion coefficient for Cu^{2+} ions estimated from chronoamperometry data using the Cottrel equation in the basic bath (0.24M $CuSO_4$ + 1.8M H_2SO_4) is 4.5 x 10^{-6} cm^2/s. A similar value (4.6 x 10^{-6} cm^2/s) was found from the SDS containing Cu/CNTs bath. Upon addition of nafion or CTAB in the Cu/CNTs bath, the diffusion coefficient value of Cu^{2+} ions slightly increases to 5.1 x 10^{-6} cm^2/s and 5.3 x 10^{-6} cm^2/s, respectively. It is clear that CNTs and surfactants in the Cu bath do not have a significant influence on the diffusion coefficient value of Cu. These results indicate that the CNT + surfactant is compatible with the basic Cu sulphate/sulphuric acid bath chemistry. An assessment of the influence of the composite materials on baths that contain the basic constituents and the necessary additives to achieve bottom-up fill or superfilling of interconnect features in silicon technology is also required.

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The kinetics of the metal nucleation and growth/dissolution can be analysed with a rotating disk electrode system. While acknowleding the limitations and complications in the kinetic analysis of Cu [12] the general trends indicated in the data are consistent with published data for the Cu sulphate system and those with typical damascene additives. It can be seen from the kinetic data analysis below that the exchange current density, i_0, for Cu nucleation and growth from the basic $CuSO_4$ bath without any additive is 7.24 mA/cm^2 and the E_0 value is - 406 mV. The exchange current value for Cu nucleation and growth in the literature varies from 1 to 15 mAcm^{-2} [73–75]. Addition of all typical additives in $CuSO_4$ bath decreases the exchange current density, i_0 for Cu nucleation and growth from 7.24 mA/cm^2 to 1.2 mA/cm^2 and increases the E_0 value from - 406 mV to - 417.5 mV. This result confirms that all additives together have a suppressor effect on Cu deposition. It can be observed that addition of 1% nafion also has a minor suppressor type behaviour on Cu nucleation and growth as it slightly decreases the exchange current density, i_0 from 7.24 mA/cm^2 to 7.07 mA/cm^2 and increases E_0 value from - 406 mV to - 410.5 mV. But addition of CNTs has an accelerator influence on Cu nucleation and growth increasing the exchange current density, i_0 from 7.24 mA/cm^2 to 10.23 mA/cm^2 and decreasing the E_0 value from - 406 mV to - 403.5 mV. It is also observed that all typical additives including nafion and nanotubes together in the solution have an overall suppressor effect on Cu deposition. The summary results are shown in table 7. It can be seen from the table that anodic slopes are in the range from 1/65 mV to 1/76 mV and cathodic slopes are in the range from 1/122 mV to 1/164 which are close to the theoretical values when the reactions are two separate single electron transfer steps. The above results show that baths containing nafion & CNTs are compatible with the existing typical $CuSO_4$ bath used in IC interconnect deposition.

Conditions	1/slope, mV		E_0/mV	I_0/ mAcm^{-2}
	Anode	Cathode		
0.24 M $CuSO_4$ + 1.8 M H_2SO_4 (Basic bath)	154	67	- 406.0	**7.24**
Basic bath + 1% nafion	161	66	- 410.5	**7.07**
Basic bath + 1% nafion + 10 ppm CNTs	164	76	- 403.5	**10.23**
Basic bath + 50 ppm Cl^- + 300 ppm PEG + 1 ppm SPS	151	67	- 417.5	**0.54**
Basic bath + All additives + 1% nafion	128	72	- 420.0	**1.70**
Basic bath + All additives + 1% nafion + 10 ppm CNTs	122	76	- 421.0	1.66

Table 7. Summary of Tafel analysis obtained from rotating disk system.

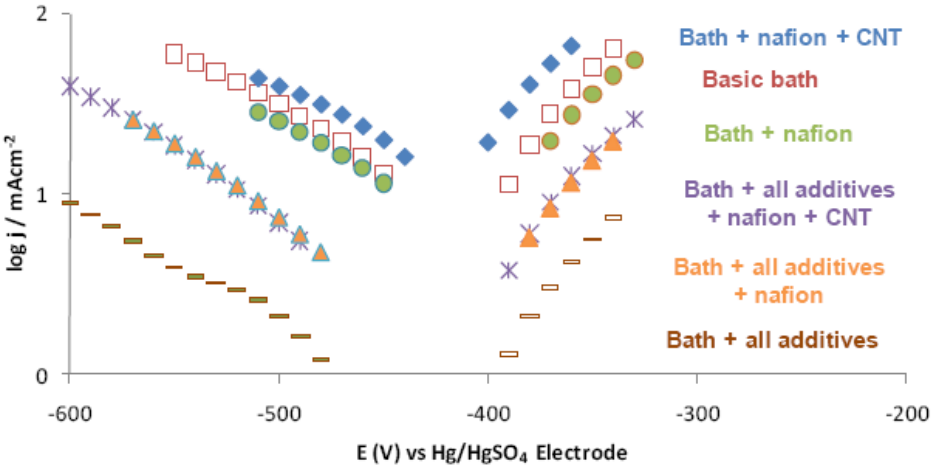

Figure 6. Comparison of Tafel plots for Cu deposition from with/without additives and CNTs in a standard Cu bath using a Cu rotating disk electrode which was rotated at 2000 rpm during experiments (Initial potential: 0 V, scan rate 0.1 V/s). Area of Cu RDE was 12.566 mm^2

On a 1 cm^2 Cu substrate (200 nm sputtered Cu on Si) the deposition current was 15 mA/cm^2 and deposition time was 1 h. The concentration of CNTs in the bath was 100 mg/l. The acid solution was then vacuum filtered using 5 μm PTFE filter paper. The length and diameter of the MWCNTs were 5-9 μm and 110-170 nm respectively. Fig. 7 shows the SEM images of PTFE membrane after filtration of Cu/CNT deposits. The CNTs are clearly observed.

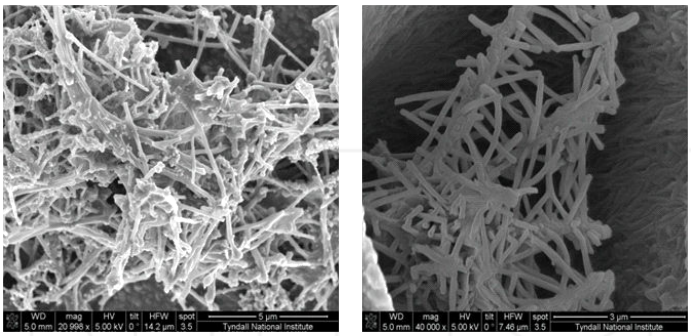

Figure 7. SEM image of CNTs on PTFE membrane after filtration of dissolved Cu/CNT composites. Image magnification 5000X on left and 40000X on right.

The amounts of CNTs in the deposit are shown in table 8 which compares the percentage of CNTs in the deposit when long or short CNTs with different surfactants were added in the bath. We found the percentage of CNTs was slightly higher (CNT content 1.69% by weight) when SDS was added with long CNTs in the bath (CNT content 1.13% by weight when

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CTAB was added). On the other hand, the percentage of CNTs was slightly higher (CNT content 1.64% by weight) when SDS or CTAB was used in the bath with short CNTs in the bath (CNT content 1.12% by weight when nafion was added). It can be seen from the table, the weight percentage of MWCNTs in the deposit was less than 2%. According to the literature [25, 60] the maximum CNT concentration in Cu/CNT composites achieved has been approximately 2.5 % by weight. So the value found in these experiments is quite reasonable. The density of MWCNTs is close to 1.3 g/cm^3 and pure Cu is 8.89 g/cm^3 which indicates that the CNT content in the deposit is up to 12% by volume.

MWCNTs Length μm	MWCNTs Diameter nm	**Surfactant**	**% CNTs**
5 – 9	110 - 170	Nafion	1.12
5 – 9	110 - 170	CTAB	1.64
5 – 9	110 - 170	SDS	1.64
<1	9.5	Nafion	1.56
<1	9.5	CTAB	1.13
<1	9.5	SDS	1.69

Table 8. The weight percentage comparison of CNTs in the composite films using different size of CNTs and surfactants in the bath. PTFE membrane was used for filtration purpose.

The electrical properties of Cu/CNT composites were assessed by determining the resistivity of submicron films. Room temperature self-anneal phenomenon is usually observed in electrodeposited Cu films [76-80]. Due to large grain growth at room temperature and annihilation of the defects (void, vacancy, stacking fault, impurities redistribution etc), the electrical resistivity of Cu may change with time. It is therefore necessary to monitor the resistivity changes of Cu and Cu/CNT composite films over time after electrodeposition. The resistivity of Cu and Cu/CNTs composite films at room temperature was monitored using a four point probe apparatus (Keithley 2400 four point probe). In each case we took 4 samples and recorded the average resistivity. The film was electrodeposited on a sputter Cu coated Si substrate. The deposition current density was 15 mAcm^{-2} and deposition time was 2 minutes. The thickness of film was measured by using surface profilometry to be approximately 660 nm.

The electrical resistivity results showed that at room temperature the resistivity of Cu/CNTs composite films (2.46 μΩ-cm) when nafion was used for the surfactant of CNTs is close to the resistivity of Cu film deposited (2.15 μΩ-cm). The resistivity of Cu/CNTs composite film was higher when SDS (3.03 μΩ-cm) or CTAB (4.19 μΩ-cm) was used as a surfactant. The results are summarised in table 9. There was a larger scatter in the distribution of resistivity data in the CTAB case. This is probably a result of a less uniform and void rich deposit from the CTAB containing bath which significantly increased the resistivity.

The resistivity of samples maintained at room temperature did not change significantly. The summary of the changes of the room temperature resistivity over time for Cu and Cu/CNT

composite films deposited from different surfactant containing baths are shown in table 10. Osaka et al [66] reported that the resistivity of a deposit from an additive free bath and Cl^- + PEG containing bath was unchanged with time. But when SPS was present in the bath, the resistivity decreased over time due to self-annealing. Lee and Park [82] reported that self-annealing is caused by Cu grain boundary diffusion. They mentioned that locally high stress originated from the trapped large molecule PEG which can accelerate grain boundary diffusion of Cu. There is a lack of consensus about the cause of self-annealing [81-86]. Among the suggested possible causes for self-annealing of electrodeposited Cu film are bath compositions [83], additives [77, 81, 82], film thickness [79, 80, 84], barrier layers [86, 87], impurities [79, 85] and deposition current [80].

Bath	Resistivity / μΩ-cm
Basic (0.24 M $CuSO_4$ + 1.8 M H_2SO_4)	2.17
Basic + Nafion + CNT	2.43
Basic + SDS + CNT	3.03
Basic + CTAB + CNT	4.69

Table 9. Comparison of the resistivity of Cu and Cu/CNT composite film at room temperature 1 hour after deposition using different surfactants in the bath.

Bath	Time after deposition / hour	Resistivity / μΩ-cm
Basic	1	2.17
	312	2.15
Basic + Nafion + CNT	1	2.43
	311	2.47
Basic + CTAB + CNT	1	4.09
	313	4.19

Table 10. Comparison of the resistivity changes of Cu and Cu/CNT composite film at room temperature and 311 to 313 hours after deposition.

It is well known that through annealing at higher temperature a reduced defect Cu microstructure can be obtained [76-87]. Cu/CNT composite films (660 nm in thickness) were annealed in nitrogen at 215°C, 265°C and 315°C for 20 minutes. It can be seen that a clear decrease of sample resistivity was observed with increasing annealing temperature which is shown in table 11. The resistivity value of Cu film approaches that of bulk Cu value (1.67 μΩ-cm) after annealing at 315°C for 20 minutes. Also the resistivity of Cu/CNTs composite films decreased with increasing annealing temperature. The electrical resistivity of the Cu/CNTs composite films deposited from a nafion and CTAB containing bath became 1.88 μΩ-

cm and 2.10 μΩ-cm respectively when the sample was annealed at 315 °C. The conductivity increase of the composite films was probably due to a decrease the interface resistance between CNTs and Cu matrix at the higher temperature, grain refinement and elimination of defects under high temperature annealing.

Annealing temperature °C	Basic bath	Resistivity / μΩ-cm Basic + Nafion + CNT	Basic + CTAB + CNT
No anneal	2.15	2.46	4.19
215	1.78	2.14	2.72
265	1.92	2.04	2.45
315	1.67	1.88	2.10

Table 11. Comparison of the resistivity of Cu and Cu/CNT composite films at room temperature and higher temperatures 312 hours after deposition using different surfactants in the bath.

The influence of CNT concentration in the Cu/CNT composite bath was investigated. The electrical resistivity results showed (fig. 8) that at room temperature the resistivity increased 10% when the concentration of CNT in the bath was increased from 10 mg/l to 100 mg/l. This data also shows no evidence of self annealing at room temperature for the composite material.

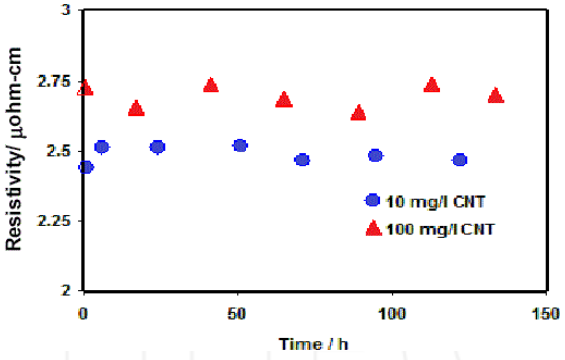

Figure 8. Comparison of the resistivity of Cu/CNT composite film at room temperature over time using 10 mg/l and 100 mg/l CNT in the bath.

It can be seen from fig. 9 that when the samples were annealed at higher temperature up to 315ºC for 20 minutes the resistivity decreased from 2.46 μΩ-cm to 1.89 μΩ-cm for 10 mg/l CNT and 2.7 μΩ-cm to 2.19 μΩ-cm for 100 mg/l CNT in the bath. It is expected that CNT content in the composite is higher when deposited from higher CNT concentration containing bath [25, 60]. The resistivity increase of the higher CNT content bath is probably due to increased CNTs content and higher contact resistance between CNTs and Cu in the composites.

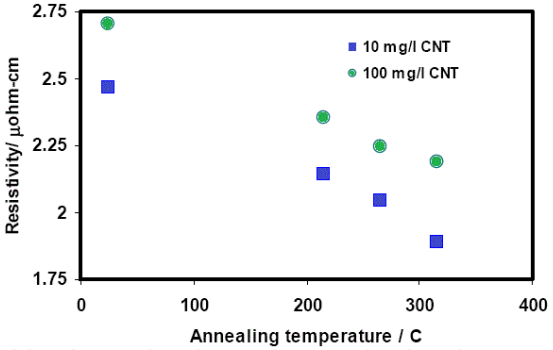

Figure 9. Comparison of the resistivity change of Cu/CNT composite film after annealing for 20 minutes at higher temperature using 10 mg/l and 100 mg/l CNT in the bath.

In summary, the Cu/CNT composites were codeposited with the aid of a surfactants at different current densities. As a comparative study, three surfactants (nafion, CTAB and SDS) were used separately to disperse CNTs in the bath and Cu/CNT composite films were electrodeposited. SDS in the bath results in a smoother deposition whereas CTAB leads to rougher deposition of the composite. The maximum CNT concentration in Cu/CNT composites achieved in our study was approximately 2 % by weight deposited from 100 mg/l CNT containing composite baths. The electrical resistivity results show that at room temperature the resistivity of Cu/MWCNT composite film (2.47 μΩ-cm) is close to the resistivity of Cu film (2.15 μΩ-cm) when nafion was used in the deposition bath for the surfactant of MWCNTs. With the use of CTAB or SDS in the bath, the resistivity of Cu/MWCNT film was higher [deposited from 10 mg/l CNT containing composite baths]. A clear decrease in sample resistivity was observed with increasing annealing temperature. The resistivity also increased when the concentration of MWCNTs was increased from 10 mg/l to 100 mg/l in the bath.

The line resistance of Cu filled and Cu/CNT filled test chip structures was measured using a Cascade probe station. The test chip structure consisted of 110 μm x 80 μm pads connected with metal lines of different widths. A Cu seed (12 nm) and a barrier Ta/TaN (25 nm) were PVD deposited. To achieve a uniform deposit the plated substrates were planarised with a CMP process. The test chip coupon was mounted on a 4 inch Si carrier-wafer. A Logitech CDP51 was used for the CMP. The polishing slurry used was a Cabot Microelectronics product, Eterpol 2362, which was mixed with H_2O_2 (30%), the ratio of H_2O_2 to slurry was 5% by volume. During CMP, the rotation of wafer holder and polishing pad was 50 rpm and the applied pressure was 2-3 psi. Fig. 10 shows the SEM image of the test structure after CMP for 2 minutes. It can be seen that excess deposits were completely removed by the developed CMP process. Before probing, the test sample was vacuum attached in a dedicated holder. Four micro-probes were placed on four pads in the structure. The pads were connected with Cu filled interconnect lines. The Cu was deposited from a damascene additive containing sulphate based bath. Fig. 11 shows the electrical measurement of 110 nm width Cu line in the test structure. It can be seen from the measurement that the I-V curves of Cu

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deposited line was linear and the resistance value was estimated to be 284 Ω which is to be expected for lines of that dimension.

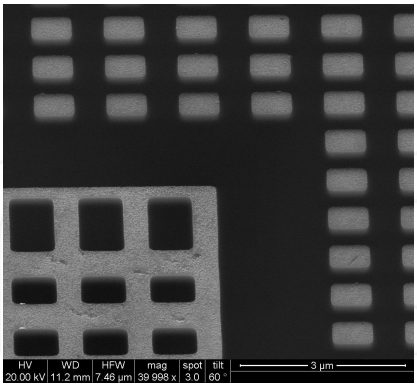

Figure 10. Plan view SEM image of test structure after complete CMP. The structure was filled by electrodeposited Cu (lighter colour in image). Image magnification 40000X.

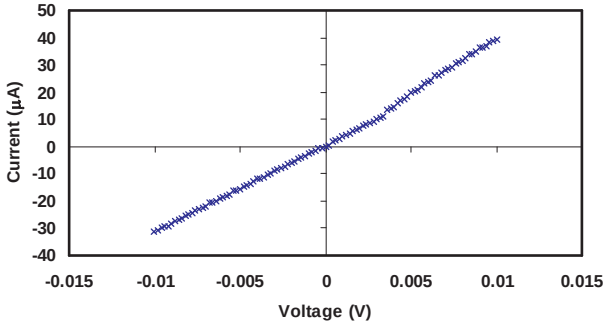

Figure 11. Current vs. voltage curve of the 110 nm line width connected with four 110 µm x 80 µm pads. The features were filled with electrodeposited Cu.

The next samples investigated contained CNTs in the Cu deposited from the nafion containing bath. The concentrations of CNTs and nafion were 50 mg/l and 0.5% respectively. Fig. 12 shows the electrical measurement of 110 nm line width filled with Cu/MWCNT in the test structure. It can be seen from the measurement that the I-V curve of the Cu/MWCNT deposited line was linear and the resistance value was 29.7 kΩ. The resistance of individual MWCNT is hundreds of kΩ (minimum resistance for a ballistic single-walled CNT is ~ 6.5 kΩ). The high resistance of individual CNTs is due to high contact and quantum resistance. Therefore, relatively dense arrays of CNTs will be needed to replace Cu interconnects. As Cu and MWCNTs were codeposited in the narrow line with 110 nm width, so the resistance

in Cu/MWCNT composites is expected to be between the resistance value of Cu (284 Ω) and MWCNT (hundreds kΩ). The resistance of the line filled with Cu/CNTs could be improved by using SWCNT instead of the MWCNTs used in this composite.

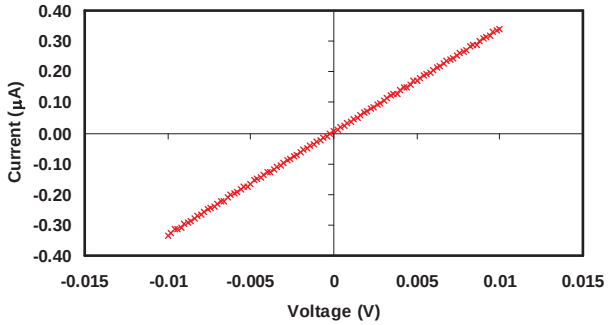

Figure 12. Current vs. voltage curve of the 110 nm line width which was filled with electrodeposited Cu/MWCNT composite. The concentrations of nafion and MWCNTs in the bath were 0.5% and 50 mg/l respectively.

6. Conclusion

In this chapter we have reported the influence of surfactants on the properties of Cu/CNT composites on Si substrates. Cu/CNTs composite films were co-deposited by electrodeposition. Before electrodeposition, CNTs were dispersed by a suitable surfactant. Electrochemical data shows that nafion or SDS accelerates the co-deposition where as CTAB suppresses the deposition. Nafion and SDS surfactants result in a relatively smooth deposit whereas CTAB surfactant leads to rougher deposition of the composite. The amount of CNTs in the deposit was up to 2 % by weight using different surfactants and different length/diameter of CNTs. Our electrical analysis showed that for Cu/CNT composite samples maintained at room temperature, the resistivity over time did not change significantly. The electrical resistivity results also showed that at room temperature the resistivity of the Cu/CNT composites film (2.43 μΩ cm) is close to the resistivity of Cu film (2.17 μΩ cm) when nafion was used in the bath to disperse the CNTs. The resistivity of Cu/CNTs film was higher when CTAB or SDS were used instead of nafion as a surfactant. The electrical resistivity results showed that at room temperature the resistivity increased 10% when the concentration of CNT in the bath was increased from 10 mg/l to 100 mg/l. A clear decrease of sample resistivity of composite films was observed with increasing annealing temperature. Cu/CNT composites deposited at a test structure with submicron lines and vias with Cu/CNT composites was only possible from the nafion surfactant containing damascene. The electrical measurement of 110 nm line width filled with Cu/MWCNT showed that the I-V curves of the Cu/MWCNT deposited line was linear and the resistance value was 29.7 kΩ which was significantly higher that the resistance value of Cu (284 Ω) deposited. Improvements on these val-

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ues will require lower resistance SWCNTs or the improvement of the density of aligned nanotubes in the composite structure. This may be more feasible in larger dimension features such as those required for TSV interconnect at the chip scale rather the use of composites for IC interconnect at deep sub micron dimensions.

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