CORA Cork Open Research Archive
Cartlann Taighde Oscailte Chorcaí

Title	Hardware reduction in digital delta-sigma modulators via error masking - part II: SQ-DDSM
Authors	Ye, Zhipeng;Kennedy, Michael Peter
Publication date	2009-02-01
Original Citation	Ye, Z., Kennedy, M.P., 2009. Hardware reduction in digital delta-sigma modulators via error masking - part II: Sq-DDSM. IEEE Transactions On Circuits and Systems II - Express Briefs, 56 (2), pp.112-116.
Type of publication	Article (peer-reviewed)
Link to publisher's version	10.1109/TCSII.2008.2010188
Rights	©2009 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE.
Download date	2026-11-07 09:34:33
Item downloaded from	https://hdl.handle.net/10468/131

UCC
University College Cork, Ireland
Coláiste na hOllscoile Corcaigh

Hardware Reduction in Digital Delta–Sigma Modulators Via Error Masking—Part II: SQ-DDSM

Zhipeng Ye, *Student Member, IEEE*, and Michael Peter Kennedy, *Fellow, IEEE*

***Abstract*—In this two-part paper, a design methodology for reduced-complexity digital delta–sigma modulators (DDSMs) based on error masking is presented. Rules for selecting the wordlengths of the stages in multistage architectures are elaborated. We show that the hardware requirement can be reduced by up to 20% compared with a conventional design, without sacrificing performance. Simulation results confirm theoretical predictions. Part I addresses multistage noise-shaping DDSMs, whereas Part II focuses on single-quantizer DDSMs.**

***Index Terms*—Delta–sigma modulator, error masking, reduced complexity.**

I. Introduction

DIGITAL delta–sigma modulators (DDSMs) are often found in consumer communications and entertainment products. Popular DDSMs are based on two classes of delta–sigma modulators (DSMs), called multistage noise-shaping (MASH) DDSMs and single-quantizer (SQ) DDSMs [1]. MASH DDSMs employ a cascade of lower order blocks to construct a high-order modulator. SQ-DDSMs typically incorporate a single nth-order discrete-time filter.

In Part I of this brief [2], we presented a design methodology for a reduced-complexity (RC) MASH-DDSM [3], where the wordlength is reduced from integrator to integrator along the signal path. The errors resulting from interstage quantizers are masked below the filtered quantization error of the last stage. In this brief, we extend our design methodology to SQ-DDSMs.

II. SQ Architectures

A. Conventional SQ-DDSM

Several topologies of SQ-DDSMs have been described in the literature [1], [4], [5]. Fig. 1 shows the third-order topology described in [4]; the quantizer Q_3 is modeled as an additive noise source e_3. The corresponding Z-transform representation is

$$Y(z) = z^{-1}X(z) + \left[\frac{(1-z^{-1})^3}{B(z)}\right] E_3(z) \quad (1)$$

$$= STF(z)X(z) + NTF(z)E_3(z) \quad (2)$$

where $Y(z)$, $X(z)$, and $E_3(z)$ are the transforms of the input, output, and quantization error, respectively, and

$$B(z) = (1-z^{-1})^3 + 2z^{-1}(1-z^{-1})^2 + 1.5z^{-2}(1-z^{-1}) + 0.5z^{-3}. \quad (3)$$

In the SQ-DDSM, the wordlengths of the internal integrators should be larger than the input wordlength in order to avoid truncation errors. In the implementation considered in [4], the wordlengths of the internal integrators are realized by adders, and their wordlengths are three bits larger than the input. The three-bit output of the DDSM is the three most significant bits (MSBs) of the sum of the three integrators' outputs; this is fed back to the three MSBs of the first adder, as shown in Fig. 1. The N least significant bits (LSBs) of the first adder's output only depend on the N-bit input signal, which is constant; they are not affected by the feedback signal.

The three MSBs of the first adder's output will be truncated by the modulator and will not affect the output cycle length of the SQ-DDSM. Compare this with the N-bit MASH DDSM, as described in Part I [2], where there is no feedback signal and the adder's output only depends on the N-bit constant input. The wordlength calculation for the MASH-DDSM [6] can be adapted to SQ-DDSMs. The maximum output cycle length for the first-, second-, and third-order SQ-DDSMs are 2^N, 2^{N+1}, and 2^{N+1}, respectively, where N is the *effective* wordlength of the internal integrators.[1]

B. RC SQ-DDSM

An RC SQ-DDSM was proposed in [4]; this is shown in Fig. 2. In order to reduce the power and area consumption, the wordlengths of the integrators are reduced stage by stage. The wordlength of the first stage is 17, whereas the wordlengths of the second and third stages are 12 and 8, respectively. As in the MASH DDSM case [2], interstage truncation quantizers are inserted between the integrators; these can be realized in practice by simply omitting the LSBs.

This system is described by

$$Y(z) = z^{-1}X(z) + \left[\frac{(1-z^{-1})^3}{B(z)}\right] E_3(z) + \left[\frac{0.5z^{-2}(1-z^{-1}) + z^{-1}(1-z^{-1})^2}{B(z)}\right] E_{12}(z) + \left[\frac{0.5z^{-1}(1-z^{-1})^2}{B(z)}\right] E_{23}(z) \quad (4)$$

where $E_3(z)$ is the Z-transform of the error introduced by the 3-bit quantizer in the third stage. Note that the first two terms

Manuscript received November 3, 2008. This work was supported in part by Science Foundation Ireland under Grant 02/IN.1/I45 and Grant 08/IN.1/I1854 and in part by the Irish Research Council for Science, Engineering and Technology (IRCSET) under Grant SC/2002/409. This paper was recommended by Associate Editor G. Manganaro.

Z. Ye was with the Department of Microelectronic Engineering, Tyndall National Institute, University College Cork, Cork, Ireland. He is now with Australian Semiconductor Technology Company (ASTC) Pty Ltd., Adelaide 5000, South Australia (e-mail: zhipeng.ye@ue.ucc.ie).

M. P. Kennedy is with the Department of Microelectronic Engineering, Tyndall National Institute, University College Cork, Cork, Ireland (e-mail: peter.kennedy@ucc.ie).

Digital Object Identifier 10.1109/TCSII.2008.2010188

[1]The *effective* wordlength of an internal integrator equals the wordlength of the integrator minus the wordlength of the output quantizer. In this example, the effective wordlength is $17 - 3 = 14$.

1549-7747/$25.00 © 2009 IEEE

Authorized licensed use limited to: UNIVERSITY COLLEGE CORK. Downloaded on March 26,2010 at 12:16:38 EDT from IEEE Xplore. Restrictions apply.

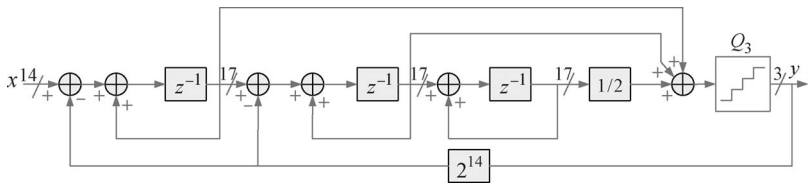


Fig. 1. Block diagram of a third-order SQ-DDSM with identical integrators.

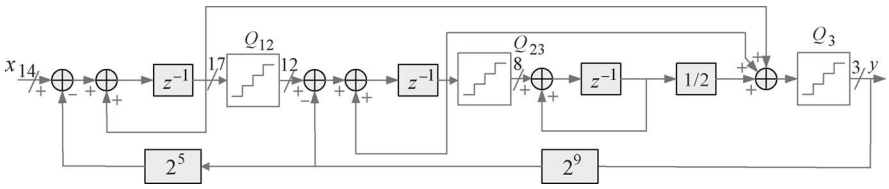


Fig. 2. Block diagram of the RC third-order SQ-DDSM [4]. Interstage quantizers Q_{12} and Q_{23} are introduced to reduce the wordlengths in successive integrator stages.

are identical to (1). $E_{12}(z)$ and $E_{23}(z)$ are the Z-transforms of the additional error signals introduced by the $M+3$-bit and $L+3$-bit interstage quantizers between the first and second and second and third accumulators, respectively. $M=9$ and $L=5$ in this example. We model these quantization effects as additive white noise sources e_{12} and e_{23} [7].

Although it describes the architecture and wordlengths, no design methodology is presented in [4]. In this brief, we show how to apply our error-masking strategy [2], [8] in a systematic way to select the wordlengths of the accumulators in this structure.

III. Design Methodology (Ditherless Case)

Let us rewrite (4) in the form

$$Y(z) = STF(z)X(z) + N_3(z) + N_{12}(z) + N_{23}(z) \tag{5}$$

where $N_3(z)$ is the filtered noise contribution from the quantizer Q_3, and $N_{12}(z)$ and $N_{23}(z)$ are the filtered contributions from the first and second interstage quantizers Q_{12} and Q_{23}, respectively.

The discrete power density spectrum $P_y[k]$ of the output y of the DDSM is defined by

$$P_y[k] = |Y[k]|^2 \tag{6}$$

where $Y[k]$ is the discrete-time Fourier series [9] of the output of the DDSM.

In this architecture, $|STF(z)|^2 = 1$, and assuming e_{12}, e_{23}, and e_3 are all white and uncorrelated with each other and the input (the so-called white-noise model (WNM) [1]), the power density spectrum at the DDSM output can be expressed as

$$S_y \approx S_x + S_3 + S_{12} + S_{23} \tag{7}$$

where S_y, S_x, S_3, S_{12}, and S_{23} are the power density spectra of the output, the input, and the idealized outputs from the output and interstage quantizers [7].[2]

Assuming a cycle of length L_s and additive uniformly distributed white quantization noise e_3, the idealized power spectrum S_3 of the shaped noise $N_3(z)$ is given as follows [10]:

$$S_3\left(f[k]\right) = \frac{1}{12L_s}\left|\frac{(1-z^{-1})^3}{B(z)}\right|^2_{z=e^{j2\pi k/L_s}}. \tag{8}$$

[2]In the examples in this work, the cross correlations are less than 0.02.

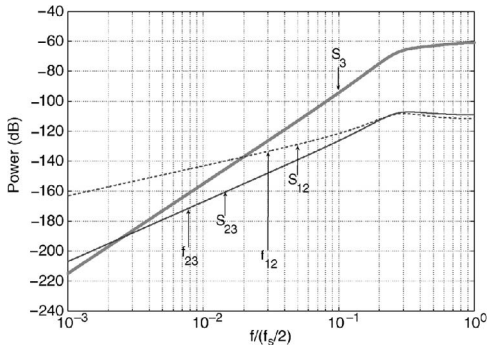


Fig. 3. Masking power density spectra (dashed) S_{12} and (solid light) S_{23} below (solid heavy) S_3. The lowest frequency tone in N_{23} is at $f_{23} = f_s/2^{N-L}$; the lowest frequency tone in N_{12} is at $f_{12} = f_s/2^{N-M}$.

In the same manner, the idealized spectra S_{12} and S_{23} resulting from e_{12} and e_{23} can be expressed as

$$S_{12}(f[k]) = \frac{\Delta_{12}^2}{12L_{12}}\left|\frac{0.5z^{-2}(1-z^{-1})}{B(z)} + \frac{z^{-1}(1-z^{-1})^2}{B(z)}\right|^2_{z=e^{j2\pi k/L_{12}}} \tag{9}$$

$$S_{23}(f[k]) = \frac{\Delta_{23}^2}{12L_{23}}\left|\frac{0.5z^{-1}(1-z^{-1})^2}{B(z)}\right|^2_{z=e^{j2\pi k/L_{23}}} \tag{10}$$

where $\Delta_3 = 1$, $\Delta_{12} = 1/2^M$, $\Delta_{23} = 1/2^L$, $L_3 = 2^N$, $L_{12} = 2^{N-M}$, and $L_{23} = 2^{N-L}$.

The three noise terms are graphically illustrated in Fig. 3. Our error-masking algorithm requires that the envelope of the error spectra S_{12} and S_{23} due to the interstage quantizers should lie below the S_3 contribution. In order to mask the discrete spectra N_{12} and N_{23}, we require that

$$S_{12} < S_3 \quad \text{at} \quad f_{12} \tag{11}$$

$$S_{23} < S_3 \quad \text{at} \quad f_{23} \tag{12}$$

where f_{12} and f_{23} are the lowest frequency components in these spectra.[3]

Recall that

$$|1-z^{-1}|^2 = |1-e^{-j2\pi f/f_s}|^2 = |2\sin(\pi f/f_s)|^2 \tag{13}$$

$$\sin(\pi f/f_s) \approx \pi f/f_s, \qquad \text{for } f \ll f_s. \tag{14}$$

[3]Because S is based on the WNM, this is a necessary, but not a sufficient, condition.

Authorized licensed use limited to: UNIVERSITY COLLEGE CORK. Downloaded on March 26,2010 at 12:16:38 EDT from IEEE Xplore. Restrictions apply.

Therefore

$$S_3(f) \approx \frac{\Delta_3^2}{12L_3} \cdot 2^6(\pi f/f_s)^6 \cdot \frac{1}{B(z)} \tag{15}$$

at low frequencies, and at the boundary frequencies f_{12} and f_{23}

$$S_{12}(f_{12}) \approx \frac{\Delta_{12}^2}{12L_{12}} \cdot \left(2 \cdot \frac{\pi^2}{2^{2(N-M)}} + 2^4 \cdot \frac{\pi^4}{2^{4(N-M)}}\right) \frac{1}{B(z)} \tag{16}$$

$$S_{23}(f_{23}) \approx \frac{\Delta_{23}^2}{12L_{23}} \cdot 2^3 \cdot \frac{\pi^4}{2^{4(N-L)}} \cdot \frac{1}{B(z)}. \tag{17}$$

Note that $B(z)$ appears in S_3, S_{12}, and S_{23}. It acts as a normalization factor and does not affect the comparison between them. Therefore, we do not need to explicitly calculate $1/B(z)$ when we apply the error-masking strategy.

By exploiting the approximations (15)–(17), the constraints (11) and (12) for the SQ-DDSM can be rewritten as

$$\frac{1}{2^{2M}} \cdot \frac{1}{12 \cdot 2^{N-M}} \cdot \left(2 \cdot \frac{\pi^2}{2^{2(N-M)}} + 2^4 \cdot \frac{\pi^4}{2^{4(N-M)}}\right) < \frac{1}{12 \cdot 2^N} \cdot \frac{2^6\pi^6}{2^{6(N-M)}} \tag{18}$$

$$\frac{1}{2^{2L}} \cdot \frac{1}{2^{(N-L)}} \cdot 2^3 \cdot \frac{\pi^4}{2^{4(N-L)}} < \frac{1}{2^N} \cdot \frac{2^6\pi^2}{2^{6(N-L)}} \tag{19}$$

which reduce to

$$2^{4N-5M-5} + \pi^2(2^{2N-3M-2}) < \pi^4 \tag{20}$$

$$2N - 3L - 3 < 2\log_2(\pi). \tag{21}$$

Based on (20) and (21), in order to design an RC SQ-DDSM with the same cycle length and similar power spectrum as a conventional $(N_0 + 3)$-bit SQ-DDSM, where N_0 is the *effective* wordlength of the conventional SQ-DDSM, the following design procedure is used.

1) Choose $N = N_0 + 1$ to ensure that the output cycle length of the RC SQ-DDSM is the same as that of the conventional $(N_0 + 3)$-bit SQ-DDSM. Set the LSB of the input to "1" to obtain the maximum output cycle length [2], [3].
2) Choose M using $2^{4N-5M-5} + \pi^2(2^{2N-3M-2}) < \pi^4$ (20) to ensure that the power of the first tone of N_{12} is less than S_3 at the frequency $f_{12} = f_s/2^{N-M}$.
3) Choose $L = \text{ceil}(2N - 3 - 2\log_2(\pi)/3)$ [from (21)] to ensure that the power of the first tone of N_{23} is less than S_3 at the frequency $f_{23} = f_s/2^{N-L}$, where ceil(x) means the smallest integer greater than x.

IV. Design Example

In order to verify the design methodology in detail, we present a design example in this section. We use a 20-bit input for the SQ-DDSM, i.e., $N_0 = 19$.[4] Applying the design equations (20) and (21), the required values of M and L are 14 and 12, respectively. Recall that we need to add three more bits to each stage to avoid truncation errors. Applying the algorithm, the wordlengths of the resulting SQ-DDSM stages are 23, 17, and 15.

[4]In this case, the conventional structure would require 22 bits per accumulator.

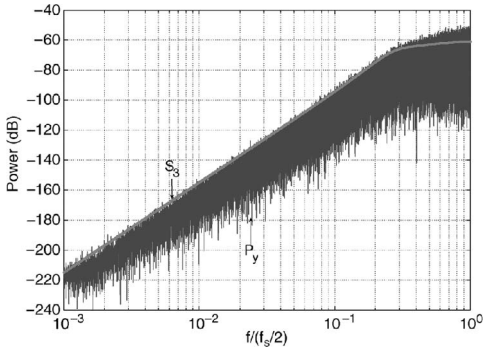


Fig. 4. Simulated PSD P_y of a conventional 22-bit SQ-DDSM and the white noise approximation S_3; the input is 65.

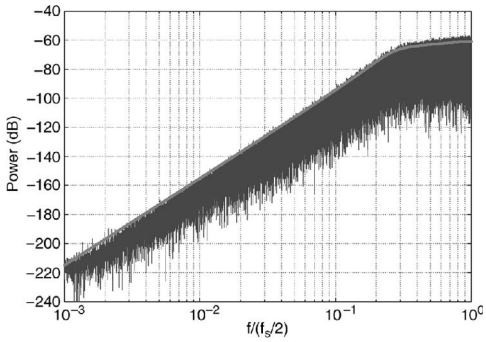


Fig. 5. Simulated PSD of an RC 23–17–15-bit SQ-DDSM and the white noise approximation S_3; the input is 65 (compare with Fig. 4).

A. Simulations

The simulated power spectral densities (PSDs) overlaid with the theoretical predictions for (a) a conventional 22-bit and (b) an RC 23–17–15-bit SQ-DDSM with a 20-bit input are shown in Figs. 4 and 5, respectively. We see that since we hide the internal error signal, the resulting output of the RC SQ-DDSM achieves comparable performance to the conventional SQ-DDSM. Moreover, since the output cycle length of the SQ-DDSM is guaranteed by the wordlength of the first integrator, the spurious tones at low frequencies are negligible, even without dithering. In addition, the spectrum of the RC SQ-DDSM is closer to the ideal near $f_s/2$ due to more effective whitening of the quantization noise.

B. Simulated Hardware Consumption

The relative hardware consumption (RHC) of the RC SQ-DDSM compared to the conventional SQ-DDSM can be calculated using

$$\text{RHC} = \frac{N + M + L + 9}{3N_0 + 9} \tag{22}$$

once N, M, and L have been determined.

In order to avoid truncation errors, three additional bits have been added to each stage, as described in Section II; this is where the number 9 in (22) comes from. For the case $N_0 = 19$, the predicted reduction in hardware consumption is 17%.

The hardware requirements for a conventional 22-bit SQ-DDSM $(N_0 = 19)$ and the 23–17–15-bit RC SQ-DDSM

Authorized licensed use limited to: UNIVERSITY COLLEGE CORK. Downloaded on March 26,2010 at 12:16:38 EDT from IEEE Xplore. Restrictions apply.

TABLE I
HARDWARE CONSUMPTION OF THE CONVENTIONAL 22-BIT SQ-DDSM AND THE 23–17–15-BIT RC SQ-DDSM

SQ-DDSM without dither	Hardware Consumption		
	FFs	LUTs	TEGs
(a) 22 bit	68	116	1760
(b) 23-17-15 bit	58	99	1469
((a)/(b))%	85%	85%	83%

are summarized in Table I. The hardware consumption is reported as the number of flip-flops (FFs) and the number of four-input lookup tables (LUTs). The total equivalent gate (TEG) count for the design is given as well. These results are based on the map report from the Xilinx ISE program [11]. The simulated RHC is close to the 83% predicted by (22).

V. DESIGN METHODOLOGY (WITH DITHER)

Dithering can be used to break up short cycles in a deterministic DDSM [12], [13]. The block diagram of a dithered RC SQ-DDSM is shown in Fig. 6. With dithering, the minimum cycle length of the DDSM is guaranteed to be at least as large as that of the pseudorandom dither generator. Consequently, the tone spacing is typically very small. When the tones are sufficiently closely spaced, the discrete spectrum tends toward a continuous spectrum. In this case, the discrete power spectrum representation $P[k]$ can be approximated by a PSD representation with $\mathcal{L}$ expressed in units of decibels relative to the carrier per hertz (dBc/Hz) [2], [10].

Assuming e_3, e_{12}, and e_{23} are white, and comparing with (8)–(10), the PSDs of the envelopes of the filtered error signals N_3, N_{12}, and N_{23} can be written as

$$\mathcal{L}_3(f) = \frac{1}{12}\left|\frac{(1-z^{-1})^3}{B(z)}\right|^2_{z=e^{j2\pi f/f_s}} \tag{23}$$

$$\mathcal{L}_{12}(f) = \frac{\Delta_{12}^2}{12}\left|\frac{0.5z^{-2}(1-z^{-1})}{B(z)} + \frac{z^{-1}(1-z^{-1})^2}{B(z)}\right|^2_{z=e^{j2\pi f/f_s}} \tag{24}$$

$$\mathcal{L}_{23}(f) = \frac{\Delta_{23}^2}{12}\left|\frac{0.5z^{-1}(1-z^{-1})^2}{B(z)}\right|^2_{z=e^{j2\pi f/f_s}}. \tag{25}$$

In this section, we apply the error-masking idea in a slightly different way for an SQ-DDSM with dither, where the goal is to mask $\mathcal{L}_{12}$ and $\mathcal{L}_{23}$ below $\mathcal{L}_3$ above a target frequency f_0. Thus, we require that

$$\mathcal{L}_{12} < \mathcal{L}_3 \quad \text{at} \quad f_0 \tag{26}$$

$$\mathcal{L}_{23} < \mathcal{L}_3 \quad \text{at} \quad f_0. \tag{27}$$

We can set the specified frequency f_0 as some fraction A of the clock frequency, i.e., $f_0 = A \cdot f_s$, where A is constant, and f_s is the clock frequency. In this case, $\mathcal{L}_3$, $\mathcal{L}_{12}$, and $\mathcal{L}_{23}$ at f_0 can be expressed in the passband as

$$\mathcal{L}_3 \approx \frac{1}{12}2^6 \cdot A^6 \cdot \pi^6 \cdot \frac{1}{B(z)} \tag{28}$$

$$\mathcal{L}_{12} \approx \frac{1}{12 \cdot 2^{2M}} \cdot (2\pi^2 \cdot A^2 + 2^4\pi^4 \cdot A^4)\frac{1}{B(z)} \tag{29}$$

$$\mathcal{L}_{23} \approx \frac{1}{12 \cdot 2^{2L}} \cdot (2^3 \cdot \pi^4 \cdot A^4)\frac{1}{B(z)}. \tag{30}$$

The methodology is graphically shown in Fig. 7. Applying the design constraints (26) and (27) using (28)–(30), we require that

$$\frac{1}{12 \cdot 2^{2M}} \cdot \left(2\pi^2 \cdot A^2 + 2^4\pi^4 \cdot A^4\right) < \frac{1}{12}2^6 \cdot A^6 \cdot \pi^6$$

$$\frac{1}{12 \cdot 2^{2L}} \cdot \left(2^3 \cdot \pi^4 \cdot A^4\right) < \frac{1}{12}2^6 \cdot A^6 \cdot \pi^6 \tag{31}$$

which reduce to

$$M > \frac{\log_2(2A^2 + 16\pi^2A^4) - \log_2(A^6\pi^4) - 6}{2} \tag{32}$$

$$L > \frac{-\log_2(A^2\pi^3) - 3}{2} \tag{33}$$

respectively.

In order to design an RC SQ-DDSM with a similar power spectrum to a conventional $(N+3)$-bit SQ-DDSM with dither, the design procedure based on (32) and (33) is given here.

1) Set the value for A so that $\mathcal{L}_{12}$ and $\mathcal{L}_{23}$ can be masked below $\mathcal{L}_3$ beyond the specified frequency $f_0 = A \cdot f_s$.
2) Choose $M = \text{ceil}[(\log_2(2A^2+16\pi^2A^4) - \log_2(A^6\pi^4) - 6)/2]$ [from (32)] to ensure that the PSD $\mathcal{L}_{12}$ is less than $\mathcal{L}_3$ at the frequency f_0, where ceil(x) means the smallest integer greater than x.
3) Choose $L = \text{ceil}(-\log_2(A^2\pi^3) - 3/2)$ [from (33)] to ensure that the PSD $\mathcal{L}_3$ is less than $\mathcal{L}_3$ at the frequency f_0.

VI. DESIGN EXAMPLE (WITH DITHER)

In a typical fractional-N frequency synthesizer, the ratio of the loop bandwidth to the reference frequency is usually below 0.001. Therefore, we select $A = 0.001$. The frequency resolution is chosen to be $f_{\text{ref}}/2^{20}$, which requires a 20-bit input signal. In this case, the required wordlengths for each stage of the SQ-DDSM using (32) and (33) are 23, 20, and 12.

A. Simulation Results

Figs. 8 and 9 show the simulated PSDs of (a) a conventional 23-bit and (b) an RC 23–20–12-bit SQ-DDSM with first-order shaped additive input dither [13]. We can see that, since the internal error has been masked beyond $f/f_s = 0.001$, the RC SQ-DDSM achieves almost identical spectral performance compared to the conventional SQ-DDSM.

The noise floor due to the first-order shaped dither [14] is

$$\mathcal{L}_{\text{noise floor}} = \frac{1}{12 \cdot (2^N)^2}\left|(2\sin(\pi f_0/f_s))\right|^2 \tag{34}$$

where $N = 20$, and $V(z) = 1 - z^{-1}$. In this example, the noise floor is always significantly lower than the PSD for N_3 in the three decades above f_0 and, therefore, has no effect on the simulation results. If fewer bits were used, the effect of the noise would be evident, but it could be masked, as outlined in Part I of this brief [2].

B. Simulated Hardware Consumption

Neglecting the dither hardware, the formula for calculating the RHC is the same in this case. For $N = 20$ and $A = 0.001$, we predict a reduction of 20% in hardware consumption.

Authorized licensed use limited to: UNIVERSITY COLLEGE CORK. Downloaded on March 26,2010 at 12:16:38 EDT from IEEE Xplore. Restrictions apply.

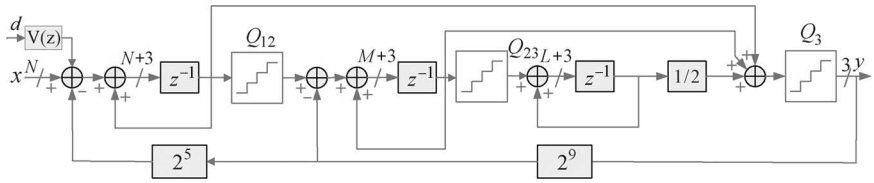


Fig. 6. Block diagram of the dithered RC SQ-DDSM.

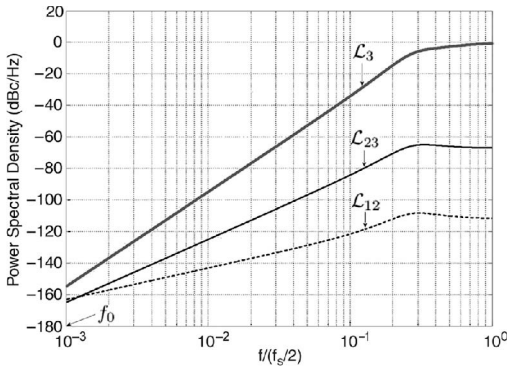


Fig. 7. Masking $\mathcal{L}_{12}$ and $\mathcal{L}_{23}$ below $\mathcal{L}_3$ above f_0.

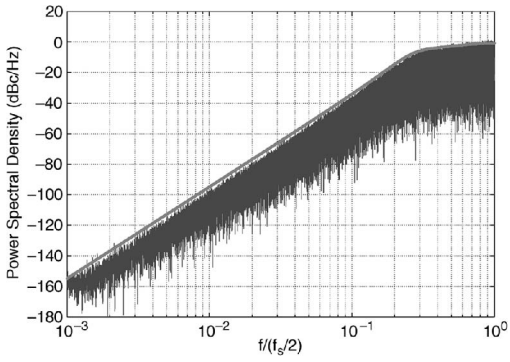


Fig. 8. Simulated PSD P_y of a conventional 23-bit SQ-DDSM with a 20-bit input and first-order additive input dither; the input is 65. The smooth curve is $\mathcal{L}_3$. The dc term has been removed.

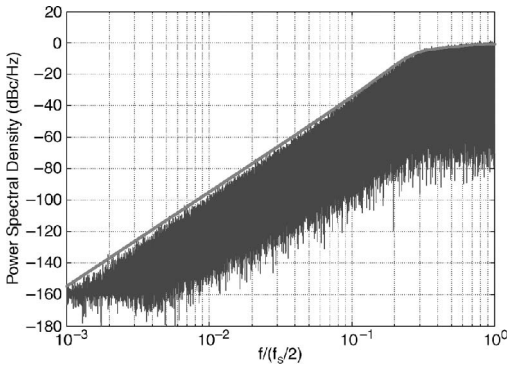


Fig. 9. Simulated PSD P_y of an RC 23–20–12-bit SQ-DDSM with a 20-bit input and first-order additive input dither; the input is 65. The smooth curve is $\mathcal{L}_3$. The dc term has been removed (compare with Fig. 8).

The hardware consumption of the SQ-DDSM with dither is shown in Table II. The 23–20–12 RC SQ-DDSM with first-order dither achieves an almost identical PSD compared to the 23-bit conventional SQ-DDSM with dither, but with 16% less hardware. If we subtract the hardware consumption for the dither block for both SQ-DDSMs, our RC SQ-DDSM has an RHC of 80%, as predicted.

TABLE II
HARDWARE CONSUMPTION OF THE CONVENTIONAL 23-BIT SQ-DDSM WITH FIRST-ORDER DITHER AND THE 23–20–12-BIT RC SQ-DDSM WITH FIRST-ORDER DITHER

SQ-DDSM with first-order dither	Hardware Consumption		
	FFs	LUTs	TEGs
(a) 23 bit with first-order dither	99	149	2248
(b) 23-20-12 bit with first-order dither	85	121	1882
((b)/(a))%	86%	81%	84%

VII. CONCLUSION

In this brief, we have presented a design methodology for SQ-DDSMs based on error masking. We have shown that, starting with a conventional DDSM having identical accumulators, it is possible to find an optimized wordlength for each stage of the SQ-DDSM, which allows a reduction in the hardware consumption by up to 20%, without degrading the spectral performance.

REFERENCES

[1] S. R. Norsworthy, R. Schreier, and G. C. Tames, *Delta–Sigma Data Converters Theory, Design and Simulation*. New York: IEEE Press, 1997.
[2] Z. Ye and M. P. Kennedy, "Hardware reduction in digital delta–sigma modulators—Part I: MASH," *IEEE Trans. Circuits Syst. I*. to be published.
[3] Z. Ye and M. P. Kennedy, "Reduced complexity MASH delta–sigma modulator," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 8, pp. 725–729, Aug. 2007.
[4] L. A. Williams and F. Cavaliere, "Reduced area digital sigma–delta modulator," U.S. Patent 7 176 821, Feb. 13, 2007.
[5] T. A. Riley, M. Copeland, and T. Kwasniewski, "Delta–sigma modulation in fractional-N frequency synthesis," *IEEE J. Solid-State Circuits*, vol. 28, no. 5, pp. 553–559, May 1993.
[6] K. Hosseini and M. P. Kennedy, "Mathematical analysis of digital MASH delta–sigma modulators for fractional-N frequency synthesizers," in *Proc. PRIME*, Otranto, Italy, Jun. 2006, pp. 309–312.
[7] W. R. Bennett, "Spectra of quantized signals," *Bell Syst. Tech. J.*, vol. 27, no. 4, pp. 446–472, Jul. 1948.
[8] M. P. Kennedy and Z. Ye, "A delta sigma modulator," Irish Patent Application Number 2006/0763, Oct. 17, 2006.
[9] S. Haykin and B. D. Van Veen, *Signals and Systems*, 2nd ed. New York: Wiley, 2003.
[10] M. J. Borkowski, T. A. D. Riley, J. Hakkinen, and J. Kostamovaara, "A practical $\Delta\Sigma$ modulator design method based on periodical behavior analysis," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 10, pp. 626–630, Oct. 2005.
[11] *ISE Quick Start Tutorial*, 2005. [Online]. Available: http://toolbox.xilinx.com /docsan/xilinx7/books/docs/qst/qst.pdf
[12] R. A. Wannamaker, S. P. Lipshitz, J. Vanderkooy, and J. N. Wright, "A theory of nonsubtractive dither," *IEEE Trans. Signal Process.,* vol. 48, no. 2, pp. 499–516, Feb. 2000.
[13] S. Pamarti, J. Welz, and I. Galton, "Statistics of the quantization noise in 1-bit dithered single-quantizer digital delta–sigma modulators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 3, pp. 492–503, Mar. 2007.
[14] H. Hsieh and C.-L. Lin, "Spectral shaping of dithered quantization errors in sigma–delta modulators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 5, pp. 947–980, May 2007.

Authorized licensed use limited to: UNIVERSITY COLLEGE CORK. Downloaded on March 26,2010 at 12:16:38 EDT from IEEE Xplore. Restrictions apply.