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Title	Random telegraph-signal noise in junctionless transistors
Authors	Nazarov, Alexei N.;Ferain, Isabelle;Akhavan, Nima Dehdashti;Razavi, Pedram;Yu, Ran;Colinge, Jean-Pierre
Publication date	2011
Original Citation	Nazarov, A. N., Ferain, I., Akhavan, N. D., Razavi, P., Yu, R. and Colinge, J. P. (2011) 'Random telegraph-signal noise in junctionless transistors', Applied Physics Letters, 98(9), pp. 092111. doi: 10.1063/1.3557505
Type of publication	Article (peer-reviewed)
Link to publisher's version	http://aip.scitation.org/doi/abs/10.1063/1.3557505 - 10.1063/1.3557505
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Citation: Appl. Phys. Lett. **98**, 092111 (2011); doi: 10.1063/1.3557505
View online: http://dx.doi.org/10.1063/1.3557505
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Random telegraph-signal noise in junctionless transistors

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(Received 4 January 2011; accepted 31 January 2011; published online 1 March 2011)

Random telegraph-signal noise (RTN) is measured in junctionless metal-oxide-silicon field-effect transistors (JL MOSFETs) as a function of gate and drain voltage and temperature. It is shown that the RTN in JL MOSFETs increases significantly when an accumulation layer is formed. The amplitude of RTN is considerably smaller in JL devices than in inversion-mode MOSFET fabricated using similar fabrication parameters. A measurement technique is developed to extract the main parameters of the traps, including the average charge capture and emission time from the traps. © *2011 American Institute of Physics*. [doi:10.1063/1.3557505]

The scaling of field-effect transistors results in an increased sensitivity of the devices to local charge trapping/detrapping processes, which influence electrical transport in the channel and generate noise. The junctionless (JL) metal-oxide-semiconductor field-effect transistor (MOSFET) has recently been proposed[1,2] as an alternative device for sub-20-nm nodes. The JL architecture eliminates the need for forming PN junctions. In a JL MOSFET, the channel containing the carriers flowing from source to drain is located inside a heavily doped silicon nanowire, and the electric field inside of the channel, perpendicular to the current flow, is very low.[3] No study on random telegraph-signal noise (RTN) in heavily doped devices has been reported yet, although it was recently shown that accumulation mode (AM) MOSFETs with highly doped substrate present unusually low levels of 1/f noise.[4]

In this letter, we study RTN in nanowire (NW) silicon JL MOSFETs and compare these results with the RTN characteristics of inversion-mode (IM) NW MOSFETs fabricated using the same processing steps. The devices reported here are multigate silicon NW n-type MOSFETs with pi-gate architecture fabricated on UNIBOND® silicon-on-insulator wafers. The width and thickness of the silicon nanowires are both approximately equal to 10 nm (see the inset of Fig. 1). The gate length is 1 μm. The gate oxide and buried oxide thickness are 7 and 340 nm, respectively. The JL MOSFETs have uniform N-type doping concentration of 1×10^{19} cm^{-3} in the source, drain, and channel regions. "Standard" IM pi-gate MOSFETs were made using the same fabrication process. These have the same dimensions as the JL devices but have a p-type channel doping concentration of 2×10^{18} cm^{-3} and an n-type doping concentration of 1×10^{20} cm^{-3} in the source and drain regions. The JL MOSFETs have a P$^+$-polysilicon gate electrode and the IM devices have an N$^+$-polysilicon gate electrode.

Figure 1 shows the drain current versus gate voltage characteristics $I_D(V_G)$ of the measured NW MOSFETs. The threshold voltage of the IM (V_{th}^{IM}) and JL devices (V_{th}^{JL}) was extracted using the second derivative of the drain current versus gate voltage technique and is equal to 0.2 and 0.33 V, respectively. The RTN of the drain current is measured above threshold, and for the same gate voltage overdrive, defined as $V_{GO}=V_G-V_{th}$. The measured RTN curves are presented in Fig. 2(a). In our case, the RTN can be described by two drain current levels: high-current (on) level and a low-current (off) level. The duration for which the drain current is in the high-current state represents the capture time (τ_c) of traps, whereas the time in the low-current state represents the emission time (τ_e).[5] It should be noted that the magnitude of the relative RTN amplitude of the drain current ($\Delta I_D/I_D$) is considerably larger in the IM devices than in the JL devices [Fig. 2(b)].

The relative RTN amplitude of the drain current in both types of the devices varies as the inverse of gate voltage overdrive: $\Delta I_D/I_D \approx (V_G-V_{th})^{-1}$ [see the inset of Fig. 2(b)]. A similar $(V_G-V_{th})^{-1}$ dependence can be obtained in first approximation for IM MOSFETs from Eq. (67) of Ref. 6,

$$\frac{\Delta I_D}{I_D}=\frac{q}{WLC_{ox}}\times\frac{g_m}{I_D}\approx\frac{q}{WLC_{ox}(V_G-V_{th})}\times\left\{1+\frac{1}{1+\theta^{-1}(V_G-V_{th})^{-1}}\right\}, \quad (1)$$

where g_m is the transconductance, W and L are the electrical width and length of the channel, C_{ox} is the gate oxide capaci-

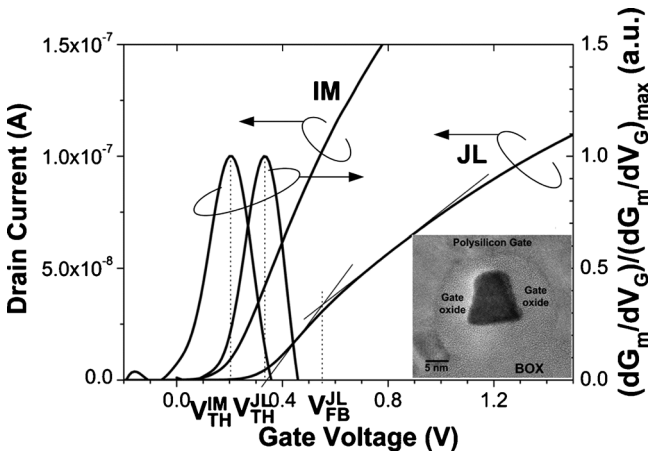


FIG. 1. $I_D(V_G)$ characteristics of JL and IM MOSFETs and their second derivatives. $V_D=50$ mV. Inset: high-resolution transmission electron microscope photograph of the cross section of a transistor.

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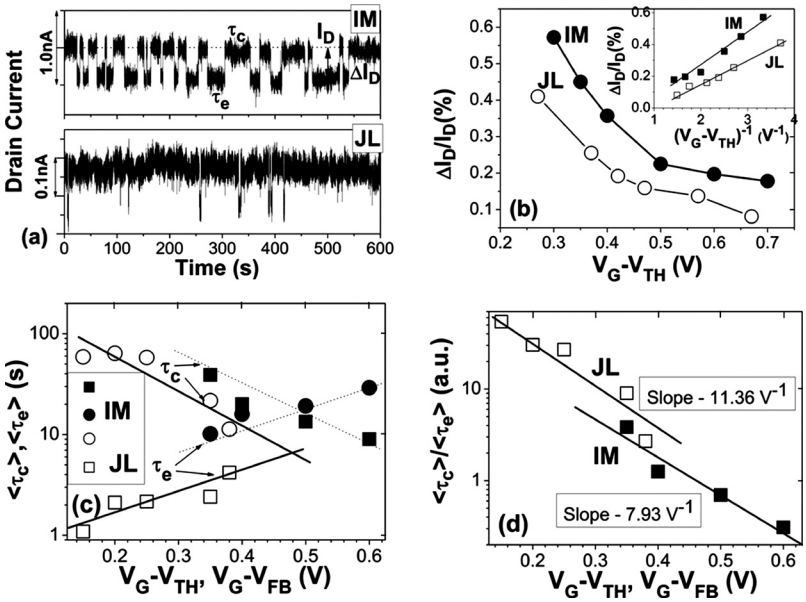


FIG. 2. (a) Random telegraph-signal noise in IM and JL MOSFETs at V_D=50 mV and V_G-V_{th}=0.52 V. (b) Dependence of the relative RTN amplitude of drain current on gate voltage overdrive (the inset represents the dependence of the relative RTN amplitude vs reverse gate voltage overdrive). (c) Average capture and emission time vs gate voltage overdrive. (d) Ratio of average capture time to average emission time vs gate voltage overdrive. In the JL device, V_{th} is replaced by V_{FB} in the expression of the gate voltage overdrive.

tance, and θ is the mobility degradation factor. Equation (1) can be applied to AM MOSFETs operating in the linear regime if the threshold voltage V_{th} is replaced by the flat-band voltage, which is the threshold of accumulation. Thus, a $(V_G-V_{th})^{-1}$ variation of the relative RTN amplitude of the drain current $\Delta I_D/I_D$ in a JL device is the signature of the presence of an accumulation channel. The AM surface-channel RTN in JL transistors follows the same general law in $\Delta I_D/I_D \approx g_m/I_D$ observed in IM devices.[7] This can be seen from comparing Fig. 2(b) with the $g_m/I_D(V_G)$ characteristics measured on JL devices.[8] The dependence of the bulk channel current on the JL MOSFET is more complicated[9] and does not follow a $(V_G-V_{th})^{-1}$ law.

The measurement of the average capture time $\langle\tau_c\rangle$ and the average emission time $\langle\tau_e\rangle$ as a function of gate voltage allows us to the estimate energy distribution and the position in the channel of the oxide trap levels responsible for RTN generation. The physical distance of the oxide trap x_T from the SiO_2-Si interface can be extracted from the dependence of $\ln(\langle\tau_c\rangle/\langle\tau_e\rangle)$ on either V_G-V_{th} (IM device) or V_G-V_{FB} (AM device) presented in Fig. 2(d), using the conventional expression[5]

$$\frac{d\left(\ln\frac{\langle\tau_c\rangle}{\langle\tau_e\rangle}\right)}{dV_G} \approx \frac{q}{kT} \times \frac{x_T}{T_{ox}}, \tag{2}$$

where T_{ox} is the gate oxide thickness. The value of x_T from the JL devices is 2.9 nm, and it is 2.0 nm for the IM devices. From the value of gate voltage overdrive $(V_G-V_{FB})^*$ corresponding to the point where $\langle\tau_c\rangle$ and $\langle\tau_e\rangle$ are equal [Fig. 2(c)], and the equation of detailed balance, $\langle\tau_c\rangle/\langle\tau_e\rangle = g\exp(E_T-E_F/kT)$, we can estimate the energy of the traps $(E_{C_{ox}}-E_T)$ from the following expression for the JL device in accumulation:

$$E_{C_{ox}} - E_T = E_{C_{ox}} - E_F - \frac{V_G - V_{FB}}{T_{ox}} x_T, \tag{3}$$

where $E_{C_{ox}}-E_F$ is the energy difference between the minimum of the conduction band of the gate oxide and the Fermi

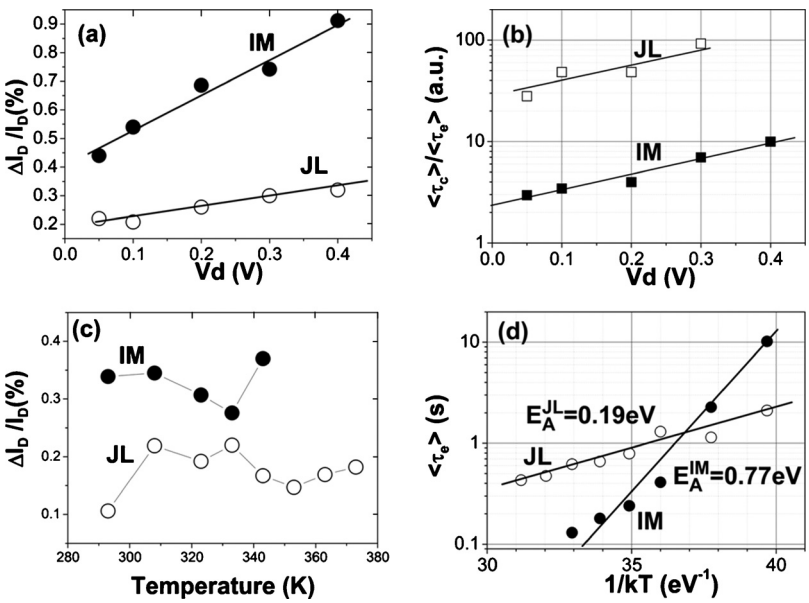


FIG. 3. (a) Relative RTN amplitude of drain current vs drain voltage. (b) Ratio of average capture time to average emission time vs drain voltage. (c) Relative RTN amplitude of drain current vs measurement temperature. (d) Arrhenius plot of emission time for the JL and IM MOSFETs (V_G-V_{th}=0.42 V).

level in the silicon nanowire. We find hat $E_{C_{ox}} - E_T$ is equal to 3.05 eV for the JL device.

For the same gate voltage overdrive, the relative RTN amplitude of the drain current in the JL devices is considerably smaller than in the IM devices. This observation is true whether the devices are analyzed as a function of drain voltage [Fig. 3(a)] or at high temperature [Fig. 3(c)]. This indicates that the drain current in JL MOSFETs is more stable than in IM devices. From the slope of $\ln(\langle\tau_c\rangle/\langle\tau_e\rangle)$ versus V_D, the position of the trap(s) along the channel Y_T can be estimated.[6] Because the slope of $\ln(\langle\tau_c\rangle/\langle\tau_e\rangle)$ versus V_D is the same for JL and IM devices [Fig. 3(b)], one can conclude that the trap location in the channel is the same for both devices. According to our calculations, the trap location in the channel is 150 nm from the source edge.

The activation energy can be determined from the dependence of the average emission time on temperature for a constant gate voltage overdrive [Fig. 3(d)] and it can be associated with the energy of the traps.[10] In the case of the JL device, the activation energy is 0.19 eV, and it is 0.77 eV for the IM device. This indicates a much larger energy band bending in the silicon nanowire near the SiO_2-Si interface in the IM MOSFET than in the JL device.

In conclusion, we observe a smaller relative RTN amplitude in the drain current of junctionless nanowire transistors than in inversion-mode MOSFETs. This is due to the absence of an electric field attracting majority carriers (in our case, electrons) toward the gate oxide/silicon interface. The average capture time of electrons into traps located in the gate oxide is considerably longer in case of the JL devices than in case of the IM transistors.

This work was supported by the Science Foundation Ireland grant (Contract No. 05/IN/I888) and enabled by the Programme for Research in Third-Level Institutions. This work was supported in part by the European Community (EC) Seventh Framework Program through the Networks of Excellence NANOSIL and EUROSOI+ under Contract Nos. 216171 and 216373.

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