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# Power Inside - Applications and Technologies for Integrated Power in Microelectronics

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***Abstract*—**The emergence of miniaturized and integrated Power Supply on Chip (PwrSoC) and Power Supply in Package (PwrSiP) platforms will be enabled by the application of thin-film, integrated magnetics on silicon. A process flow for, and the design of, a thin-film coupled-inductor, switching at 60MHz, is described. Based on the large signal characterization data, measured up to 100MHz,, the efficiency of the inductor is calculated to be 91.7% for a power of 0.5W.

## I. INTRODUCTION

Power Supply on Chip (PwrSoC) has been widely investigated as one of the most promising technologies to achieve cost-effectiveness, miniaturization and reliability in fully-integrated power management for low-voltage electronic circuits and systems [1].

The passive components in a dc-dc converter are used to provide temporary energy storage and filtering within the power management circuit. Realizing a fully-integrated power management solution requires developing integrated passive components that can be monolithically fabricated or packaged on active power IC circuitry. In their simplest form, these integrated passive components can be air-core inductors built on the active silicon substrate, but a large device footprint area is needed to fulfill the inductance requirements for the converter and the solution may also result in EMI issues [2, 3].

Thin-film, magnetic-core, inductor technology is an emerging technology that promises high-efficiency and high power density magnetic devices for integrated power converters [4, 5]. These thin-film inductor devices can be packaged with integrated capacitor and CMOS switch/driver technologies in either a PwrSoC form-factor or in miniaturized Power Supply in Package (PwrSiP) platforms based on embedded, 2.5D or 3D packaging solutions (Fig. 1).

These thin-film magnetics allow the design of low-value, and therefore small footprint, inductors that can operate at very high frequencies typically in the range 20 to 100MHz. The authors have demonstrated device values in the range 10nH to 100nH, with footprints of less than 1mm$^2$, a thickness profile as low as 0.2mm and costs of less than 1US cent/mm$^2$. This concept of magnetics-on-silicon, as seen in Fig. 2, is compatible with the application of back-end-of-line (BEOL) and microsystems/MEMS processing technologies including the deposition and patterning of thin-film magnetic core materials, used extensively in the magnetic disk-head and magnetic sensors industries.

Applications for thin-film power magnetics include inductors for standalone point-of-load (POL) and multi-output PMIC (Power Management IC) converters and micro-transformers for isolated power transfer [4]. However, the most disruptive application is expected to be in the full integration of last-stage power management with complex loads such as microprocessors and systems on chip (SoC).

The current interest in integrated power was clearly demonstrated at the International Workshop on Power Supply on Chip (PwrSoC16) in Madrid [5] with attendance from companies across the broad microelectronics supply-chain from semiconductor equipment vendors to foundry, fabrication facilities and OSATs (outsourced assembly and test houses) to power converter and passive component suppliers as well as system-on-chip (SOC) and electronic system companies.

The work in this paper describes the design, fabrication and characterization of a thin-film, coupled inductor using patterned thin-film, NiFe (nickel-iron) as the magnetic core material capable of operating up to 100MHz. Initially, the fabrication process flow is described and the device design specifications are provided. A large-signal characterization and analysis of the fabricated coupled inductor devices was undertaken for a converter operating frequency of 60MHz. This allowed the simulation of the true in-converter operating conditions for the inductor.

## II. COUPLED INDUCTORS FOR GRANULAR POWER

Research has shown that a large array of thin-film, coupled inductors integrated, in 2.5D or 3D format, with a microprocessor (which also incorporates the power management circuits and, potentially, high density capacitors), can enhance battery lifetime for mobile electronics while delivering power to multi-voltage rail processors in a scheme which has been termed granular power management [6,7].

This drive to a fully-integrated, granular power management platform for SoCs has recently attracted research into thin-film, coupled inductors [1,2,8,9]. The use of a coupled, power converter topology with multi-phases, arranged to achieve flux cancellation in the core material, addresses the challenge of low saturation currents associated with thin-film materials. Additionally, the coupled topology offers in-phase ripple reduction and faster transient response due to energy being stored as leakage inductance. This leads to significant reduction in output capacitor size and offers the

opportunity to integrate the power management circuit with the load.

## III. Fabrication of Coupled-Inductors

Fig. 3 shows the fabrication process-flow for a thin-film, coupled-inductor structure. The structure is composed of two sandwiched racetrack coils between two $Ni_{45}Fe_{55}$ thin-film, magnetic cores. In order to minimise the component footprint, the coupled-inductor has been fabricated by stacking two layers of electroplated copper coils, requiring a Double-Layer-Metal (DLM) process for the windings. This requires a 7-mask fabrication process [8]. The top and bottom electroplated magnetic cores are electrically connected to create a closed magnetic path around the inductor windings, thereby enhancing the inductance and minimizing emi issues in the converter and neighbouring circuits.

## IV. Design of Coupled-Inductor Devices

The coupled-inductor design consists of a two-phase coupled inductor, with self-inductance, L1=L2=45nH, and moderate coupling, $k \approx 0.4$. The total inductance required by the buck converter circuit is 90nH. The output power of the buck converter is 0.5W with input voltage of 3.3V and output voltage of 1.2V.

The inductors have been designed to optimize the overall energy efficiency within a minimal footprint. These low-coupling inductors are composed of two stacked racetrack coils each of 3 turns with calculated dc resistance of 282 mΩ. The total footprint area is 1.25 $mm^2$. The fully-fabricated inductor and its cross-section are shown in Fig. 4(a) and Fig. 4(b).

## V. Characterisation of Coupled-Inductors

Presently, impedance analyzers are used to characterize the small-signal performance of the magnetic devices at high frequencies. This methodology only provides information on certain loss-factors that contribute to the device performance i.e. eddy current losses. However, in many cases, designers will wish to characterize the high frequency, in-circuit performance (in particular, the efficiency) of the integrated magnetics separately and in advance of having access to a high frequency integrated power converter circuit. In order to accurately measure the inductor performance in such a 'simulated power converter circuit' condition requires the application of operational voltage and current signals to the magnetics.

With these larger signals, core losses, such as hysteresis and excess eddy current losses, can also be measured. With certain magnetic materials, these losses can be more dominant than eddy currents, hence an accurate assessment of the overall device performance is critical prior to full power converter circuit implementation. In this work, we focus on the large-signal characterization of the devices for operation at 60MHz.

The high frequency measurement system for the characterization of the integrated inductor has been implemented in an optimized Printed Circuit Board (PCB) to reduce the effects of the parasitic elements. The measurement circuit is shown in Fig. 5. The details of the characterization set-up are described in previous work [8].

Fig. 6 shows the variation of self and magnetizing inductance with frequency from the large-signal characterization set-up with ac current amplitudes of both 20mA and 200mA. It can be seen that the inductance stays constant up to 70MHz after which the eddy current losses in the core dominate and inductance, both self and magnetizing, drop with frequency. Fig. 7 compares the resistance of the coupled inductor at different frequencies for the same ac current amplitudes of 20mA and 200mA.

Based on the large signal characterization of the coupled inductor devices, the overall efficiency was calculated to be 91.7% for a switching frequency of 60MHz and an output power of 0.5W.

## VI. Conclusions

This paper introduces the concept of integrated power management circuits based on magnetics on silicon using thin film magnetic cores. The authors believe that this technology platform is key to the microelectronics industry delivering the disruptive opportunity of PwrSoC. A case study describes the development of a two-phase coupled inductor switching at 60MHz. The coupled inductor has been characterized using large-signal characterization techniques. Based on the characterization data, the efficiency of the coupled inductor, for operation in a 60MHz converter, is calculated to be 91.7%.


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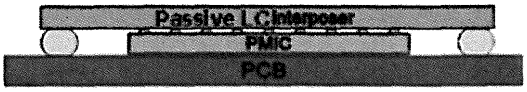



Figure 1: Integrated power converter incorprating a PMIC flip-chipped to a passive LC interposer. The assembly uses a mother-daughter chip scale package assembly to produce a 2.5D PwrSiP.

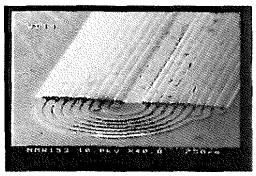


Figure 2(a): A thin-film inductor on silicon using a single layer racetrack of copper windings wrapped in a thin film magnetic core.

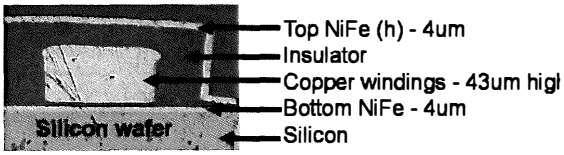



Figure 2(b): A cross-section of the single layer racetrack inductor.

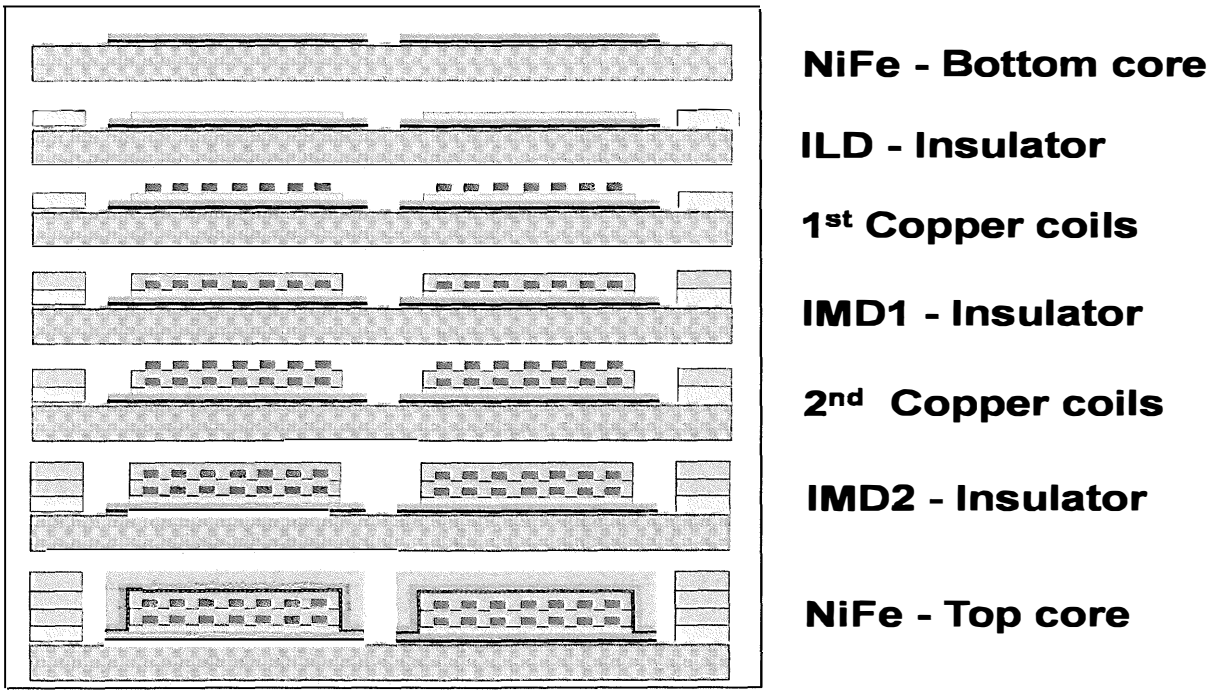



Figure 3: Process flow for the double layer metal (DLM) thin film inductor. ILD is inter-layer dielectric; IMD is inter-metal dielectric.

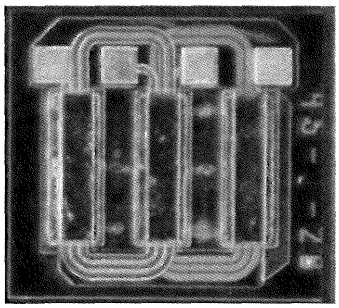


Figure 4(a): Plan-view of 2-phase, coupled racetrack inductor using thin-film magnetics. The bottom racetrack is on the left and the top racetrack is on the right. The stacked copper windings are in the centre.

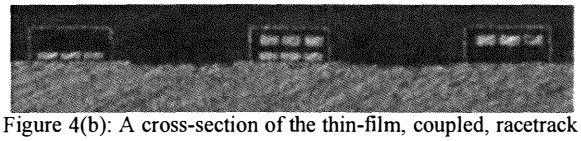


Figure 4(b): A cross-section of the thin-film, coupled, racetrack inductor on a silicon wafer using Double Layer Metal (DLM) windings. On the left are 3 copper windings of the bottom racetrack. In the centre is the combined bottom and top layer copper windings. On the right is the top layer copper winding of the top racetrack.

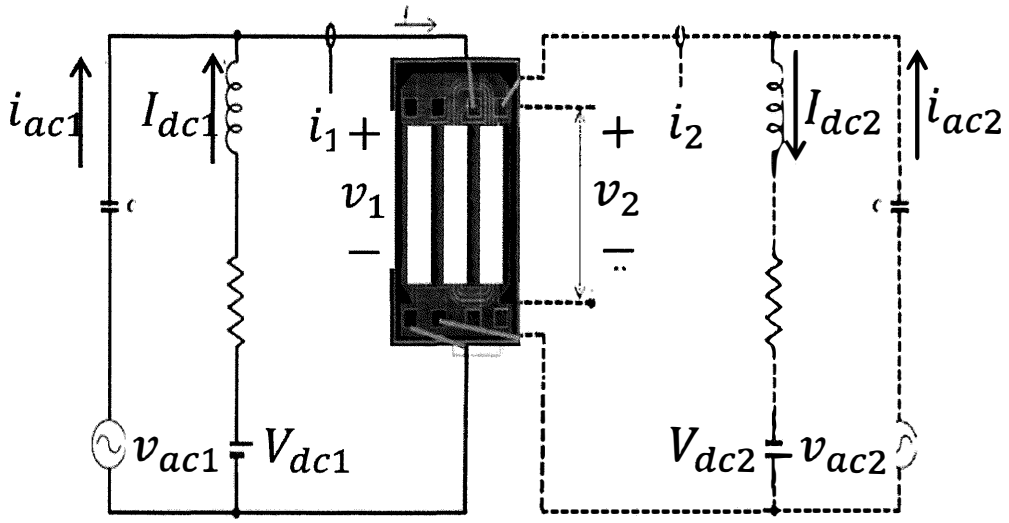



Figure 5: Measurement circuit for large signal testing of coupled inductor.

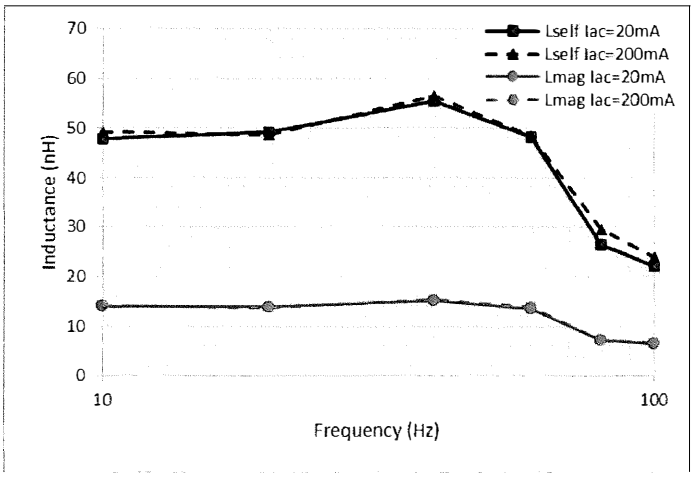



Fig. 6: The variation of self and magnetizing inductance with frequency from the large-signal characterization set-up with ac current amplitudes of both 20mA and 200mA.

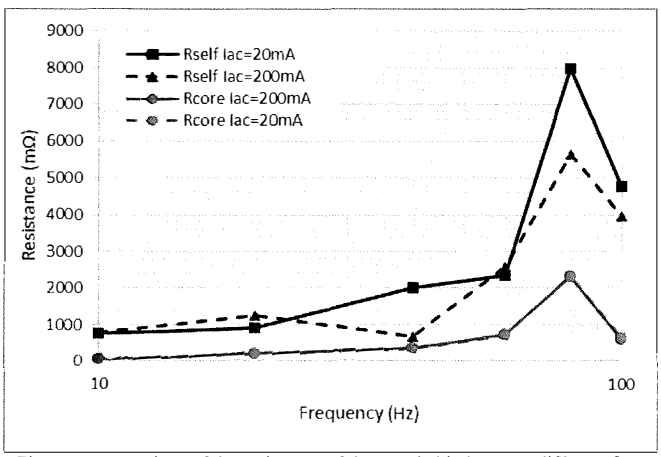



Fig. 7: A comparison of the resistance of the coupled inductor at different frequencies for ac current amplitudes of both 20mA and 200mA.